Construction Analysis

Lattice ispLSI2032-180L CPLD

Report Number: SCA 9712-573

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Lattice ispLSI 2032-180L Complex Programmable Logic Device (CPLD). One device packaged in a 44-pin Thin Quad-Flat-Pack (TQFP) was received for the analysis.

MAJOR FINDINGS

Questionable Items:[1]

- Excessive metal 2 and metal 1 aluminum thinning.

Special Features:

- Three types of EEPROM cells were used.

- Mature technology using thin tunnel-oxide windows.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Die Process and Design:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate. No epi was used.

- Final passivation: A layer of nitride over a layer of glass (no die coat was present).

- Metallization: Two levels of metal interconnect were used. Both metal 2 and metal 1 consisted of aluminum with a thin titanium-nitride (TiN) cap and barrier. Standard vias and contacts were employed (no plugs).

- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of two layers of glass, with a spin-on-glass (SOG) between to provide planarization.

- Pre-metal dielectric: Consisted of a single layer of reflow glass (probably BPSG) over various densified oxides.

- Polysilicon: A single layer of dry-etched polycide (poly and tungsten silicide) was used. This layer formed all gates on the die, and in the cell array it formed the capacitors, word lines, and tunnel oxide device. Oxide sidewall spacers were used on all gates, and left in place.

- Diffusion: Standard implanted N+ and P+ diffusions formed the sources/drains of the MOS transistors.

- Wells: Twin-wells in an N substrate. A shallow N-well was located under the P-channel devices. N-channel devices were located within the P-wells. A step was noted in the local oxide at the edges of the well boundaries.

TECHNOLOGY DESCRIPTION (continued)

- The memory cell consisted of a standard EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, capacitors, and the tunnel oxide devices.

- Redundancy fuses were not present.

ANALYSIS RESULTS

Die Process: **Figures 1 - 43**

Questionable Items:[1]

- Excessive metal 2 and metal 1 aluminum thinning.

Special Features:

- Three types of EEPROM cells were used.
- Mature technology using thin tunnel-oxide windows.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-well in a N substrate (no epi was used). No problems were found in this process.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Final passivation: A layer of nitride over a layer of glass. An integrity test indicated defect-free passivation. Edge seal was good.
- Metallization: Both metal 2 and metal 1 consisted of aluminum with a thin titanium-nitride (TiN) cap and barrier defined by dry-etch techniques. Standard vias and contacts were used (no plugs).

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS (continued)

- Metal patterning: The metal layers were patterned by a dry etch of normal quality. Contacts were completely surrounded by metal and metal lines were widened at contacts.

- Metal defects: No voiding, notching, or neckdown was noted in either metal layer.

- Metal step coverage: Metal 2 aluminum thinned up to 100 percent at vias. It was reduced to 95 percent with the addition of the cap and barrier. Metal 1 aluminum thinned up to 100 percent at the contacts. This thinning was reduced to 95 percent with the addition of the cap and barrier. This thinning appears to be excessive and not under good control.

- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of two layers of glass with a spin-on-glass between for planarization. No problems were found with these layers.

- Pre-metal dielectric: Consisted of a single layer of reflow glass (probably BPSG) over a densified oxide. The glass was reflowed before contact cuts only. No problems were found.

- Vias and contacts: Via and contact cuts appeared to be defined by a two-step dry etch. No over-etching or other contact problems were found.

- Polysilicon: A single layer of polycide (poly and tungsten silicide) was used to form all the gates on the die. In the cell, poly formed the word/select lines, capacitors, and the tunnel oxide device. Oxide sidewall spacers were used on all gates and left in place.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the MOS transistors. Diffusions were not silicided. No problems were noted.

ANALYSIS RESULTS (continued)

- Isolation: Local oxide (LOCOS) isolation was used. A step was present in the oxide at the well boundaries.

- EEPROM arrays: Three types of EEPROM memory cells were used. Metal was used to form the bit lines. Poly formed the word/select lines, capacitors, and the tunnel oxide device. Smallest cell pitch was 8.95 x 13.5 microns.

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection

SEM inspection of passivation

Passivation integrity test

Delayer to metal 2 and inspect

Aluminum removal (metal 2)

Delayer to metal 1 and inspect

Delayer to poly/substrate and inspect

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP (thinning)
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIAL ANALYSIS

Final passivation:	A layer of nitride over a layer of silicon-dioxide.
Metallization 2:	Aluminum with a thin titanium-nitride (TiN) cap and barrier. An apparent titanium (Ti) adhesion layer under the barrier metal.
Interlevel dielectric:	Two layers of silicon-dioxide.
Metallization 1:	Aluminum with a thin titanium-nitride (TiN) cap and barrier. An apparent titanium (Ti) adhesion layer under the barrier metal.
Pre-metal dielectric:	A single layer of BPSG reflow glass over a densified oxide.
Poly:	Tungsten (W) silicide.

HORIZONTAL DIMENSIONS

Die size:	2.1 x 4.5 mm (84 x 175 mils)
Die area:	9.5 mm^2 (14,700 $mils^2$)
Min pad size:	0.1 x 0.1 mm (4.1 x 4.1 mils)
Min pad window:	0.08 x 0.08 mm (3.4 x 3.4 mils)
Min pad space:	0.05 mm (2.2 mils)
Min metal 2 width:	1.1 micron
Min metal 2 space:	1.3 micron
Min metal 2 pitch - (uncontacted):	2.2 microns
- (contacted):	2.6 microns
Min via:	1.0 micron
Min metal 1 width:	0.8 micron
Min metal 1 space:	1.0 micron
Min metal 1 pitch - (uncontacted):	1.85 microns
- (contacted):	2.3 microns
Min contact:	1.0 micron
Min poly width - (cell):	0.65 micron
Min poly width - (periphery):	0.5 micron
Min poly space:	0.9 micron
Min gate length[1] - (N-channel):	0.5 micron
- (P-channel):	0.65 micron
Cell area[2] (smallest):	120.8 $microns^2$
Cell size[2] (smallest):	8.95 x 13.5 microns

[1] *Physical gate length.*
[2] *Cell shown in Figures 22 - 31.*

VERTICAL DIMENSIONS

Die thickness:	0.3 mm (13 mils)

Layers

Passivation 2:	0.45 micron
Passivation 1:	0.27 micron
Metal 2 - cap:	0.04 micron
- aluminum:	0.74 micron
- barrier:	0.11 micron
Interlevel dielectric 1 - glass 2:	0.48 micron
- SOG:	0 - 1.2 microns
- glass 1:	0.17 micron
Metal 1 - cap:	0.07 micron
- aluminum:	0.47 micron
- barrier:	0.11 micron
Reflow glass:	0.3 - 0.75 micron
Poly - silicide:	0.15 micron
- poly:	0.12 micron
Local oxide:	0.48 micron
N+ S/D diffusion:	0.25 micron
P+ S/D diffusion:	0.25 micron
N-well:	1.0 micron
P-well:	3.5 microns

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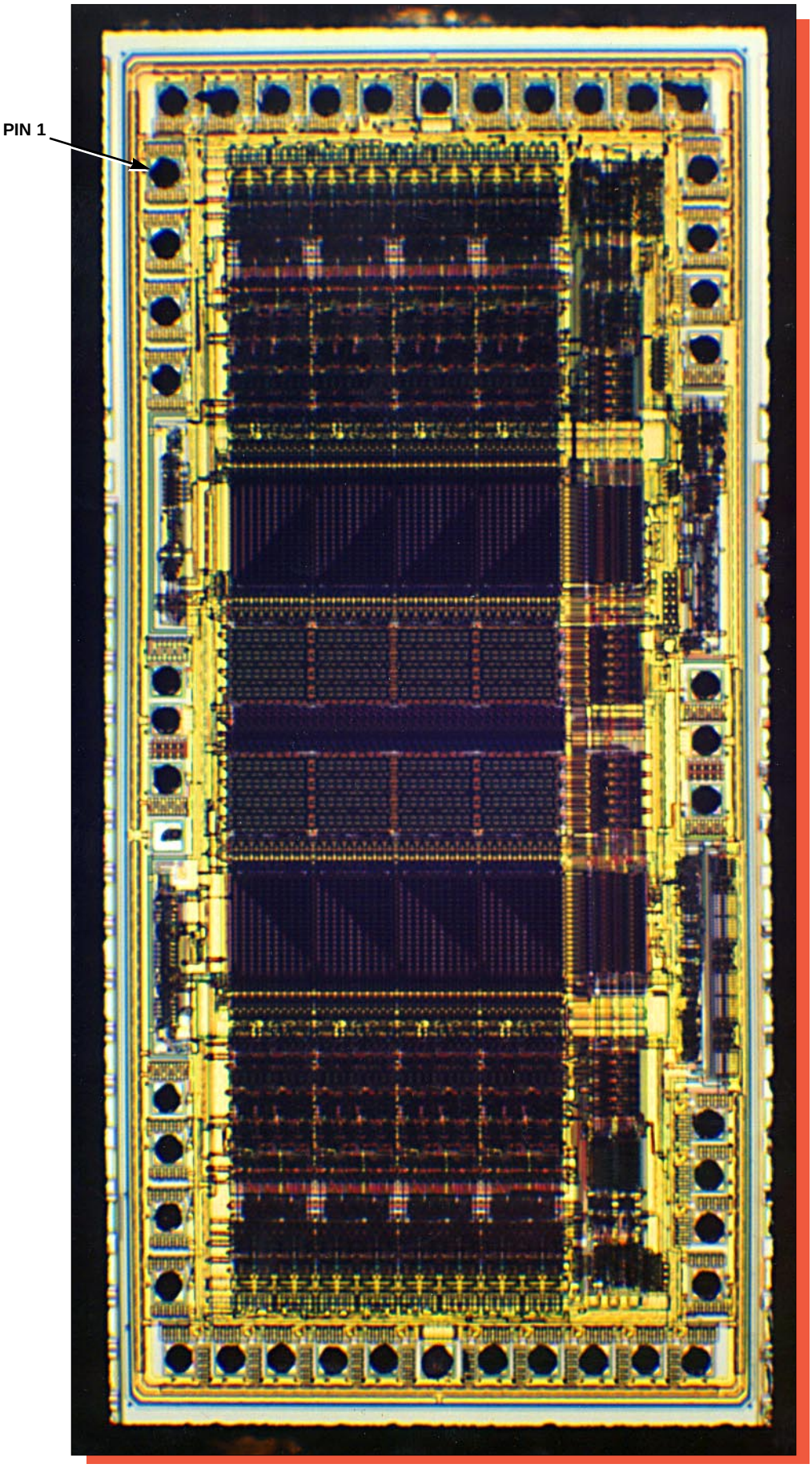
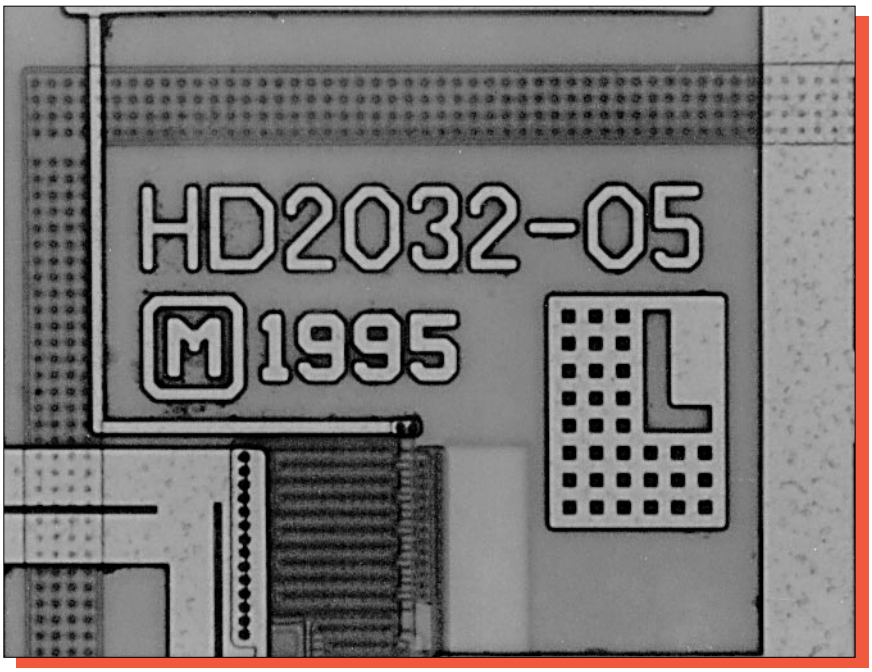


Figure 1. Whole die photograph of the Lattice ispLSI 2032-180L CPLD. Mag. 50x.



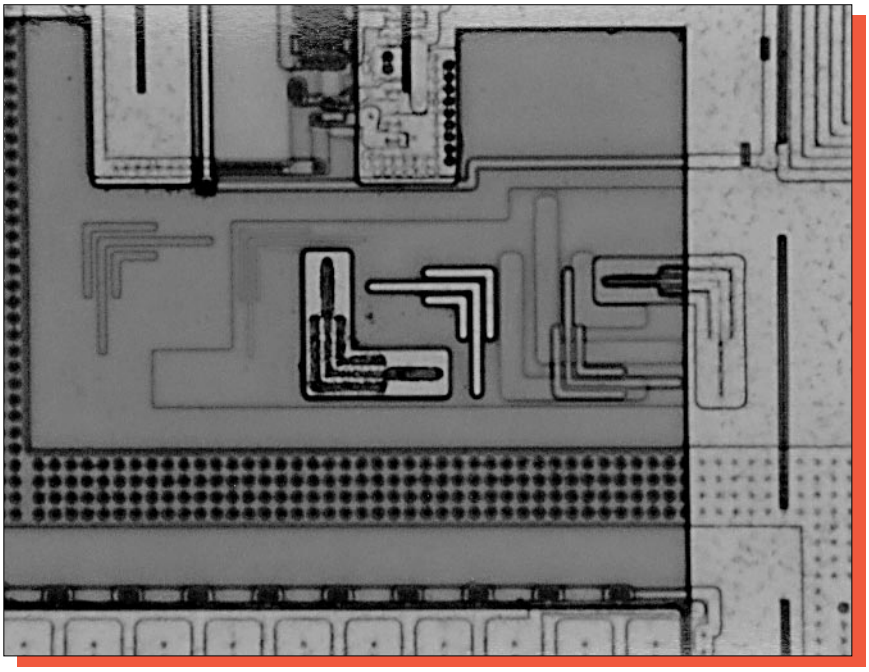
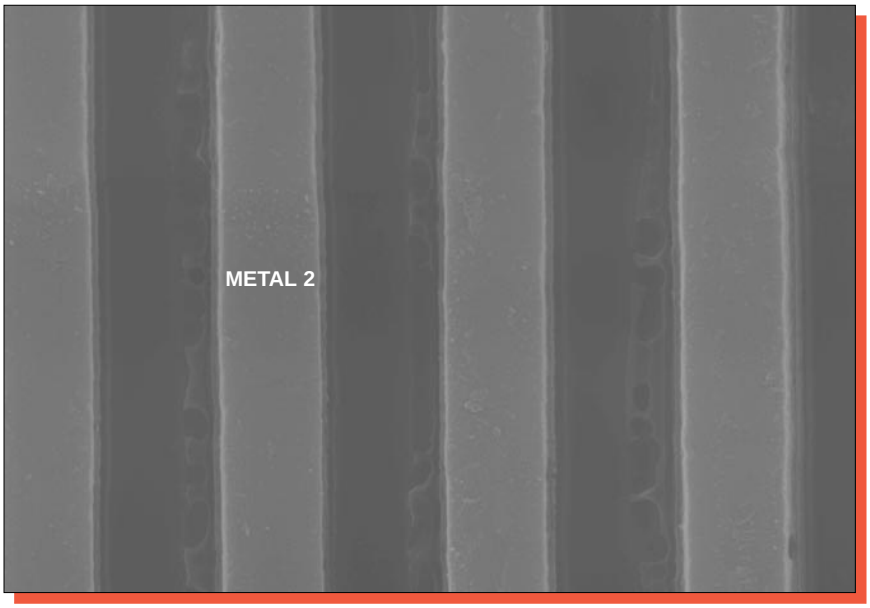
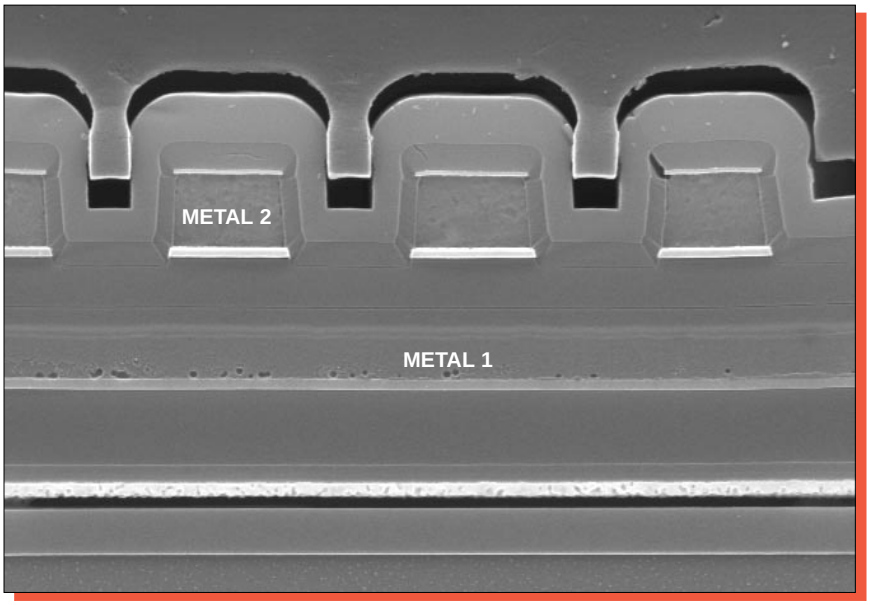


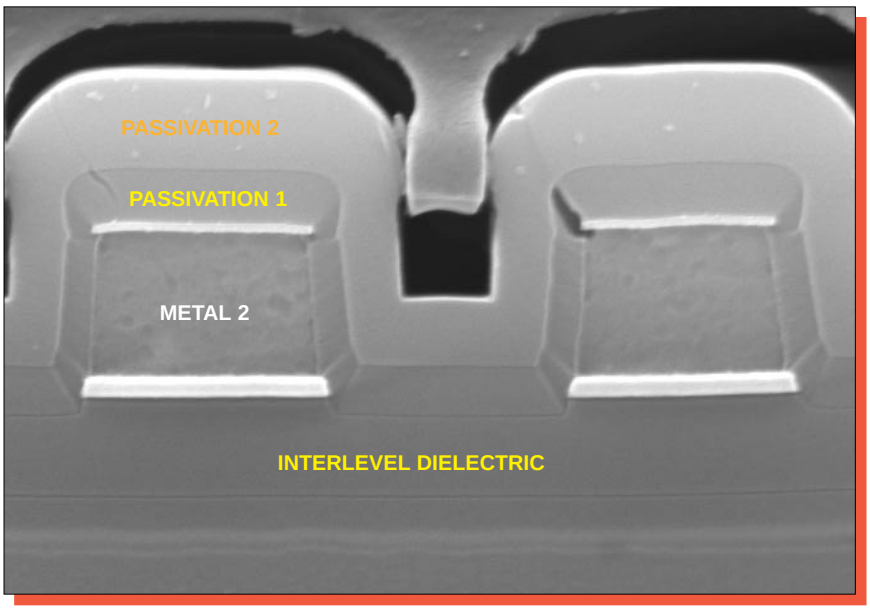
Figure 2. Optical views of the die markings from the surface. Mag. 800x.



Photograph #8,
Mag. 13,000x

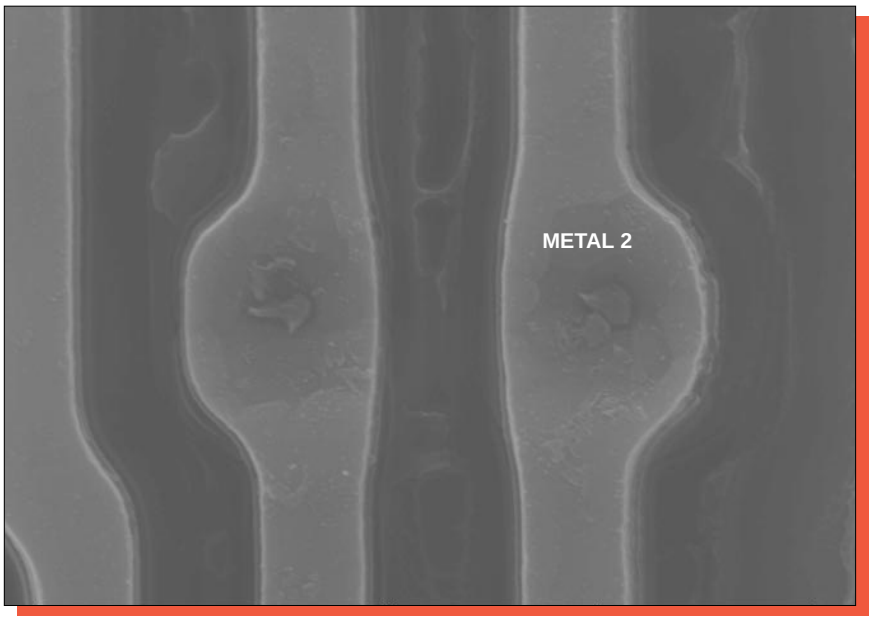


Photograph #9,
Mag. 13,000x

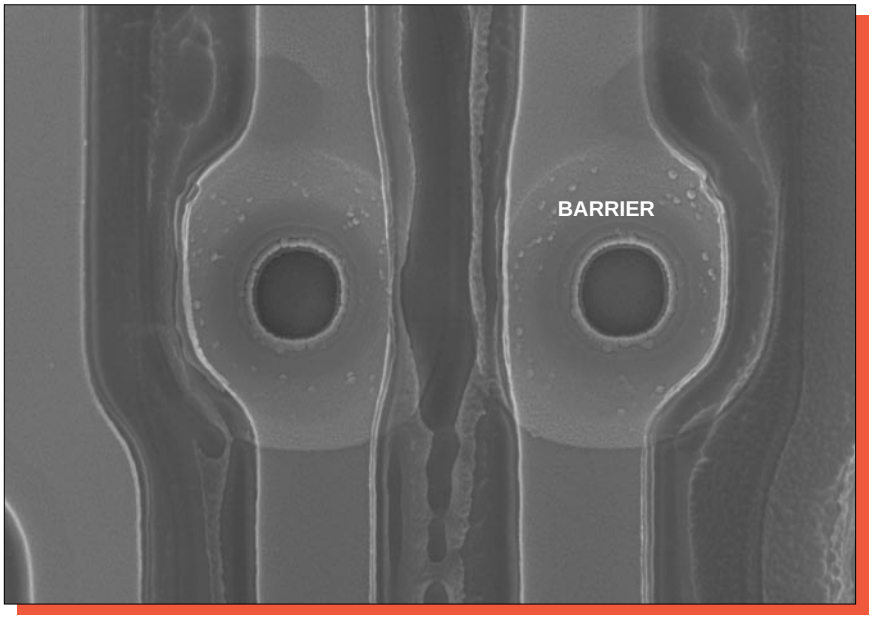


Photograph #9,
Mag. 26,000x

Figure 3. SEM views illustrating design rules 9 and 10.

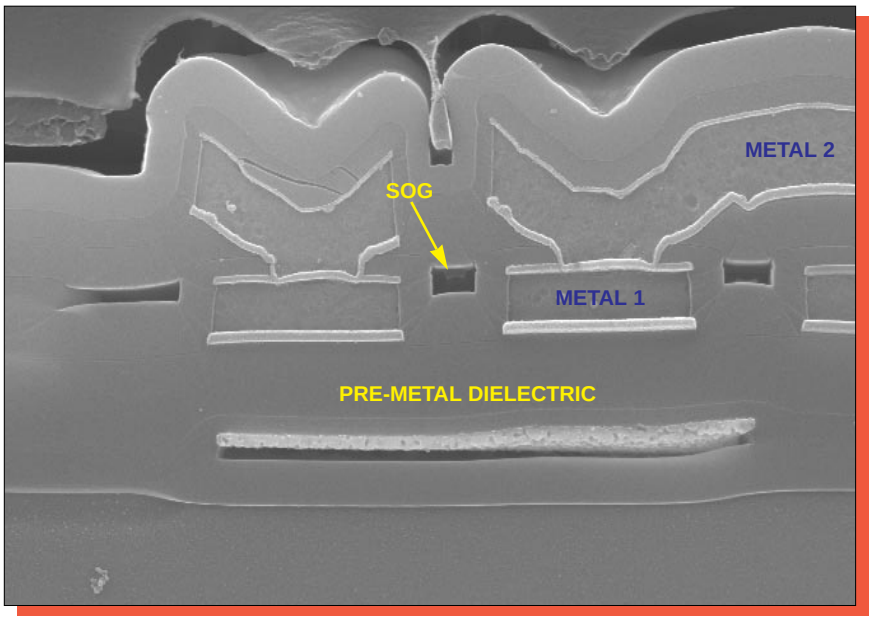


Photograph #10, type C,
aluminum intact

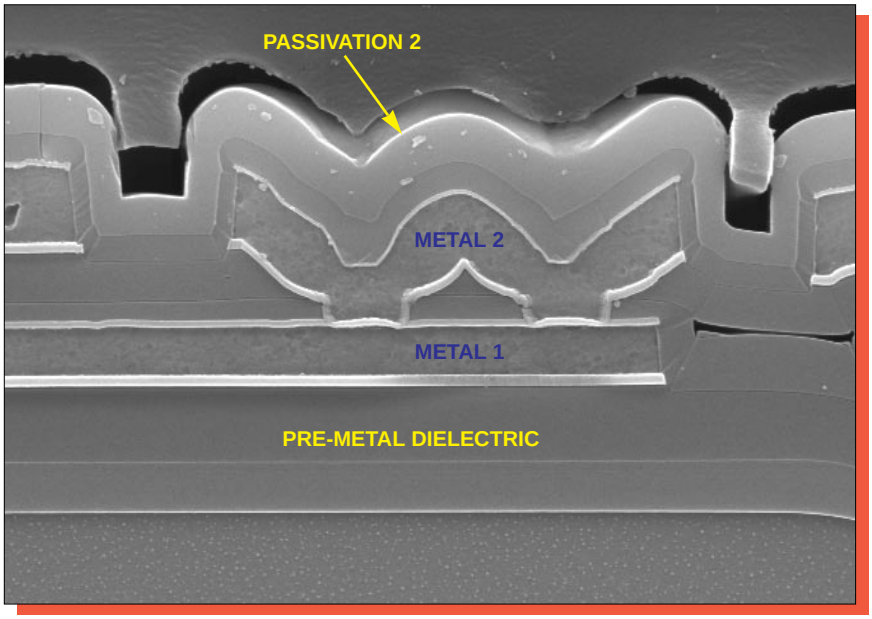


Photograph #10, type C,
aluminum removed

Figure 4. SEM views illustrating design rule 11. Mag. 13,000x.

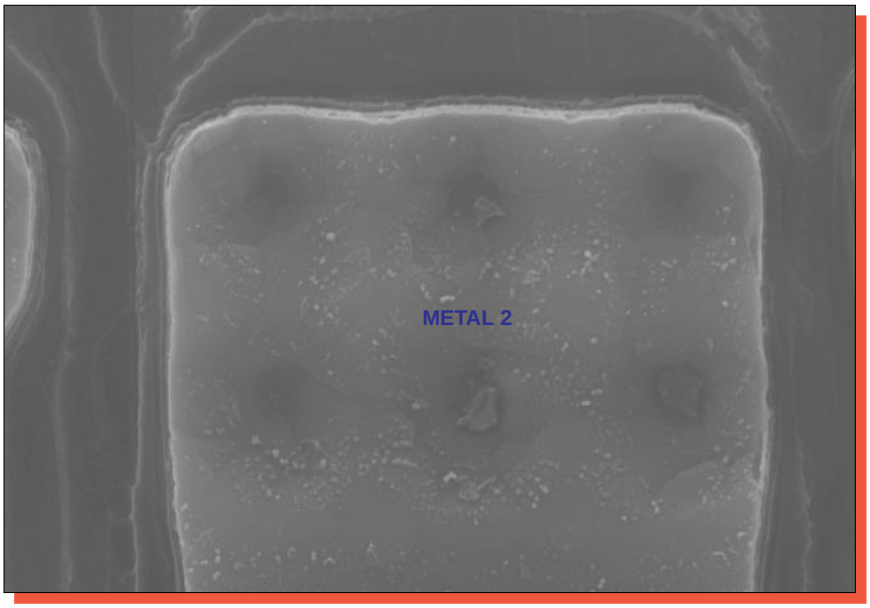


Photograph #11

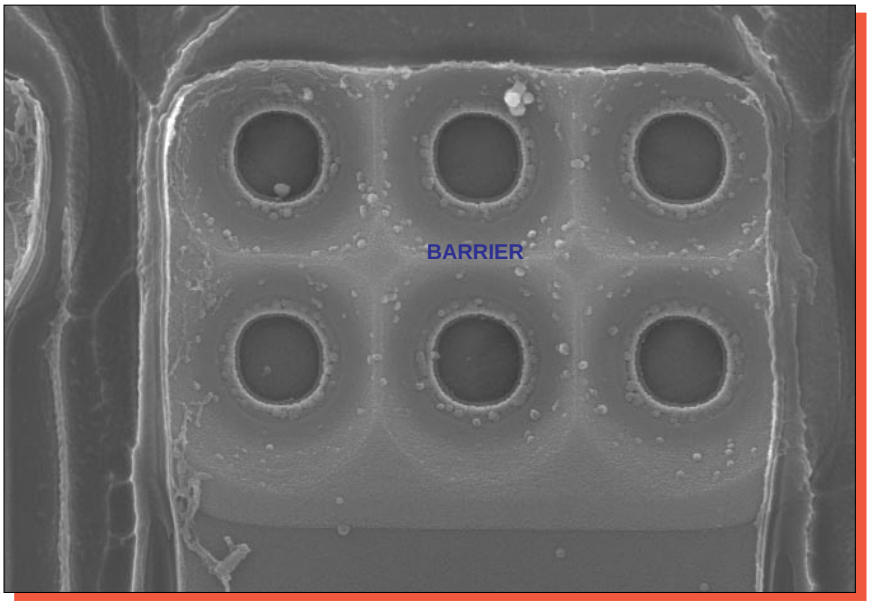


Photograph #12

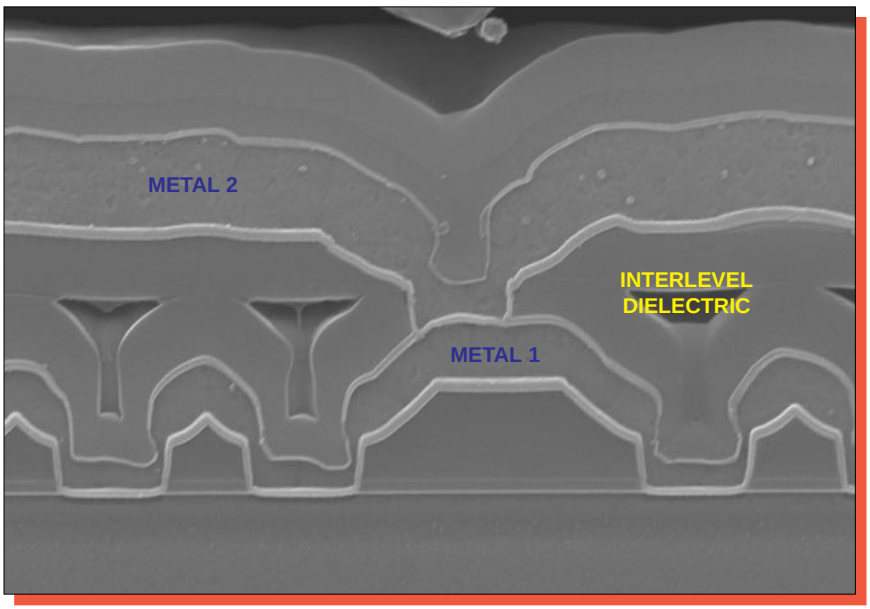
Figure 5. SEM views illustrating design rules 12, 13, and 14. Mag. 13,000x.



Photograph #13,
aluminum intact,
Mag. 13,000x

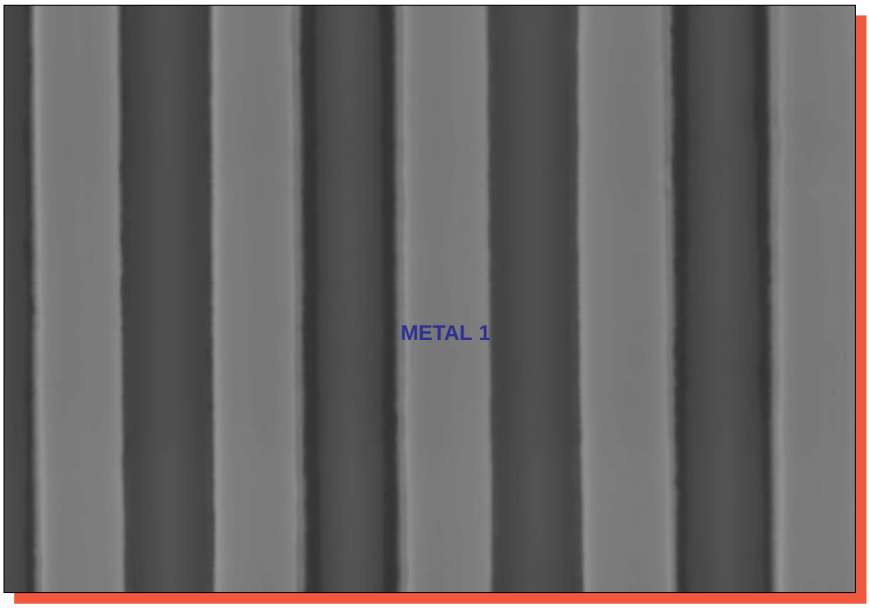


Photograph #13,
aluminum removed,
Mag. 13,000x



Photograph #14,
Mag. 15,000x

Figure 6. SEM views illustrating design rules 15 and 16.



Photograph #15,
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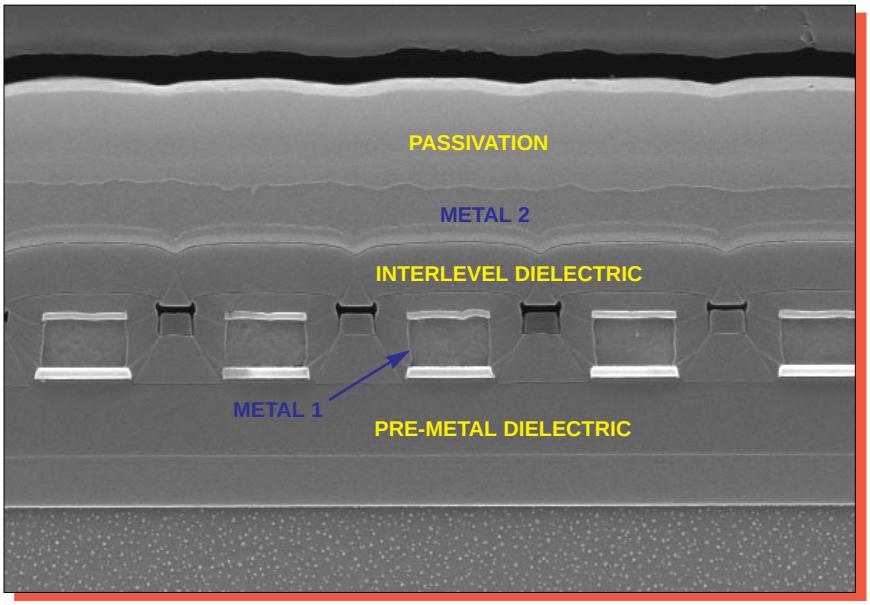
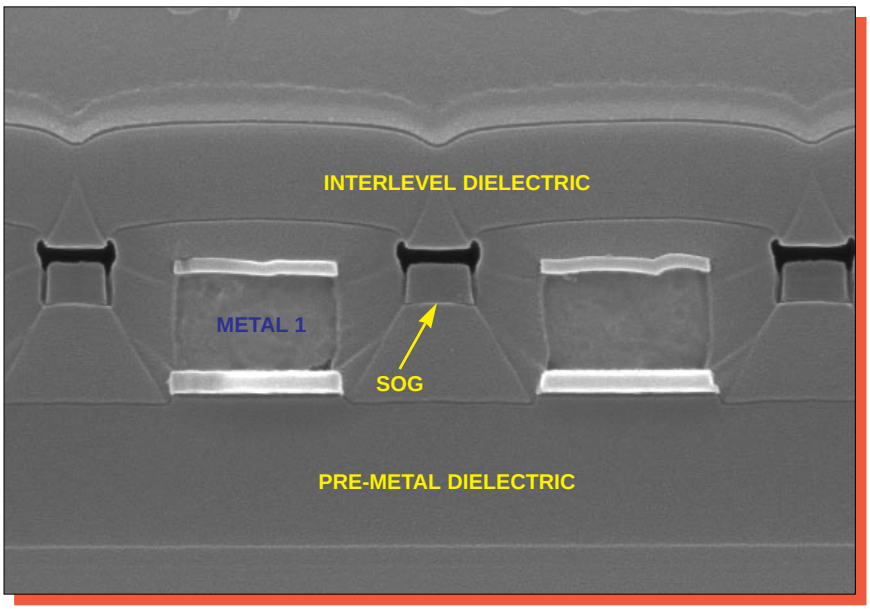
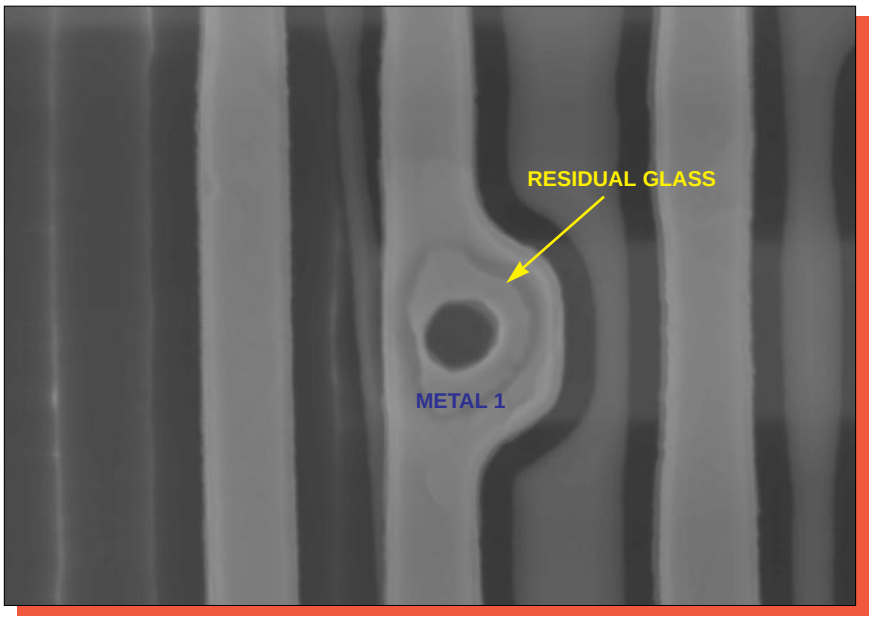


Photograph #16,
Mag. 13,000x

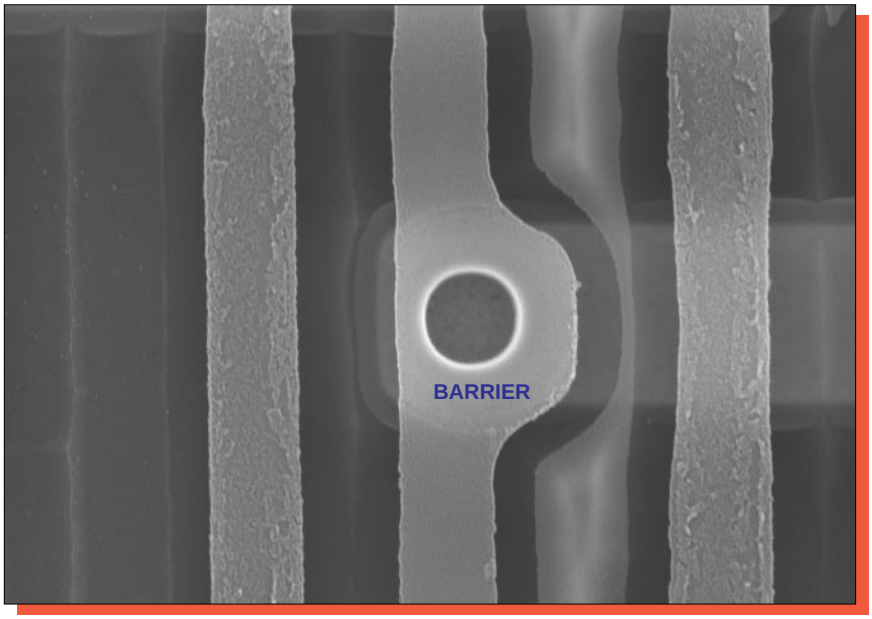


Photograph #16,
Mag. 26,000x

Figure 7. SEM views illustrating design rules 17 and 18.

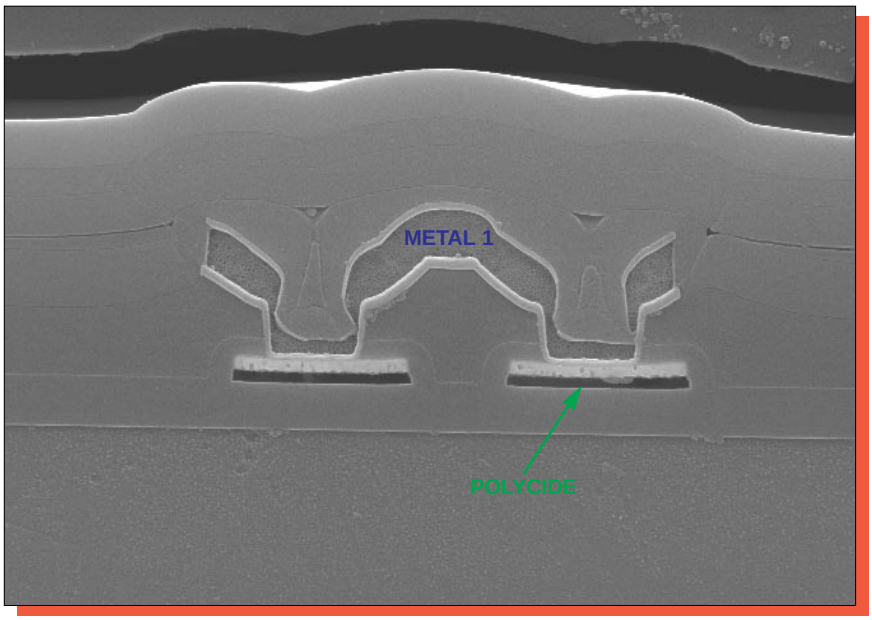


Photograph #17, Type B,
aluminum intact

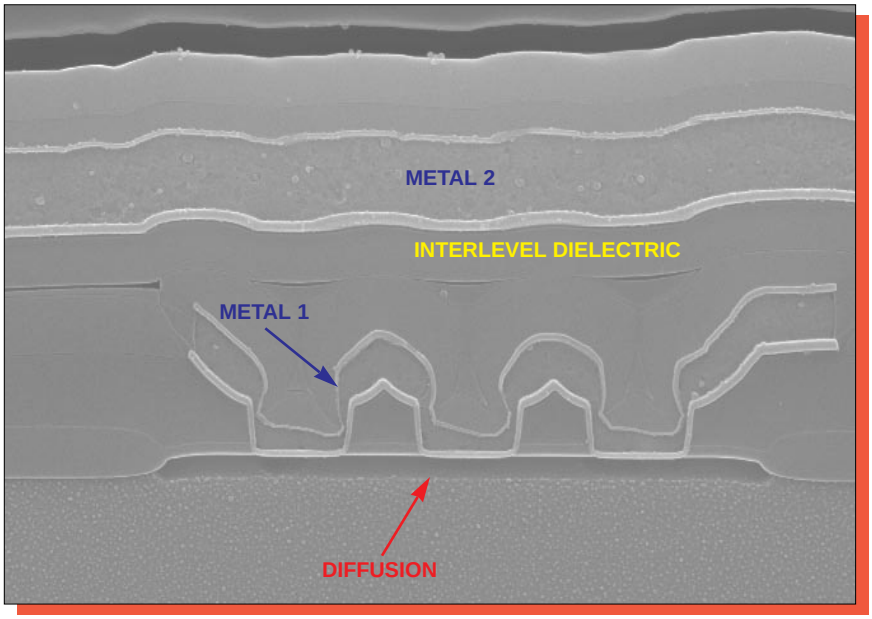


Photograph #17, Type B,
aluminum removed

Figure 8. SEM views illustrating design rule 19. Mag. 13,000x.

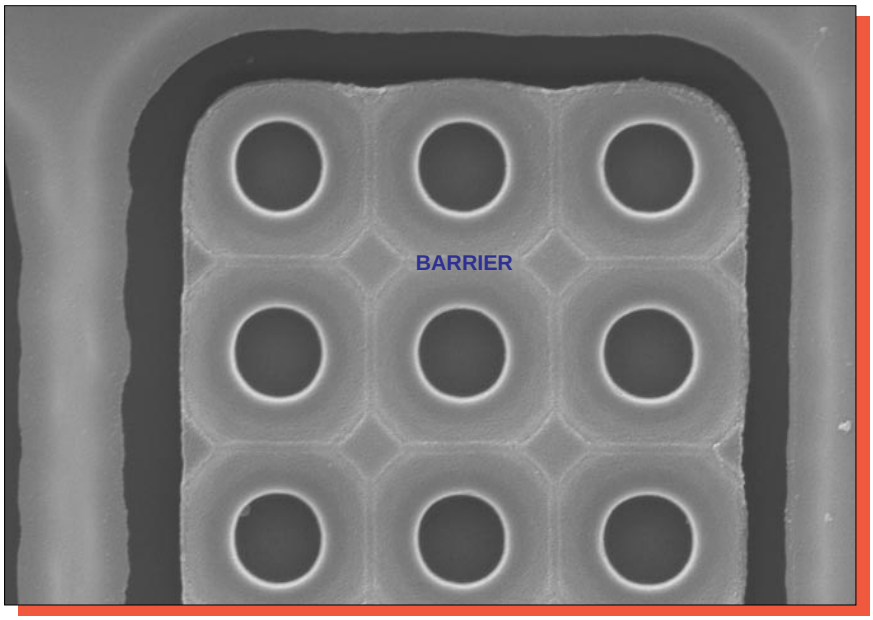


Photograph #18



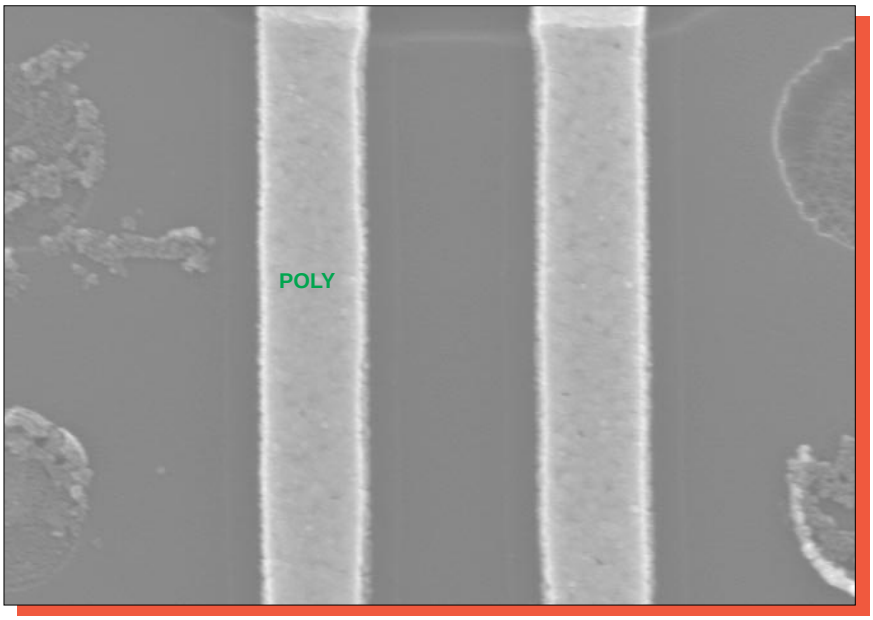
Photograph #19

Figure 9. SEM views illustrating design rules 20, 21, and 22. Mag. 13,000x.



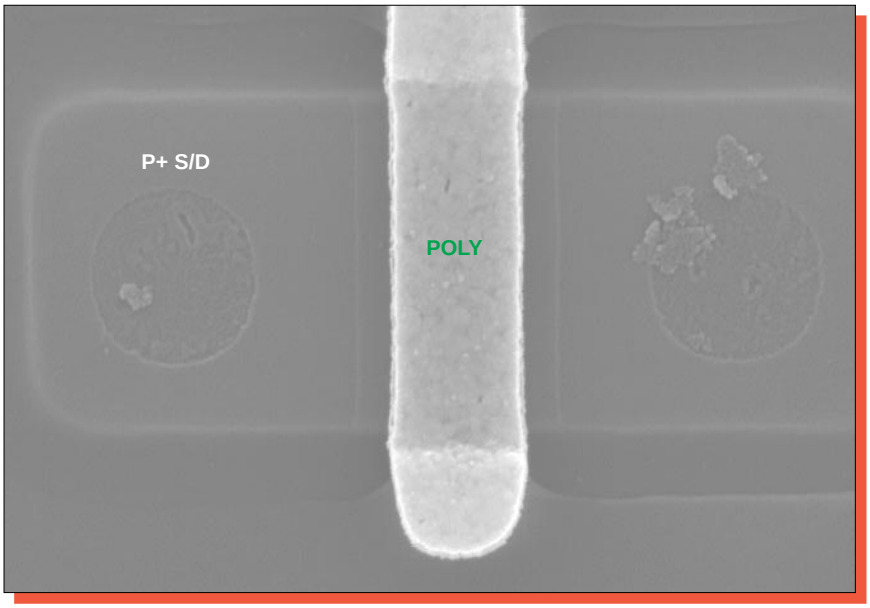
Photograph #20, aluminum removed

Figure 10. SEM view illustrating design rule 23. Mag. 13,000x.

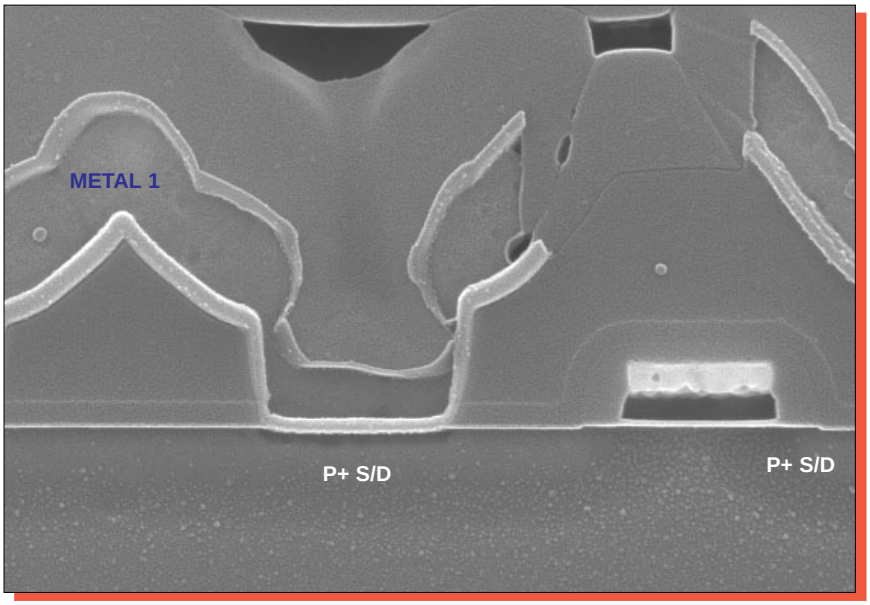


Photograph #22

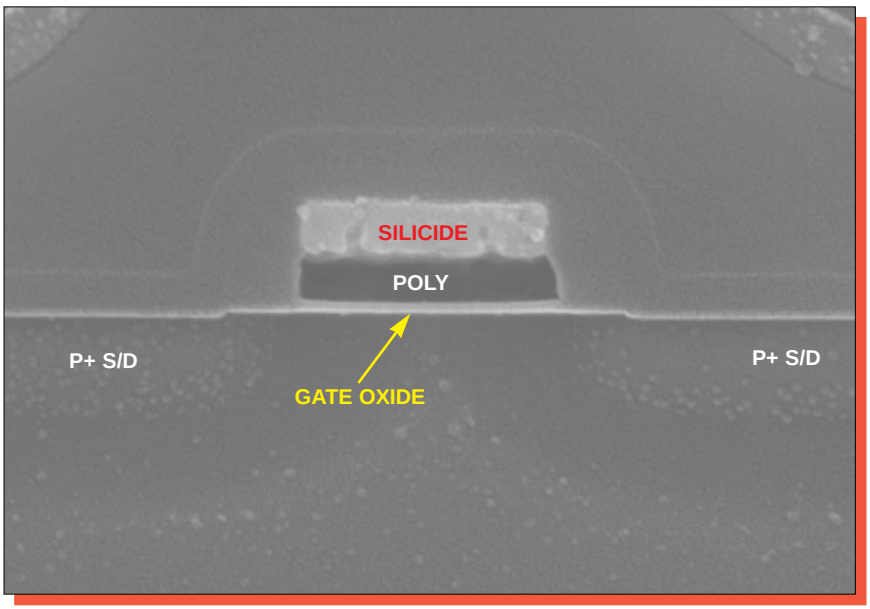
Figure 11. SEM view illustrating design rules 25 and 26. Mag. 26,000x.



Photograph #23,
Mag. 26,000x

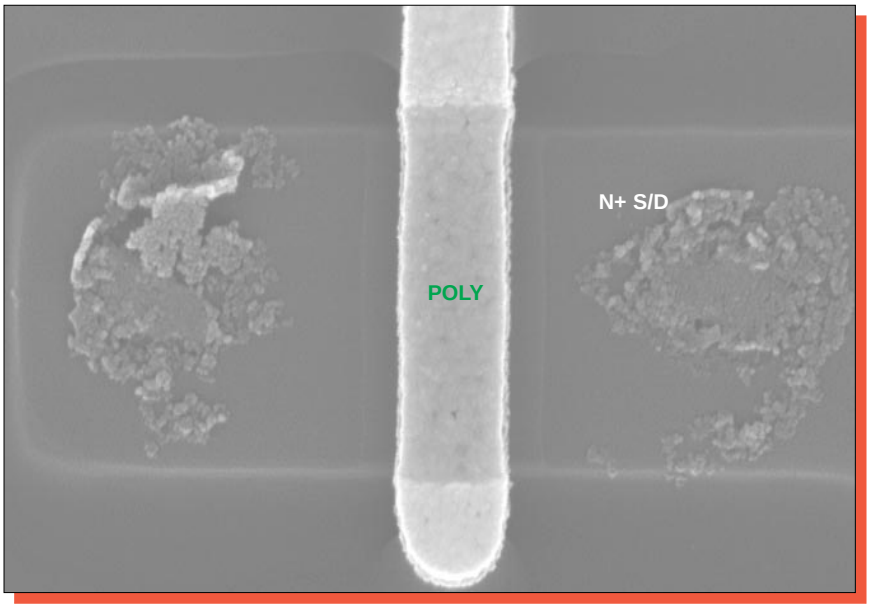


Photograph #25,
Mag. 30,000x

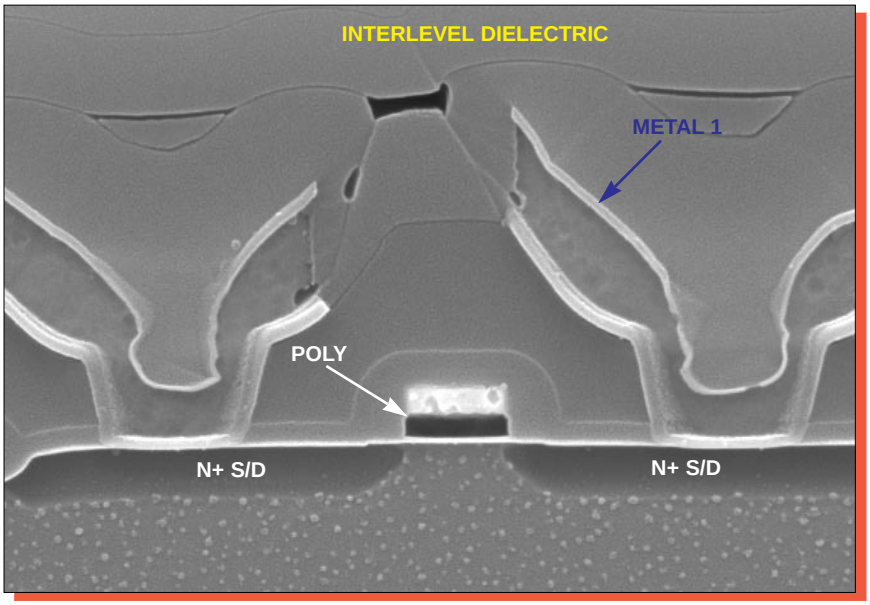


Photograph #25,
Mag. 52,000x

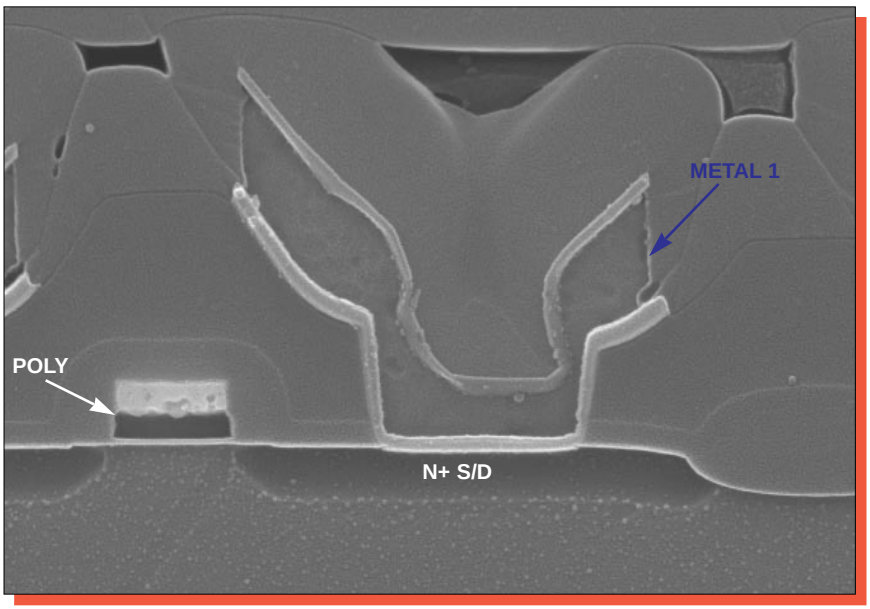
Figure 12. SEM views illustrating design rules 27 and 28.



Photograph #24,
Mag. 26,000x

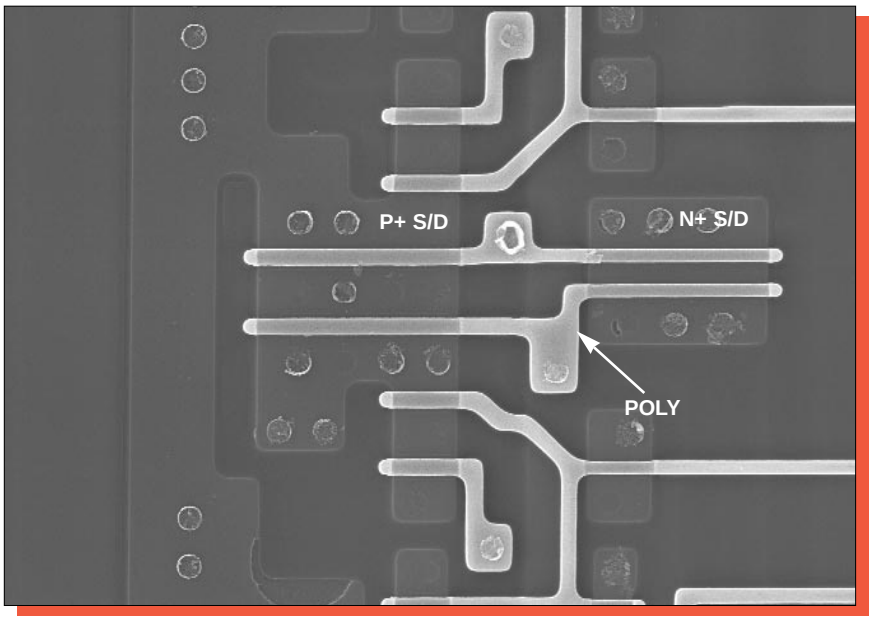


Photograph #26,
Mag. 26,000x

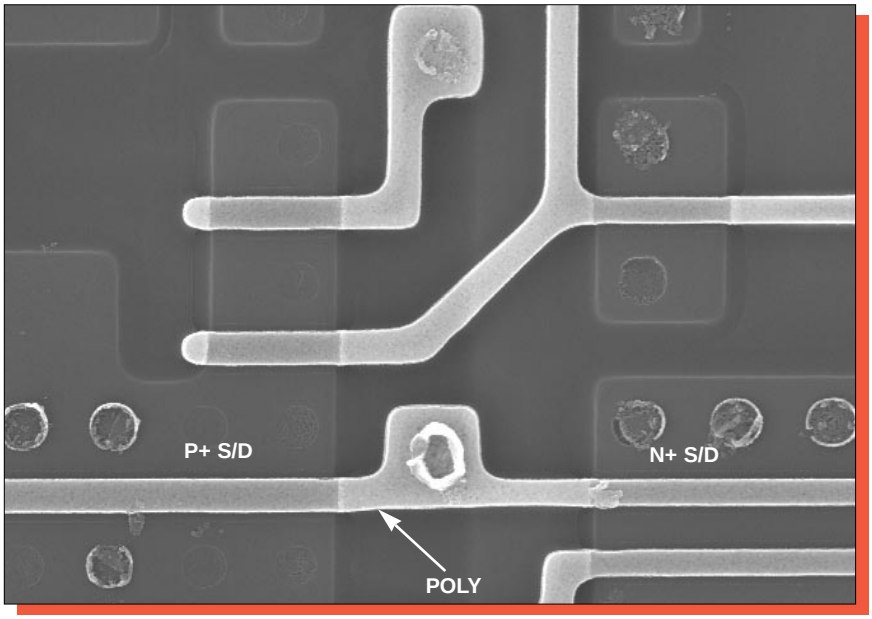


Photograph #26,
Mag. 30,000x

Figure 13. SEM views illustrating design rules 27 and 29.



Photograph #27, Mag. 3250x



Photograph #27, Mag. 6500x

Figure 14. SEM views illustrating design rule 30.

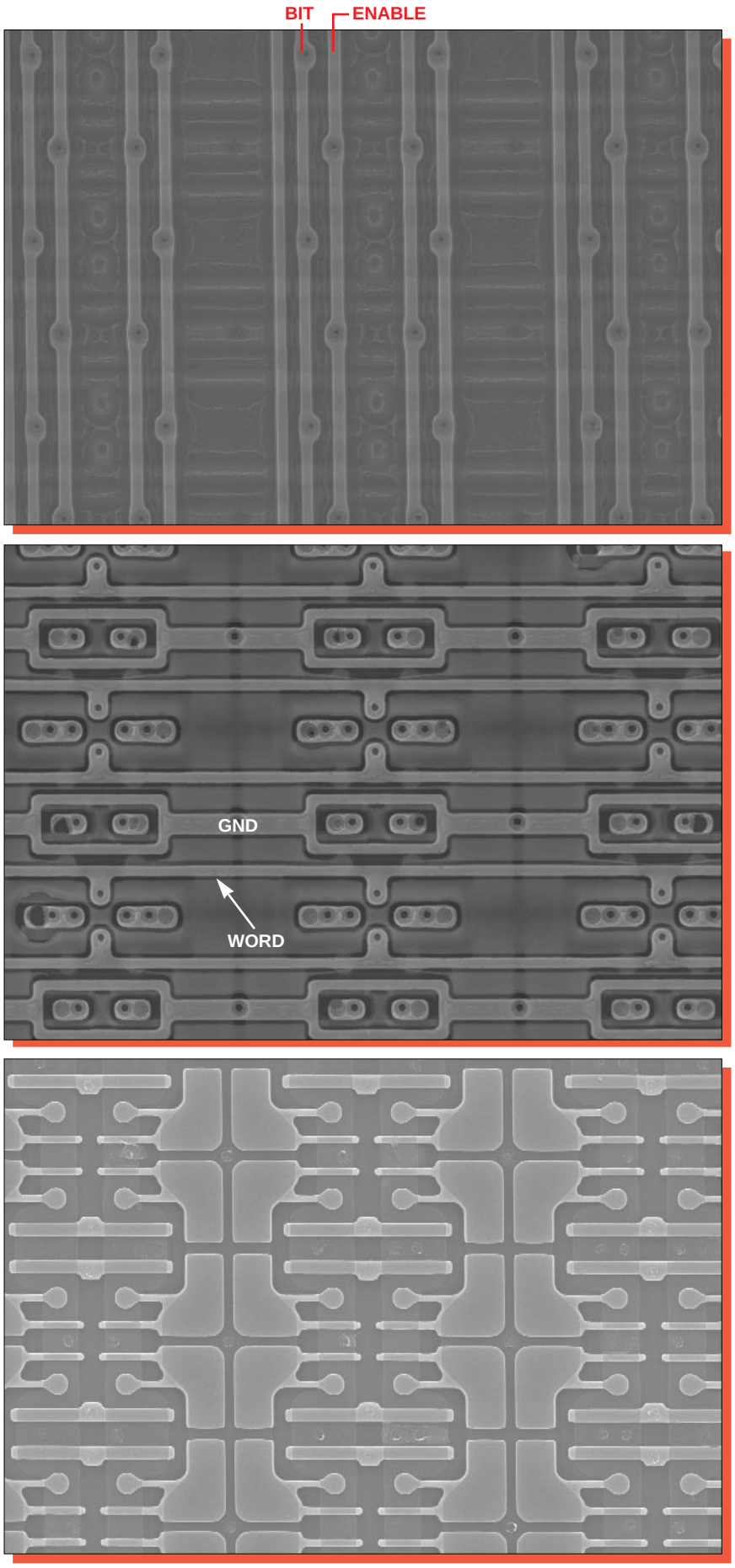
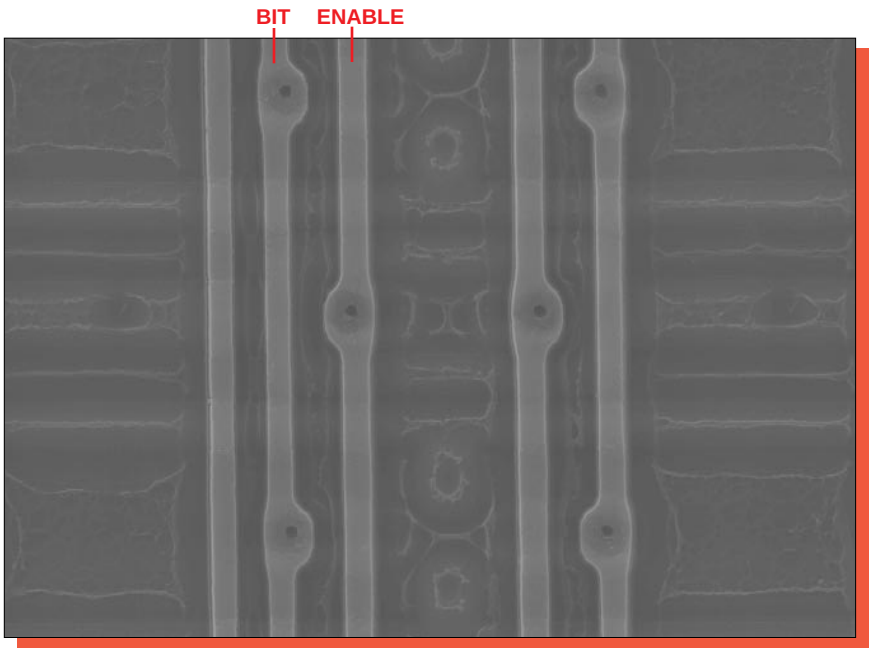
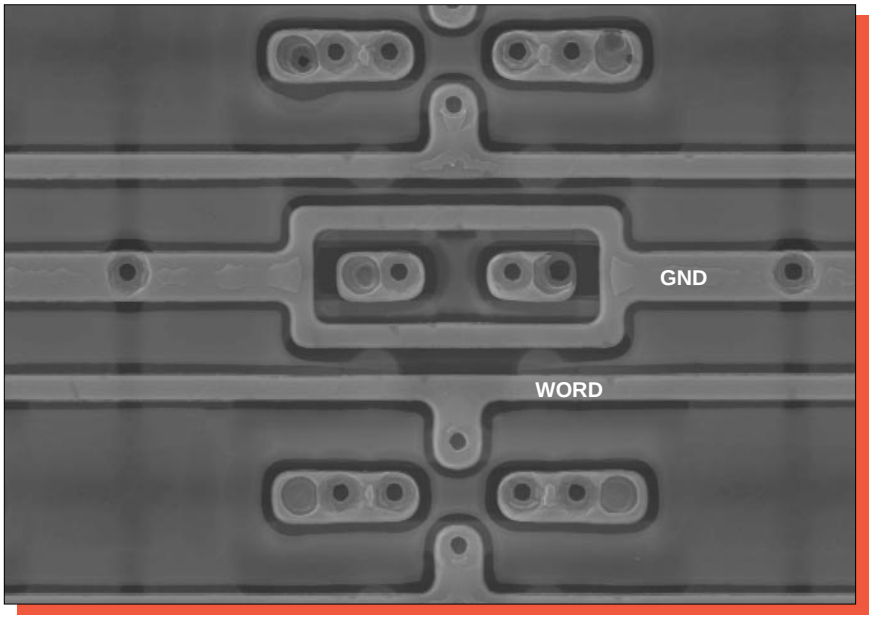


Figure 15. Topological SEM views of the EEPROM cell. Mag. 1625x, 0°.

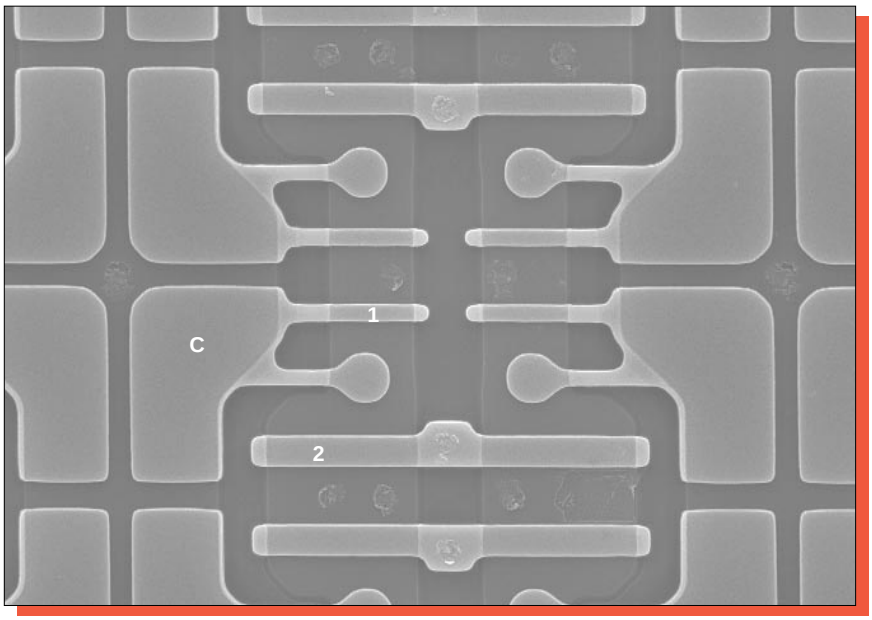


metal 2



metal 1

Figure 16. Topological SEM views of the EEPROM cell. Mag. 3250x, 0°.



poly

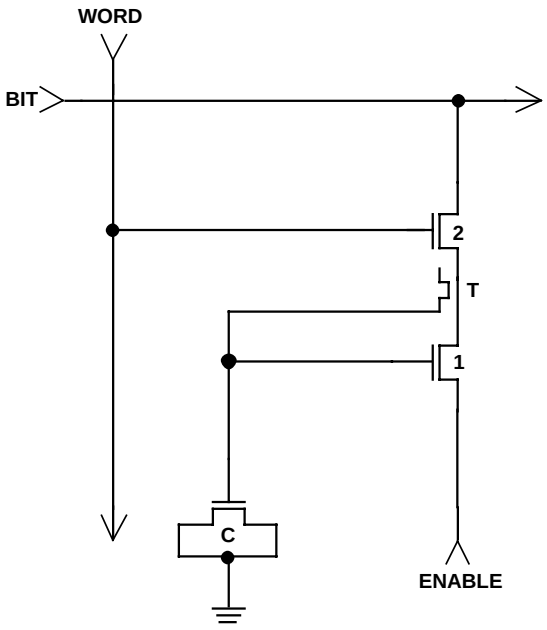


Figure 17. Topological view and schematic of the EEPROM cell. Mag. 3250x, 0°.

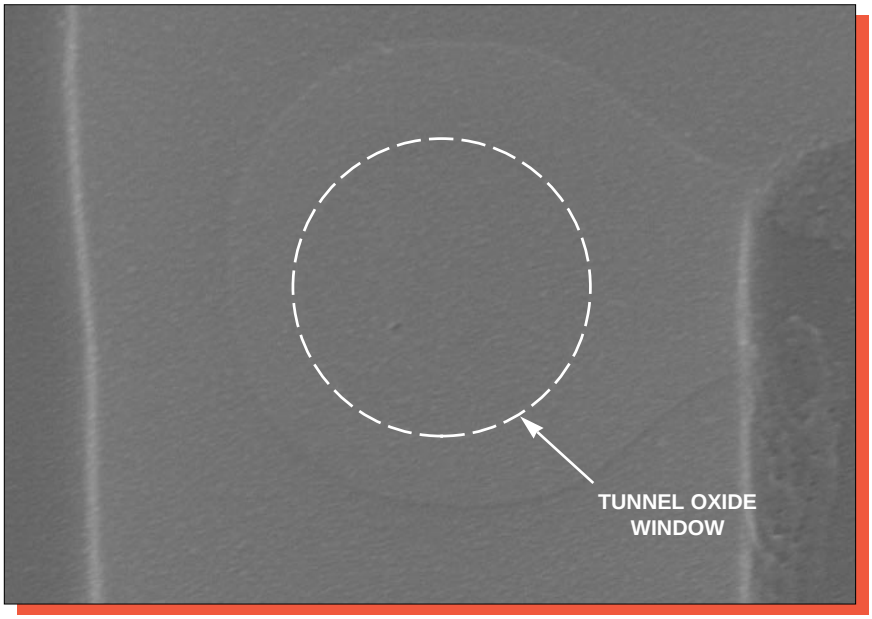
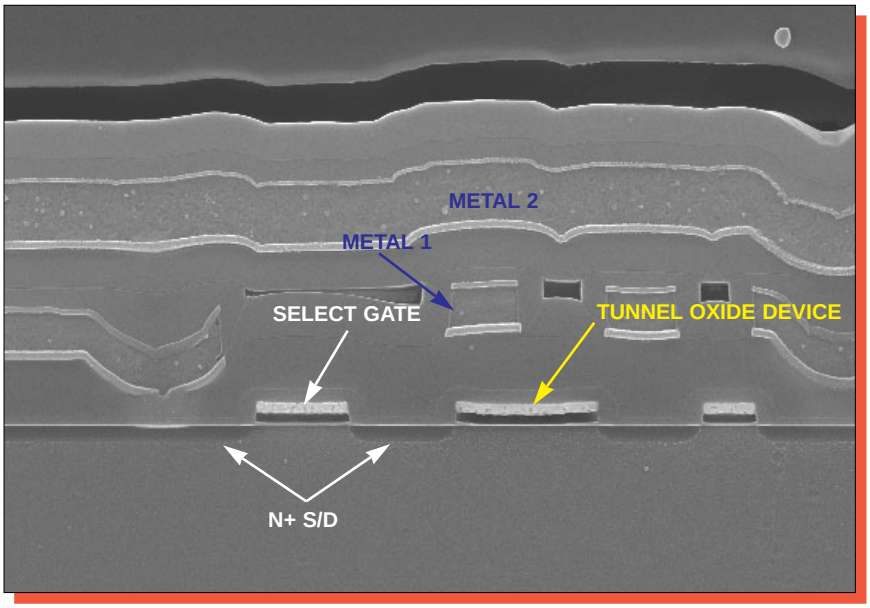
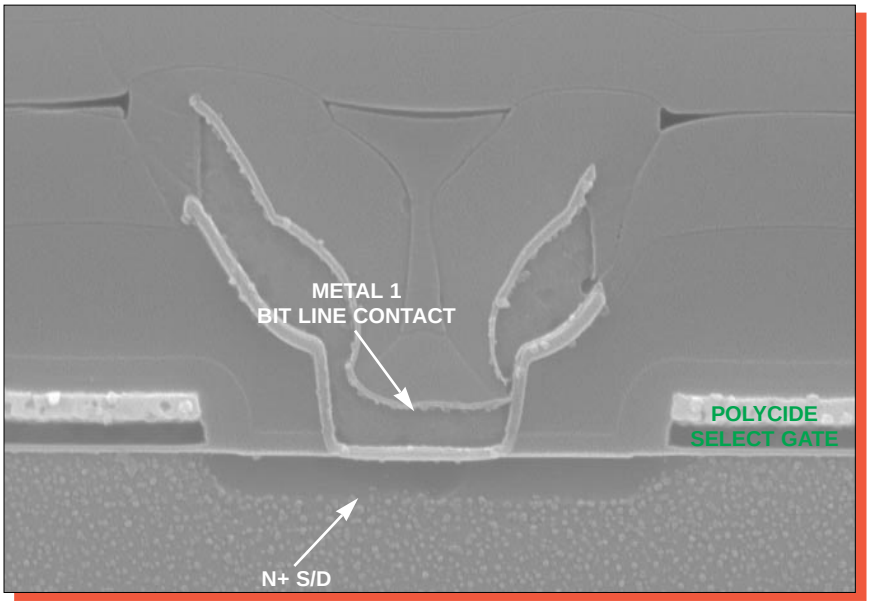


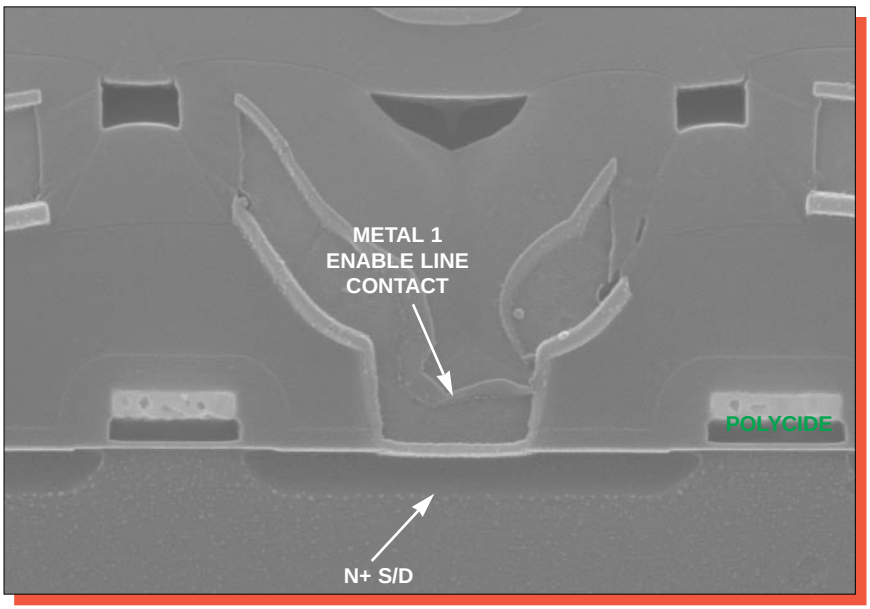
Figure 18. Topological SEM view of the tunnel oxide window. Mag. 26,000x, 0°.



Mag. 10,000x

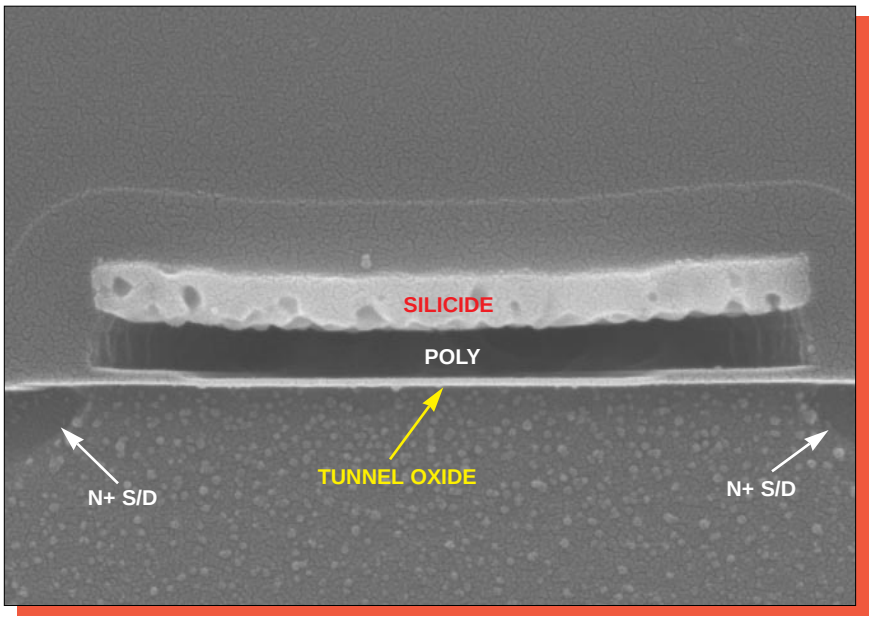


Mag. 26,000x

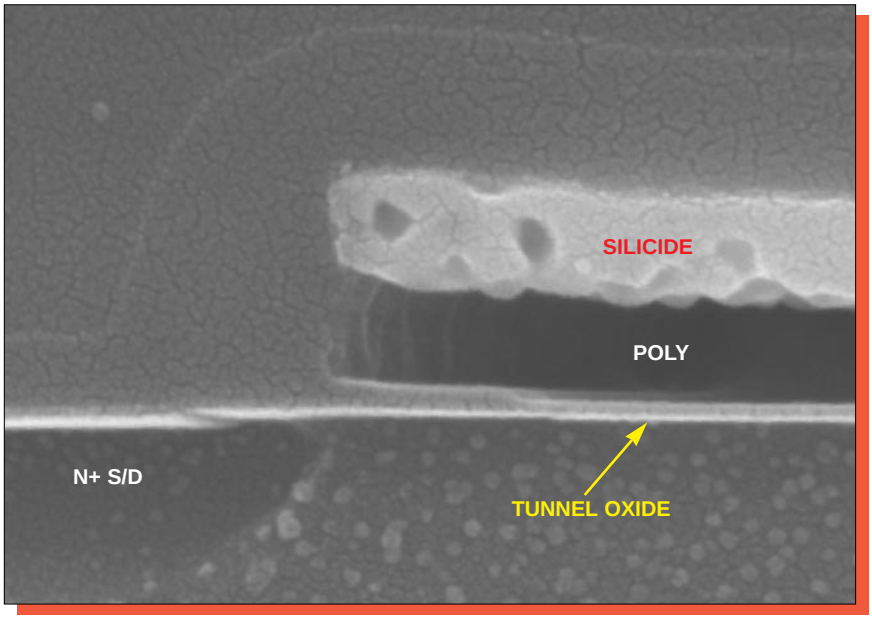


Mag. 26,000x

Figure 19. SEM section views of an EEPROM cell (parallel to bit line).

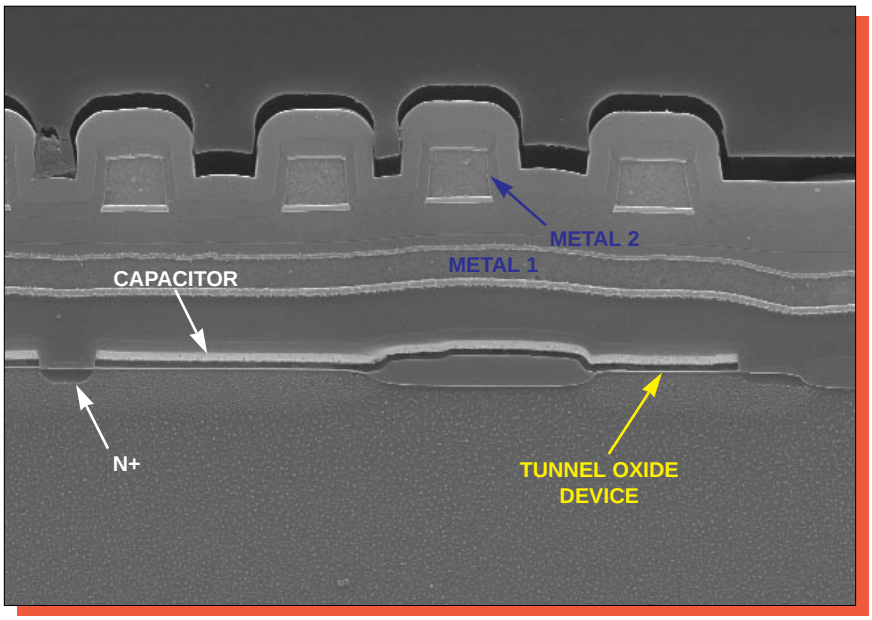


Mag. 52,000x

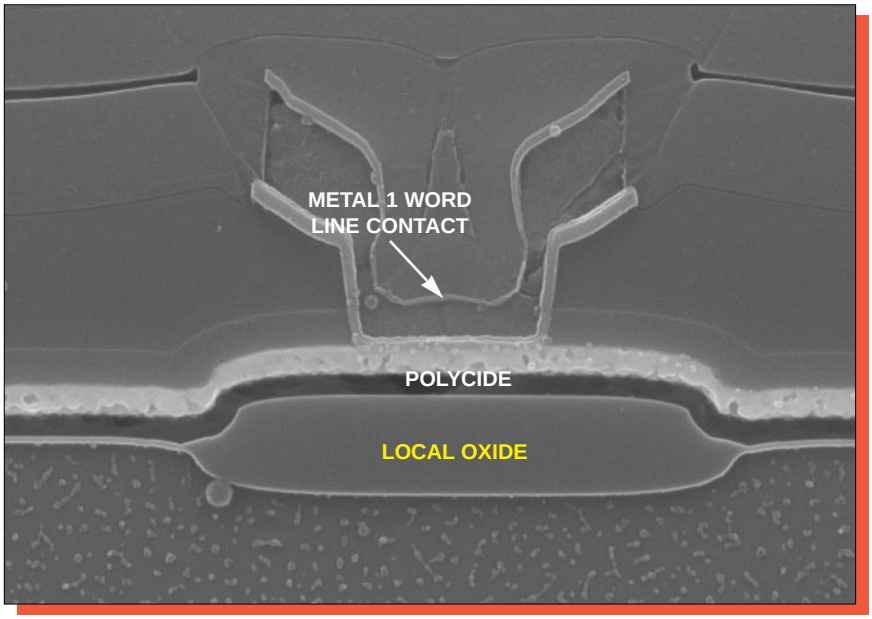


Mag. 104,000x

Figure 20. SEM section views of an EEPROM cell (parallel to bit line).

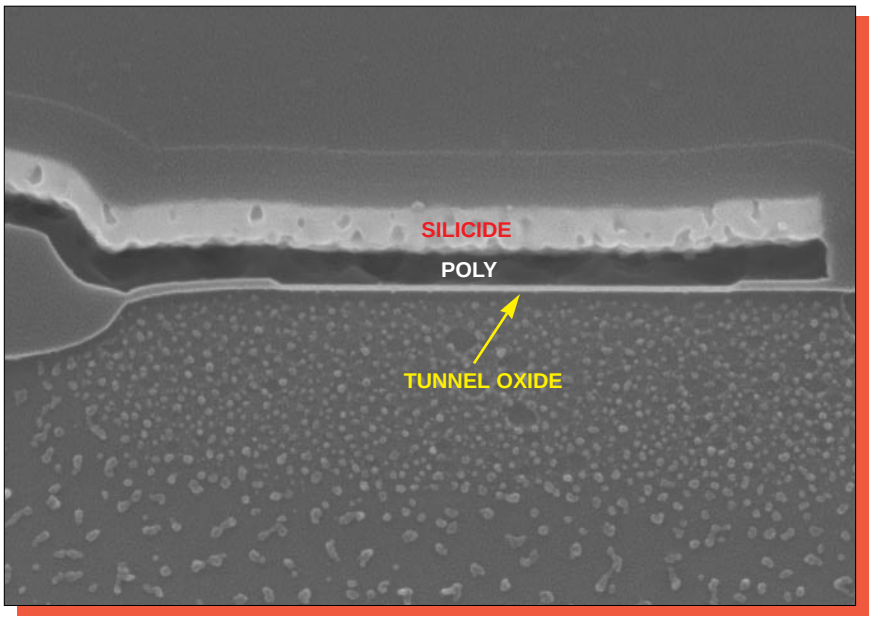


Mag. 8000x

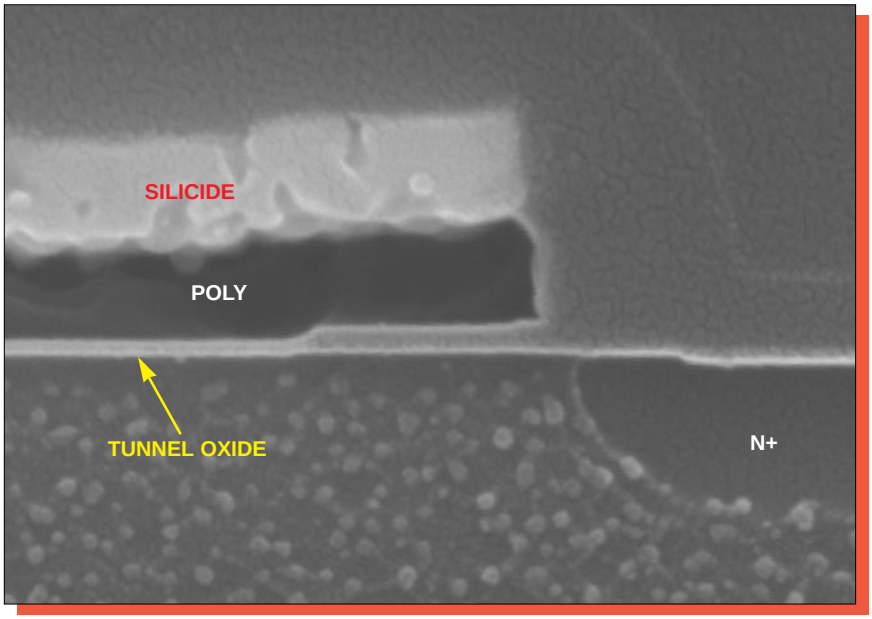


Mag. 26,000x

Figure 21. SEM section views of an EEPROM cell (perpendicular to bit line).

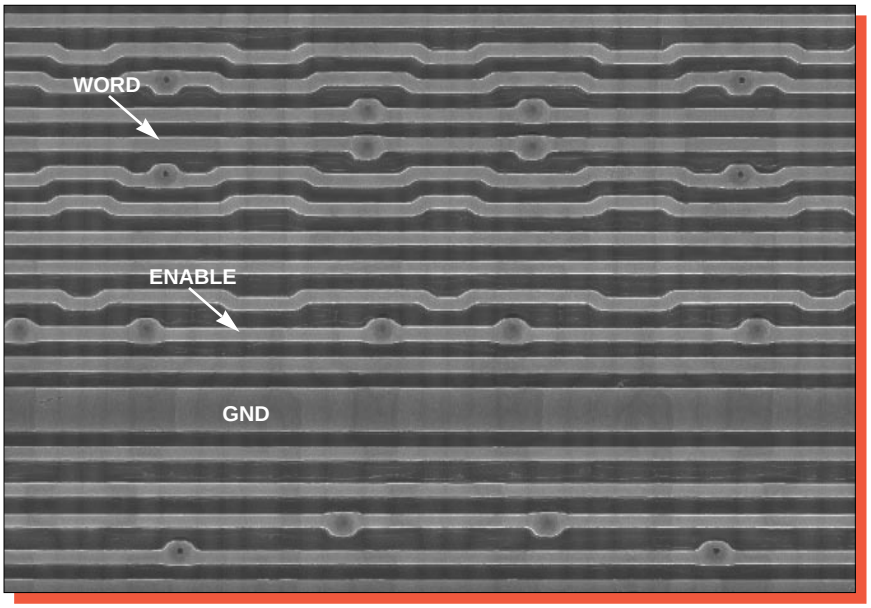


Mag. 40,000x

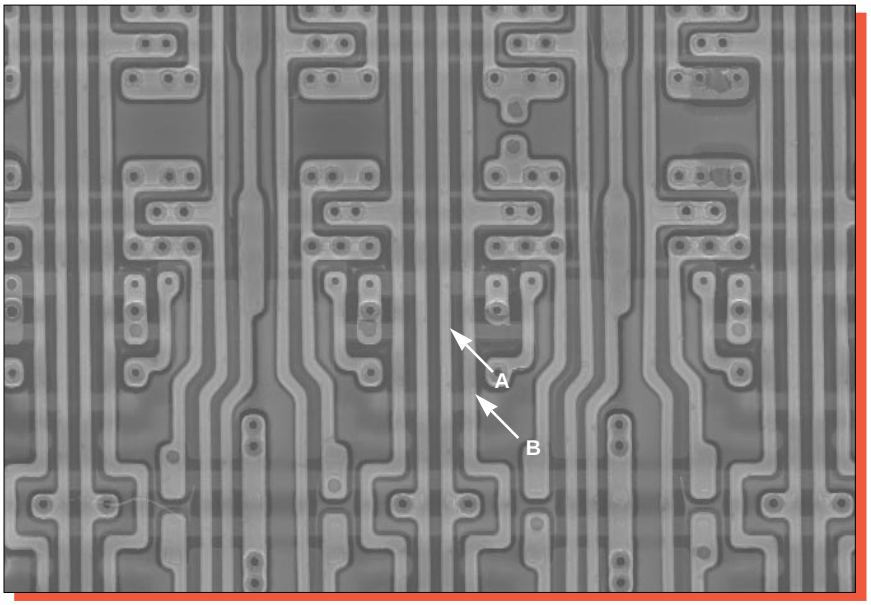


Mag. 104,000x

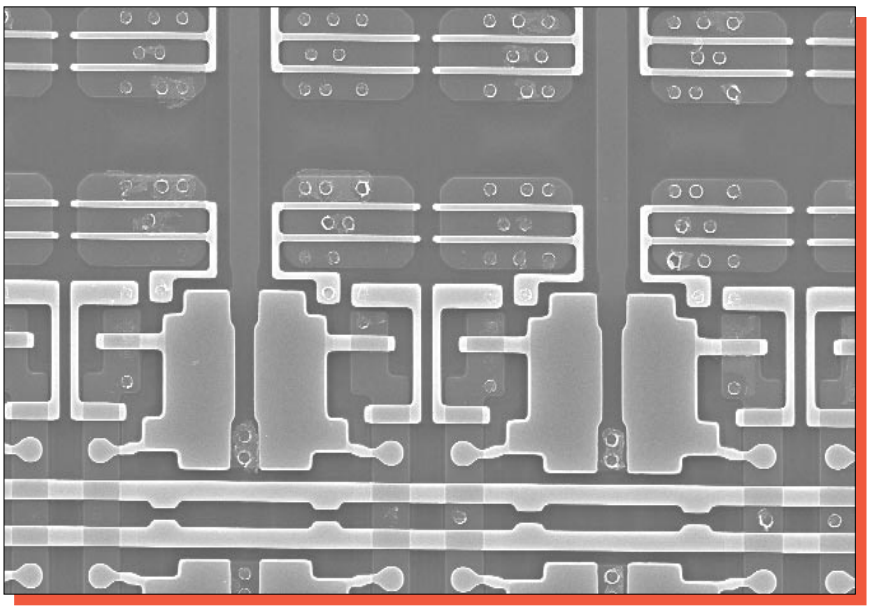
Figure 22. SEM section views of an EEPROM cell (perpendicular to bit line).



metal 2

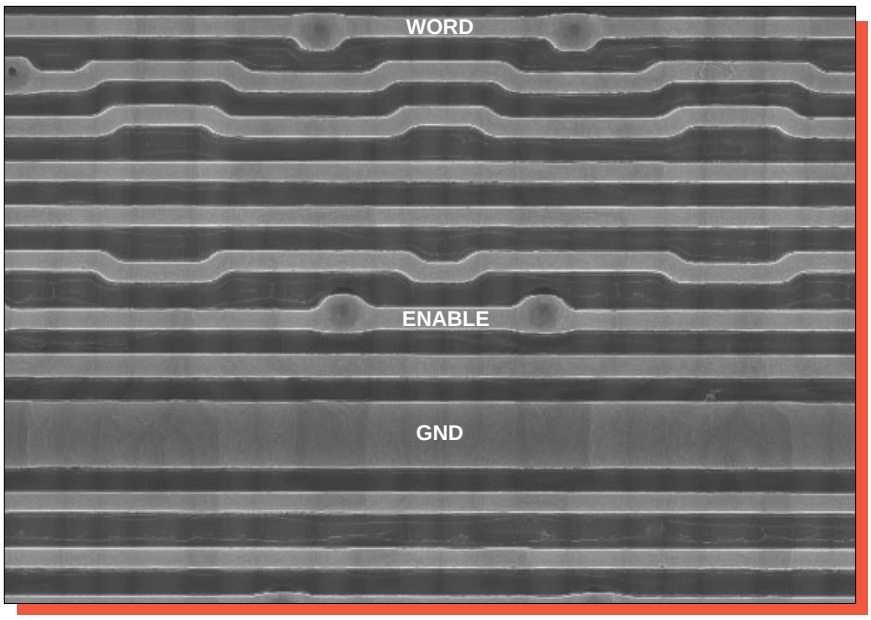


metal 1

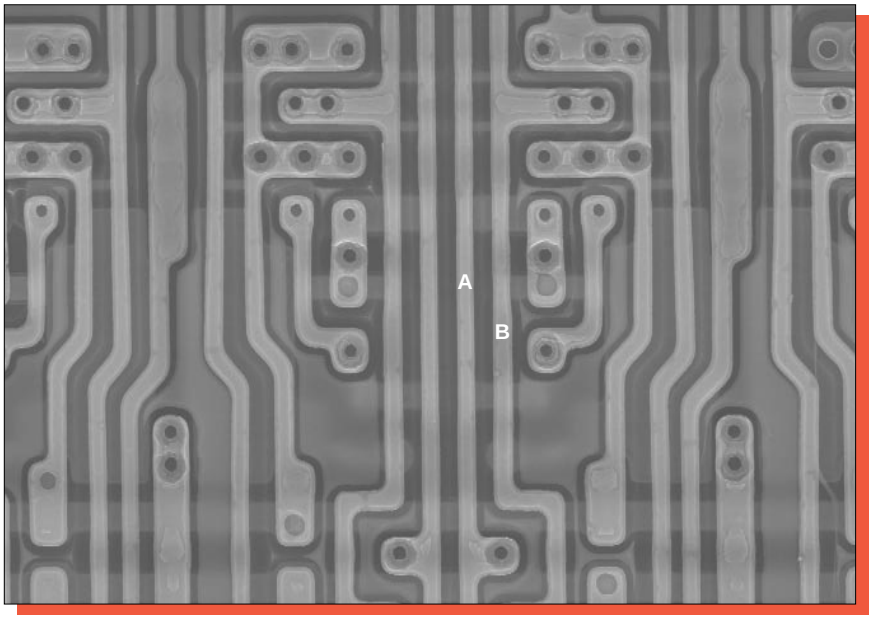


poly

Figure 23. Topological SEM views of an additional EEPROM cell. Mag. 1625x.

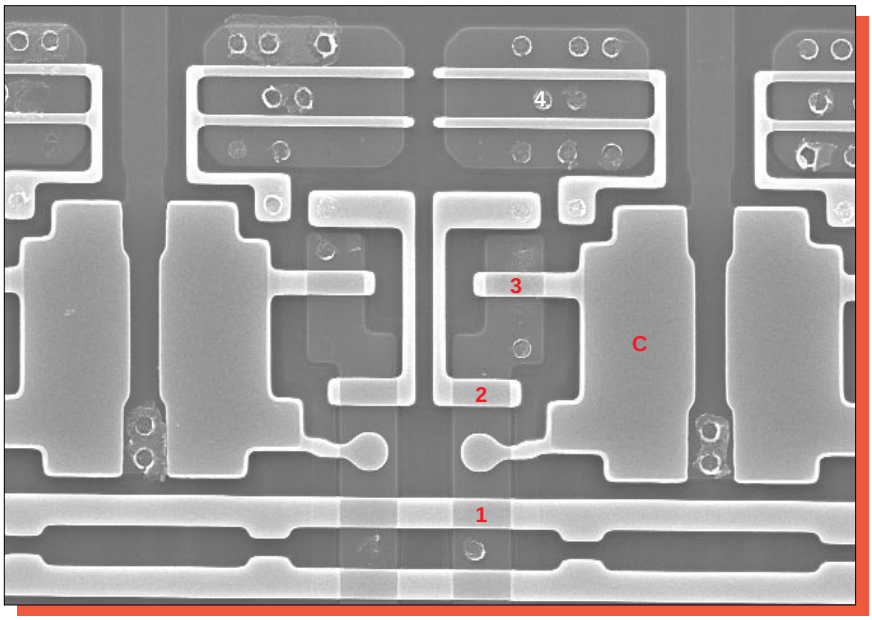


metal 2



metal 1

Figure 24. Topological SEM views of an additional EEPROM cell. Mag. 2500x.



poly

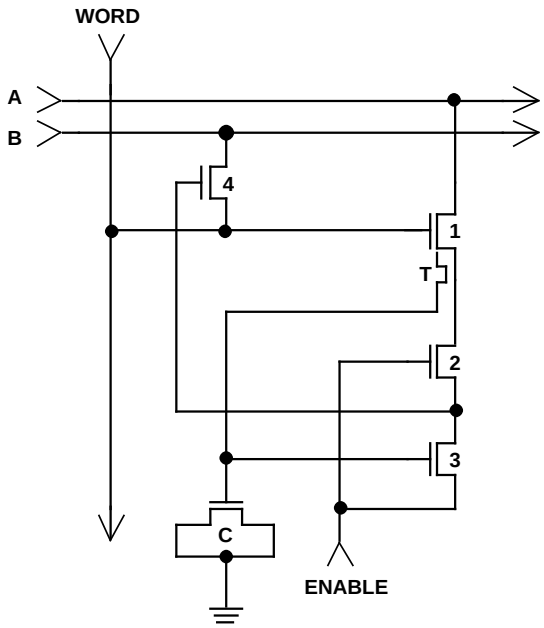
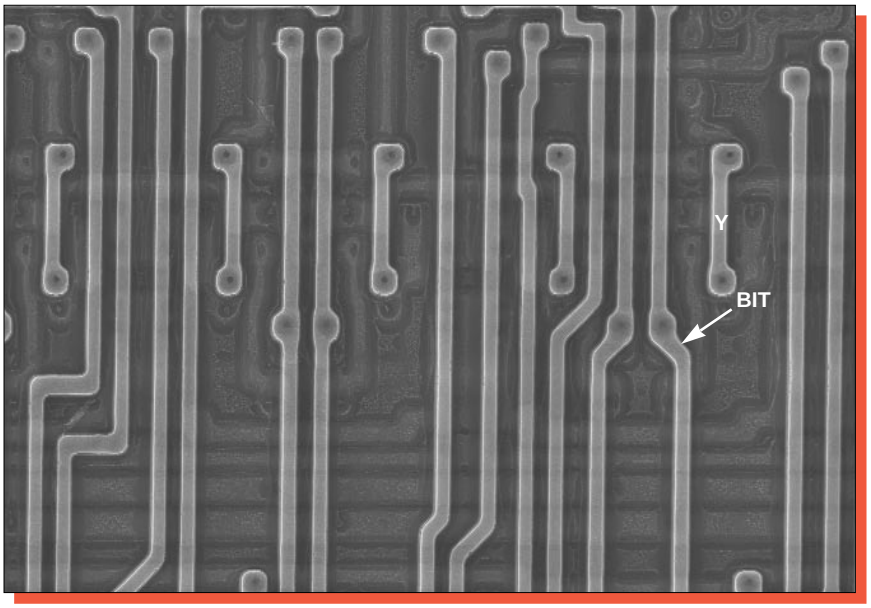
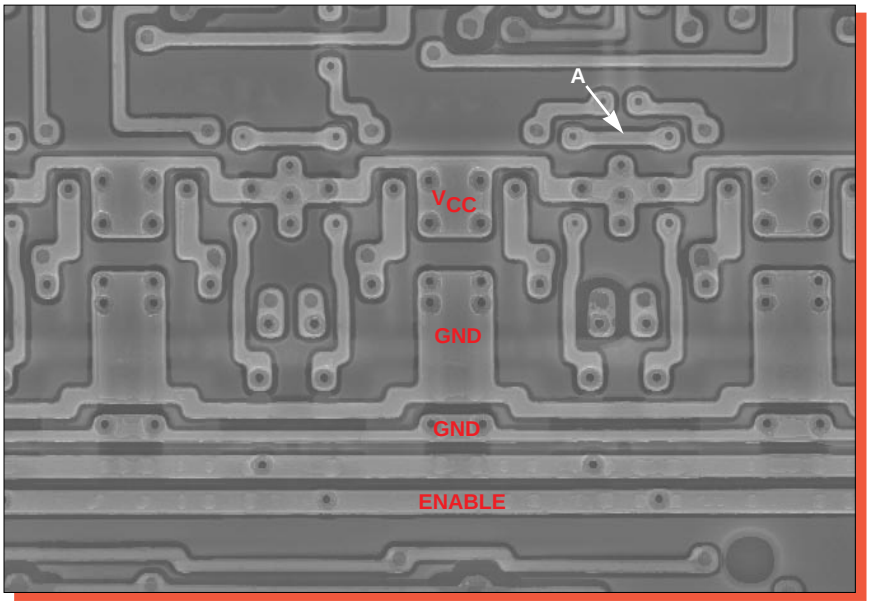


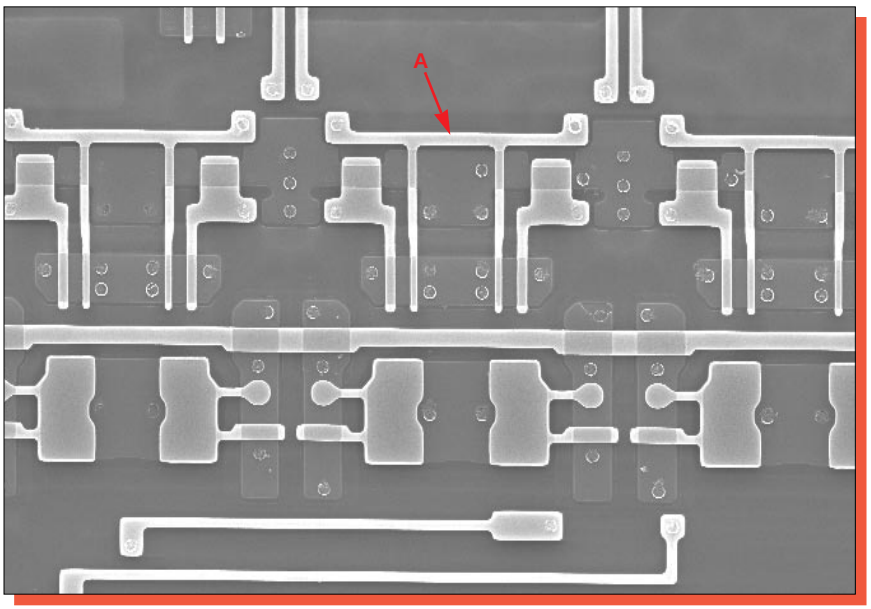
Figure 25. Topological view and schematic of an additional EEPROM cell.
Mag. 2500x.



metal 2

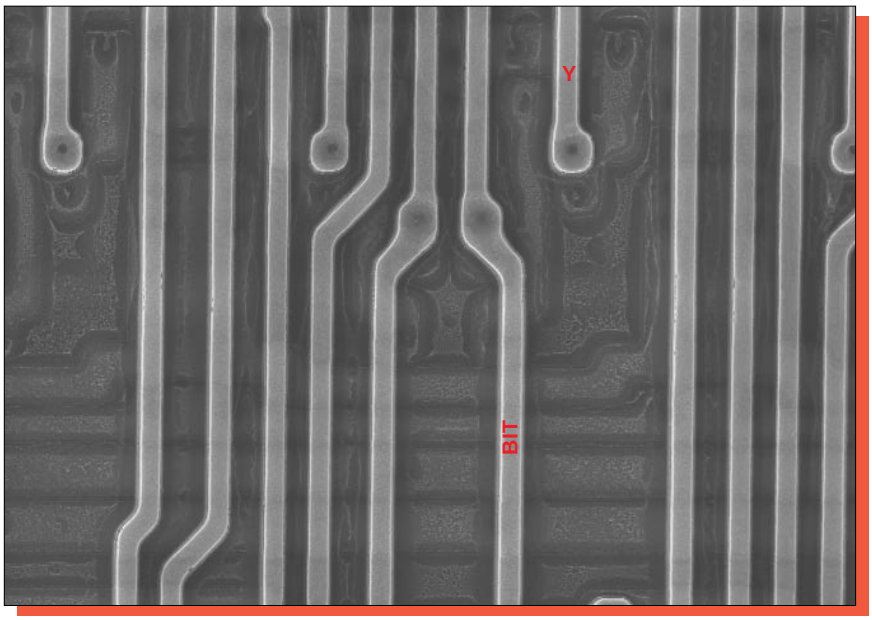


metal 1

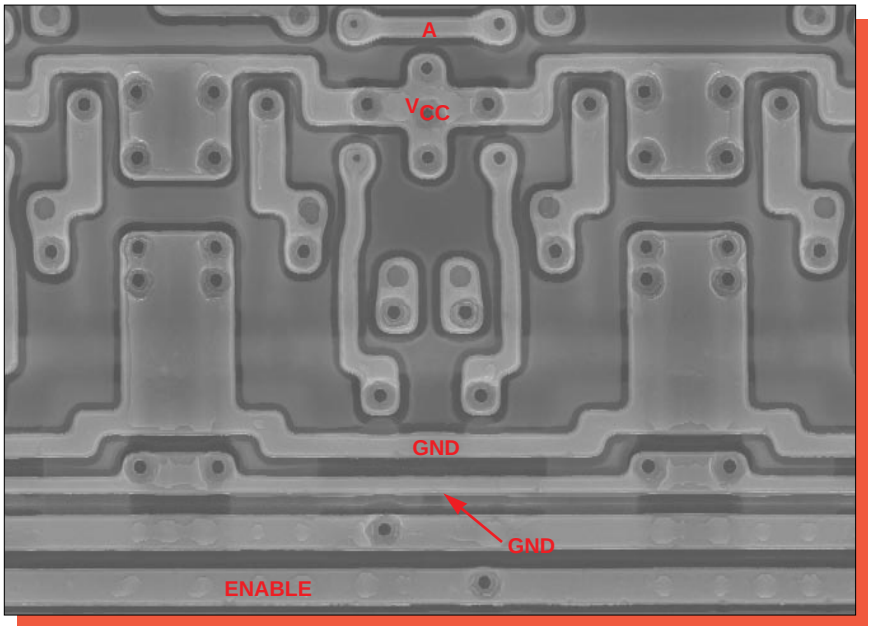


poly

Figure 26. Topological SEM views of an additional EEPROM cell. Mag. 1625x.

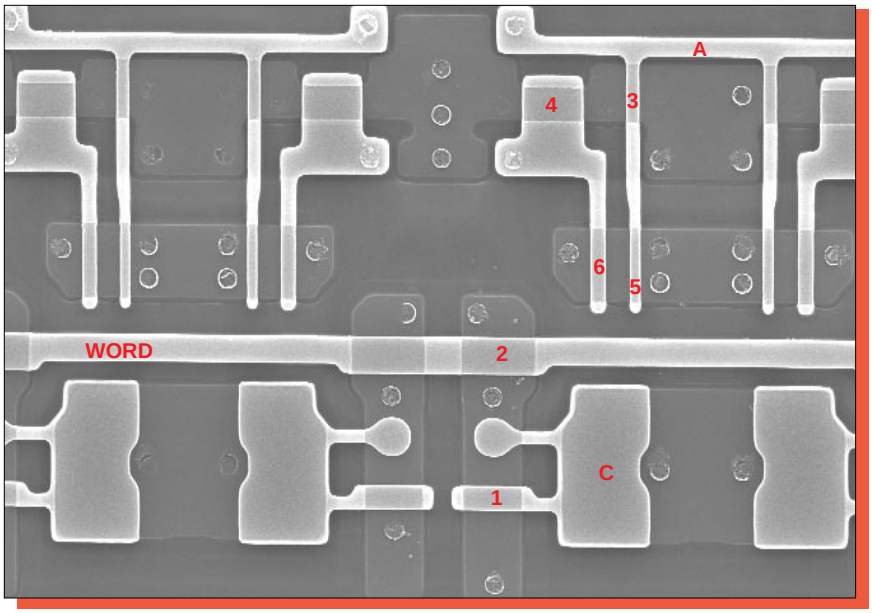


metal 2



metal 1

Figure 27. Topological SEM views of an additional EEPROM cell. Mag. 2500x.



poly

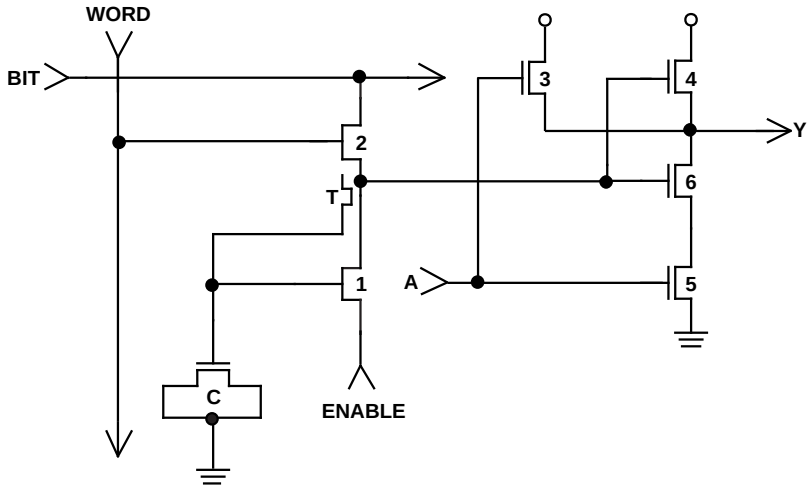


Figure 28. Topological view and schematic of an additional EEPROM cell.
Mag. 2500x.