Construction Analysis

Macronix 27C8100PC-10
8Mbit NAND EPROM

Report Number: SCA 9712-572

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Macronix 27C8100PC-10, 8Mbit NAND EPROM (OTP). Two samples were received for the analysis. The devices were packaged in 42-pin Dual In-Line plastic Packages (DIPs) date coded 9717.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 1 aluminum thinned up to 100 percent[2] at some locations of some contacts. Barrier metal remained intact to provide continuity.

Special Features:

- Unique cell design.

[1]These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application

[2]Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 42-pin plastic Dual In-Line Packages (DIPs).
- The copper (Cu) leadframe was internally plated with silver (Ag).
- External pins were tinned with tin-lead (SnPb) solder.
- Lead-locking provisions were present at all pins.
- Thermosonic wirebonding using 1.2 mil O.D. gold wire.
- Sawn dicing (full depth).
- Silver epoxy die attach.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-substrate.
- Die coat: No die coat was present.
- Final passivation: Three layers of passivation with a planarizing SOG between. As determined by etch characteristics, passivation 1 and 3 appeared to be nitide. However, this is unusual for a UV EPROM to have nitride overlay.
- Metallization: A single level of metal defined by standard dry-etch techniques. The metal consisted of aluminum with a titanium-nitride cap and titanium-nitride/titanium barrier. Standard contacts were employed throughout (no plugs).
- Pre-metal dielectric: A single layer of reflow glass over densified oxide.

TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Three layers of dry-etched polysilicon. Poly 3 (tungsten silicide on poly) was used to form all peripheral gates on the die and program lines in the array. Poly 3 was also used to form the control lines in the array. Poly 2 was used in conjunction with poly 1 to form all floating gates in the array. Direct poly-to-diffusion contacts were not used.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process using shallow S/D implants was used with the oxide sidewall spacers left in place.

- Isolation: LOCOS (local oxide isolation).

- Wells: N-wells in a P-substrate. No step was present at well boundaries.

- Redundancy: Poly 3 redundancy fuses were present on the die. Some laser blown fuses were noted. Cutouts in the passivation were present over all fuses.

- Memory cells: The UV EPROM array employed a unique stacked gate structure implemented in a NAND configuration. Metal 1 formed the bit lines and carried GND. Poly 1 was used for all memory gates although it was contacted directly by poly 2 at floating gates. Poly 1 also defined the channel region for control gates, but was removed prior to poly 3 formation. The same gate oxide is thus present in both locations. Poly 3 formed all program and control lines in the array.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 4**

Questionable Items:[1] None.

General Items:

- Devices were packaged in 42-pin plastic DIPs.
- Overall package quality: Good. No defects were found on the external or internal portions of the packages. External pins were well formed and no voids or cracks were noted.
- Wirebonding: Thermosonic bond method using 1.2 mil O.D. gold wire. Wire spacing and placement was good. No problems were noted.
- Die attach: Silver epoxy die attach of good quality.
- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.
- Die coat: No die coat was used on the die.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 5 - 33**

Questionable Items:[1]

- Metal 1 aluminum thinned up to 100 percent[2] at some locations of some contacts. Barrier metal remained intact to provide continuity.

Special Features:

- Unique cell design.

General Items:

- Fabrication process: Devices were fabricated using selective oxidation CMOS process employing N-wells in a P-substrate.

- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Die coat: No die coat was used.

- Final passivation: Three layers of passivation with an SOG layer to planarize the surface. As stated above, passivation 1 and 3 appeared to be nitride. Edge seal was good as the passivation extended beyond the metallization.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metallization: A single level of metal was used. It consisted of aluminum with a titanium-nitride cap and a titanium-nitride on titanium barrier. Standard contacts were used (no plugs).

- Metal patterning: The metal layer was defined by a dry etch of normal quality.

- Metal defects: None. No voiding, notching or cracking of the metal layer was found. No silicon nodules were found following removal of the metal layer.

- Metal step coverage: Aluminum thinned up to 100 percent at some contacts. Barrier metal remained intact to provide continuity. This thinning was a result of minimum contact spacing. Normal metal thinning was typically 70 percent.

- Contacts: All contact cuts were defined by a dry etch of normal quality. Alignment of the metal was good. No overetching was present.

- Pre-metal dielectric: A layer of reflow glass (BPSG) over densified oxide was used under the metal layer. Reflow was performed after contact cuts and resulted in well rounded steps. No problems were found.

- Polysilicon: Three layers of polysilicon were used. Poly 3 (tungsten silicide on poly) was used to form all peripheral gates on the die and program lines in the array (over poly 2). Poly 3 was also used to form the control lines in the array. Poly 2 was used in conjunction with poly 1 to form all floating gates in the array. Definition of all layers was by a dry-etch of normal quality. Direct poly-to-diffusion contacts were not used.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process using shallow S/D implants was used with oxide sidewall spacers left in place. No problems were found.

- Isolation: LOCOS (local oxide isolation). No step was present at well boundaries.

ANALYSIS RESULTS II (continued)

- Wells: N-wells formed in a P-substrate. No problems were found.

- Redundancy: Poly 3 redundancy fuses were present on the die. Some laser blown fuses were noted. Cutouts were present in the passivation over all fuses. No problems were found.

- Memory cells: The EPROM array employed a unique stacked gate structure implemented in a NAND configuration. Metal 1 formed the bit lines and carried GND. Poly 1 was used for all memory gates although it was contacted directly by poly 2 at floating gates. Poly 1 also defined the channel region for control gates, but was removed prior to poly 3 formation. The same gate oxide is thus present in both locations. Poly 3 formed all program and control lines in the array.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Passivation integrity test

Passivation removal

SEM inspection of metal

Aluminum removal and inspect contacts

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal to Poor.

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	N
Die attach quality	N
Die attach method	Silver epoxy
Dicing method:	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.2 mil O.D. gold wire
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP
Metal registration	G
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP	BOTTOM
MX (logo) 27C8100PC-10 M12829 TAIWAN B9717 VPP = 12.5V	B9717 M12829

DIE MATERIALS

Overlay passivation:	Layer of glass over two layers of nitride? with an SOG between.
Metallization:	Aluminum with a titanium-nitride cap and a titanium-nitride on titanium barrier.
Pre-metal dielectric:	Reflow glass (BPSG).
Polycide:	Tungsten-silicide on polysilicon.

HORIZONTAL DIMENSIONS

Die size:	7.4 x 7.5 mm (291 x 294 mils)
Die area:	55.5 mm^2 (85,554 $mils^2$)
Min pad size:	0.1 x 0.1 mm (3.9 x 3.9 mils)
Min pad window:	0.09 x 0.09 mm (3.5 x 3.5 mils)
Min pad space:	0.02 mm
Min metal width:	0.9 micron
Min metal space:	1.0 micron
Min metal pitch (uncontacted):	1.9 micron
Min metal pitch (contacted):	2.5 microns
Min contact:	0.9 micron (round)
Min poly 3 width:	0.6 micron
Min poly 3 space:	0.6 micron
Min diffusion spacing:	0.75 micron
Min gate length*	
- (N-channel):	0.8 micron
- (P-channel):	0.9 micron
Min poly 2/poly 1 width -	
- (floating gate):	0.6 micron

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (19 mils)

Layers

Passivation 4:	0.8 micron
Passivation 3:	0.65 micron
Passivation 2 (SOG):	0 - 1.5 micron
Passivation 1:	0.35 micron
Metal 1 - cap:	0.05 micron (approx.)
- aluminum:	0.9 micron
- TiN/Ti barrier:	0.15 micron
Pre-metal glass:	0.35 micron (average)
Poly 3 - silicide:	0.13 micron
- poly:	0.17 micron
Poly 2:	0.06 micron (approx.)
Poly 1:	0.06 micron (approx.)
Local oxide:	0.5 micron
N+ S/D diffusion:†	0.2 micron
P+ S/D diffusion:	0.3 micron
N-well:	2.5 microns (approx.)

**Physical gate length.*

†*Shallow S/D implant could not be delineated well enough to measure.*

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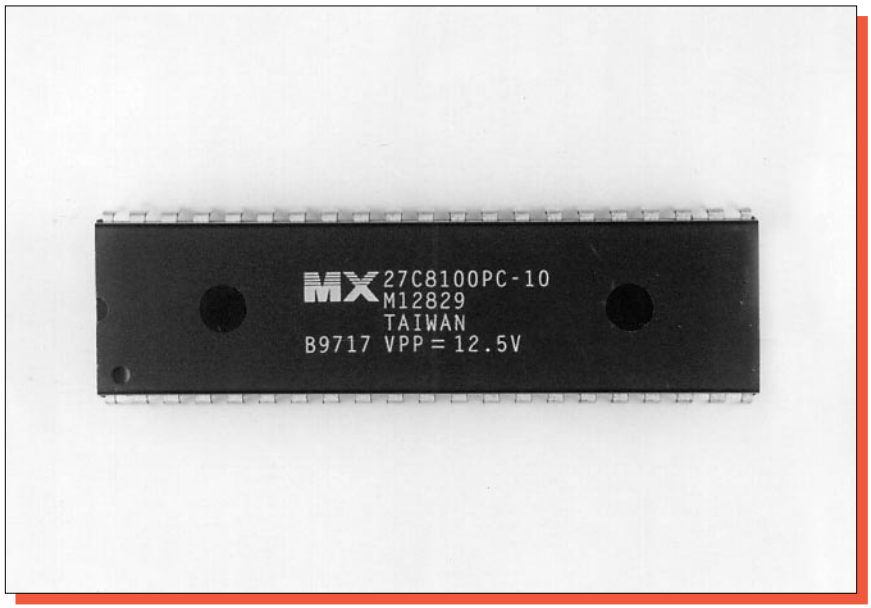
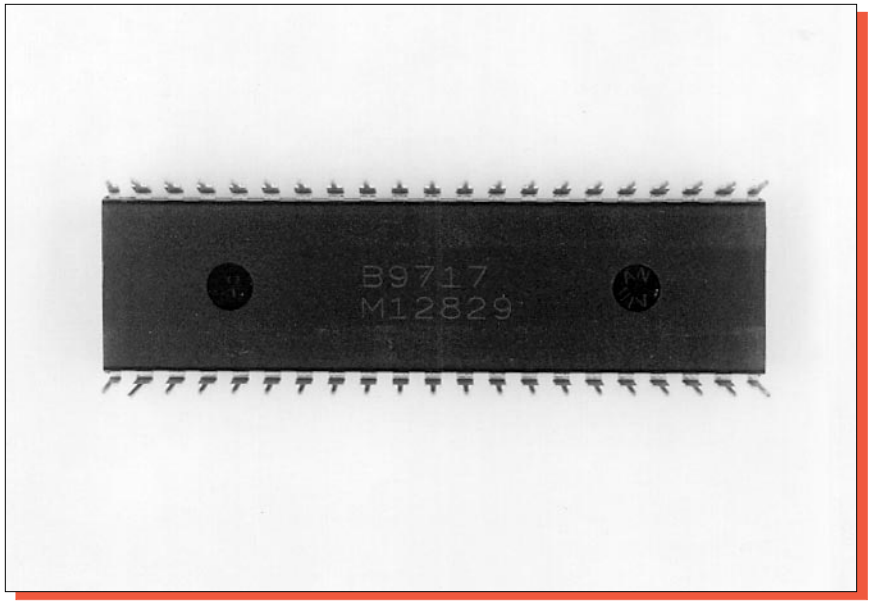




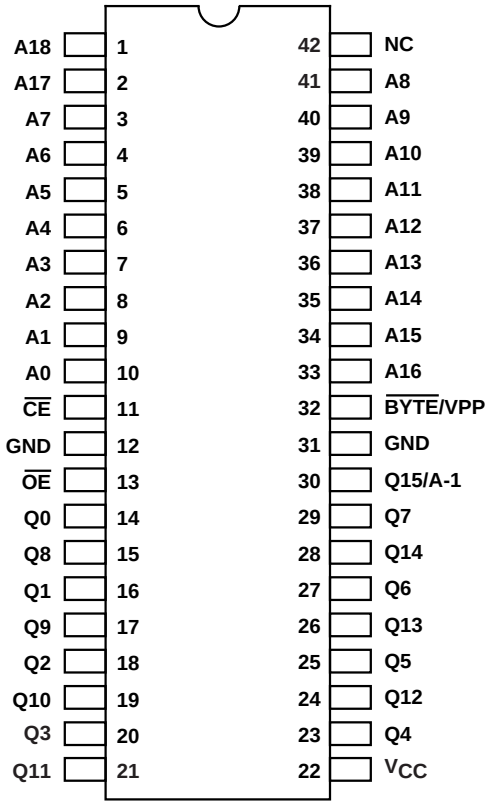


Figure 1. Package photographs and pinout of the Macronix 27C8100PC-10, 8Mb EPROM. Mag. 1.6x.

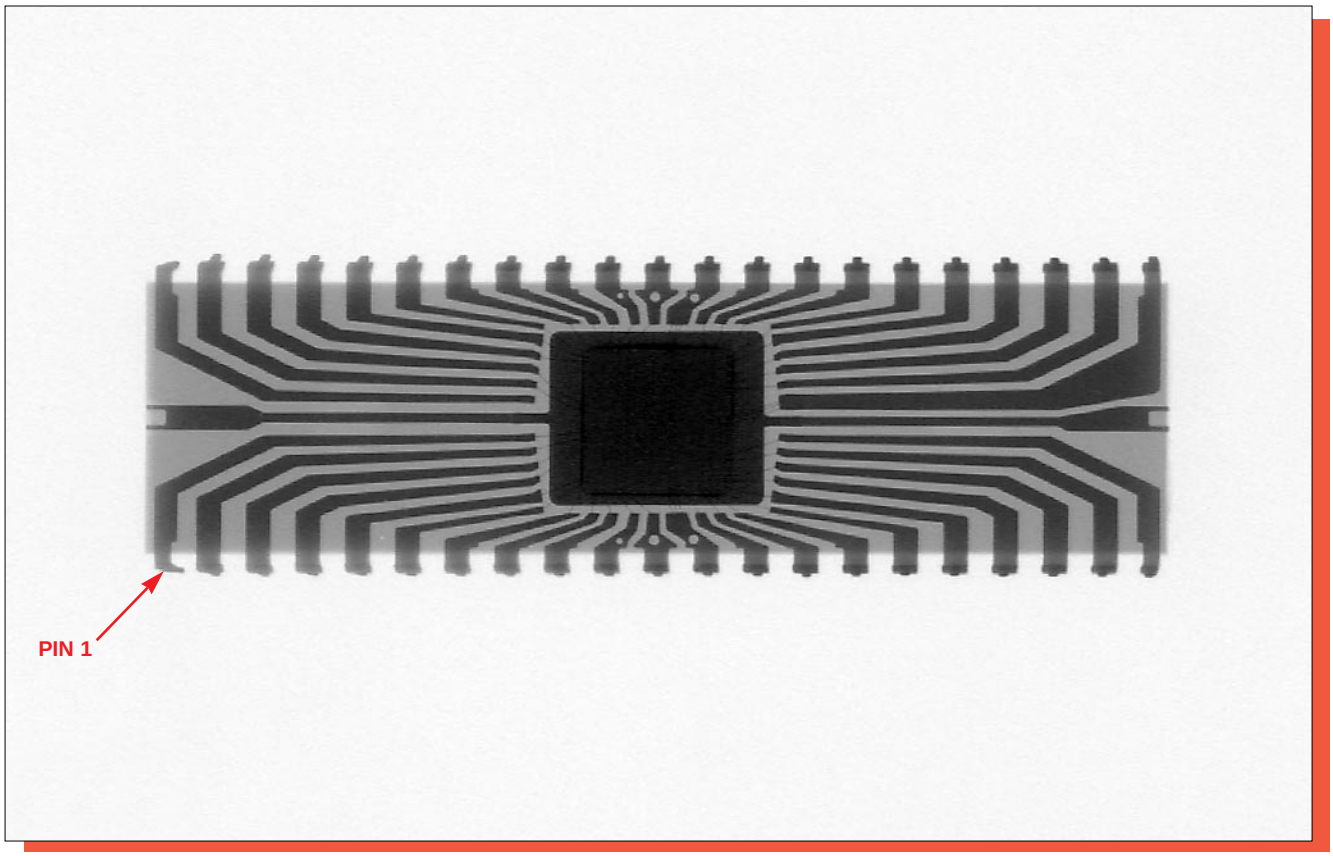
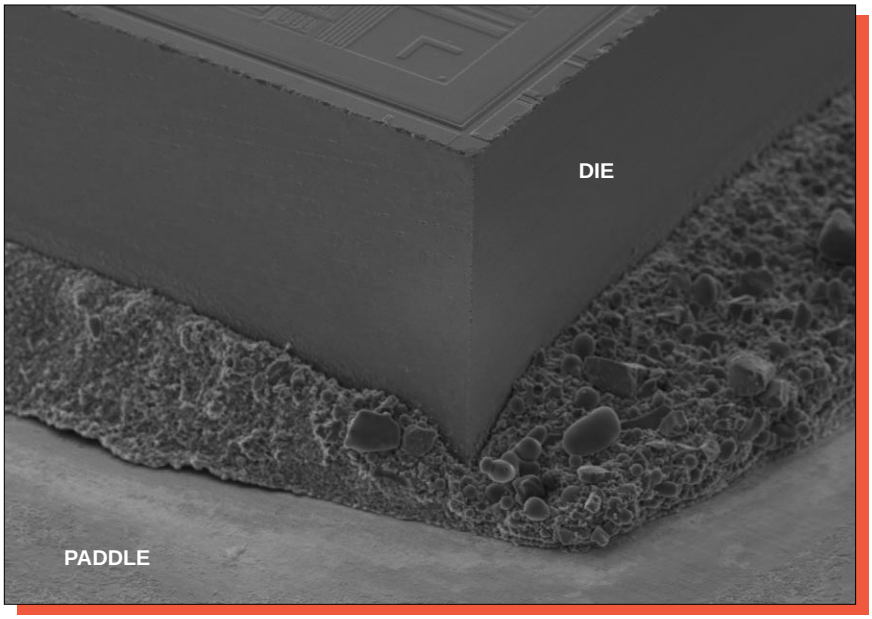
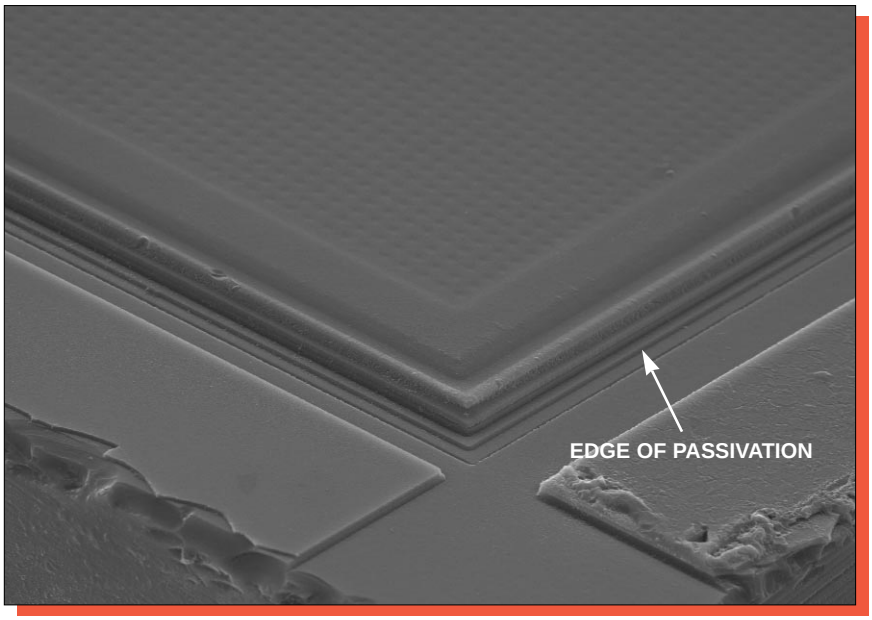


Figure 2. X-ray view of the package. Mag. 2.5x.

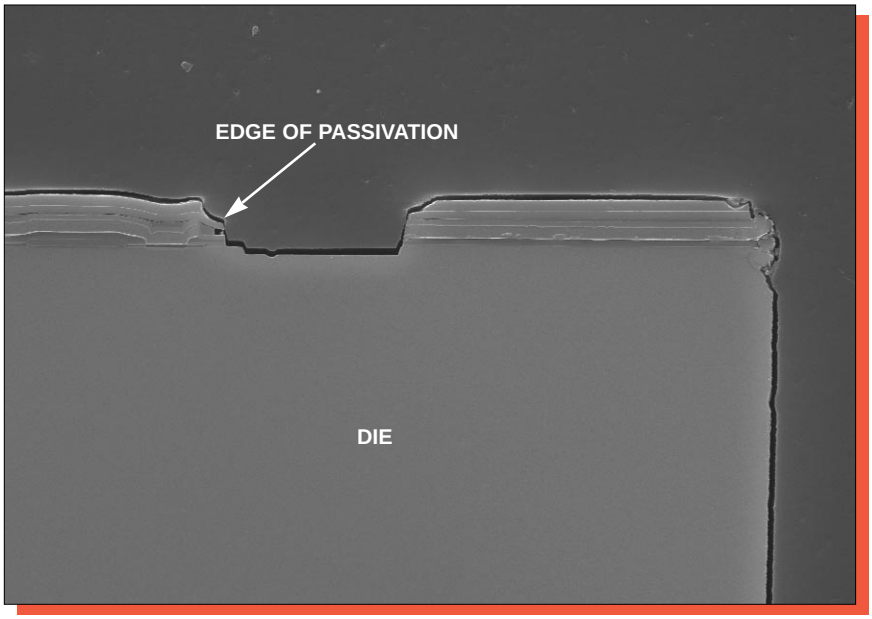


Mag. 110x

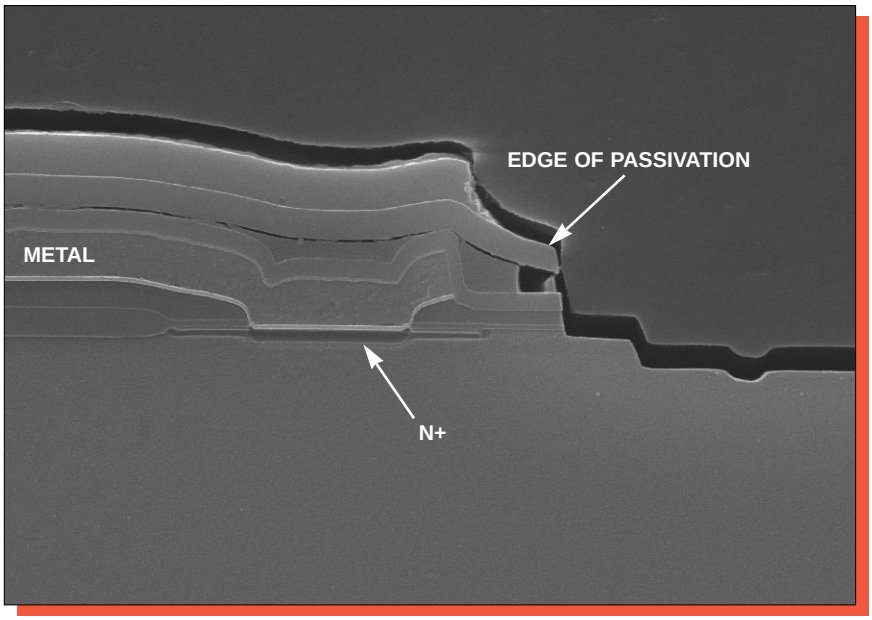


Mag. 1000x

Figure 3. SEM views of dicing and edge seal. 60°.



Mag. 1600x



Mag. 6500x

Figure 4. SEM section views of the edge seal.

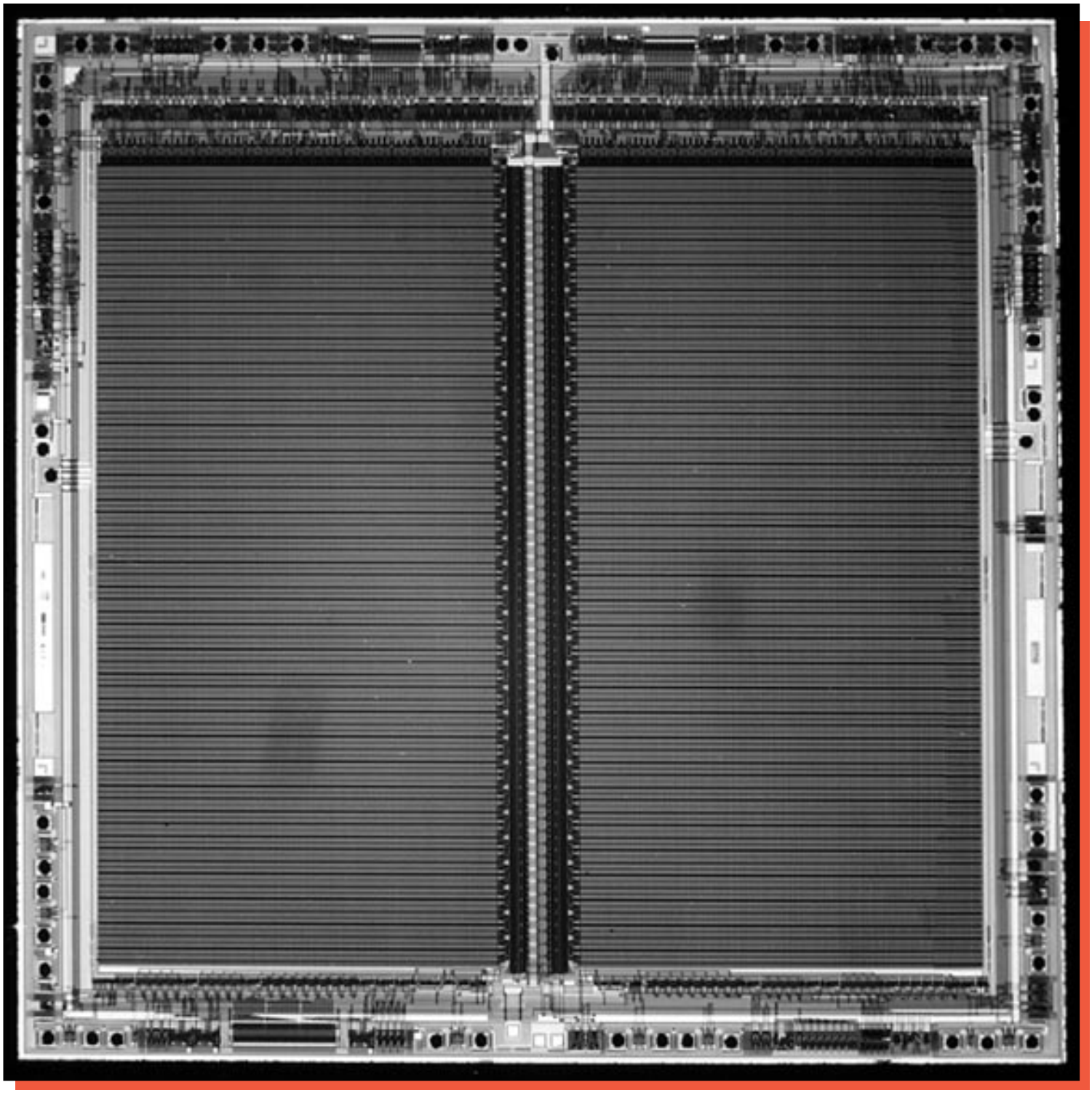


Figure 5. Whole die photograph of the Macronix 27C8100PC-10, 8Mb EPROM.
Mag. 25x.

Figure 6. Optical views of die markings. Mag. 350x.

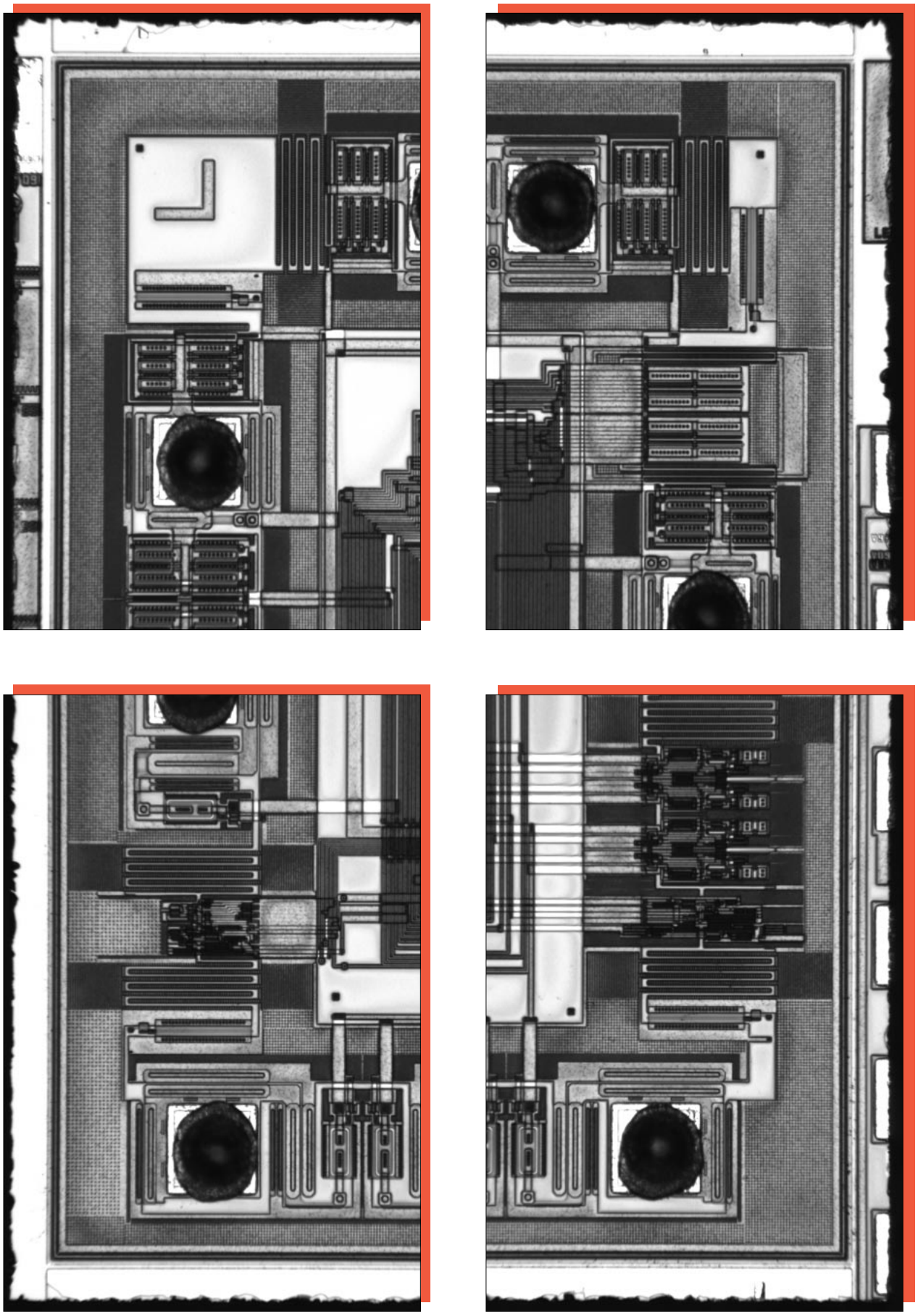
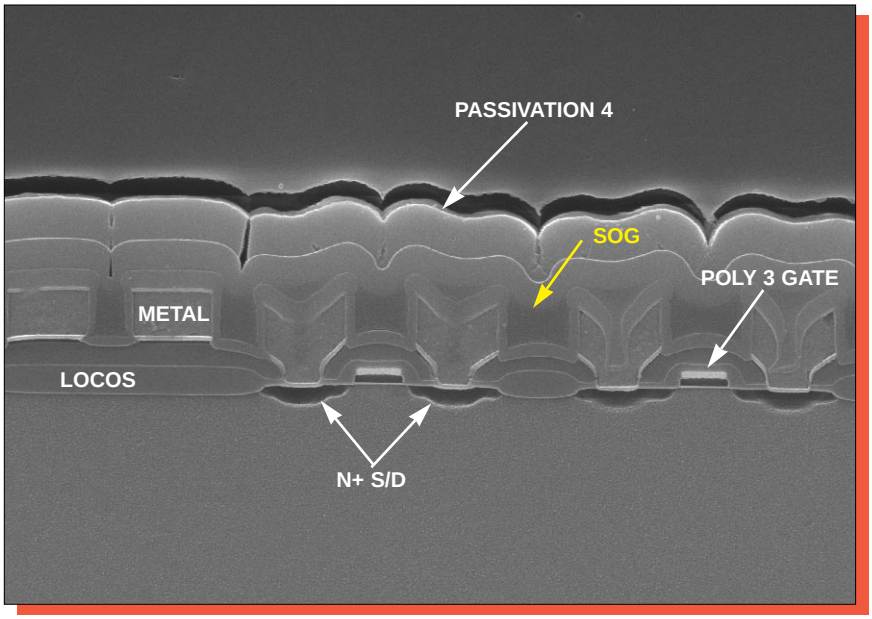
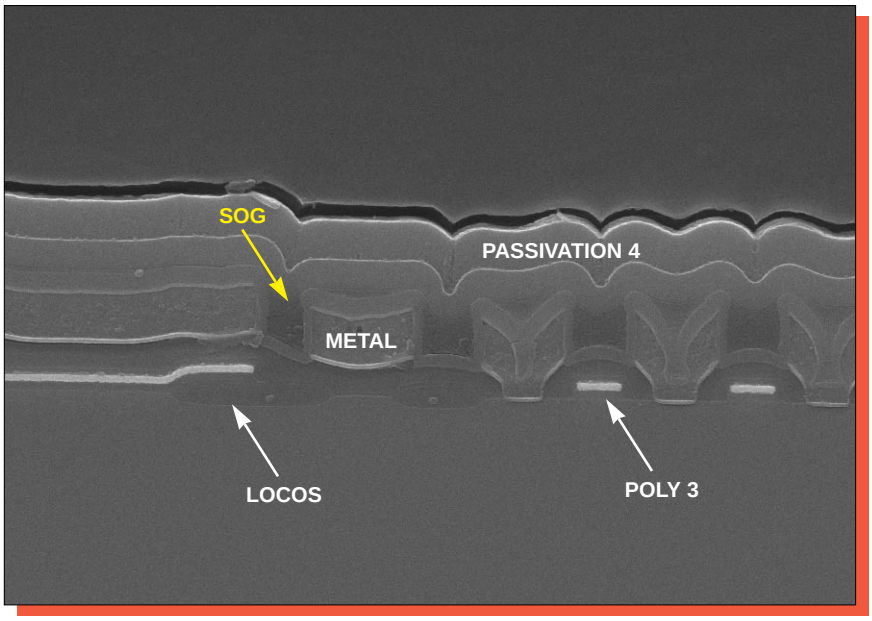


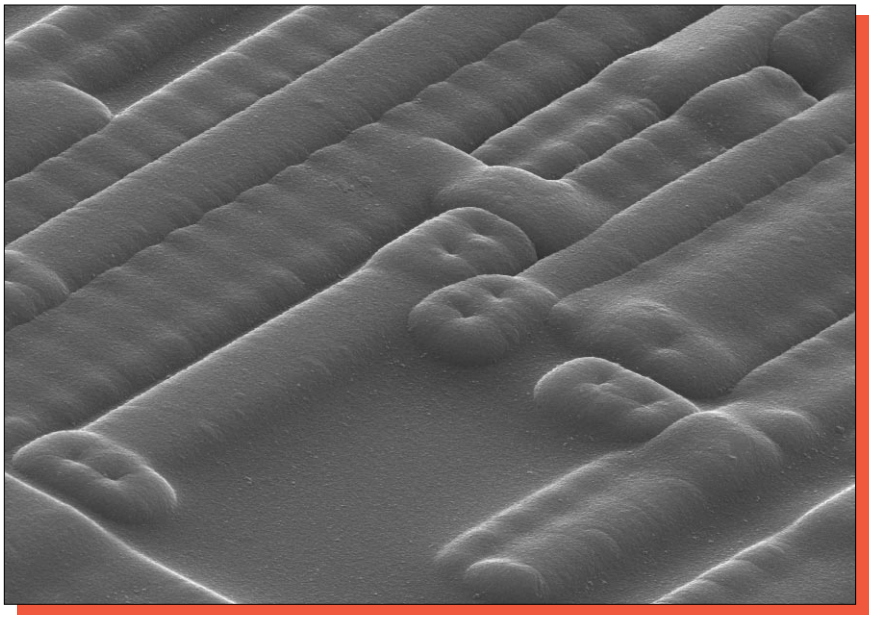
Figure 7. Optical views of die corners. Mag. 170x.



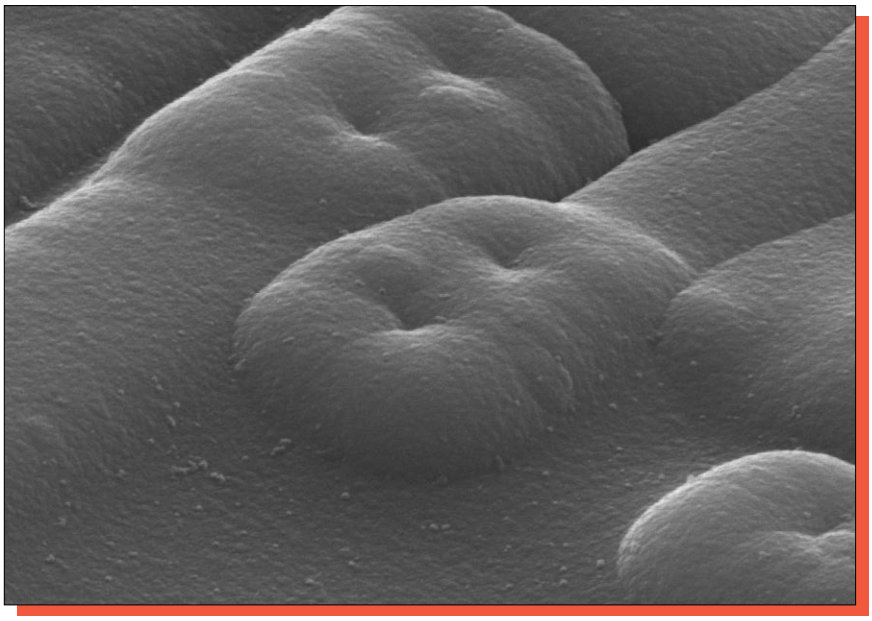


glass etch

Figure 8. SEM section views illustrating general structure. Mag. 6500x.

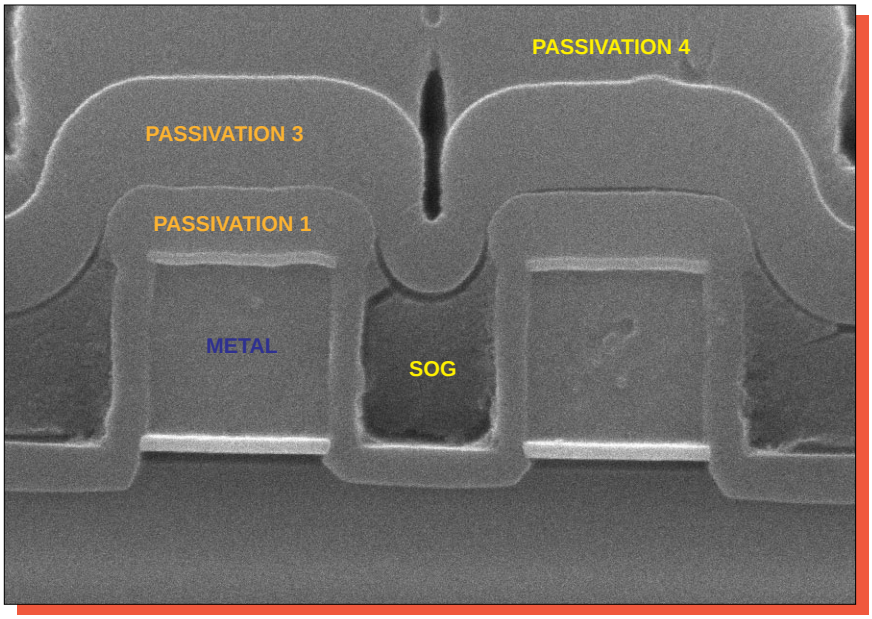


Mag. 4200x

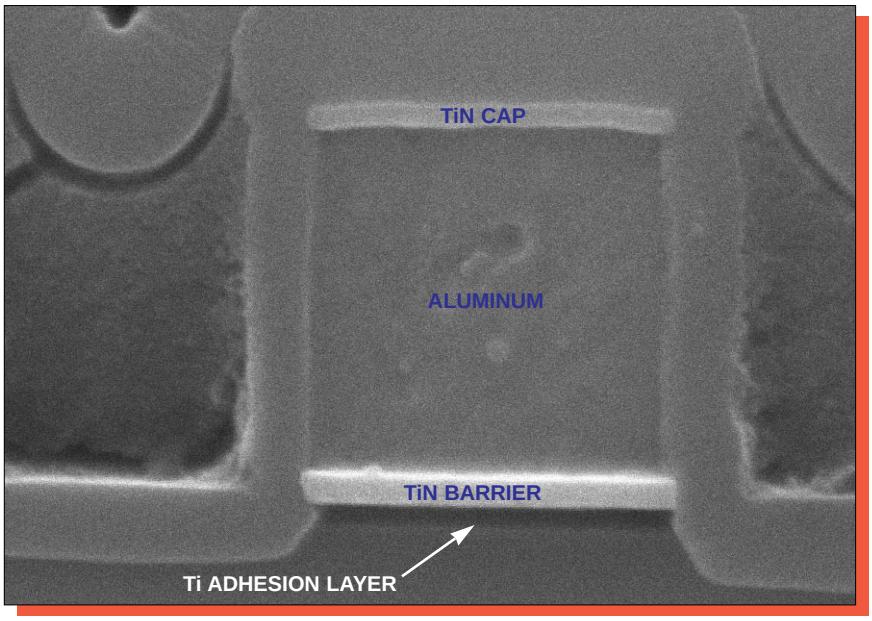


Mag. 13,000x

Figure 9. Perspective SEM views illustrating final passivation. 60°.



Mag. 26,000x



Mag. 52,000x

Figure 10. SEM section views of metal line profiles.

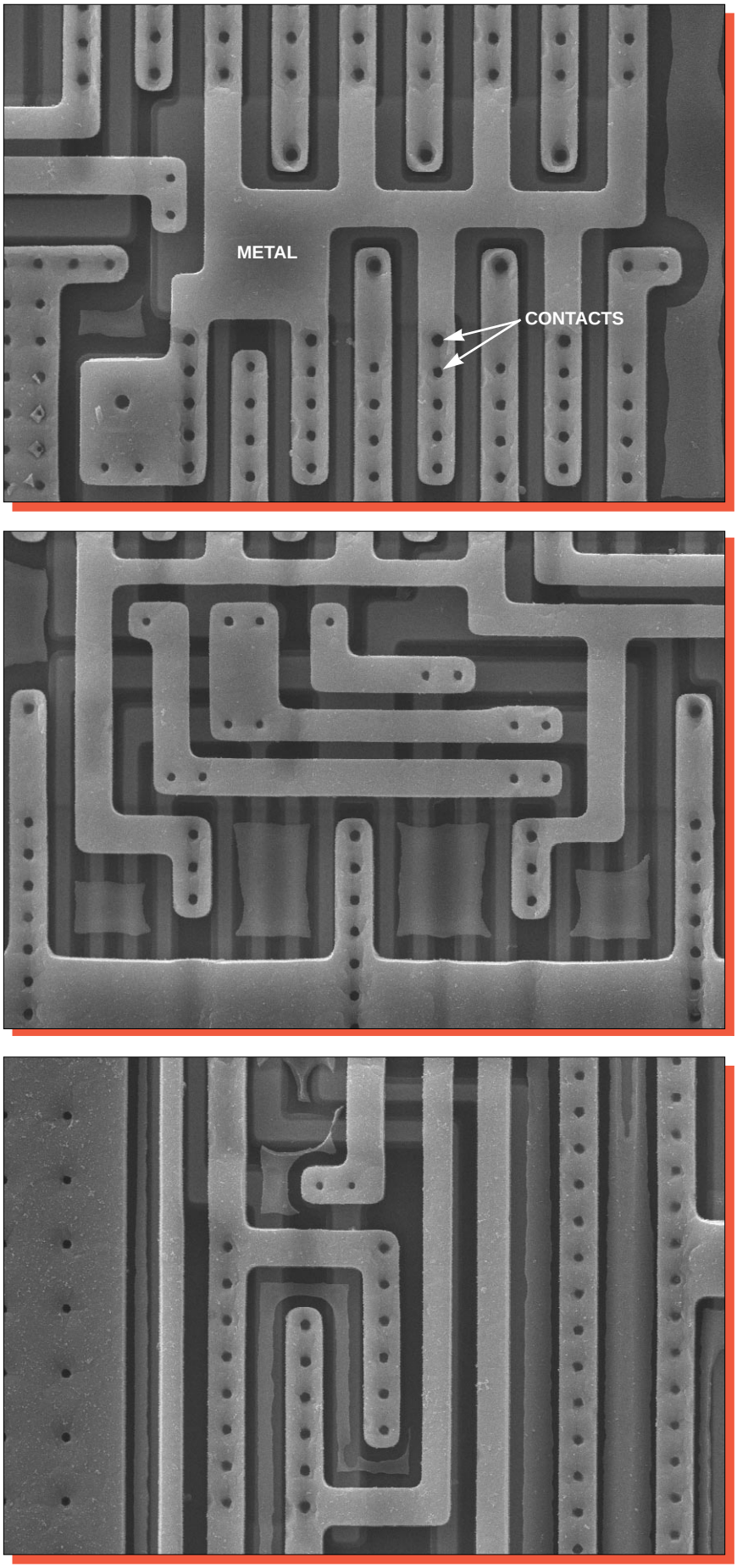
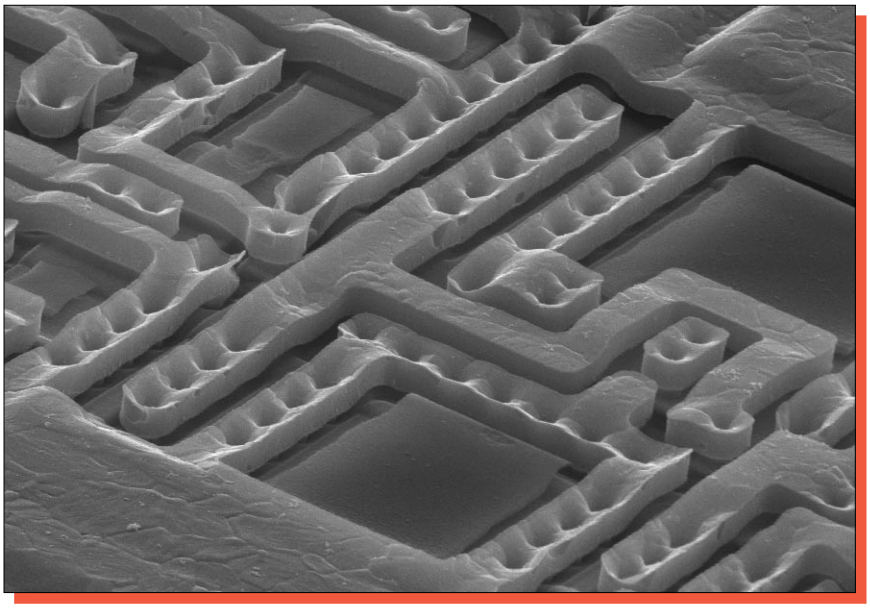
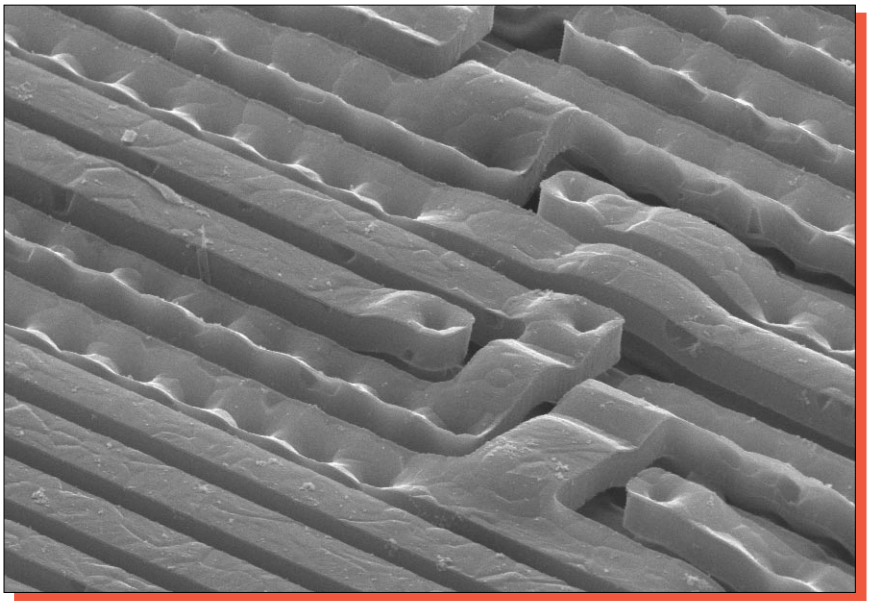


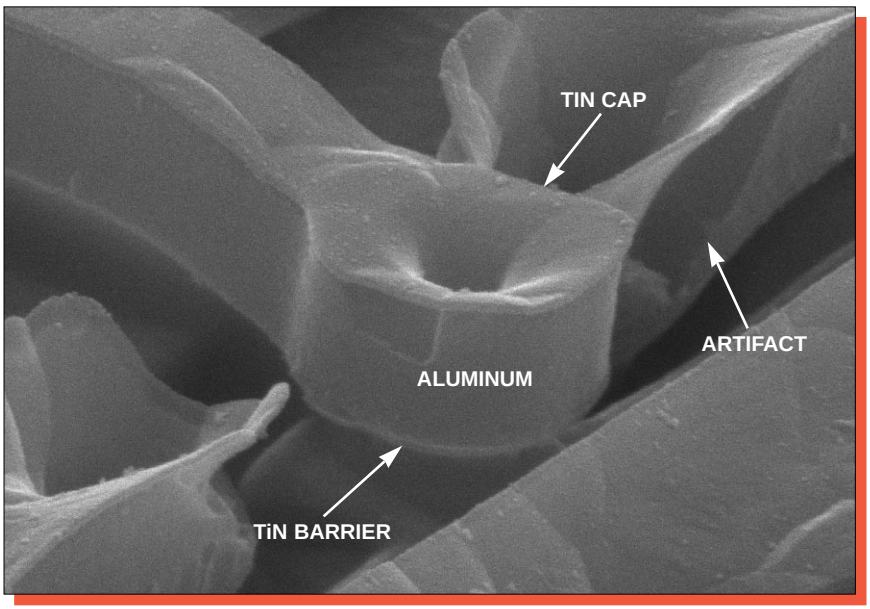
Figure 11. Topological SEM views of metal patterning. Mag. 3200x, 0°.



Mag. 4200x



Mag. 5700x



Mag. 23,000x

Figure 12. Perspective SEM views of metal step coverage. 60°.

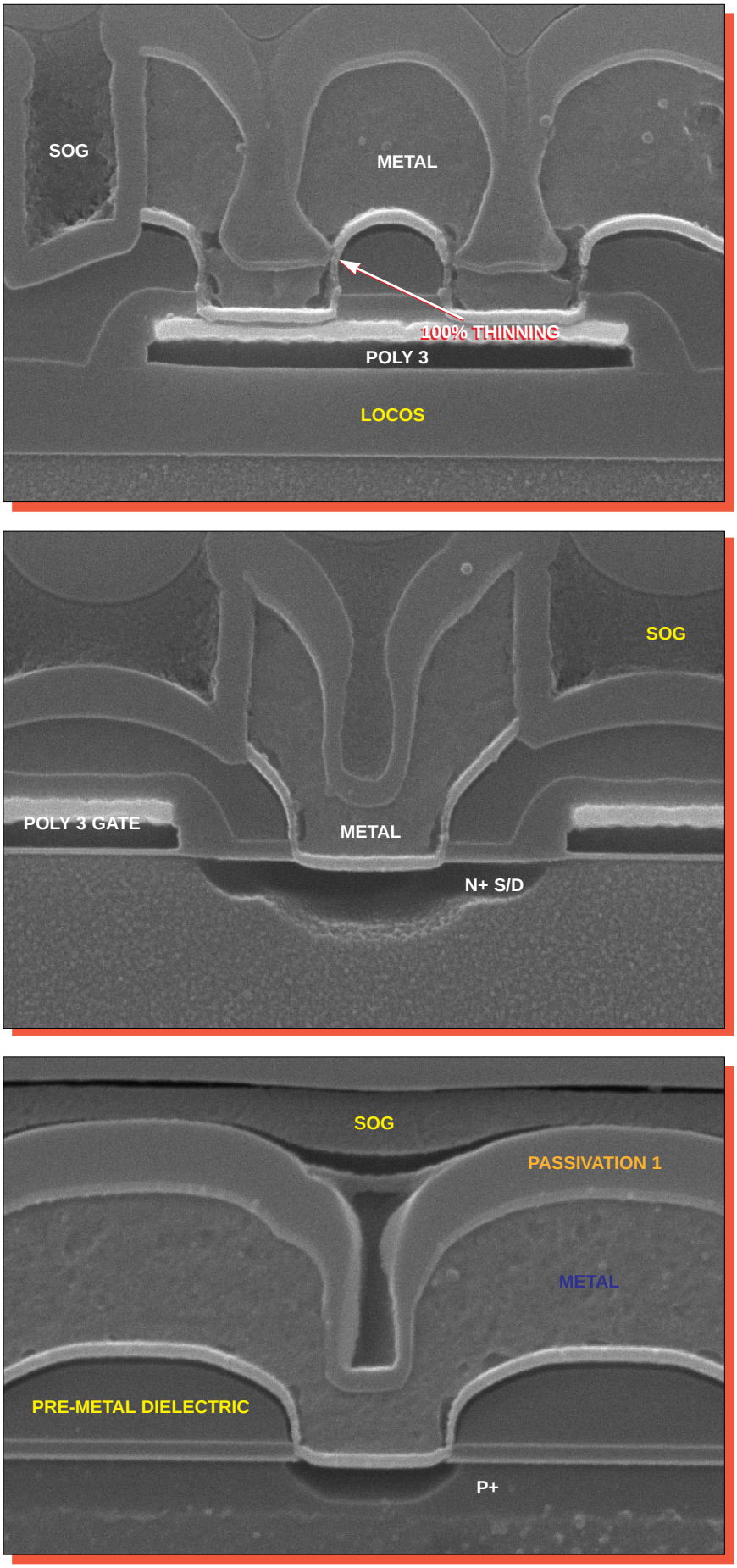
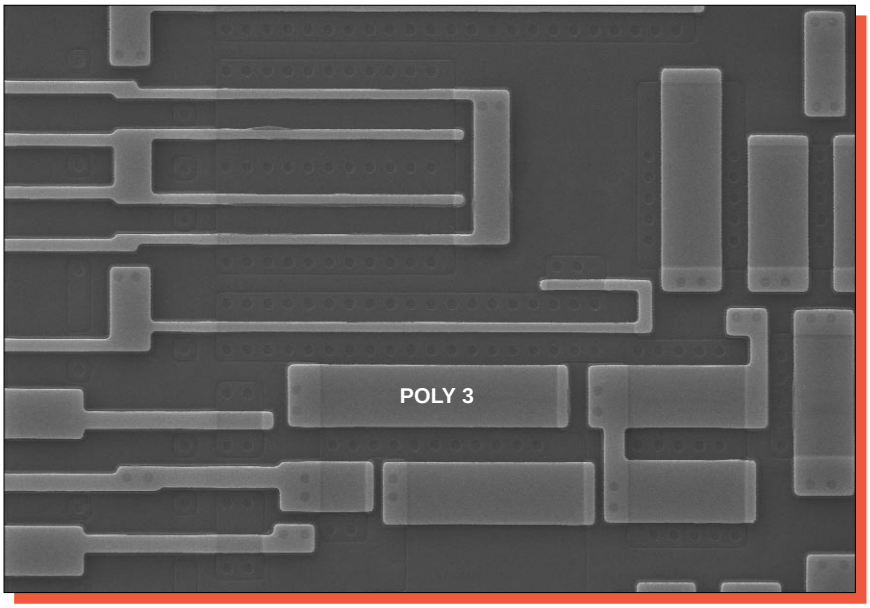
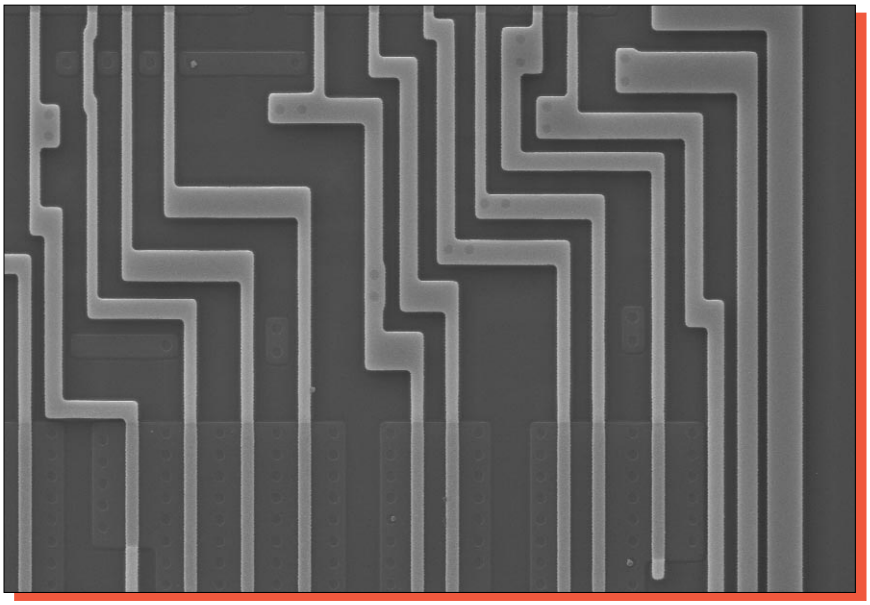


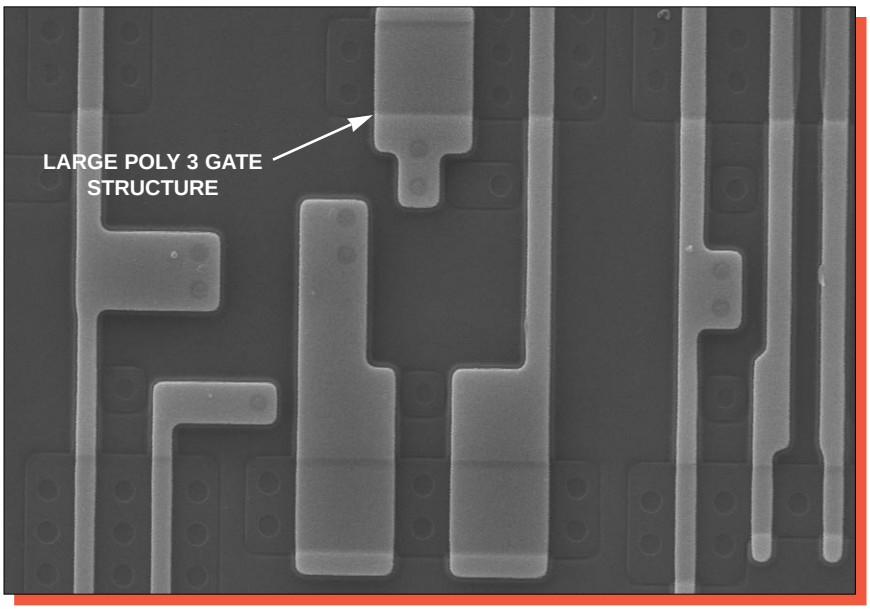
Figure 13. SEM section views of typical metal contacts. Mag. 26,000x.



Mag. 1600x

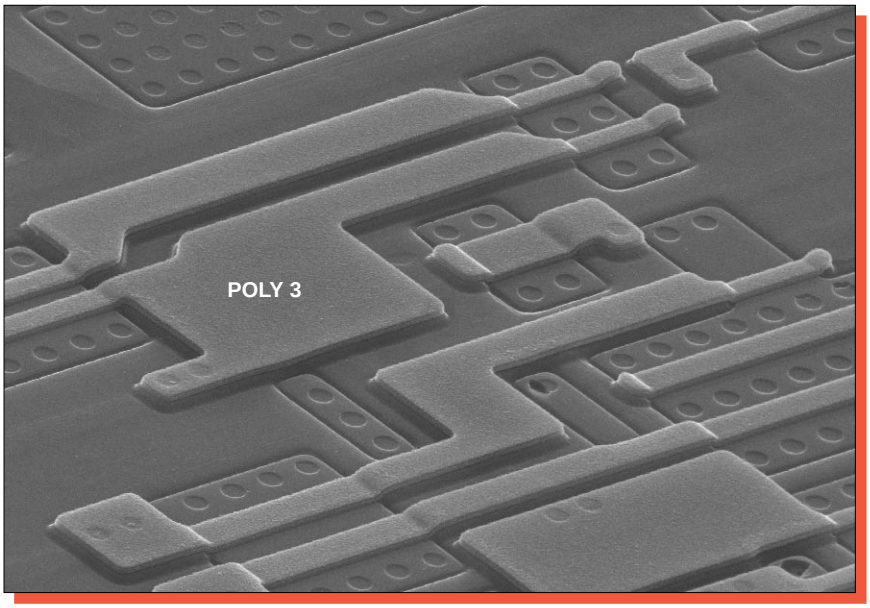


Mag. 1600x

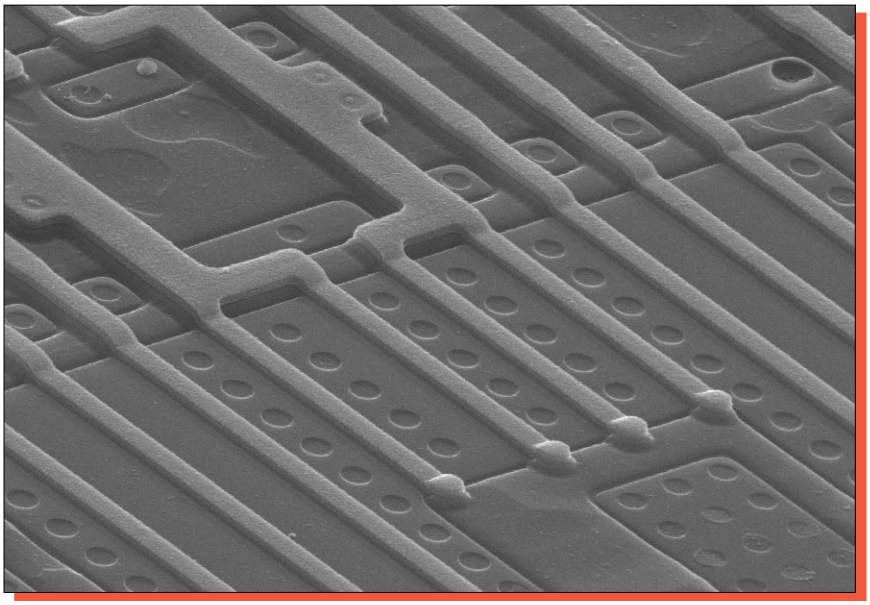


Mag. 3200x

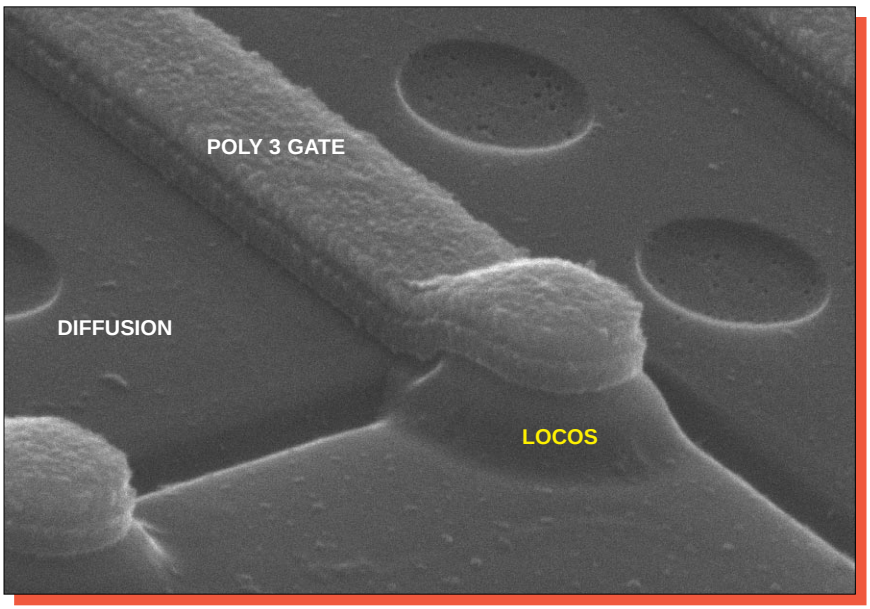
Figure 14. Topological SEM views of poly 3 patterning. 0°.



Mag. 4000x

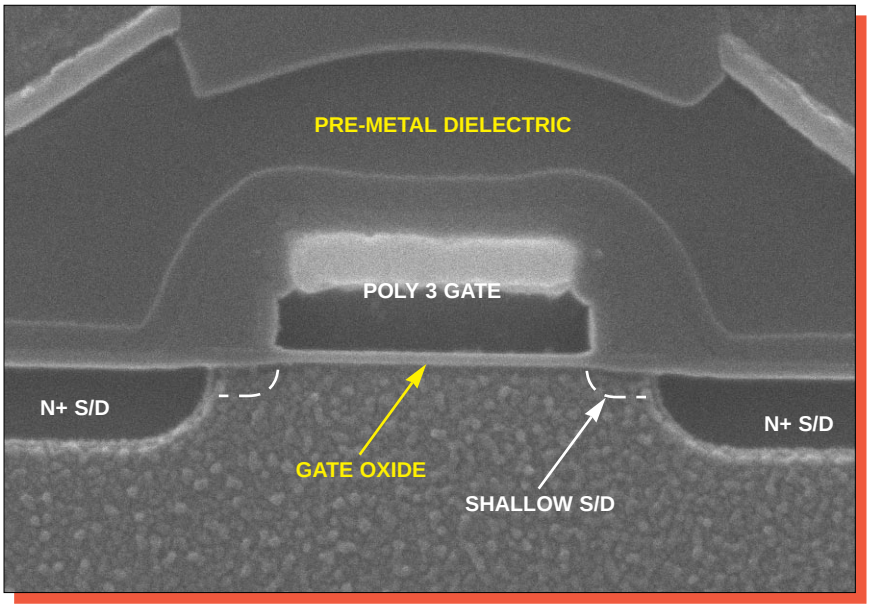


Mag. 5000x

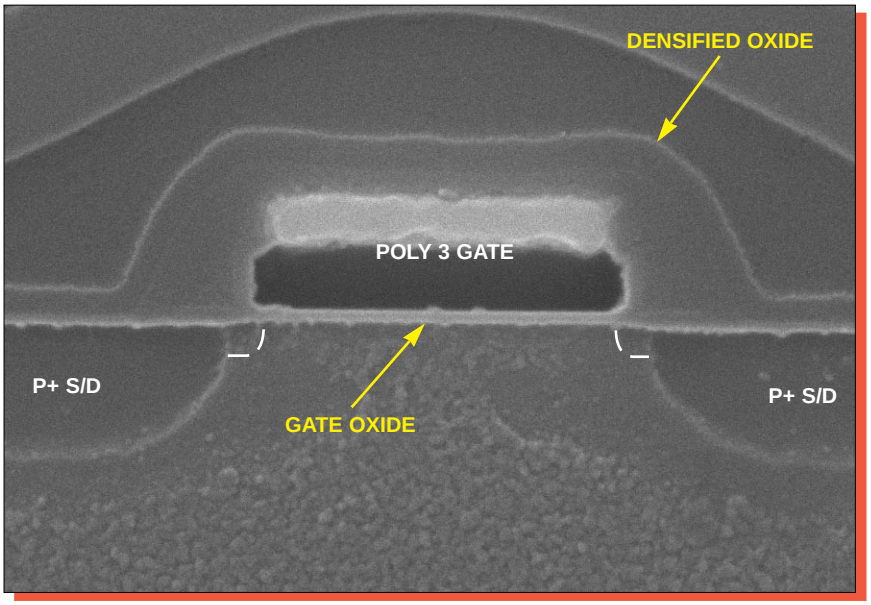


Mag. 30,000x

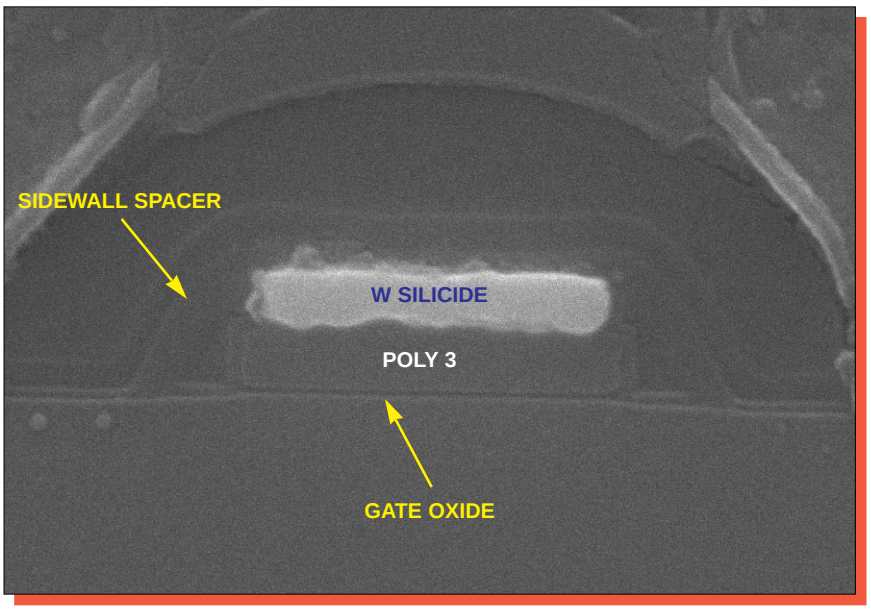
Figure 15. Perspective SEM views of poly 3 coverage. 60°.



N-channel



P-channel



glass etch

Figure 16. SEM section views of typical transistors. Mag. 52,000x.

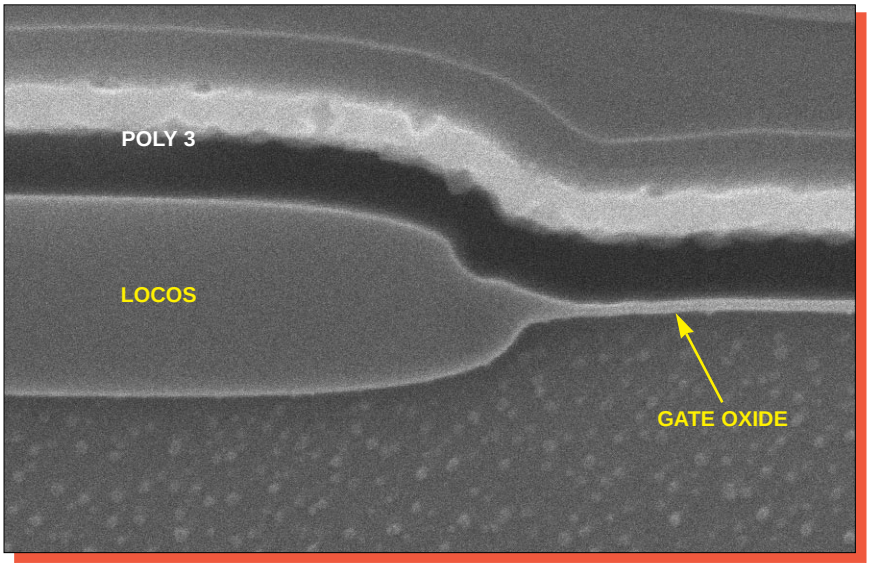
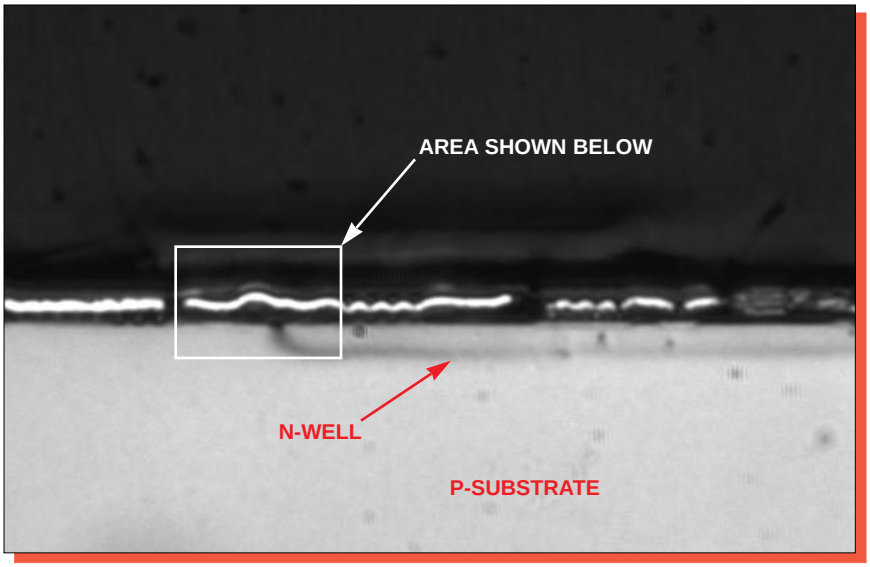
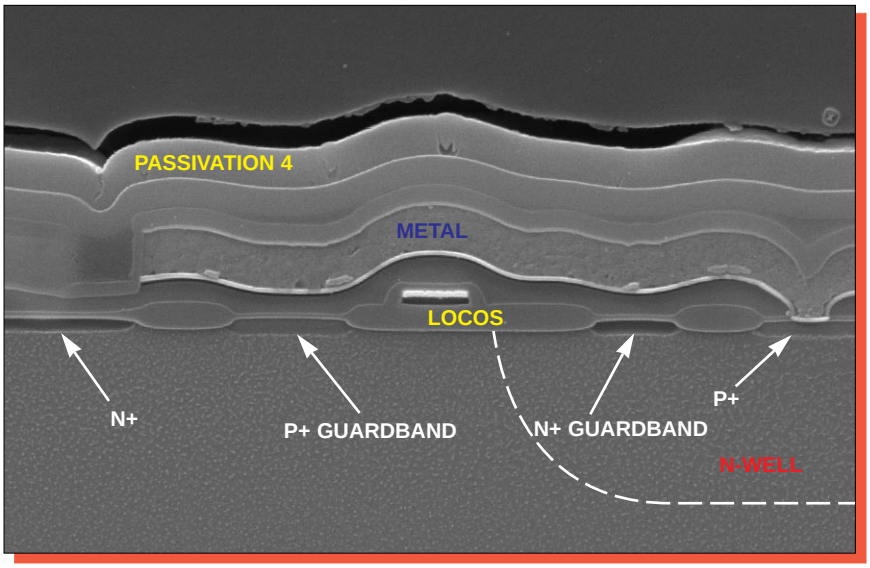


Figure 17. SEM section view of a typical birdsbeak. Mag. 52,000x.

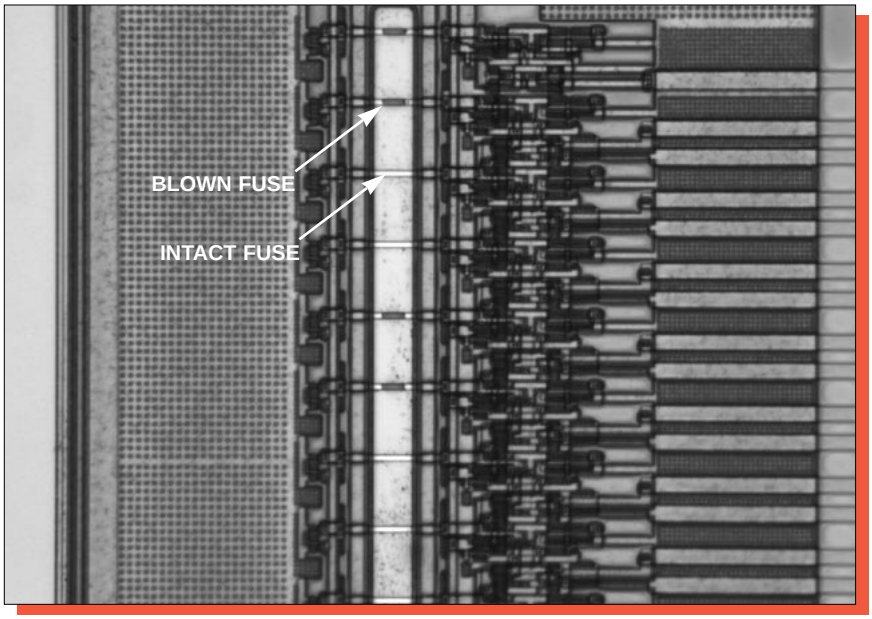


Mag. 1500x

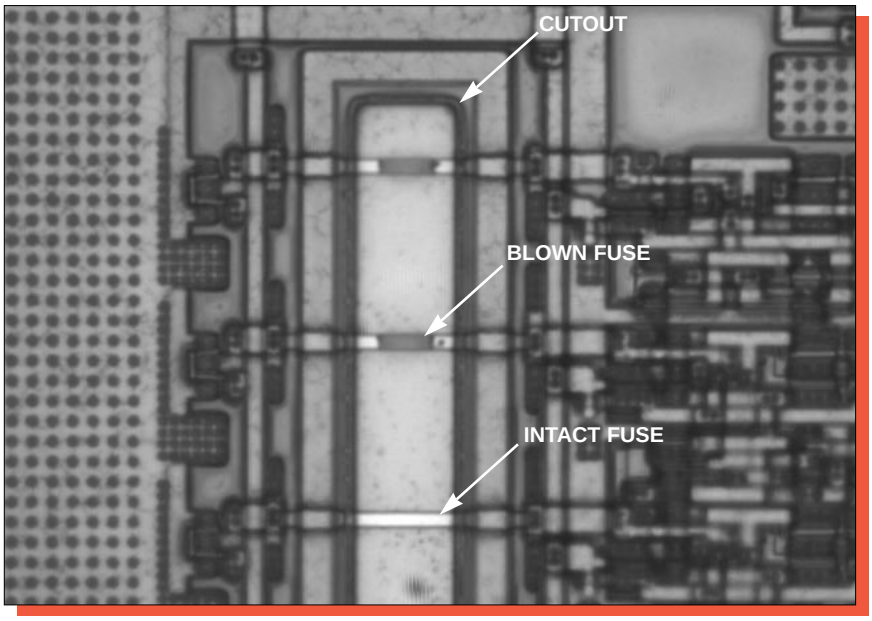


Mag. 6500x

Figure 18. Section views illustrating well structure.

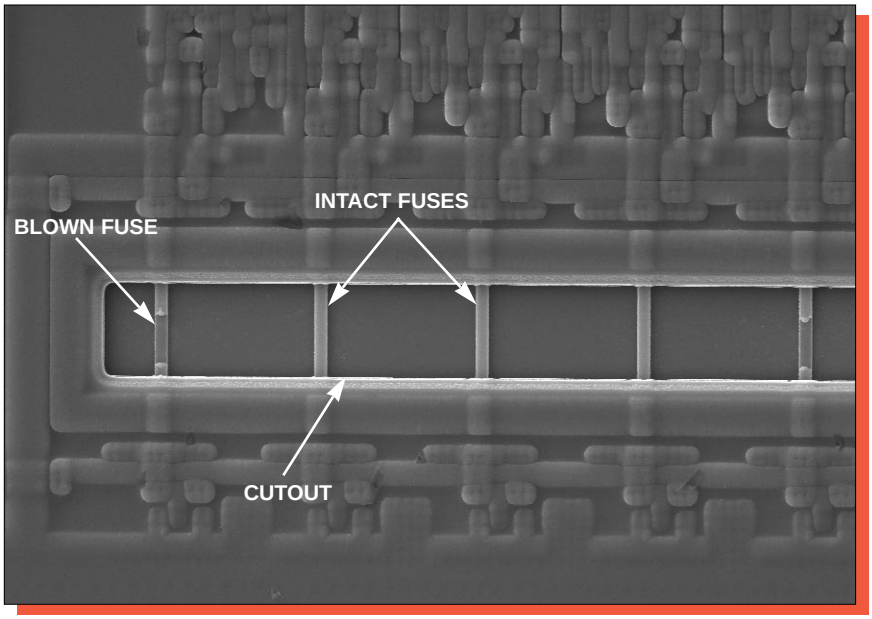


Mag. 350x

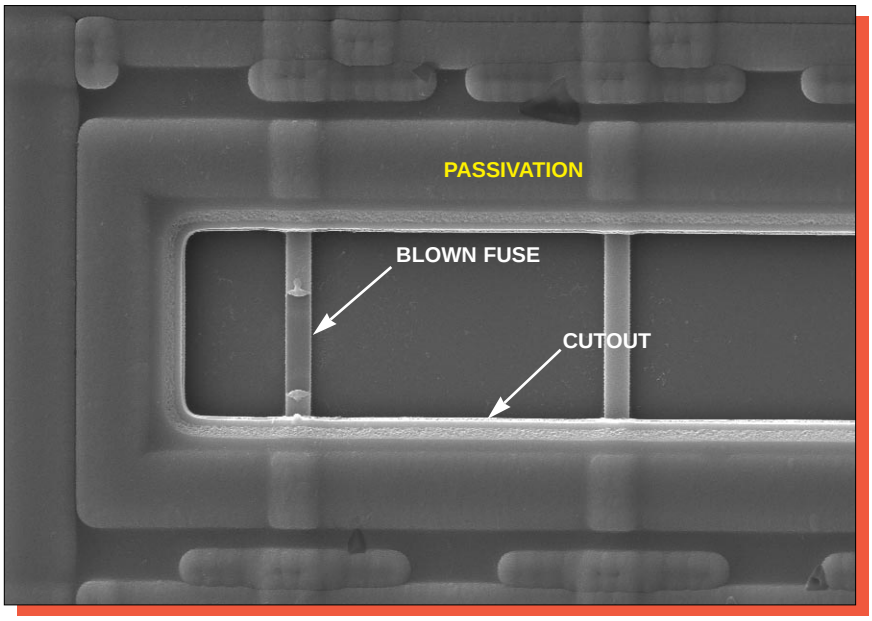


Mag. 860x

Figure 19. Optical views of typical fuses.

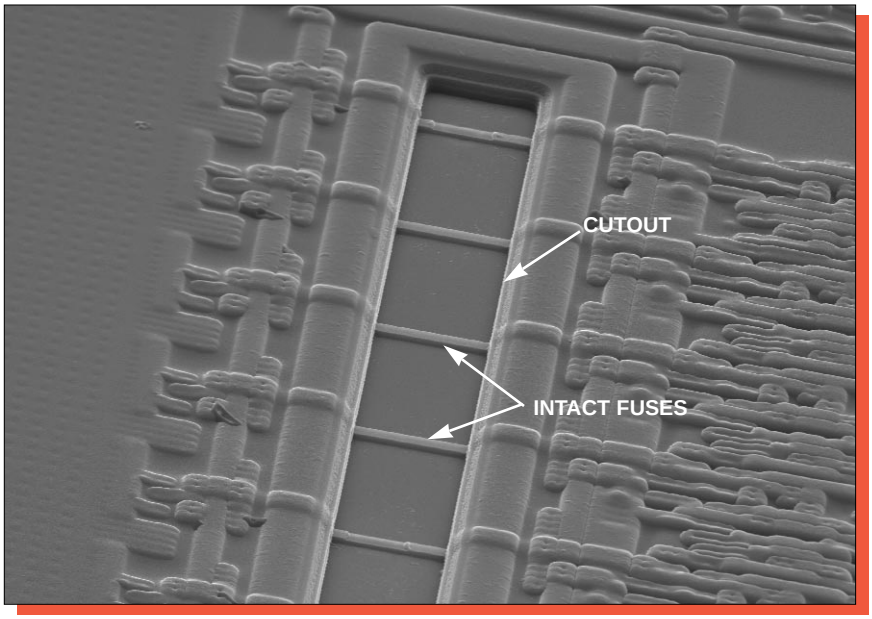


Mag. 810x

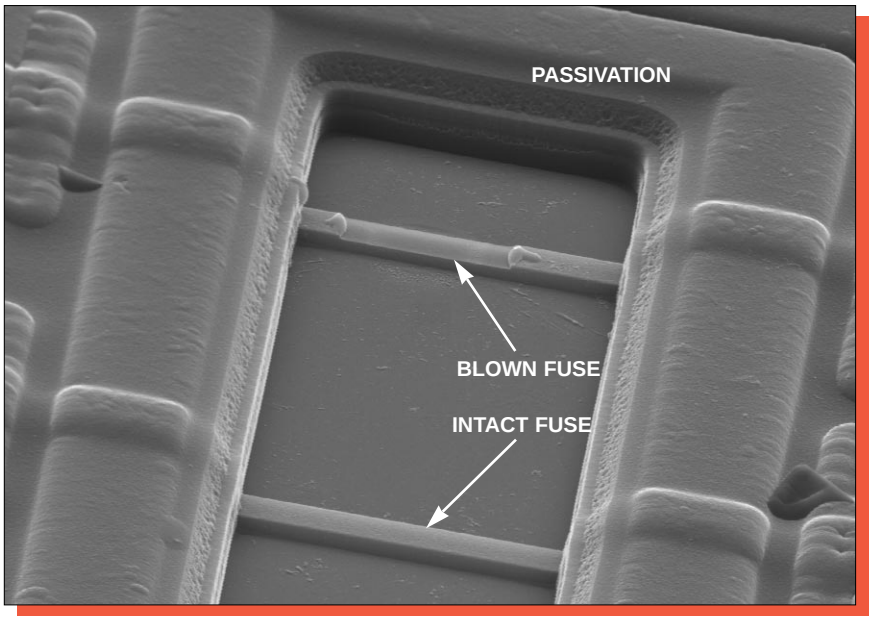


Mag. 1600x

Figure 20. Topological SEM views of typical fuses. 0°.

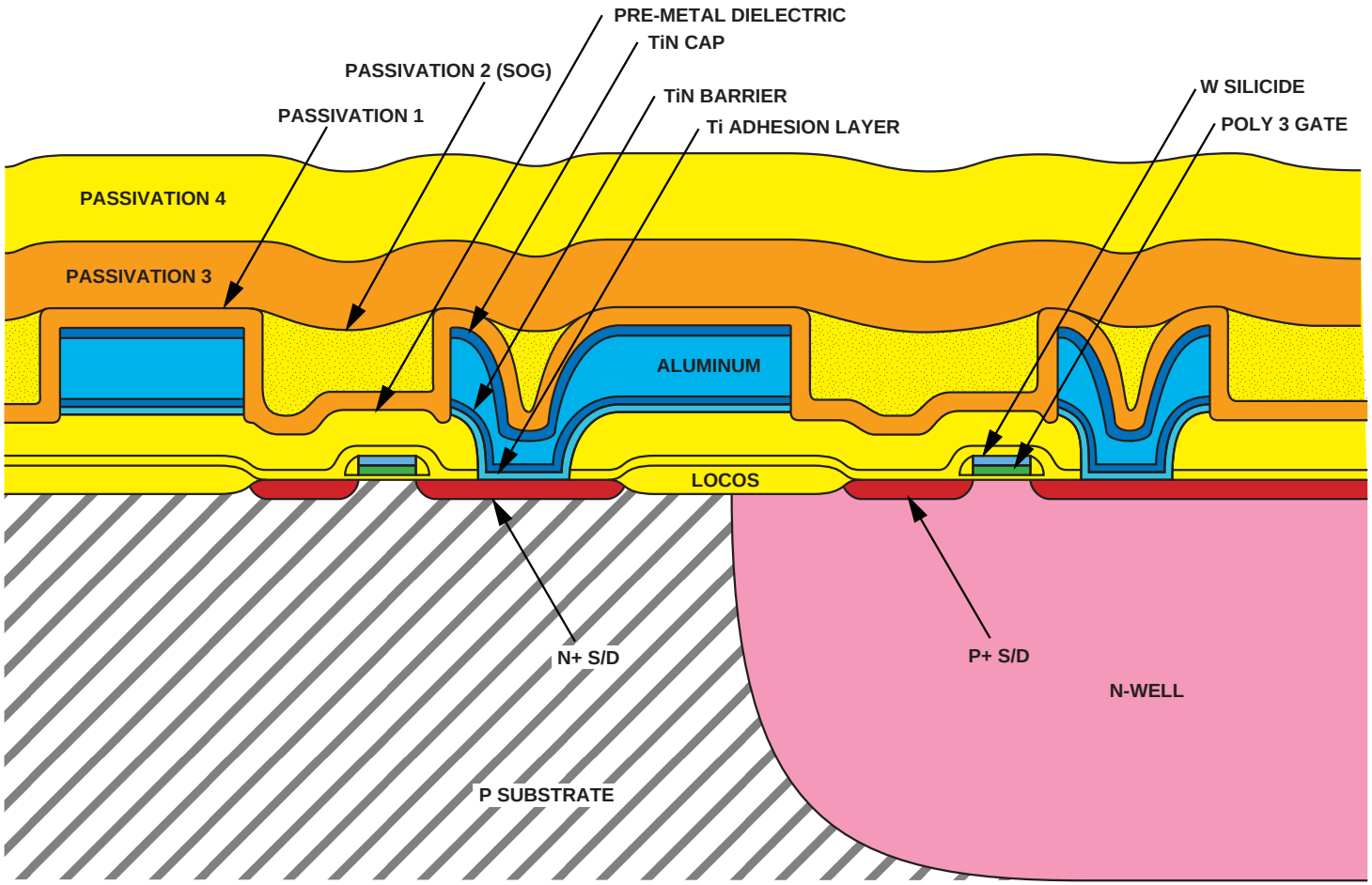


Mag. 1000x



Mag. 3000x

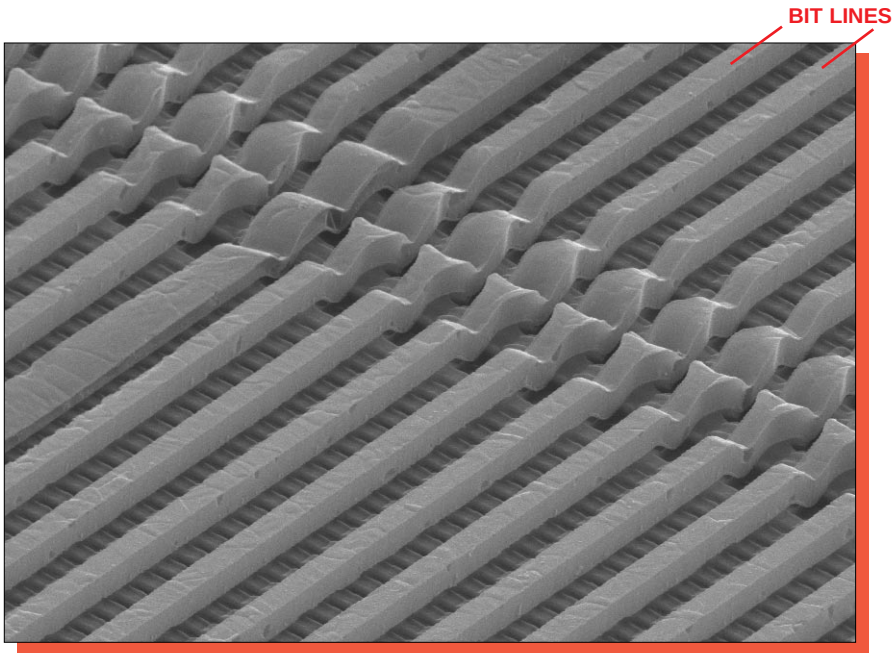
Figure 21. Perspective SEM views of typical fuses. 60°.



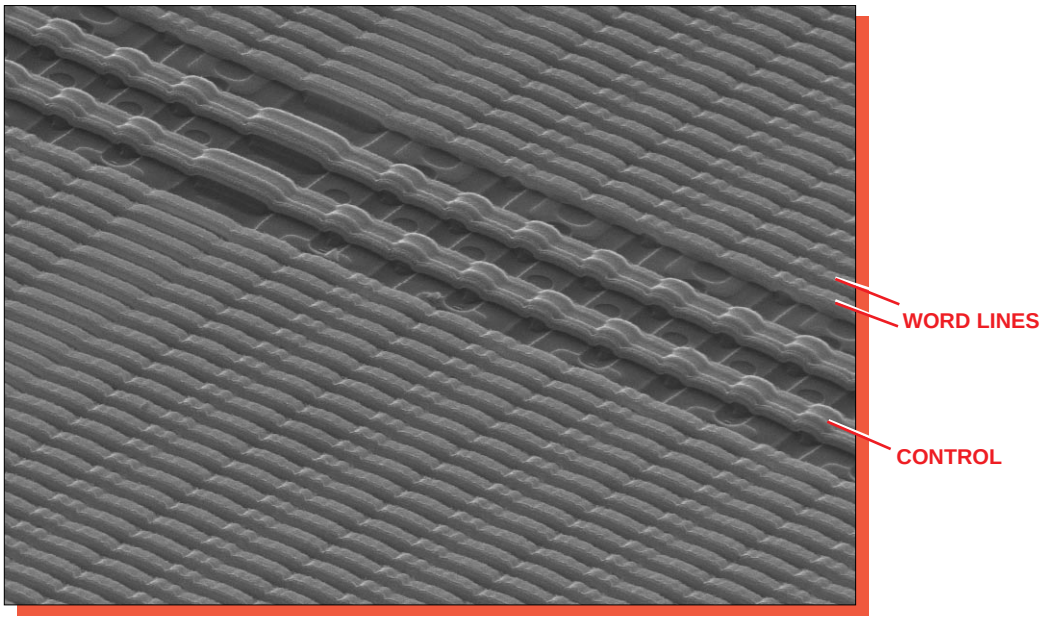
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 22. Color cross section drawing illustrating device structure.

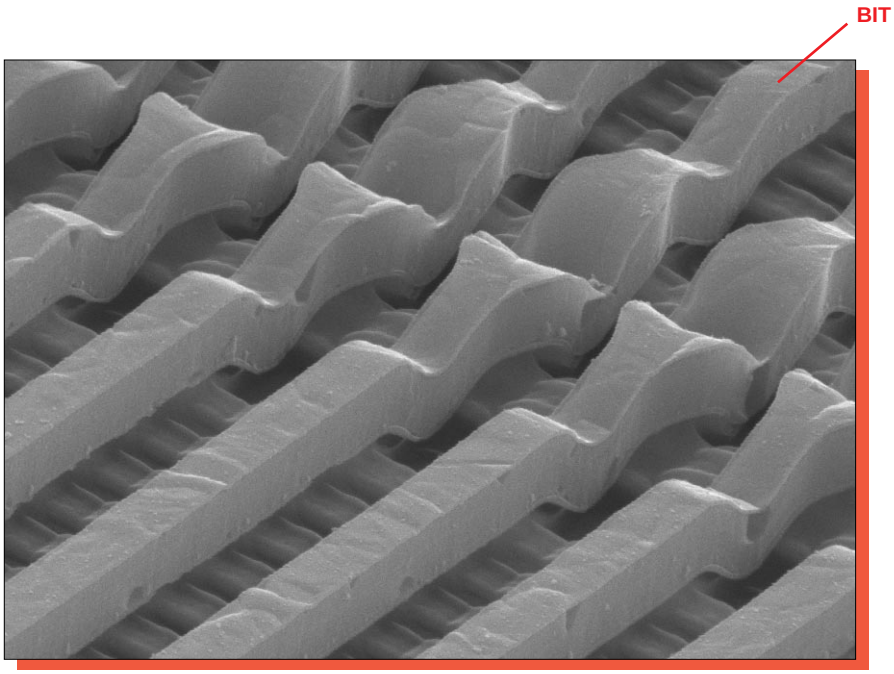


metal

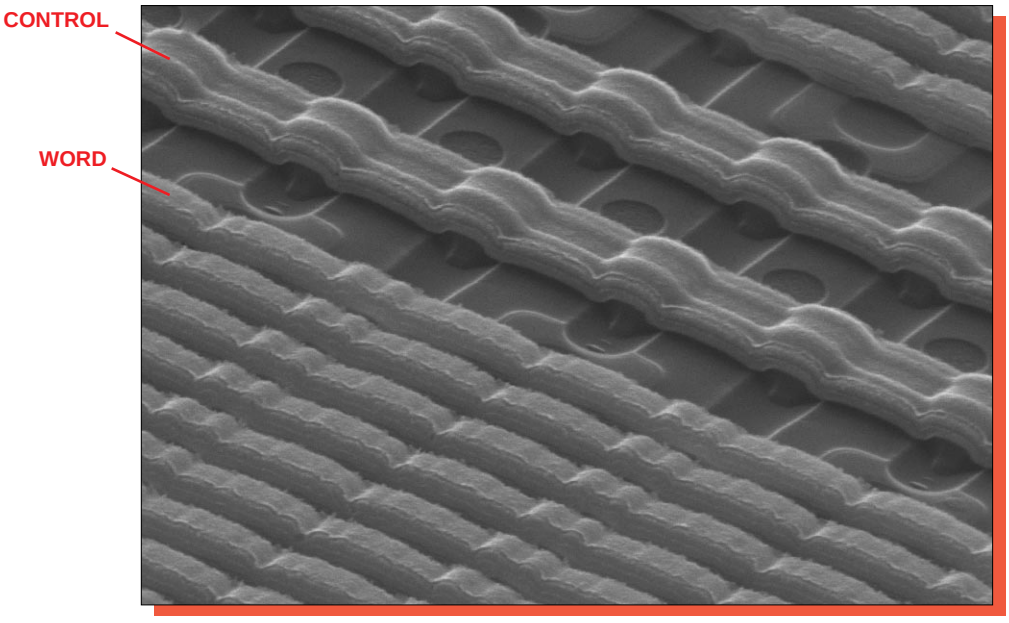


poly 3

Figure 23. Perspective SEM views of the NAND EPROM cell array. Mag. 4200x, 60°.

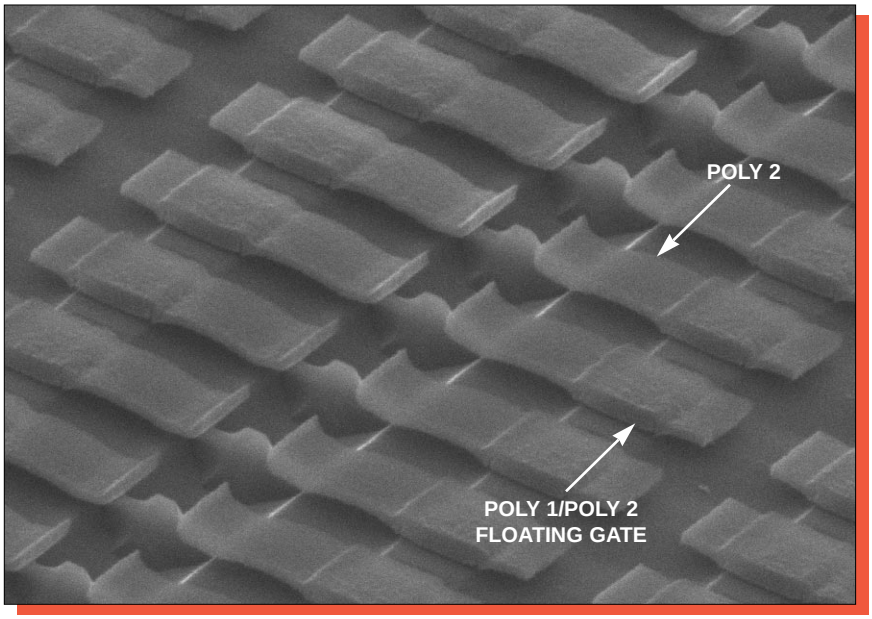


metal

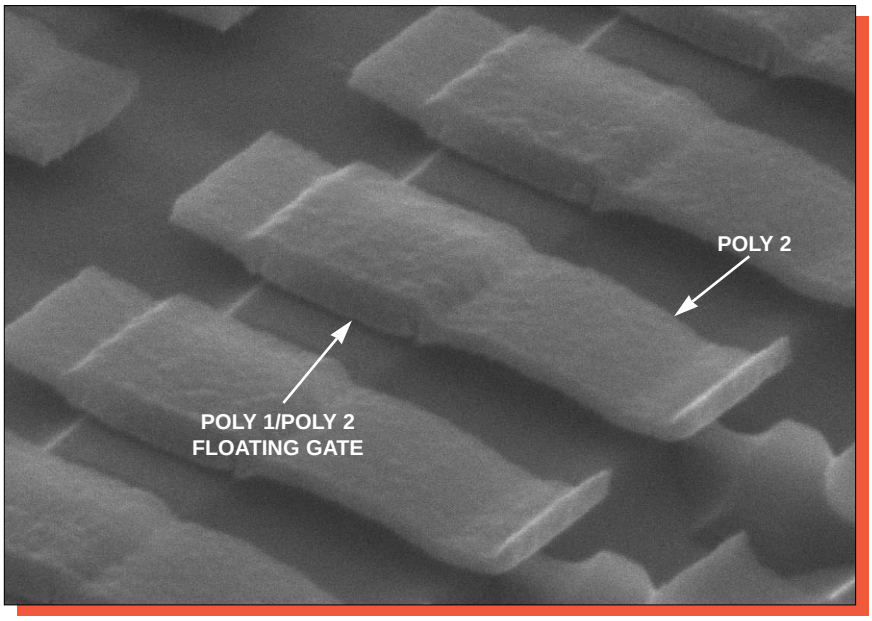


poly 3

Figure 24. Perspective SEM views of the NAND EPROM cell array. Mag. 10,000x, 60°.

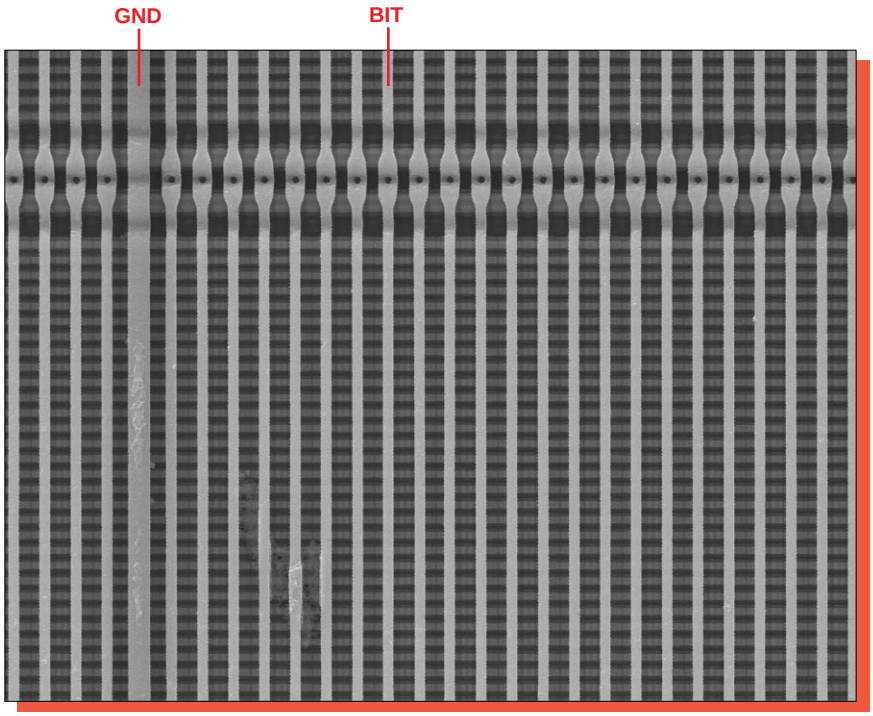


Mag. 20,000x

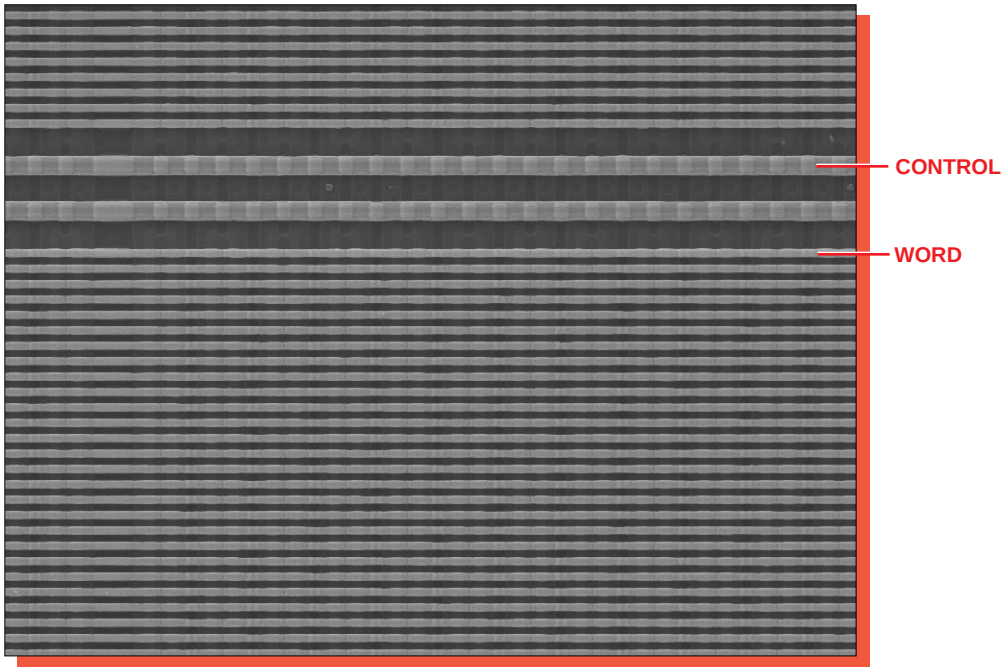


Mag. 40,000x

Figure 25. Detailed perspective SEM views of the NAND EPROM cell array (word lines removed). 60°.

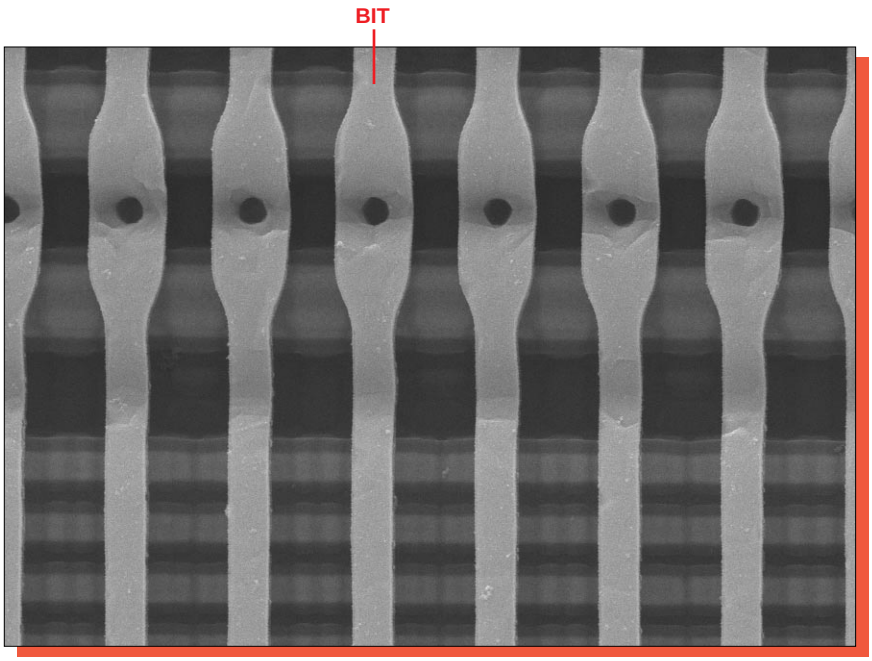


metal

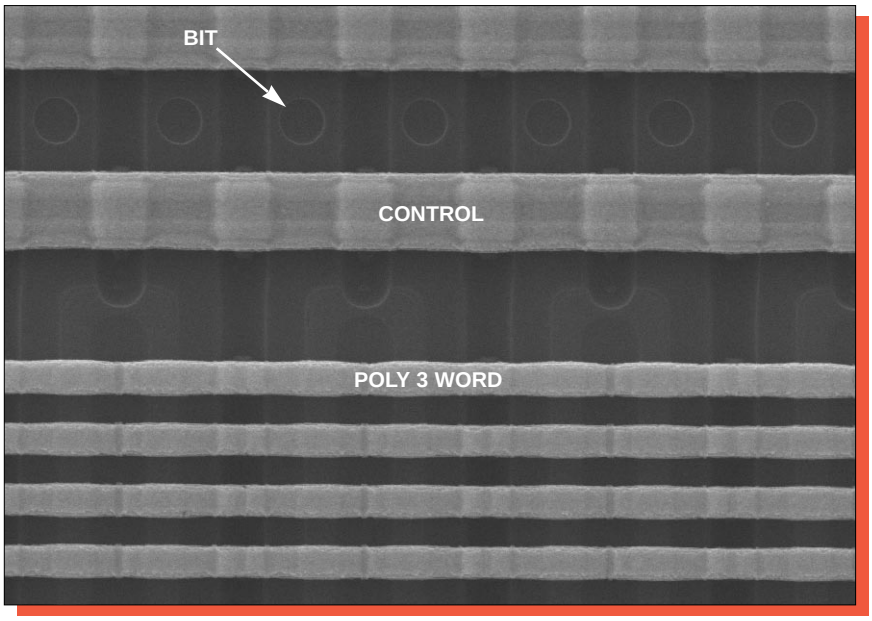


poly

Figure 26. Topological SEM views of the NAND EPROM cell array. Mag. 1600x, 0°.

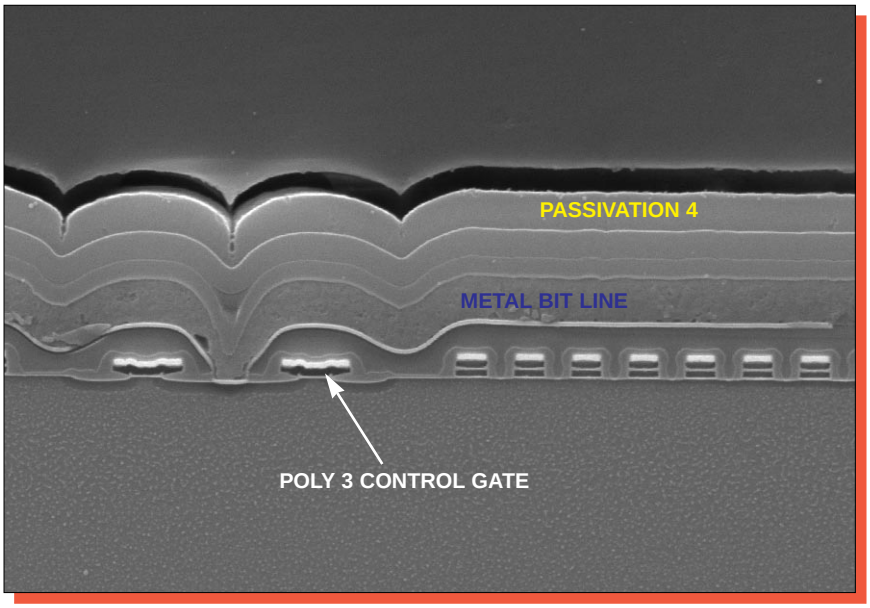


metal

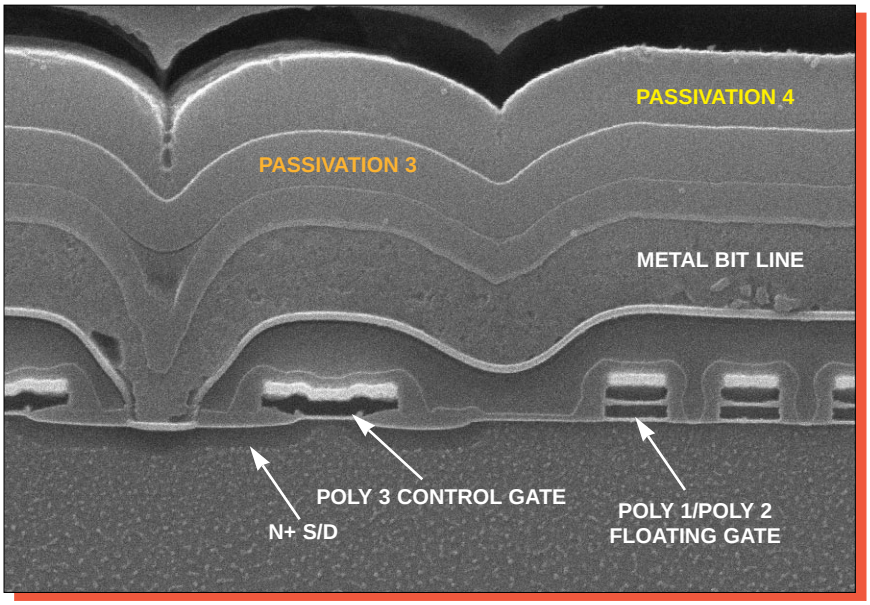


poly

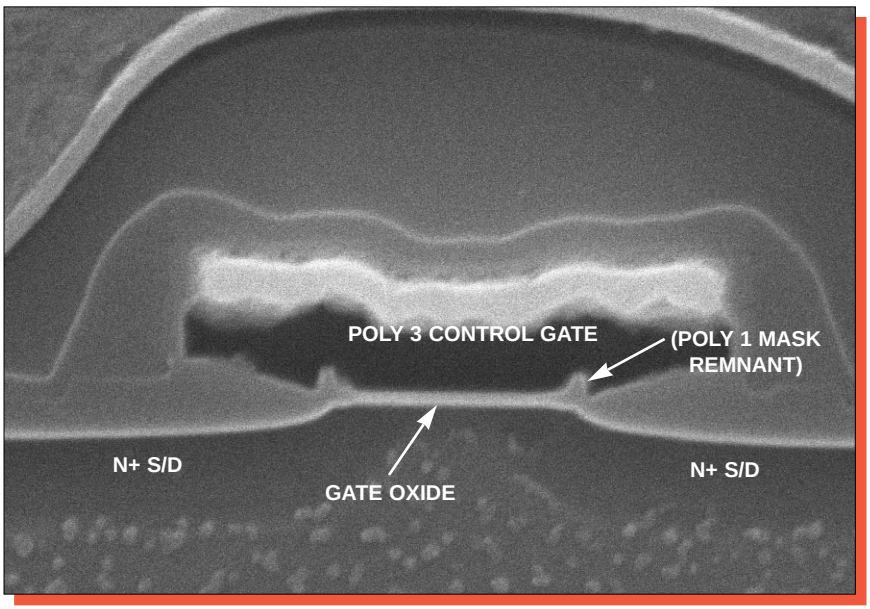
Figure 27. Topological SEM views of the NAND EPROM cell array. Mag. 6500x, 0°.



Mag. 6500x

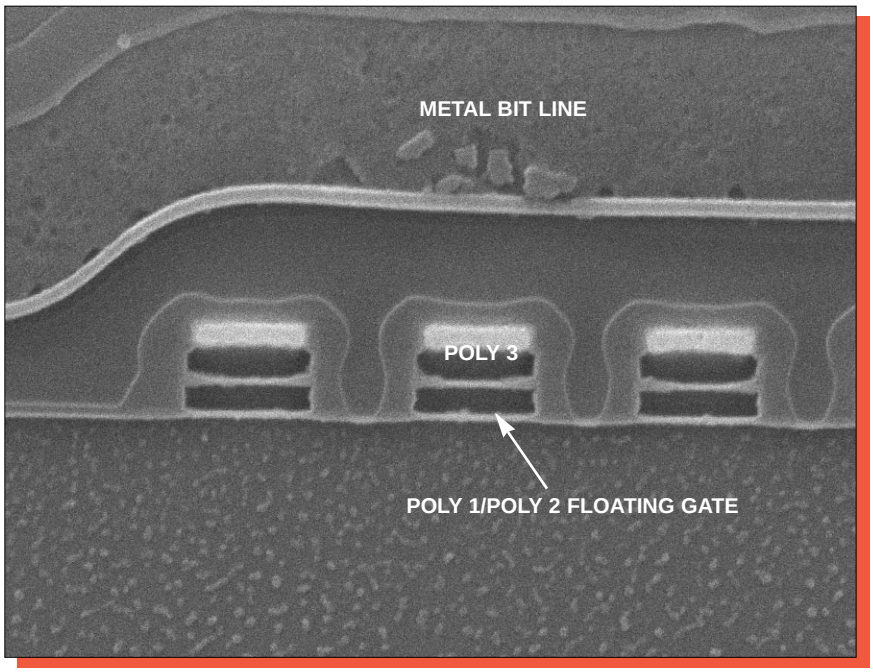


Mag. 13,000x

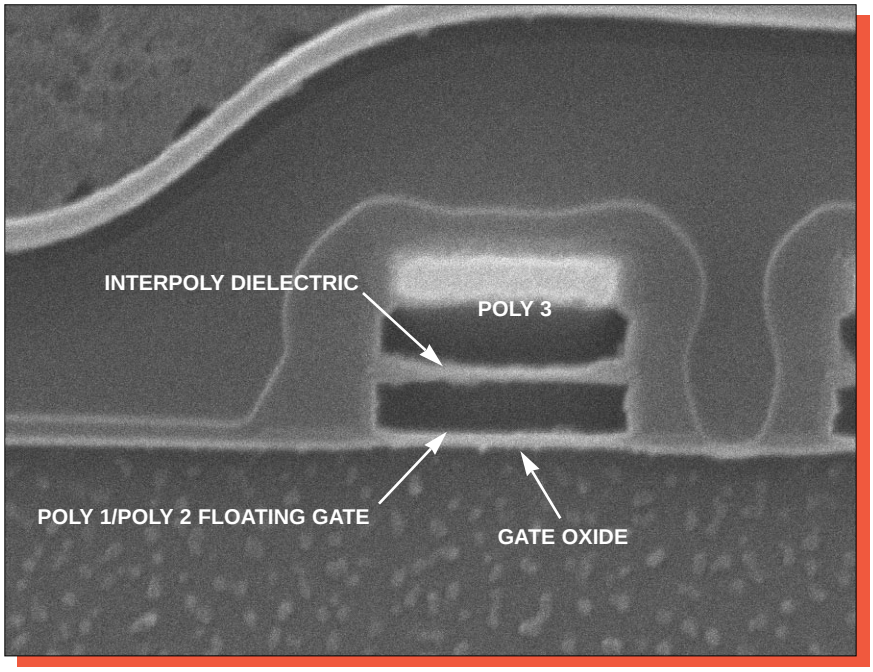


Mag. 52,000x

Figure 28. SEM section views of the NAND EPROM cell array (parallel to bit lines).

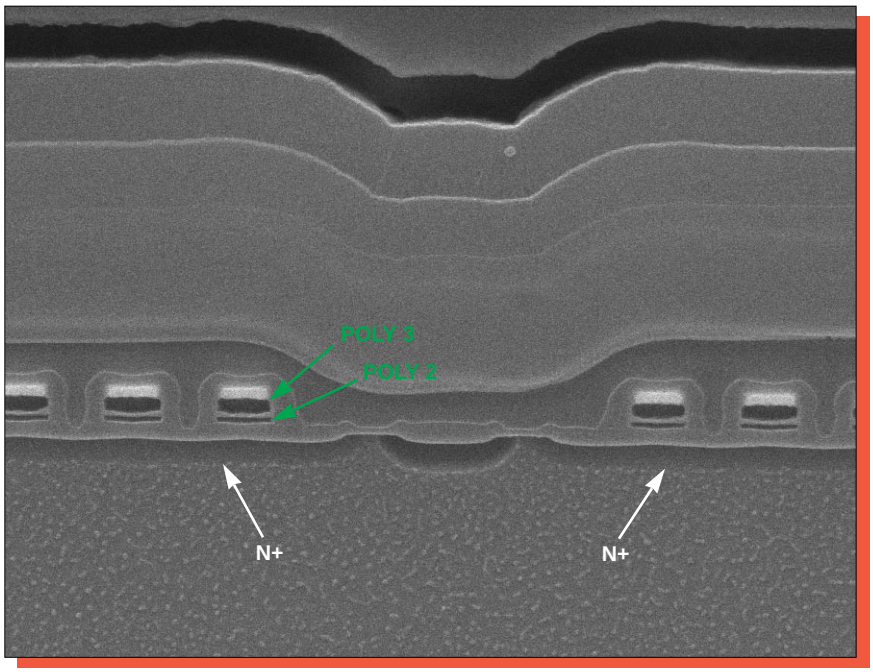


Mag. 26,000x

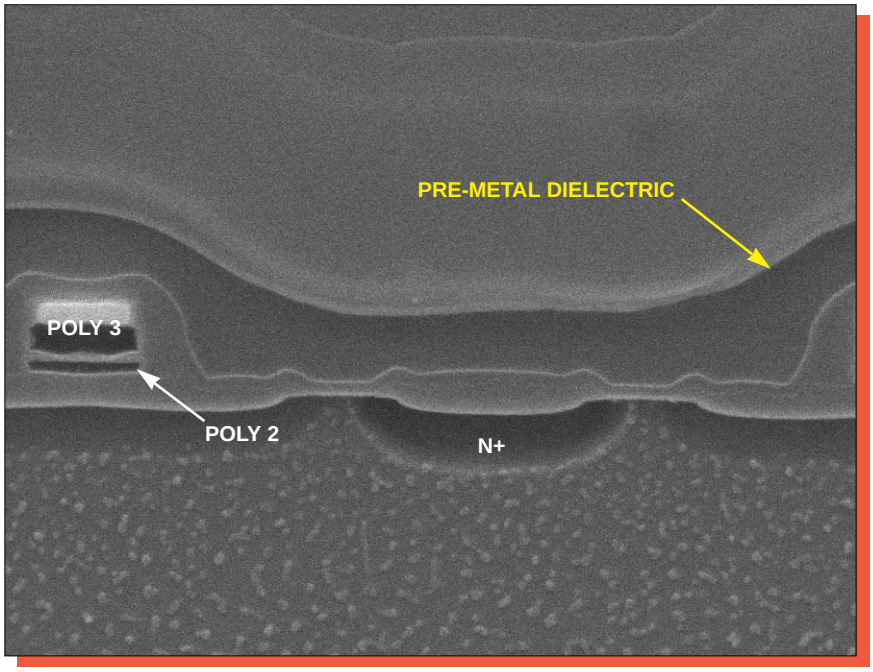


Mag. 52,000x

Figure 29. Detailed SEM views of the NAND EPROM cell array (parallel to bit lines).

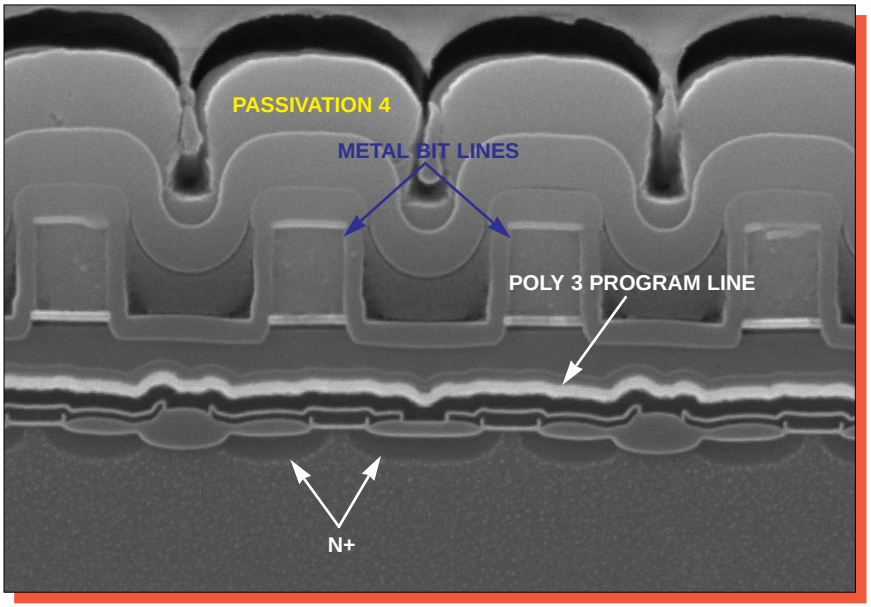


Mag. 13,000x

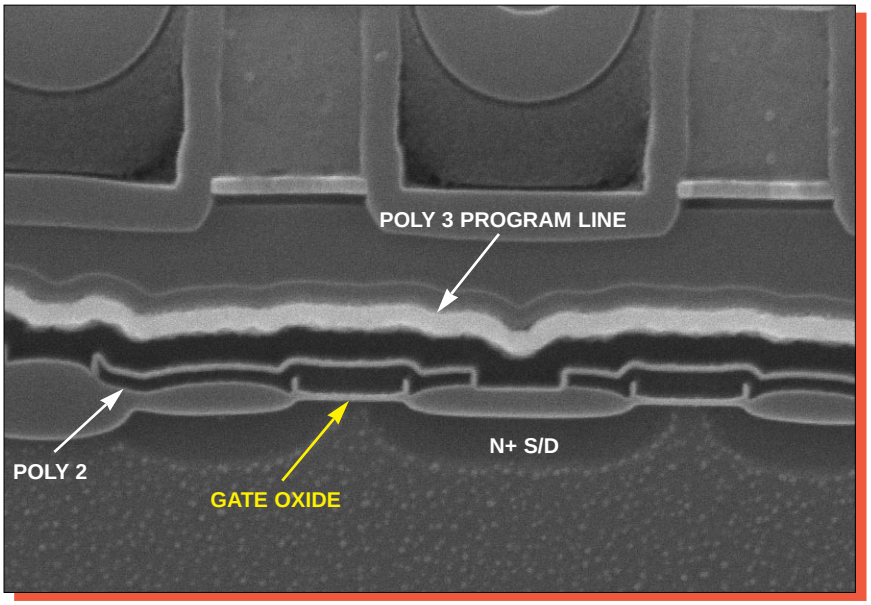


Mag. 26,000x

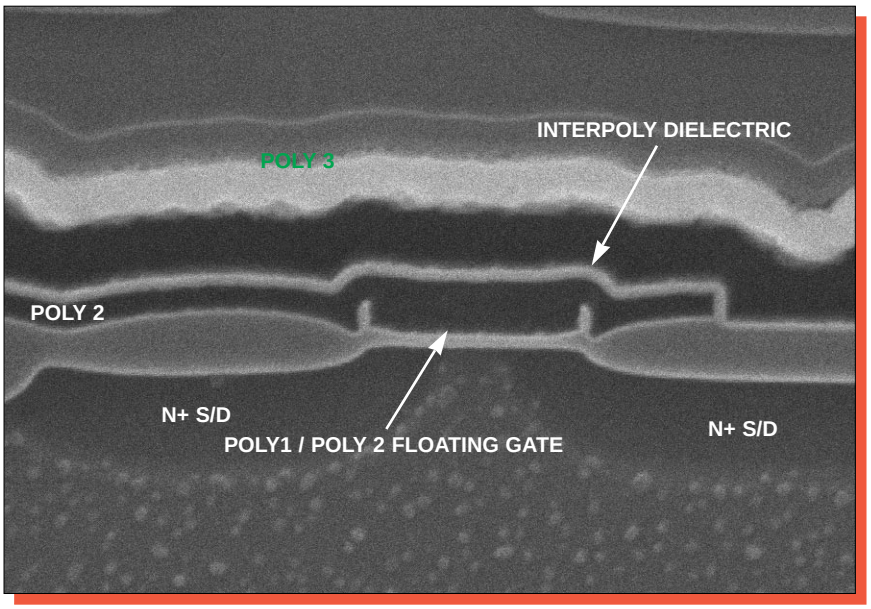
Figure 30. SEM section views of the NAND EPROM cell array between bit lines (parallel to bit lines).



Mag. 13,000x

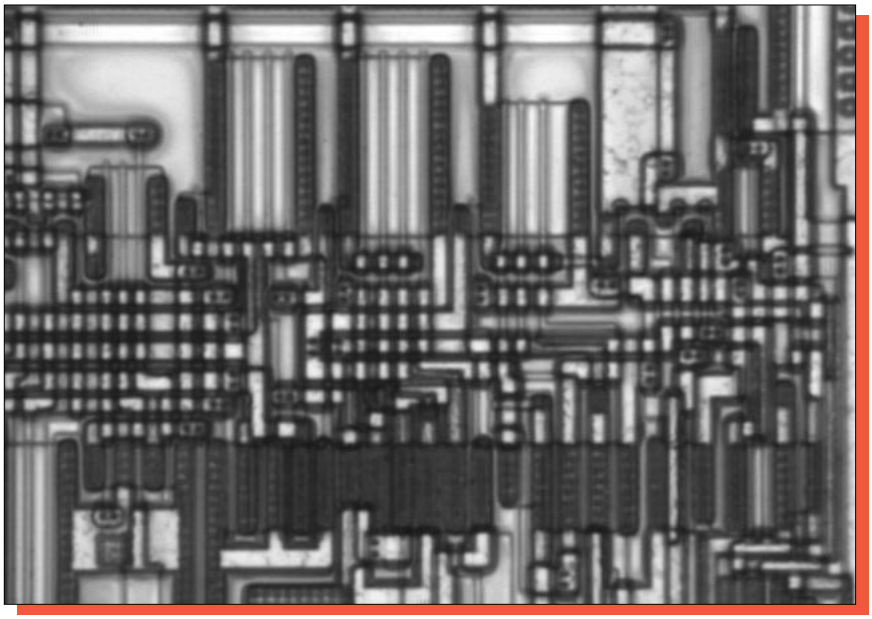


Mag. 26,000x

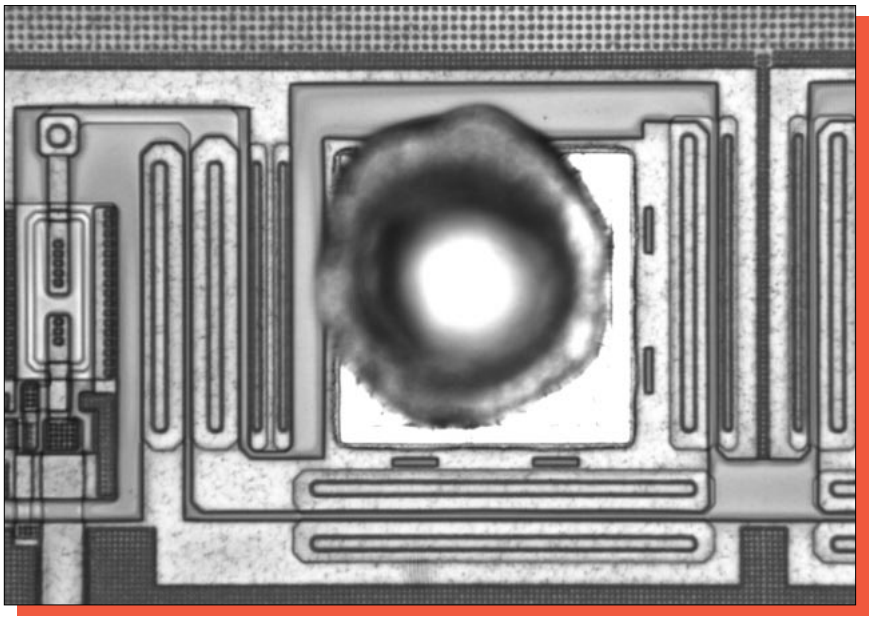


Mag. 52,000x

Figure 31. SEM section views of the NAND EPROM cell array (perpendicular to bit lines).

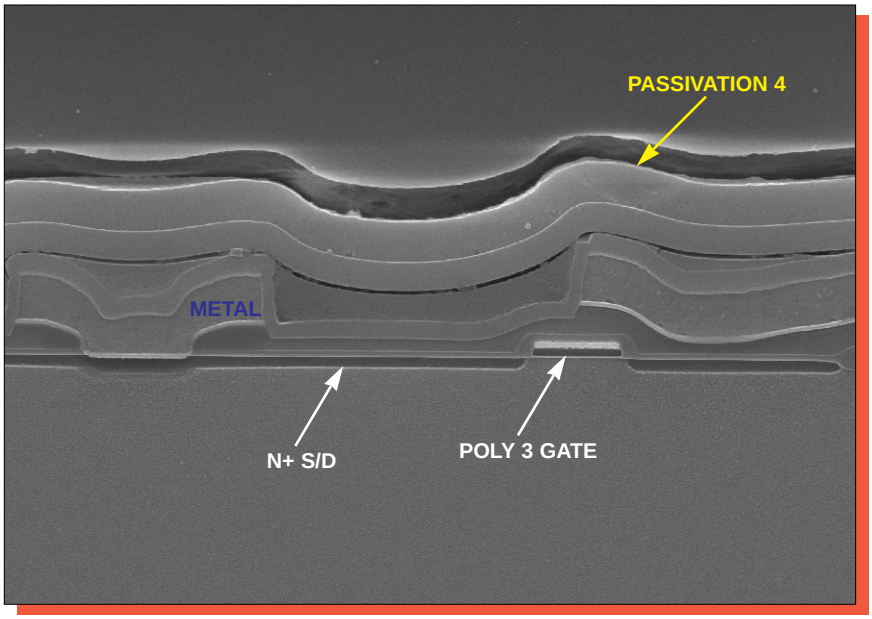


Mag. 820x

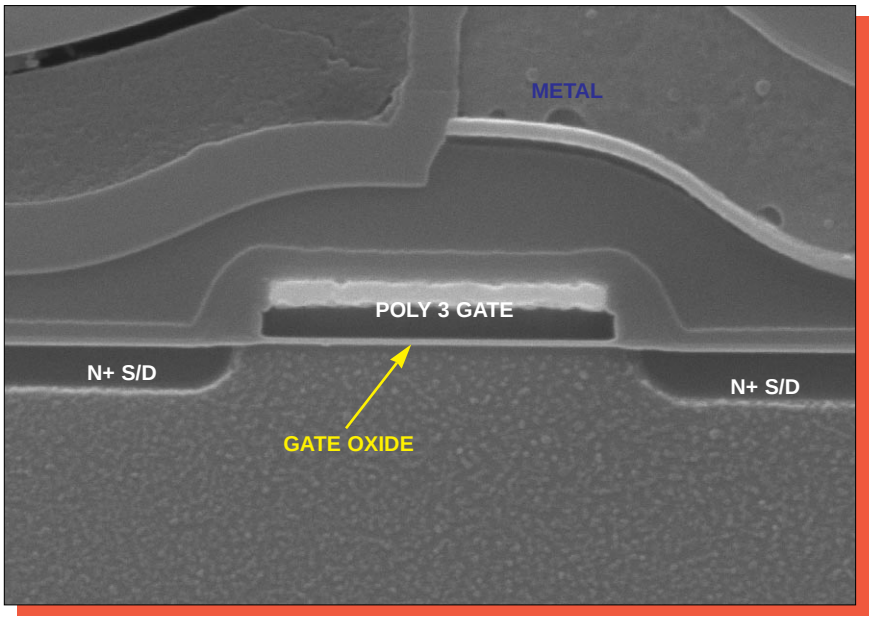


Mag. 410x

Figure 32. Optical views of typical circuitry and input protection.



Mag. 6500x



Mag. 26,000x

Figure 33. SEM section views illustrating typical I/O structure.