

## Construction Analysis

# Altera EPM7128SQC160-15 EPLD

Report Number: SCA 9712-569



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## **INTRODUCTION**

This report describes a construction analysis of the Altera EPM7128SQC160-15 PLD. One device packaged in 160-pin PQFP (plastic quad flat pack) with gull-wing leads for surface mount applications was provided. The part was date coded 9719.

## **MAJOR FINDINGS**

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Two-metal, twin-well, CMOS process.
- EEPROM cell programming with tunnel oxide windows for programming.
- Sub-micron gates (0.55 micron N-channel, 0.8 micron P-channel).

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **TECHNOLOGY DESCRIPTION**

### **Packaging/Assembly:**

- Device was encapsulated in a 160-pin plastic quad flat pack with gull-wing leads.
- Lead-locking provisions (anchors) at all pins and (holes) in paddle tie bar.
- Dimpled paddle for additional package strength.
- Sawn dicing (full depth).
- Silver (Ag) epoxy die attach.

### **Die Process:**

- Fabrication: Twin-well, CMOS, P substrate, selective oxidation process. No epi.
- Final passivation: A layer of silicon-nitride over silicon-dioxide.
- Metallization: Two levels of aluminum interconnect patterned by dry-etch techniques. A titanium-nitride (TiN) cap metal and a titanium-tungsten (TiW) barrier metal were employed with both metal levels. The aluminum layers were silicon doped but no copper was detected.
- Interlevel dielectric: Two layers of silicon-dioxide. A spin-on-glass (SOG) was used between these layers for planarization purposes. The first layer of silicon dioxide appeared to be undoped. No evidence of chemical-mechanical-planarization (CMP) was present.
- Pre-metal glass: A BPSG reflow glass over various densified oxides. It appeared to have been reflowed prior to contact cuts only.
- Polysilicon: A single layer of dry etched polycide (tungsten silicide on poly) formed all gates on the die.

## **TECHNOLOGY DESCRIPTION (continued)**

- Diffusions: Transistors were formed using an LDD process in which the oxide sidewall spacers were left in place. Implanted N+ and P+ sources/drains. Twin-wells were used in a P substrate. No epi was present.
- No buried contacts were employed on this device.
- Memory cells: The programmable array consisted of EEPROM cells (E<sup>2</sup> CMOS process). Metal 2 was used to form "piggyback" word lines. Metal 1 formed the bit 1, bit 2, enable and word interconnect lines. Poly formed the word lines, all gates and one plate of the capacitor. A thin tunnel-oxide window was utilized in the cell design. An N+ implant was present beneath the tunnel oxide device.

## ANALYSIS RESULTS I

### Assembly:

### Figures 1 - 2

**Questionable Items:** None.

### **General Items:**

- 160-pin PQFP packages with gull-wing leads.
- Overall package quality: Normal. No serious defects were found on the external or internal portions of the package.
- Leadframe: Lead-locking provisions (anchors) were present at all pins (holes) were present in the header tie bar.
- Paddle: A dimpled paddle was employed for additional package strength.
- Die attach: The die was attached to the paddle with silver-epoxy of good quality.
- Die dicing: Die separation was by sawing with normal quality workmanship. No cracks or large chipouts were found in the die.

## ANALYSIS RESULTS II

### Die Process:

Figures 3 - 29

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Two-metal, twin-well, CMOS process.
- EEPROM cell programming with tunnel oxide windows for programming.
- Sub-micron gates (0.55 micron N-channel, 0.8 micron P-channel).

### **General Items:**

- Fabrication process: Selective oxidation CMOS using twin-wells in a P substrate. No epi was present.
- Process Implementation: Die layout was clean and efficient. Alignment/registration was good at all levels and no damage or contamination was found.
- Final passivation: A layer of silicon-nitride over silicon-dioxide. Passivation extended in scribe lane covering all metal lines.
- Metallization: Two levels of silicon-doped aluminum interconnect (no copper detected). A titanium-nitride (TiN) cap metal and a titanium-tungsten (TiW) barrier metal was employed with each metal level.
- Metal patterning: Both layers were defined by dry-etch techniques. Definition was normal for both layers.
- Metal defects: No voiding or notching of the metals was found. Silicon nodules found following the removal of aluminum were small and well distributed. No problems were noted.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS II (continued)**

- Metal step coverage: Metal 2 aluminum thinned up to 70 percent at via edges. Metal 1 aluminum thinned up to 80 percent at contact edges; however, total metal 1 thinning including barrier was typically 70 percent.
- Vias and contacts: Metal 2 vias were slightly over-etched into the metal 1 cap (Figure 12). Metal 1 contacts were slightly over-etched at diffusion contacts (Figure 17). Neither condition appeared to present an area of concern.
- Interlevel dielectric: The dielectric between the two metal levels consisted of two layers of silicon-dioxide with a spin-on-glass (SOG) employed between for planarization purposes. The first layer of silicon-dioxide appeared to be undoped. No problems were noted.
- Pre-metal glass: The glass under metal 1 consisted of a BPSG reflow glass which was apparently reflowed prior to contact cuts only. This deposited glass was located over various densified oxides. No problems were found in any of the glass layers.
- Polysilicon: A single layer of polycide (tungsten silicide on poly) formed all gates. Definition was by a dry etch of good quality.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeak. A step was present in the field oxide indicating a twin-well process was used.
- Diffusions: Transistors were formed using an LDD process in which the oxide sidewall spacers were left in place. Implanted N+ and P+ sources/drains were employed. Definition was normal and no problems were present. Diffusions were not silicided.
- Wells: Twin-wells in a P substrate. No problems were apparent.
- Epi: No epi was used. No substrate defects were found.
- Buried contacts: No buried contacts were used on this device.

## **ANALYSIS RESULTS II (continued)**

- Memory cells: The programmable array consisted of EEPROM cells (E<sup>2</sup> CMOS process). Metal 2 was used to form "piggyback" word lines. Metal 1 formed the bit 1, bit 2, enable and word interconnect lines. Poly formed the word lines, all gates and one plate of the capacitor. A thin tunnel-oxide window was utilized in the cell design. An N+ implant was present beneath the tunnel oxide device. Cell size was 5.5 x 13.5 microns and cell area was 74 microns<sup>2</sup>. One of the eight array blocks measured 20 x 60 mils (1200 mils<sup>2</sup>).

## **PROCEDURE**

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

Passivation removal and inspect metal 2

Metal 2 removal and inspect vias

Delayer to metal 1 and inspect

Aluminum 1 removal and inspect barrier

Delayer to poly/substrate and inspect poly structures and die surface

Die material analysis

Die sectioning (90° for SEM)\*

Measure horizontal dimensions

Measure vertical dimensions

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

Package integrity	N
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	G
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)

Die surface integrity:

Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity	N
Metal registration	G
Contact coverage	G
Contact registration	G

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## PACKAGE MARKINGS

### TOP

ALTERA  
MAX  
EPM7128SQC160-15  
BDB099725

### BOTTOM

NCB90627  
9719 A N

## DIE MATERIAL ANALYSIS

Final passivation:	Silicon-nitride over silicon-dioxide.
Metallization 2:	Silicon-doped aluminum* (no copper detected).** A titanium-nitride cap and a titanium-tungsten barrier were employed.
Interlevel dielectric:	Two layers of silicon-dioxide with a spin-on glass.
Metallization 1:	Silicon-doped aluminum* (no copper detected).** A titanium-nitride cap and a titanium-tungsten barrier were employed.
Intermediate glass:	BPSG reflow glass.
Polycide metal:	Tungsten.

\*There is no known method to accurately determine the metal doping level on a finished die.

\*\*Detection limit 0.5 percent.

## HORIZONTAL DIMENSIONS

Die size:	5.0 x 8.6 mm (200 x 340 mils)
Die area:	43 mm <sup>2</sup> (68,000 mils <sup>2</sup> )
Min pad size:	0.09 x 0.09 mm (3.8 x 3.8 mils)
Min pad window:	0.08 x 0.08 mm (3.4 x 3.4 mils)
Min pad space:	40 microns (1.5 mils)
Min pad-to-metal:	10 microns
Min metal 2 width:	0.8 micron
Min metal 2 space:	0.8 micron
Min metal 2 pitch (contacted):	3.0 microns
Min metal 2 pitch (uncontacted):	1.8 micron
Min via:	1.2 micron (round)
Min via pitch:	2.2 microns
Min metal 1 width:	0.8 micron
Min metal 1 space:	0.8 micron
Min metal 1 pitch (contacted):	2.4 microns
Min metal 1 pitch (uncontacted):	1.6 micron
Min contact:	0.9 micron
Min contact pitch:	2.1 microns
Min contact-to-gate:	0.5 micron
Min poly width:	0.55 micron
Min poly space:	0.8 micron
Min gate length* (N-ch):	0.55 micron
(P-ch):	0.8 micron
Cell size:	5.5 x 13.5 microns
Cell area:	74 microns <sup>2</sup>
Array size:	20 x 60 mils
Array area:	1200 mils <sup>2</sup>

\*Physical gate length.

## VERTICAL DIMENSIONS

Die thickness: 0.4 mm (16 mils)

### Layers:

Passivation 2:	0.7 micron
Passivation 1:	0.35 micron
Metallization 2 - cap:	0.05 micron (approx.)
- aluminum:	0.75 micron
- barrier:	0.2 micron
Interlevel dielectric:	0.5 - 1.5 micron
Metallization 1 - cap:	0.15 micron
- aluminum:	0.5 micron
- barrier:	0.15 micron
Pre-metal glass:	0.6 - 1.5 micron
Polycide - silicide:	0.1 micron
- poly:	0.15 micron
Local oxide:	0.4 micron
N+ under tunnel oxide:	0.2 micron
N+ S/D:	0.15 micron
P+ S/D:	0.15 micron
P-well:	1.5 micron
N-well:	2.0 microns

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PHYSICAL DIE STRUCTURES	Figures 7 - 28
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CIRCUIT LAYOUT AND I/O STRUCTURE	Figures 28 - 29

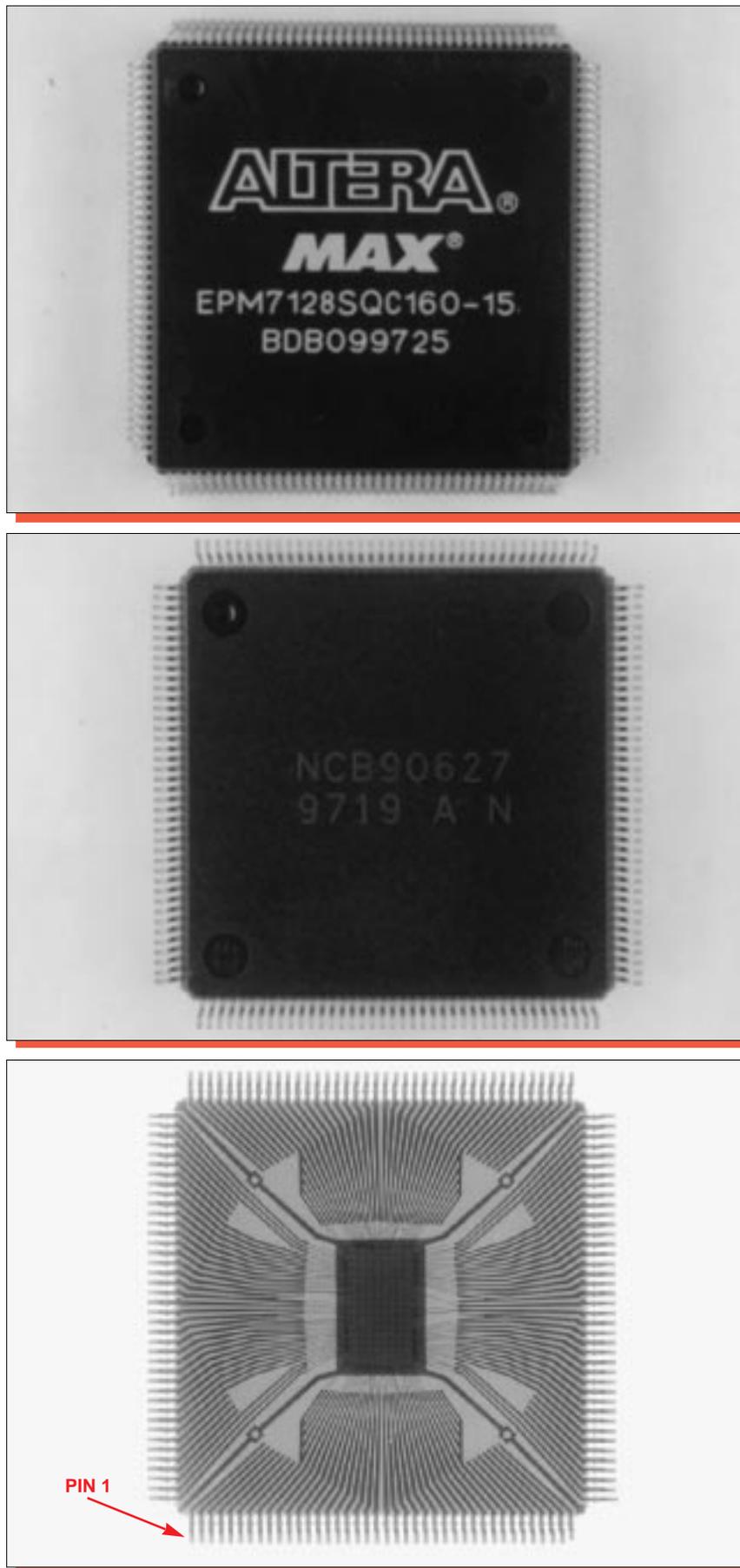
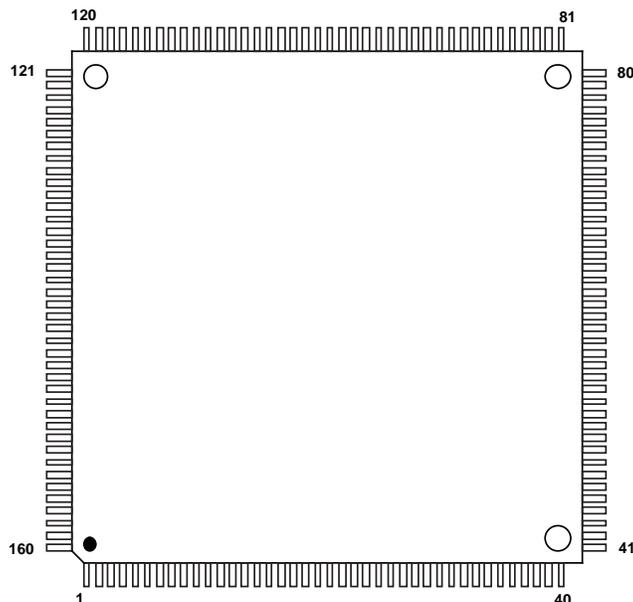


Figure 1. Package photographs and x-ray view of the Altera EPM7128SQC160-15.  
Mag. 2.3x.



PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION
1	N.C.	41	I/O	81	N.C.	121	I/O
2	N.C.	42	GND	82	N.C.	122	I/O
3	N.C.	43	I/O	83	N.C.	123	I/O
4	N.C.	44	N.C.	84	N.C.	124	N.C.
5	N.C.	45	N.C.	85	N.C.	125	N.C.
6	N.C.	46	N.C.	86	N.C.	126	N.C.
7	N.C.	47	N.C.	87	N.C.	127	N.C.
8	V <sub>CCIO</sub>	48	I/O	88	I/O	128	I/O
9	IO/TDI*	49	I/O	89	I/O	129	I/O
10	I/O	50	I/O	90	I/O	130	I/O
11	I/O	51	I/O	91	I/O	131	I/O
12	I/O	52	I/O	92	I/O	132	I/O
13	I/O	53	I/O	93	I/O	133	V <sub>CCIO</sub>
14	I/O	54	I/O	94	I/O	134	I/O
15	I/O	55	V <sub>CCIO</sub>	95	GND	135	I/O
16	I/O	56	I/O	96	I/O	136	I/O
17	GND	57	I/O	97	I/O	137	I/O
18	I/O	58	I/O	98	I/O	138	GND
19	I/O	59	I/O	99	I/O/TCK*	139	INPUTGCLK1
20	I/O	60	I/O	100	I/O	140	INPUT/EO1
21	I/O	61	V <sub>CCINT</sub>	101	I/O	141	INPUT/GCLRn
22	V <sub>CCIO</sub>	62	I/O	102	I/O	142	INPUT/OE2/GCLK2
23	I/O	63	I/O	103	I/O	143	V <sub>CCINT</sub>
24	I/O	64	I/O	104	V <sub>CCIO</sub>	144	I/O
25	I/O	65	I/O	105	I/O	145	I/O
26	V <sub>CCIO</sub>	66	GND	106	I/O	146	I/O
27	I/O	67	I/O	107	I/O	147	I/O
28	I/O	68	I/O	108	I/O	148	GND
29	I/O	69	I/O	109	I/O	149	I/O
30	I/O	70	I/O	110	I/O	150	I/O
31	I/O	71	I/O	111	I/O	151	I/O
32	I/O	72	I/O	112	I/O/TDO*	152	I/O
33	I/O	73	I/O	113	GND	153	I/O
34	N.C.	74	N.C.	114	N.C.	154	N.C.
35	N.C.	75	N.C.	115	N.C.	155	N.C.
36	N.C.	76	N.C.	116	N.C.	156	N.C.
37	N.C.	77	N.C.	117	N.C.	157	N.C.
38	N.C.	78	I/O	118	N.C.	158	I/O
39	N.C.	79	V <sub>CCIO</sub>	119	N.C.	159	I/O
40	N.C.	80	I/O	120	N.C.	160	I/O

\*In MAX 7000S devices, this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for boundary-scan testing or for ISP, this pin is not available as a user I/O pin.

Figure 2. Pinout of the Altera EPM7128SQC160-15.

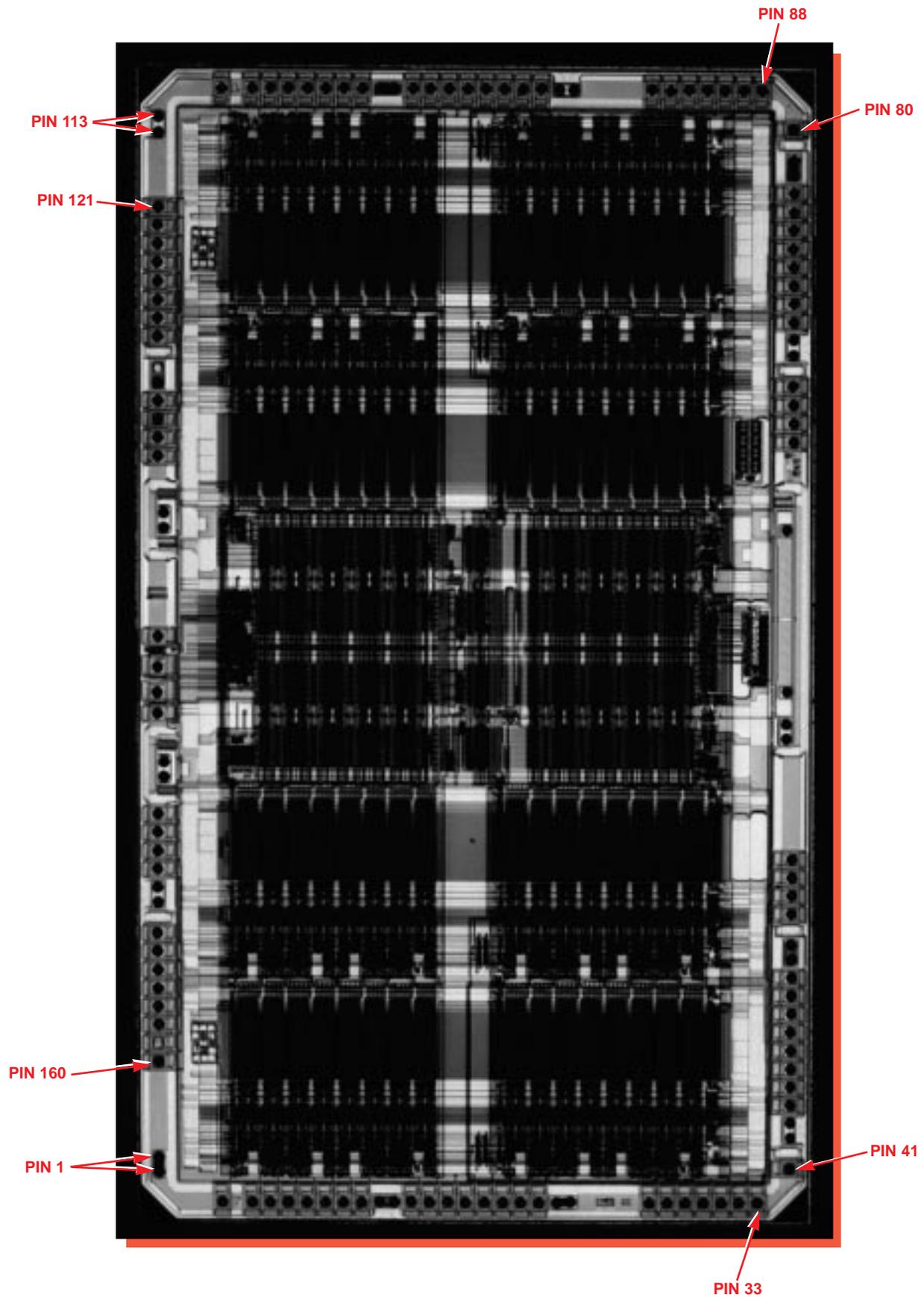


Figure 3. Whole die photograph of the Altera EPM7128SQC160-15. Mag. 24x.

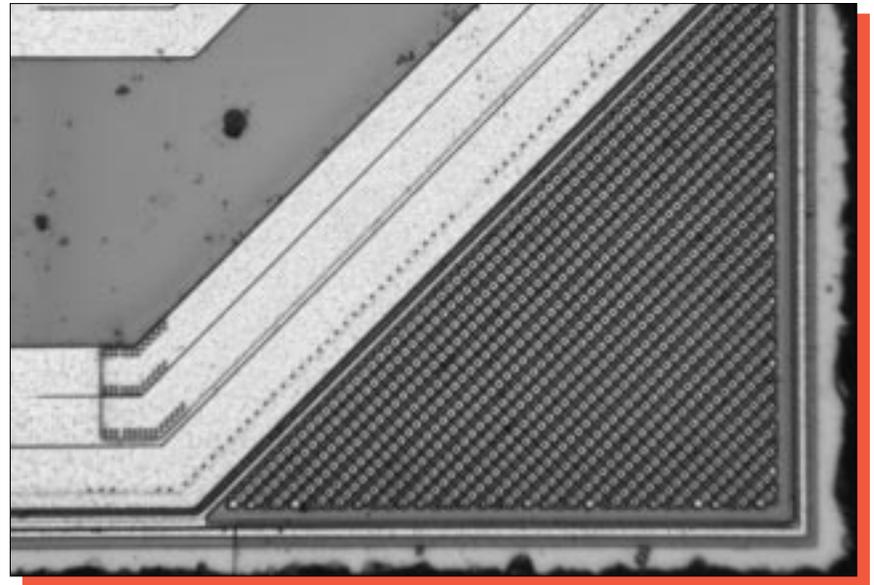
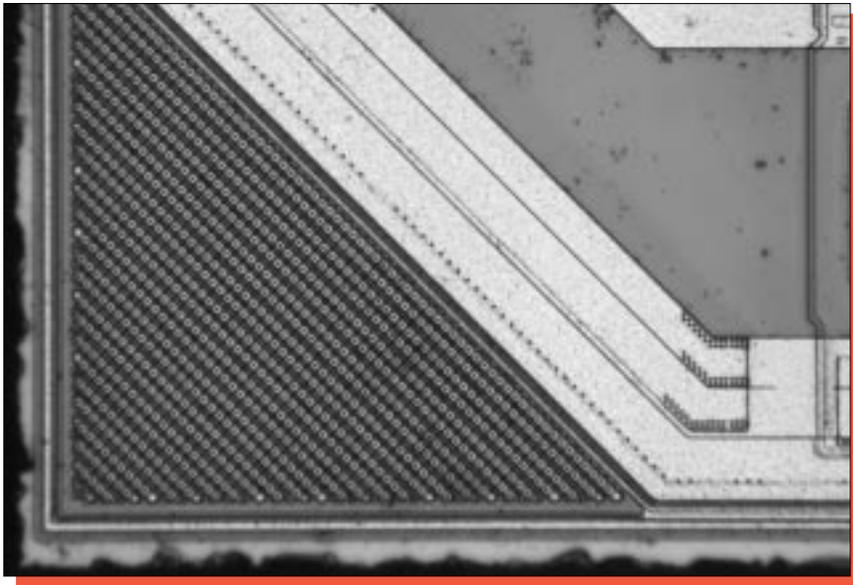
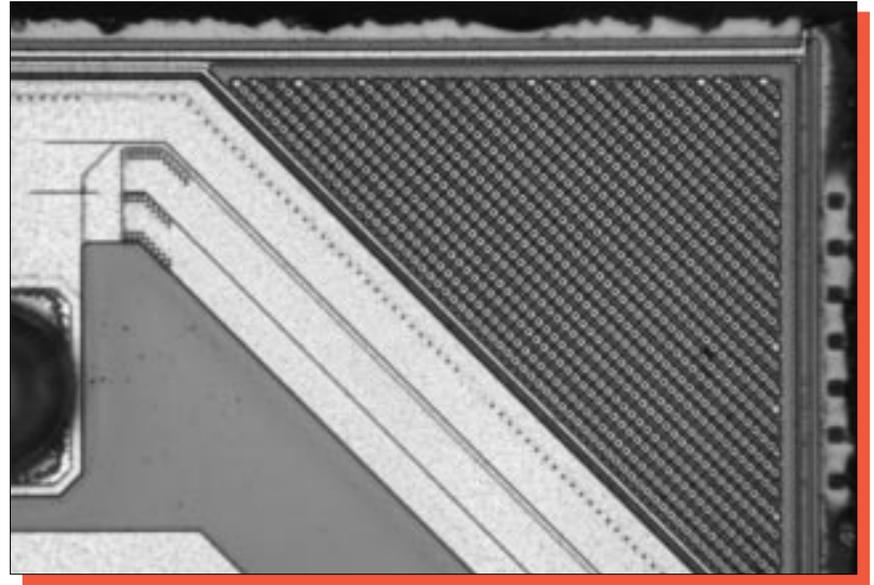
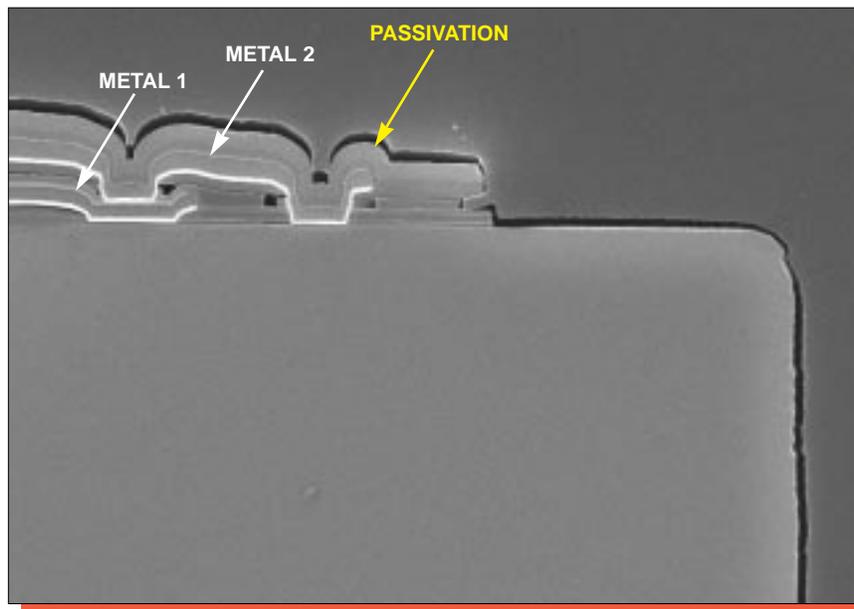
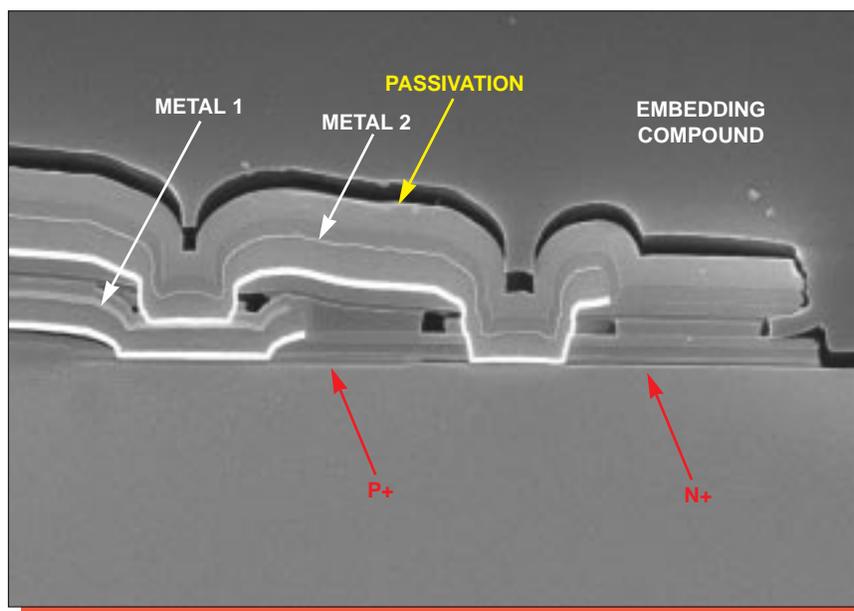


Figure 4. Optical views of die corners. Mag. 300x.



Mag. 3250x

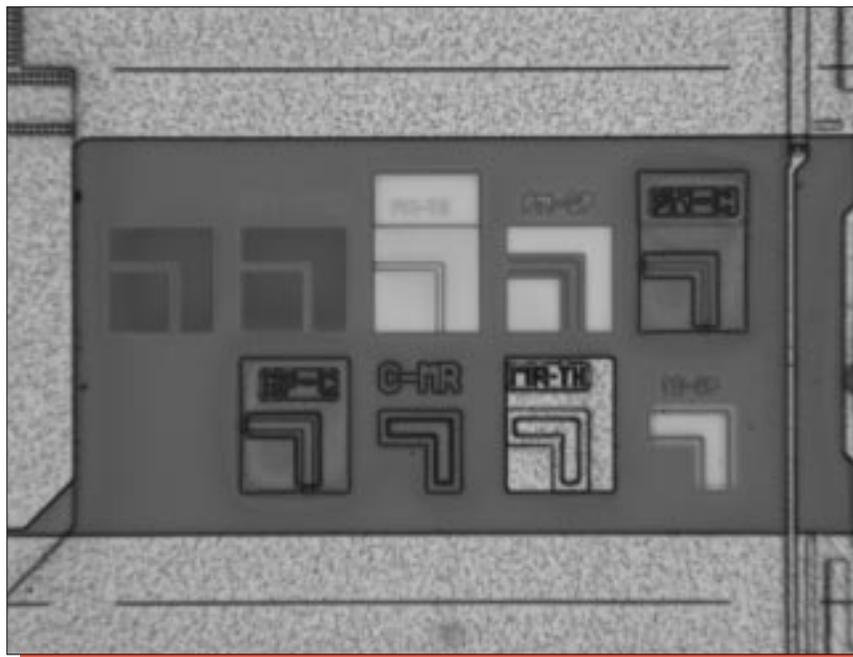


Mag. 6000x

Figure 5. SEM section views illustrating edge seal structure.

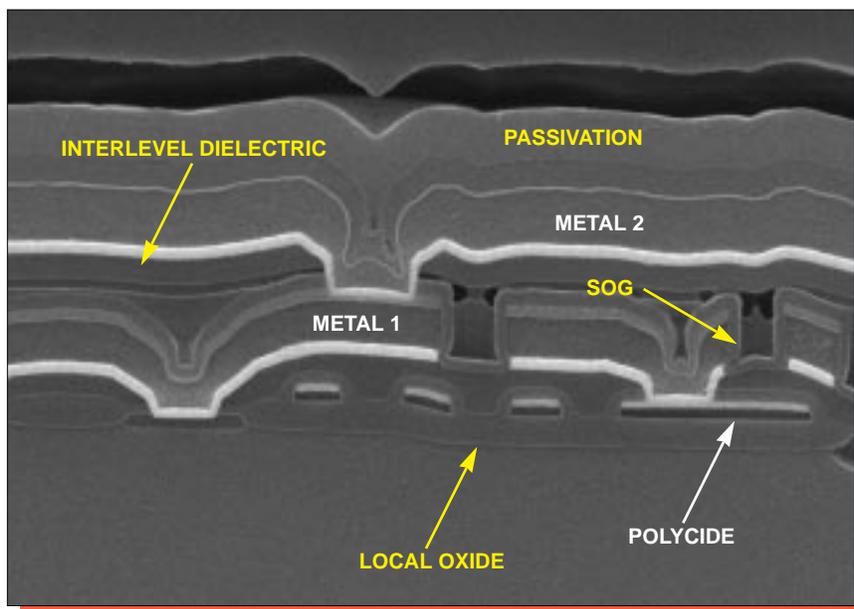


Mag. 350x

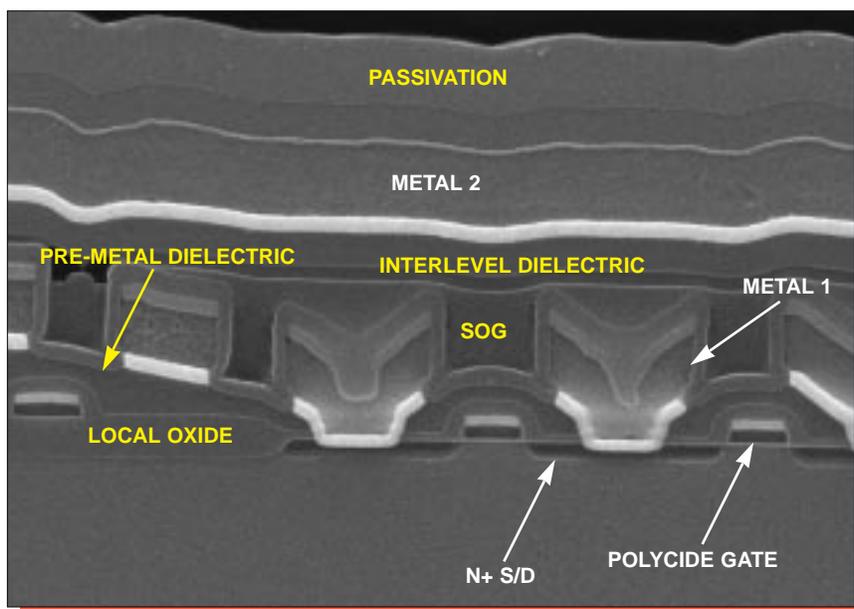


Mag. 410x

Figure 6. Optical views of die markings.

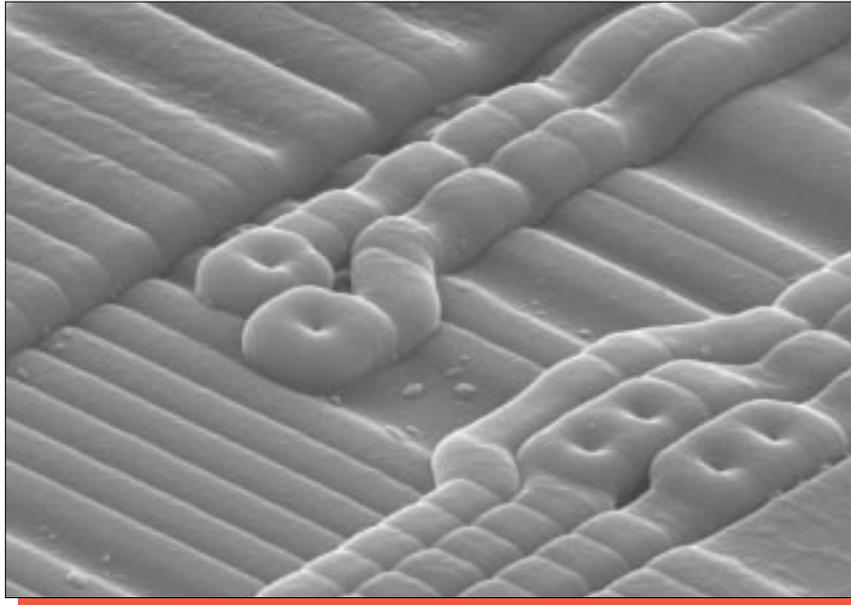


Mag. 10,000x

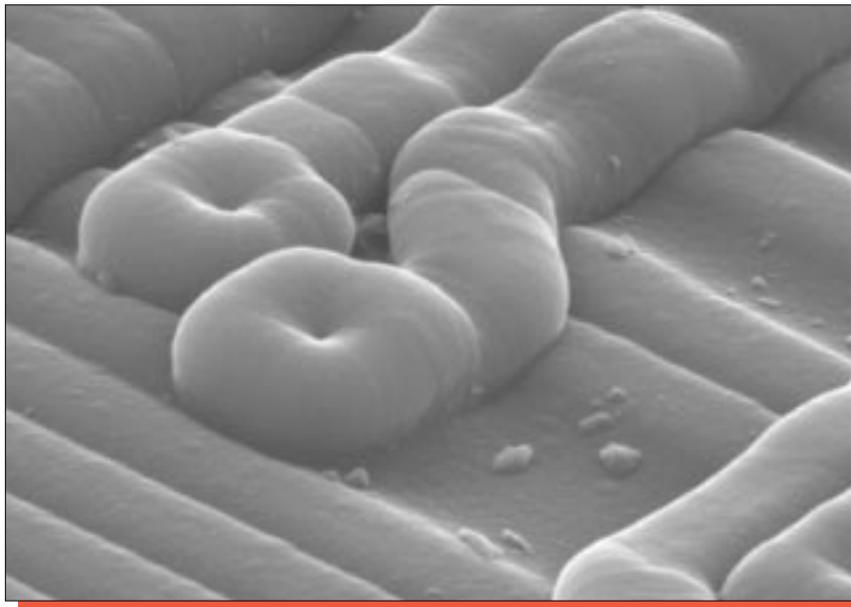


Mag. 13,000x

Figure 7. SEM section views illustrating general structure.

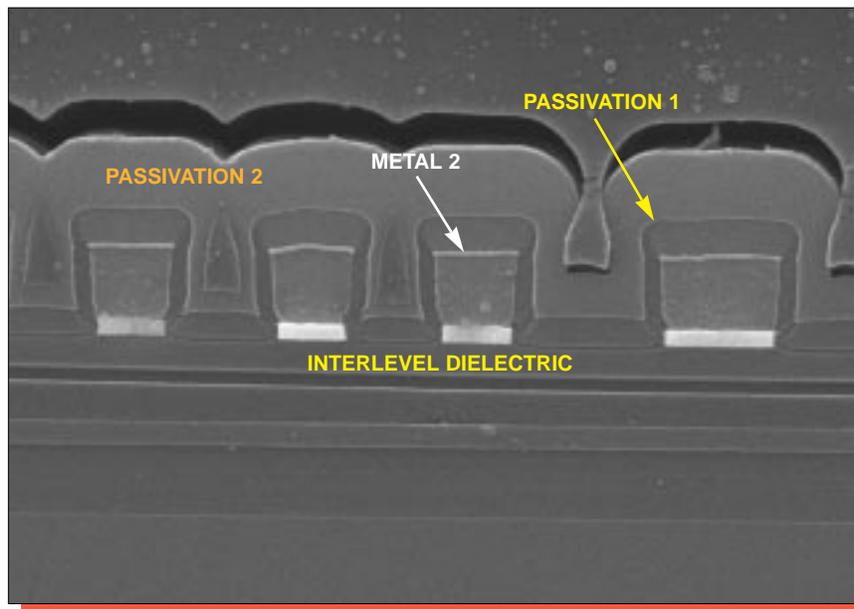


Mag. 5000x

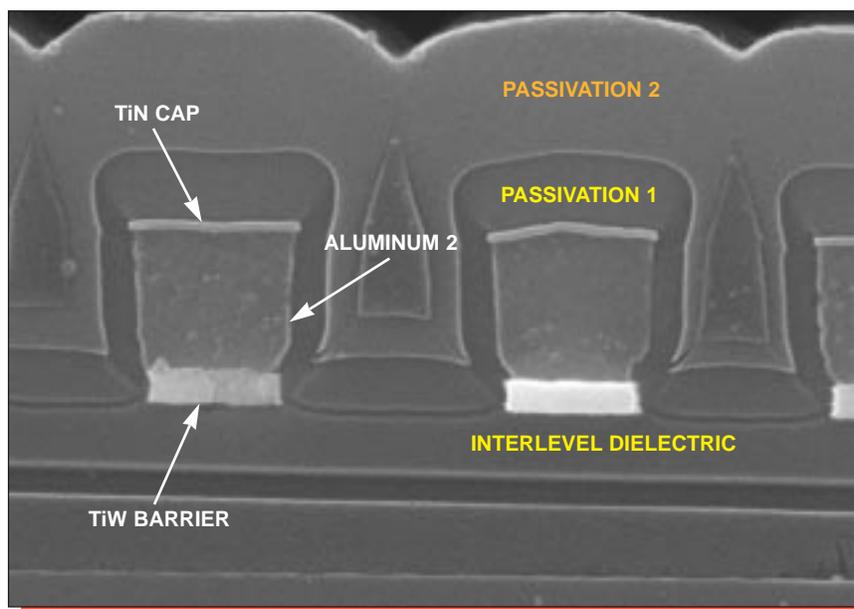


Mag. 10,000x

Figure 8. SEM views illustrating passivation coverage. 60°.



Mag. 13,000x



Mag. 26,000x

Figure 9. SEM section views illustrating metal 2 line profiles.

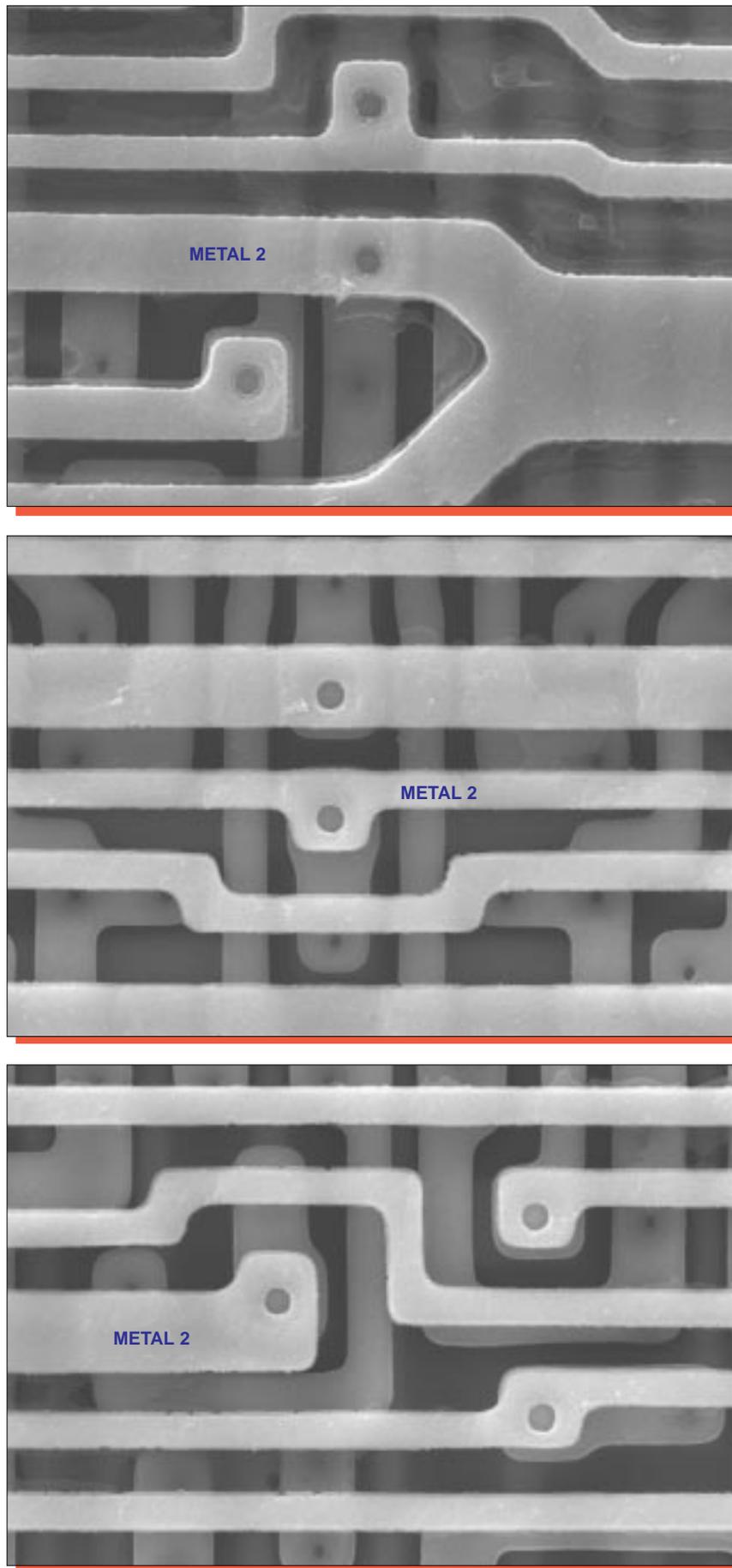
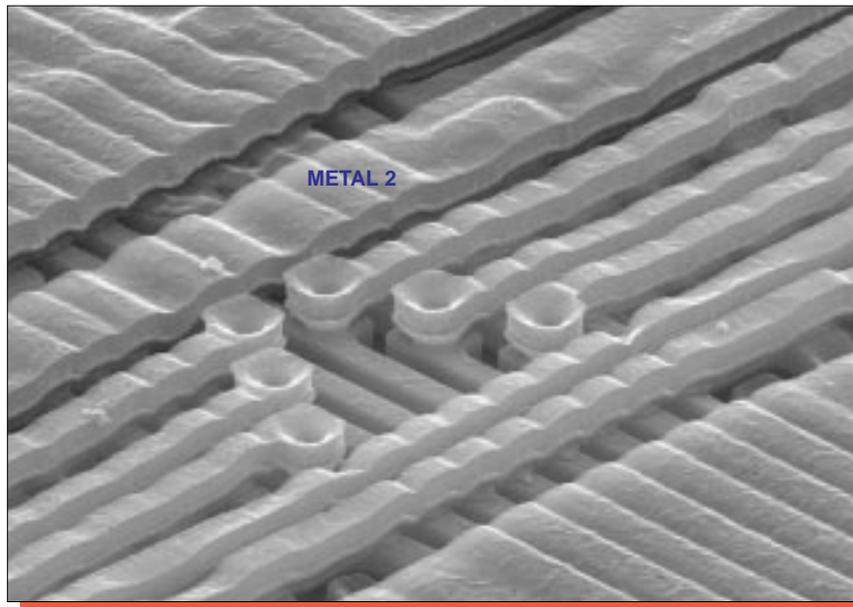
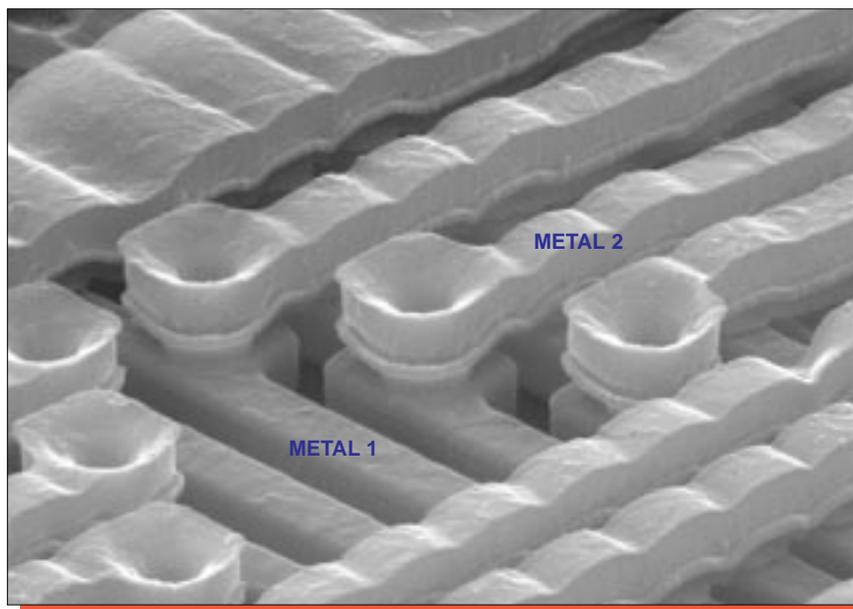


Figure 10. Topological SEM views illustrating metal 2 patterning. Mag. 6500x, 0°.



Mag. 5000x



Mag. 10,000x

Figure 11. SEM views illustrating metal 2 step coverage. 60°.

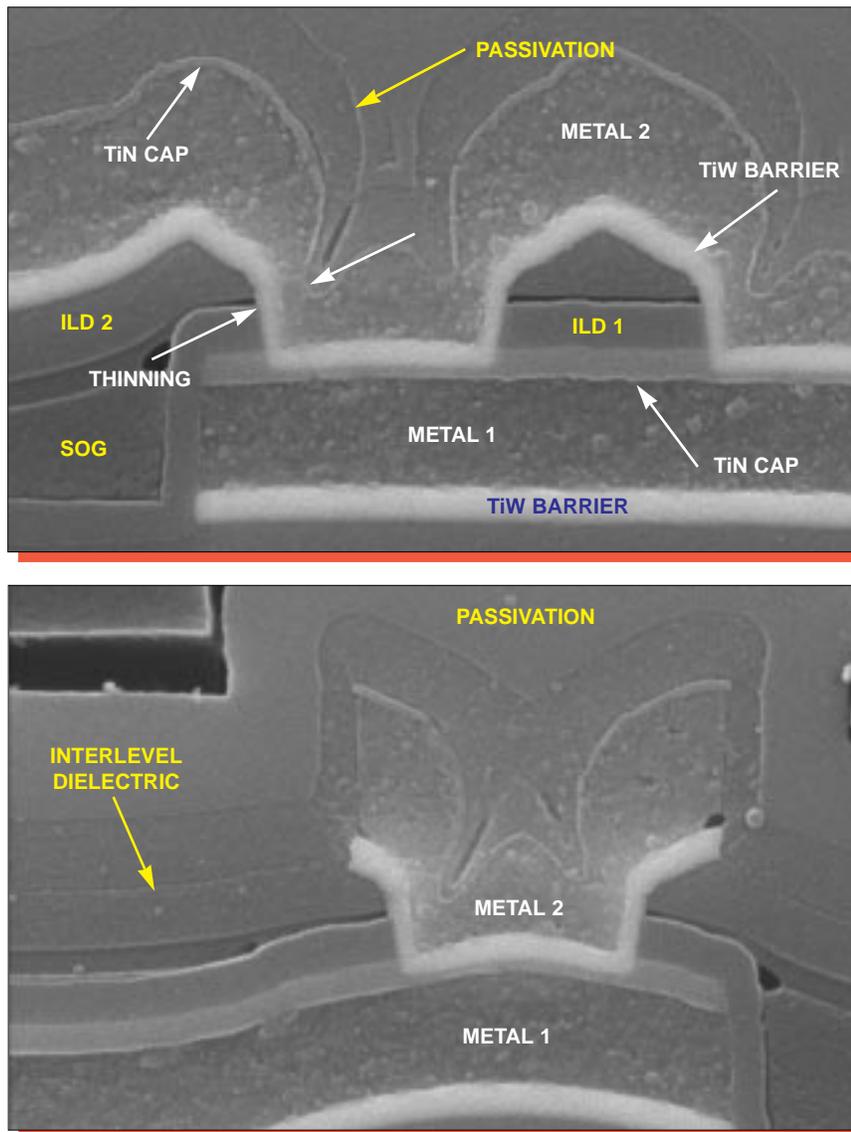


Figure 12. SEM section views illustrating typical metal 2-to-metal 1 vias.  
Mag. 26,000x.

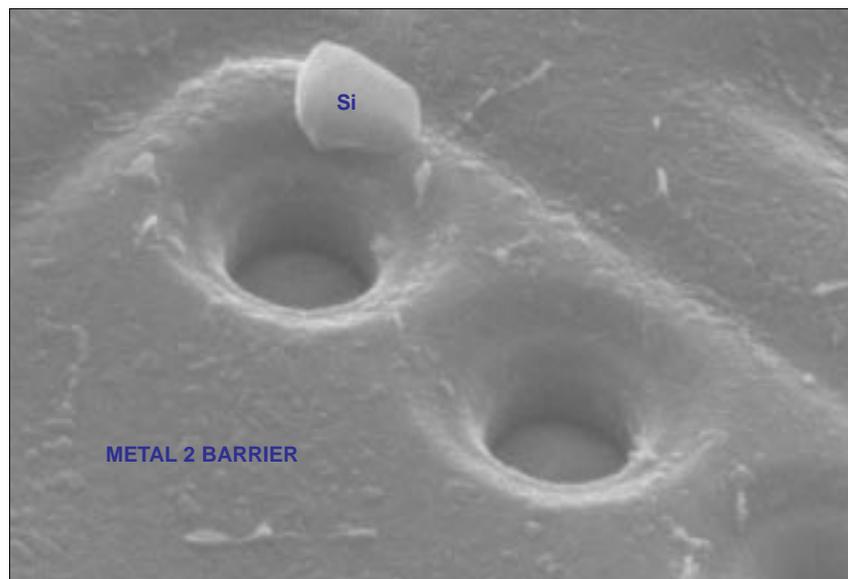
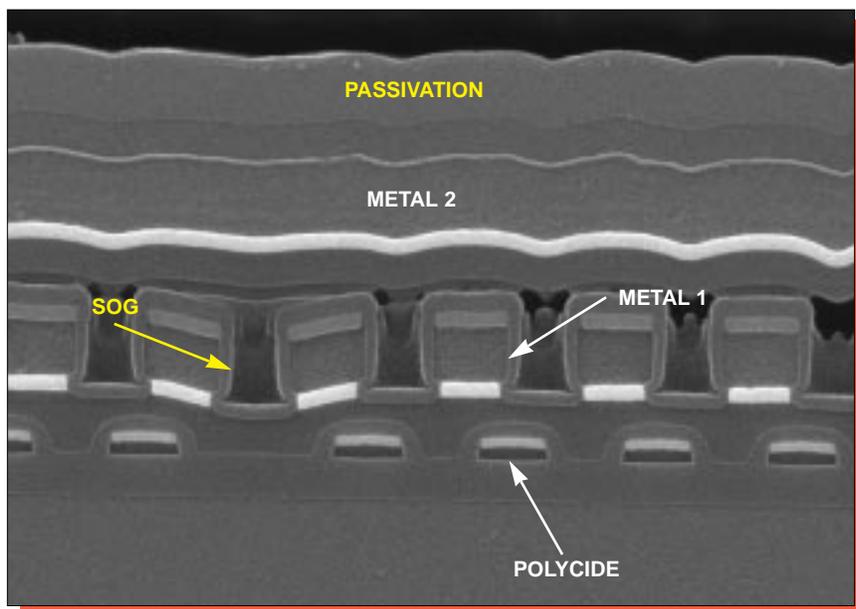
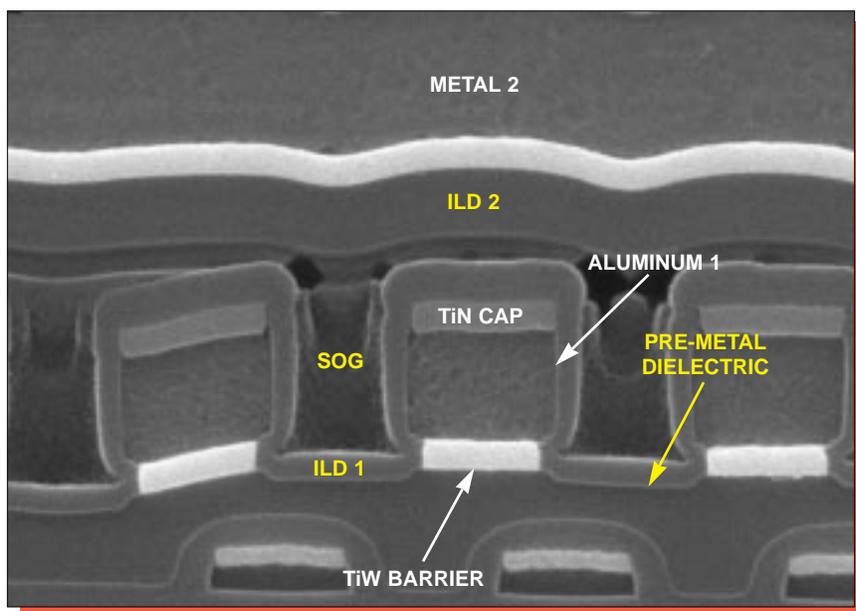


Figure 13. SEM view illustrating metal 2 barrier. Mag. 20,000x, 45°.



Mag. 13,000x



Mag. 26,000x

Figure 14. SEM section views illustrating metal 1 line profiles.

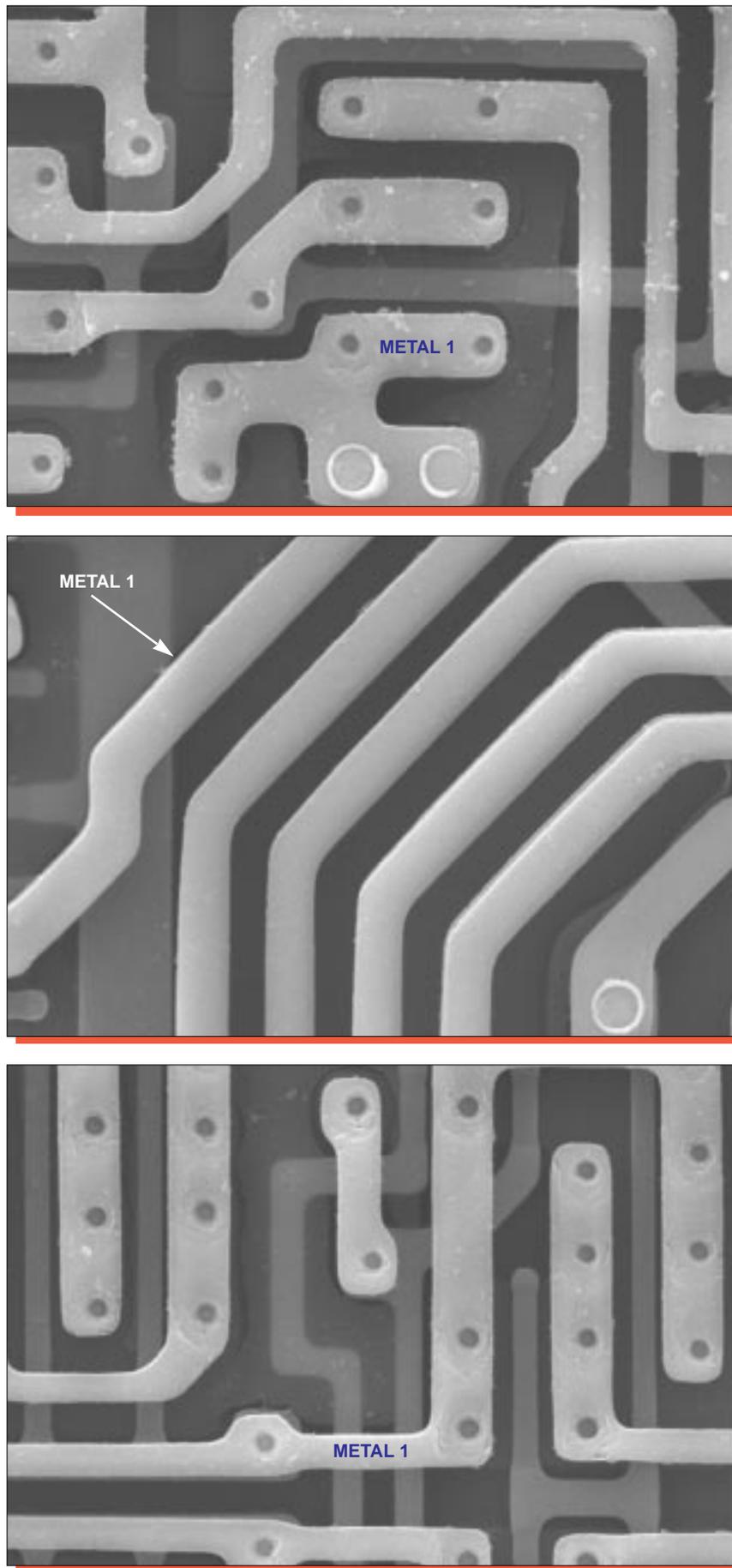
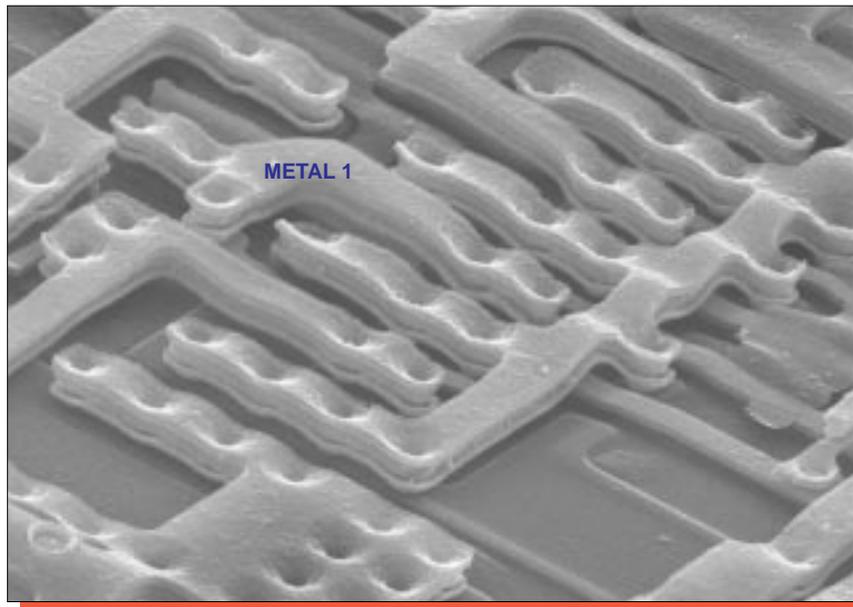
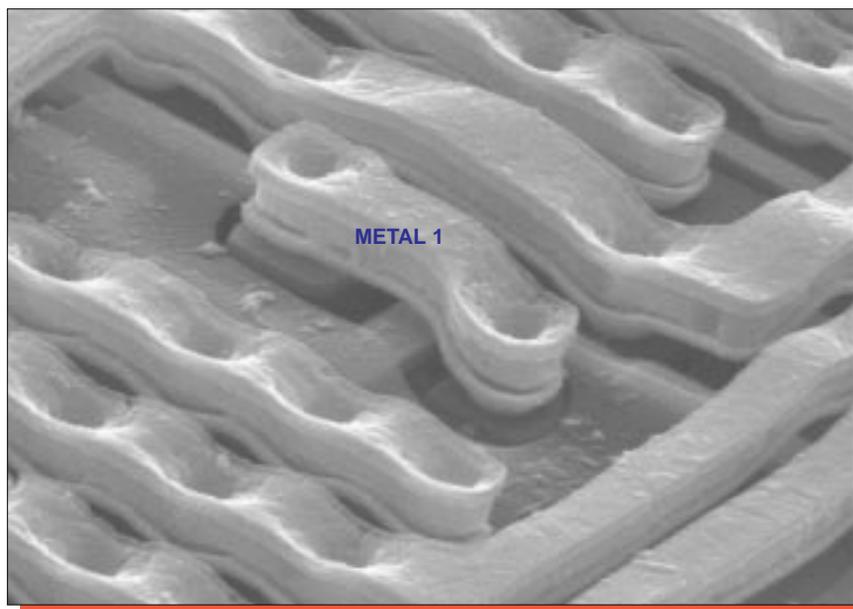


Figure 15. Topological SEM views illustrating metal 1 patterning. Mag. 6500x, 0°.



Mag. 5000x



Mag. 10,000x

Figure 16. SEM views illustrating metal 1 step coverage. 60°.

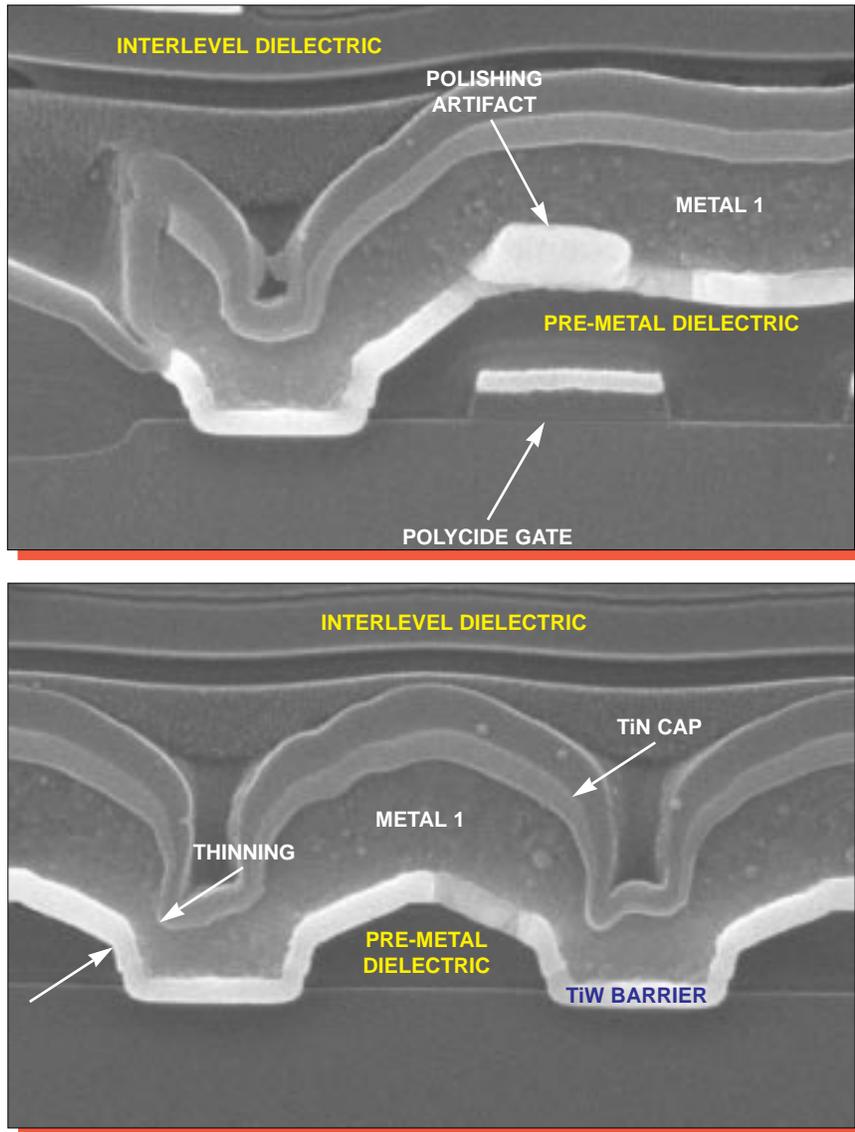


Figure 17. SEM section views illustrating typical metal 1 contacts. Glass etch, Mag. 26,000x

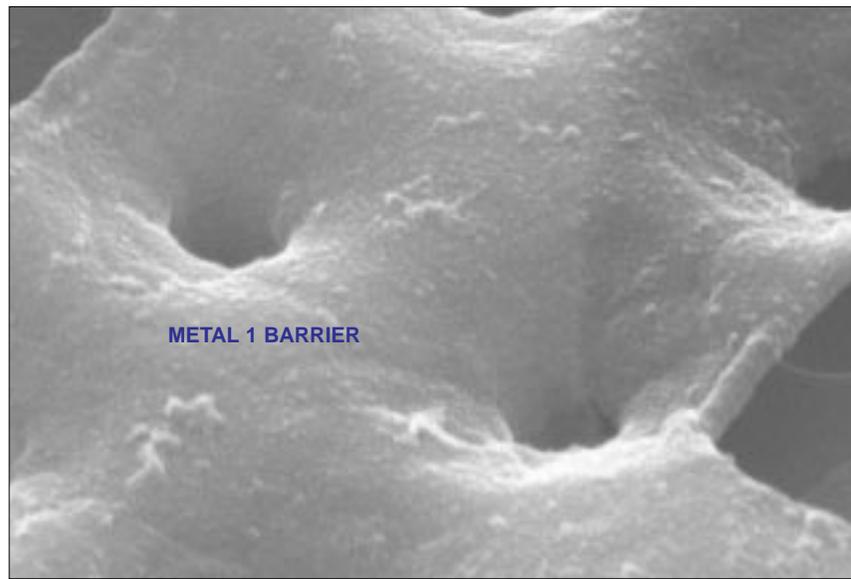
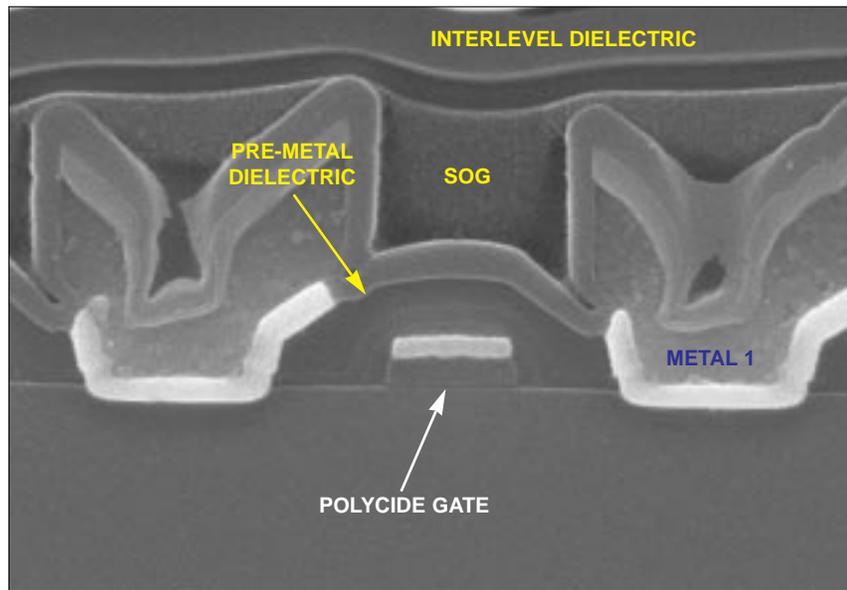
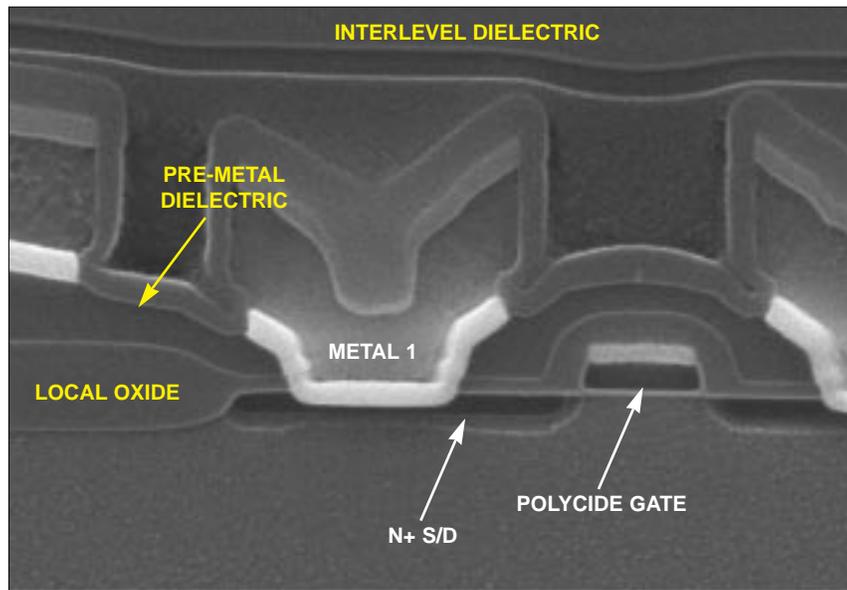


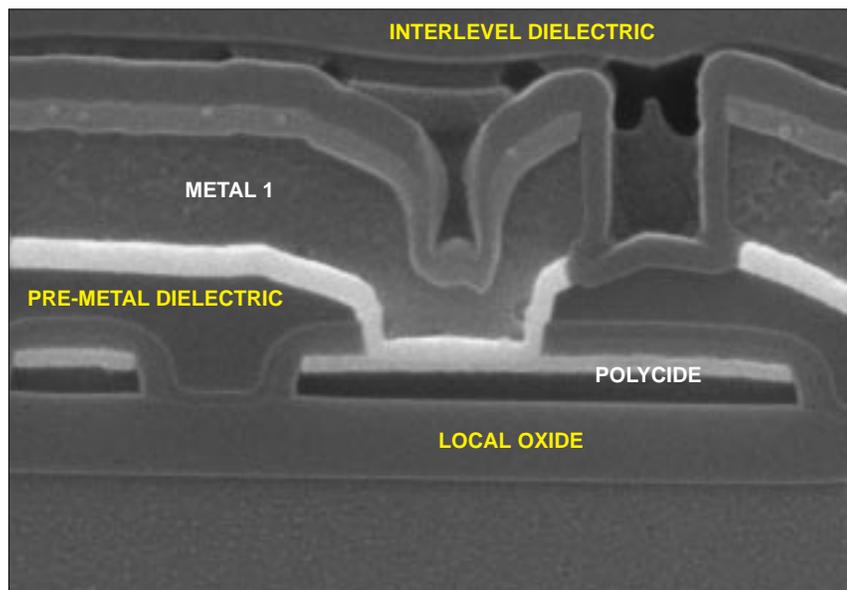
Figure 18. SEM view illustrating metal 1 barrier. Mag. 30,000x, 45°.



glass etch

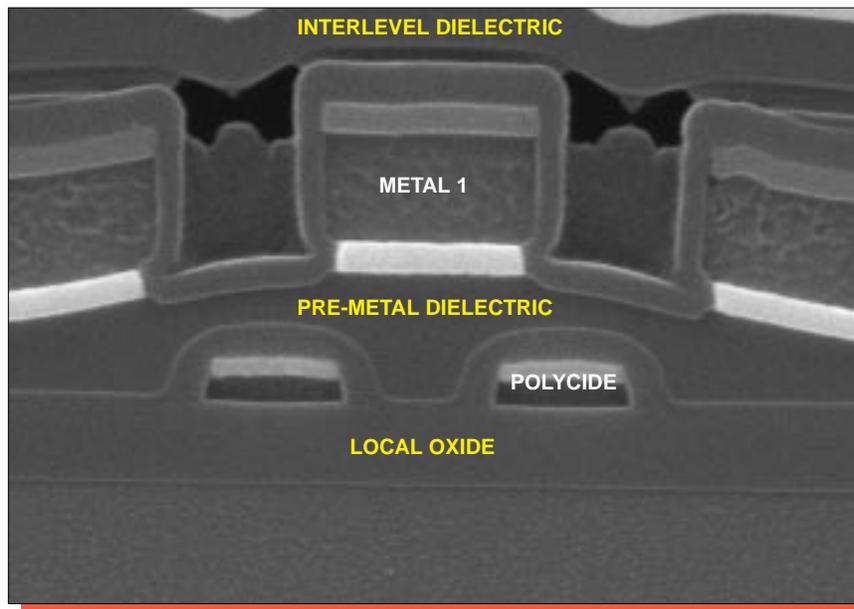


metal 1-to-N+

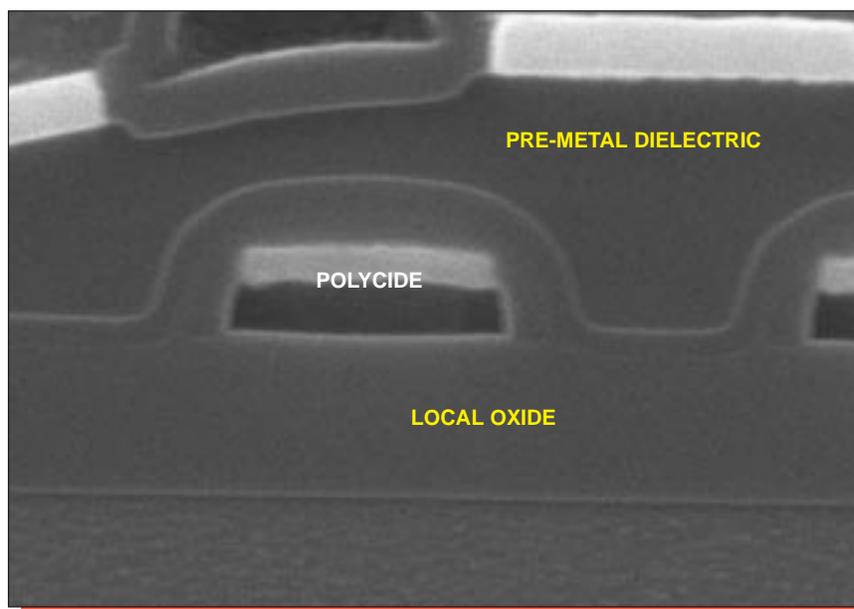


metal 1-to-polycide

Figure 19. Additional SEM section views illustrating metal 1 contacts. Mag. 26,000x.

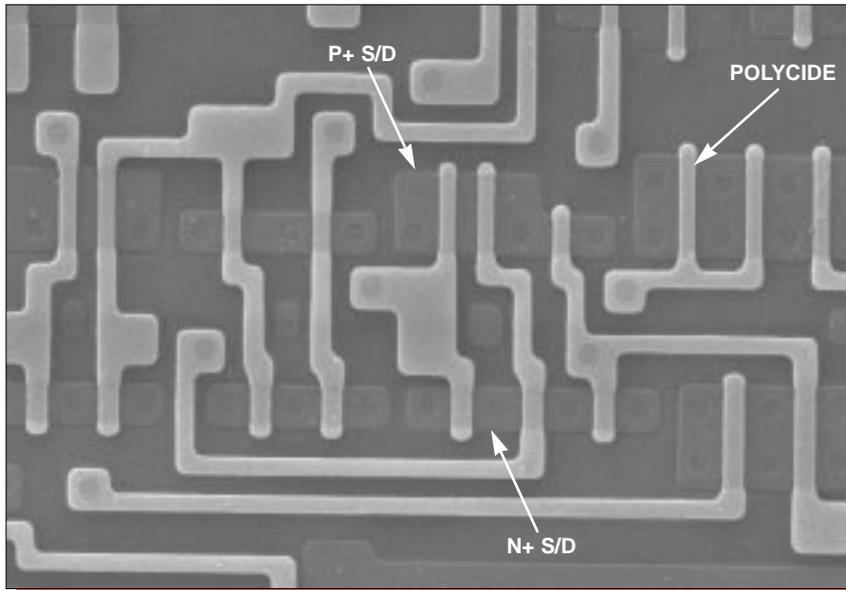


Mag. 26,000x

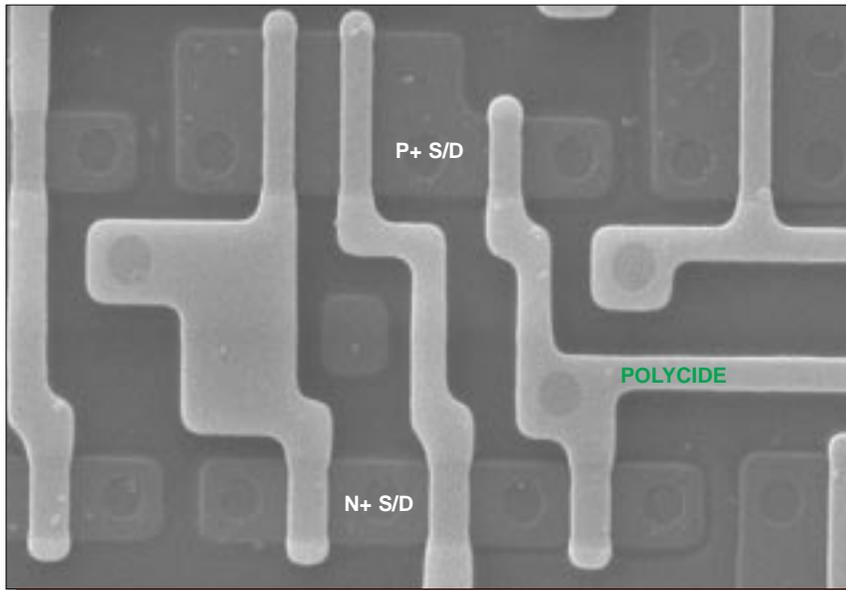


Mag. 52,000x

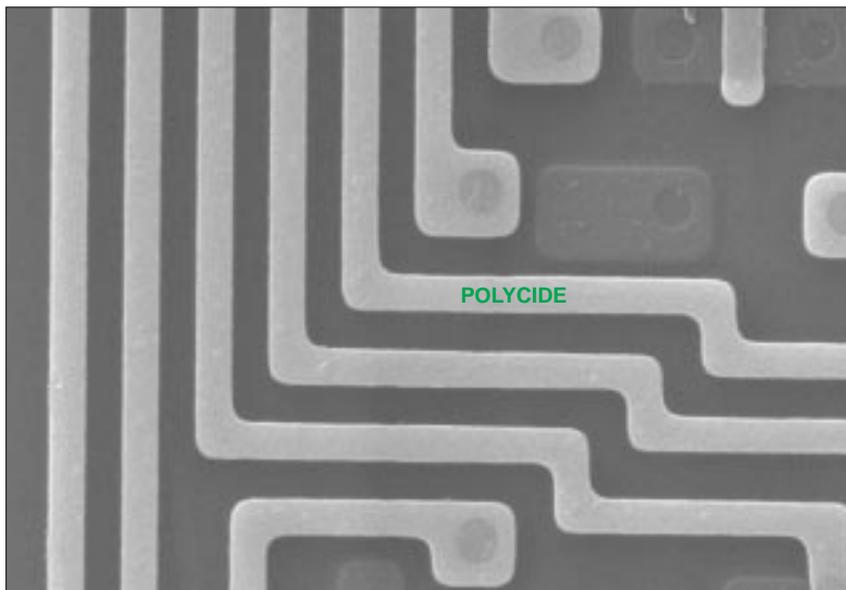
Figure 20. SEM section views illustrating polycide profiles.



Mag. 3250x

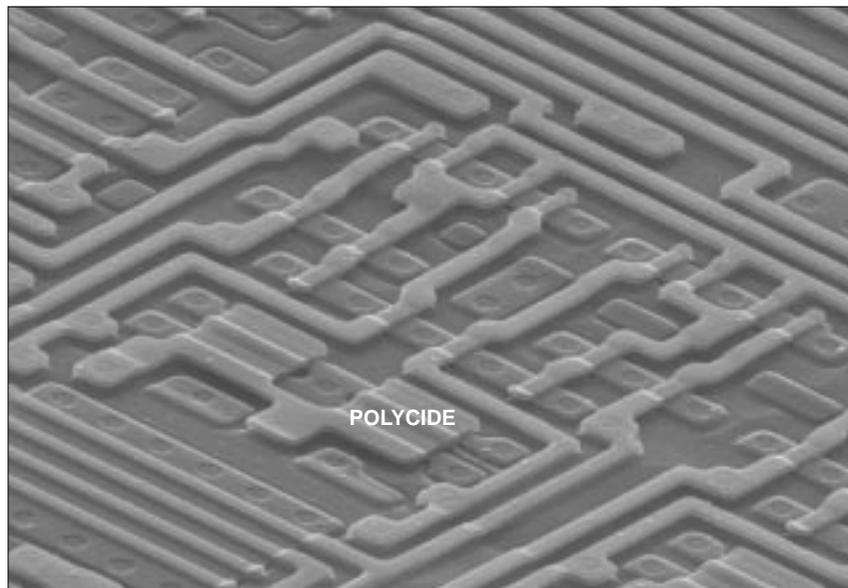


Mag. 6500x

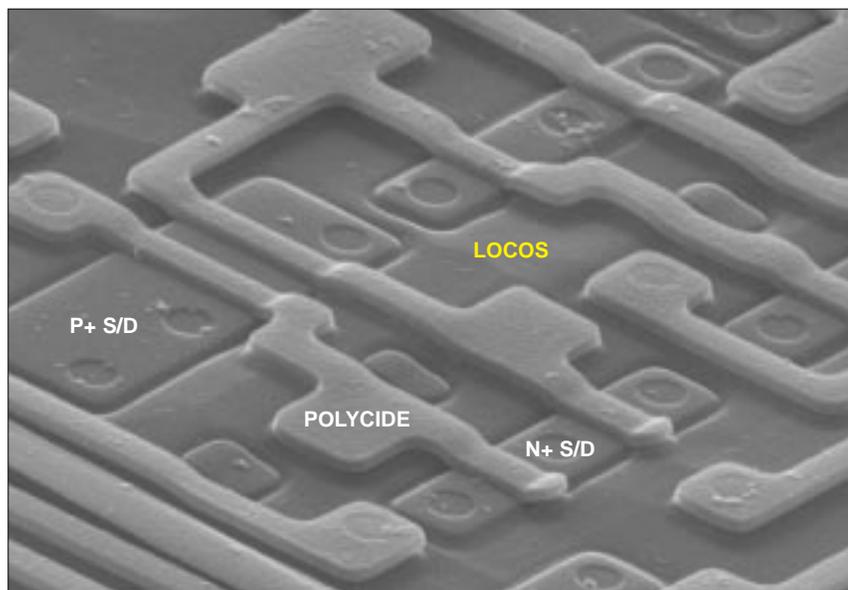


Mag. 6500x

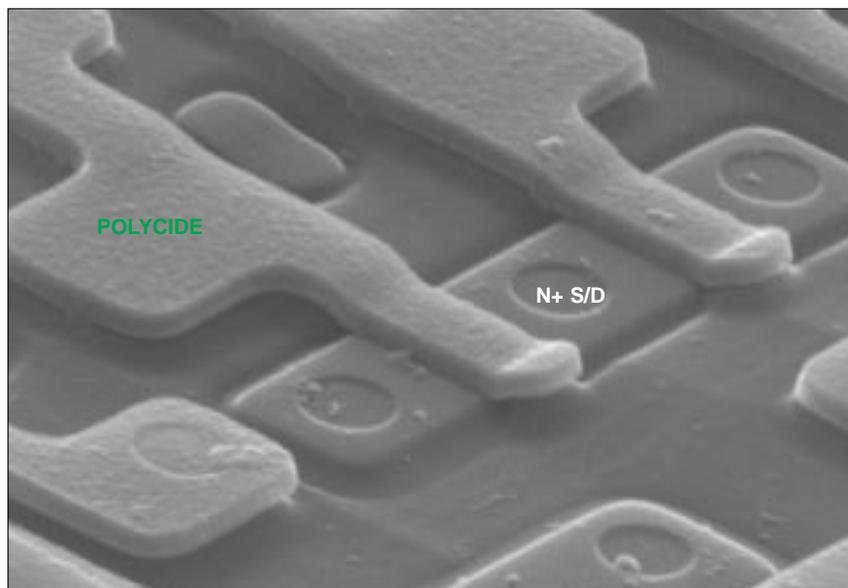
Figure 21. Topological SEM views illustrating polycide patterning. 0°.



Mag. 4000x



Mag. 8000x



Mag. 16,000x

Figure 22. SEM views illustrating polycide step coverage. 60°.

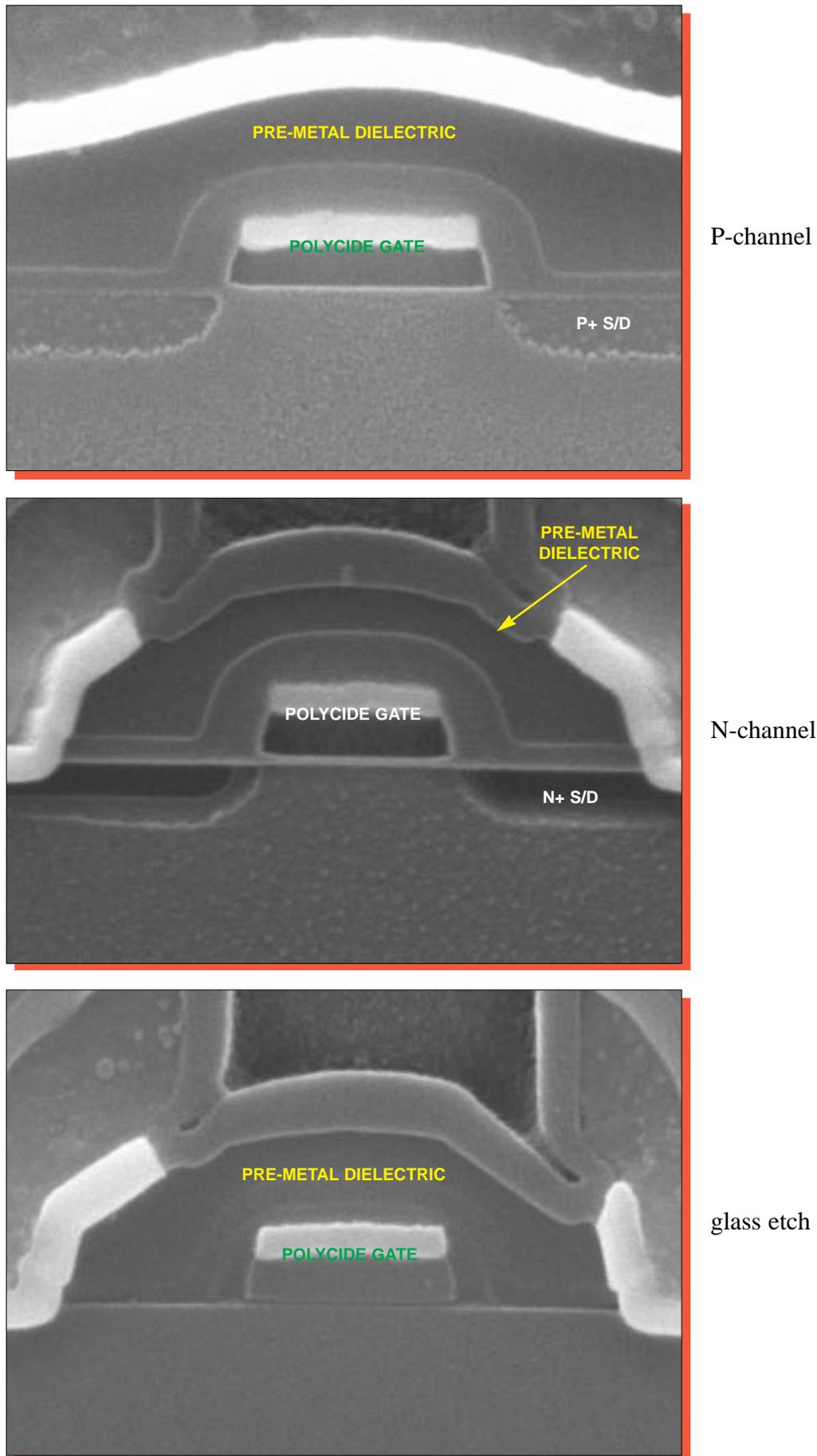
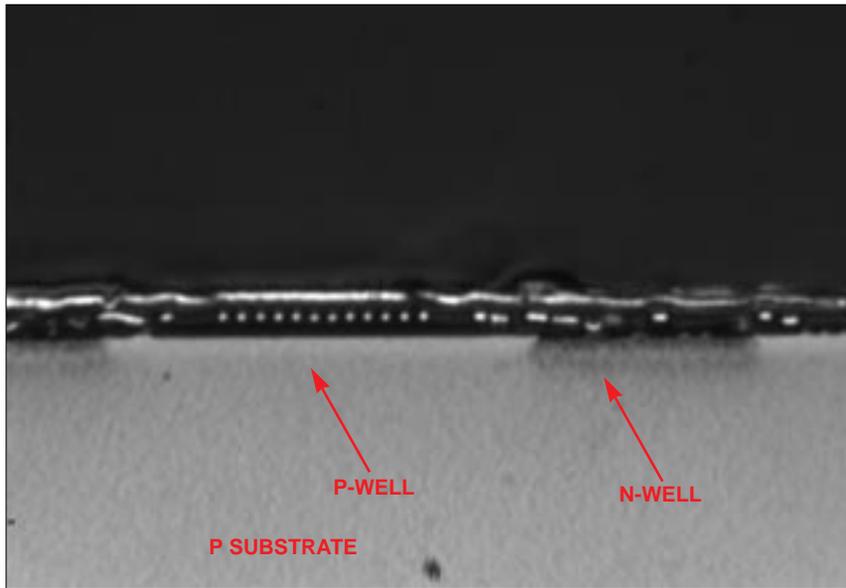
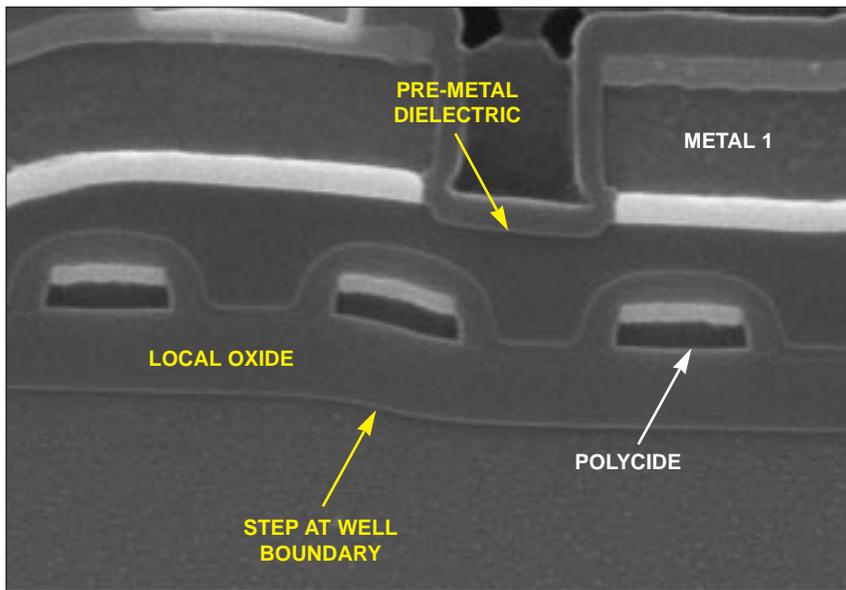


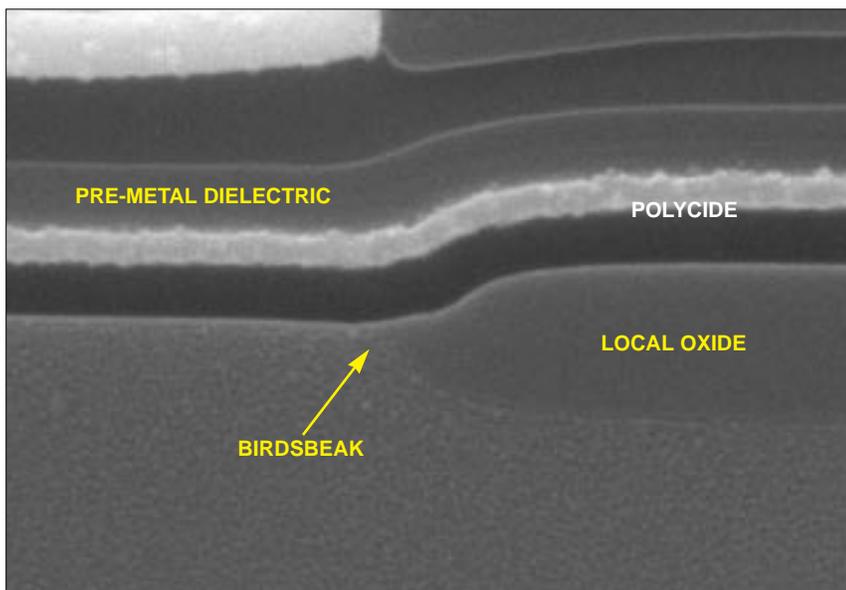
Figure 23. SEM section views illustrating typical gate structure. Mag. 52,000x.



Mag. 1535x

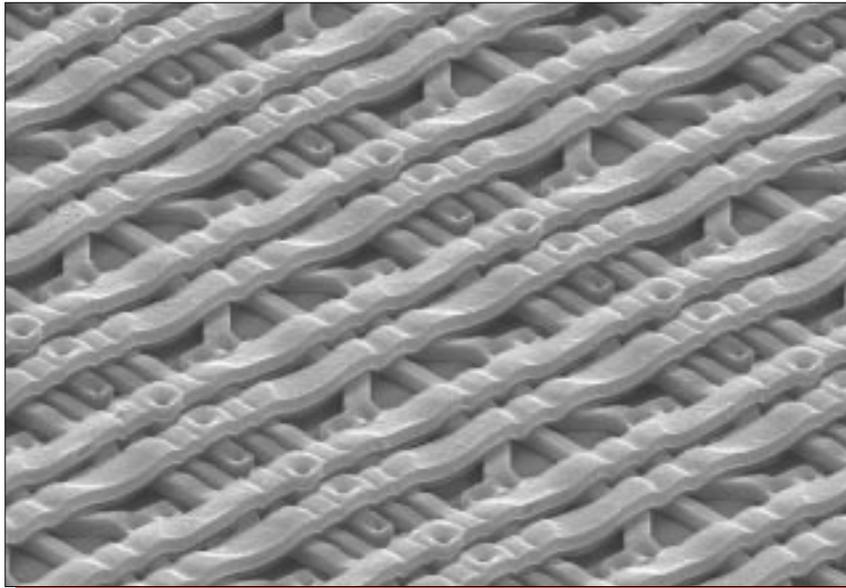


Mag. 26,000x

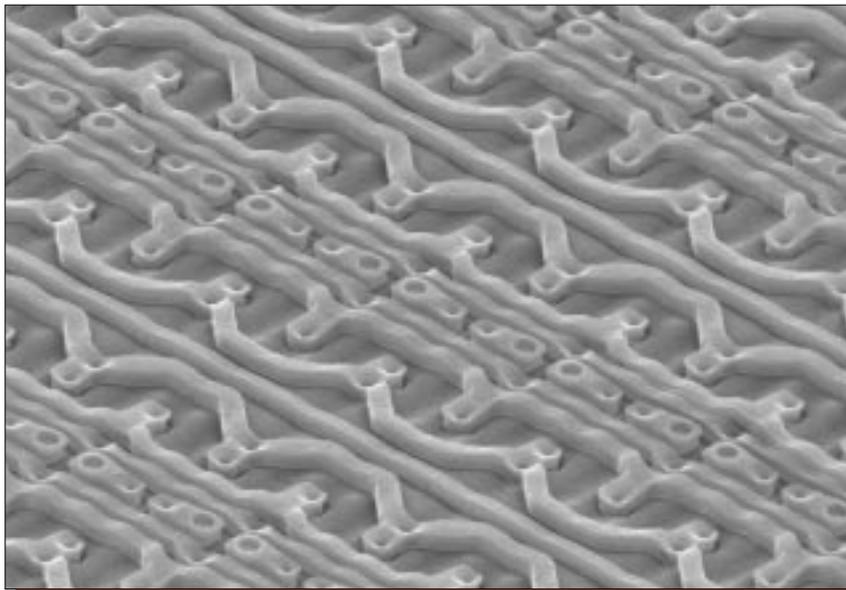


Mag. 52,000x

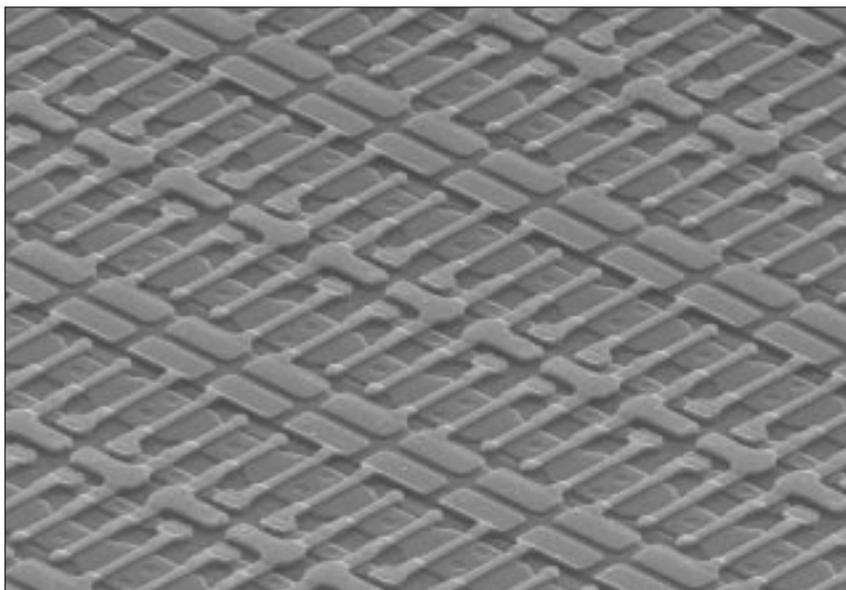
Figure 24. Section views illustrating well structure and a typical birdsbeak.



metal 2

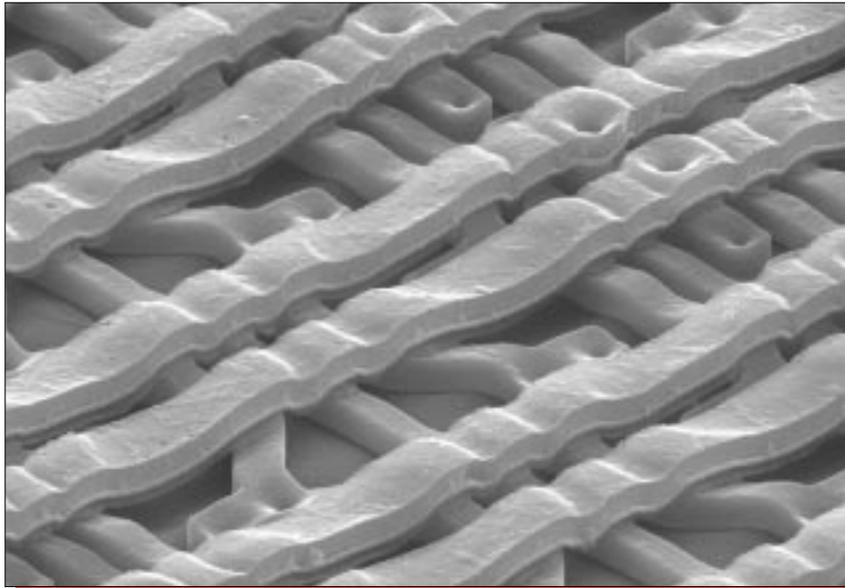


metal 1

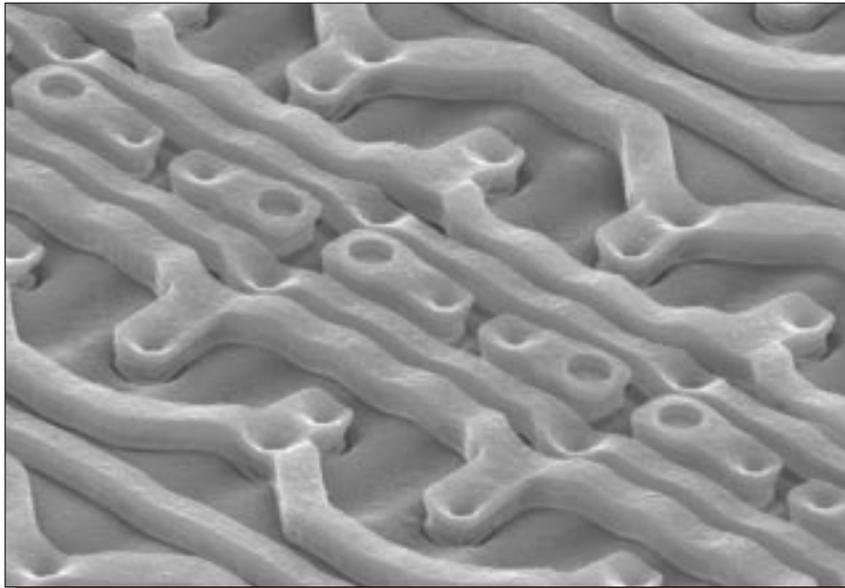


polycide

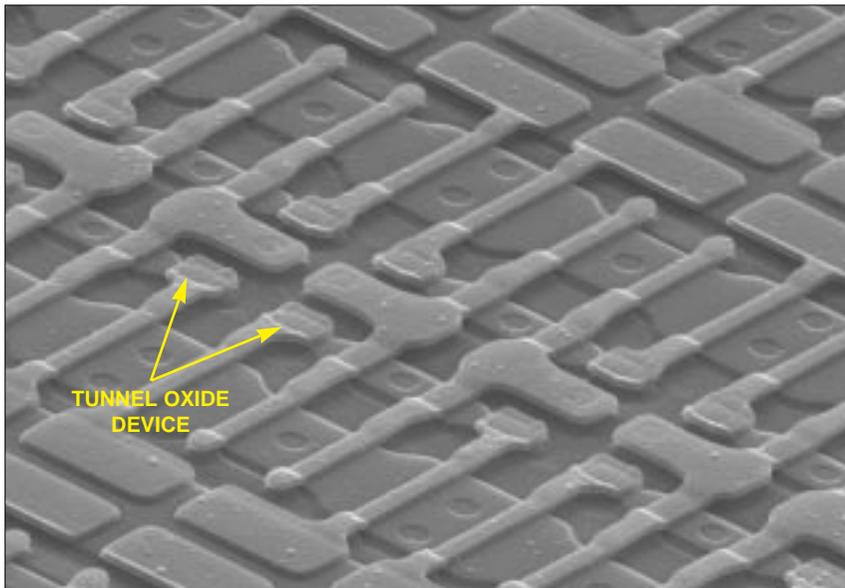
Figure 25. SEM views illustrating EEPROM cell array. Mag. 2500x, 60°.



metal 2



metal 1



polycide

Figure 25a. SEM views illustrating EEPROM cell array. Mag. 5000x, 60°.

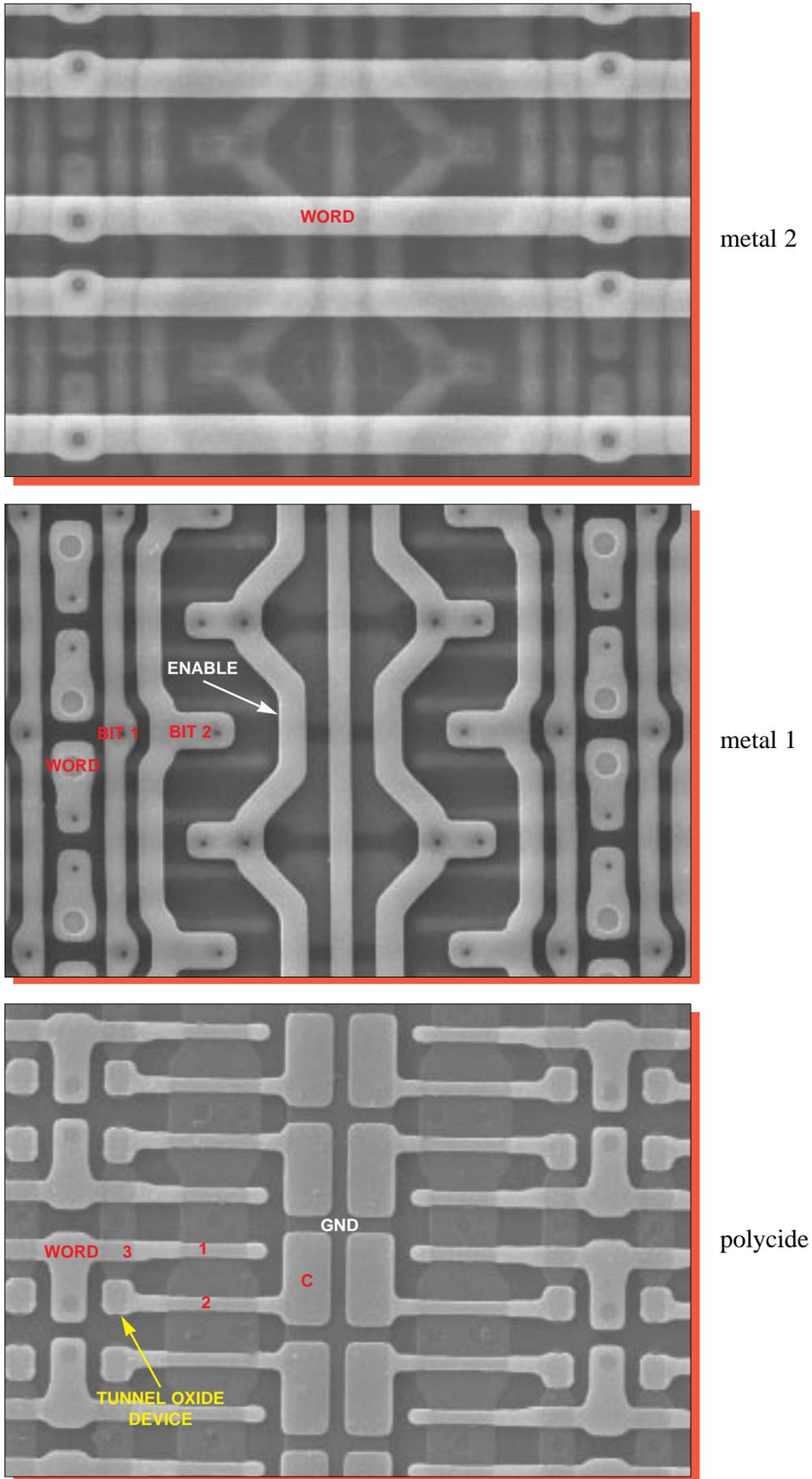
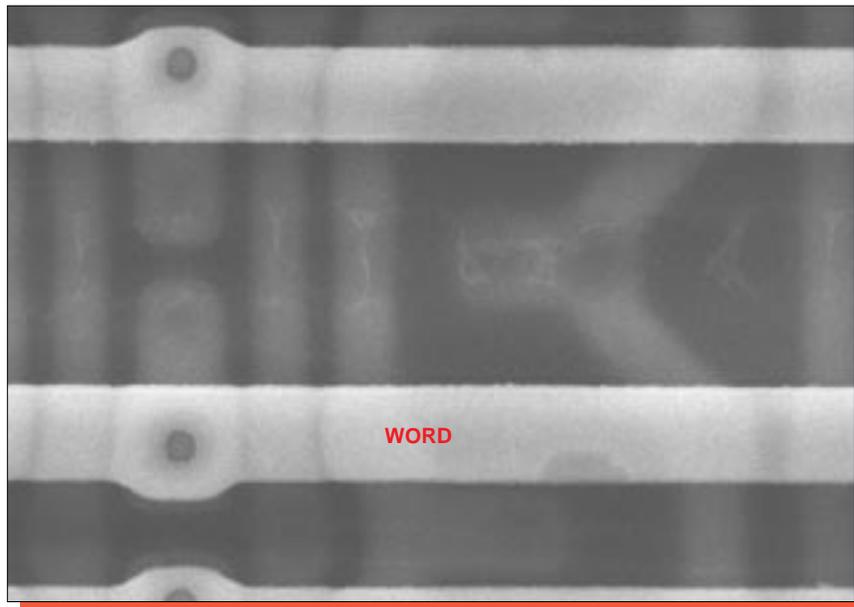
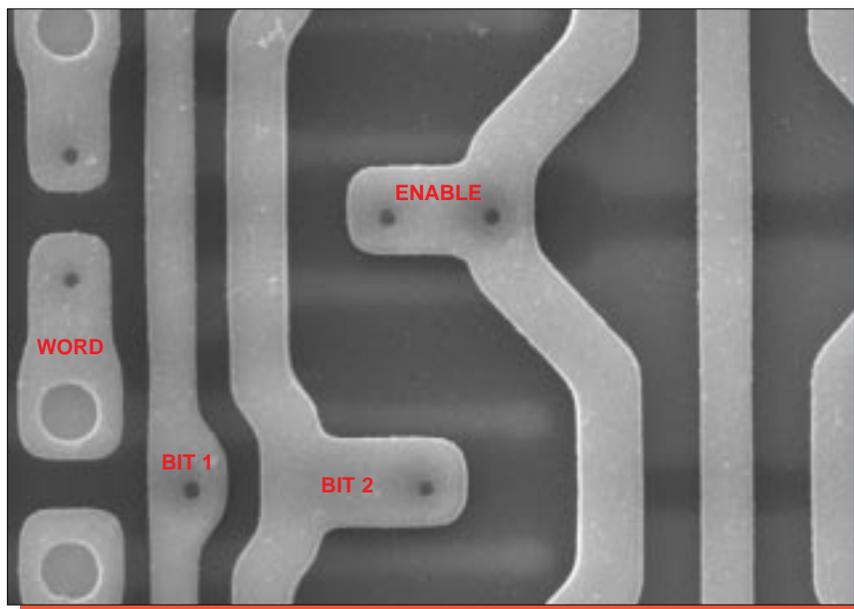


Figure 26. Topological SEM views illustrating EEPROM cell array. Mag. 3250x, 0°.

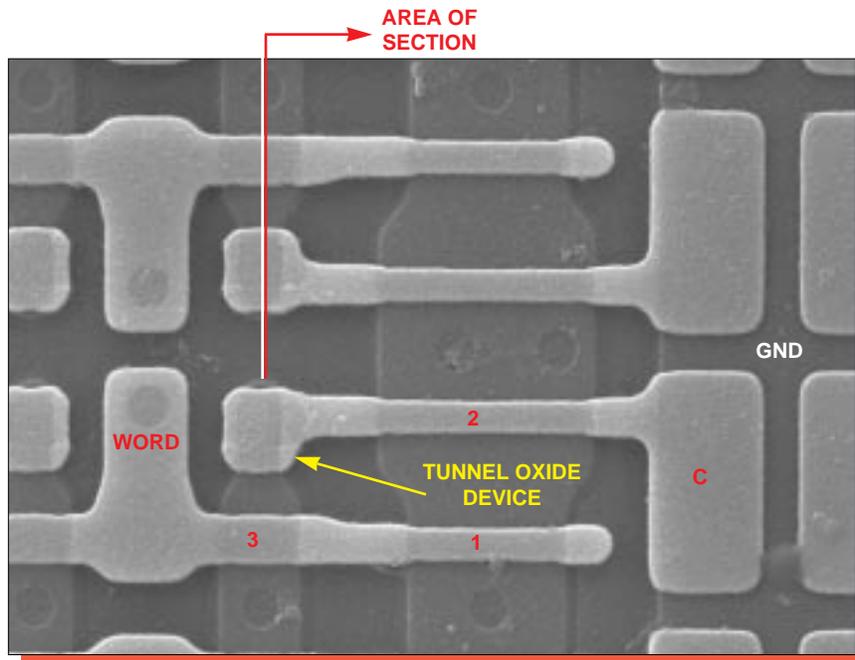


metal 2



metal 1

Figure 26a. Topological SEM views illustrating EEPROM cell array. Mag. 6500x, 0°.



polycide

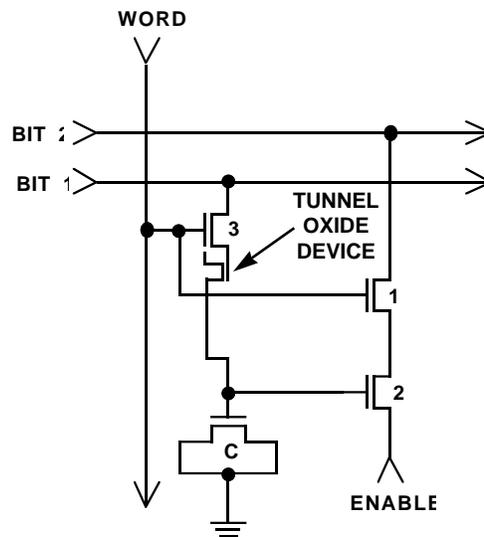
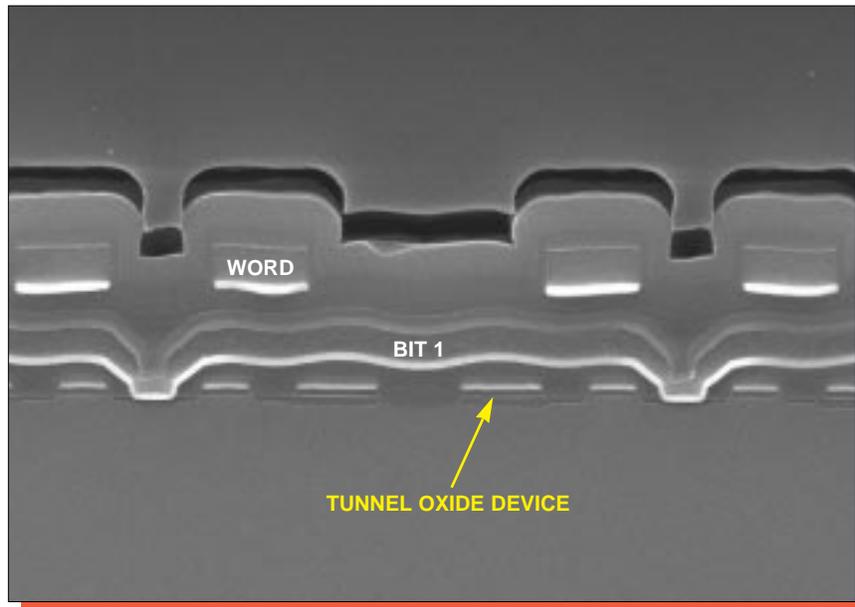
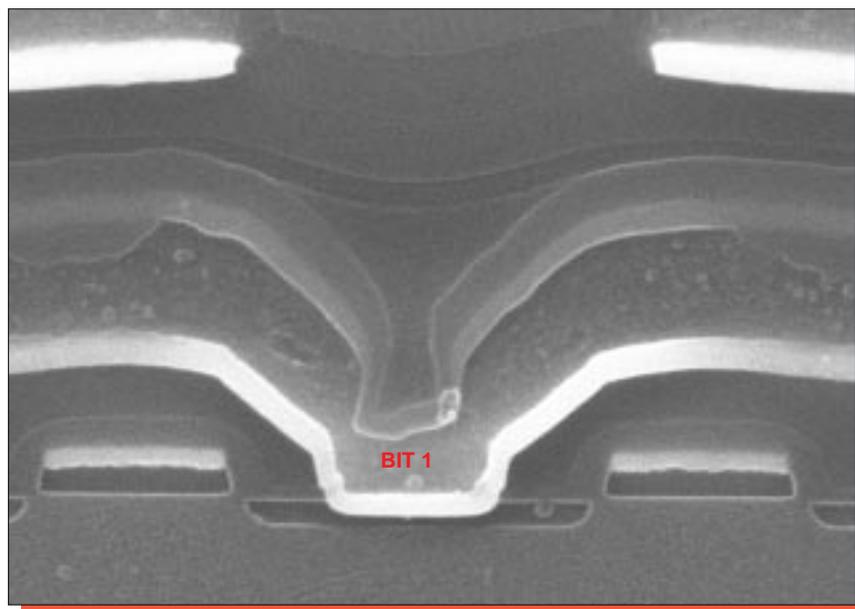


Figure 26b. Topological SEM view and schematic of EEPROM cell array. Mag. 6500x, 0°.

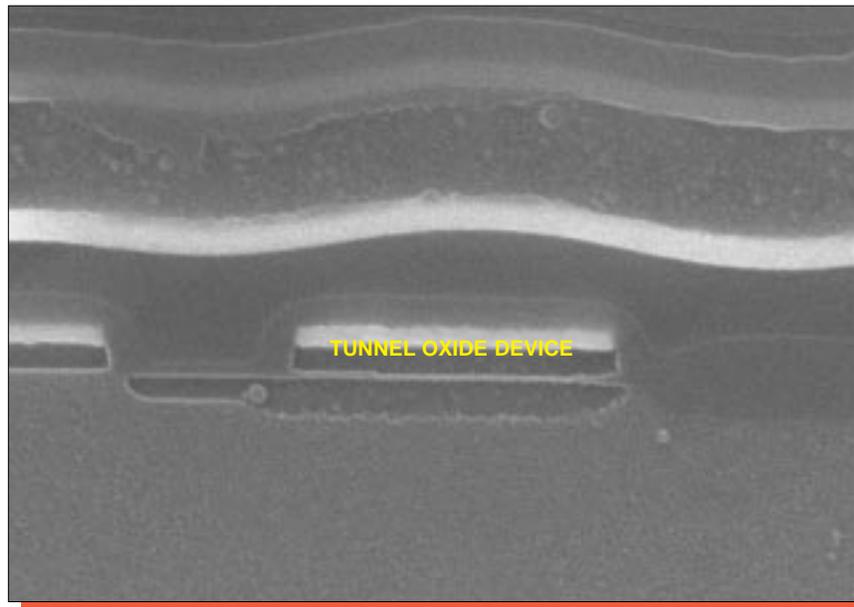


Mag. 6500x

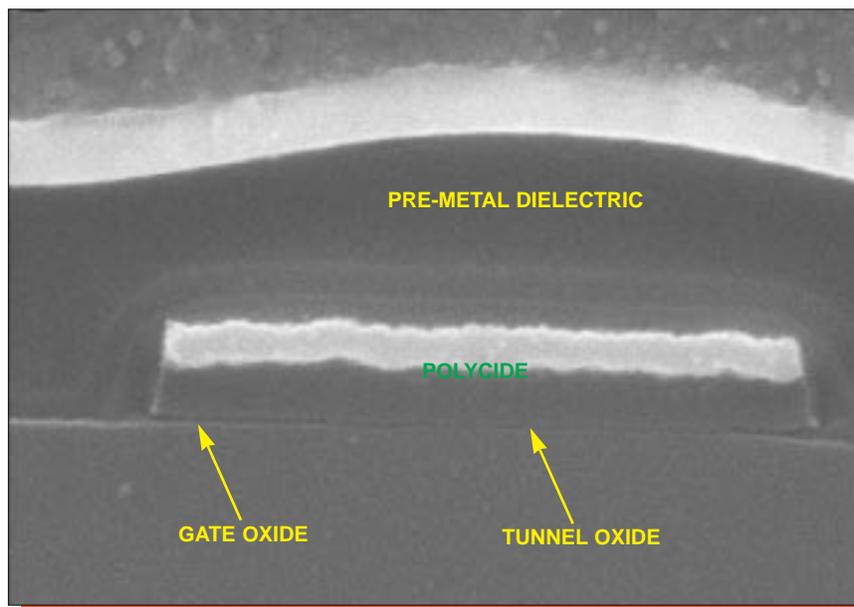


Mag. 26,000x

Figure 27. SEM section views illustrating EEPROM cell array.

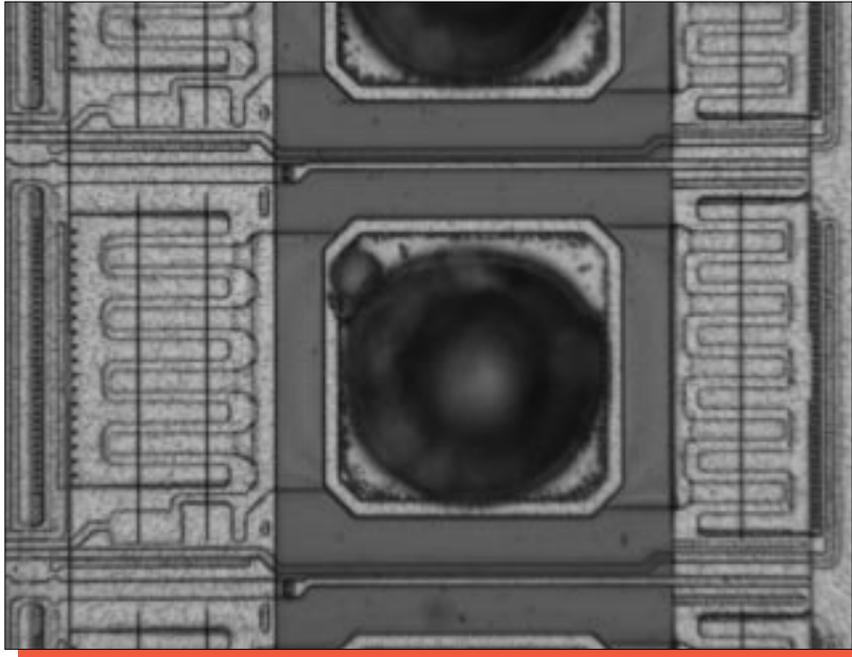


Mag. 26,000x

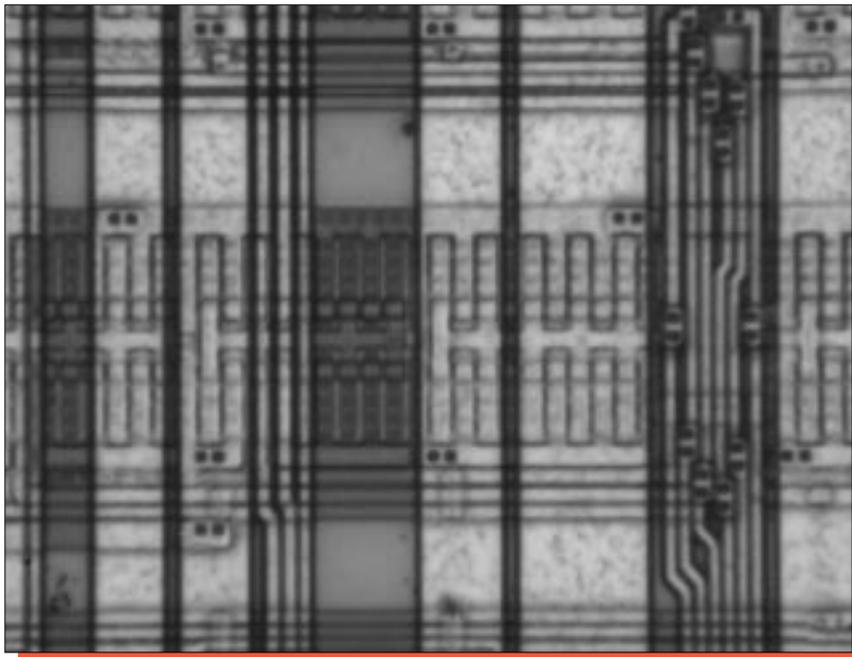


glass etch, Mag. 52,000x

Figure 27a. SEM section views illustrating the tunnel oxide device in EEPROM circuitry.

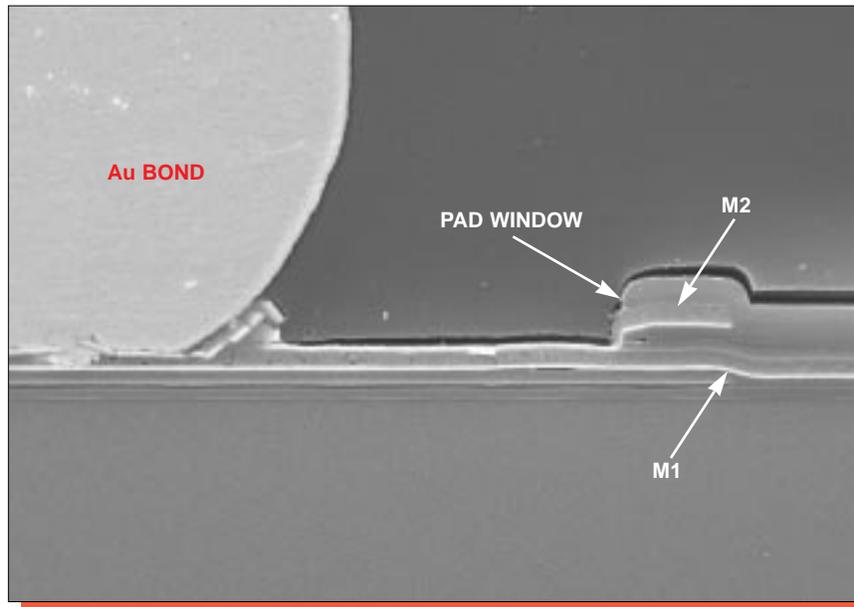


Mag. 410x

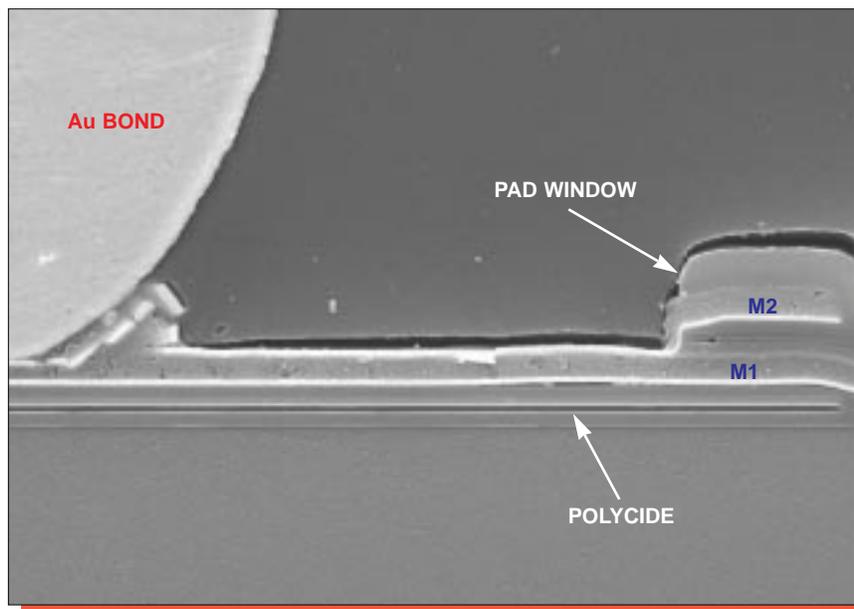


Mag. 1000x

Figure 28. Optical views illustrating I/O structure and typical circuitry.



Mag. 3250x



Mag. 5000x

Figure 29. SEM section views of bond pad structure.