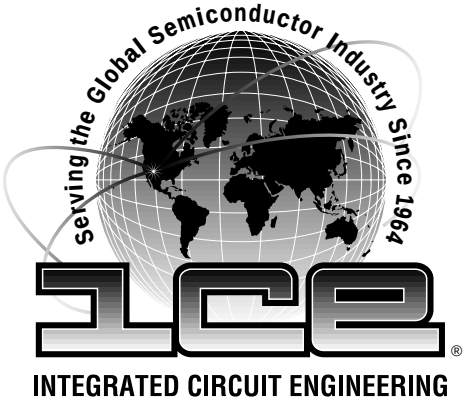
Construction Analysis

Mitsubishi M5M465405AJ
64Mbit DRAM (16M x 4 bit)

Report Number: SCA 9712-566



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INTRODUCTION

This report describes a construction analysis of the Mitsubishi M5M465405AJ 64-megabit DRAM (16M x 4 bit). Three devices were supplied for the analysis. They were packaged in 32-pin Small Outline J-lead (SOJ) packages.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 2 aluminum thinning up to 95 percent[2] at via edges (Figure 13).

Special Features:

- Four layers of polysilicon. Poly 2 was used as interconnect in the decode areas and bit lines in the array.
- Sub-micron gate lengths (0.4 micron).
- Textured poly capacitor structure in array. Cell size of 1.28 microns^2.

Noteworthy Items:

- The capacitor structure in the cell was changed from the previously analyzed 64M-bit DRAM. The individual capacitor plates had a "crown" design previously, instead of the textured plate presently being employed.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 32-pin Small-Outline J-lead packages (SOJ).
- Lead On Chip Center Bonded (LOCCB) leadframe design with die paddle.
- Dimpled header and lead-locking provisions (anchors) for added package strength.
- Multiple finger leads at power pins. Pins 4 - 7, 24 and 27 - 29 were not connected.
- Thermosonic ball bond method employing 1.1 mil O.D. gold wire.
- Sawn dicing (full depth).
- Silver-epoxy die attach.
- Polyimide die coat.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing twin wells in a P substrate (no epi).
- Final passivation: Passivation consisted of a thick layer of nitride.
- Metallization: Two levels of aluminum interconnect were used. Metal 2 employed a titanium-nitride cap and barrier layer. Metal 1 employed a titanium-nitride cap and no barrier. Both metal levels were patterned by a dry etch of good quality. Standard vias were employed with metal 2 and tungsten plugs were used at all metal 1 to silicon contacts. The plugs were lined with titanium-nitride. Poly 2 (polycide) was used as a metal substitute in the decode and array.

TECHNOLOGY DESCRIPTION (continued)

- Intermetal dielectric: The intermetal dielectric consisted of two layers of deposited glass with a spin-on-glass (SOG) between to aid in planarization. The SOG layer had been subjected to an etchback.

- Pre-metal glass: Several layers of CVD glass and densified oxides.

- Polysilicon: Four layers of polysilicon were used. Poly 3 and 4 (no silicides) were used exclusively in the cell array and for fuses. Poly 4 (sheet) formed the common plate of the capacitors in the array and the redundancy fuses. Poly 3 formed the individual capacitor plates in the array and was textured. Poly 1 and 2 employed tungsten silicide; poly 2 was used as a layer of interconnect in the decode areas and as bit lines in the array, poly 1 was used for all gates on the die.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and appeared to have been partially removed. Diffusions were not silicided.

- Isolation: LOCOS (local oxide). A notch at the top was noted in the oxide at well boundaries.

- Wells: Twin-wells employed in a P substrate (no epi). The P-wells could not be delineated in cross section.

- Buried contacts: Poly 2 and 3 contacted diffusion in the decode and array circuitry.

- Fuses: Redundancy fuses were made with poly 4. Some laser blown fuses were present. N+ guardbands surrounded the fuse blocks. A passivation cutout was present over the fuses.

TECHNOLOGY DESCRIPTION (continued)

- Memory cells: The memory cells consisted of a stacked capacitor DRAM design employing four poly layers. Metal 1 formed “piggyback” word lines. Poly 4 was a thin sheet which formed the top plate of all capacitors in the array and was tied to a memory enable. Poly 3 was used to form the individual plates of the capacitors which was connected to one side of the select gates. Poly 2 (polycide) formed the bit lines and poly 1 (polycide) was used to form the word lines and select gates. The capacitor dielectric was probably oxide-nitride; however, positive identification was beyond the scope of the analysis.

ANALYSIS RESULTS I

Assembly: **Figures 1, 2, 7 and 8**

Questionable Items[1]: None.

Special Items:

- Lead On Chip Center Bonded (LOCCB) leadframe design with die paddle.

General Items:

- Devices were packaged in 32-pin plastic Small Outline J-Lead packages (SOJ).

- Overall package quality: Normal. No defects were found on the external or internal portions of the packages. No gaps were noted at lead exits. A dimpled paddle was used for added package strength.

- Wirebonding: Thermosonic ball bond method using 1.1 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 11). Wire spacing and placement was also good. Only metal 2 formed the bond pad structure.

- Die attach: Silver-epoxy of normal quantity and quality.

- Die dicing: Die separation was by sawing (100 percent) and showed normal quality workmanship. No large chips or cracks were present at the die surface. Test pads and patterns were present in the scribe lanes.

[1]These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design: **Figures 3 - 37**

Questionable Items[1]:

- Metal 2 aluminum thinning up to 95 percent[2] at via edges (Figure 13).

Special Features:

- Four layers of polysilicon. Poly 2 was used as interconnect in the decode areas and bit lines in the array.
- Sub-micron gate lengths (0.4 micron).
- Textured capacitor structures in array.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate (no epi).
- Design and layout: Die layout was clean and efficient. No mask copyright markings were present on the die. Alignment was good at all levels.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.
- Final passivation: Passivation consisted of a thick layer of nitride. Integrity tests indicated defect-free passivation. The scribe lanes were cleared (possible to prevent cracks from radiating inward during dicing); however, the metal line at the die perimeter which appears to be a diode connection to the substrate was also exposed.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metallization: Two levels of metal defined by standard dry-etch techniques. Both levels consisted of aluminum with a titanium-nitride cap. Metal 2 also used a titanium-nitride barrier. Metal 2 utilized standard vias. Metal 1 used tungsten plugs which were lined with titanium nitride. Poly 2 was used as a metal substitute in the decode and array.

- Metal patterning: As mentioned, metal layers were defined by a dry etch of good quality. Metal lines were widened around vias and contacts where needed. Via and contact coverage was 100 percent.

- Metal defects: None. No voiding, notching, or neckdown of the metal layers was found. No silicon nodules were observed following removal of the metal layers.

- Metal step coverage: Metal 2 aluminum thinned up to 95 percent at vias. The barrier metal aids in maintaining continuity. Metal 1 aluminum thinned up to 70 percent at contacts. The excessive metal 2 thinning appears to be due to the deep and small via cuts and the metal 1 thinning appears to mainly be due to the overetch of the tungsten plugs, causing a deeper hole to fill.

- Contacts: Vias were significantly overetched into the metal 1 affecting the metal step coverage mentioned above. No significant overetching of metal 1 contacts was found.

- Intermetal dielectric: Two layers of silicon-dioxide separated by a spin-on-glass (SOG) for planarization. Only the SOG appeared to have been etched back. No problems were present.

- Pre-metal glass: Two layers of reflow glass and densified oxide. No problems were found.

ANALYSIS RESULTS II (continued)

- Polysilicon: Four layers of polysilicon were used. Poly 3 and 4 (no silicides) were used exclusively in the cell array and for fuses. Poly 4 (sheet) formed the common plate of the capacitors in the array and the redundancy fuses. Poly 3 (textured) formed the individual capacitor plates in the array. Poly 1 and 2 employed tungsten silicide; poly 2 was used as a layer of interconnect in the decode areas and as bit lines in the array, poly 1 was used for all gates on the die. Definition and coverage was good. No stringers or spurs were noted.

- Isolation: Local oxide (LOCOS) etched back to be almost planar with the silicon surface. A notch was noted at the top of this oxide at the well boundaries. No problems were present at the birdsbeaks or elsewhere.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the transistors. An LDD process was used employing oxide sidewall spacers which appeared to have been partially removed. Diffusions were not silicided. No problems were found in these areas.

- Wells: Twin-wells employed in a P substrate (no epi). Definition was normal. The P-wells could not be delineated in cross section.

- Buried contacts: Direct poly 2 and 3-to-diffusion (buried) contacts were used in the array and decode areas. No problem areas were identified.

- Fuses: Redundancy fuses were made with poly 4. Some laser blown fuses were present. N+ guardbands surrounded the fuse blocks. A passivation cutout was present over the fuses.

- Memory cells: The memory cells consisted of a stacked capacitor DRAM design employing four poly layers. Metal 1 formed “piggyback” word lines. Poly 4 was a thin sheet which formed the top plate of all capacitors in the array and was tied to a memory enable. Poly 3 was used to form the individual plates of the capacitors which was connected to one side of the select gates. The surface of the poly 3 pedestal was textured to increase capacitor area. Poly 2 (polycide) formed the bit lines and poly 1 (polycide) was used to form the word lines and select gates. The capacitor dielectric was probably oxide-nitride. Cell size was 0.8 x 1.6 microns.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM of assembly features and passivation

Passivation integrity test

Wirepull test

Passivation removal and inspect metal 2

Delayer to metal 1 and inspect

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	N
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	G
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity	NP*
Contact coverage	G
Contact registration	G
Contact defects	G

*****_Metal 2 aluminum thinning up to 95 percent._

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

(Logo) M5M465405AJ
732CB03-5

WIREBOND STRENGTH

Wire material:	1.1 mil diameter gold
Die pad material:	Aluminum
Material at package post:	Silver
# of wires tested:	15
Bond lifts:	0
Force to break - high:	19.0g
- low:	15.0g
- avg.:	17.7g
- std. dev.	1.3

DIE MATERIAL ANALYSIS

Passivation:	A thick layer of nitride.
Metal 2:	Aluminum with a titanium-nitride cap and barrier.
Intermetal dielectric:	Two layers of silicon-dioxide with spin-on-glass (SOG) between.
Metal 1:	Aluminum with a titanium-nitride cap.
Pre-metal glass:	BPSG reflow glass and densified oxides.
Poly 1 and 2:	Tungsten-silicide on polysilicon.
Plugs:	Tungsten lined with titanium-nitride.

HORIZONTAL DIMENSIONS

Die size:	8.3 x 16.6 mm (327 x 654 mils)
Die area:	137.8 mm^2 (213,858 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.09 x 0.09 mm (3.8 x 3.8 mils)
Min pad space:	2.3 mils (0.06 mm)
Min metal 2 width:	1 micron
Min metal 2 space:	0.8 micron
Min metal 2 pitch:	1.9 micron
Min via (M2 - M1):	0.55 micron (diameter)
Min metal 1 width:	0.5 micron
Min metal 1 space:	0.4 micron
Min metal 1 pitch:	0.9 micron
Min contact:	0.35 micron (diameter)
Min poly 3 width:	0.55 micron
Min poly 3 space:	0.25 micron
Poly 3 stem:	0.2 micron (diameter)
Min poly 2 width:	0.2 micron
Min poly 2 space:	0.3 micron
Min poly 1 width:	0.4 micron
Min poly 1 space:	0.45 micron
Min gate length - N-channel:	0.4 micron
- P-channel:	0.45 micron
Cell size:	1.28 $microns^2$
Cell pitch:	0.8 x 1.6 micron

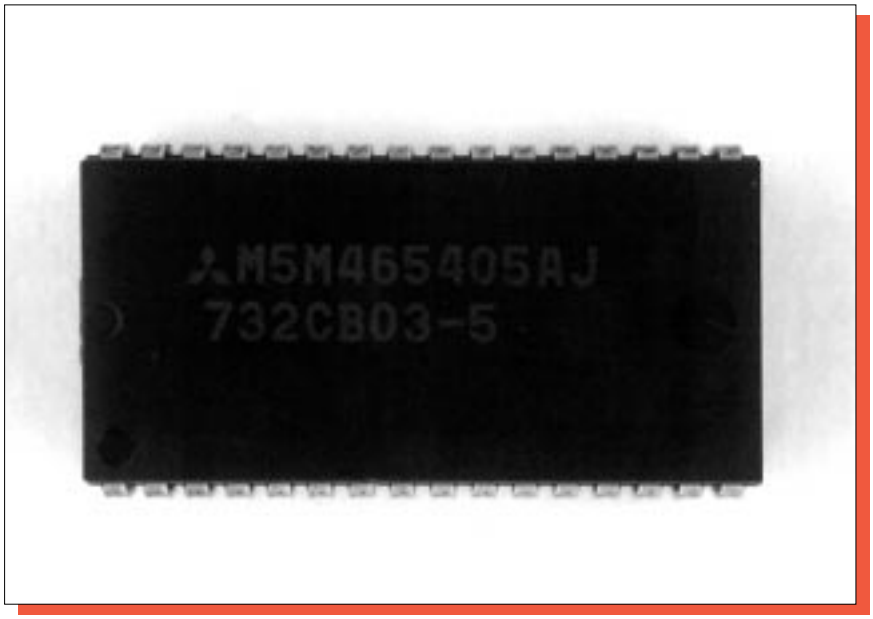
VERTICAL DIMENSIONS

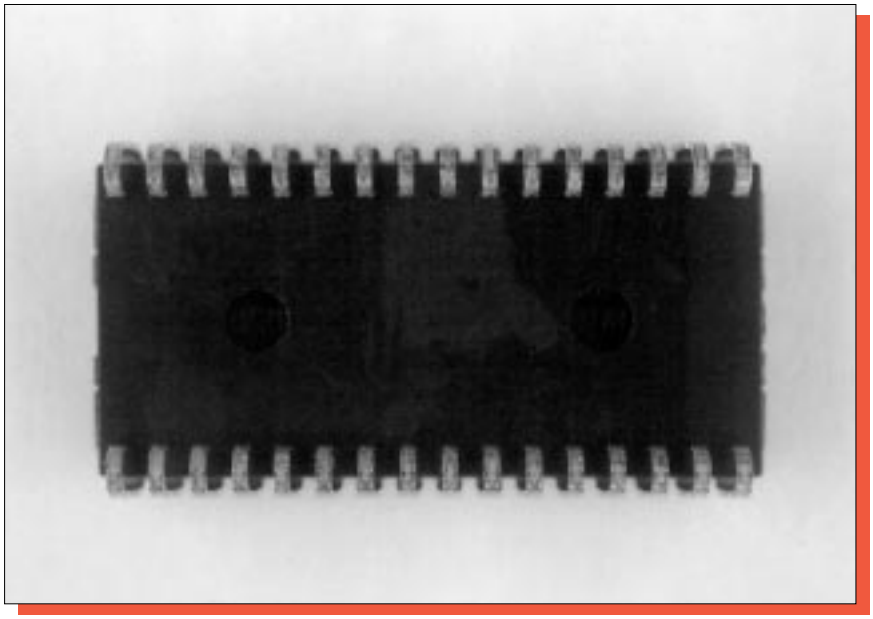
Die thickness:	0.5 mm (19.5 mils)

Layers:

Passivation:	0.8 micron
Metallization 2 - cap:	0.03 micron (approximate)
- aluminum:	0.8 micron
- barrier:	0.06 micron
Intermetal dielectric - glass 2:	0.55 micron
- SOG:	0 - 0.4 micron
- glass 1:	0.15 micron
Metallization 1 - cap:	0.05 micron
- aluminum:	0.35 micron
- plugs:	1.0 micron
Pre-metal glass:	1.3 micron
Poly 4:	0.13 micron
Poly 3 - body:	0.6 micron
- stem:	0.8 micron
Poly 2 - silicide:	0.04 micron (approximate)
- poly:	0.07 micron
Poly 1 - silicide:	0.1 micron
- poly:	0.08 micron
Local oxide:	0.3 micron
N+ S/D diffusion:	0.13 micron
P+ S/D diffusion:	0.12 micron
N-well:	2 microns (approximate)

INDEX TO FIGURES





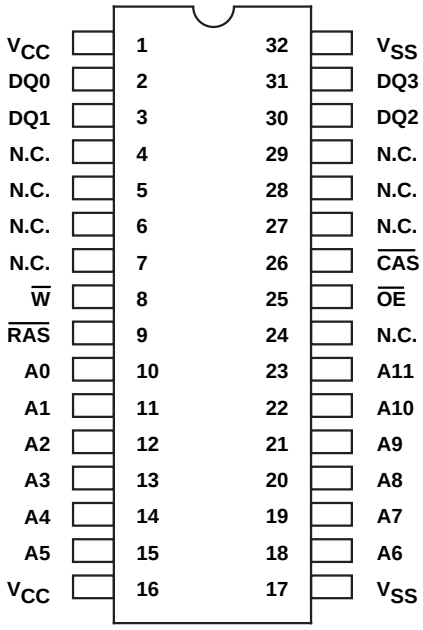


Figure 1. Package photographs and pinout of the Mitsubishi M5M465405AJ 64Mbit DRAM. Mag. 4x.

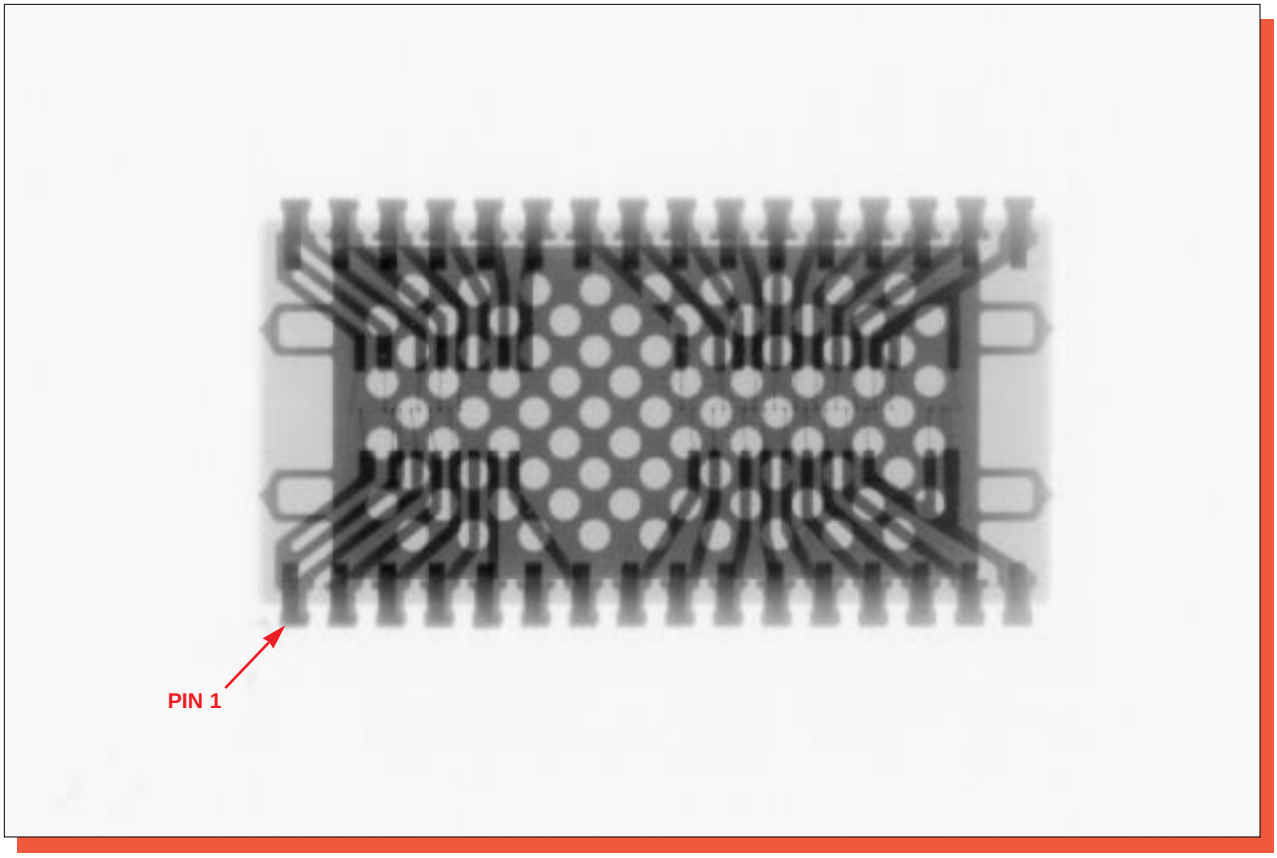


Figure 2. X-ray of the Mitsubishi 64Mbit DRAM. Mag. 5x.

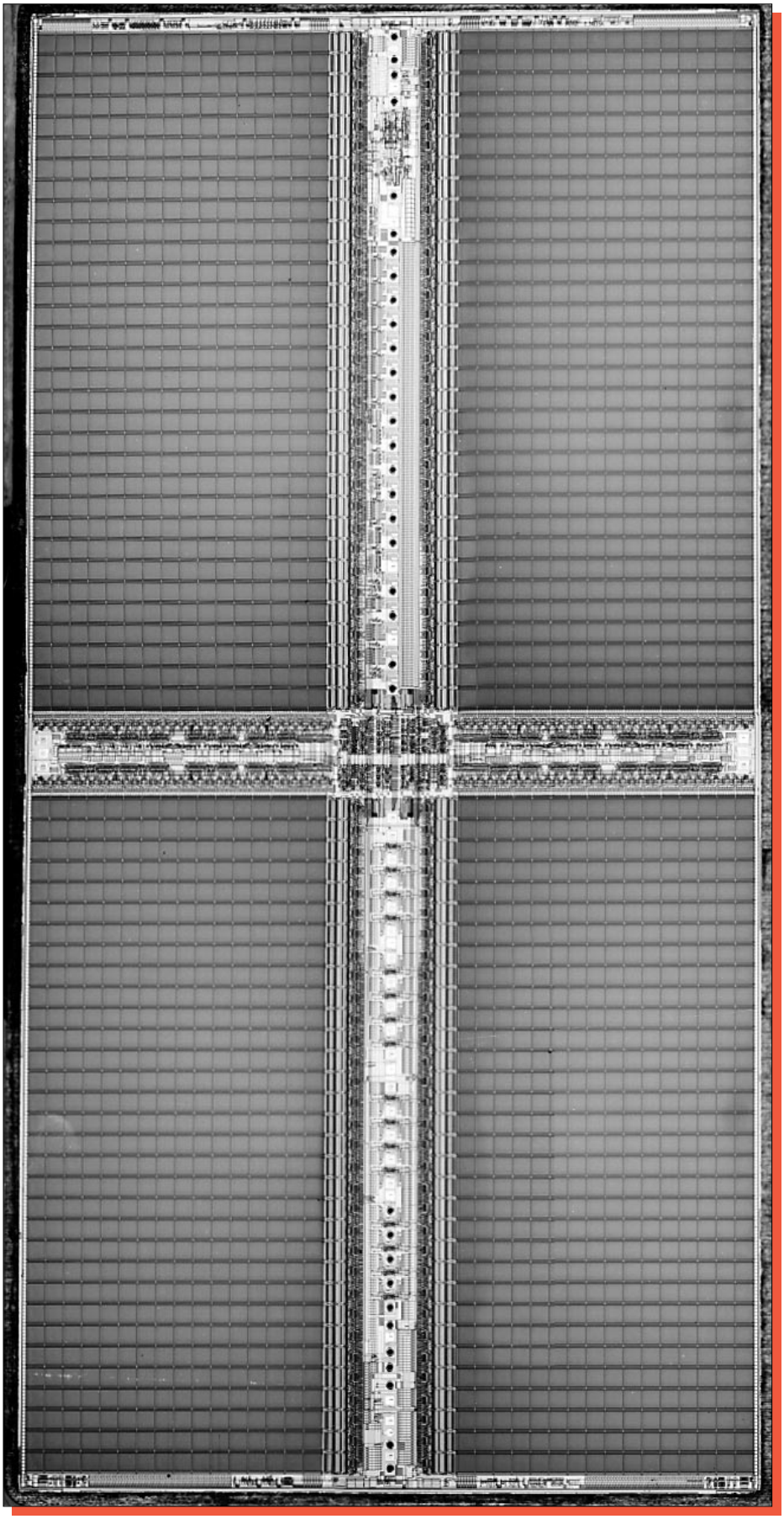


Figure 3. Whole die photograph of the Mitsubishi M5M465405AJ 64Mbit DRAM. Mag. 13x.

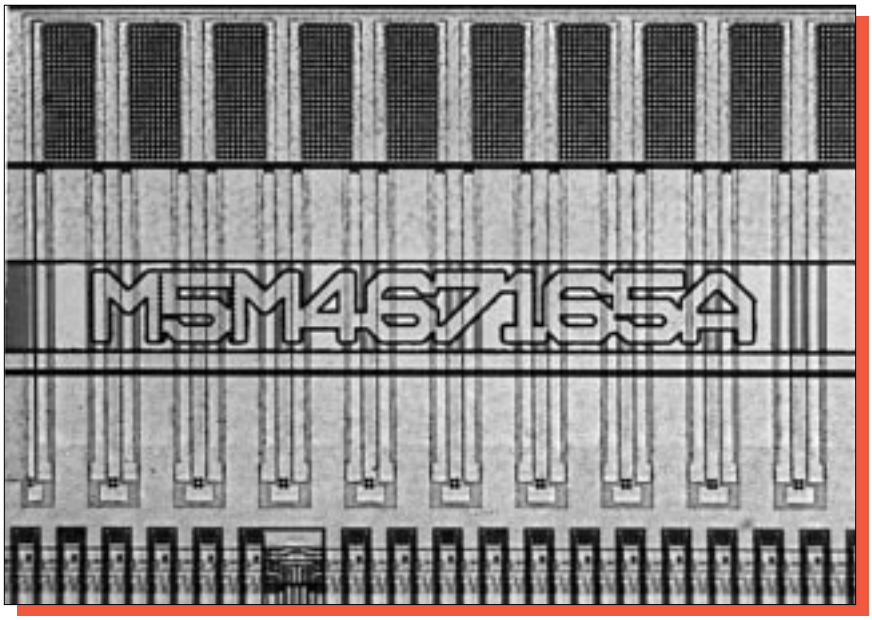


Figure 4. Die identification markings. Mag. 500x.

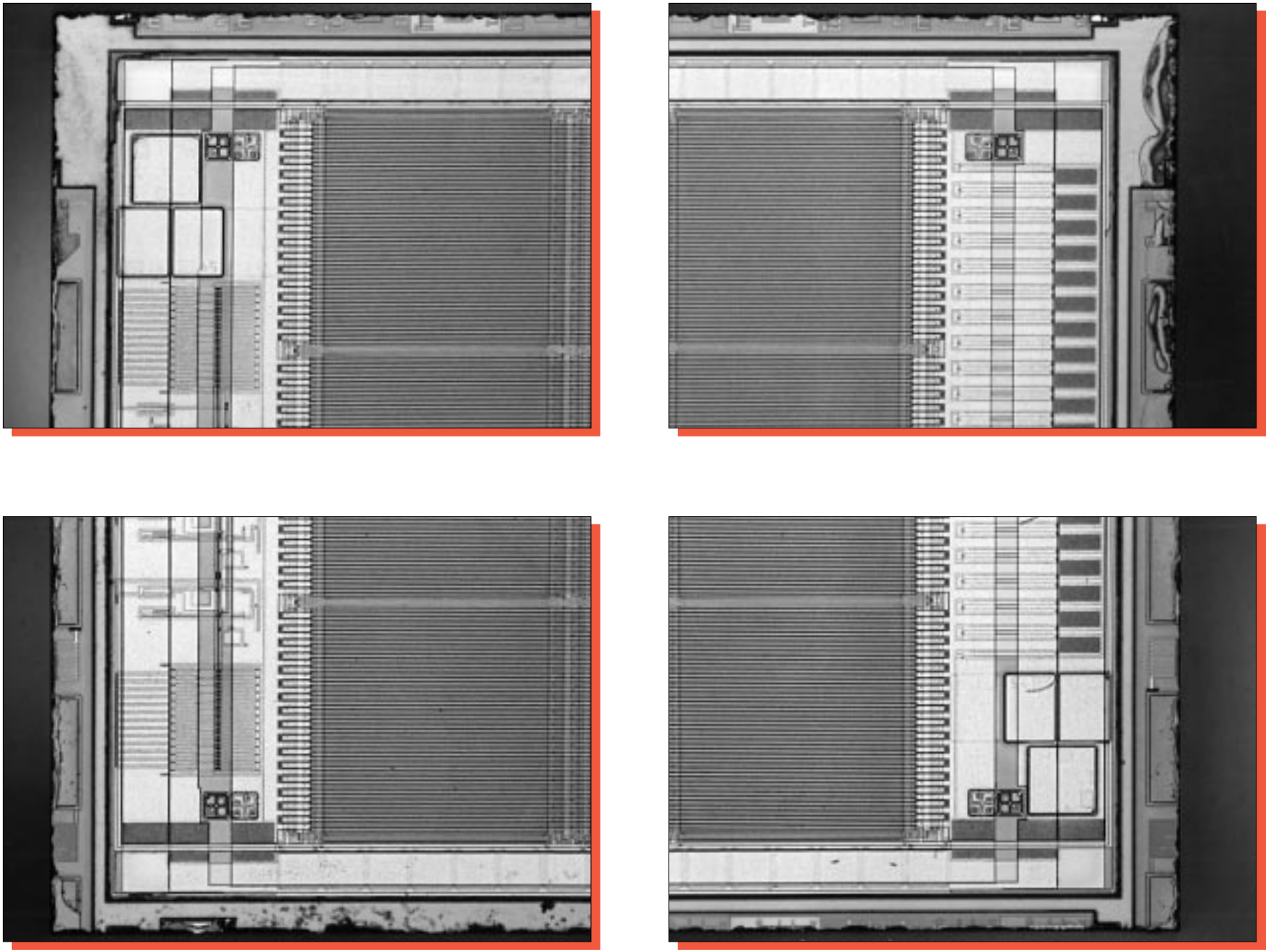
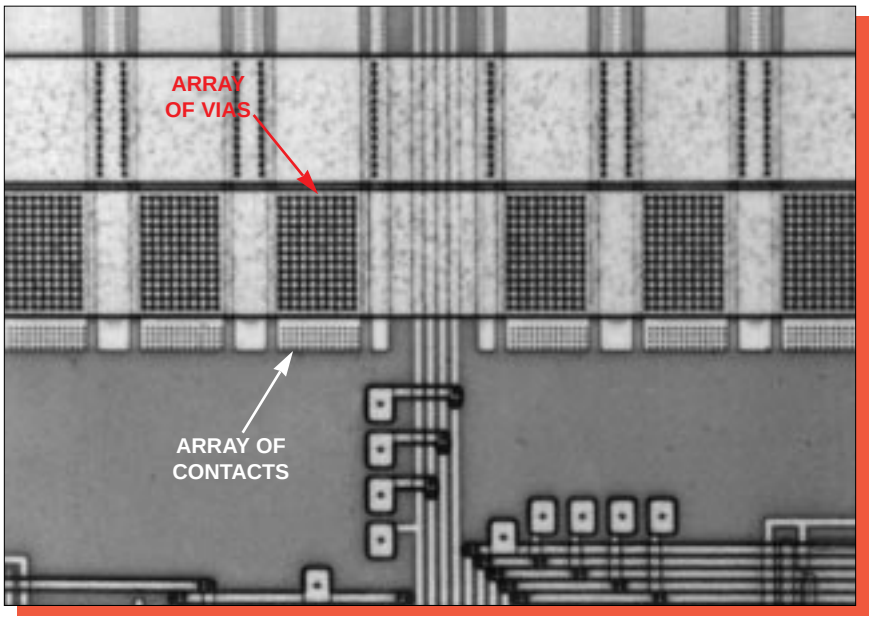


Figure 5. Optical views of the die corners. Mag. 200x.



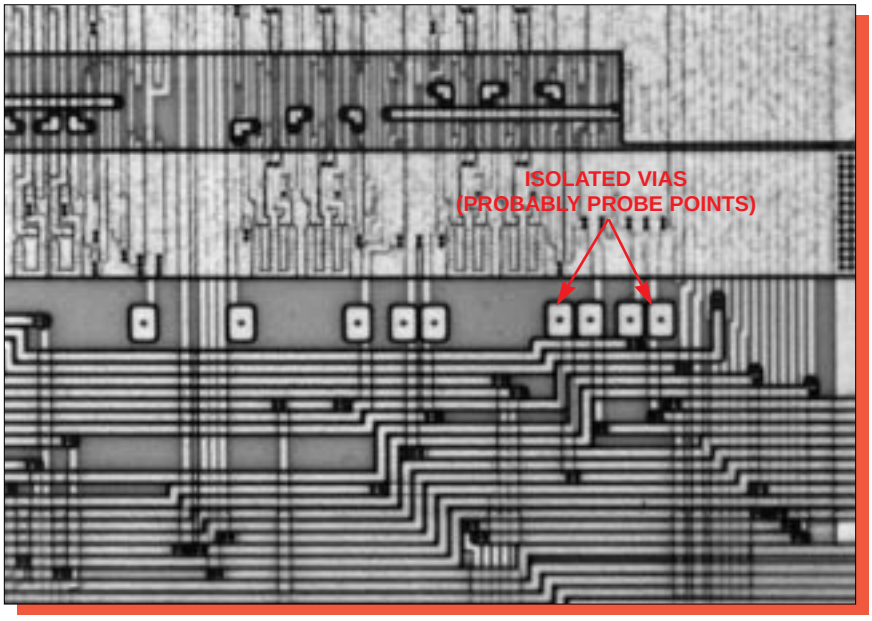
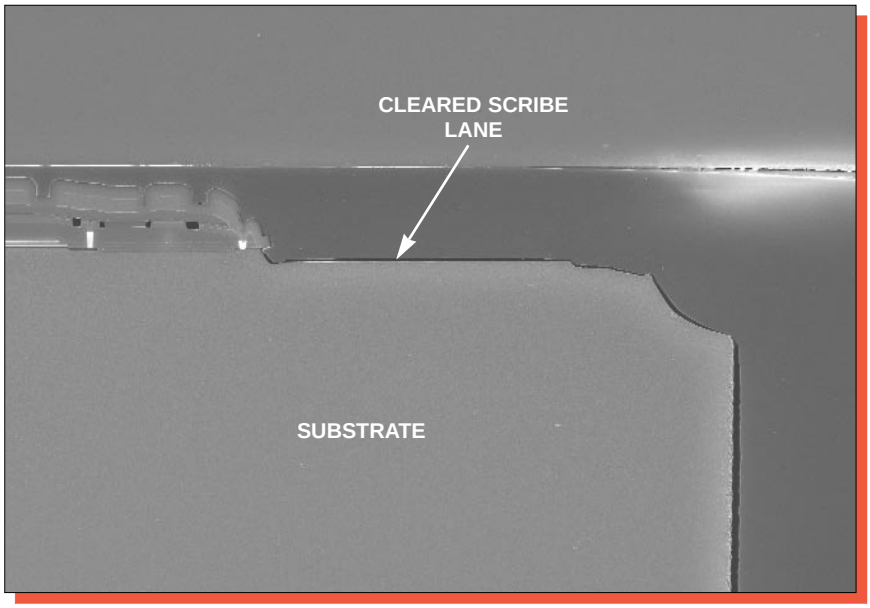
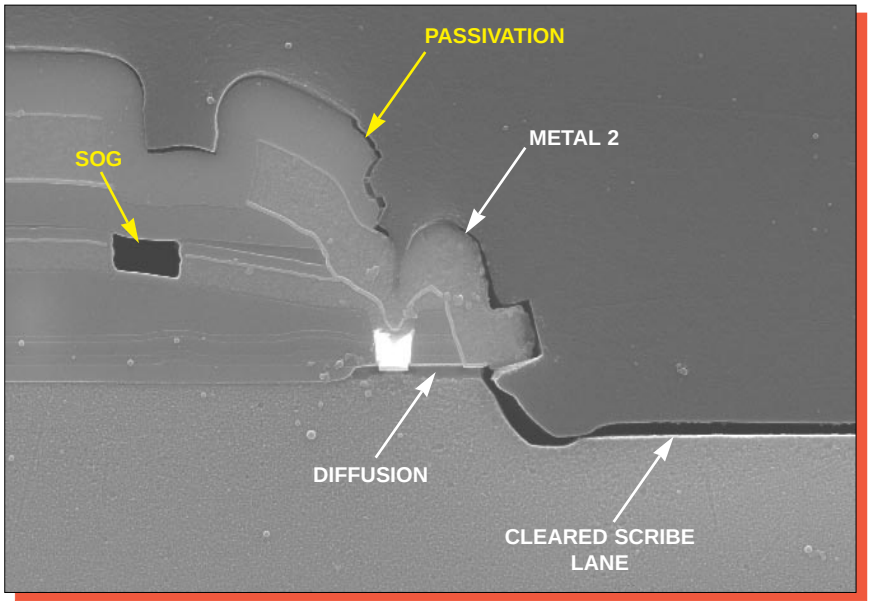


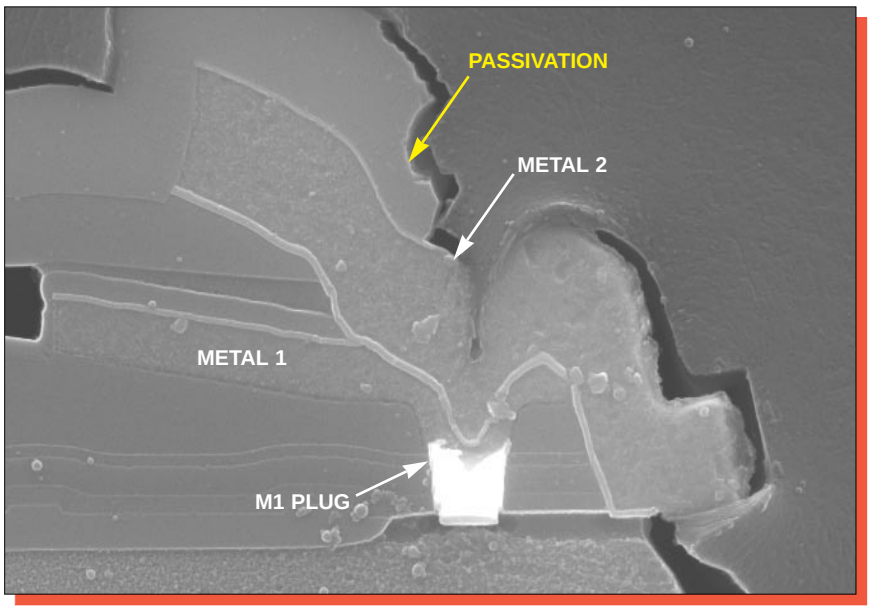
Figure 6. Optical views of design features. Mag. 800x.



Mag. 2000x

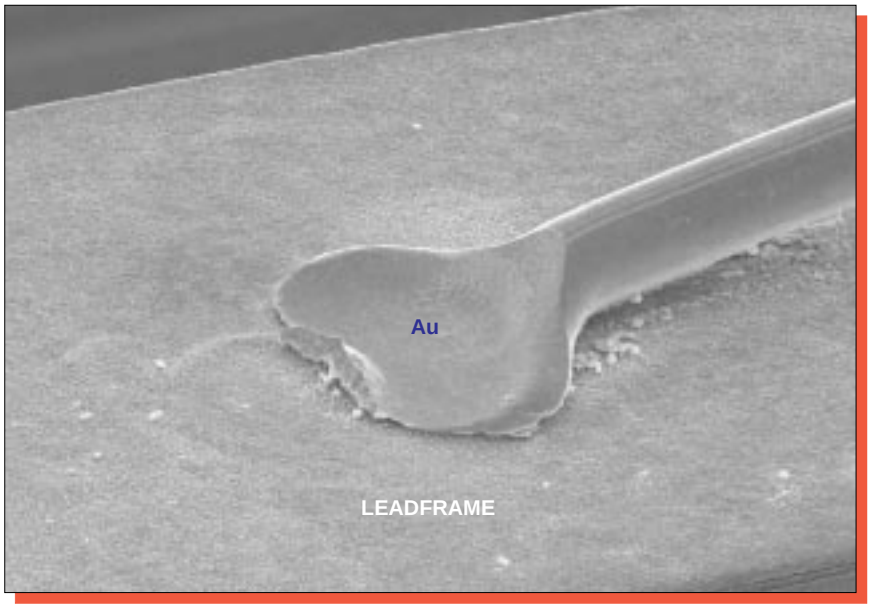


Mag. 10,000x

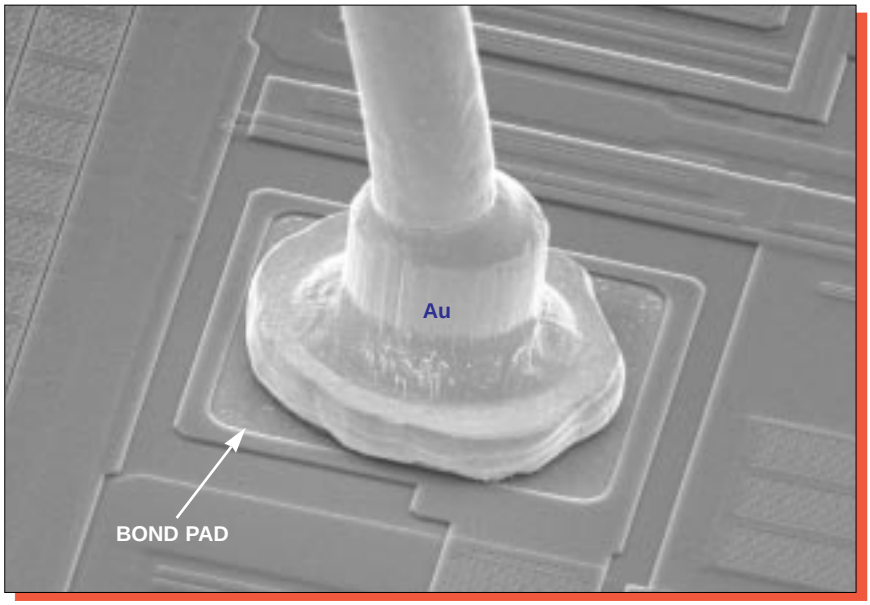


Mag. 20,000x

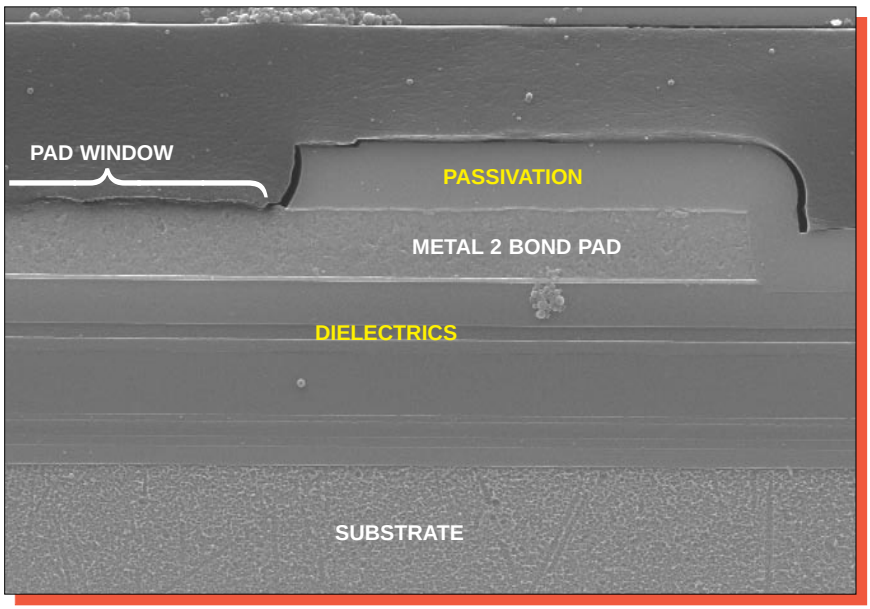
Figure 7. SEM section views of the edge seal structure.



Mag. 460x, 60°

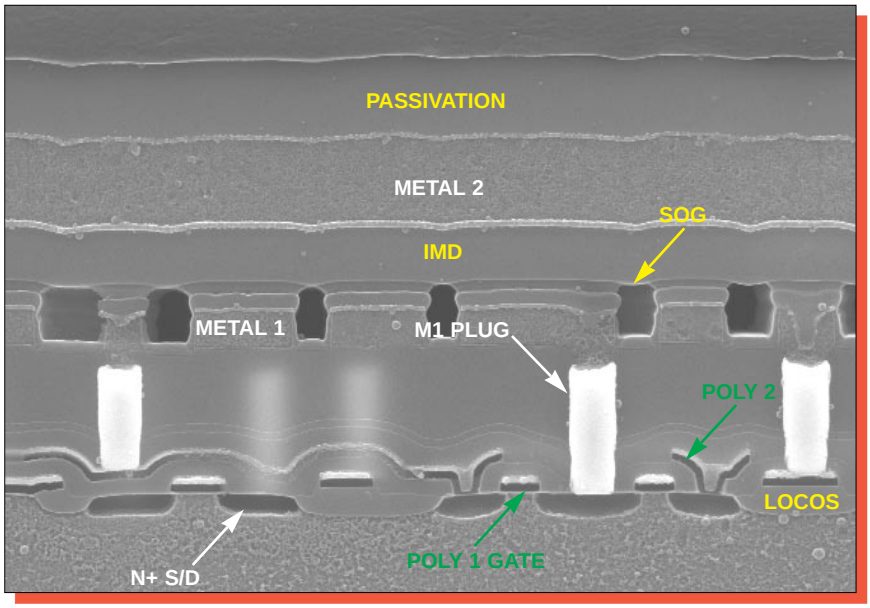


Mag. 570x, 60°

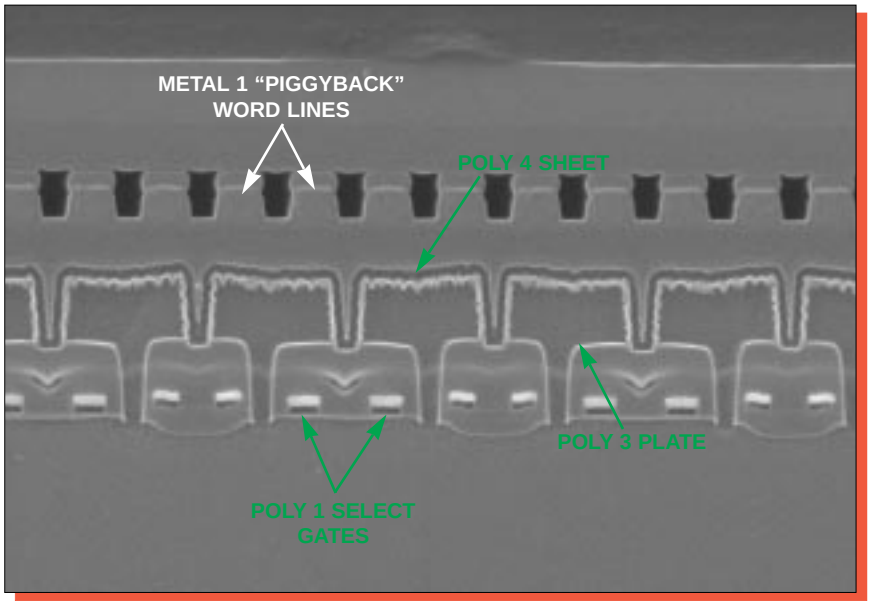


Mag. 10,400x

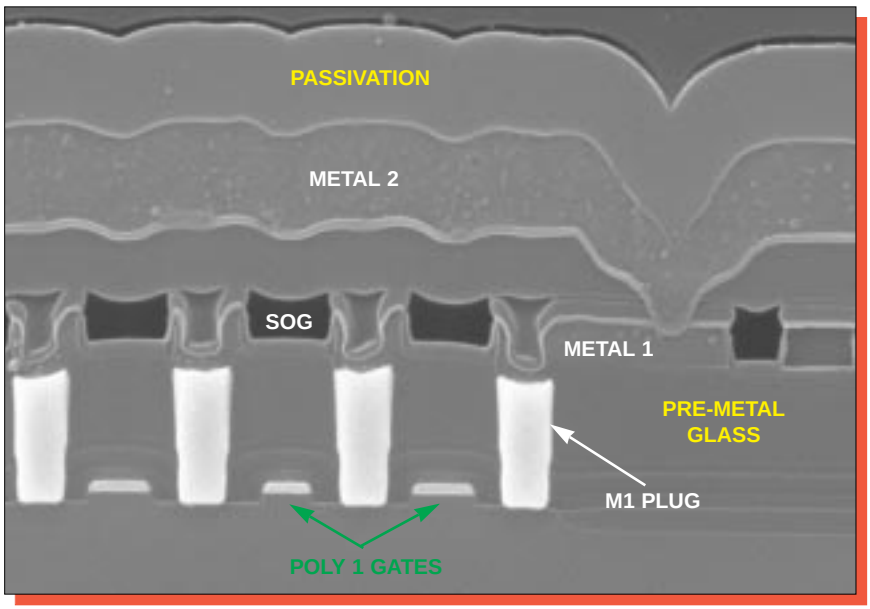
Figure 8. SEM views of typical wirebonds and bond pad structure.



Mag. 13,000x

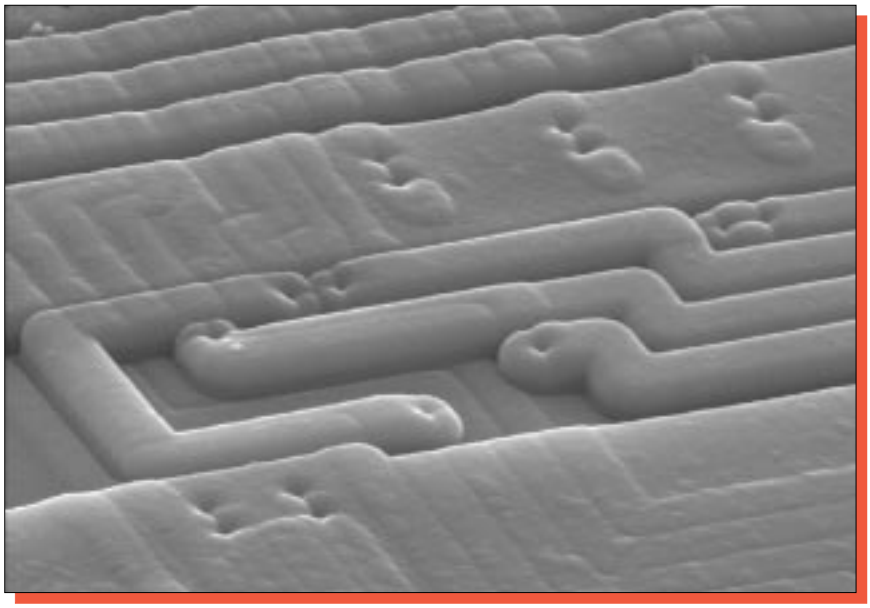


cell array,
Mag. 13,000x

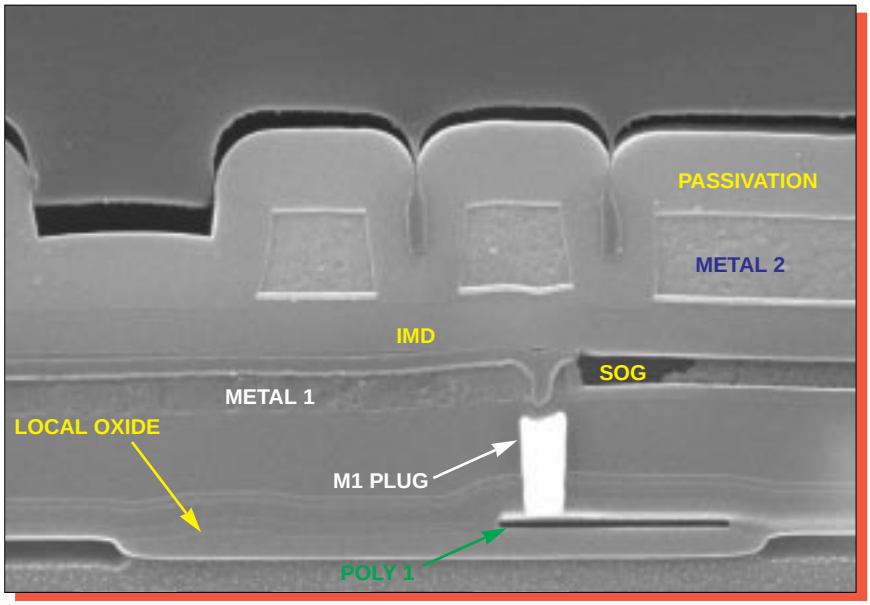


glass-etch,
Mag. 15,400x

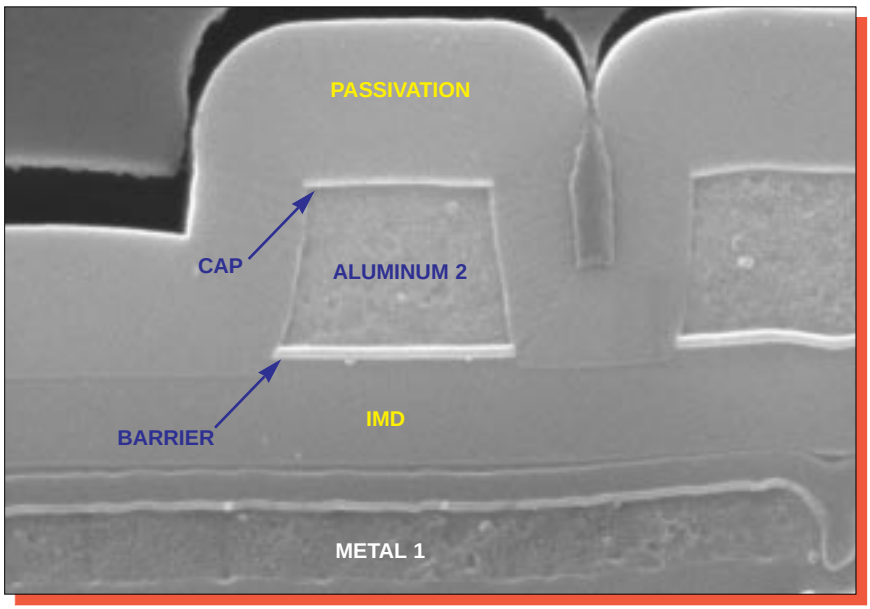
Figure 9. SEM section views illustrating general device structure.



Mag. 5000x, 60°

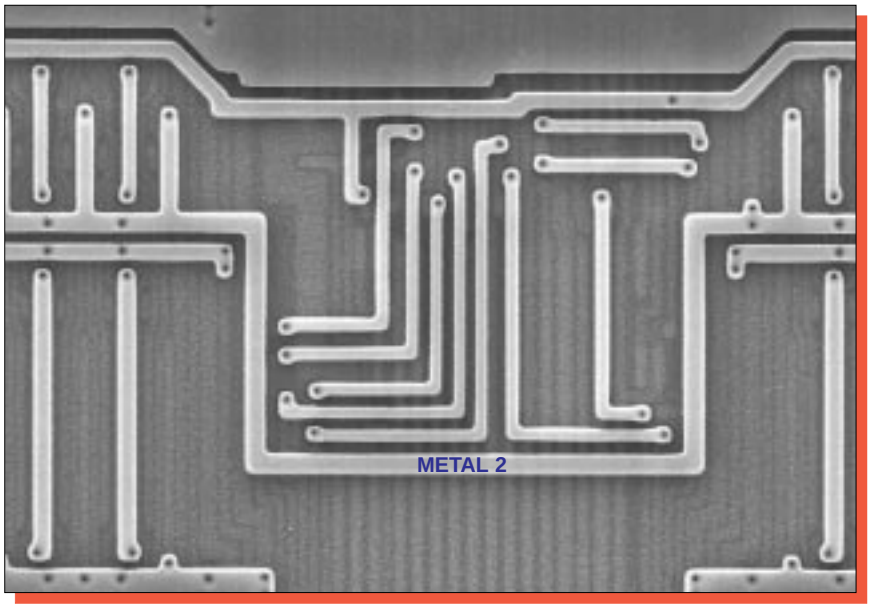


Mag. 13,000x



Mag. 26,000x

Figure 10. SEM views of final passivation coverage and metal 2 line profiles.



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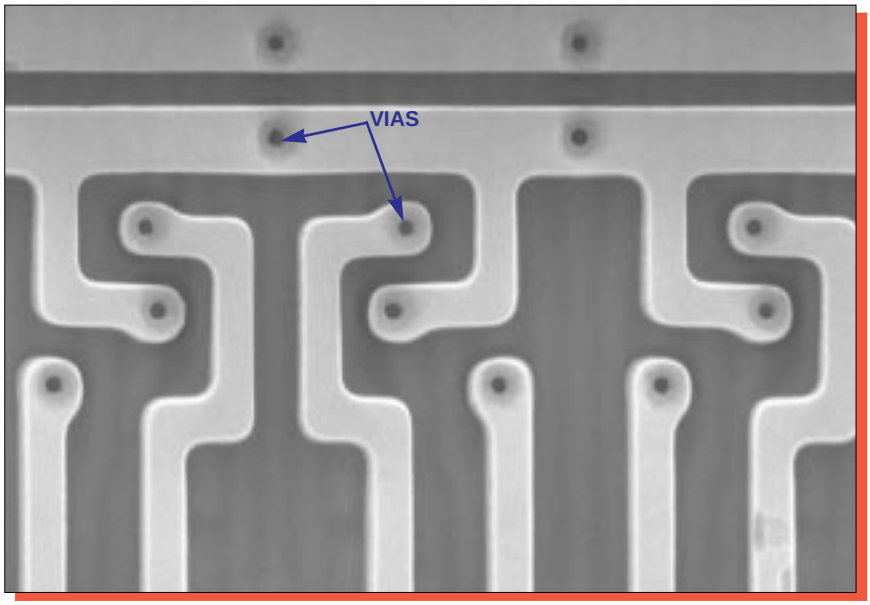

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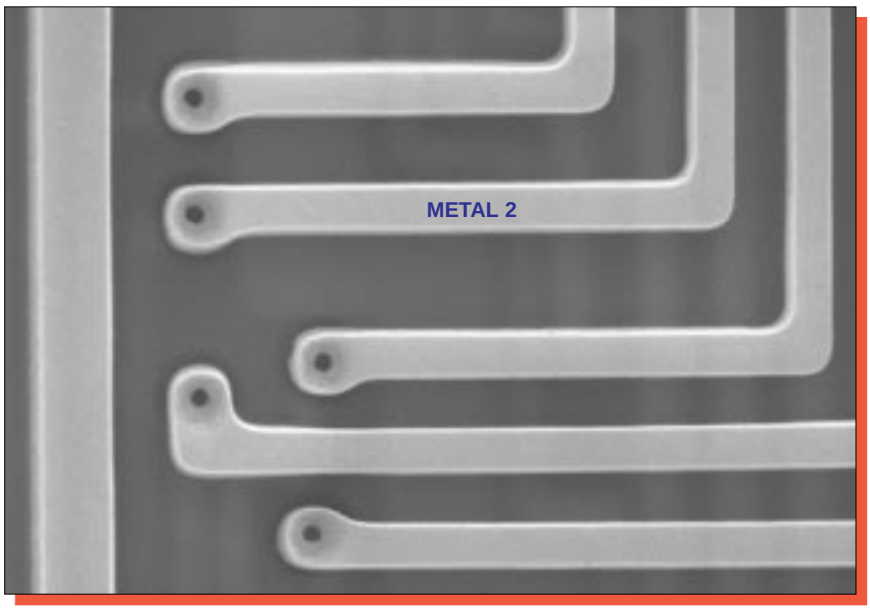
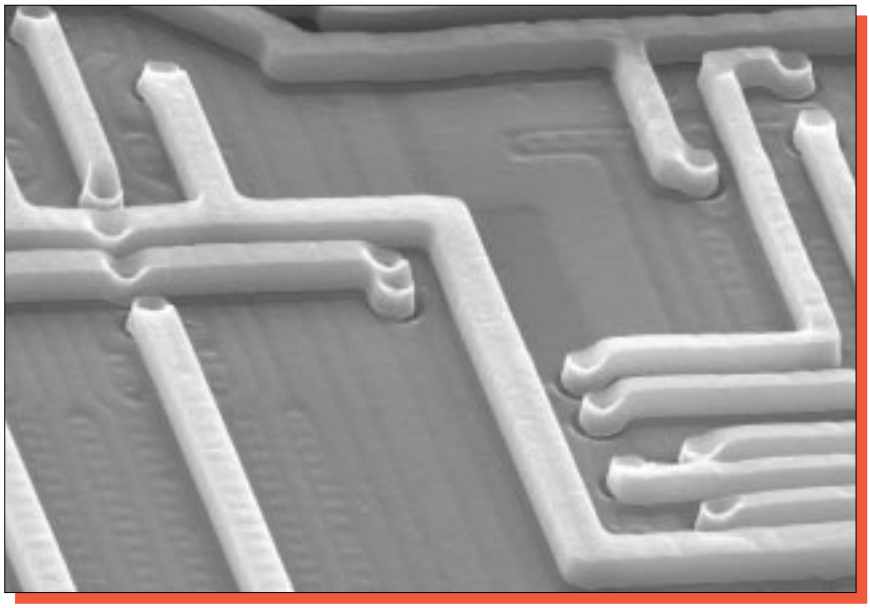
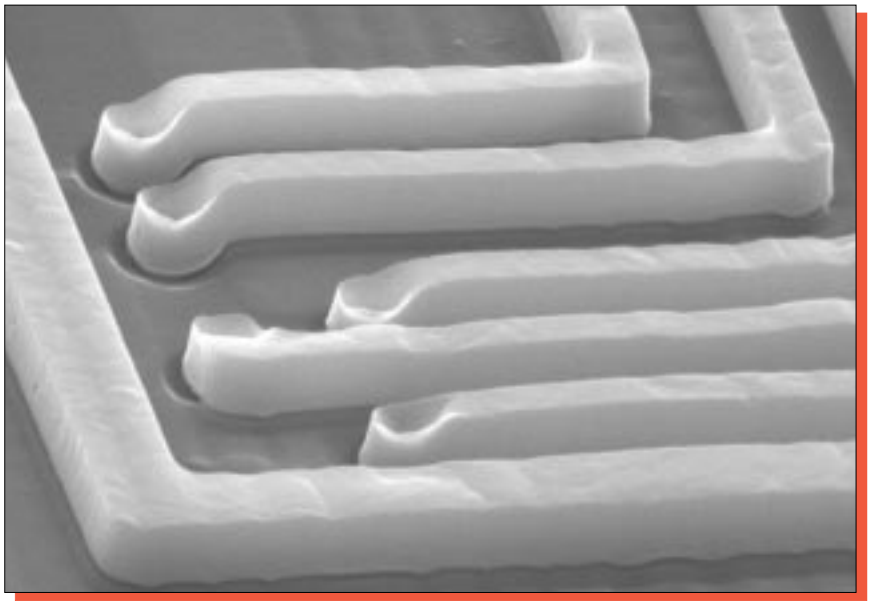


Mag. 8000x

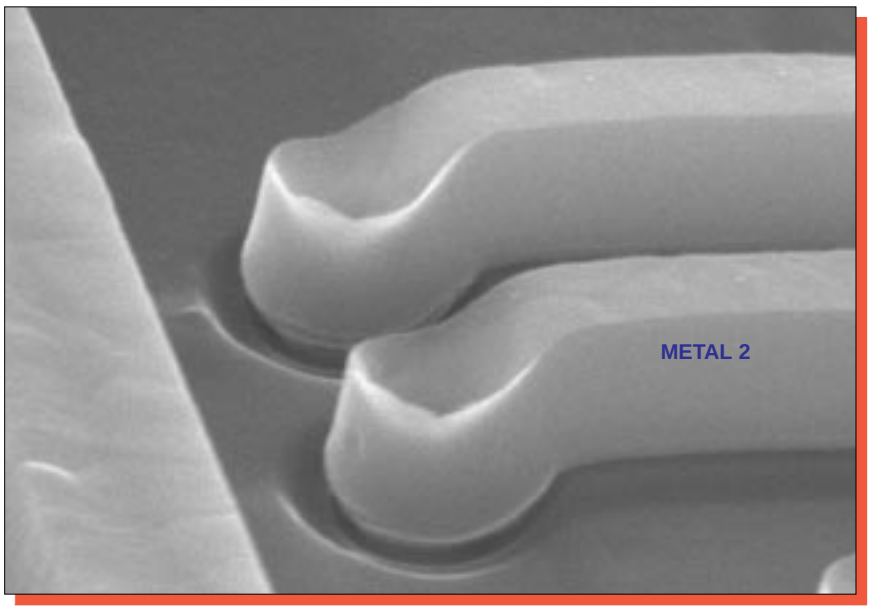
Figure 11. Topological SEM views of metal 2 patterning. 0°.



Mag. 5000x

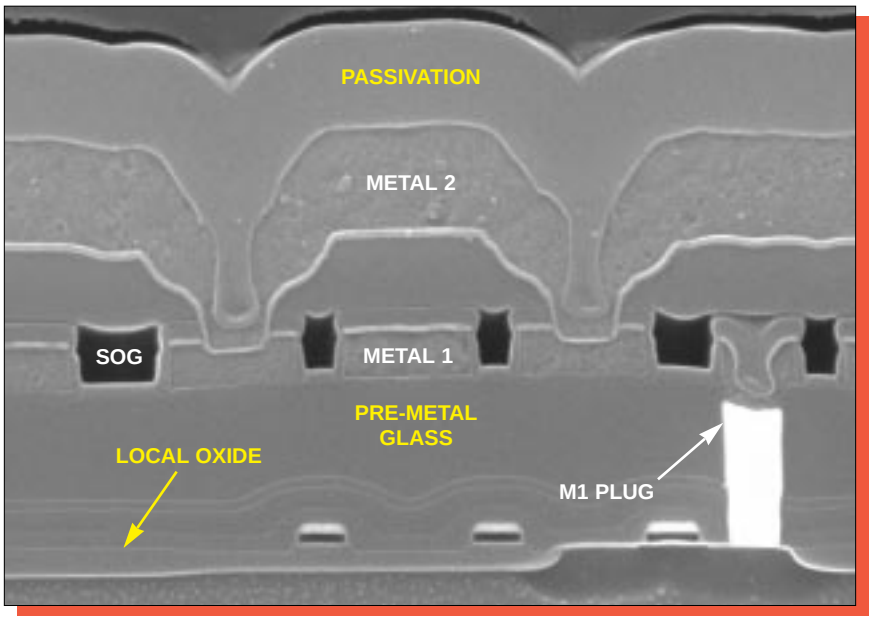


Mag. 10,000x

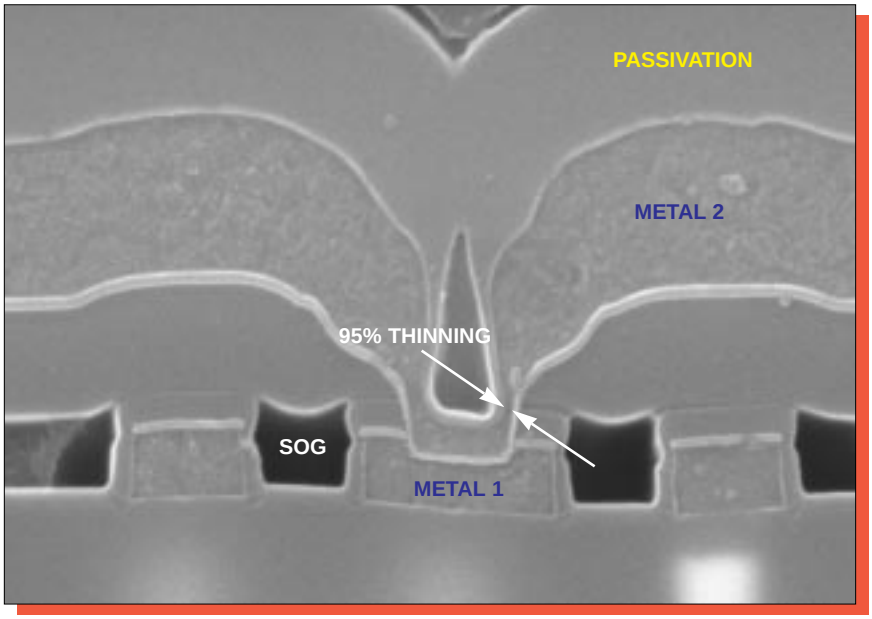


Mag. 24,000x

Figure 12. SEM views illustrating general metal 2 integrity. 60°.

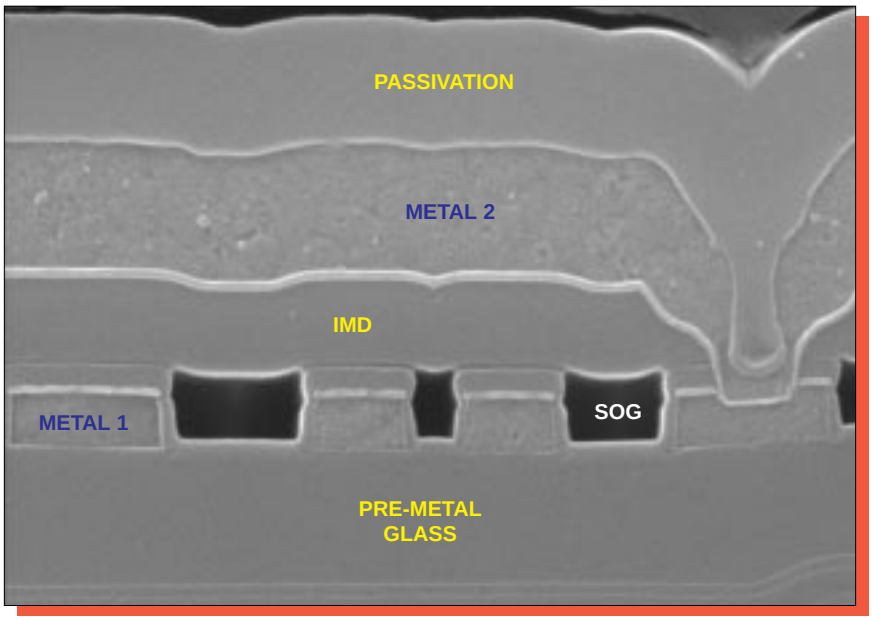


Mag. 16,800x

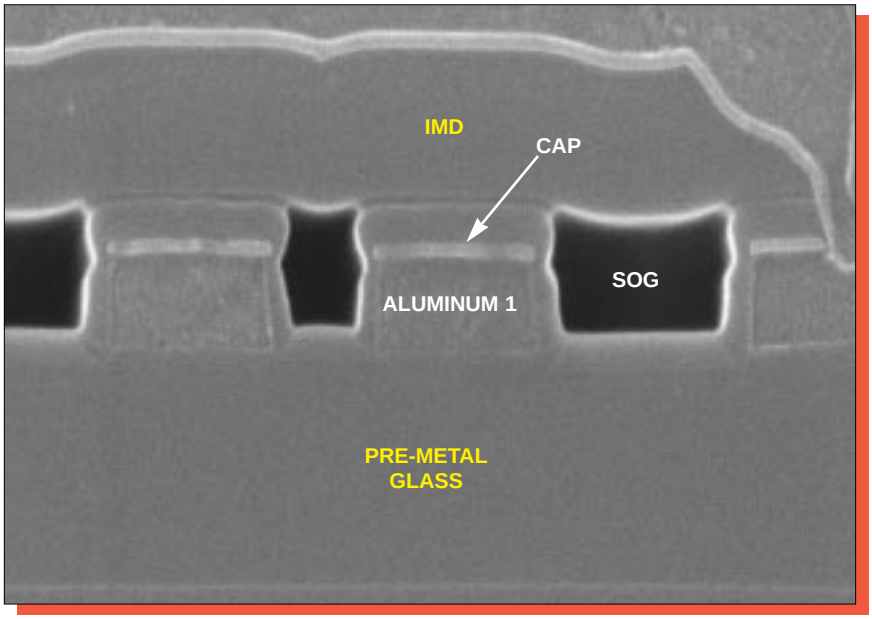


Mag. 26,000x

Figure 13. SEM section views illustrating metal 2-to-metal 1 vias.

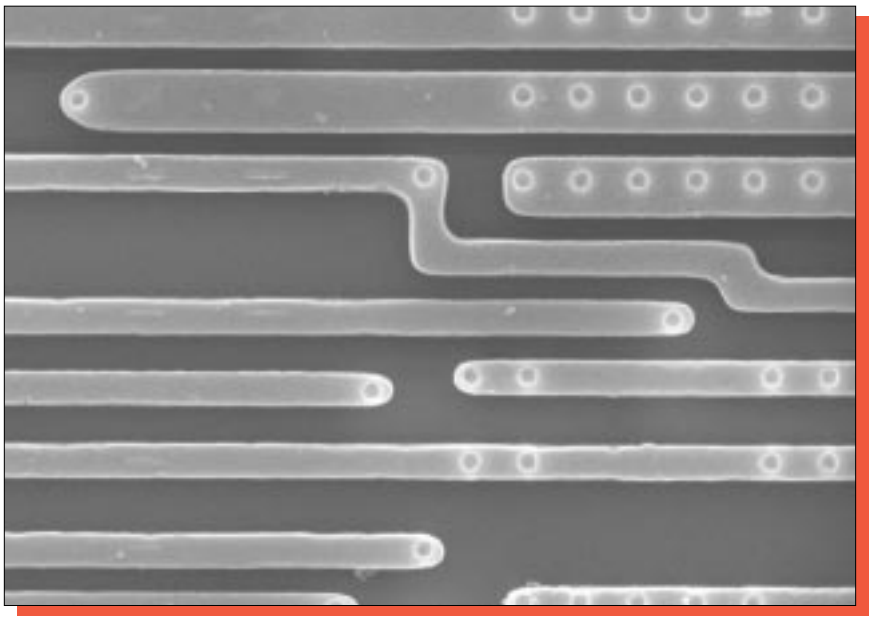


Mag. 20,800x

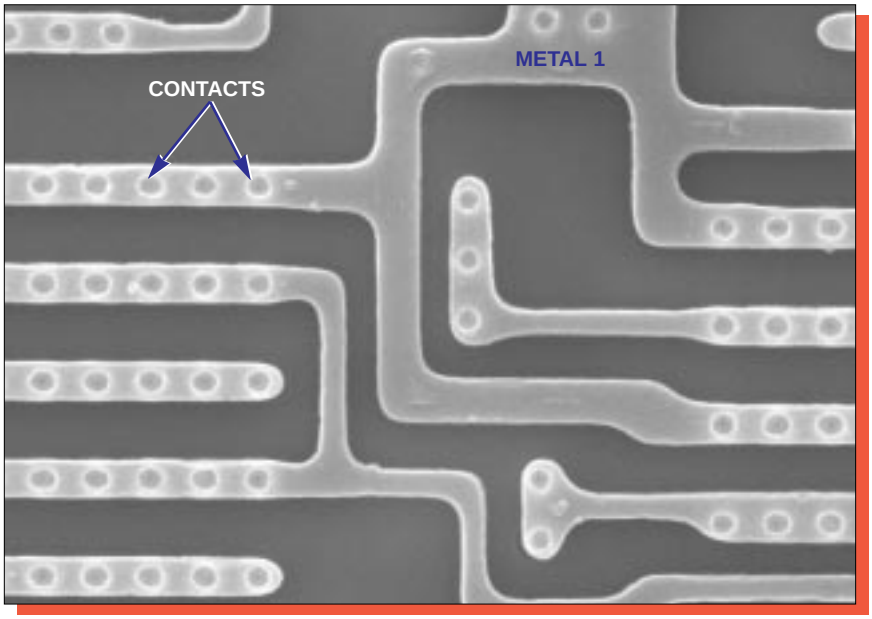


Mag. 36,600x

Figure 14. SEM section views illustrating metal 1 line profiles.

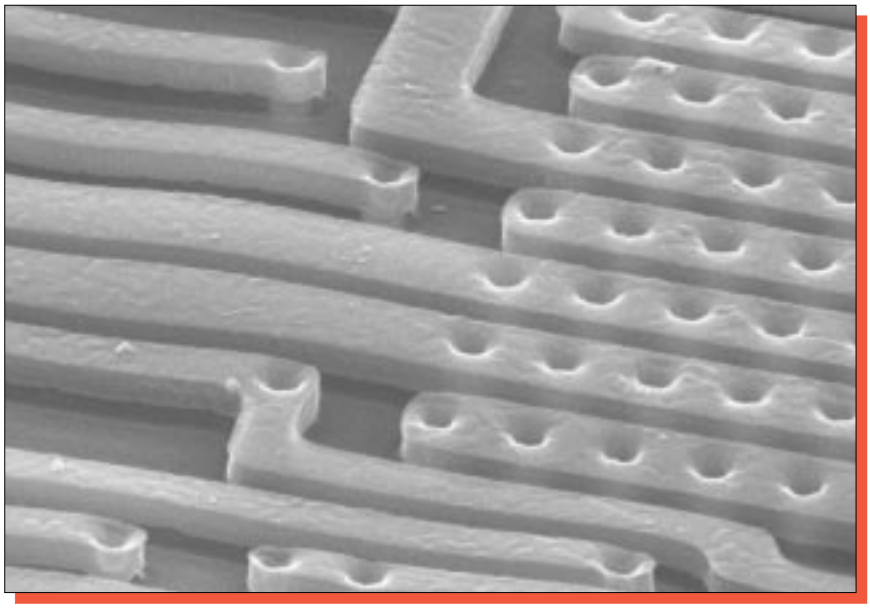


Mag. 8000x

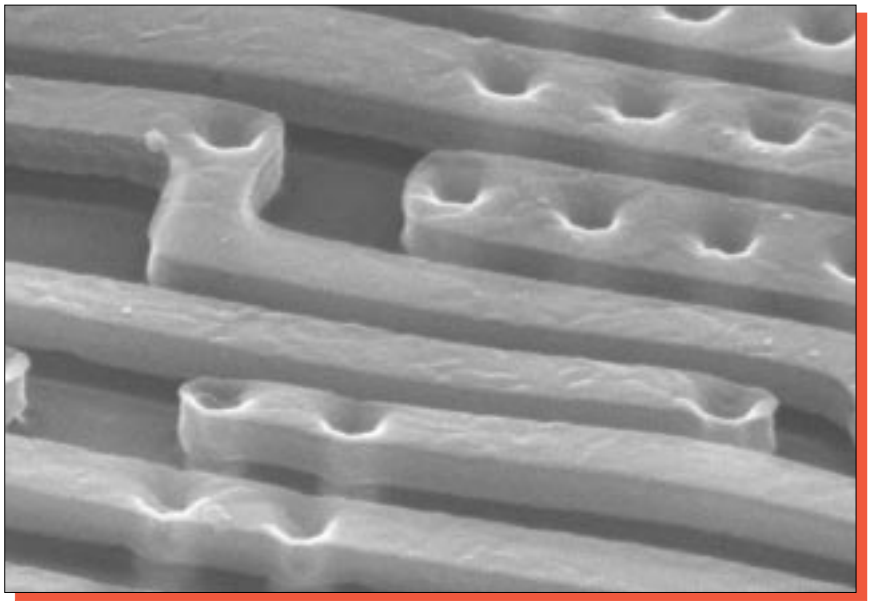


Mag. 10,000x

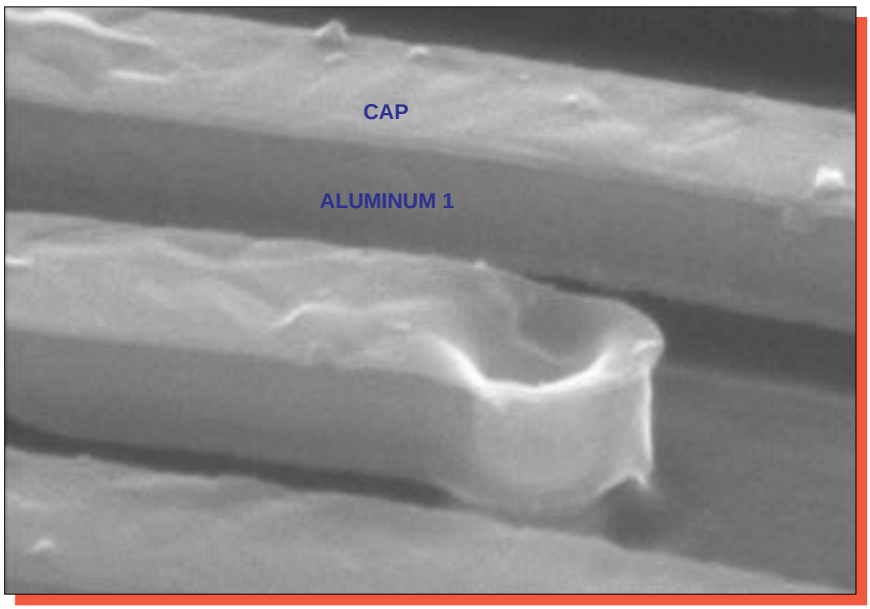
Figure 15. Topological SEM views illustrating metal 1 patterning. 0°.



Mag. 13,000x

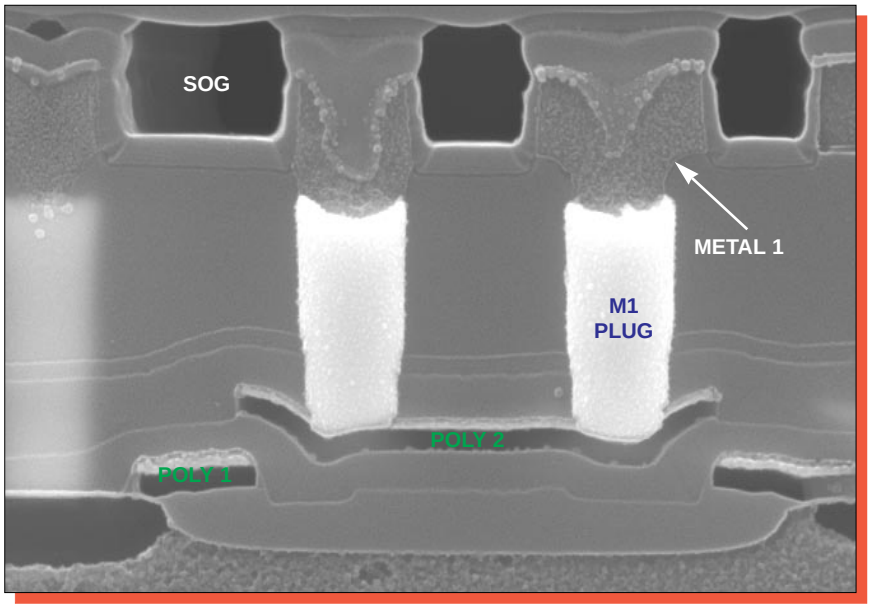


Mag. 20,000x

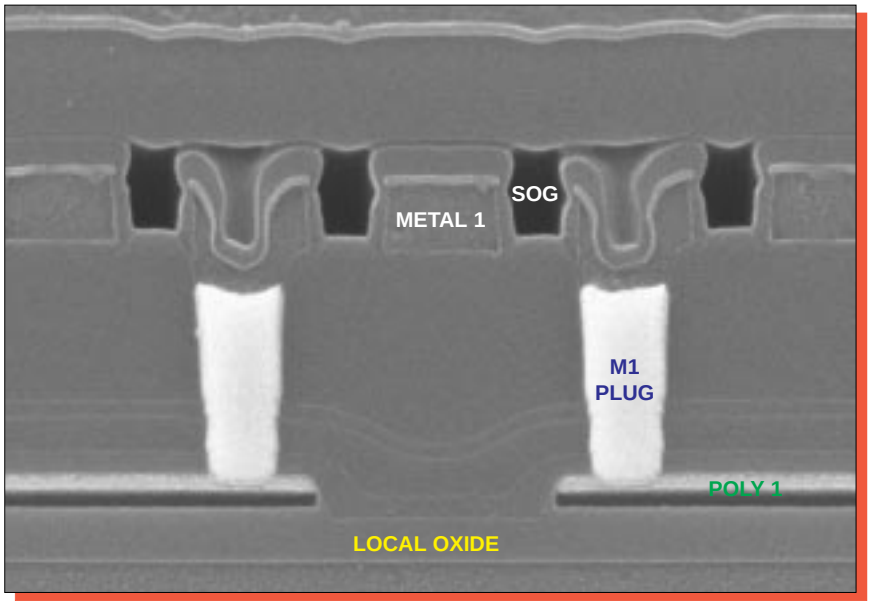


Mag. 52,000x

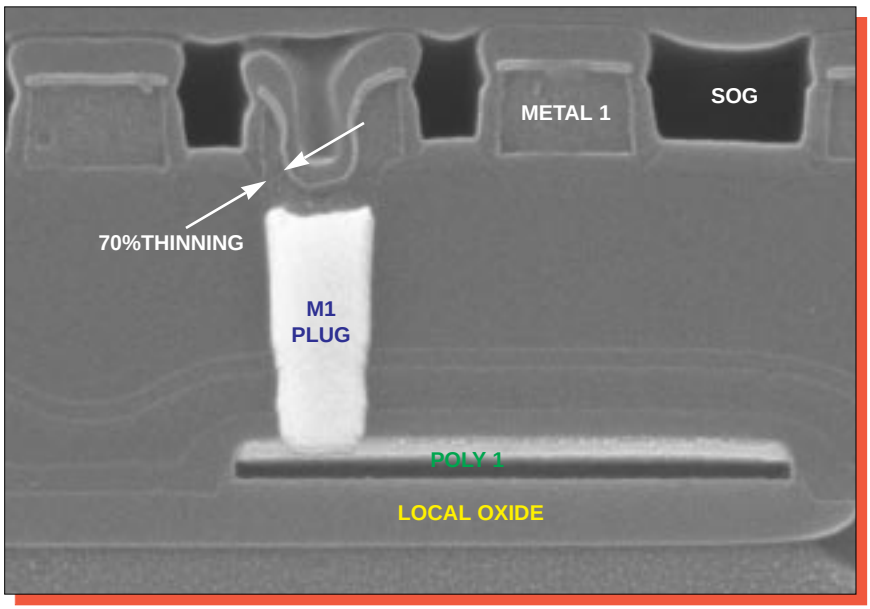
Figure 16. SEM views illustrating metal 1 integrity. 60°.



metal 1-to-poly 2,
Mag. 31,000x

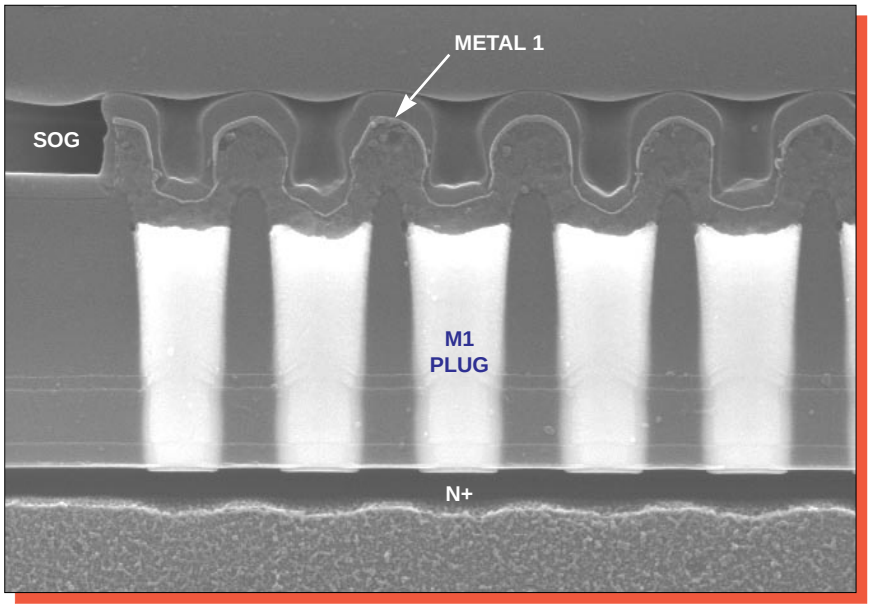


metal 1-to-poly 1,
Mag. 26,000x

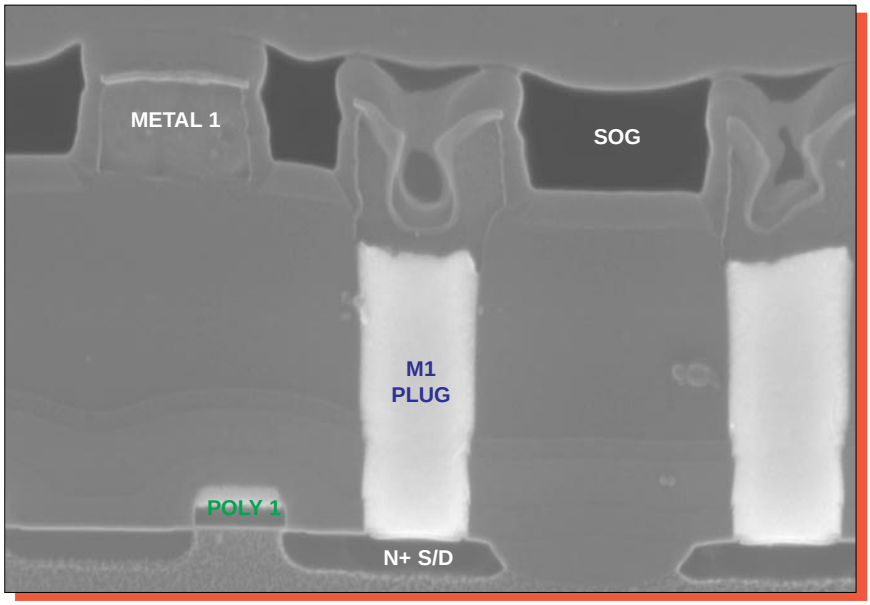


metal 1-to-poly 1,
Mag. 32,000x

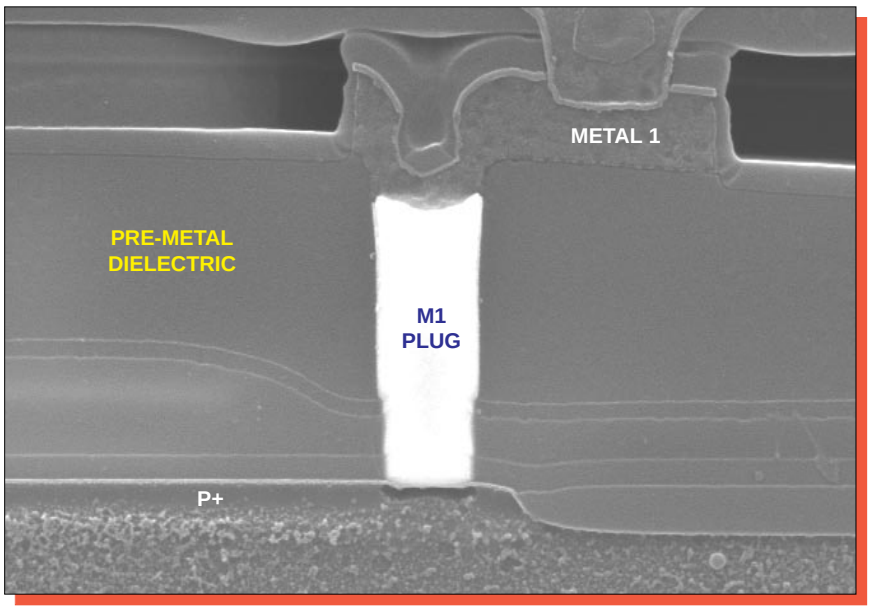
Figure 17. SEM section views of metal 1-to-poly contacts.



metal 1-to-N+,
Mag. 24,000x

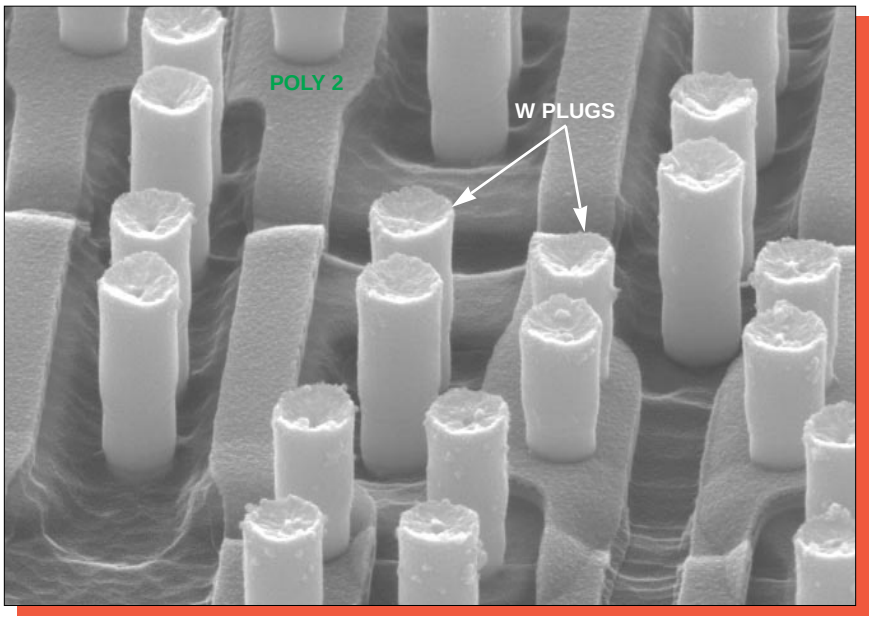


metal 1-to-N+,
Mag. 33,000x

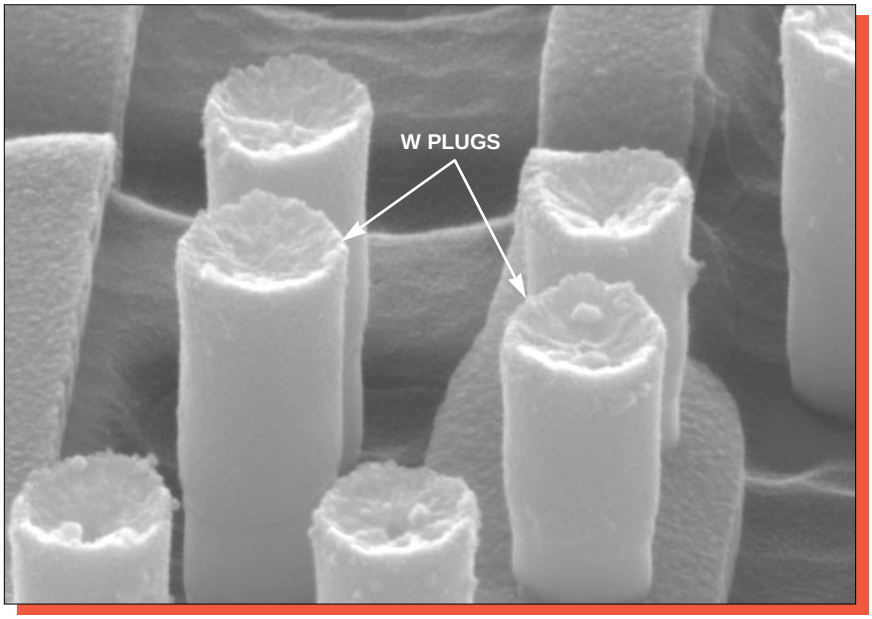


metal 1-to-P+,
Mag. 29,000x

Figure 18. SEM section views of metal 1-to-diffusion contacts.

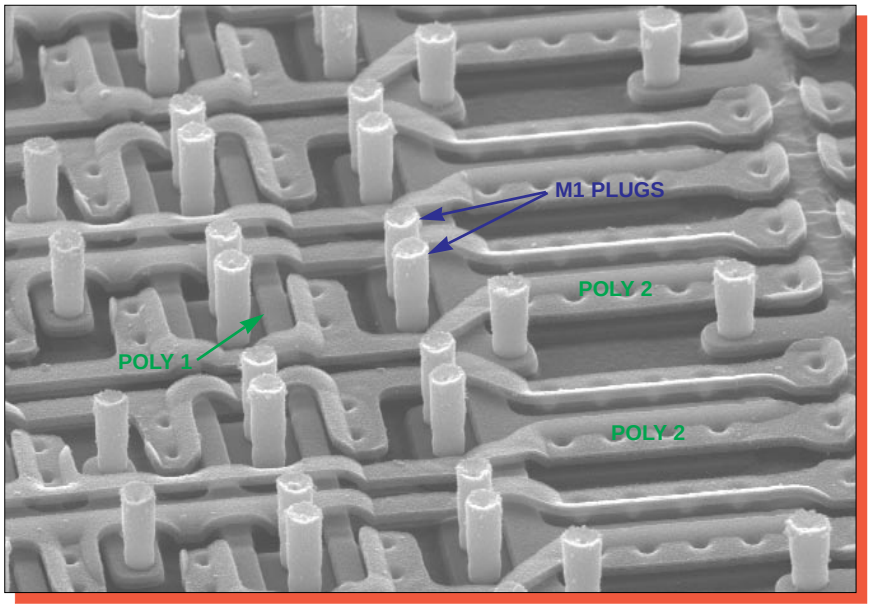


Mag. 23,000x

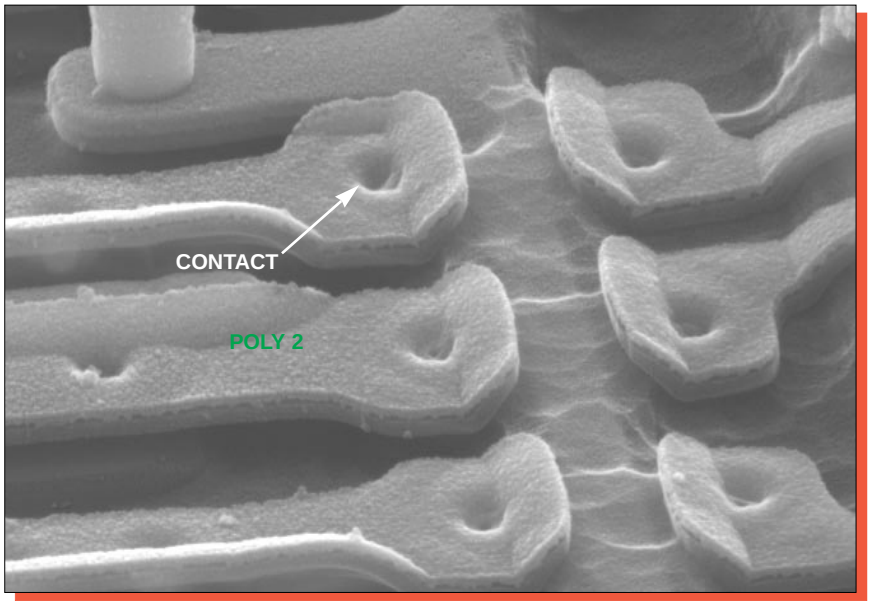


Mag. 46,000x

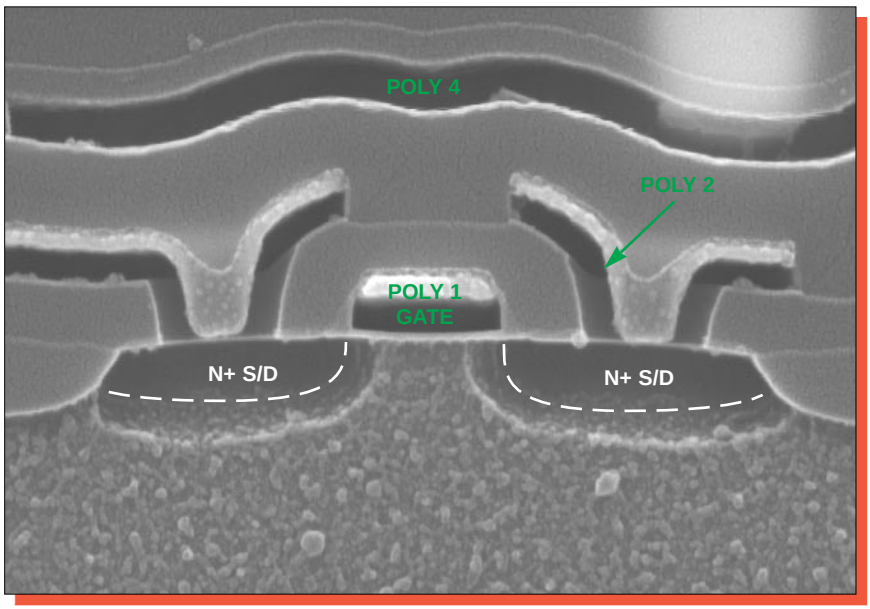
Figure 19. SEM views of metal 1 tungsten plugs. 60°.



Mag. 10,000x

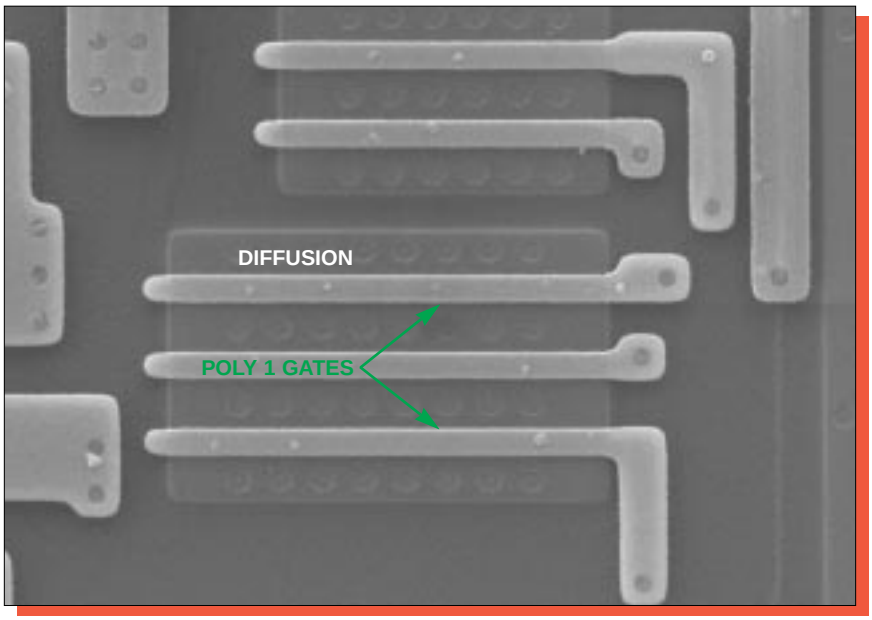


Mag. 30,000x

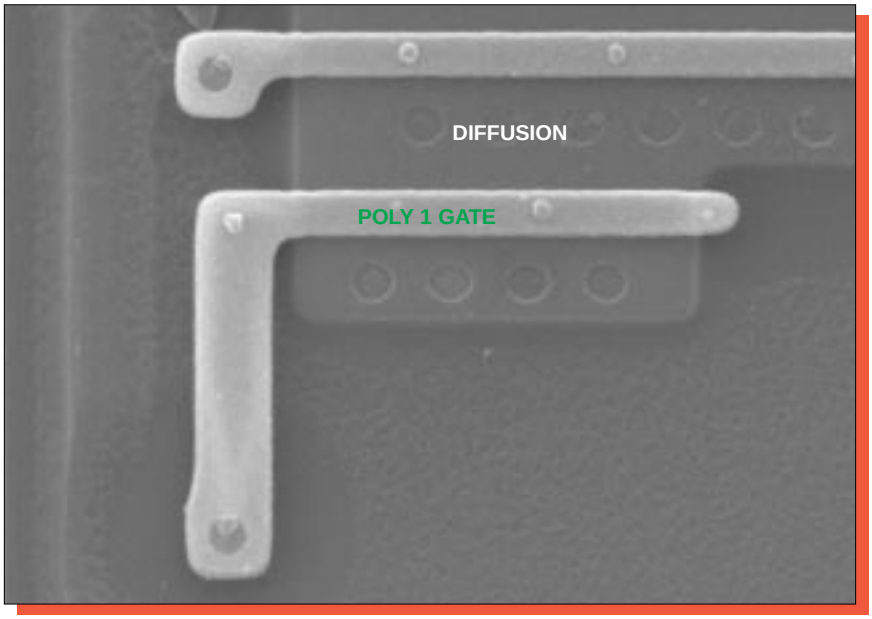


Mag. 51,000x

Figure 20. SEM views of poly 2 interconnect. 60°.

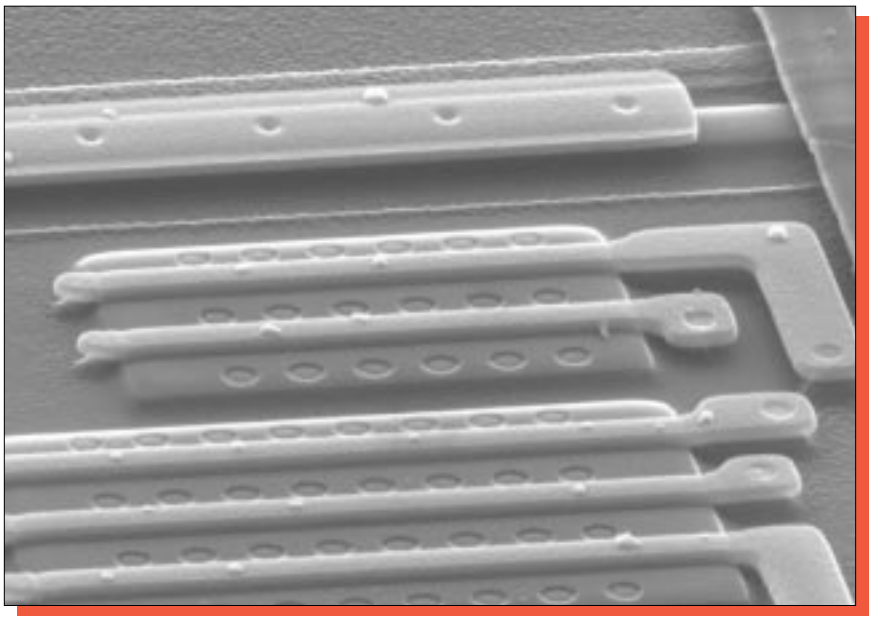


Mag. 9000x

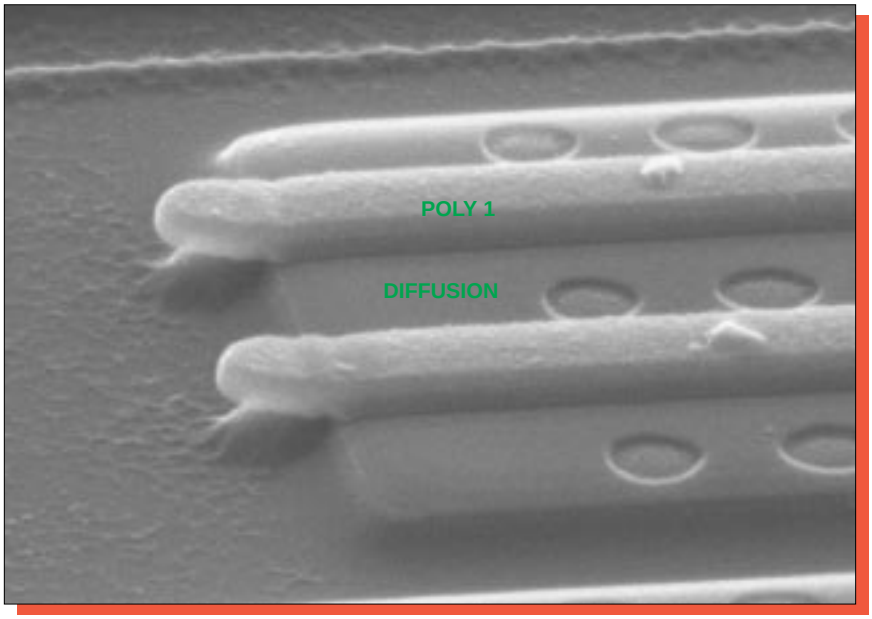


Mag. 17,000x

Figure 21. Topological SEM views of poly 1 patterning. 0°.

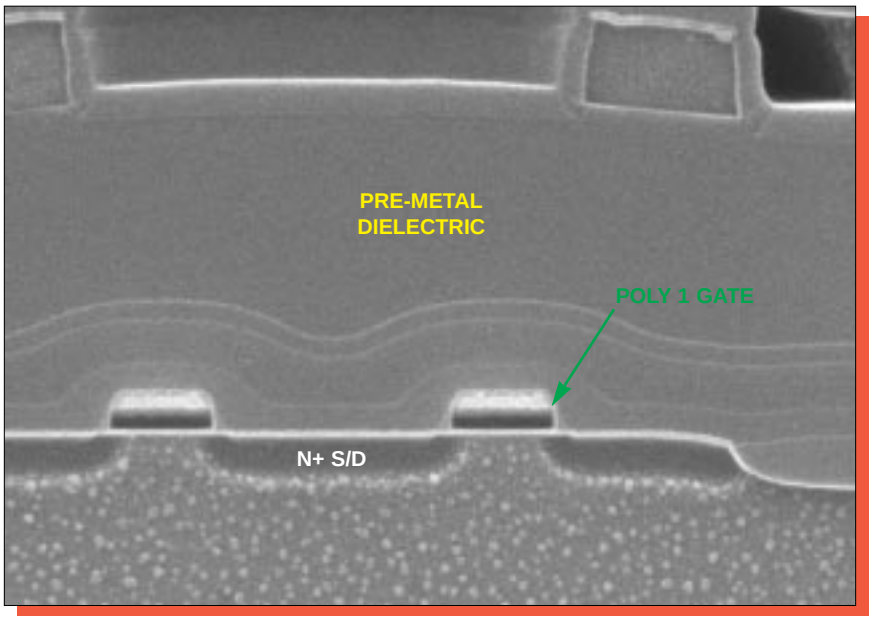


Mag. 13,500x

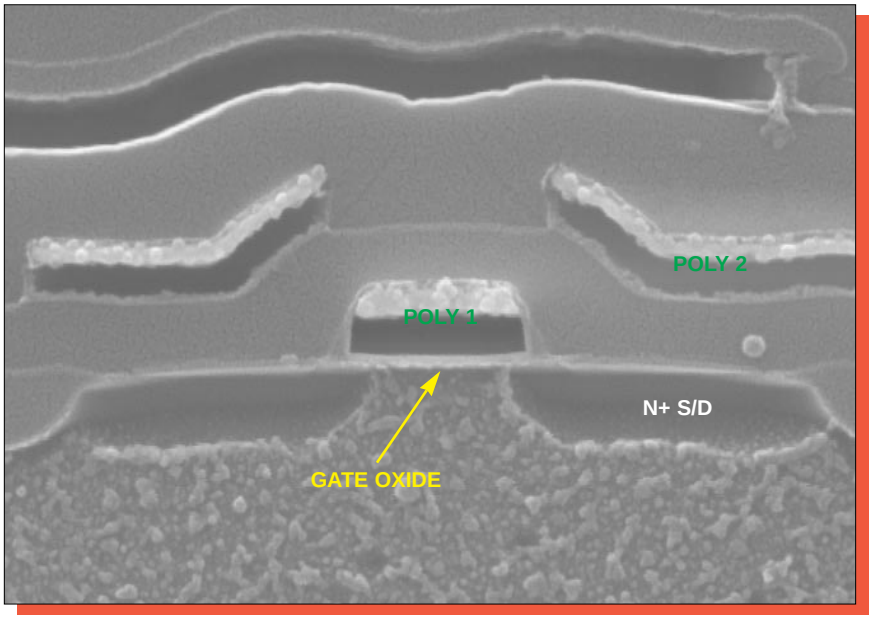


Mag. 40,000x

Figure 22. Perspective SEM views of poly 1 coverage. 60°.

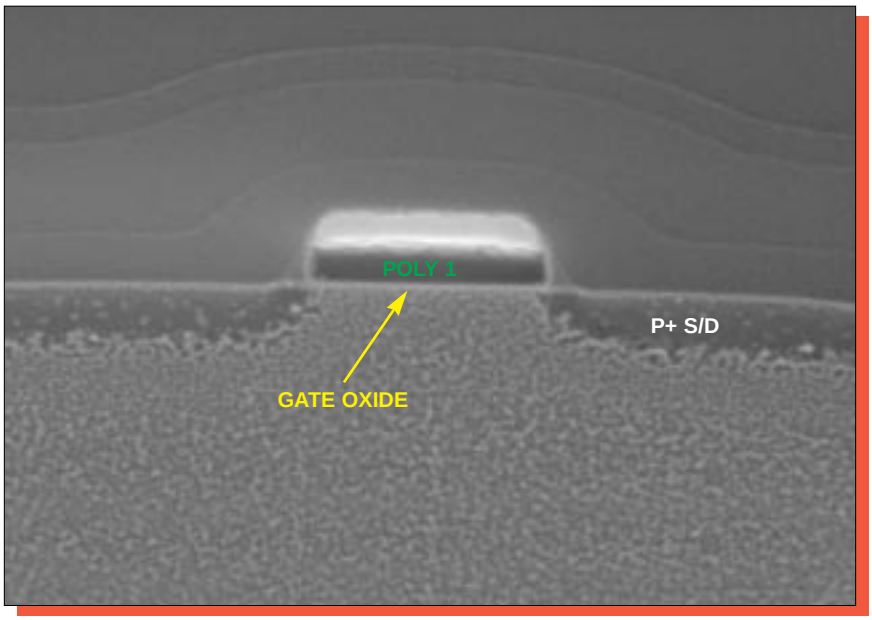


Mag. 33,600x

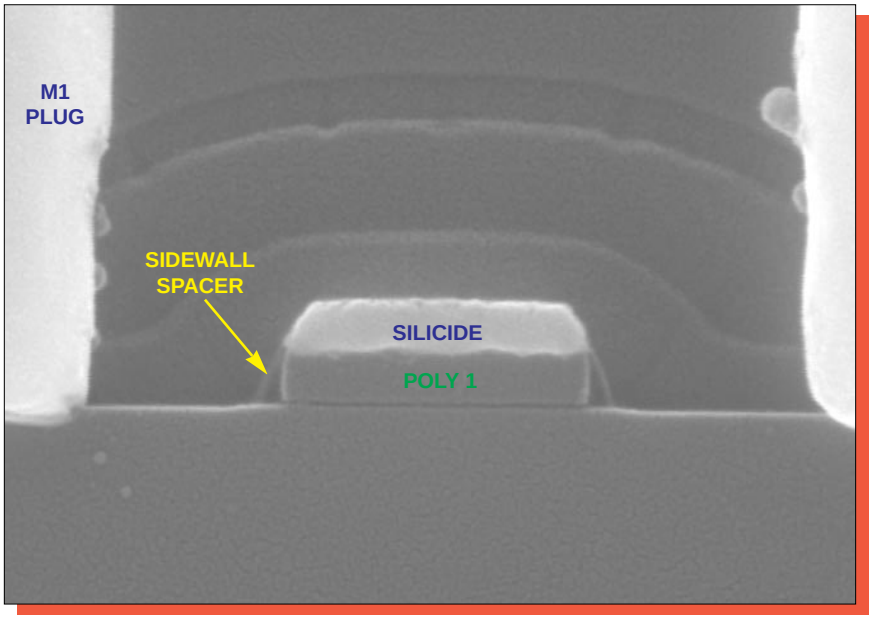


Mag. 60,000x

Figure 23. SEM section views of N-channel transistors.

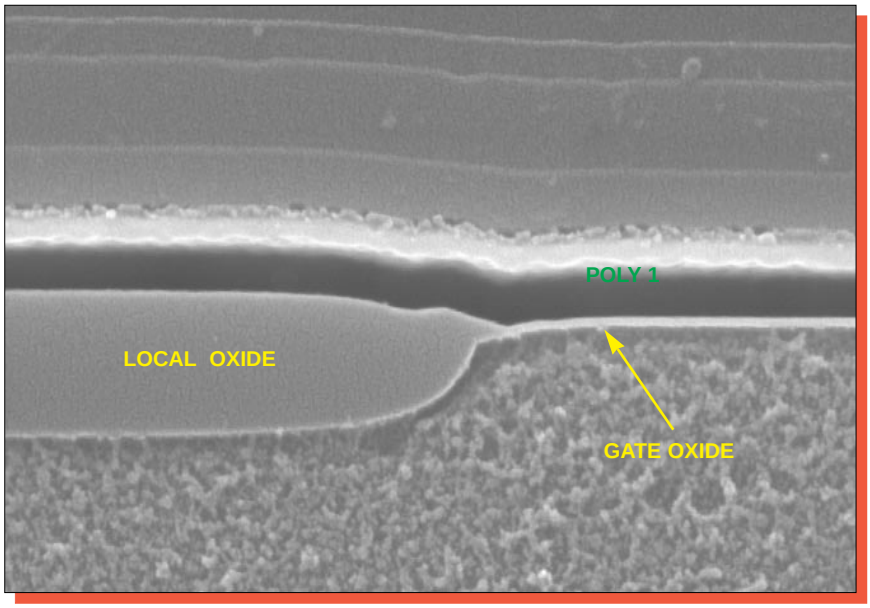


Mag. 66,000x

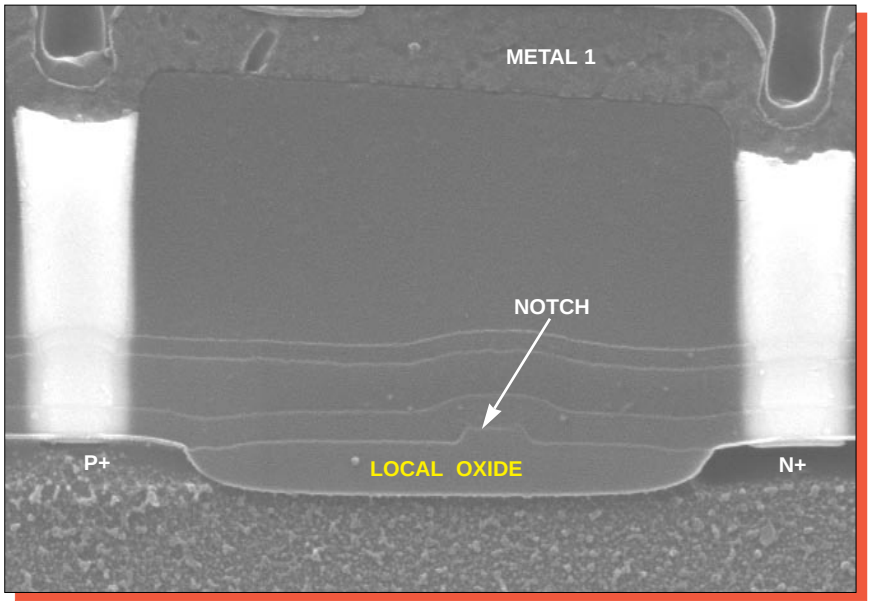


Mag. 80,100x

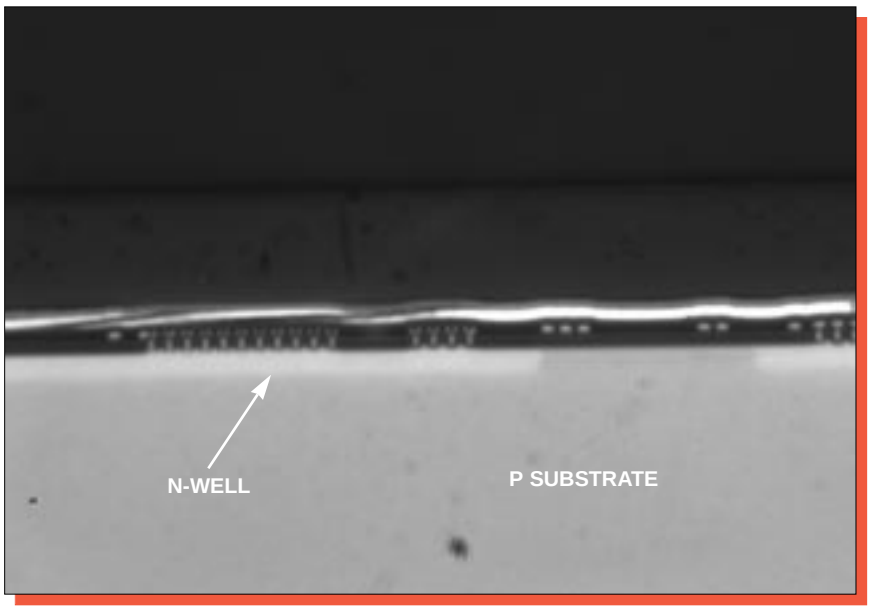
Figure 24. SEM section views illustrating typical P-channel transistors.



Mag. 63,500x

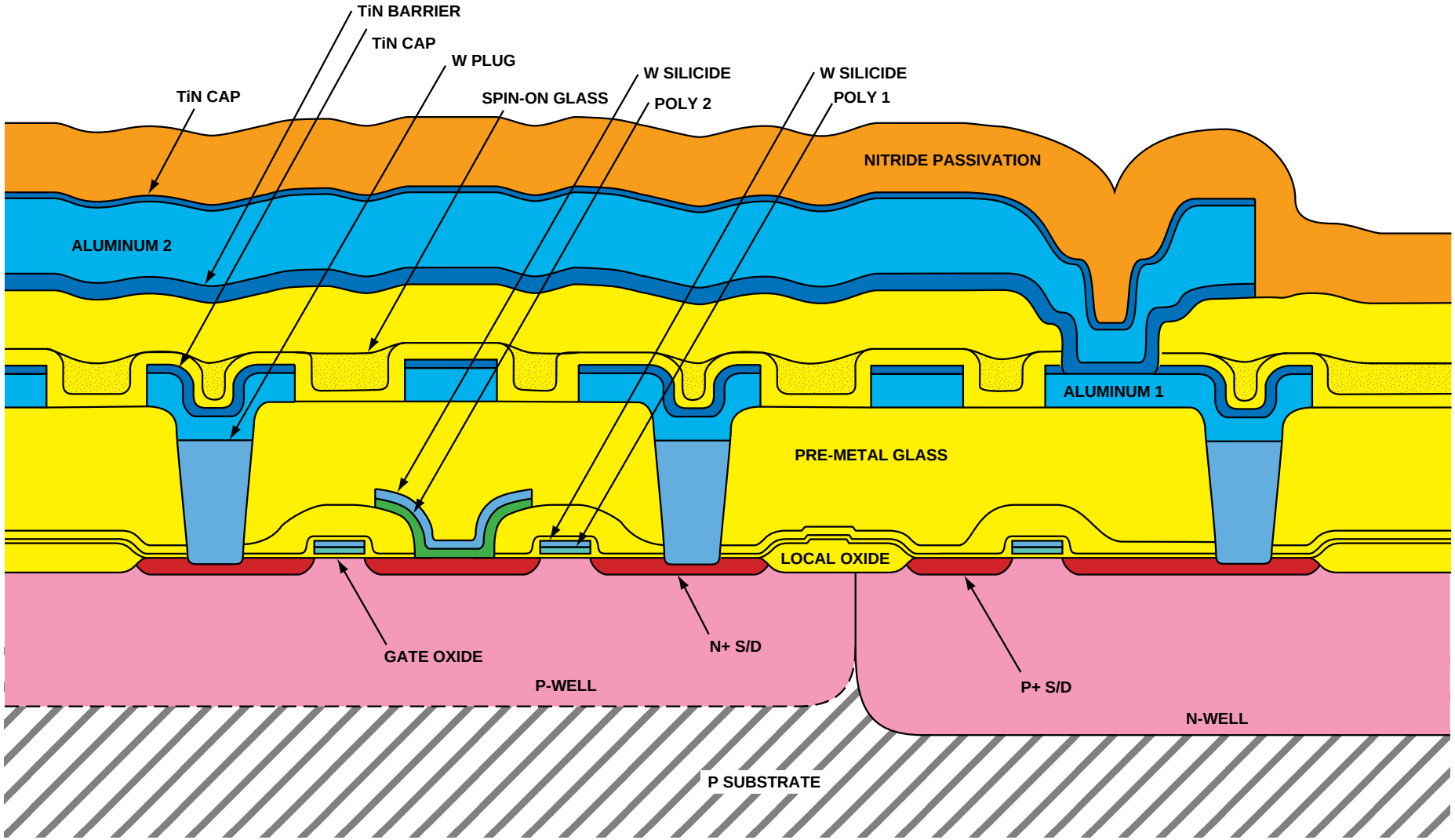


Mag. 33,000x



Mag. 1550x

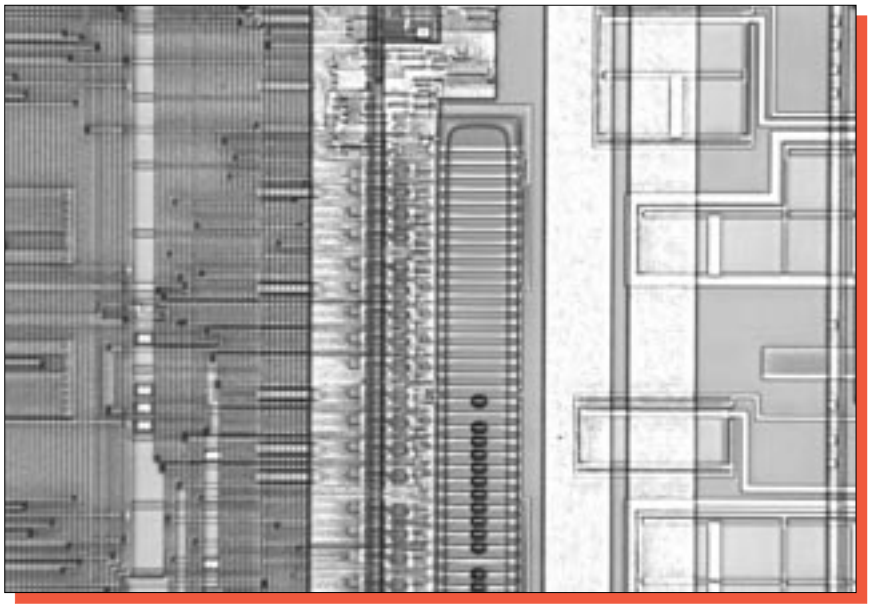
Figure 25. Section views of a local oxide birdsbeak and well structure.



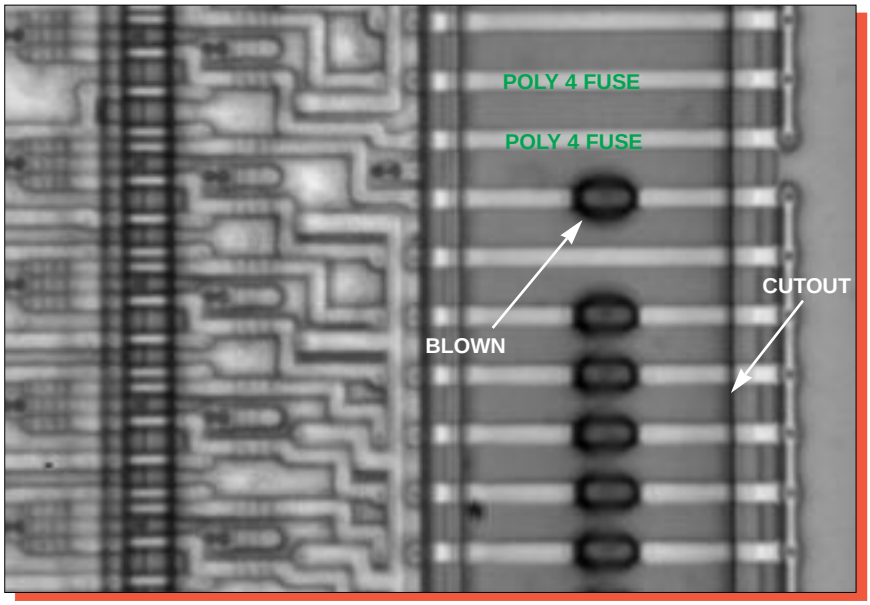
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

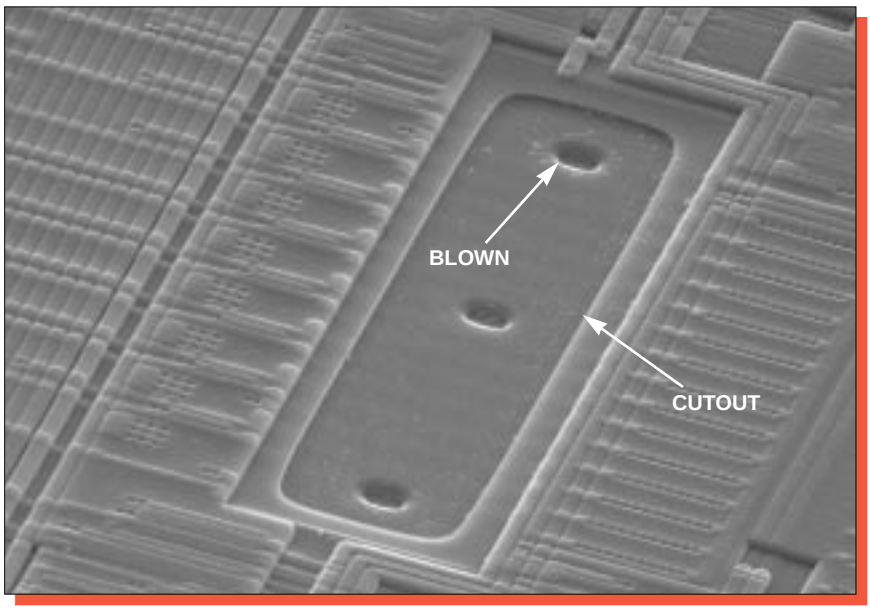
Figure 26. Color cross section drawing illustrating device structure.



Mag. 350x

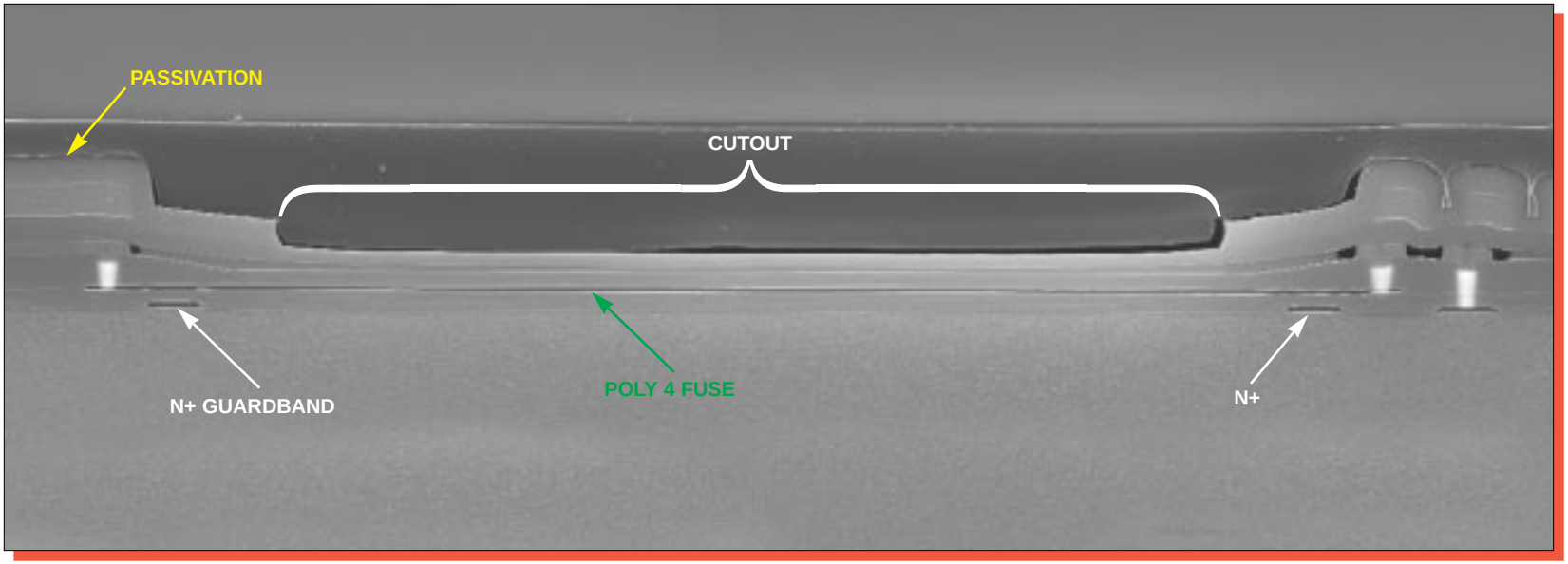


Mag. 1550x

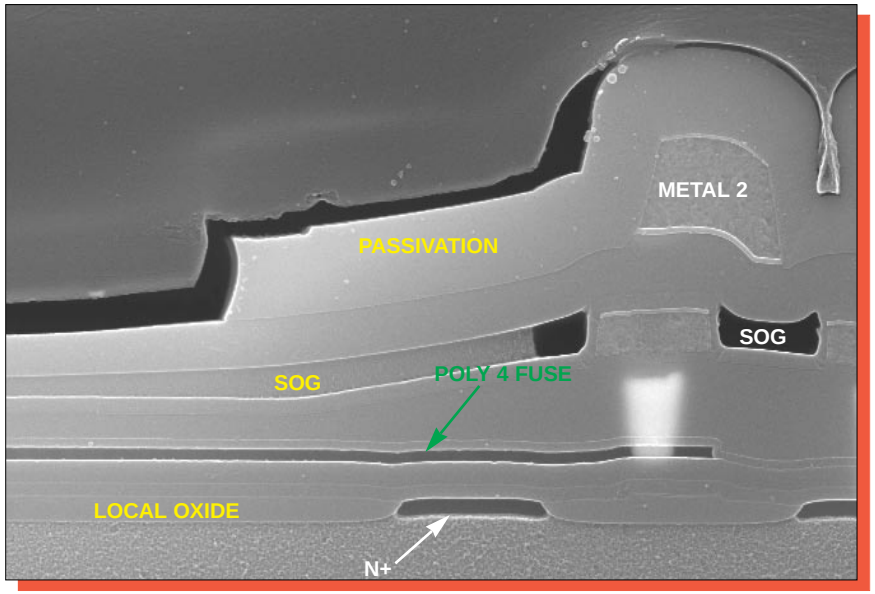


Mag. 1300x, 60°

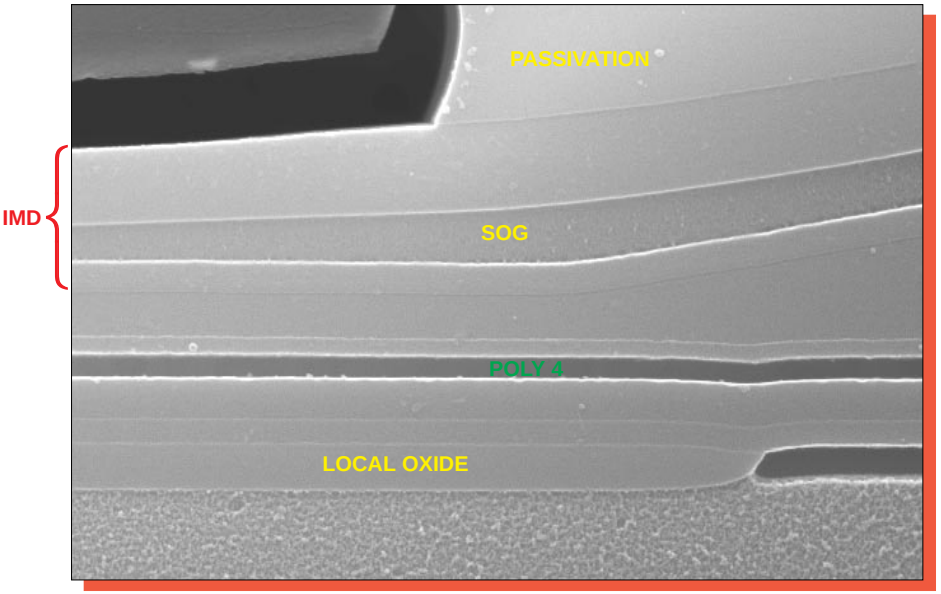
Figure 27. Optical and SEM views of poly 4 fuses.



Mag. 5500x

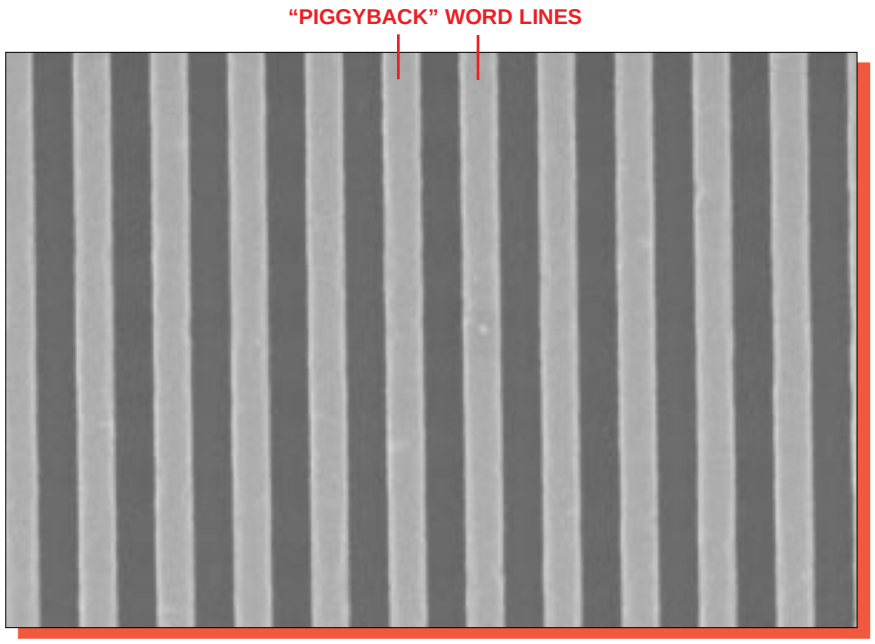


Mag. 14,000x

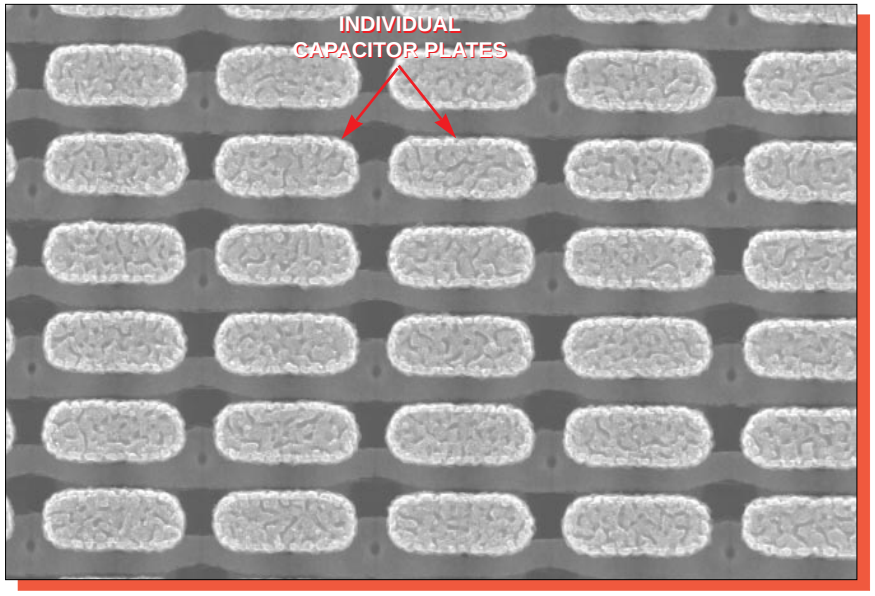


Mag. 25,750x

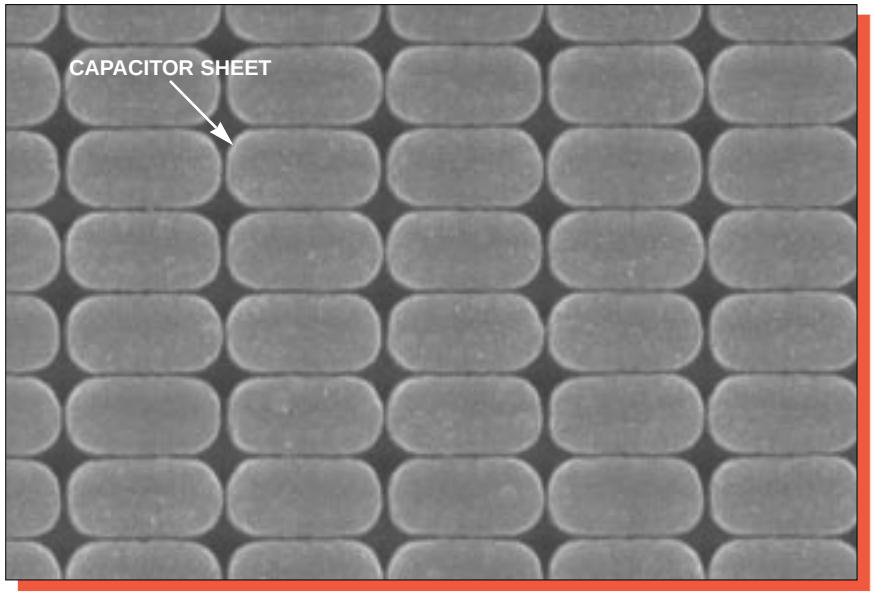
Figure 28. SEM section views of a poly 4 fuse.



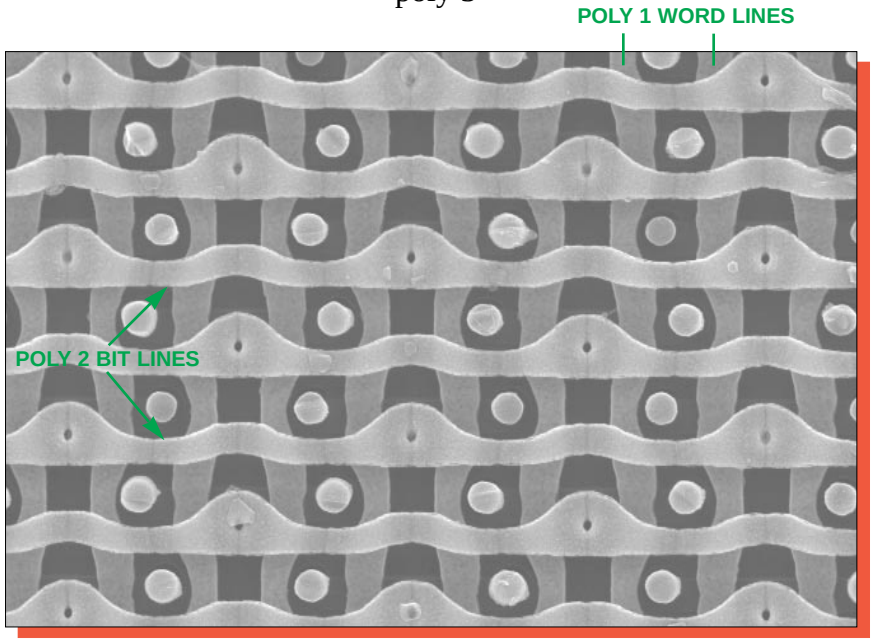
metal 1



poly 3

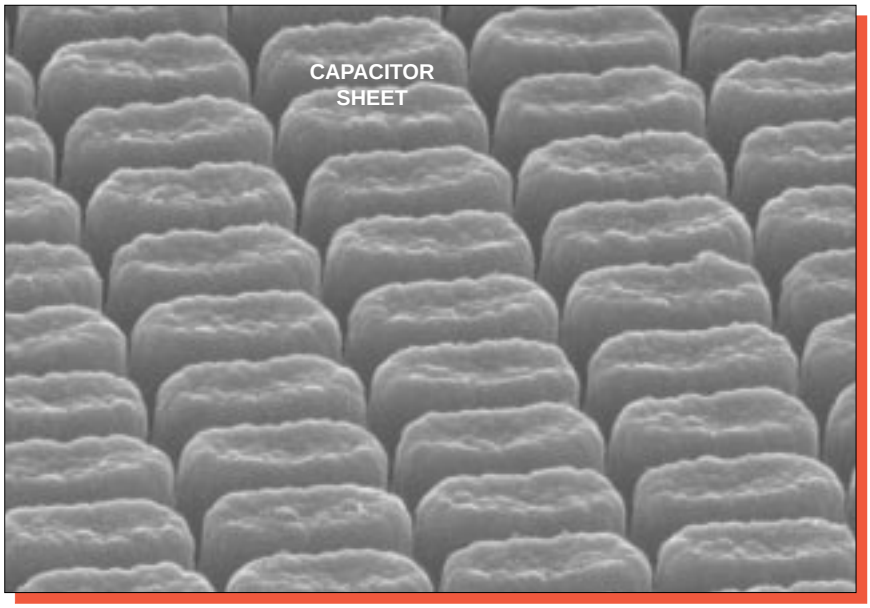


poly 4

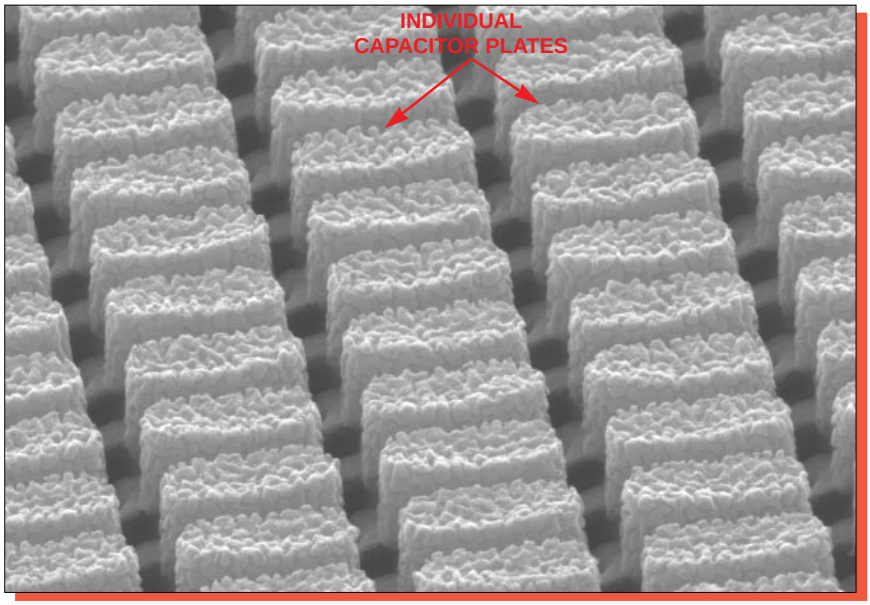


poly 1 and 2

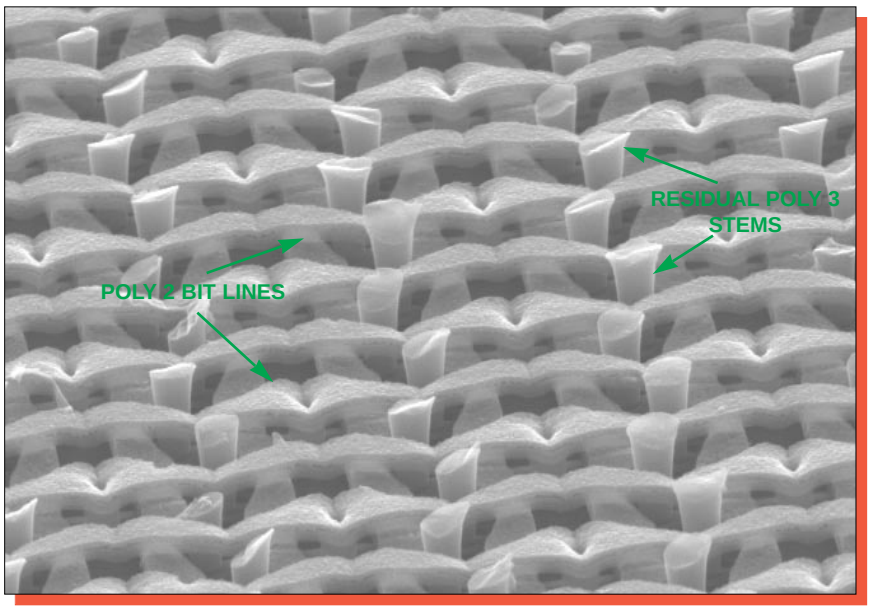
Figure 29. Topological SEM views of the cell array. Mag. 15,000x, 0°.



poly 4

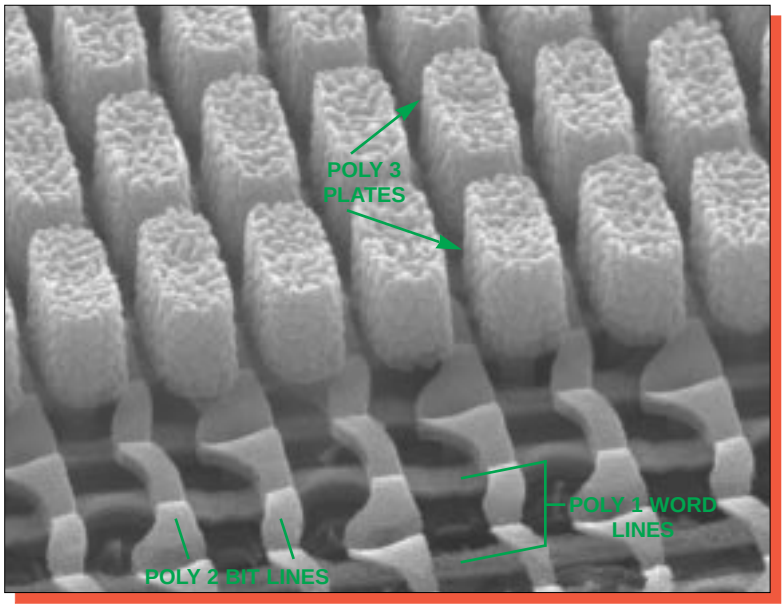


poly 3

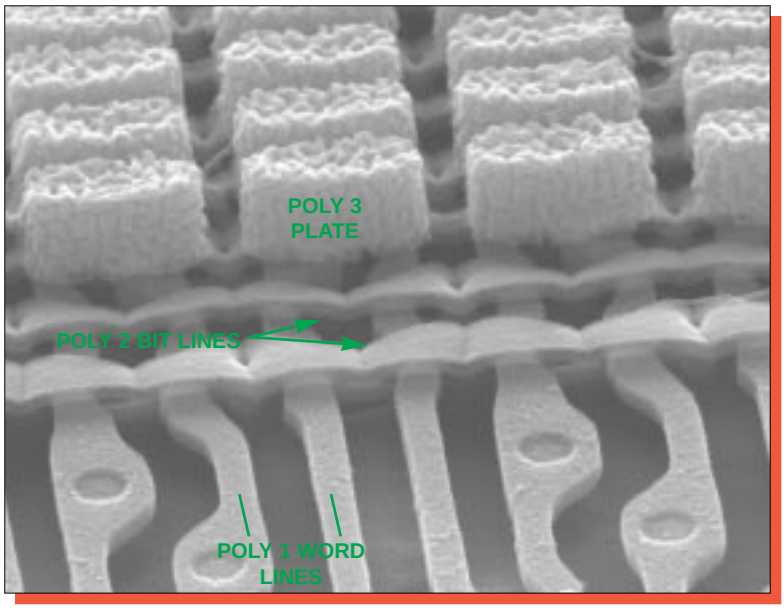


poly 1 and 2

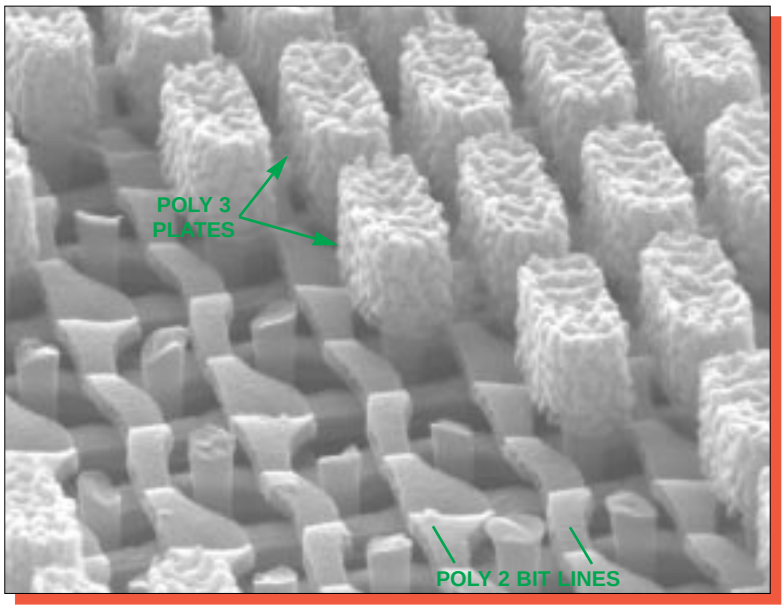
Figure 30. Perspective SEM views of the cell array. Mag. 20,000x, 60°.



Mag. 19,100x

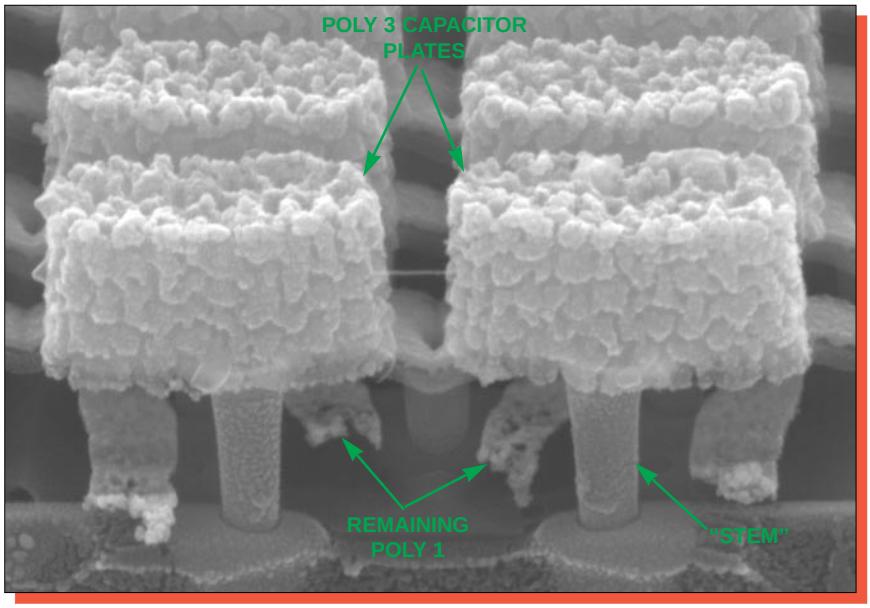


Mag. 18,700x

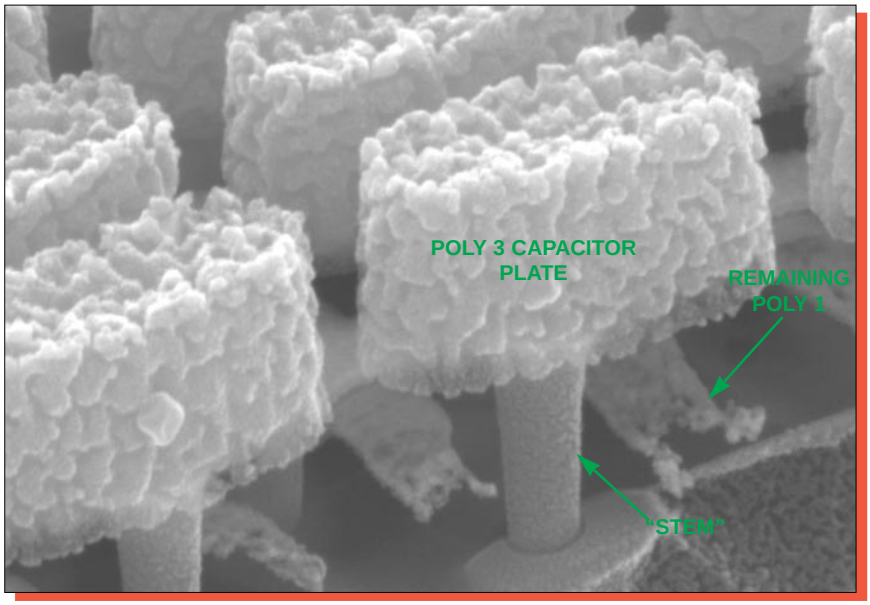


Mag. 21,250x

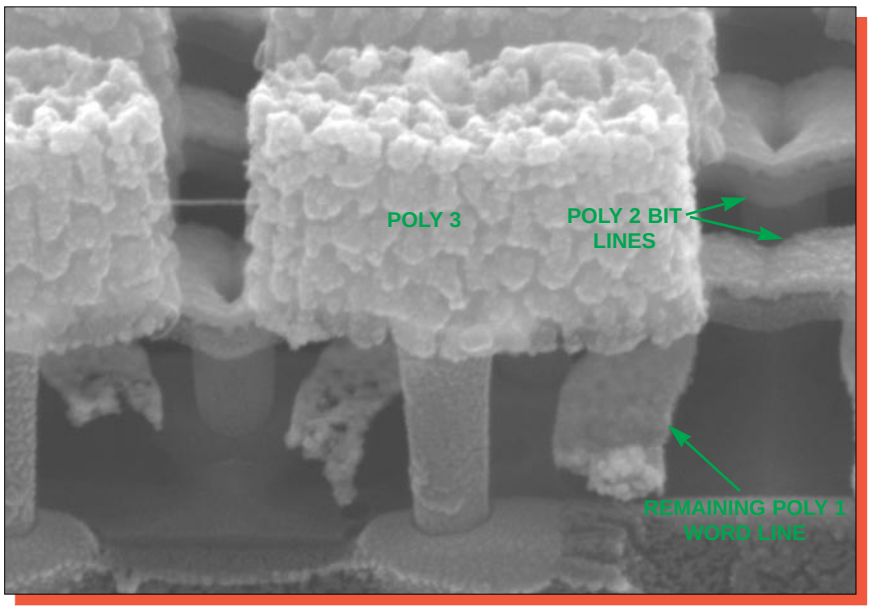
Figure 31. Illustrative SEM views of the cell array. 60°.



Mag. 35,000x

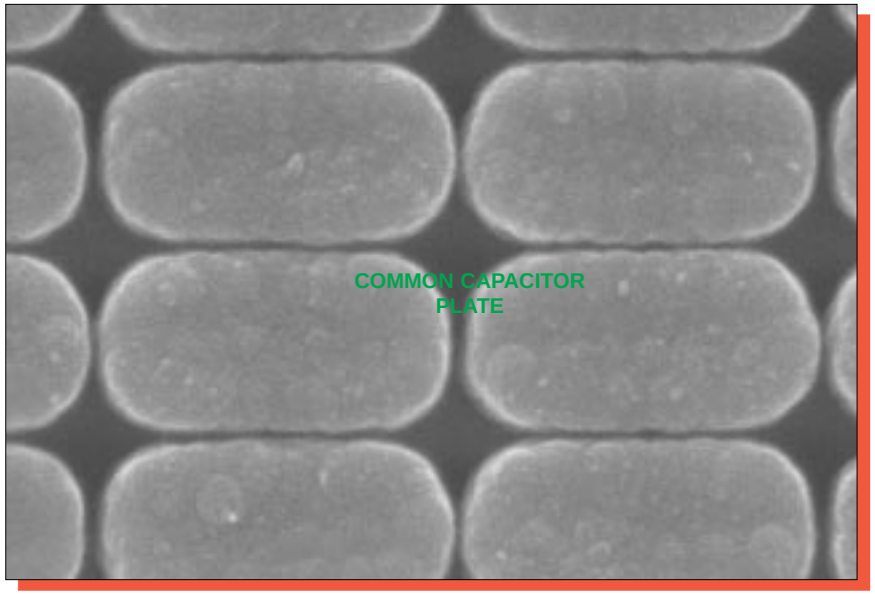


Mag. 44,000x

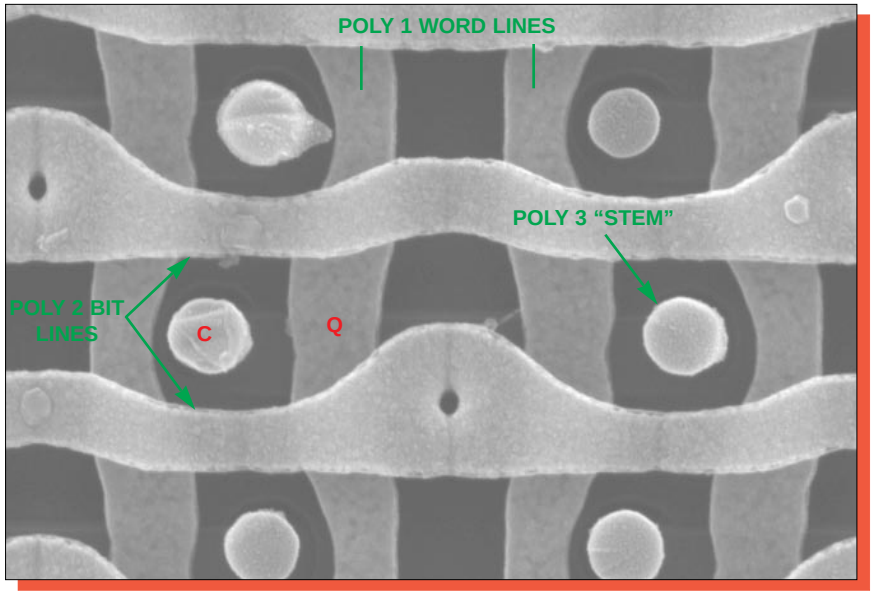


Mag. 45,000x

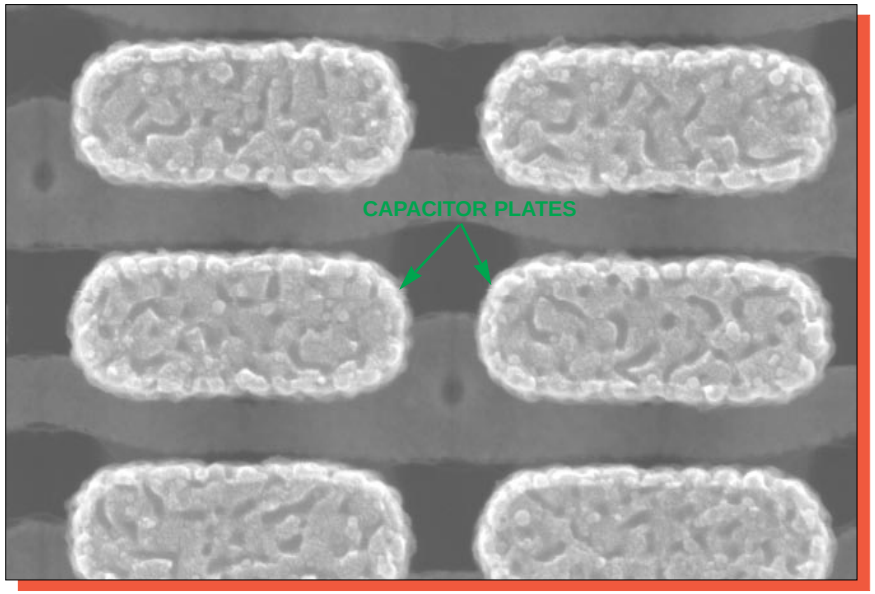
Figure 32. Detailed views of the capacitors. 60°.



poly 4



poly 1 and 2



poly 3

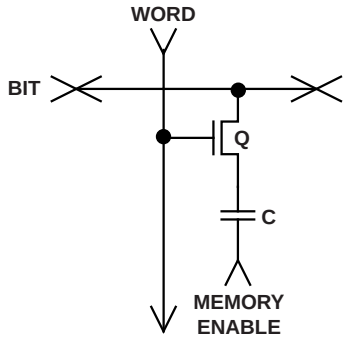
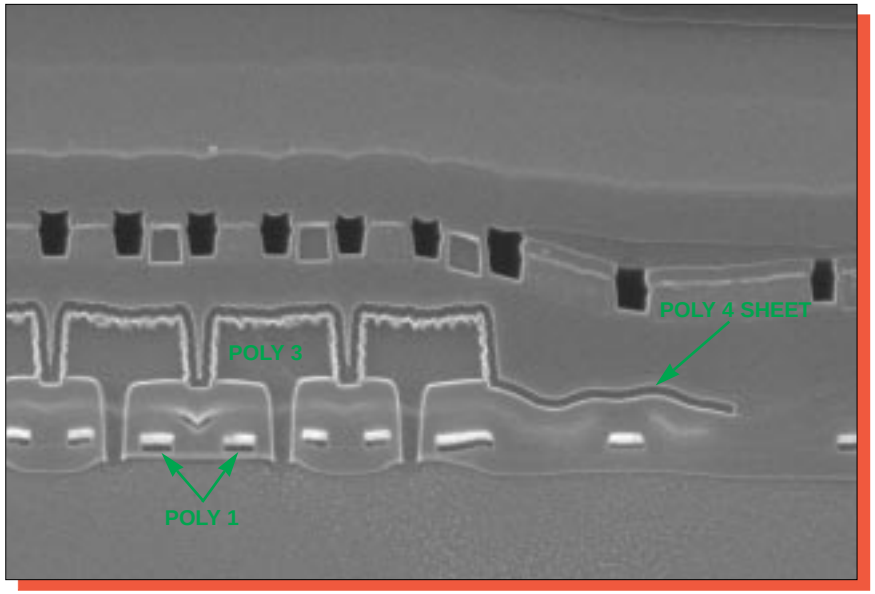
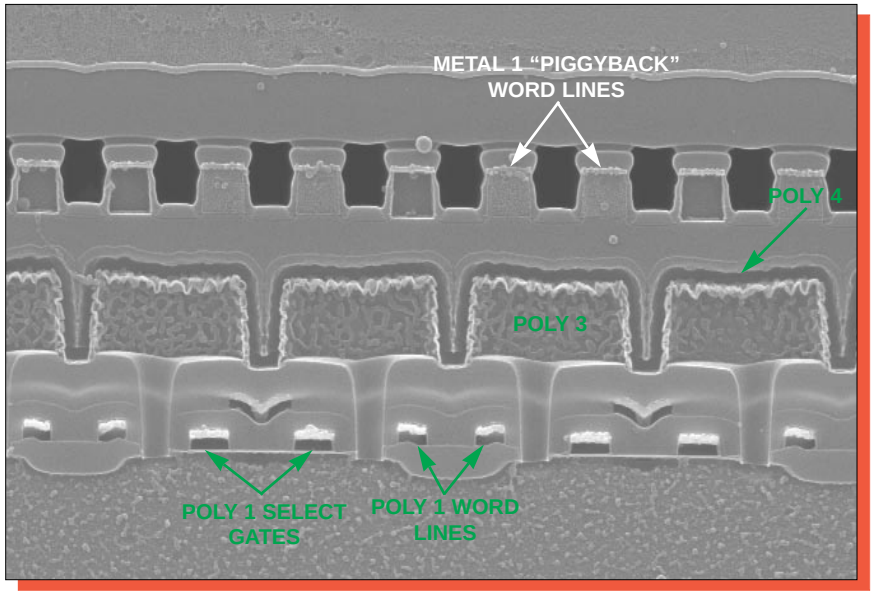


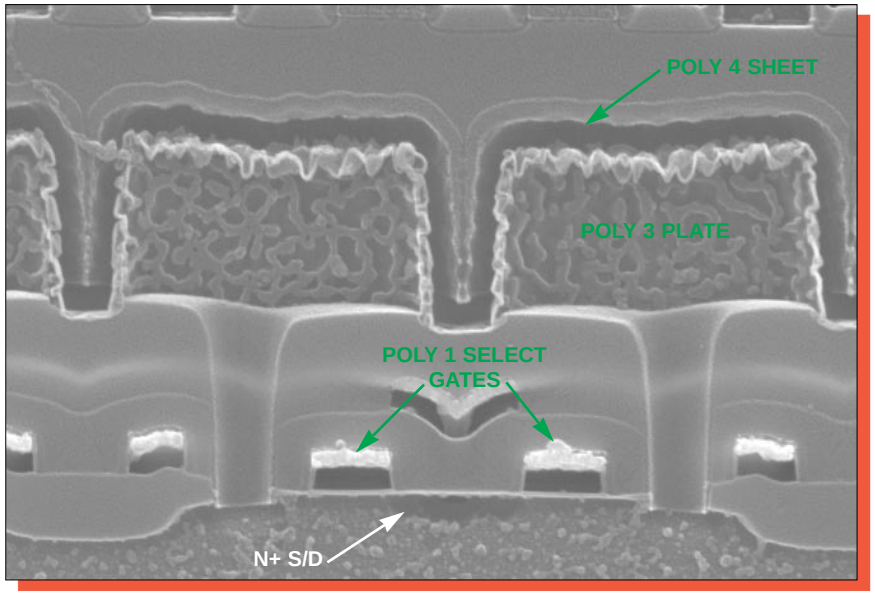
Figure 33. Topological SEM views and schematic of the DRAM cells. Mag. 35,000x, 0°.



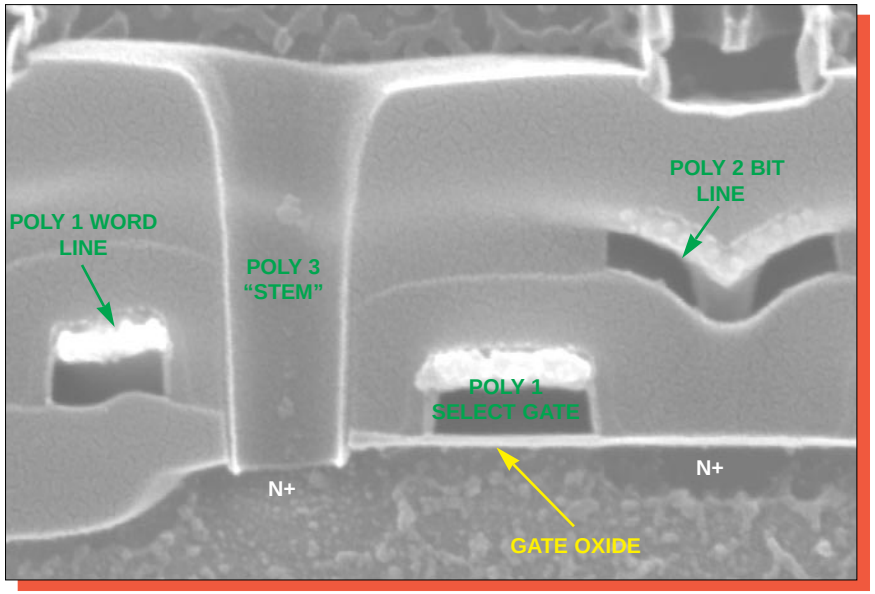
Mag. 13,000x



Mag. 16,000x

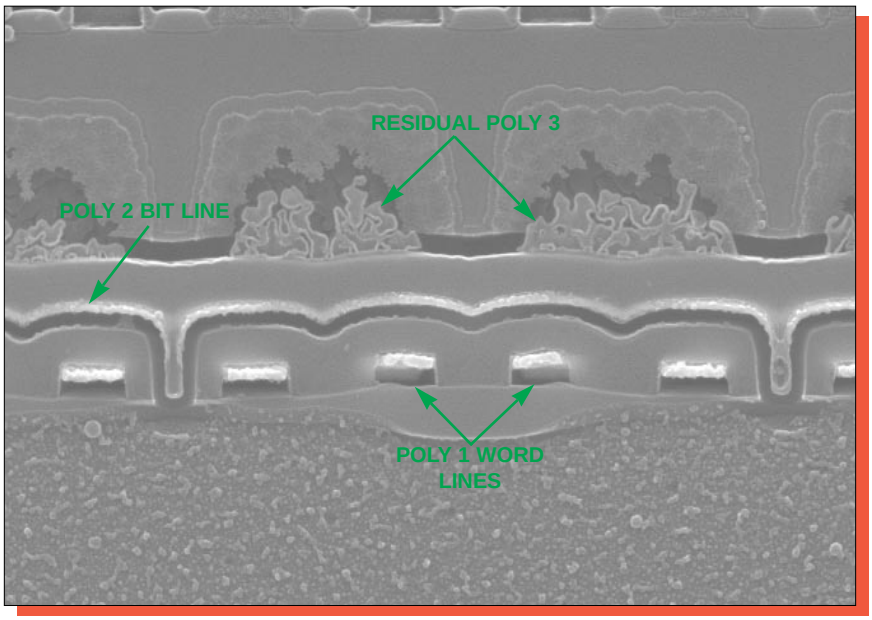


Mag. 32,750x

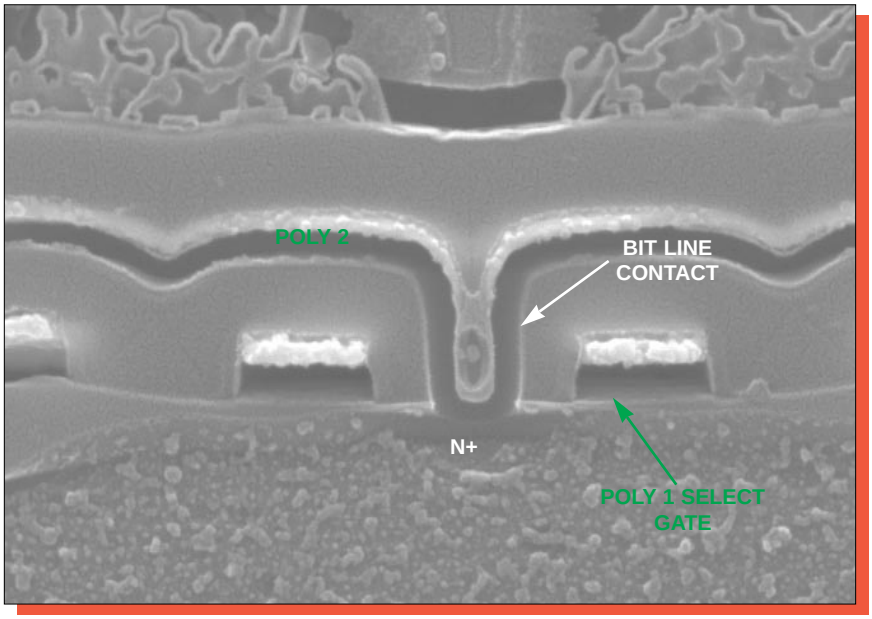


Mag. 66,000x

Figure 34. SEM section views of the DRAM cell array (parallel to bit lines).

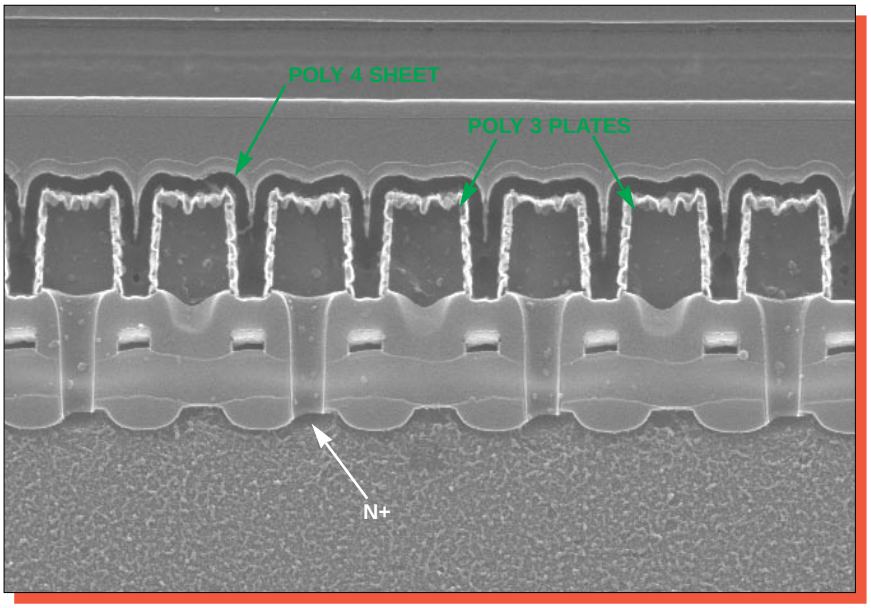


Mag. 26,000x

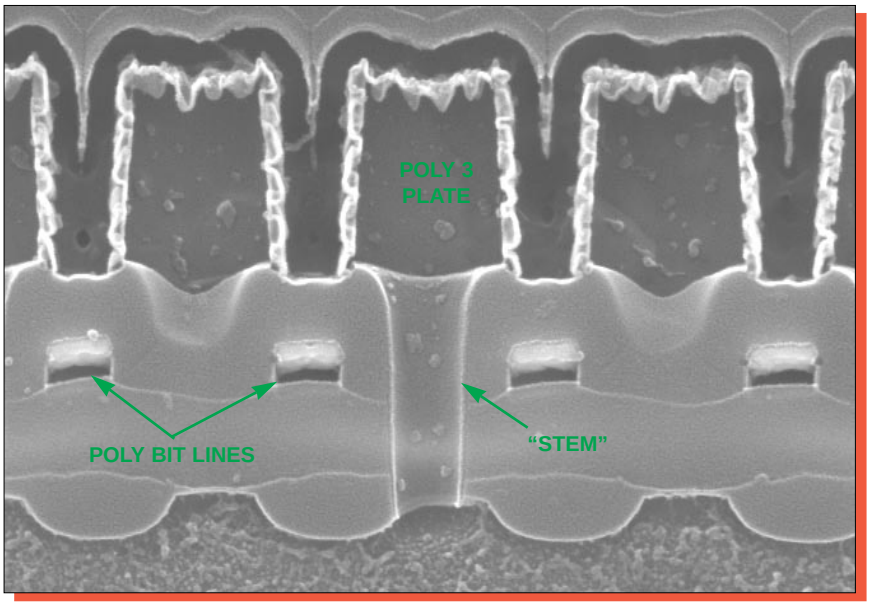


Mag. 52,000x

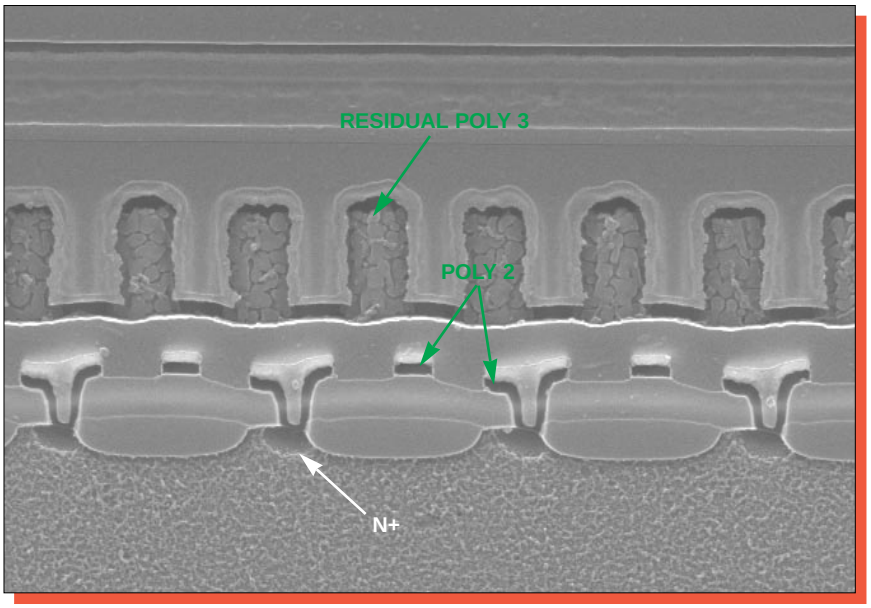
Figure 35. SEM section views of the poly 2 bit line (parallel to bit lines).



Mag. 20,000x

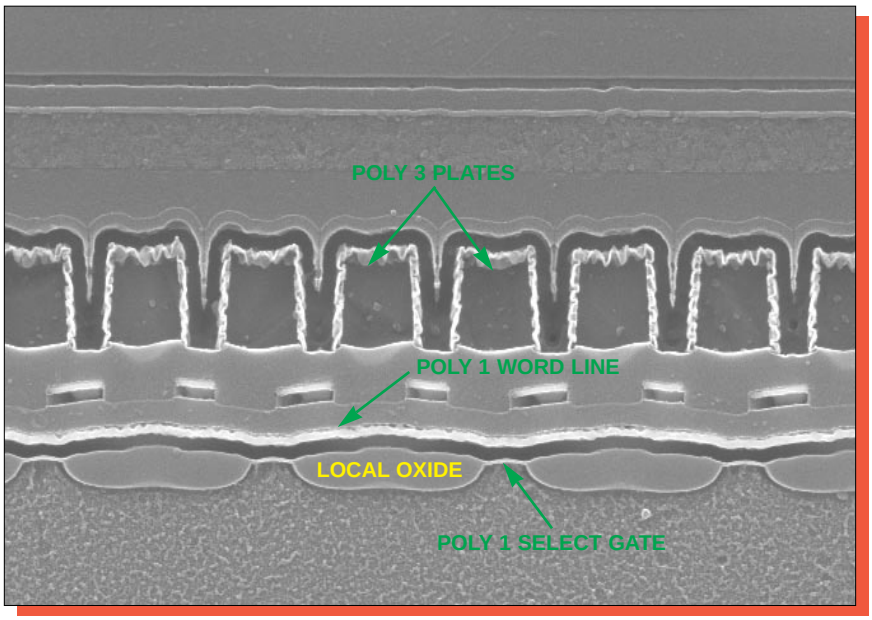


Mag. 40,000x

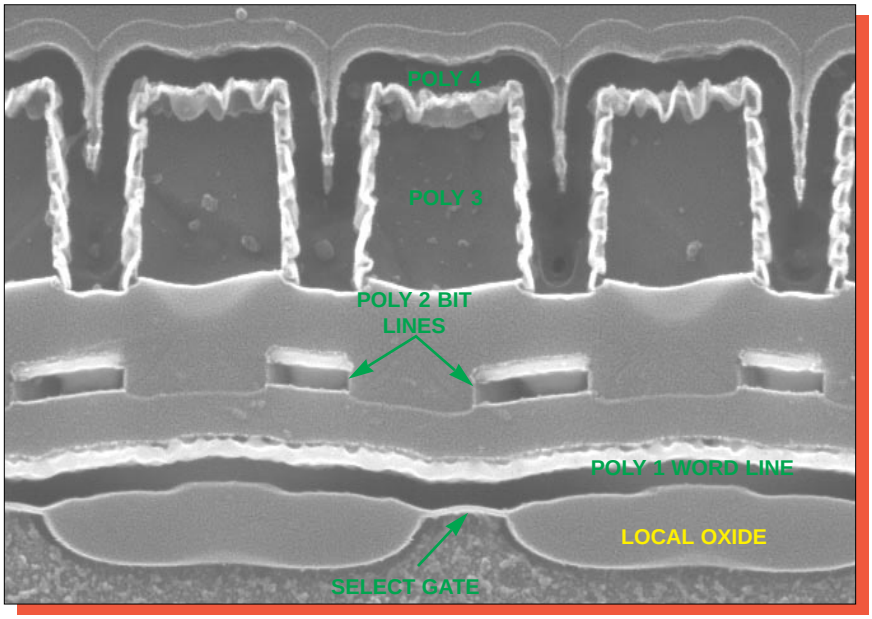


Mag. 20,000x

Figure 36. SEM section views of DRAM cells and bit line contacts (parallel to word lines).



Mag. 20,000x



Mag. 40,000x

Figure 37. SEM section views of the poly 1 word line (parallel to word line).