Construction Analysis

Hitachi 5165805A
64Mbit (8Mb x 8) Dynamic RAM

Report Number: SCA 9712-565

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Hitachi 5165805A 64-megabit (8 mb x 8) Dynamic RAM. The devices were packaged in 32-pin plastic Thin Small Outline Packages (TSOP). Date codes were 9705

MAJOR FINDINGS

Questionable Items:[1]

- Aluminum 2 and 3 thinning up to 100 percent[2] at via edges (Figures 13 and 17). Barrier metal maintained continuity.

Special Features:

- Sub-micron gates (N-ch 0.35 micron, P-ch 0.5 micron).
- Three layers of metal (no plugs). Tungsten used as metal 1 interconnect.
- Five layers of polysilicon.
- "Crown" DRAM capacitor structure. Cell size 1.2 microns^2.
- Unique fuse structure.

Noteworthy Items:

- The capacitor structure in the cell was changed from the previously analyzed 64M-bit DRAM. The individual capacitor plates had a "fin" design previously, instead of the "crown" plate presently being employed.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- 32-pin Thin Small Outline Package (TSOP) with gull wing leads.
- Lead On Chip Center Bonded (LOCCB) leadframe design.
- Lead-locking design (anchors at power rails and corner pins) for added package strength.
- Power rails ran the entire length of the package on both sides (pins 1 and 16 Vcc and pins 17 and 32 Vss).
- Multiple bonding wires connected the power rails. Pin 6 was not connected.
- Dicing was by the sawn method.
- Wirebonding method was by thermosonic ball using 0.9 mil gold wire.
- The surface of the die was attached to the underside of the leadframe with an adhesive (probably Kapton tape).
- A patterned polyimide die coat was present over the die surface.

Die Process and Design:

- Fabrication process: Selective oxidation multiple well CMOS process in a P substrate (no epi). An apparent deep N-well was used under the array with a P-well employed within.
- Final passivation: Passivation consisted of a thick layer of nitride over two layers of silicon-dioxide.

TECHNOLOGY DESCRIPTION (continued)

- Metallization: Metal 3 and Metal 2 consisted of aluminum with a titanium-nitride/titanium cap and a tungsten barrier. Metal 1 consisted of tungsten and was surrounded by a titanium-nitride cap and had a thick titanium-nitride barrier. A thin titanium adhesion layer was also present under the metal 1 barrier. All metal levels were patterned by a dry etch of good quality. Standard vias and contacts were used (no plugs.)

- Intermetal dielectrics (IMD 2 and IMD 1): Both intermetal dielectrics consisted of the same oxide structure. Two layers of silicon-dioxide with a SOG (spin-on-glass) between. It did not appear that either layer of silicon-dioxide had been subjected to an etchback or CMP (chemical-mechanical-planarization).

- Pre-metal glass: Two layers of reflow glass with undoped oxides between. Both glass layers were reflowed prior to contact cuts only.

- Polysilicon: Five layers of polysilicon were used. Poly 5 formed the capacitor sheet in the array and poly 4 formed the individual capacitor plates with poly 2 "stems" in the array. Poly 3 (poly 3 and tungsten-silicide) formed the bit lines in the array and poly 1 (poly 1 and tungsten-silicide) was used to form all gates on the die.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Sidewall spacers (densified oxide or nitride) provided the LDD spacing and were left in place.

- A multiple-well structure was used. In addition to the twin wells, a deep N-well was present under the array with the P-well employed within the N-well.

TECHNOLOGY DESCRIPTION (continued)

- Memory cells: The memory cells consisted of a stacked capacitor "crown" DRAM design employing five poly layers. No metal layers were used directly in the cells. Poly 5 was a thin sheet of poly used to form the top plate of all capacitors in the array and was tied to a memory enable. Poly 4 was used to form the individual bottom plates of the capacitors with poly 2 "stems" which were connected to one side of the select gates. Poly 3 (polycide) formed the bit lines and poly 1 (polycide) was used to form all word lines and select gates. The capacitor dielectric was probably an oxide-nitride; however, positive identification was beyond the scope of the analysis. There also appeared to be a thin nitride layer over the poly 3 and directly under the poly 5 sheet.

- Fuses: Fuse structure was highly unique. Metal 3 formed the fuses and were laser blown prior to final passivation deposition. Poly 1 links were located directly beneath the fuses and appeared to be used to absorb the excess laser energy. No cutouts were present over the fuses.

ANALYSIS RESULTS I

Assembly: **Figures 1, 2, 6 and 7**

Questionable Items:[1] None.

Special Features:

- Lead On Chip Center Bonded (LOCCB) leadframe design.

General Items:

- 32-pin Thin Small Outline Package (TSOP) with LOCCB leadframe design.
- Overall package quality: Normal. No defects were found on the external portion of the packages. No cracks or voids were found in the plastic packages.
- Die dicing: Die separation was by sawing of normal quality workmanship. No cracks or large chips were present. Test patterns were present in the scribe lane.
- Die attach: The surface of the die was attached to the underside of the leadframe with an adhesive tape (probably Kapton tape).
- Wirebonding: Thermosonic ball bond method using 0.9 mil gold wire. Wire spacing and placement were good. Ball bonds were somewhat overcompressed; however, no problems are foreseen.
- Die coat: Patterned polyimide was present over the die surface. No problems were found.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process and Design: **Figures 3 - 39**

Questionable Items:[1]

- Aluminum 2 and 3 thinning up to 100 percent[2] at via edges (Figures 13 and 17). Barrier metal maintained continuity.

Special Features:

- Sub-micron gates (N-ch 0.35 micron, P-ch 0.5 micron).
- Three layers of metal (no plugs). Tungsten used as metal 1 interconnect.
- Five layers of polysilicon.
- "Crown" DRAM capacitor structure. Cell size 1.2 microns.

General Items:

- Fabrication process: Selective oxidation, multiple-well CMOS process in a P substrate, no epi. An apparent deep N-well was used under the array with a P-well employed within.
- Process Implementation: Die layout was clean and efficient. Alignment was good at all levels and no damage, process defects, or contamination was found.
- Final passivation: Passivation consisted of a single layer of nitride over two layers of silicon-dioxide. Integrity tests indicated defect-free passivation. Edge seal was also good as the passivation extended to the scribe lane. A cutout was present at the die edge, which may prevent cracks from radiating inward over active circuitry during dicing.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metallization: Metal 3 and Metal 2 consisted of aluminum with titanium-nitride/titanium cap and a tungsten barrier. Metal 1 consisted of tungsten and was surrounded by a titanium-nitride cap and had a thick titanium-nitride barrier. A thin titanium adhesion layer was also present under the metal 1 barrier. No cracks were present in any cap or barrier metals.

- Metal patterning: All metal layers were defined by a dry etch of good quality. Minimum width metal lines were widened around contact and vias.

- Metal defects: No voiding, notching, or neckdown of the metal layers was found. No silicon nodules were found following removal of either aluminum layer.

- Metal step coverage: Metal 3 and Metal 2 aluminum thinned up to 100 percent at vias. The barrier metal maintained continuity and will compensate for some aluminum thinning. Metal 1 thinned up to 75 percent at some contacts.

- Contact defects: None. No significant overetching of the vias or contacts was noted.

- Intermetal dielectrics: Both intermetal dielectrics consisted of two layers of silicon-dioxide separated by a spin-on-glass (SOG) for planarization. It did not appear that either layer of silicon-dioxide was subjected to an etchback or CMP. No problems were present

- Pre-metal glass: Two layers of reflow glass with undoped oxides between. Both glass layers were reflowed prior to contact cuts only. No problems were found.

- Polysilicon: Five layers of polysilicon were used. Poly 1 (polycide) was used to form all gates. Poly 2 through 5 were used exclusively in the cell array. Poly 3 (polycide) was used as an interconnect (metal substitute) for the bit lines in the array. Poly 4 formed the individual plates of the stacked capacitor cell with poly 2 “stems” and poly 5 formed the common plate. Definition of all layers was by a dry etch of good quality. No stringers or spurs were noted and no problems were found.

ANALYSIS RESULTS II (continued)

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Sidewall spacers (densified oxide or nitride) provided the LDD spacing and were left in place. No problems were found.

- Wells: Multiple wells in a P substrate (no epi). A deep N-well appeared to be used under the array with a P-well employed within.

- Fuses: Fuse structure was highly unique. Metal 3 formed the fuses and were laser blown prior to final passivation deposition. Poly 1 links were located directly beneath the fuses and appeared to be used to absorb the excess laser damage. No cutouts were present over the fuses.

- Memory cells: The memory cells consisted of a stacked capacitor "crown" DRAM design employing five poly layers. No metal layers were used directly with the cells. Poly 5 was a thin sheet of poly used to form the top plate of all capacitors in the array and was tied to a memory enable. Poly 4 was used to form the individual bottom plates of the capacitors with poly 2 "stems" which were connected to one side of the select gates. Poly 3 (polycide) formed the bit lines and poly 1 (polycide) was used to form all word lines and select gates. The capacitor dielectric was probably an oxide-nitride; however, positive identification was beyond the scope of the analysis. There also appeared to be a thin nitride layer over the poly 3 and directly under the poly 5 sheet. Cell size was 0.9 x 1.4 microns.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 3

Metal 3 removal and delayer to metal 2

SEM inspection of metal 2

Metal 2 removal and delayer to metal 1

SEM inspection of metal 1

Metal 1 removal

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Material analysis

Horizontal dimensions

Vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal/Poor

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wire spacing	N
Wirebond placement	N
Wirebond quality	N
Dicing quality	N
Dicing method	Sawn (full depth)
Die attach method	Adhesive
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal registration	G
Metal integrity	NP*
Contact coverage	G
Contact registration	G

**Metal 2 and 3 aluminum thinning up to 100 percent.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

Top

(LOGO) JAPAN A001
9705 31N
5165805ATT6

WIREBOND STRENGTH

Wire material:	0.9 mil diameter gold
Die pad material:	aluminum
# of wires tested:	16
Bond lifts:	0
Force to break - high:	8 g
- low:	4 g
- avg.: 5.3 g	
- std. dev.:	1.0

DIE MATERIAL ANALYSIS

Overlay passivation:	A single layer of nitride over two layers of silicon-dioxide.
Metal 3:	Aluminum with a thin titanium-nitride/ titanium cap and a tungsten barrier.
Intermetal dielectric:	Two layers of silicon-dioxide separated by a spin-on-glass (SOG).
Metal 2:	Aluminum with a thin titanium-nitride/ titanium cap and a tungsten barrier.
Metal 1:	Tungsten surrounded by a titanium-nitride cap on a titanium-nitride/titanium barrier.
Pre-metal dielectric:	Two layers of CVD glass.

Silicide on poly 1 and 2:	Tungsten.

HORIZONTAL DIMENSIONS

Die size:	8.7 x 18.4 mm (343 x 723 mils)
Die area:	160 mm^2 (247,989 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.1 x 0.1 mm (4 x 4 mils)
Min pad space:	0.03 mm (1.3 mils)
Min metal 3 width:	1.0 micron
Min metal 3 space:	1.1 micron
Min metal 3 pitch:	2.1 microns
Min metal 2 width:	0.8 micron
Min metal 2 space:	0.8 micron
Min metal 2 pitch:	1.6 micron
Min metal 1 width:	0.4 micron
Min metal 1 space:	0.5 micron
Min metal 1 pitch:	0.9 micron
Min via (M3 - M2):	0.7 micron (round)
Min via (M2 - M1):	0.9 micron (round)
Min contact:	0.4 micron (round)
Min poly 4 width:	0.5 micron
Min poly 4 space:	0.25 micron
Min poly 3 width:	0.25 micron
Min poly 3 space:	0.4 micron
Min poly 1 width:	0.2 micron
Min poly 1 space:	0.4 micron
Min gate length - N-channel:	0.35 micron (in array)
- P-channel:	0.5 micron
Cell pitch:	0.9 x 1.4 microns
Cell size:	1.26 $micron^2$

VERTICAL DIMENSIONS

Layers

Passivation 3:	1.2 micron
Passivation 2:	0.4 micron
Passivation 1:	0.5 micron
Metal 3 - cap:	0.04 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.18 micron
Intermetal dielectric 2 - glass 2:	0.25 micron
- SOG:	0 - 1.1 micron
- glass 1:	0.3 micron
Metal 2 - cap:	0.07 micron (approximate)
- aluminum:	0.4 micron
- barrier:	0.2 micron
Intermetal dielectric 1 - glass 2:	0.25 micron
- SOG:	0 - 1.05 micron
- glass 1:	0.25 micron
Metal 1 - cap:	0.02 micron (approximate)
- tungsten:	0.25 micron
- barrier:	0.1 micron
Pre-metal glass:	1.05 micron
Poly 5:	0.1 micron
Poly 4:	0.15 micron
Poly 3 - silicide:	0.08 micron
- poly:	0.17 micron
Poly 1 - silicide:	0.08 micron
- poly:	0.06 micron
Local oxide (under poly 1):	0.3 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.22 micron
N-well:	1.2 micron

Deep N-well:	3.2 microns

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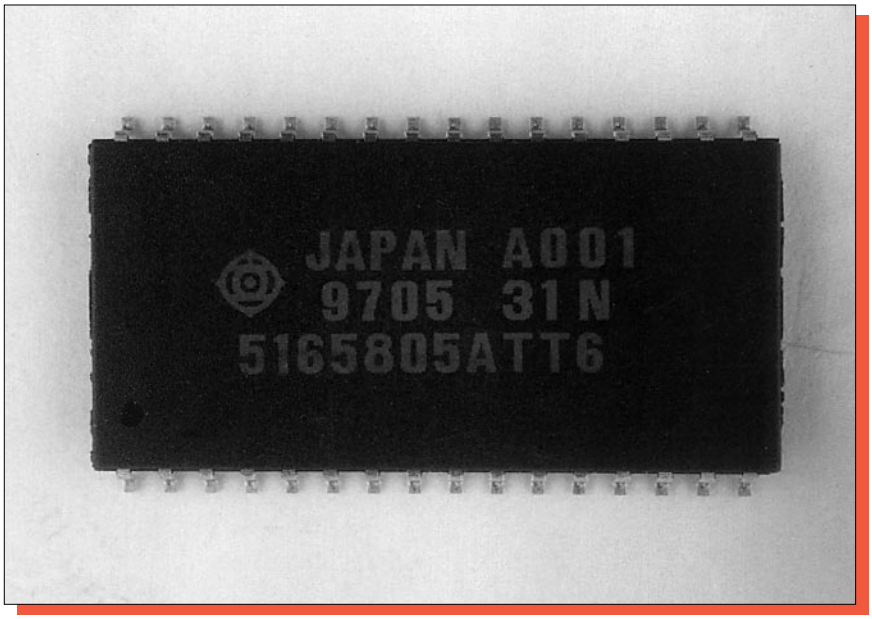


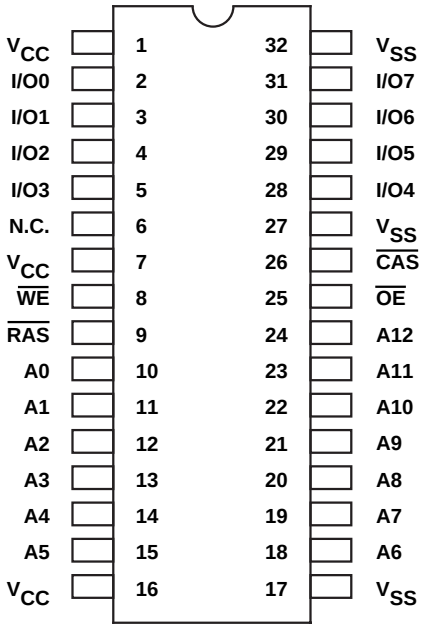


Figure 1. Package photograph and pinout of the Hitachi 5165805ATT6 64Mbit DRAM. Mag. 4x.

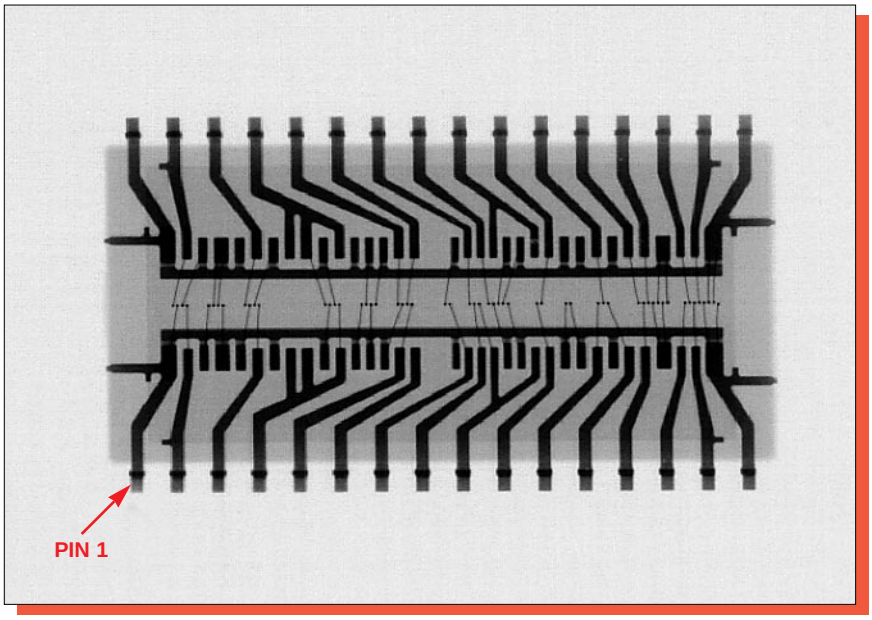


Figure 2. X-ray view of the Hitachi 64Mbit DRAM. Mag. 4x.

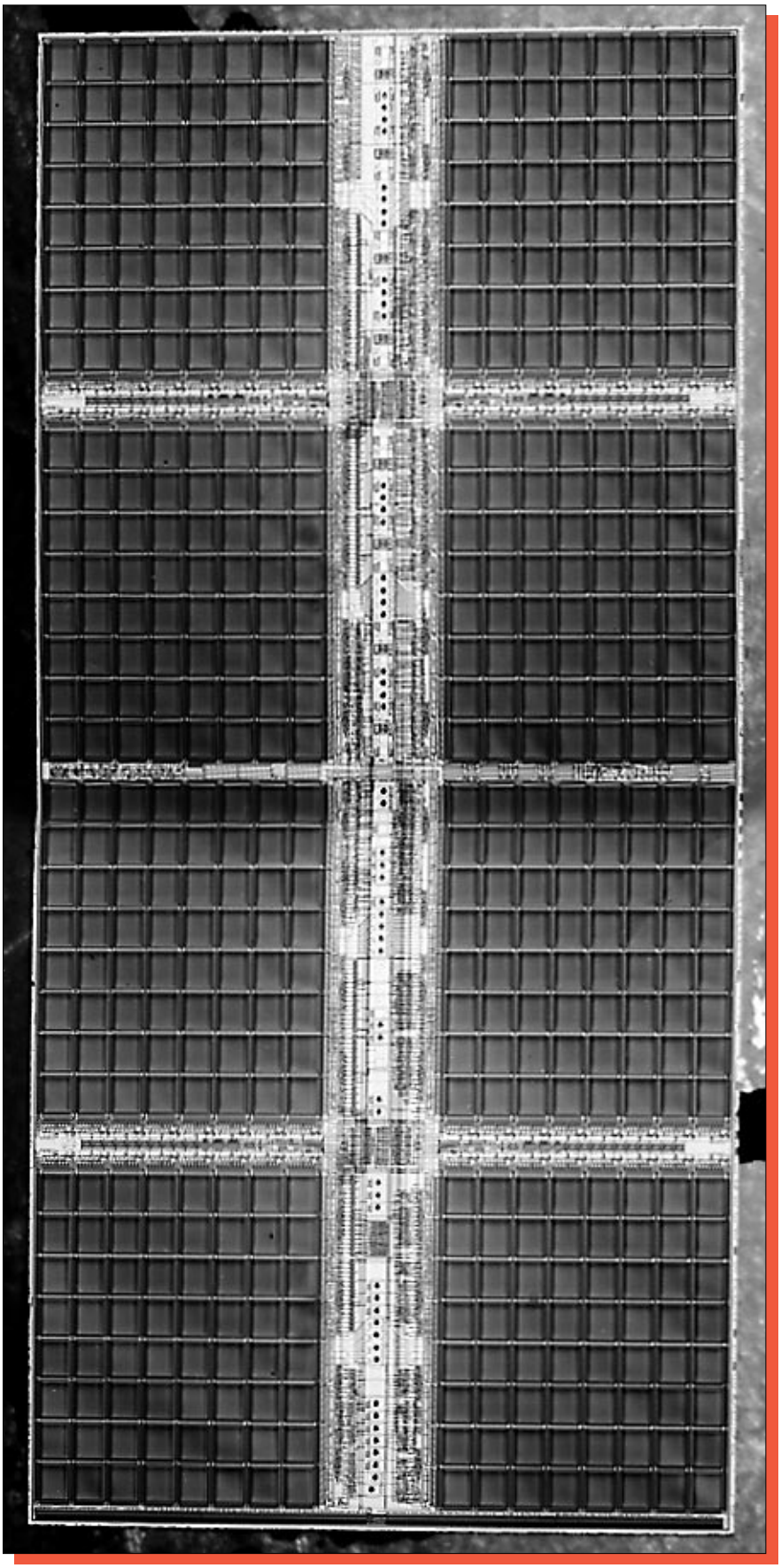
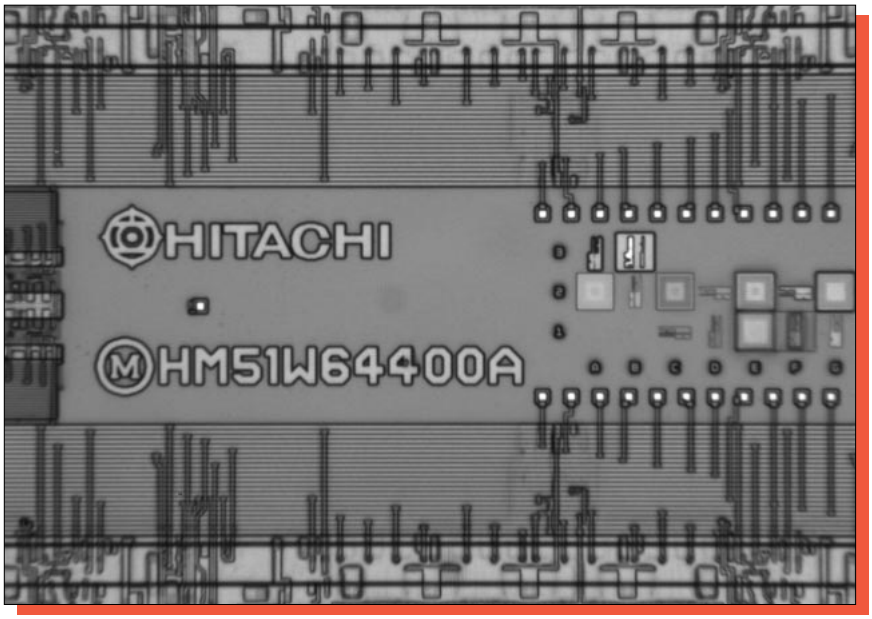


Figure 3. Whole die photograph of the Hitachi 64Mbit DRAM. Mag. 12x.



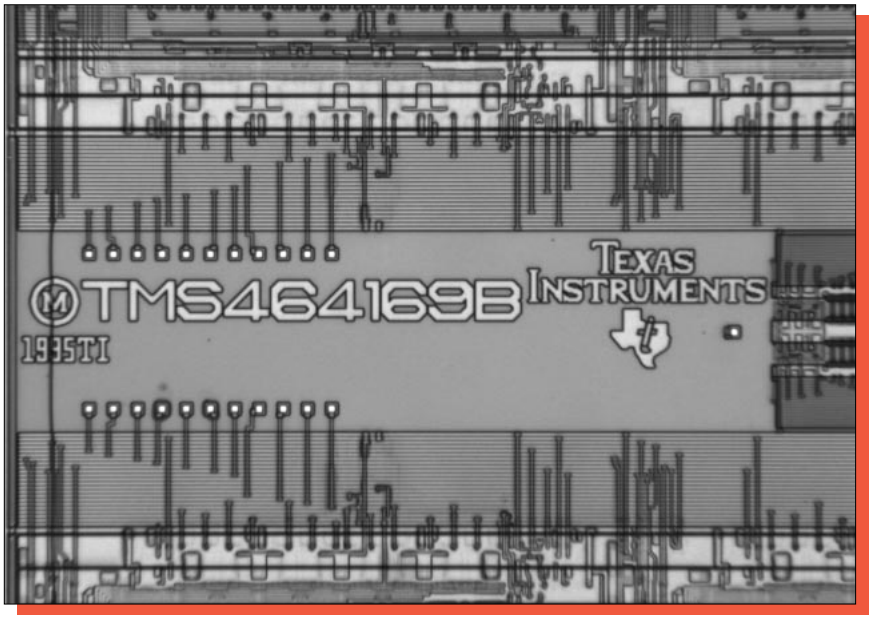


Figure 4. Optical views of die markings. Mag. 175x.

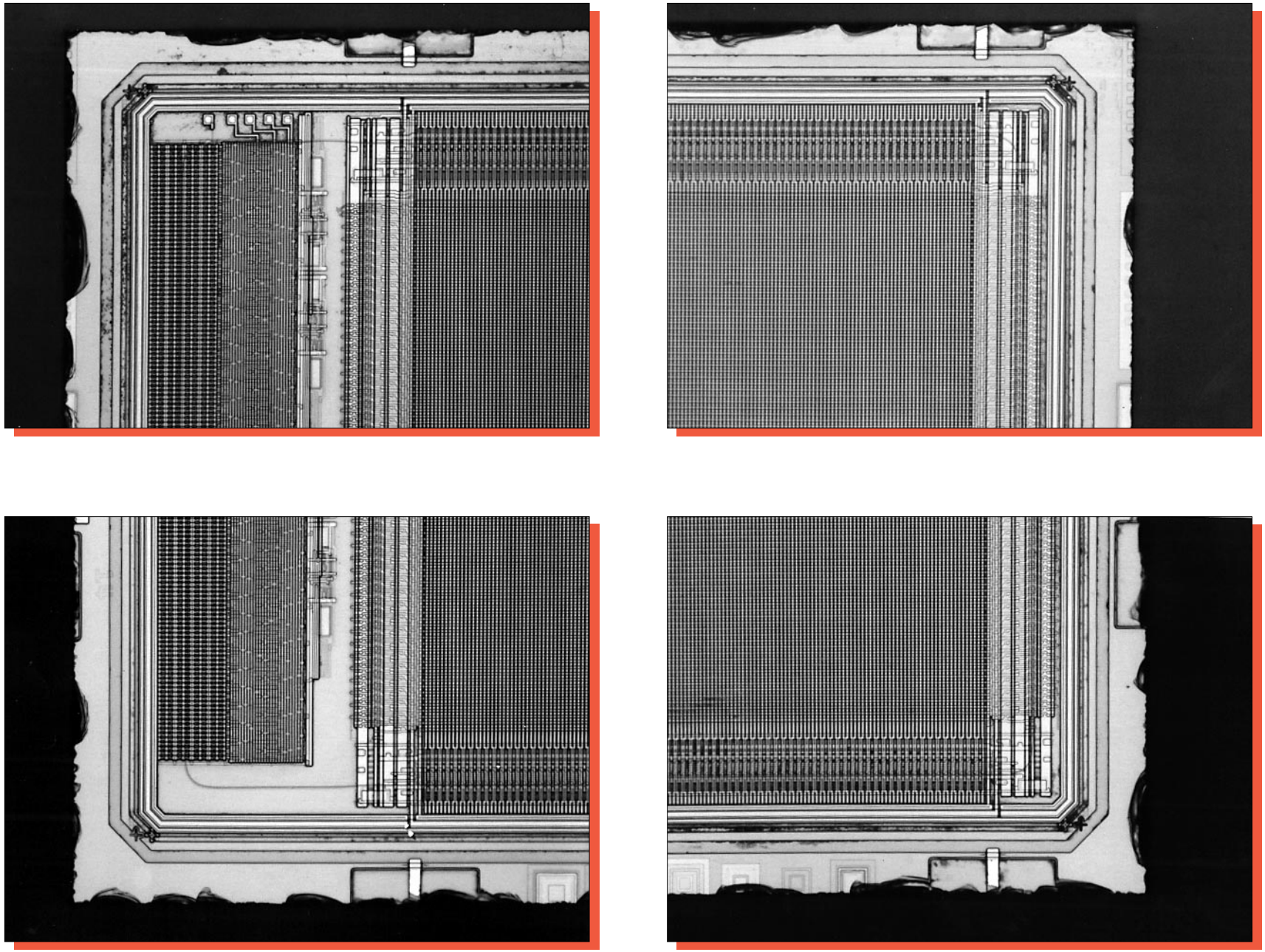
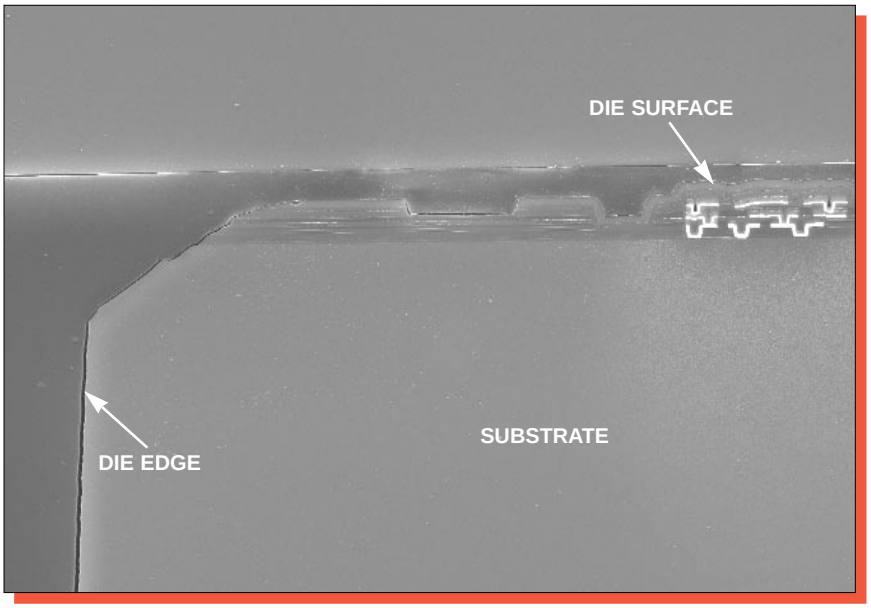
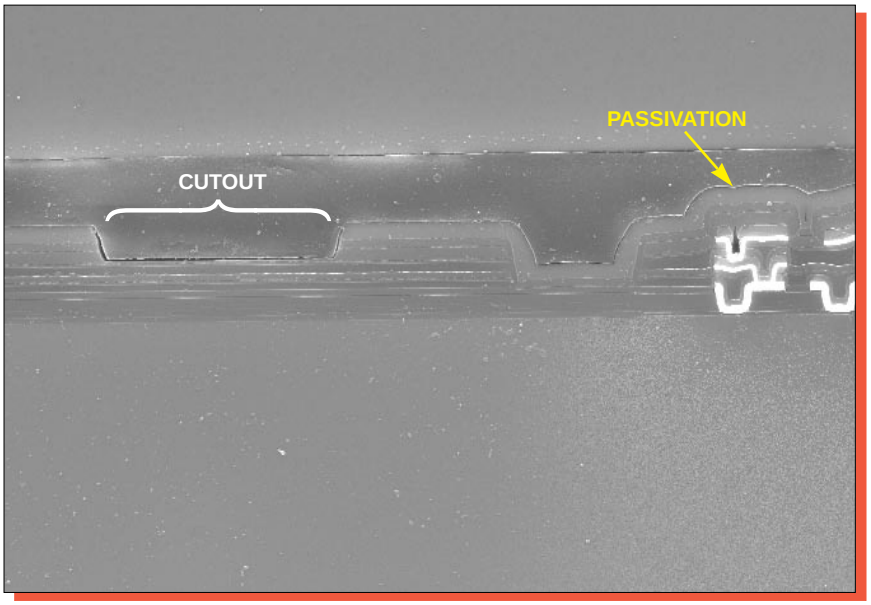


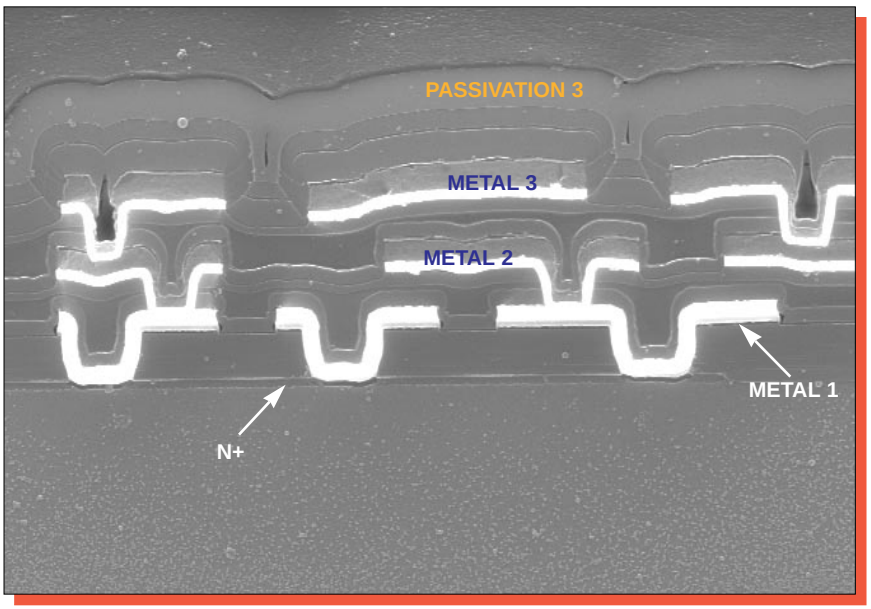
Figure 5. Optical views of die corners. Mag. 200x.



Mag. 1300x

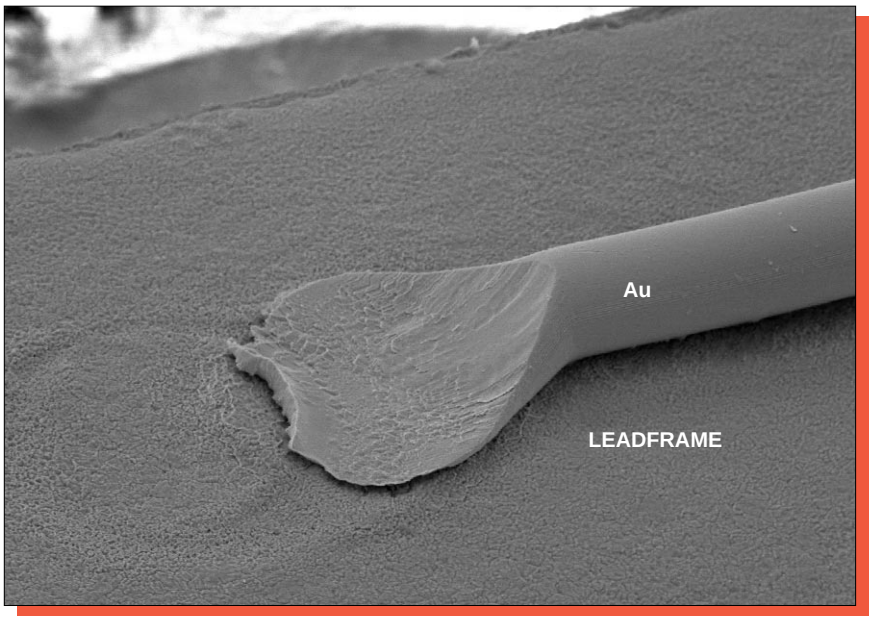


Mag. 2900x

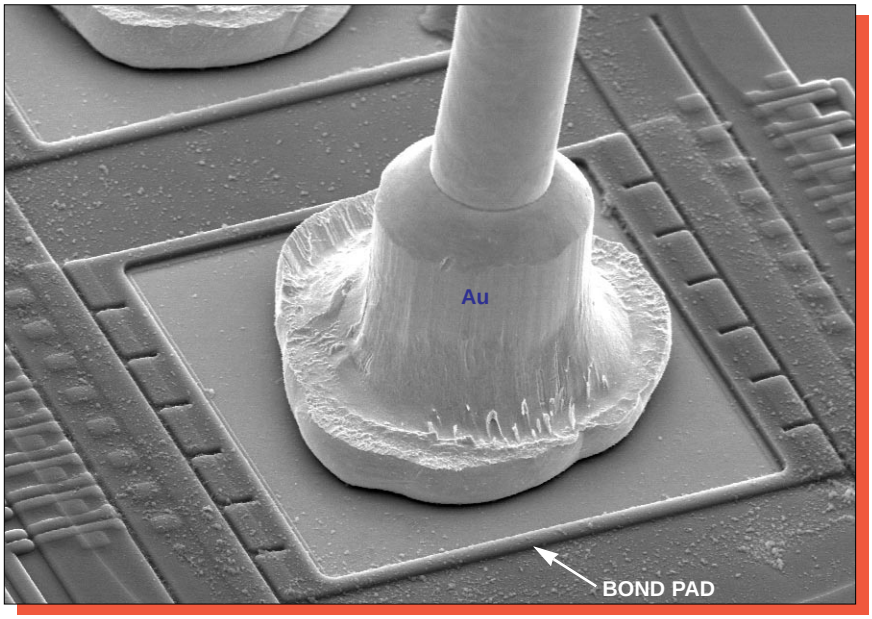


Mag. 7000x

Figure 6. SEM section views of the edge seal structure.

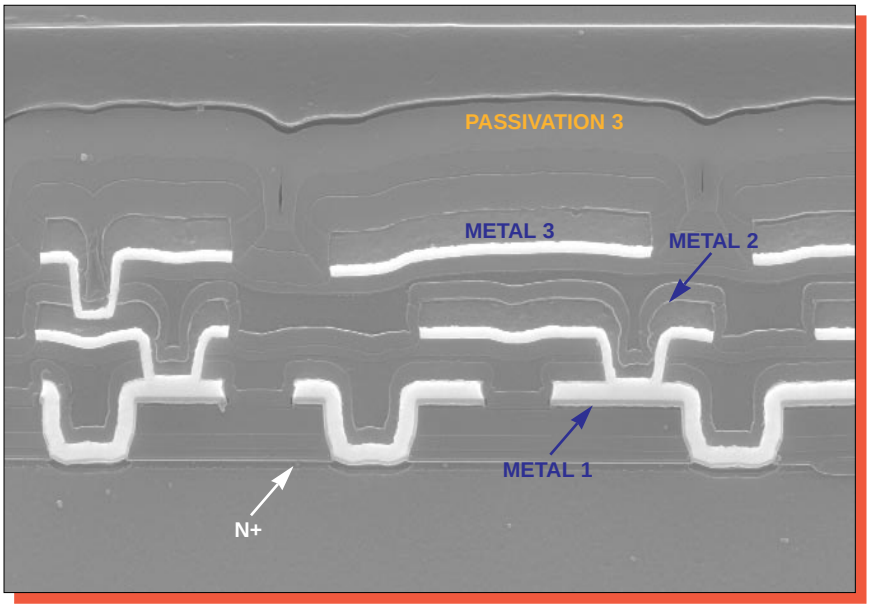


Mag. 600x

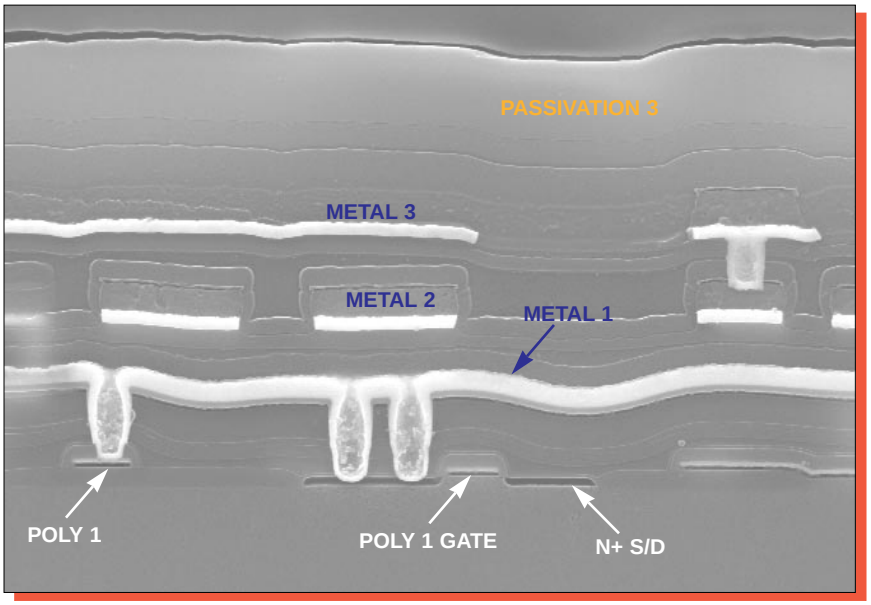


Mag. 680x

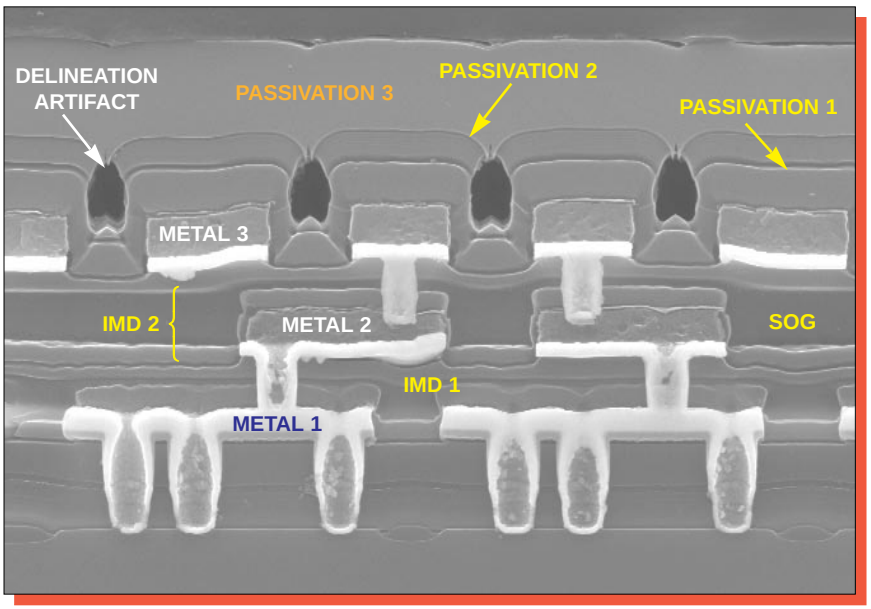
Figure 7. SEM views of typical wirebonds. 60°.



Mag. 8100x

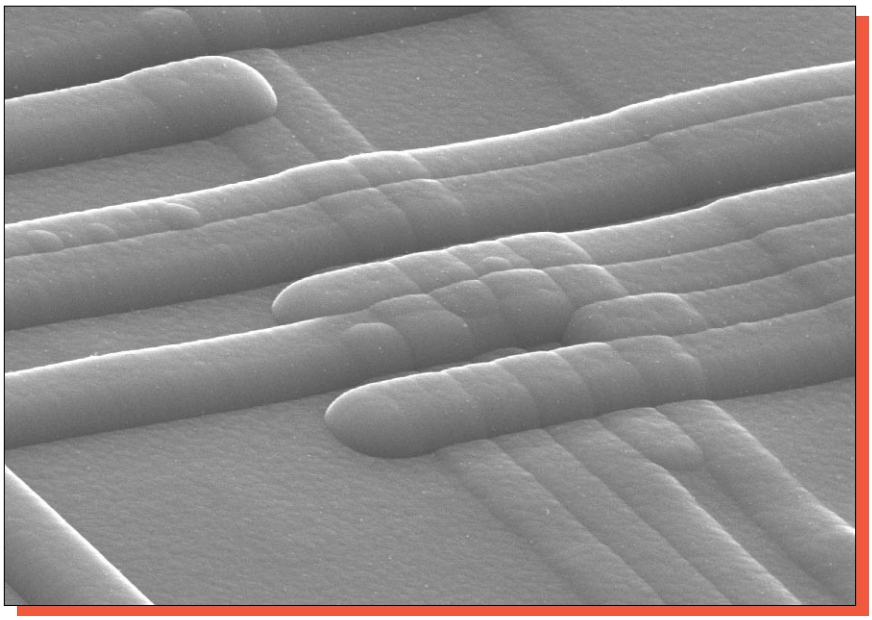


Mag. 9000x

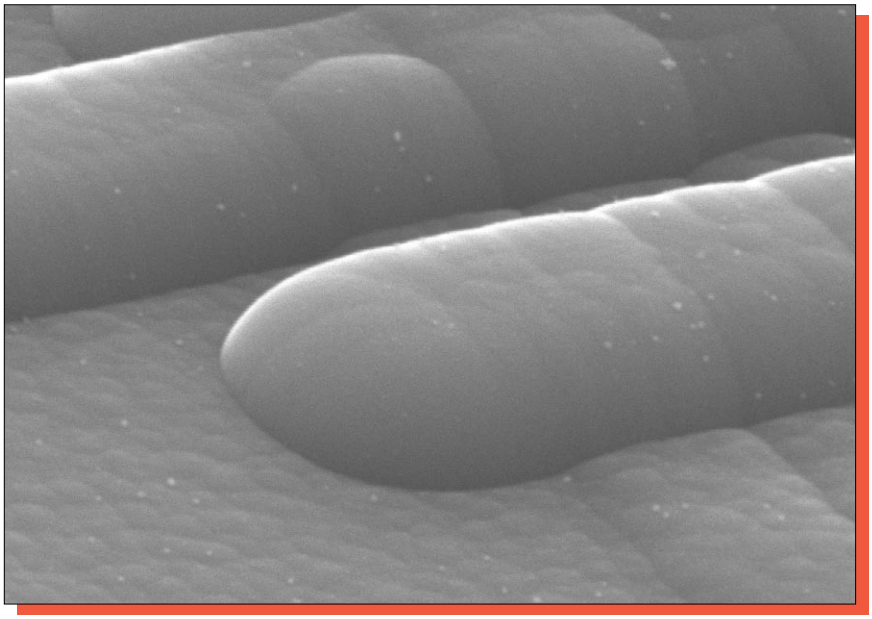


glass etch,
Mag. 10,500x

Figure 8. SEM section views illustrating general device structure.

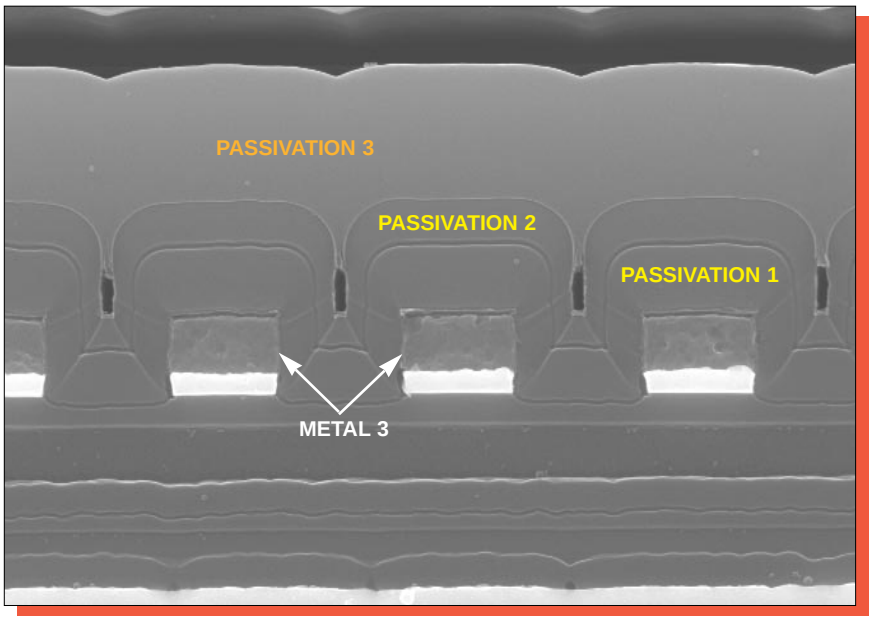


Mag. 4000x

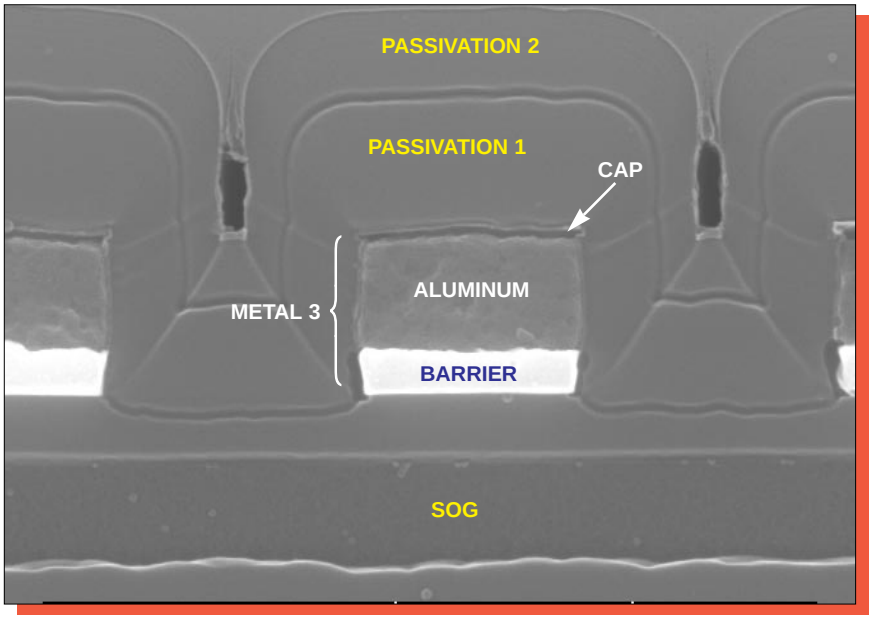


Mag. 13,500x

Figure 9. Perspective SEM views illustrating final passivation coverage. 60°.

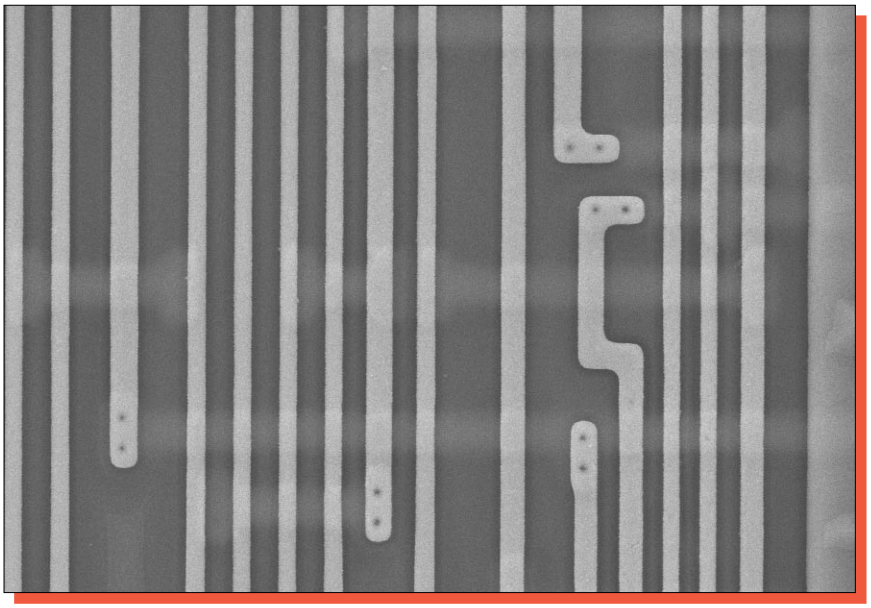


Mag. 15,000x

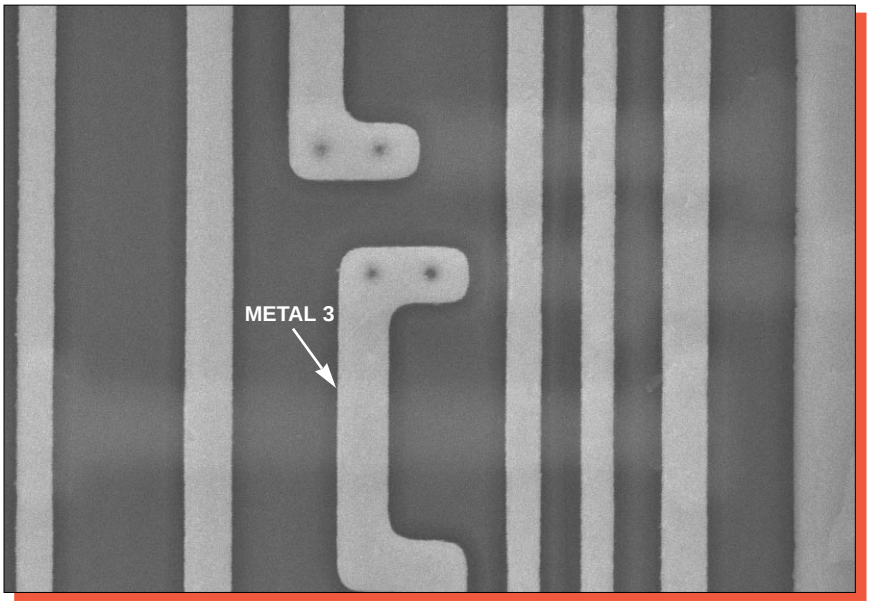


Mag. 30,000x

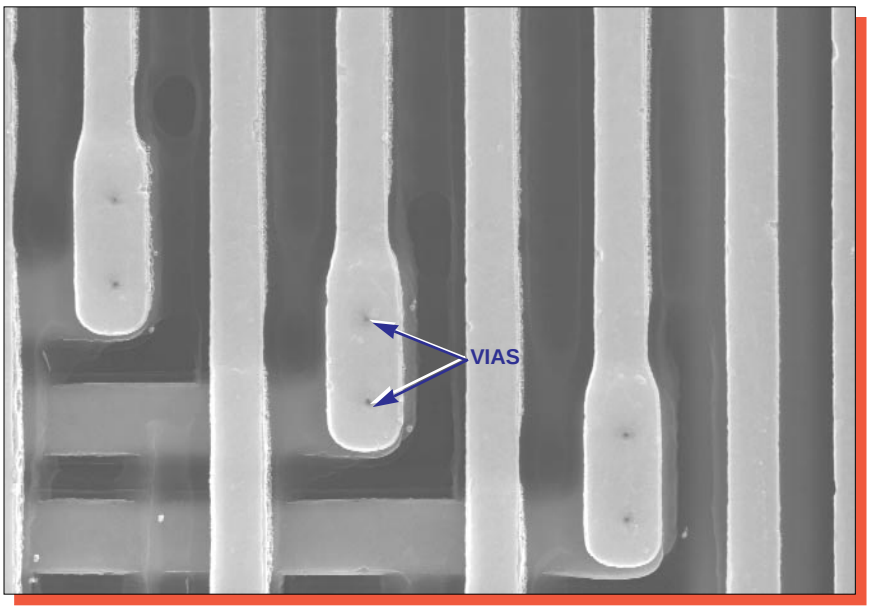
Figure 10. SEM section views of metal 3 line profiles.



Mag. 3100x

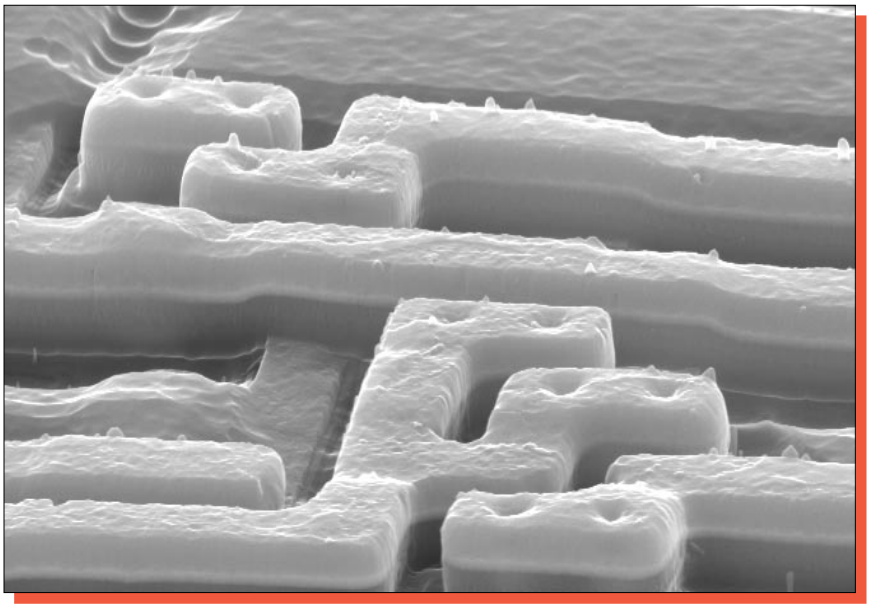


Mag. 6200x

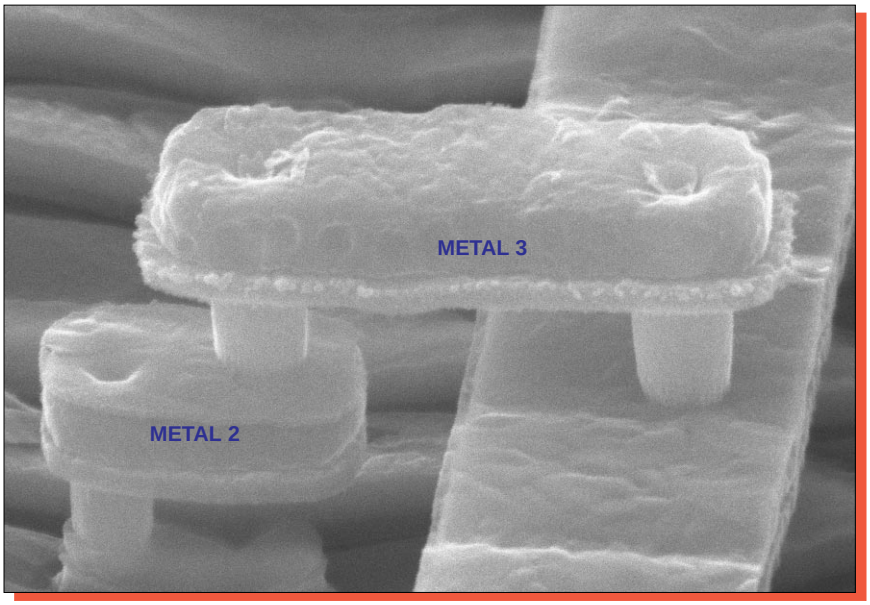


Mag. 8000x

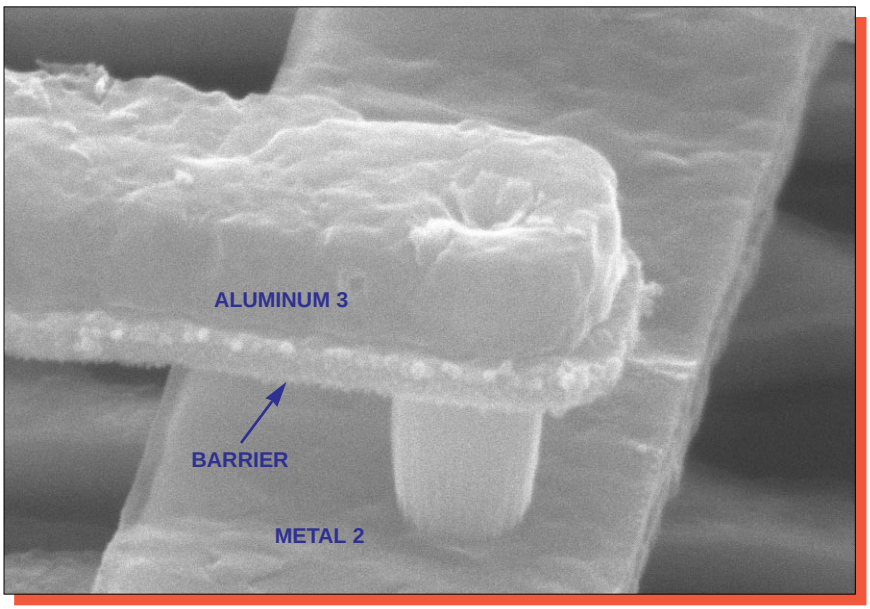
Figure 11. Topological views illustrating metal 3 patterning. 0°.



Mag. 9500x

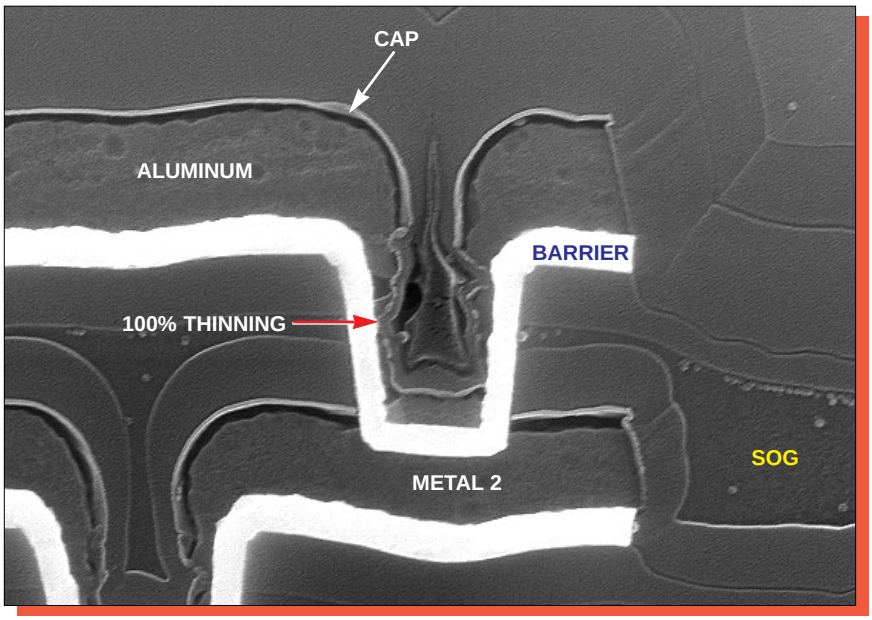


Mag. 25,000x

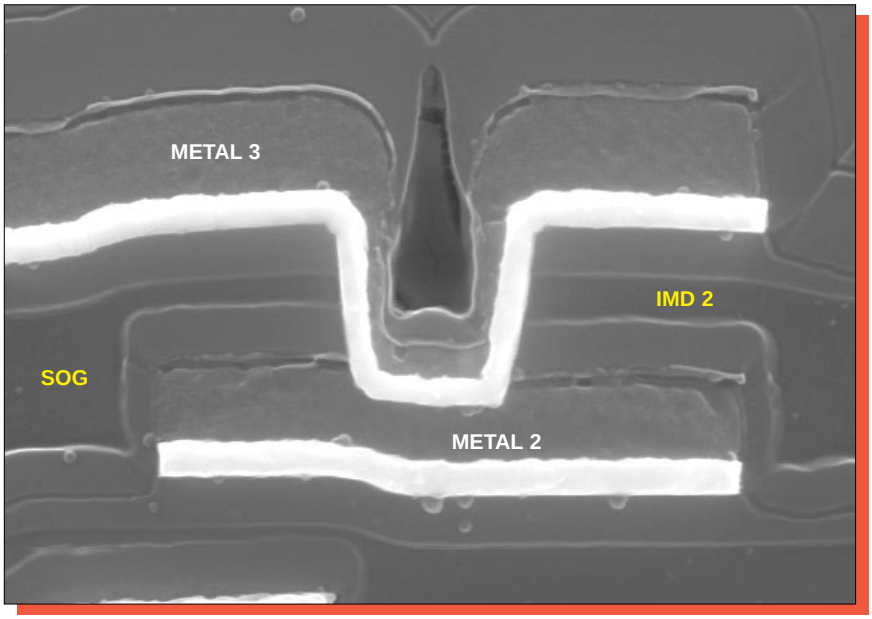


Mag. 35,000x

Figure 12. SEM views illustrating general metal 3 integrity. 60°.

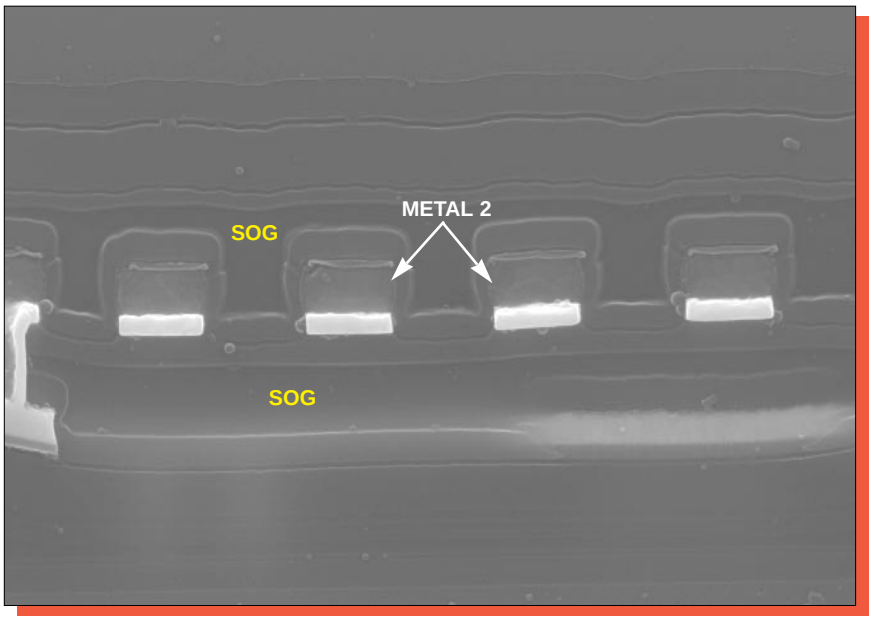


Mag. 28,500x

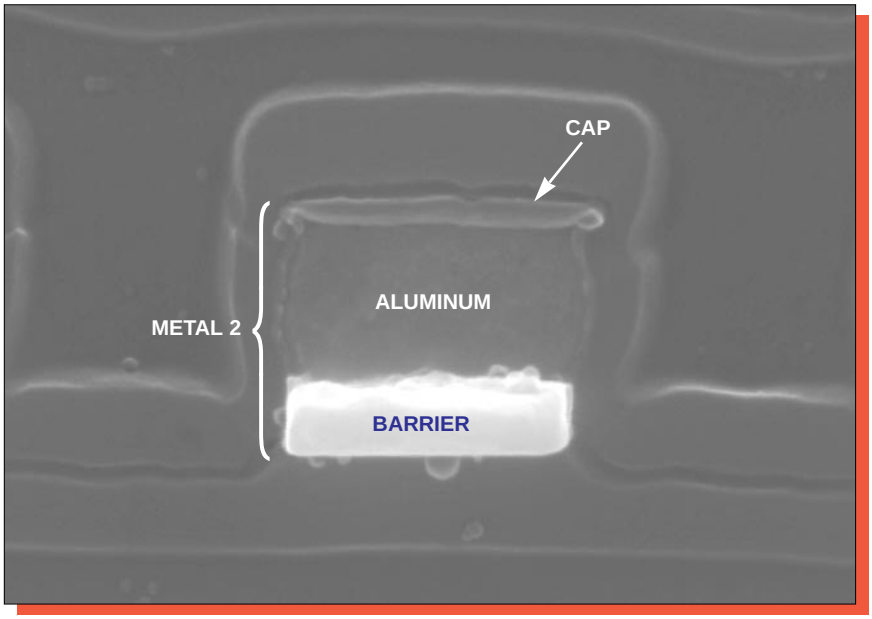


Mag. 25,600x

Figure 13. SEM section views of metal 3-to-metal 2 vias.

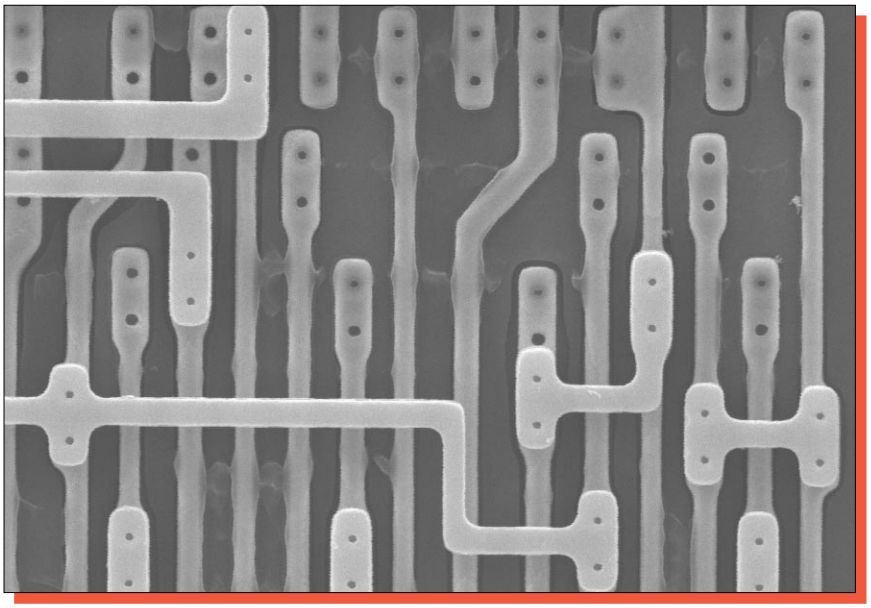


Mag. 15,000x

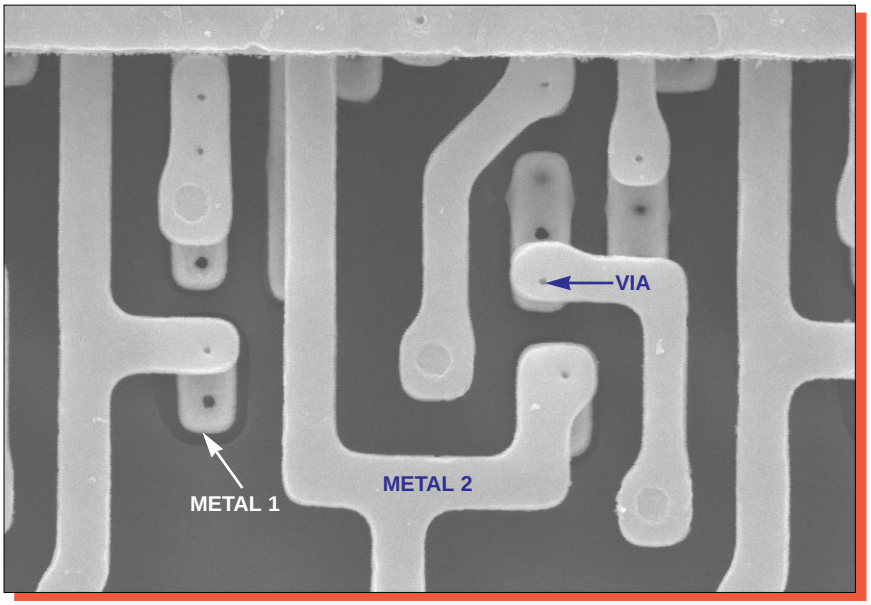


Mag. 50,000x

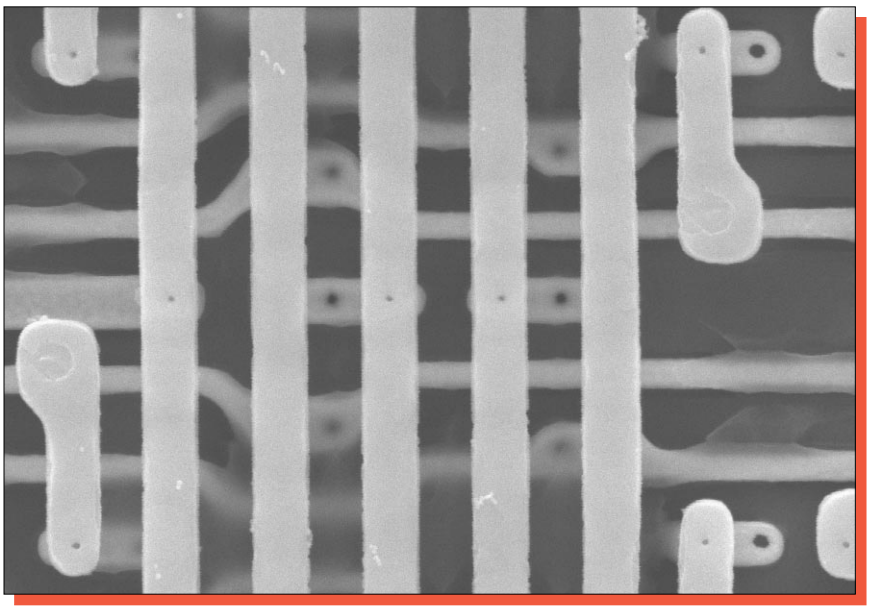
Figure 14. SEM section views of metal 2 line profiles.



Mag. 5000x

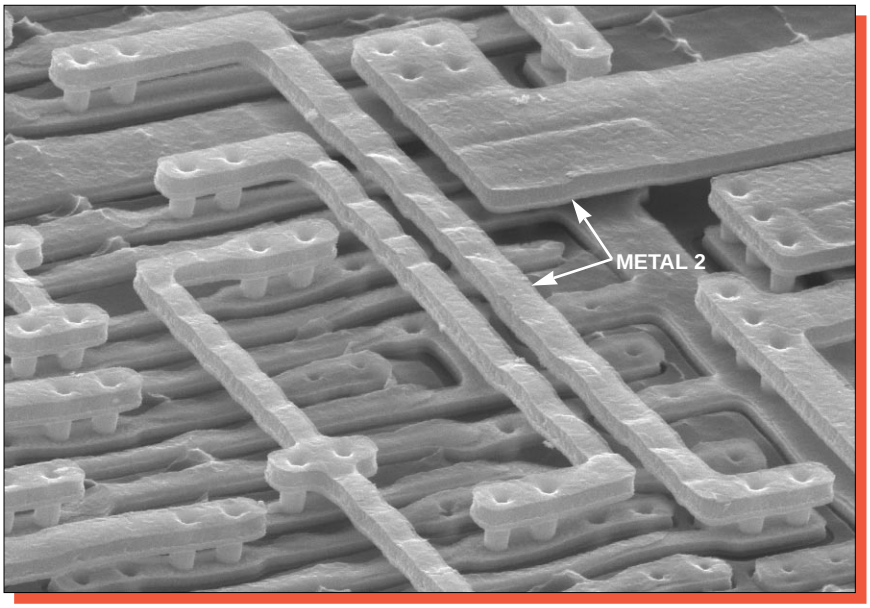


Mag. 9000x

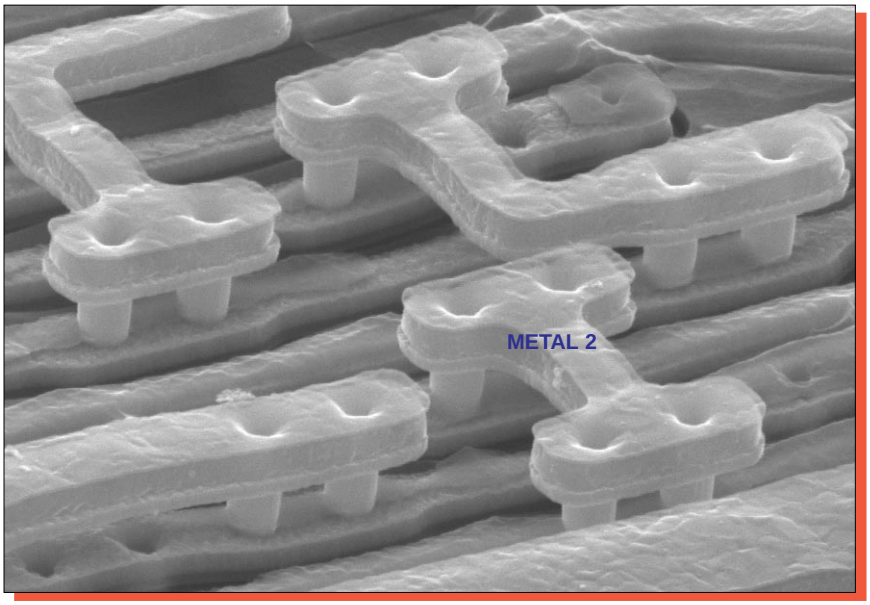


Mag. 10,000x

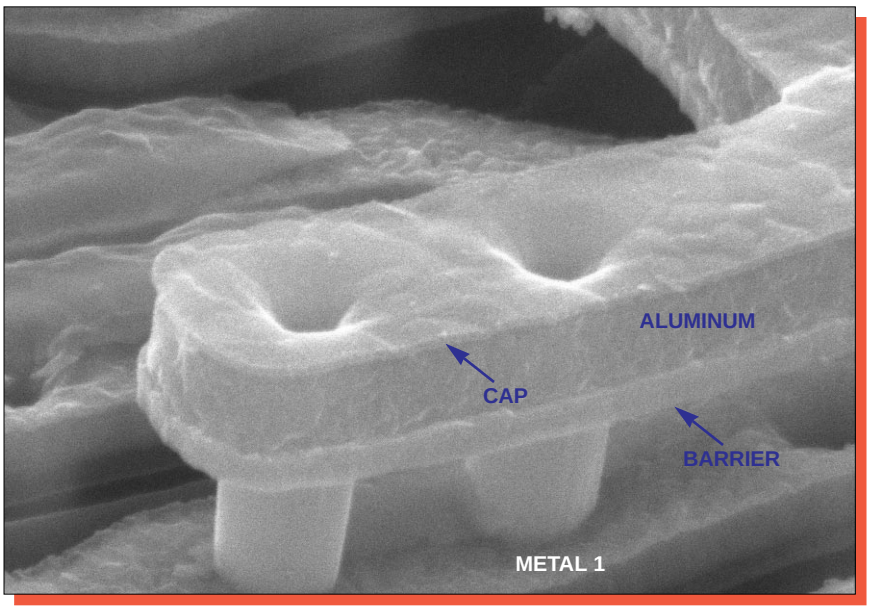
Figure 15. Topological SEM views of metal 2 patterning. 0°.



Mag. 6000x

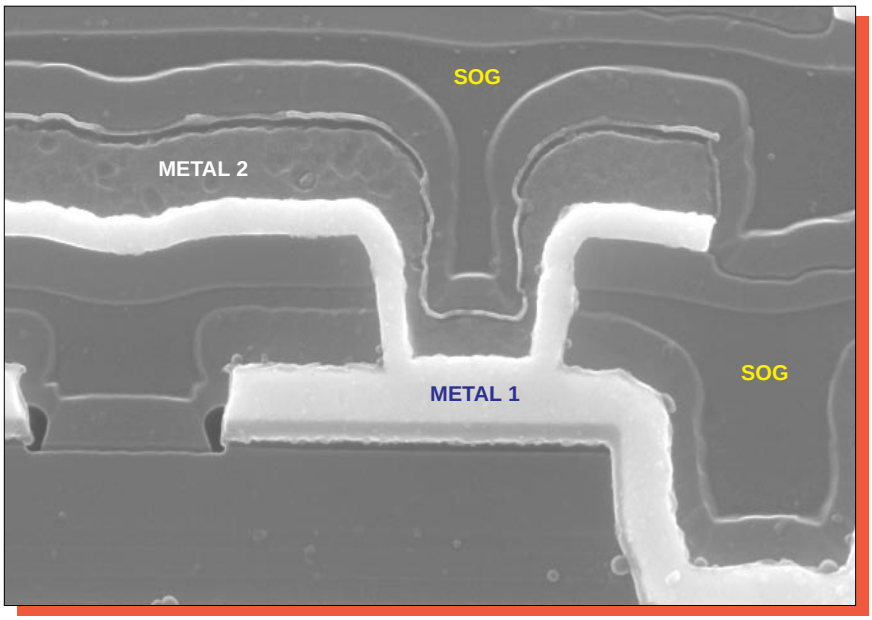


Mag. 12,000x

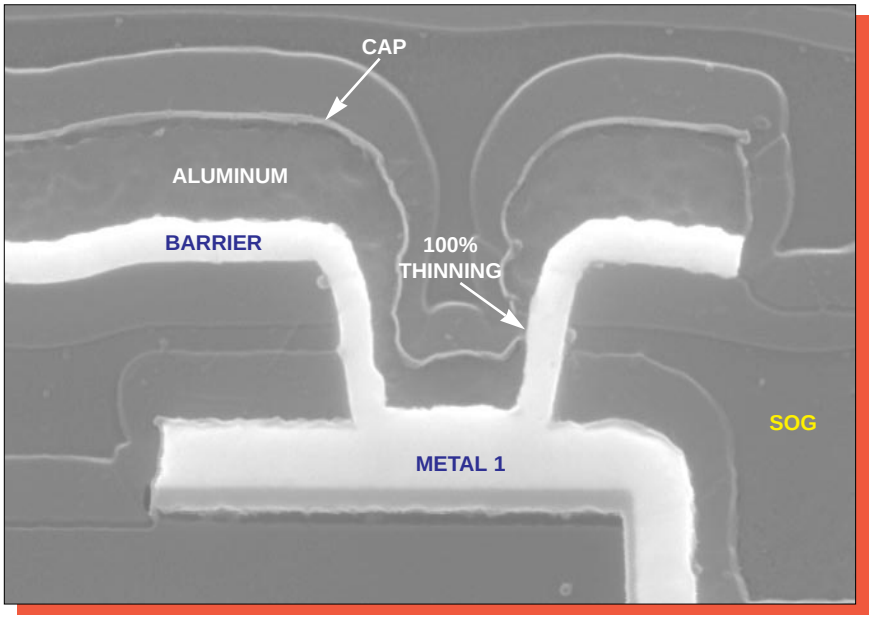


Mag. 32,000x

Figure 16. SEM views of general metal 2 integrity. 60°.

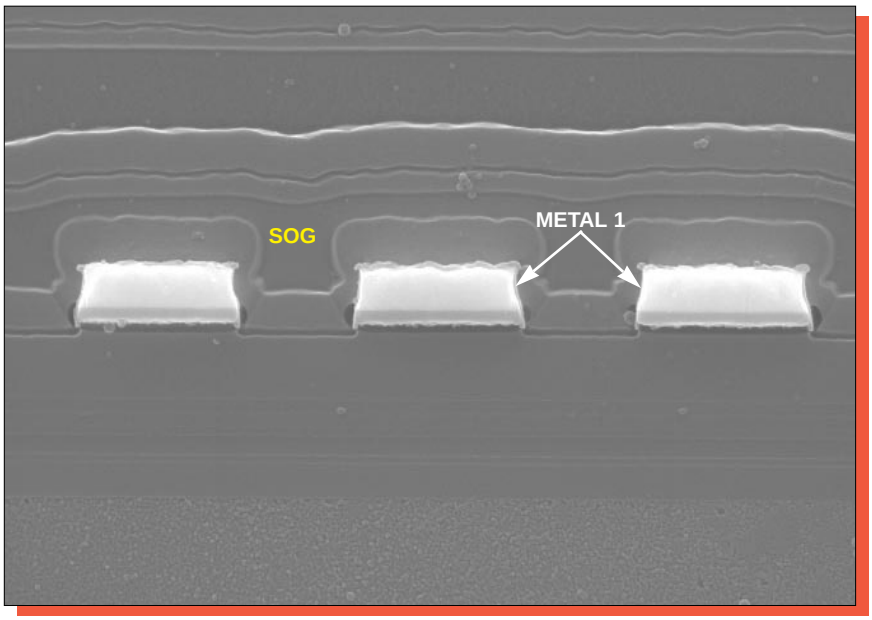


Mag. 25,000x

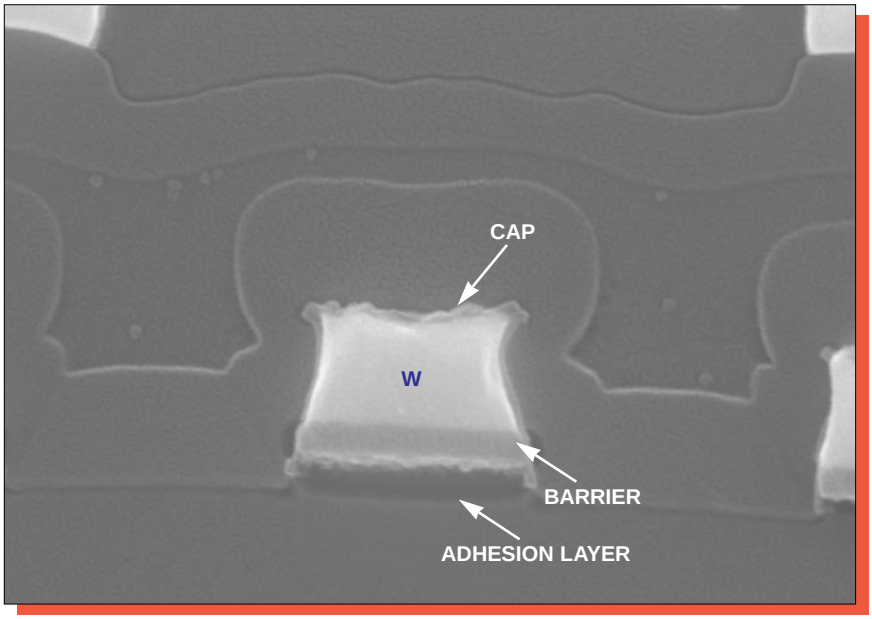


Mag. 30,000x

Figure 17. SEM section views of metal 2-to-metal 1 vias.

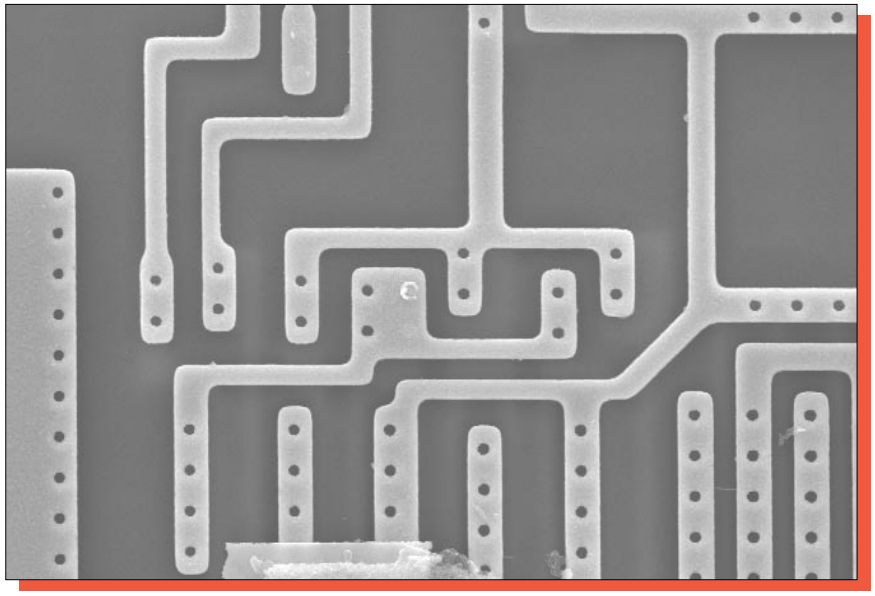


Mag. 20,000x

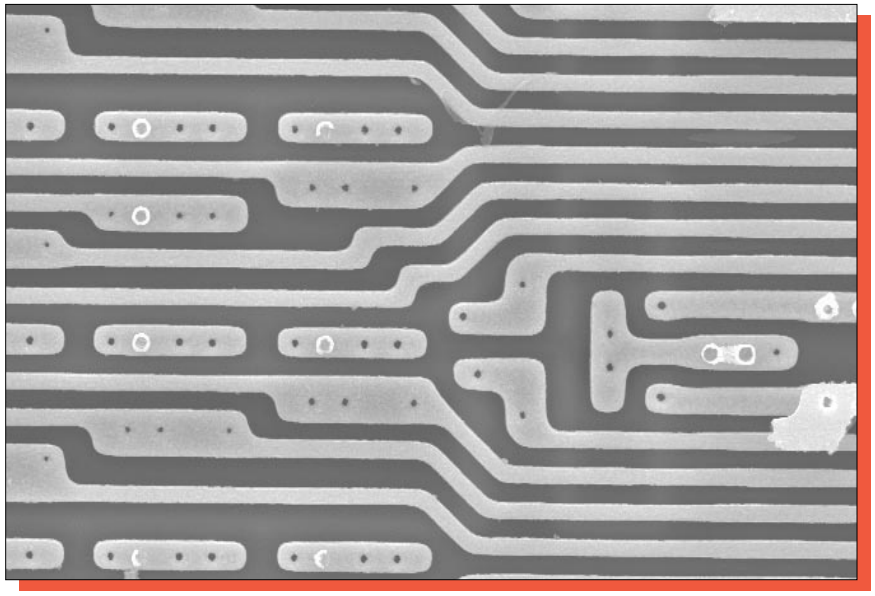


Mag. 55,000x

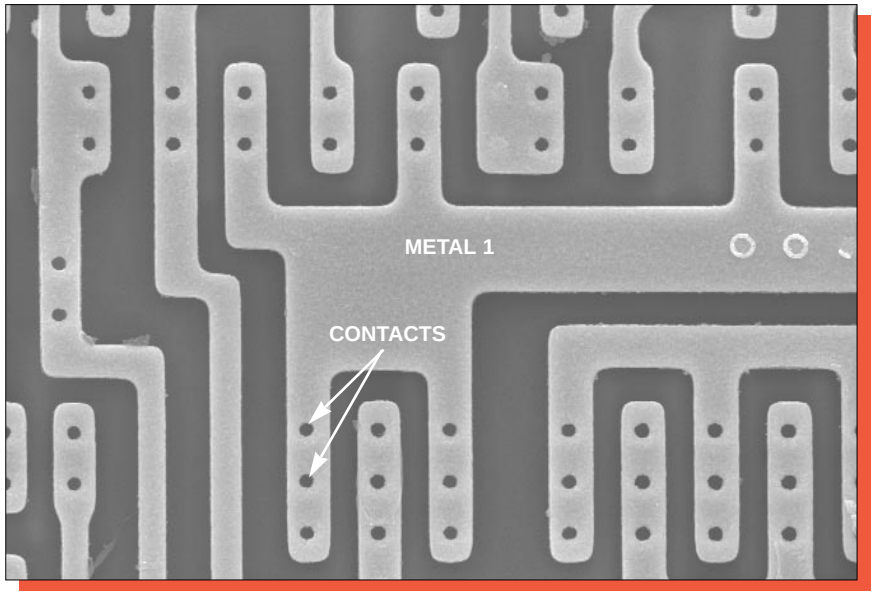
Figure 18. SEM section views of metal 1 profiles.



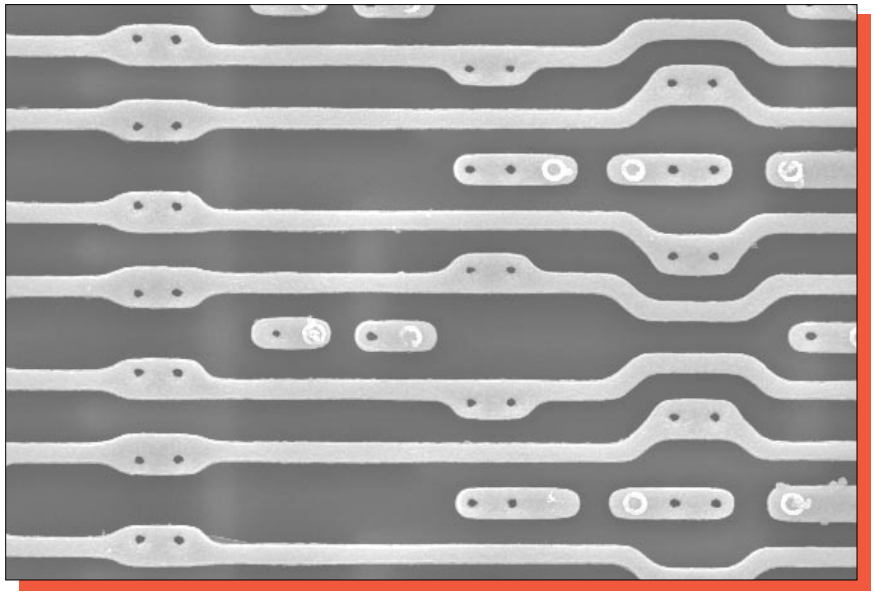
Mag. 4000x



decode, Mag. 5000x

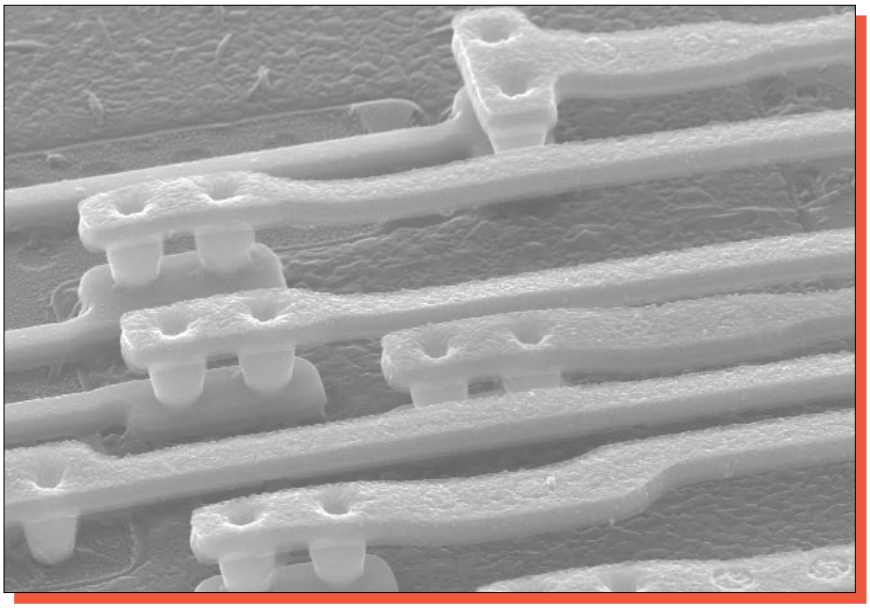


Mag. 5000x

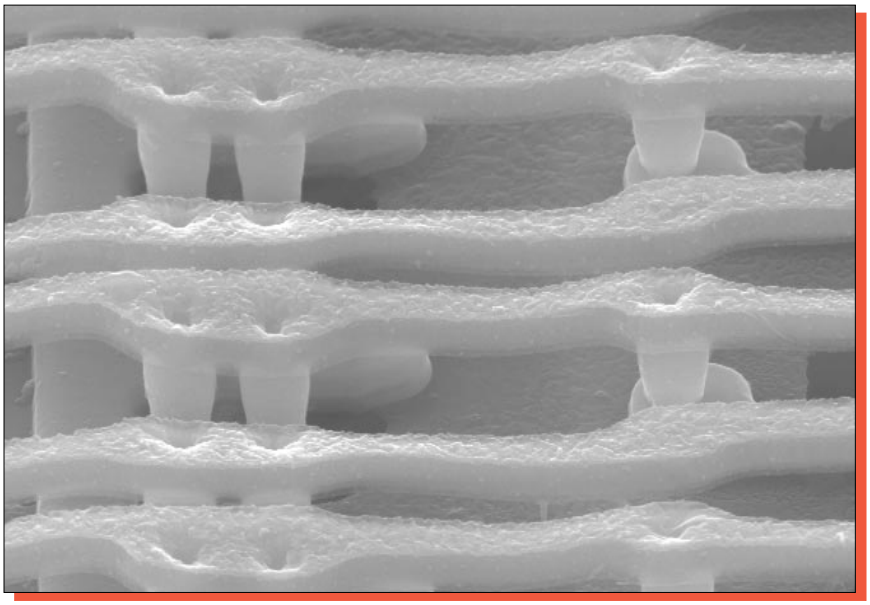


decode, Mag. 6000x

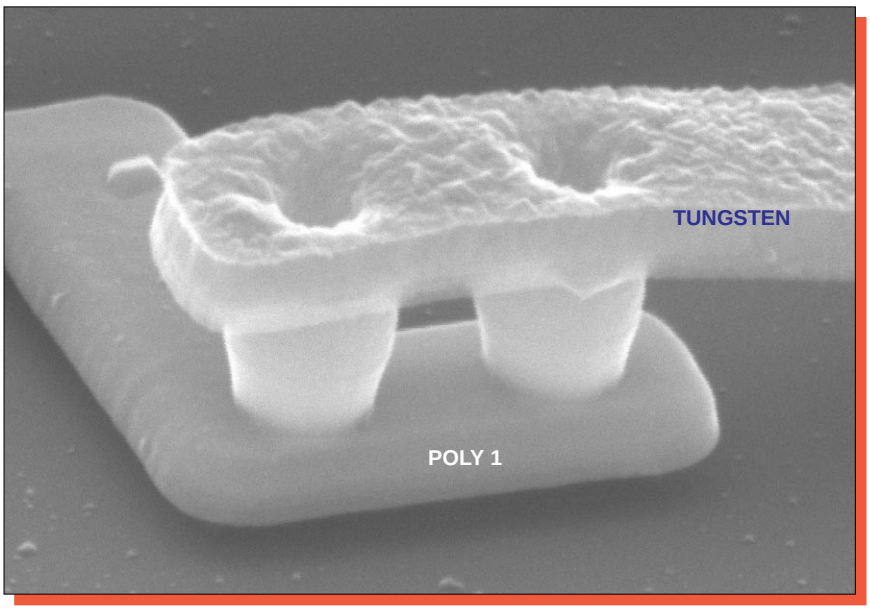
Figure 19. Topological SEM views of metal 1 patterning. 0°.



Mag. 9000x

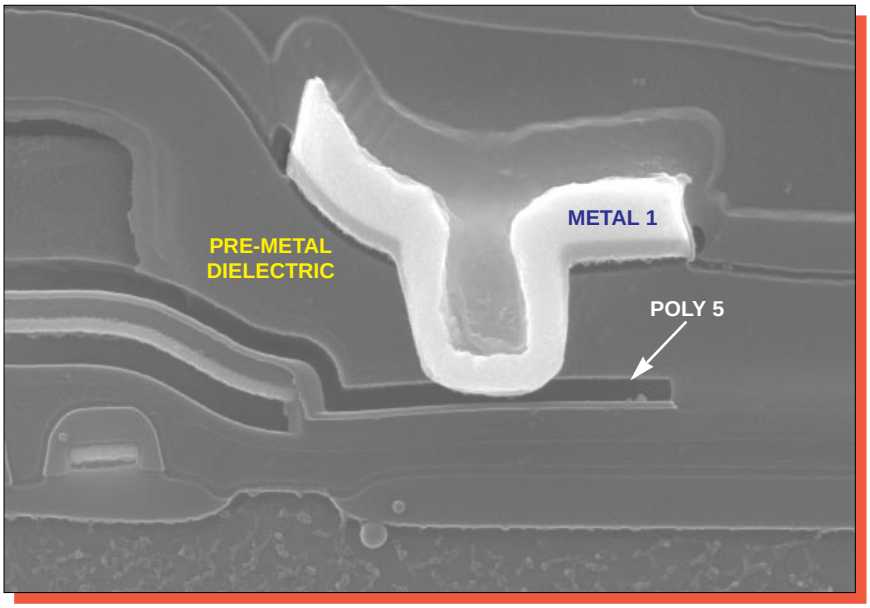


Mag. 15,000x

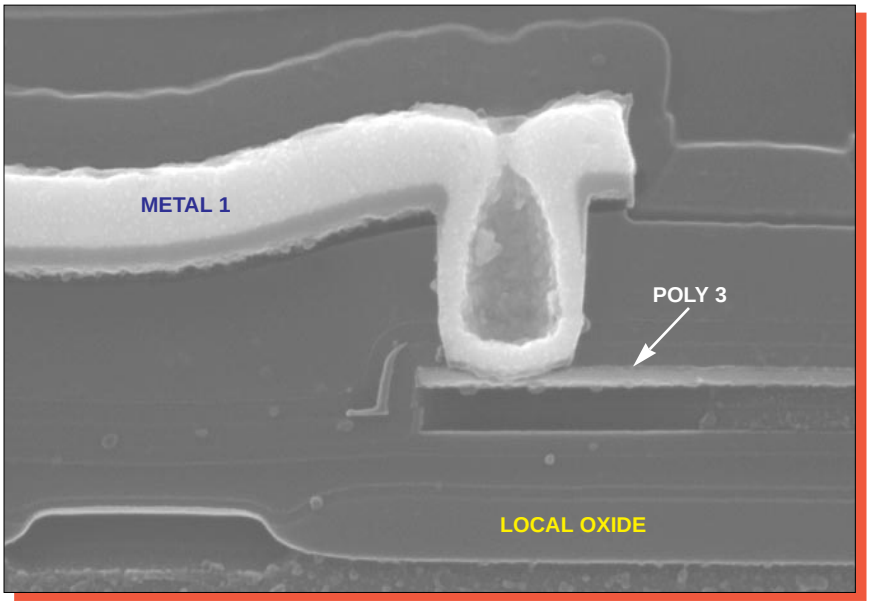


Mag. 34,000x

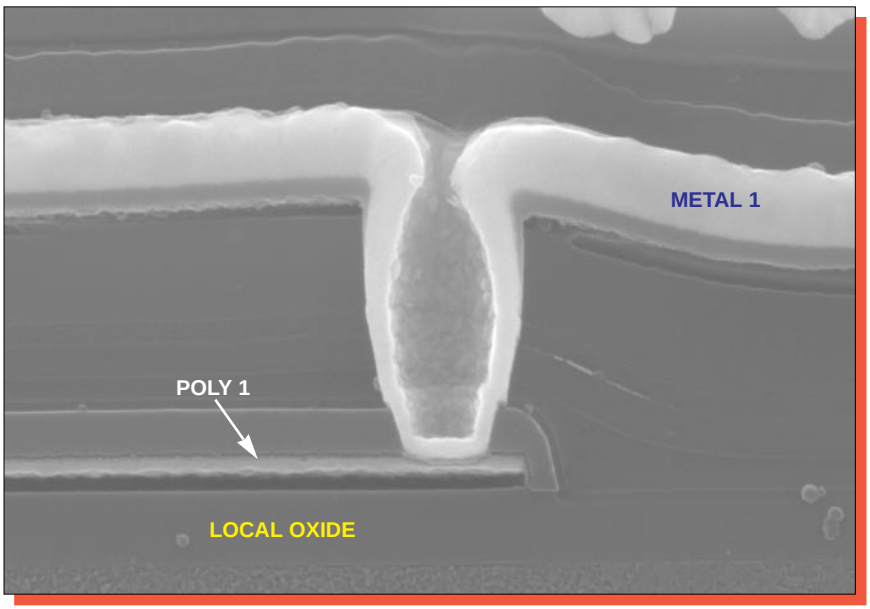
Figure 20. SEM views of general metal 1 integrity. 60°.



metal 1-to-poly 5,
Mag. 26,500x

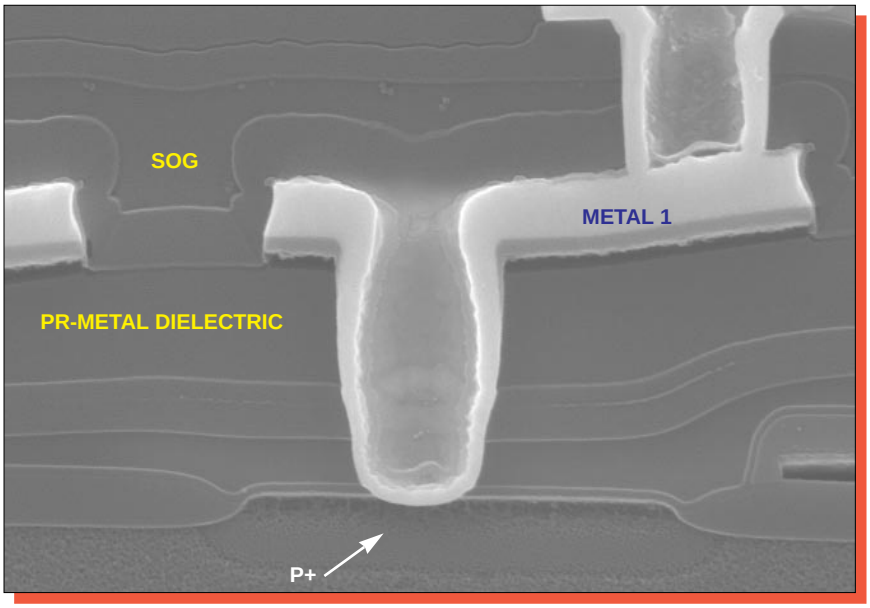


metal 1-to-poly 3,
Mag. 35,000x

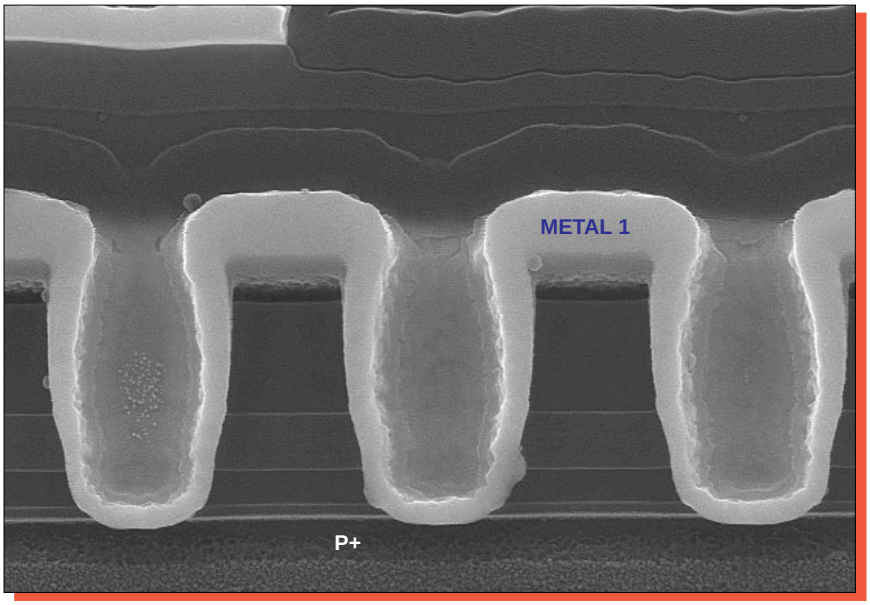


metal 1-to-poly 1,
Mag. 33,000x

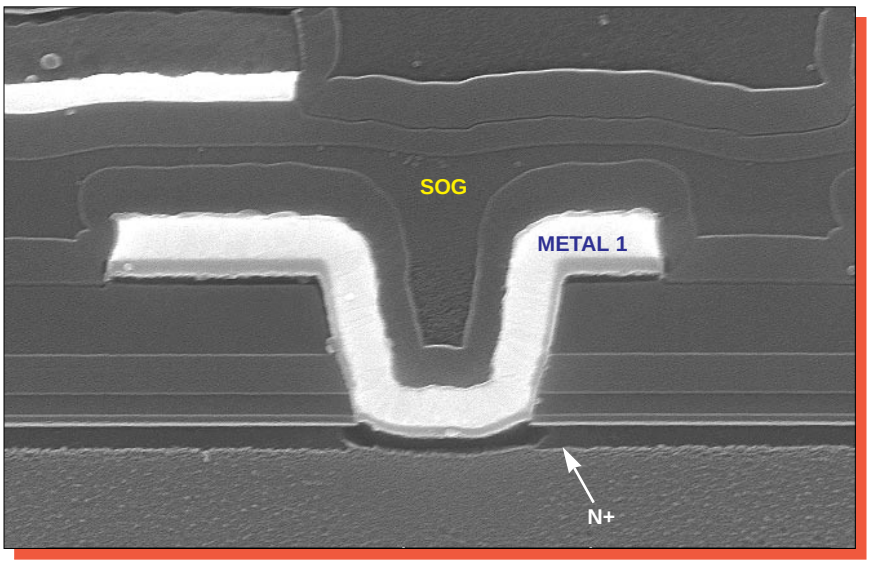
Figure 21. SEM section views of metal 1-to-poly contacts.



metal 1-to-P+,
Mag. 27,500x

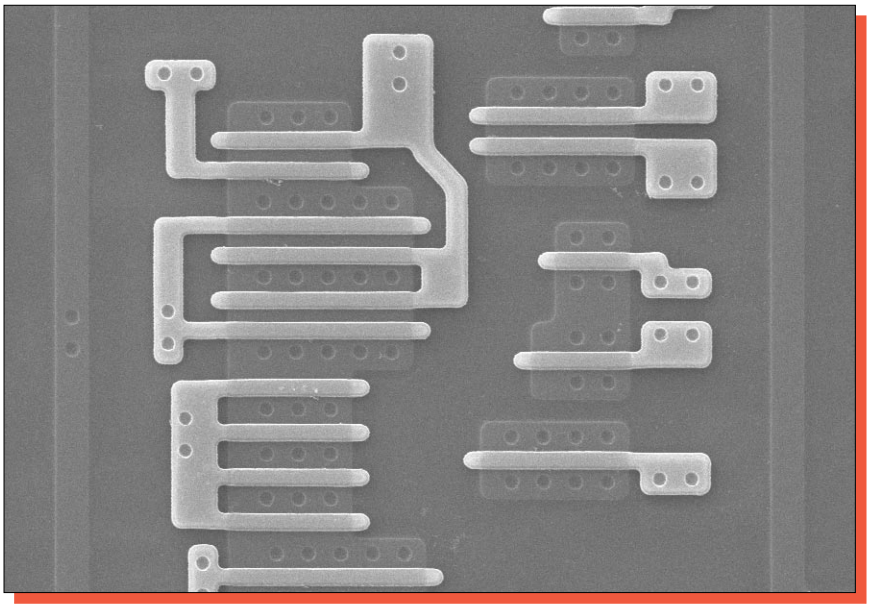


metal 1-to-P+,
Mag. 30,000x

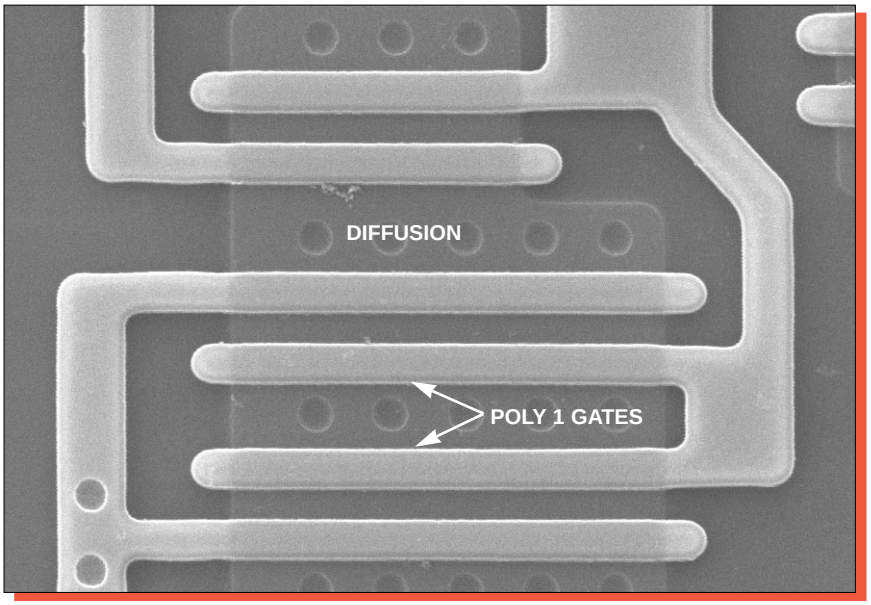


metal 1-to-N+,
Mag. 28,500x

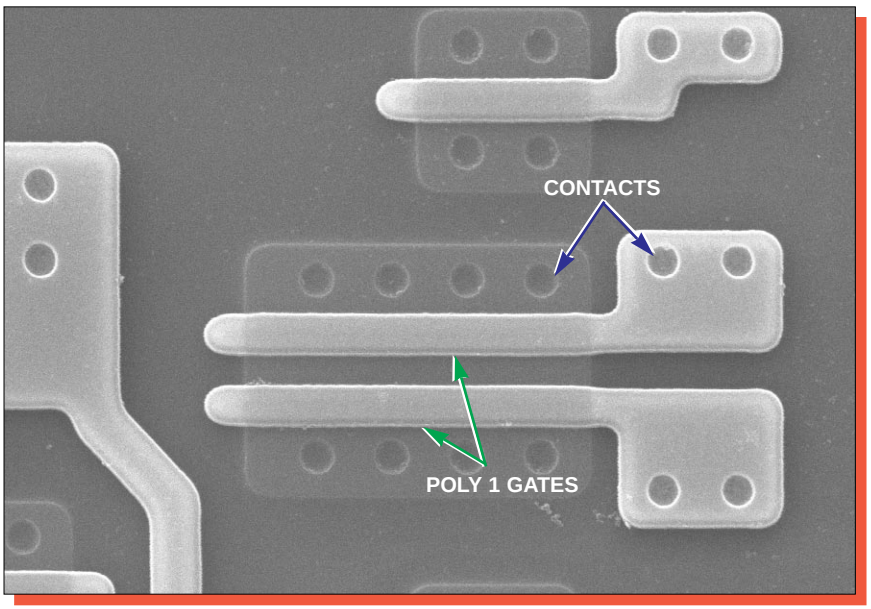
Figure 22. SEM section views of metal 1-to-diffusion contacts.



Mag. 3200x

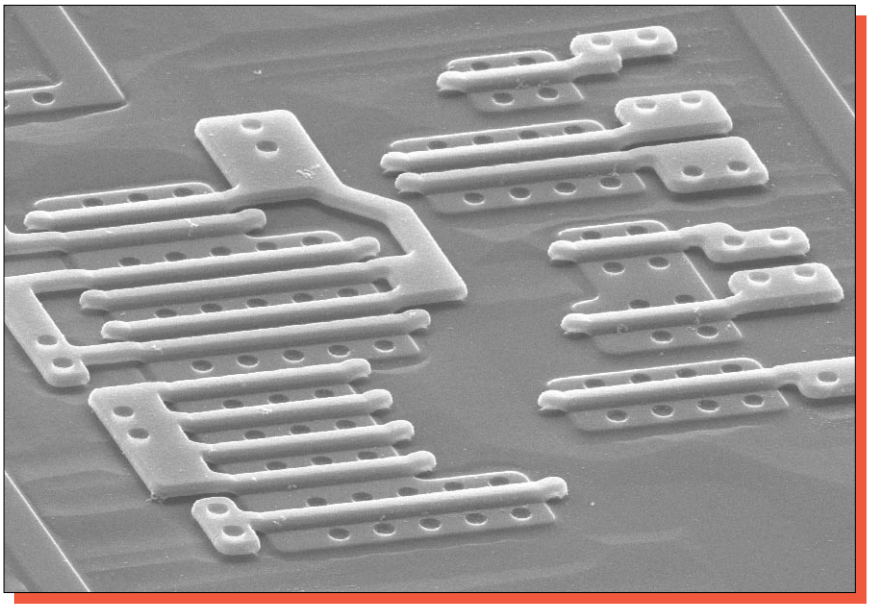


Mag. 8000x

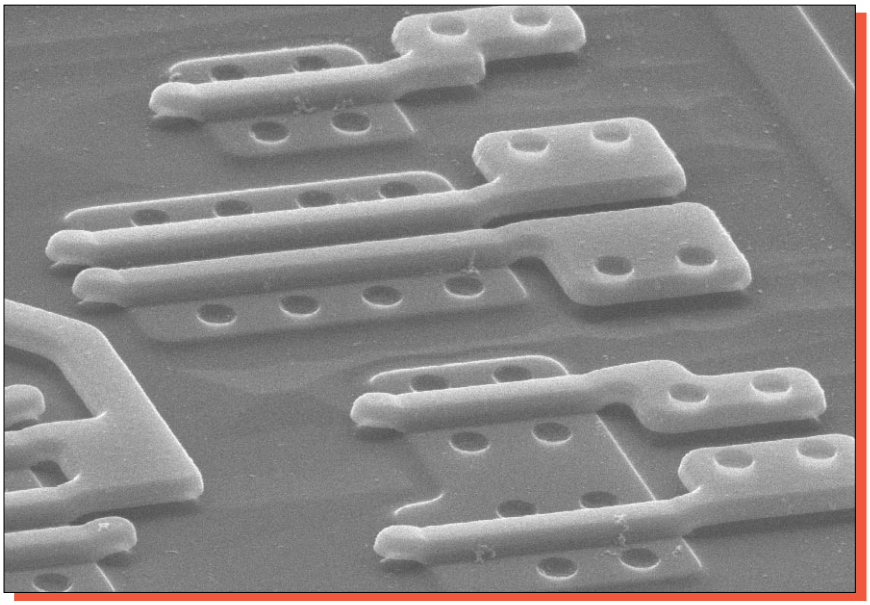


Mag. 8000x

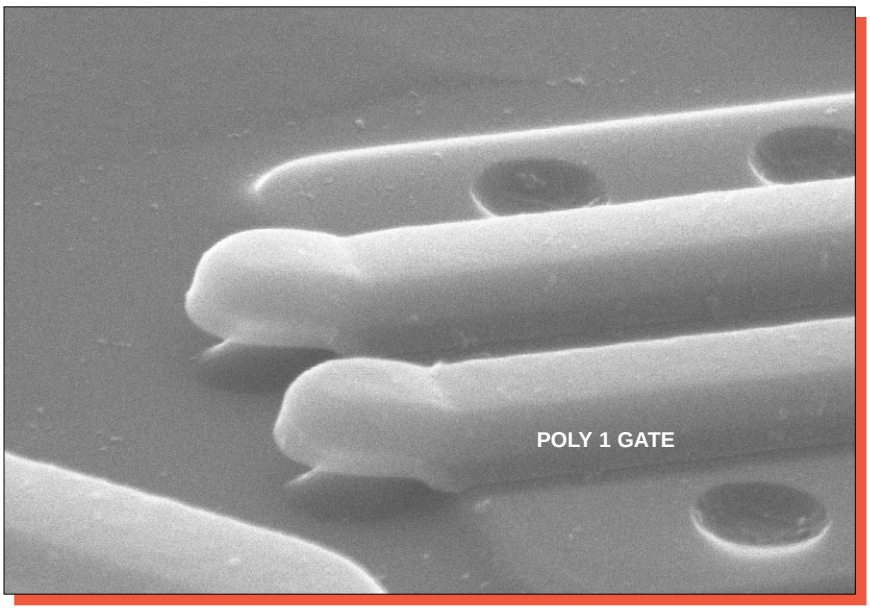
Figure 23. Topological SEM views of poly 1 patterning. 0°.



Mag. 5000x

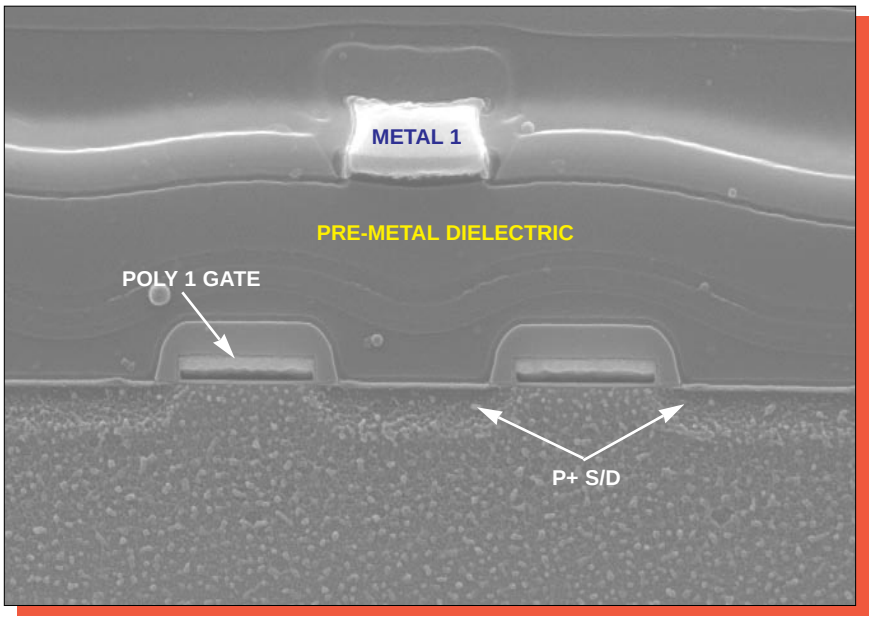


Mag. 9000x

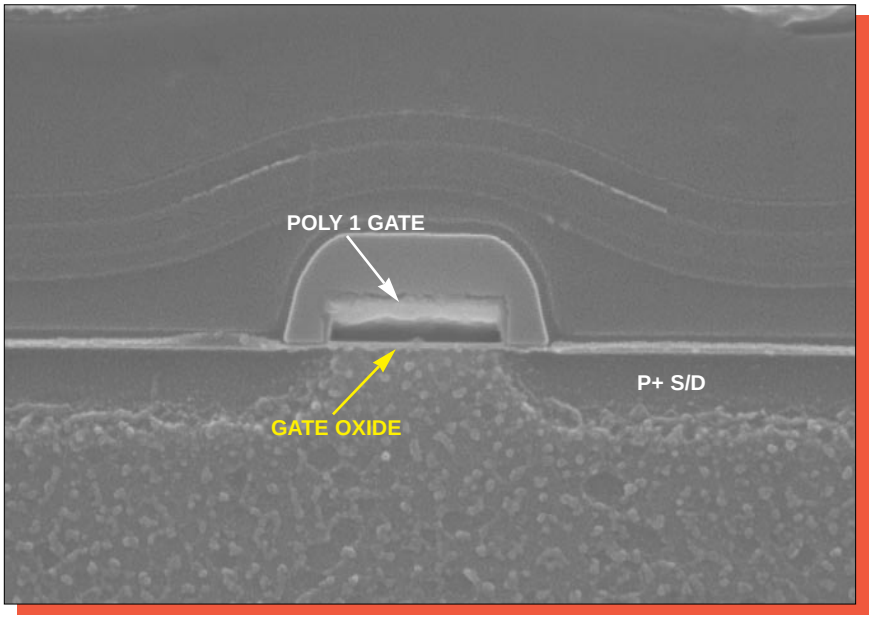


Mag. 30,000x

Figure 24. Perspective SEM views of poly 1 coverage. 60°.

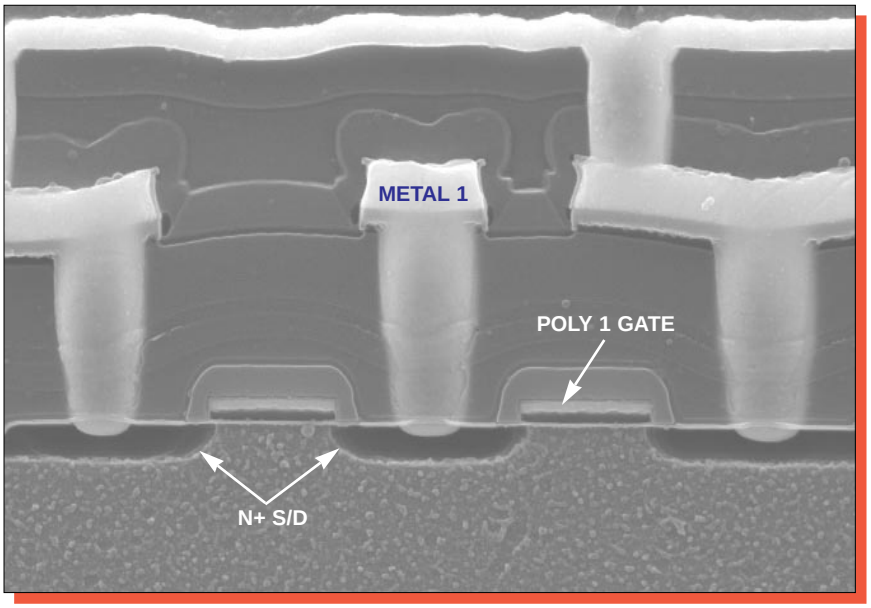


Mag. 24,500x

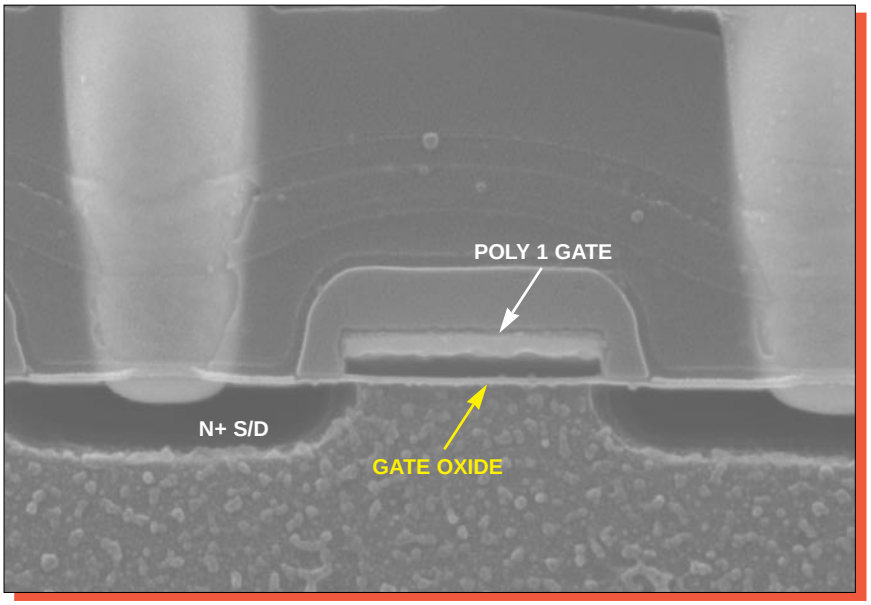


Mag. 45,000x

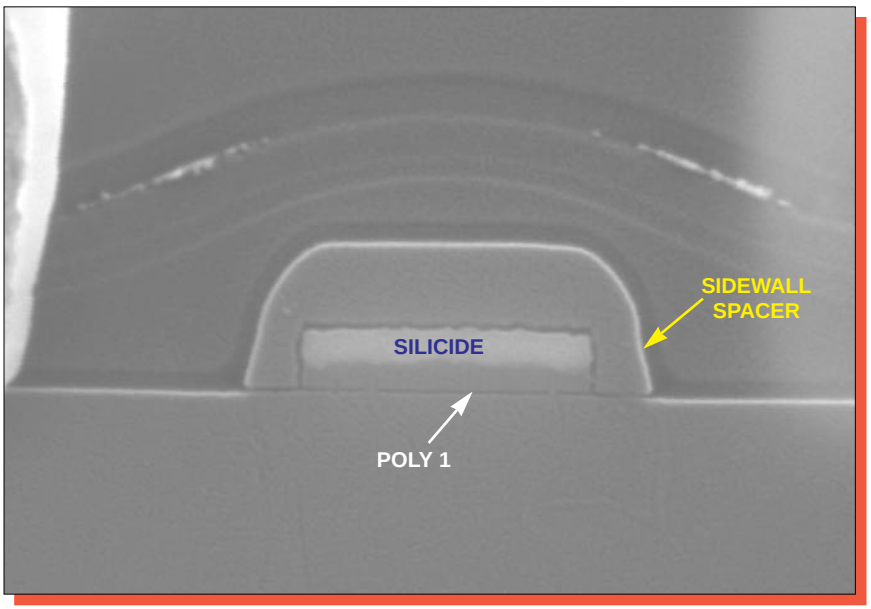
Figure 25. SEM section views of P-channel transistors.



Mag. 22,500x

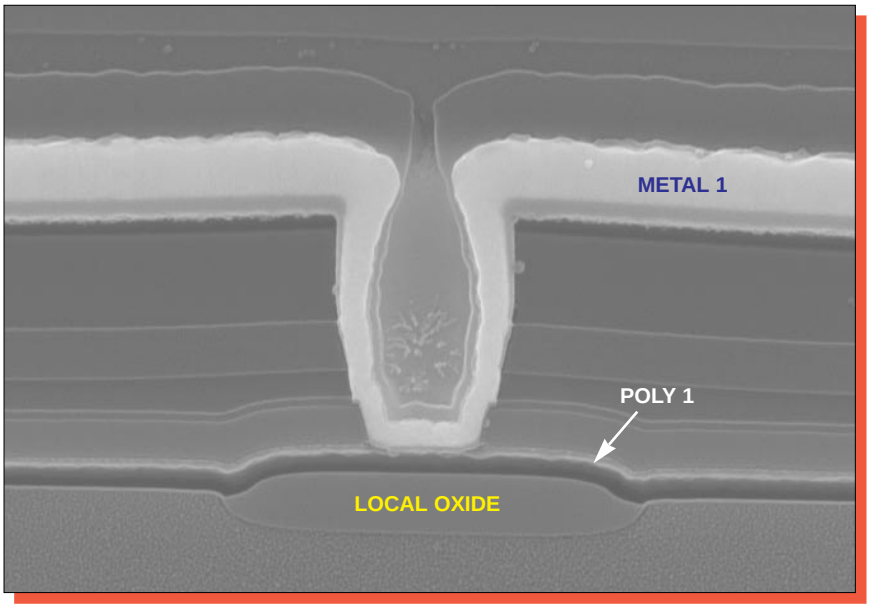


Mag. 45,000x

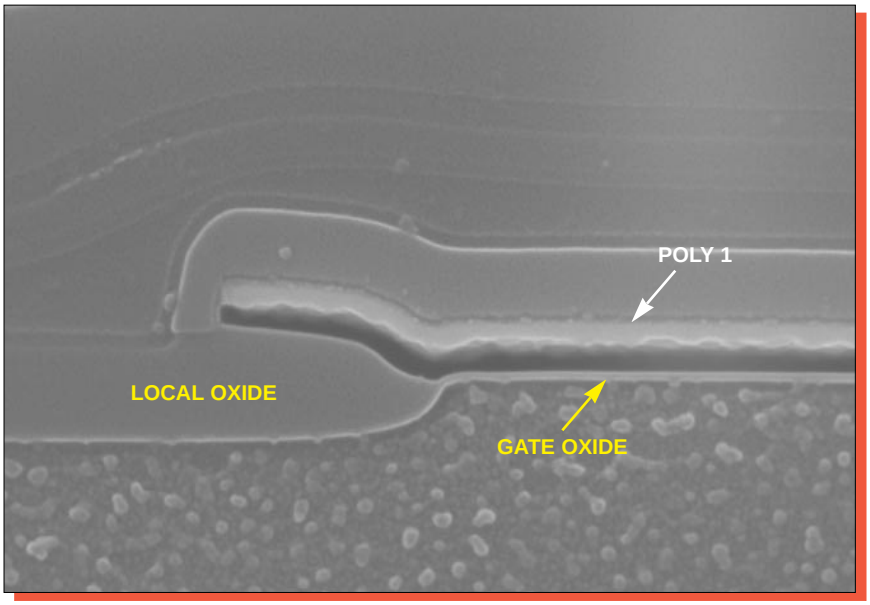


glass etch,
Mag. 60,000x

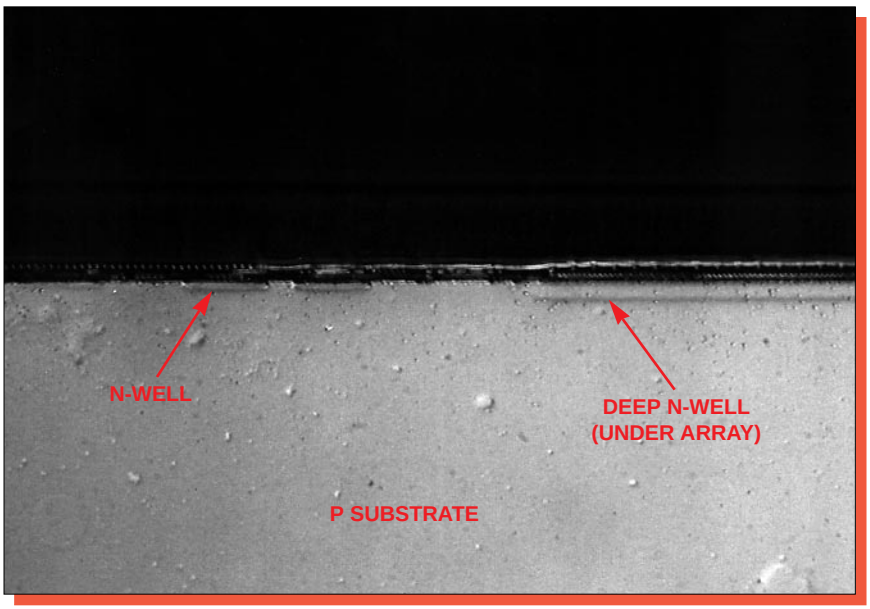
Figure 26. SEM section views of N-channel transistors.



Mag. 27,500x

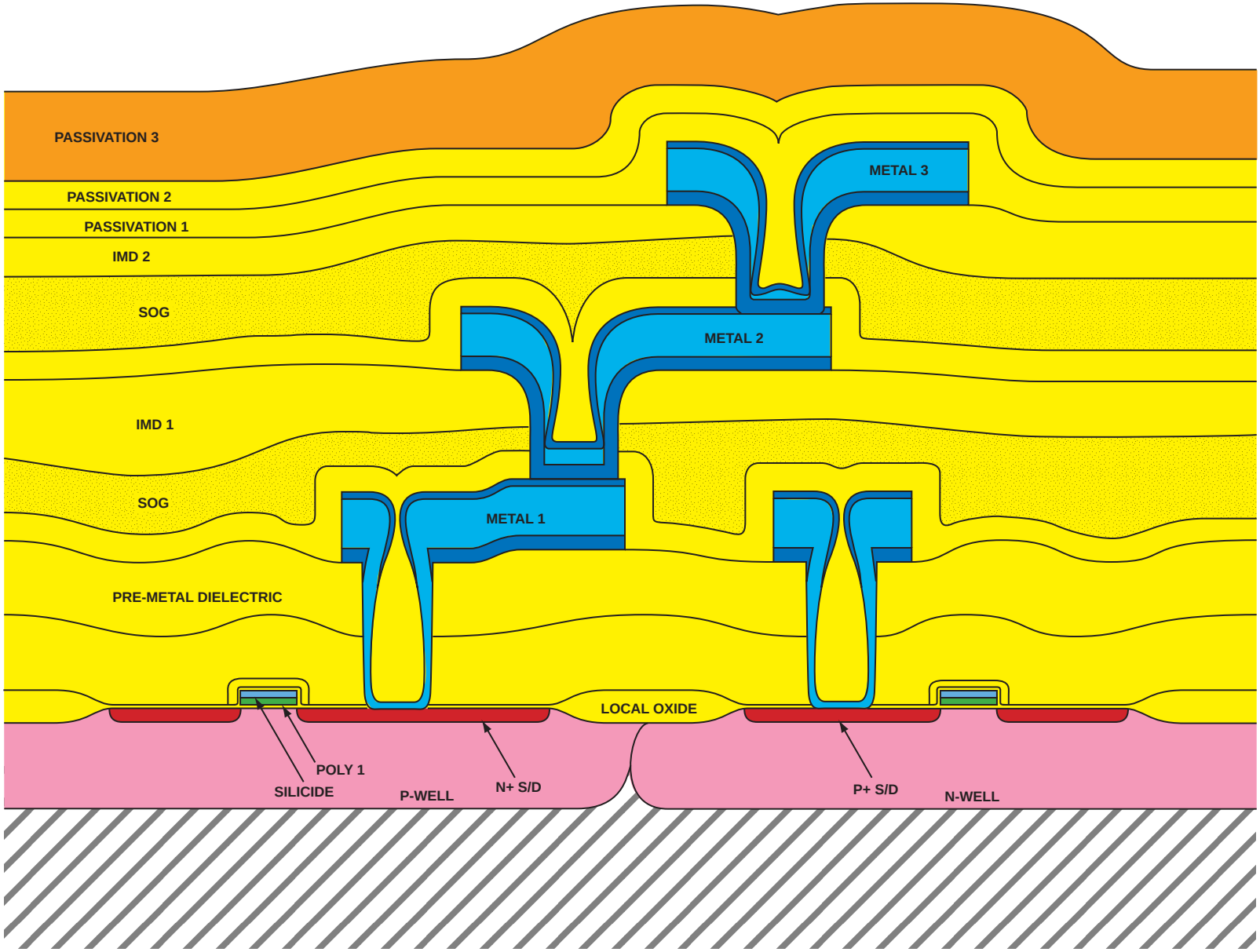


Mag. 50,000x



Mag. 800x

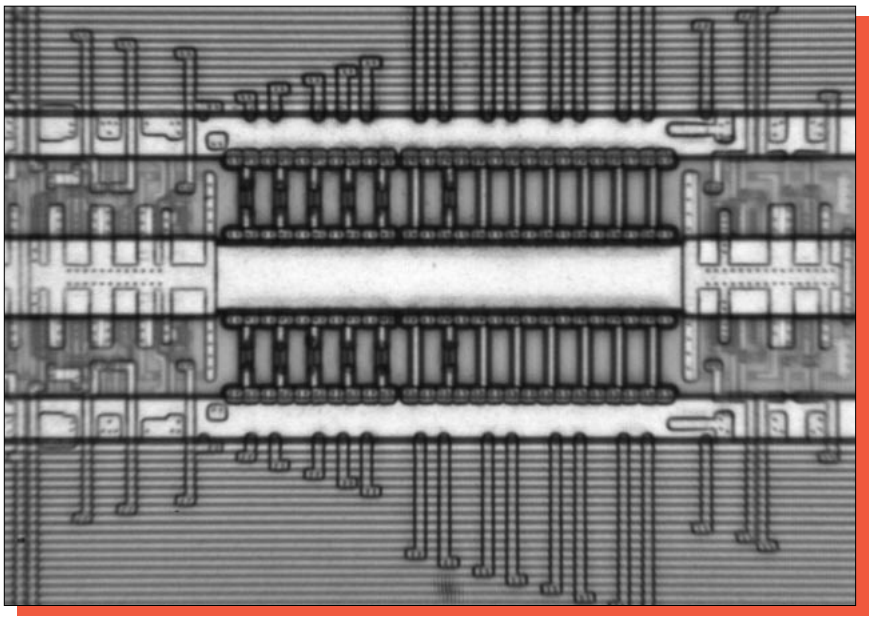
Figure 27. Section views illustrating birdsbeak profiles and well structure.



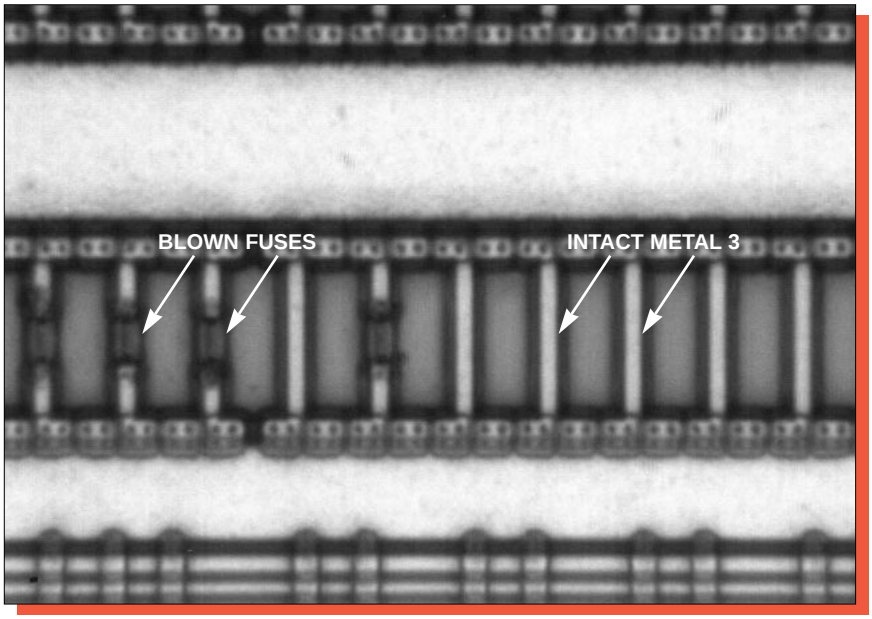
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 28. Color cross section drawing illustrating device structure.

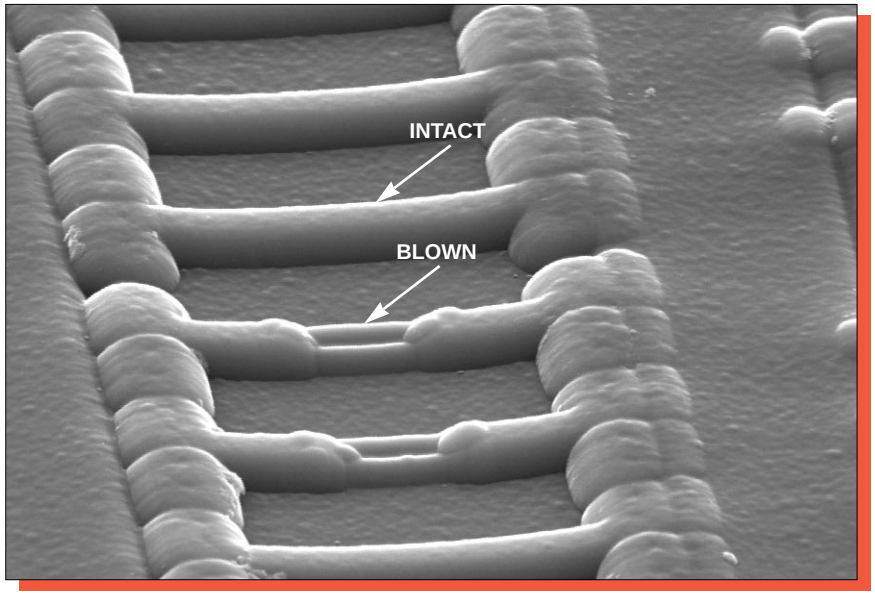


Mag. 620x

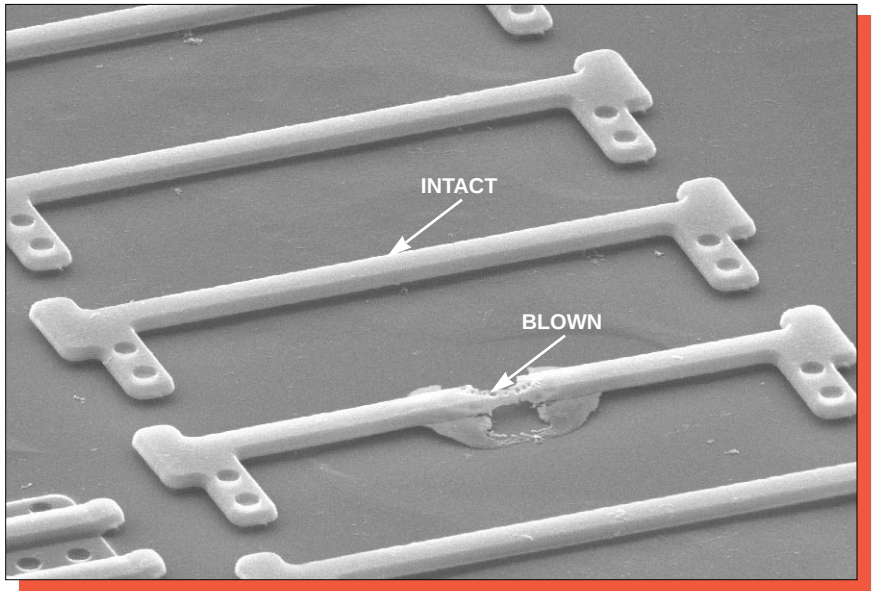


Mag. 1535x

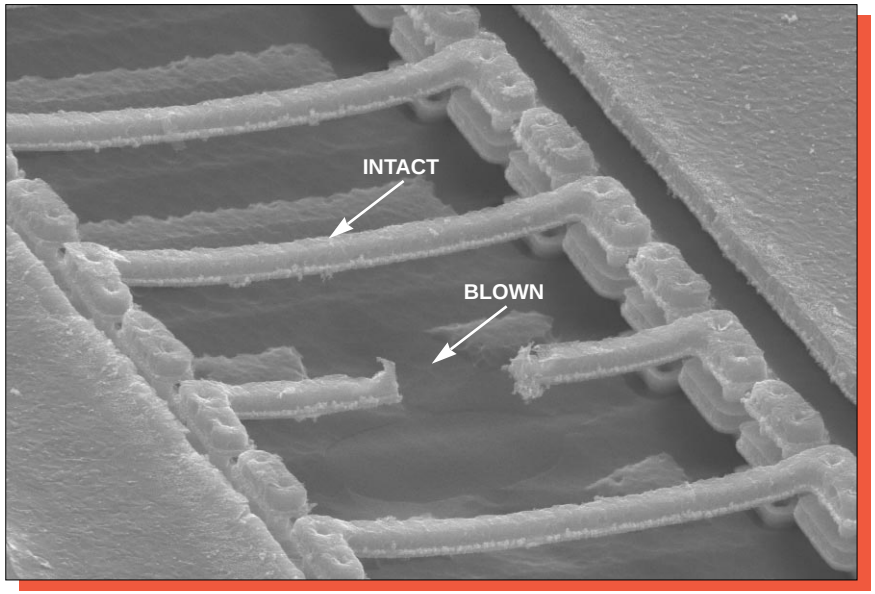
Figure 29. Optical views of fuse blocks.



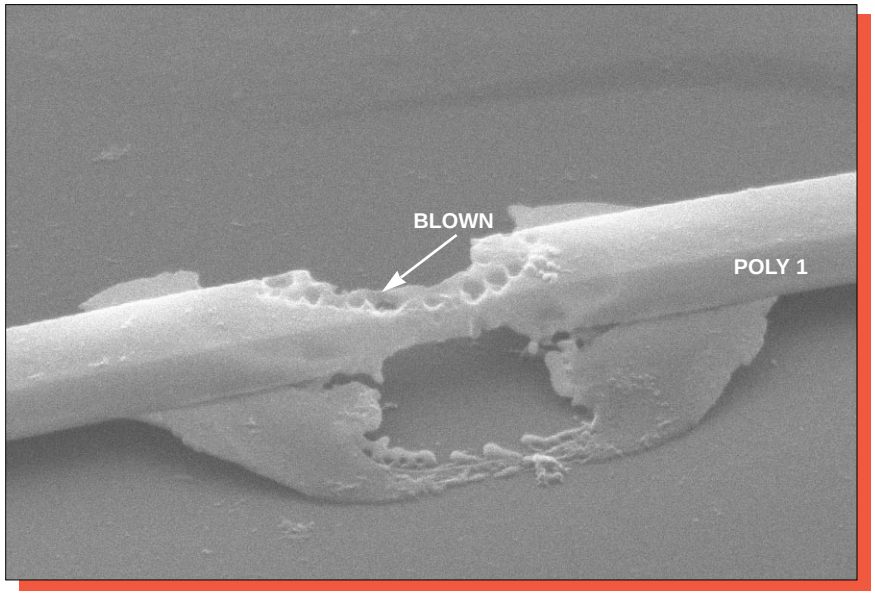
intact, Mag. 4000x



poly 1, Mag. 5500x

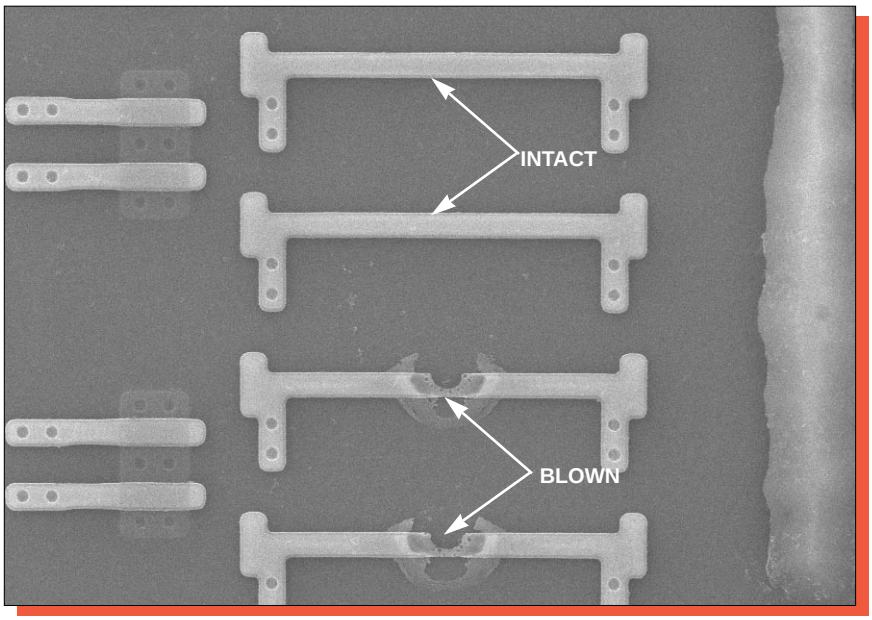


metal 3, Mag. 5500x

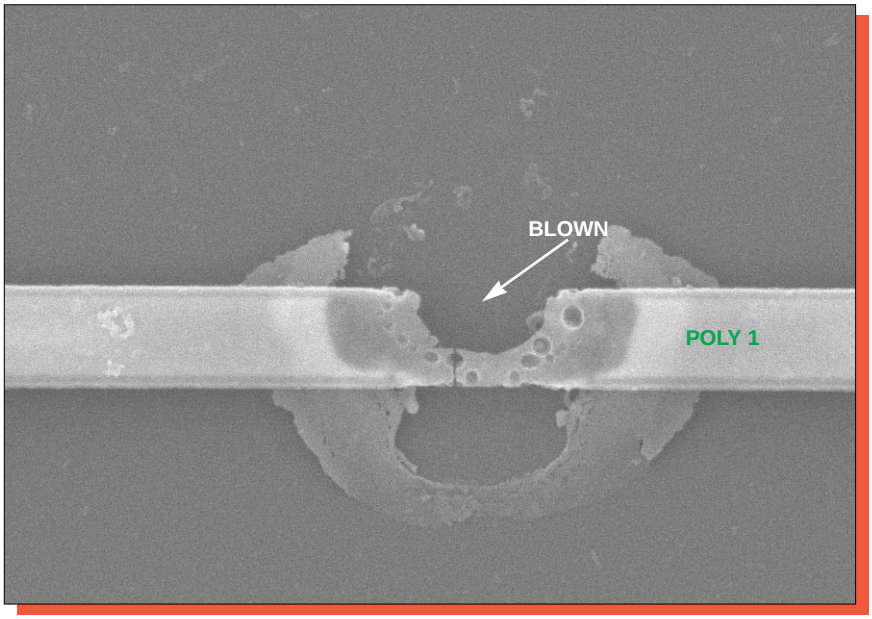


poly 1, Mag. 20,000x

Figure 30. Perspective SEM views of fuses. 60°.

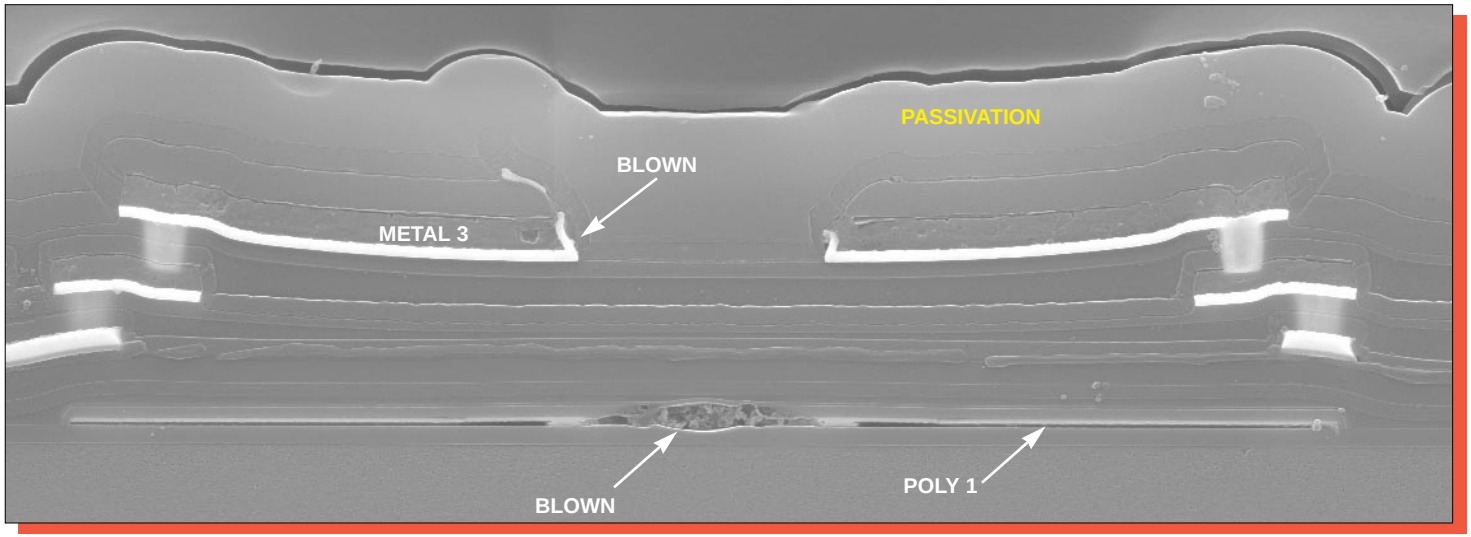


Mag. 3000x

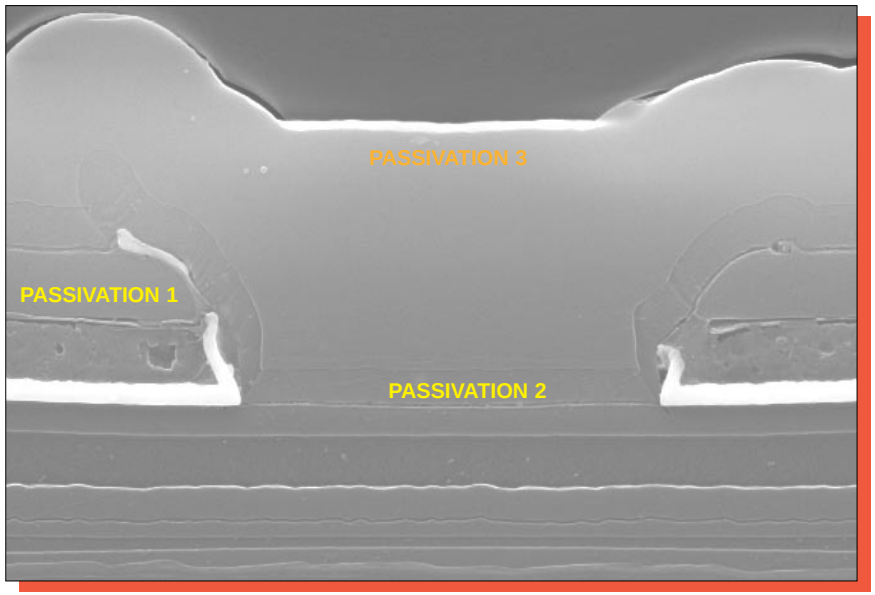


Mag. 12,000x

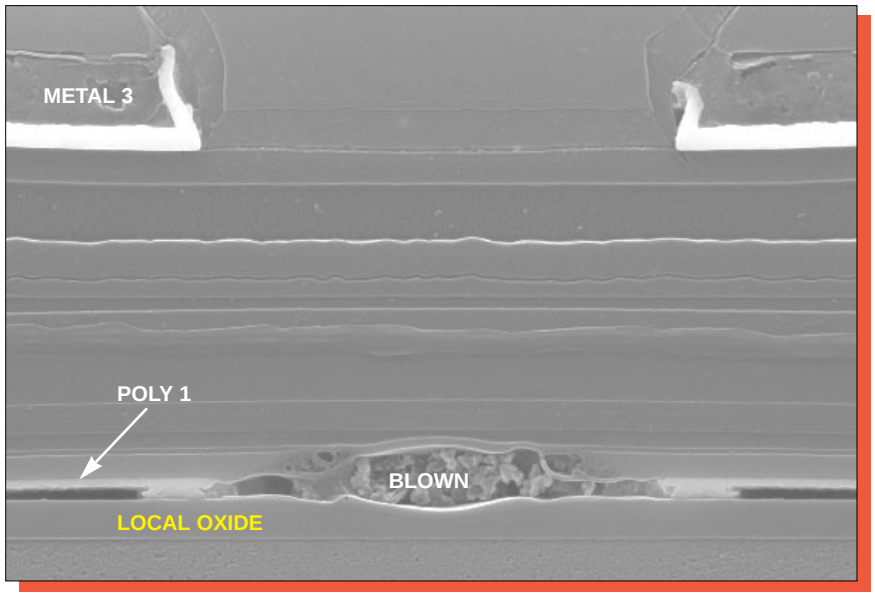
Figure 31. Topological SEM views of fuses (poly 1). 0°.



Mag. 9000x

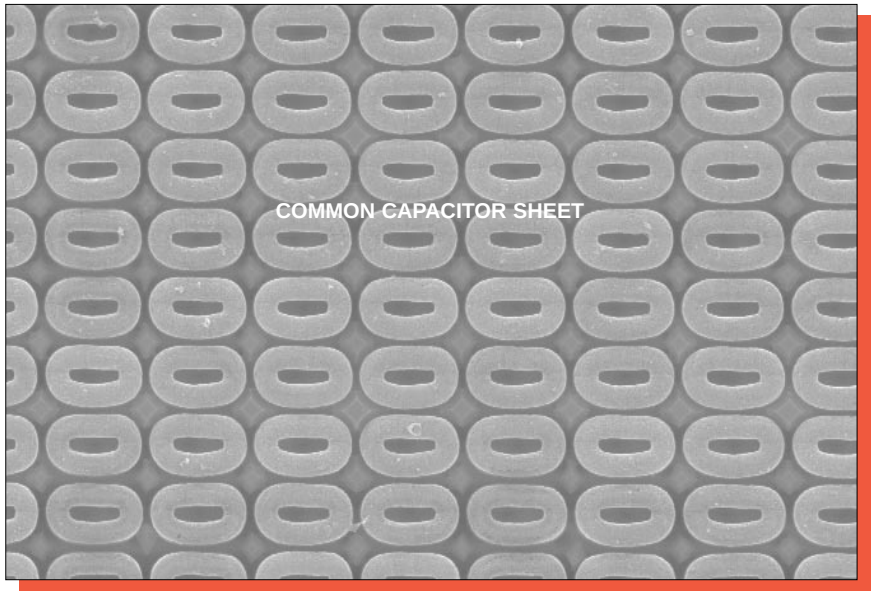


Mag. 15,000x

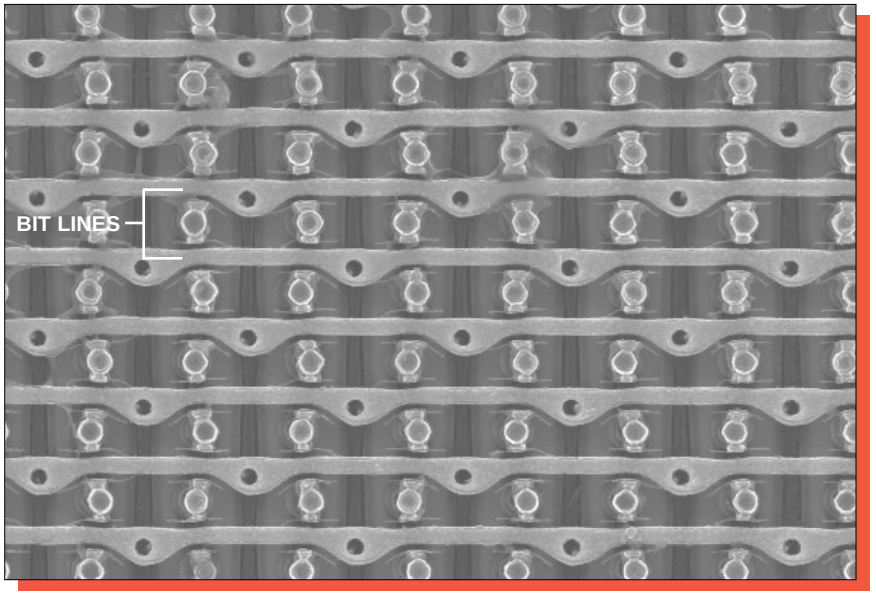


Mag. 17,000x

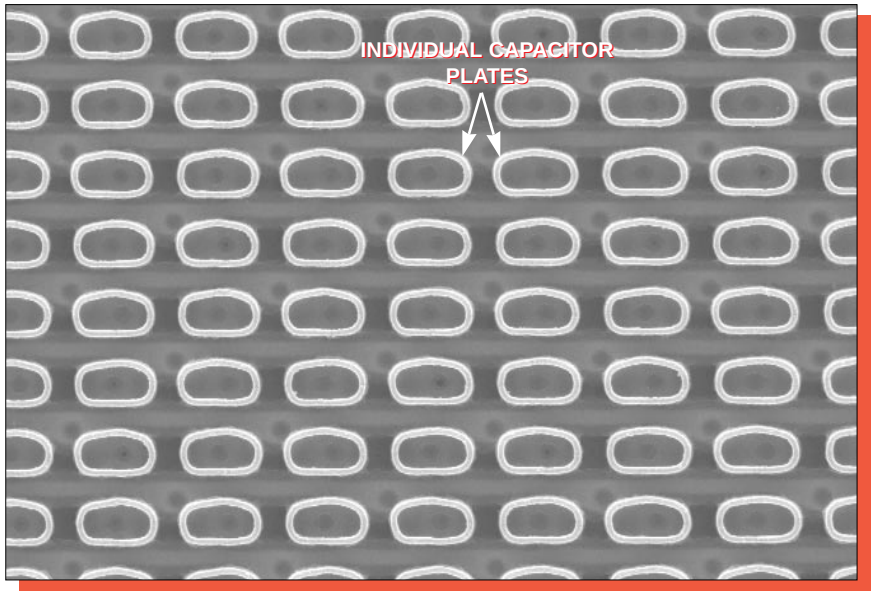
Figure 32. SEM section views of a fuse.



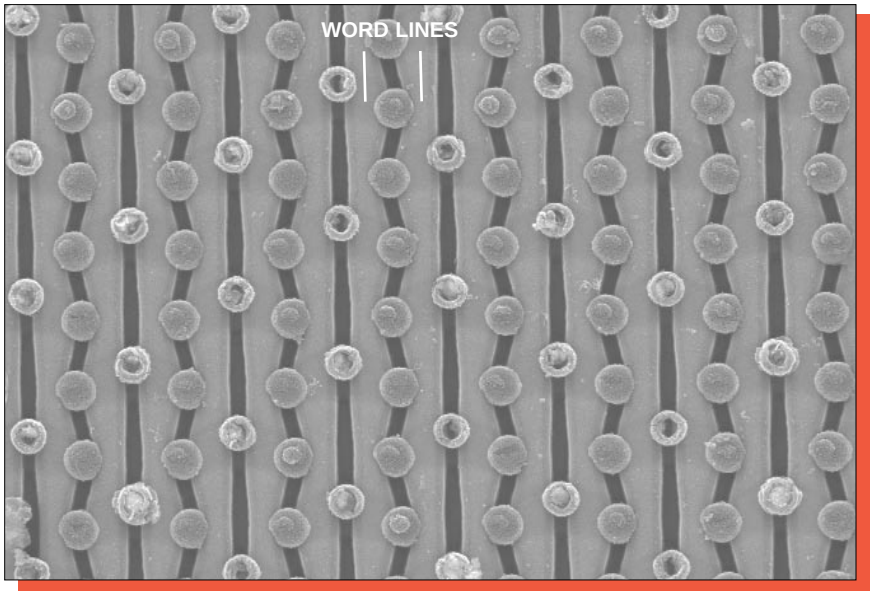
poly 5



poly 3

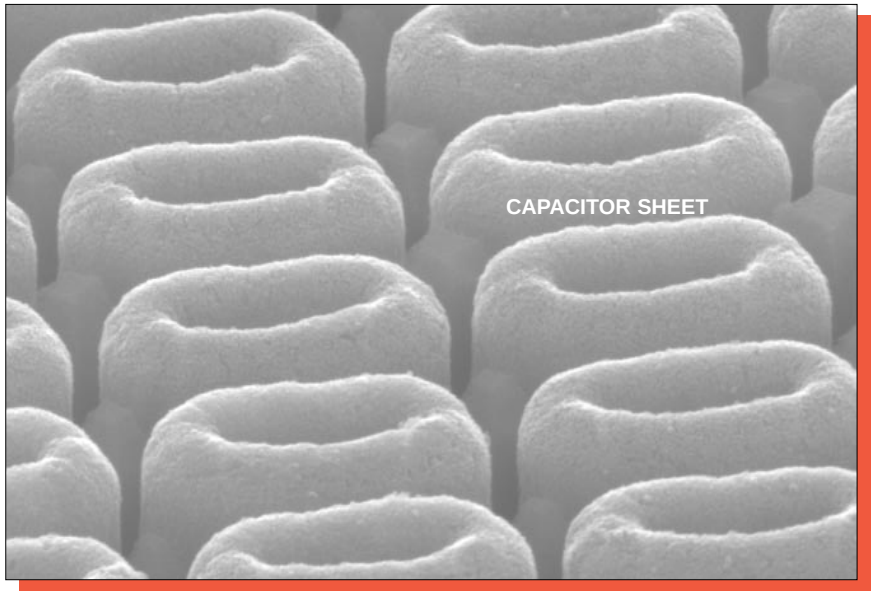


poly 4

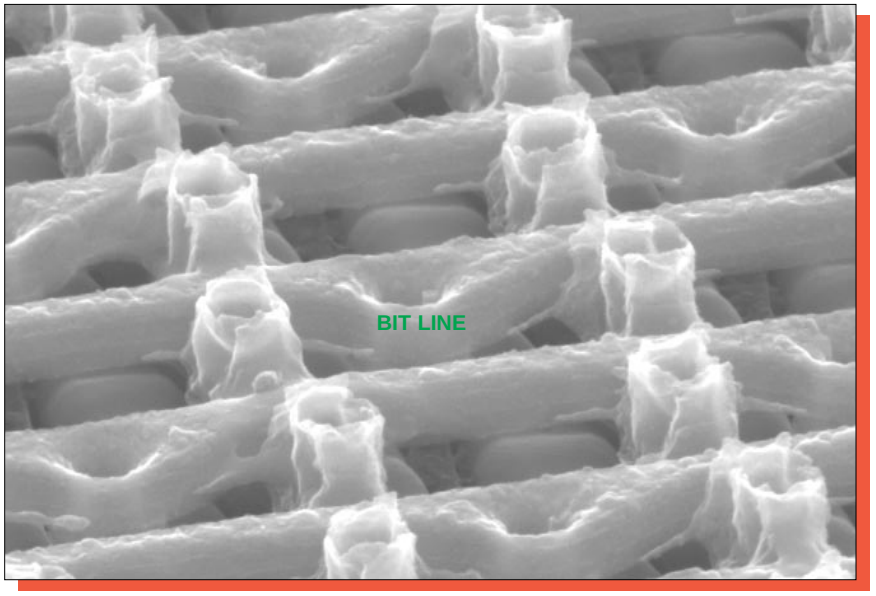


poly 1

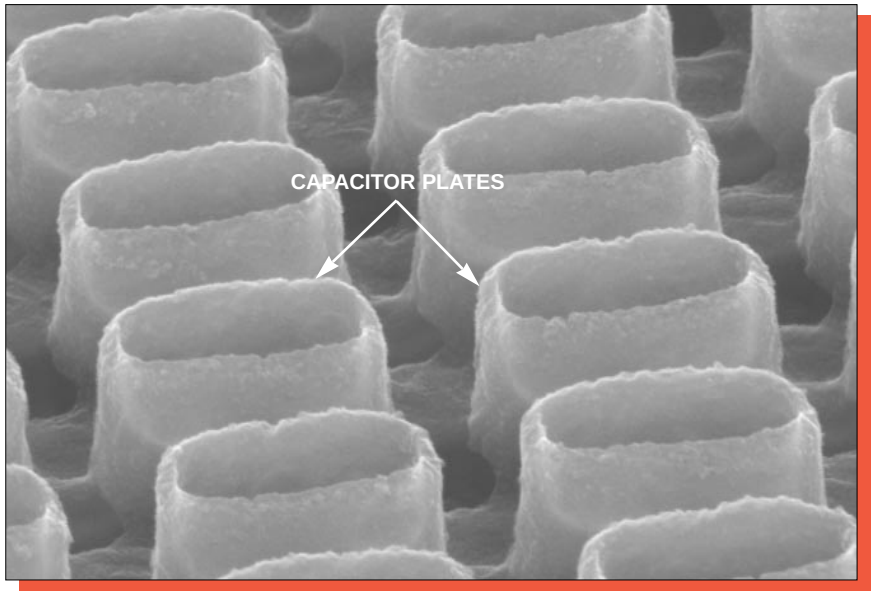
Figure 33. Topological SEM views of the DRAM array, Mag. 10,000x, 0°.



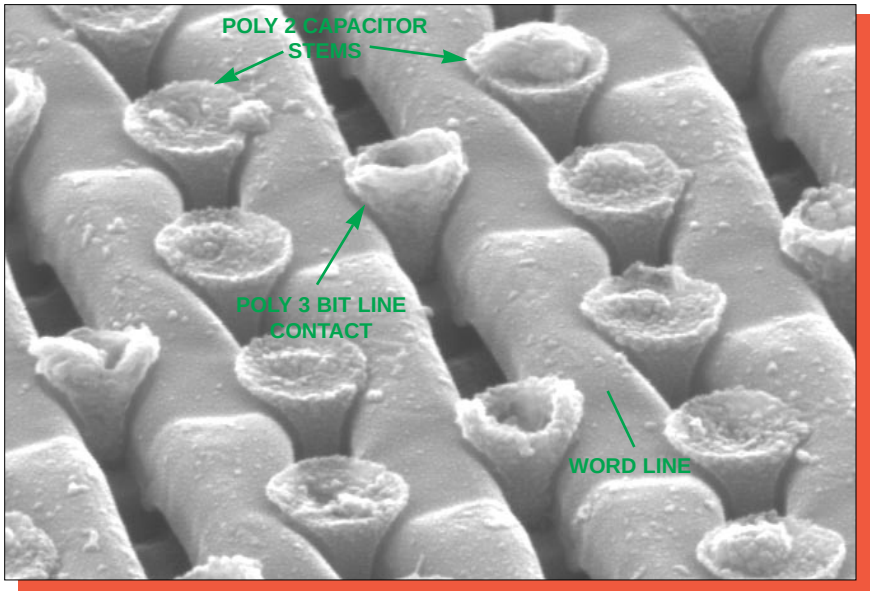
poly 5



poly 3

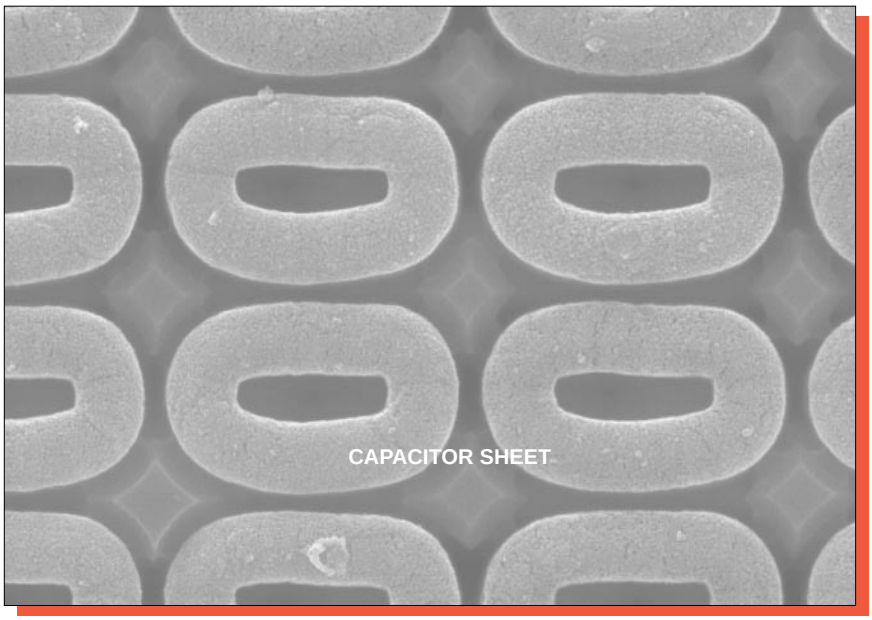


poly 4

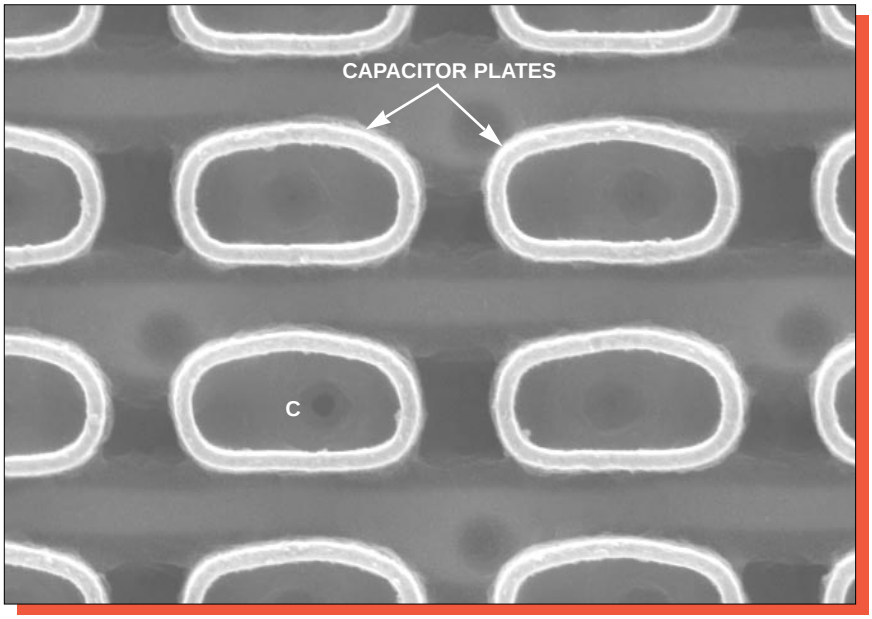


poly 1

Figure 34. Perspective SEM details of DRAM cells. Mag. 36,000x, 60°.

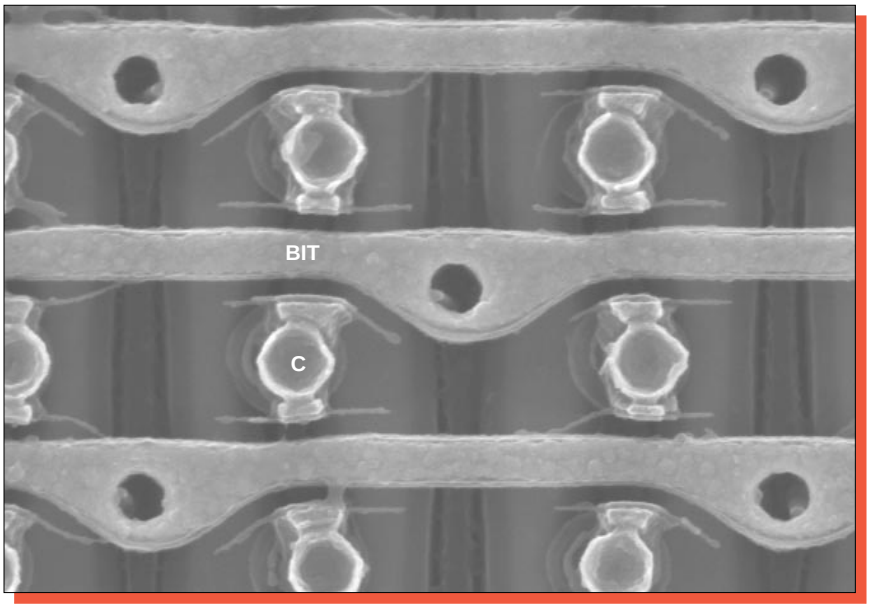


poly 5

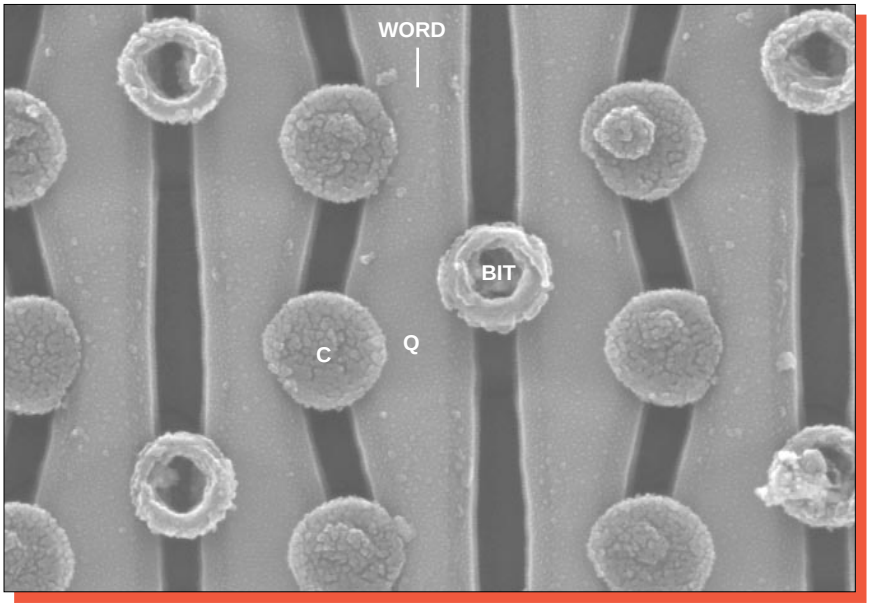


poly 4

Figure 35. Topological SEM views of DRAM cells. Mag. 30,000x, 0°.



poly 3



poly 1

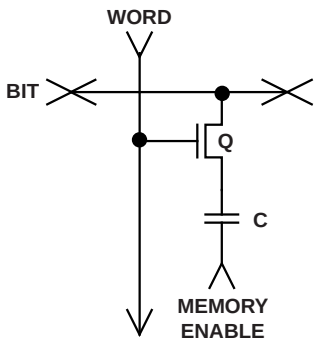
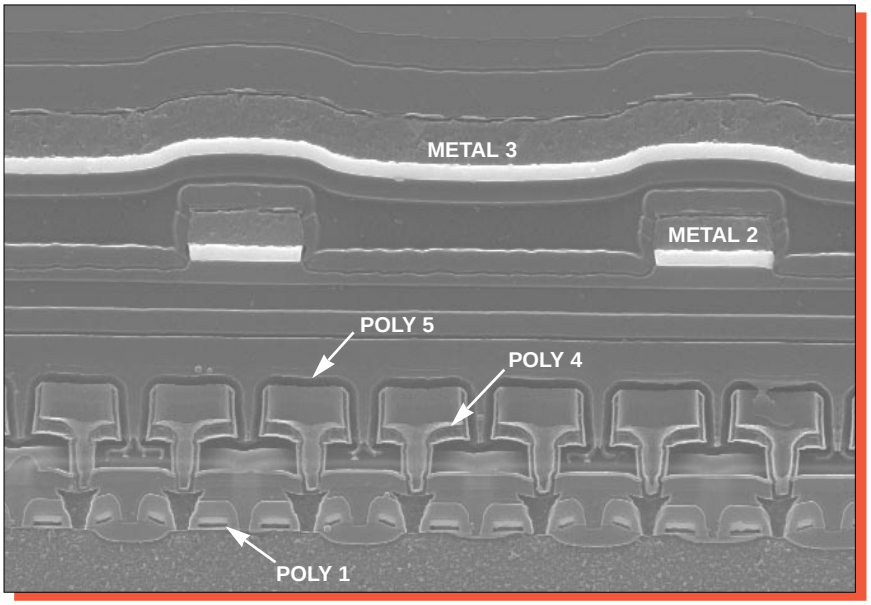
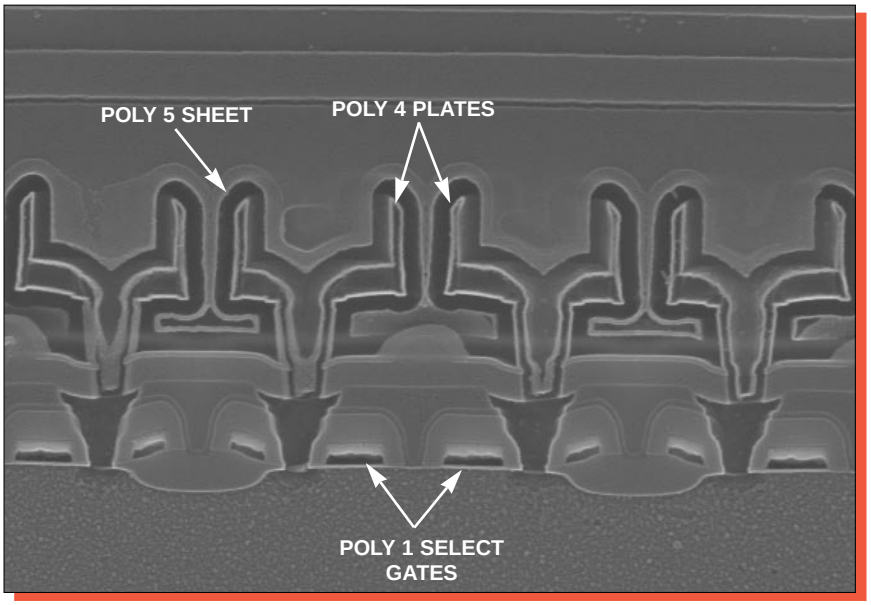


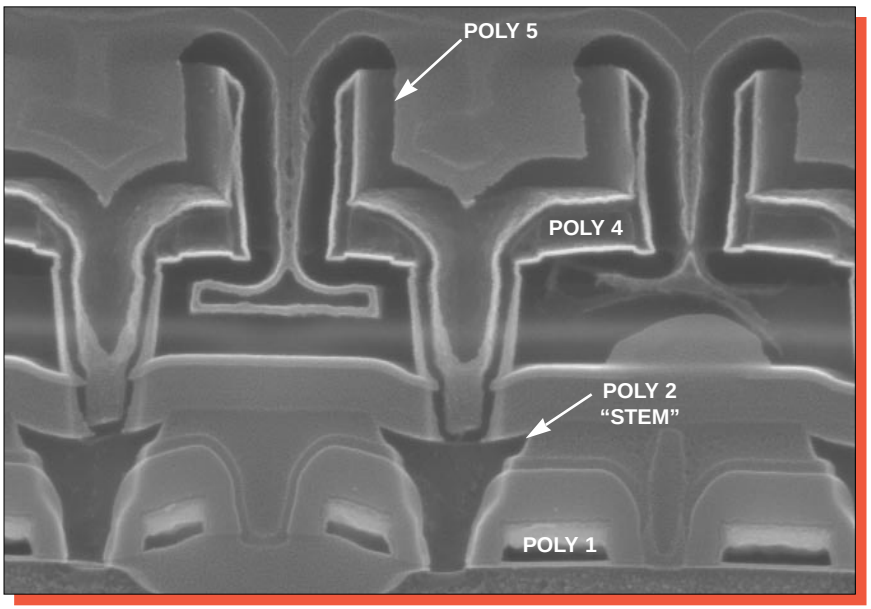
Figure 35a. Topological SEM views of DRAM cells and schematic. Mag. 30,000x, 0°.



Mag. 11,000x

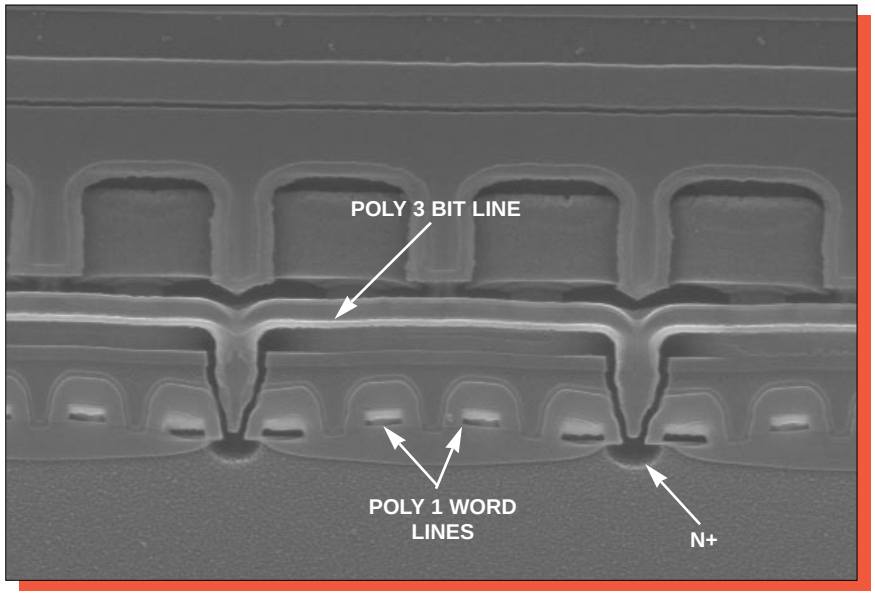


Mag. 20,000x

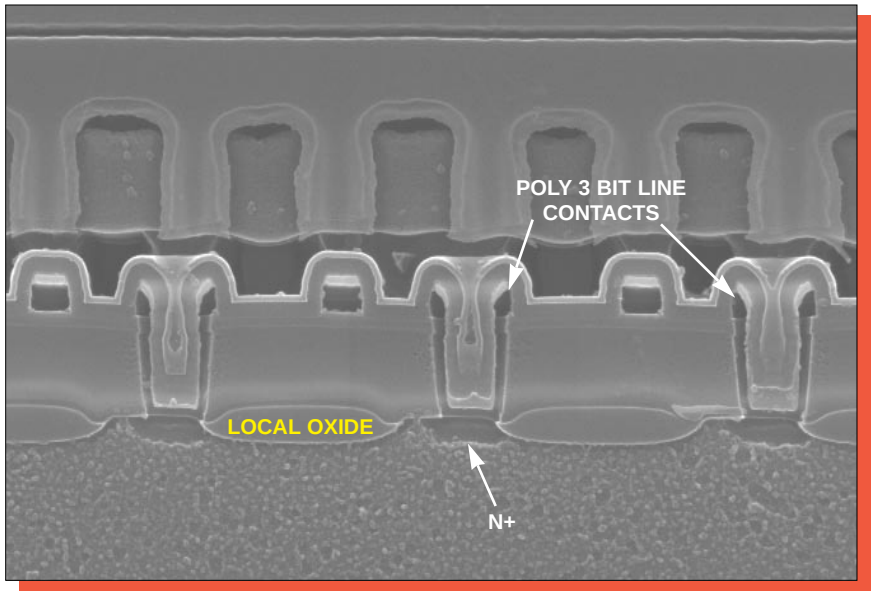


Mag. 38,000x

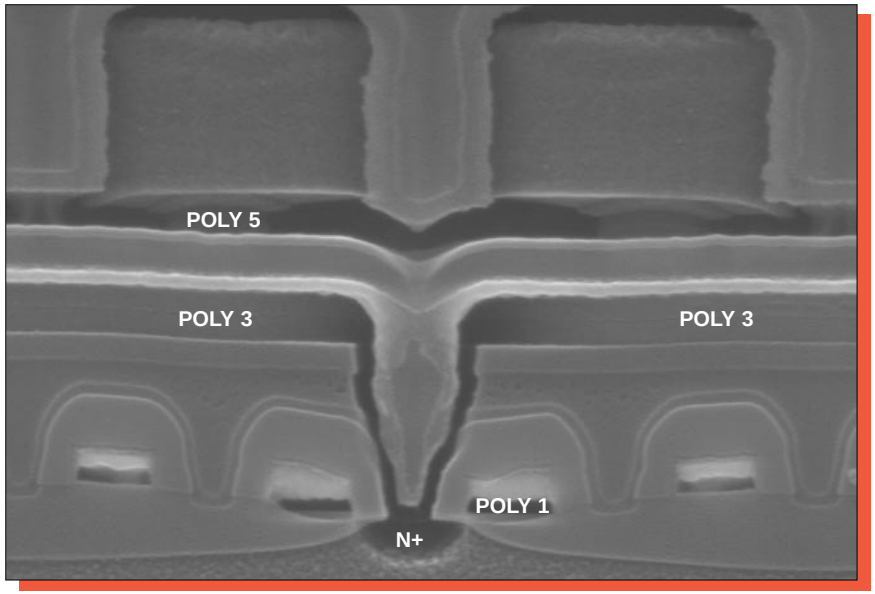
Figure 36. SEM section views of DRAM cells (parallel to bit line).



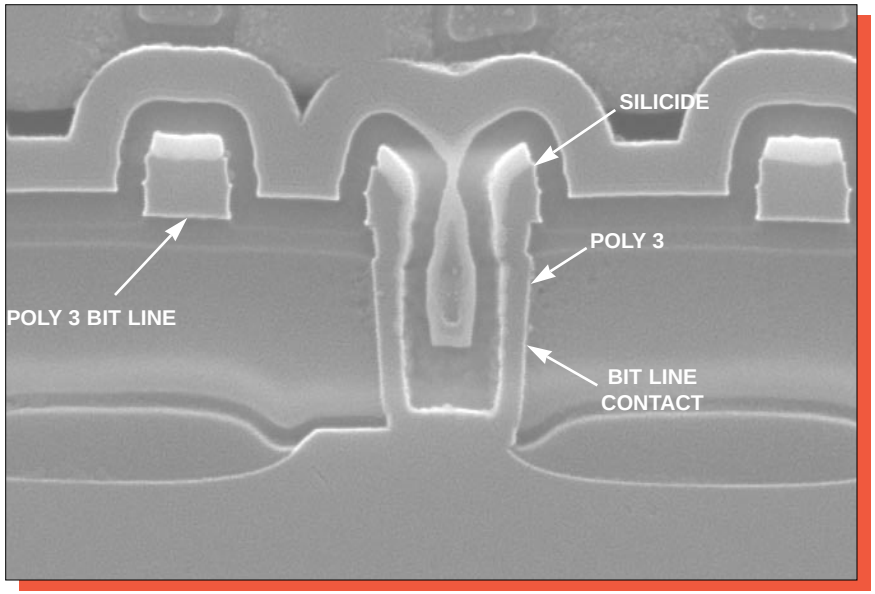
parallel, Mag. 19,000x



perpendicular, Mag. 22,000x

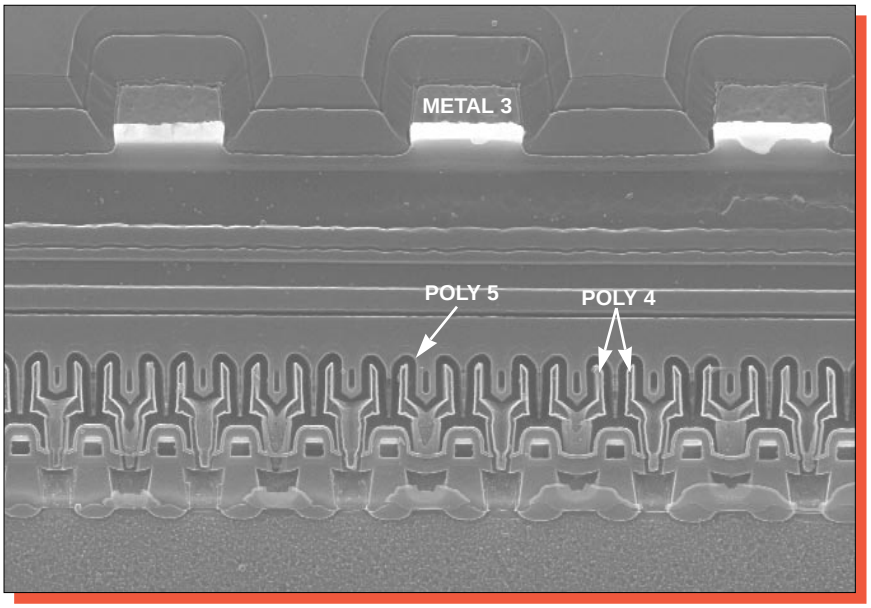


parallel, Mag. 38,000x

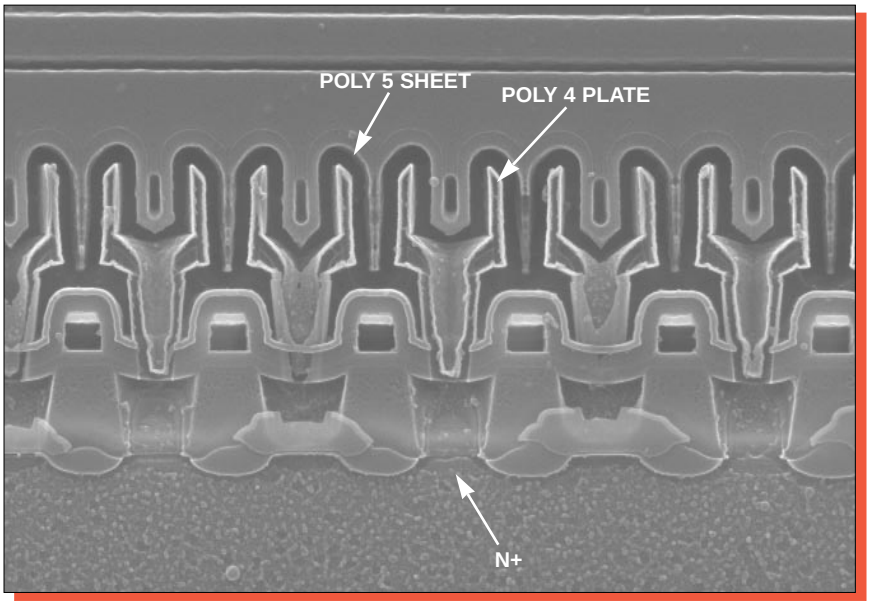


perpendicular, glass etch,
Mag. 45,000x

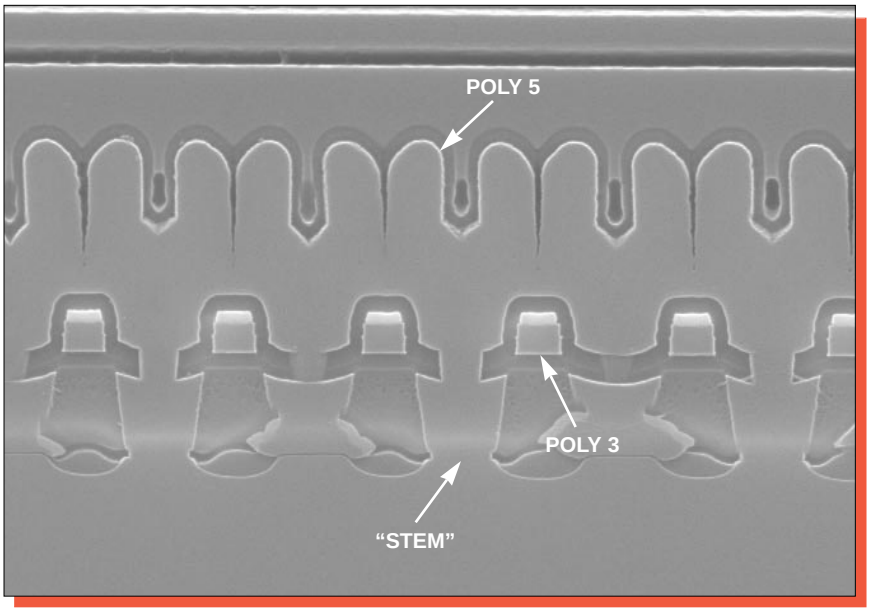
Figure 37. SEM section views of poly 2 bit lines.



Mag. 11,000x

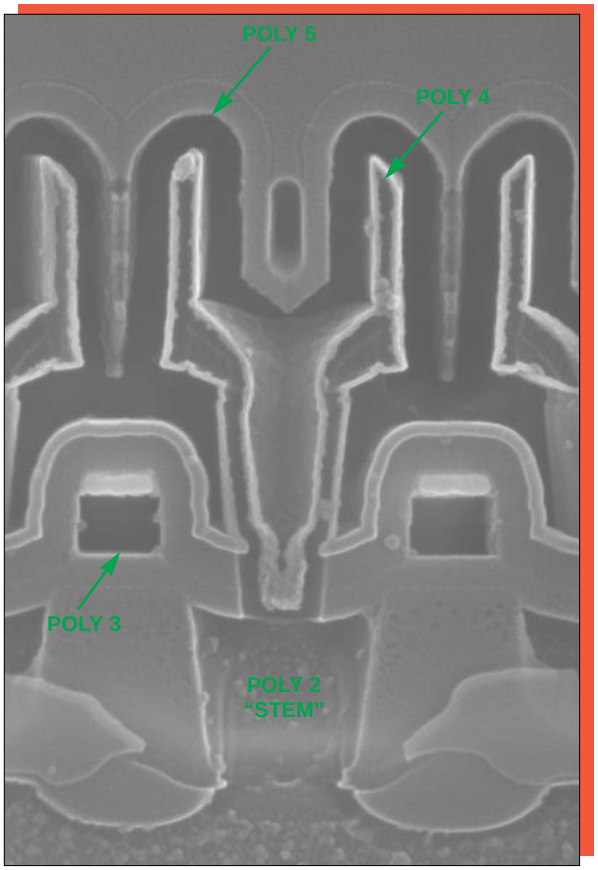


Mag. 22,000x

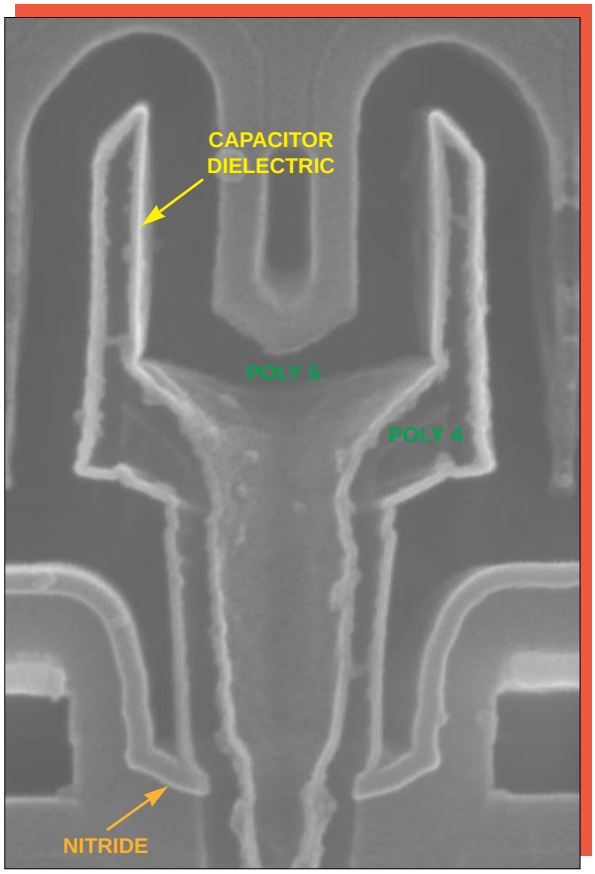


glass etch,
Mag. 22,500x

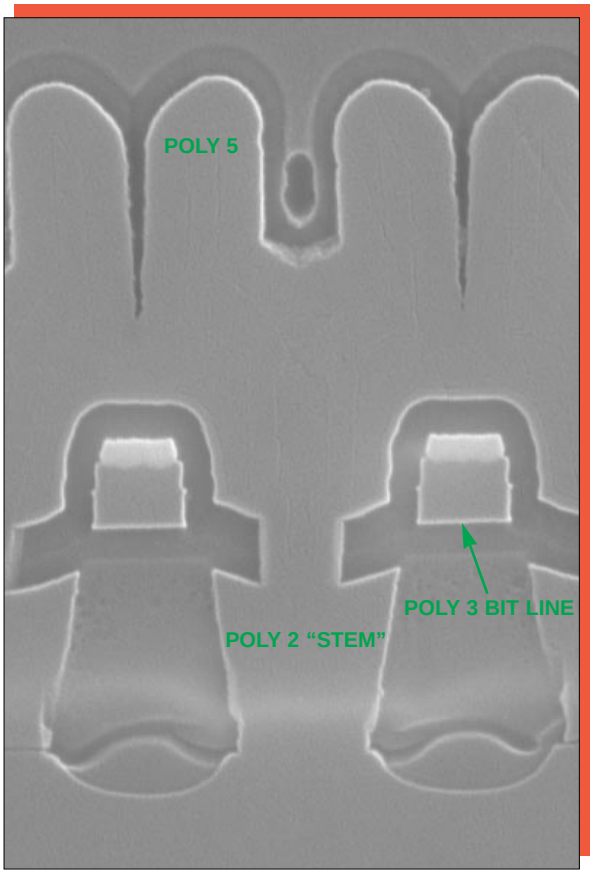
Figure 38. SEM section views of DRAM cells (perpendicular to bit lines).



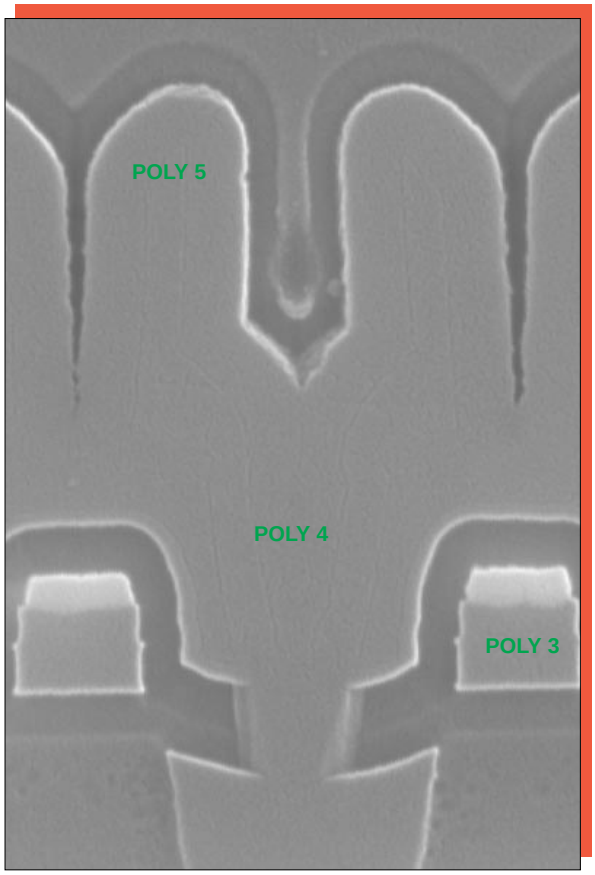
Mag. 48,000x



Mag. 82,000x

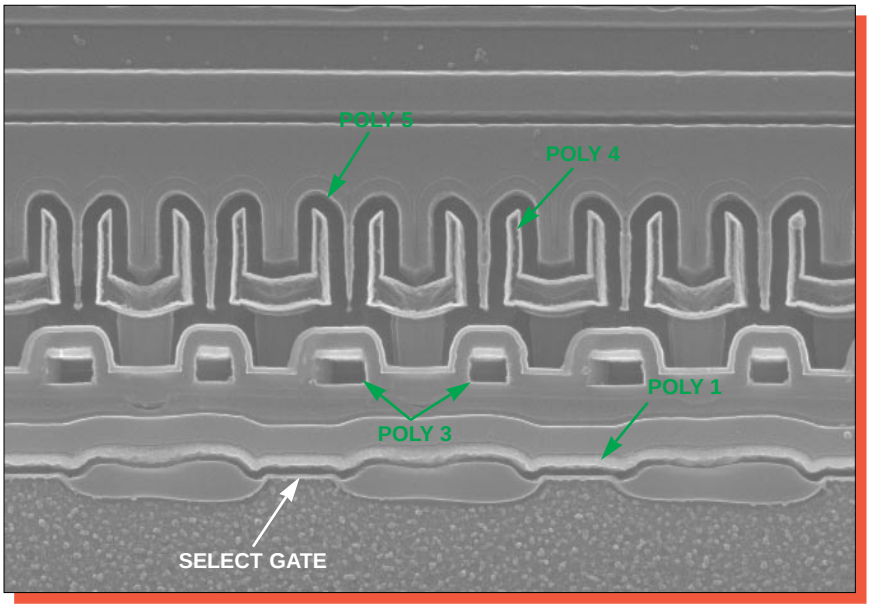


glass etch, Mag. 48,000x

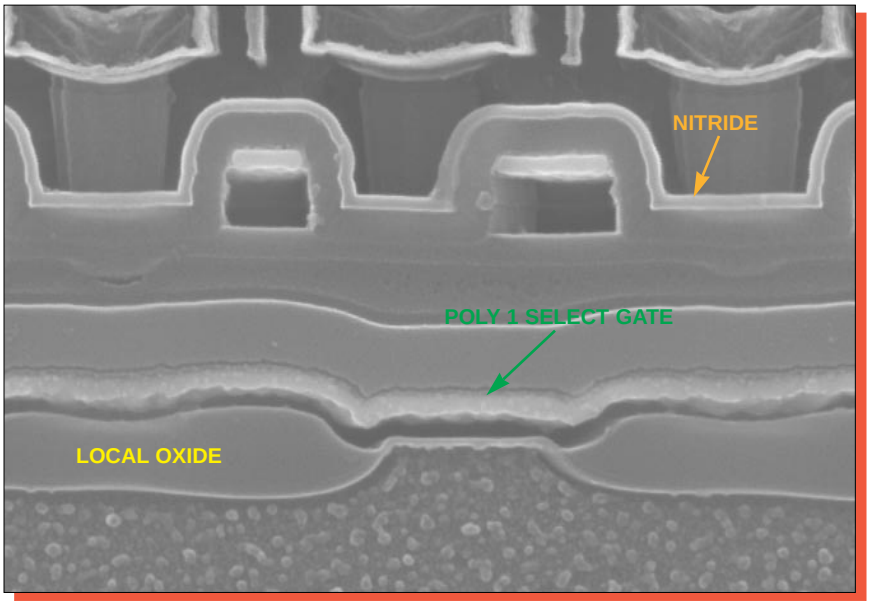


glass etch, Mag. 65,000x

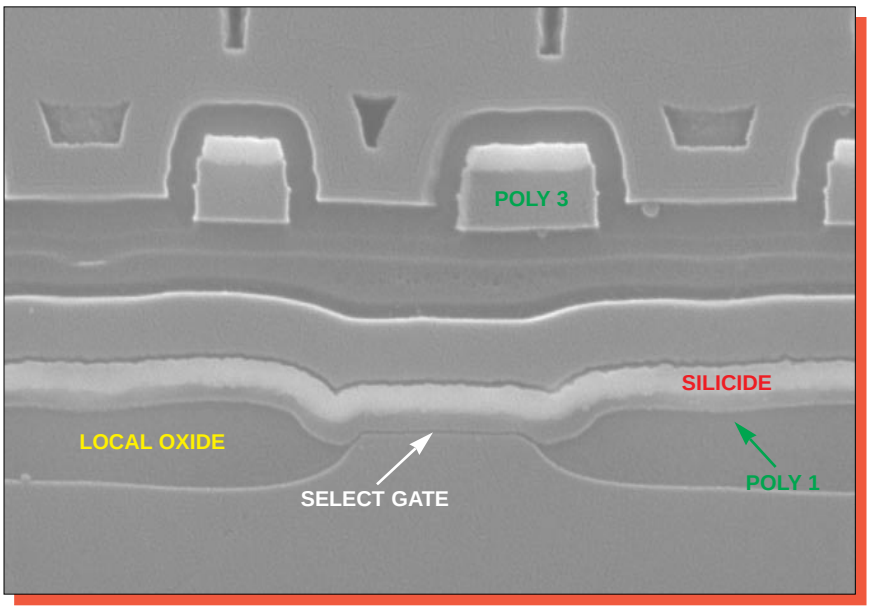
Figure 38a. SEM section details of DRAM cells (perpendicular to bit lines).



Mag. 20,000x



Mag. 46,000x



glass etch,
Mag. 46,000x

Figure 39. SEM section views of the poly 1 word line (perpendicular to bit lines).