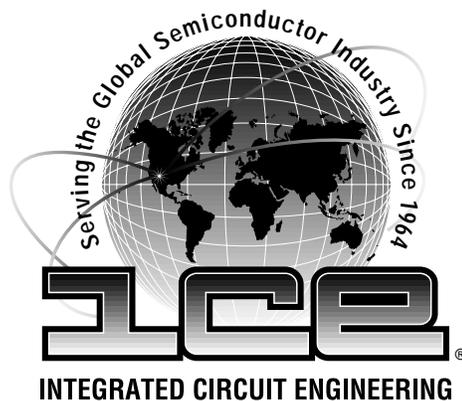


Construction Analysis

NEC 79VR5000 RISC Microprocessor

Report Number: SCA 9711-567



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INTRODUCTION

This report describes a construction analysis of the NEC 75VR5000 RISC Microprocessor. One device packaged in a 272-pin fiberglass BGA (ball grid array) package was received for the analysis. The device was date coded 9711.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

- Three metal, twin-well, P-epi, CMOS process.
- All metal layers employed tungsten via/contact plugs.
- Chemical-mechanical-planarization (CMP).
- Titanium silicided diffusion structures, and a tungsten polycide.
- Sub-micron (0.25 micron) physical gate lengths.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- Package: 272-pin fiberglass BGA (ball grid array).
- Metal lid of package was used as die paddle.
- Internal copper leadframe with gold plated package lands.
- Die attach: Silver-epoxy die attach.
- Die dicing: Sawn (full depth).
- Wirebonding: Thermosonic ball bond method using 1.1 mil O.D. gold wire to single tier package lands.

Die Process:

- Fabrication: Selective oxidation CMOS process employing twin-wells in a P-epi on a P substrate.
- Final passivation: A layer of silicon-nitride over a thin layer of silicon-dioxide.
- Metallization: Three levels of aluminum interconnect patterned by dry-etch techniques. Titanium-nitride (TiN) caps and barriers over titanium (Ti) adhesion layers were employed for each layer. Titanium nitride lined tungsten plugs were employed for all vertical interconnect.
- Intermetal dielectric (IMD2 and IMD1): Both intermetal dielectrics consisted of a multilayered glass followed by a thick deposited glass (TEOS?). Both IMD 1 and 2 were planarized by CMP prior to plug formation only.
- Pre-metal glass: Multilayered borophosphosilicate glass over a nitride sealing layer over densified oxide.

TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Polycide (poly and tungsten silicide) formed all gates on the die including the select and storage gates in the Cache memory arrays.
- Diffusions: LDD process with oxide sidewall spacers left in place, and implanted N+ and P+ sources/drains with a titanium silicide on top. Twin-wells were used in a P-epi on a P substrate.
- Memory cells: Cache SRAM cell arrays were employed on this device. Metal 2 formed "piggyback" word lines, the bit lines and distributed Vcc (via metal 1). Polycide formed the word lines, select and storage gates.
- Fuses: No redundancy fuses were found.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 5

Questionable Items:¹ None.

Design Features:

- The metal lid of the package was employed as a paddle to mount the die.

General Items:

- 272-pin fiberglass BGA (ball grid array). The die was connected to the package lands by wirebonds.
- Overall package quality: Normal. The Ball Grid Array package included a multilayer fiberglass board with solder balls that were evenly spaced and the die was sealed with a black encapsulant on the underside of the package. No voids or problems were noted with the package.
- Die attach: The die was attached to the metal lid/paddle using a silver epoxy die attach of good quality.
- Die dicing: Die separation was by sawing with normal quality workmanship.
- Edge seal: Good. The passivation extended to the scribe lane to seal off the metallization.
- Wirebonding: Single tier wirebonding employing a thermosonic ball bond method using 1.1 mil O.D gold wire. Wire spacing and clearance were adequate at the die edge. The die was mounted low enough in the cavity of the fiberglass board to assist with bonding wire clearance. All wires had normal bond pull strengths (see page 12).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process:

Figures 6 - 37

Questionable Items:¹ None.

Special Features:

- Three metal, twin-well, P-epi, CMOS process.
- All metal layers employed tungsten via/contact plugs.
- Chemical-mechanical-planarization (CMP).
- Titanium silicided diffusion structures, and tungsten silicide on poly.
- Sub-micron (0.25 micron) physical gate lengths.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi on a P substrate.
- Process Implementation: No areas of concern were found. Active area die layout was clean. Alignment/registration was good at all levels and no damage or contamination was found.
- Final Passivation: A layer of silicon-nitride over a thin layer of silicon-dioxide was employed. Integrity tests indicated defect-free passivation. Edge seal was good as the passivation extended into the scribe lane.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II (continued)

- Metallization: Three levels of aluminum interconnect patterned by dry-etch techniques. Titanium-nitride (TiN) caps and barriers over titanium (Ti) adhesion layers were employed for each layer. Tungsten plugs lined underneath with titanium-nitride were used for all vertical interconnect. Plugs had not been subjected to CMP so were not particularly well planarized.
- Metal patterning: Metal layers were defined by dry-etch techniques. Definition was normal for both layers, and no defects were found.
- Metal defects: No voiding or notching of the metals was found.
- Metal step coverage: No excessive metal thinning was present due to the use of tungsten plugs; however, metal 2 and metal 3 aluminum thinned up to 50 percent at via edges.
- Vias and contacts: Via and contact cuts were dry-etched after the dielectric layers were planarized. Slight overetching of the M3 and M2 vias was used to penetrate the cap metal. This appeared well controlled.
- Intermetal dielectrics (IMD2 and IMD1): Both intermetal dielectrics consisted of a multilayered glass followed by another layer of deposited glass (TEOS?). As mentioned, both dielectrics were well planarized by CMP.
- Pre-metal glass: The dielectric between metal 1 and polysilicon consisted of a borophosphosilicate glass over a nitride sealing layer over grown oxide. The top of this dielectric was also planarized by CMP. No problems were found in any of the dielectric layers.
- Polysilicon: Polycide (poly and tungsten silicide) formed all gates on the die including the select and storage gates in the Cache memory array. Oxide sidewall spacers were left in place although they appeared to have been backetched some.
- Isolation: Heavily backetched local oxide (LOCOS). No problems were present at the birdsbeaks. A step was present indicating a twin-wells process.

ANALYSIS RESULTS II (continued)

- Diffusions: LDD process with oxide sidewall spacers left in place. Implanted N+ and P+ source/drains employed a titanium silicide process, although poly used a tungsten silicide. Definition was normal and no problems were present.
- Wells: Twin-wells in a P-epi on a P substrate. No problems were apparent.
- Memory cells: Cache SRAM cell arrays were employed on this device. Metal 2 formed "piggyback" word lines, the bit lines, and distributed Vcc (via metal 1). Polycide formed the word lines and storage gates. Cell pitch was 4.35 x 6.9 microns (30 microns²).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM of assembly features

Wirepull tests

Passivation integrity tests

Passivation removal and inspect metal 3

Aluminum 3 removal

Delayer to metal 2 and inspect

Aluminum 2 removal

Delayer to metal 1 and inspect

Aluminum 1 removal

Delayer to poly/substrate and inspect poly structures and die surface

Die material analysis

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Die placement	G
Die attach quality	G
Wire spacing	N
Wirebond placement	N
Wirebond quality	N
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.1 mil gold.
Die attach method	Silver-epoxy.
Dicing method	Sawn (full depth).
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	G
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

NEC JAPAN
D30500S2-200
VR5000
971119900 ES2.4

WIREBOND STRENGTH

Wire material:	1.1 mil diameter gold
Die pad material:	aluminum
Material at package land:	gold
# of wires tested:	58
Bond lifts:	0
Force to break - high:	13.0g
- low:	8.0g
- avg.:	10.4g
- std. dev.:	0.9

DIE MATERIAL ANALYSIS

Final passivation:	Silicon-nitride over a thin layer of silicon-dioxide.
Metallization:	Aluminum with titanium-nitride (TiN) caps and barriers. All 3 levels employed a titanium (Ti) adhesion layer.
Intermetal dielectrics (IMD2 and IMD1):	Multilayered glass followed by another layer of deposited glass (TEOS?).
Plugs:	Tungsten (W), lined underneath with titanium-nitride.
Pre-metal glass:	Borophosphosilicate glass containing 4.8 wt. % phosphorus and 4.0 wt. % boron.
Silicide on poly:	Tungsten (W).
Silicide on diffusions:	Titanium (Ti).

VERTICAL DIMENSIONS

Die thickness: 0.3 mm (14.5 mils)

Layers:

Passivation 2:	0.25 micron
Passivation 1:	0.1 micron
Metallization 3 - cap:	0.05 micron
- aluminum:	0.6 micron
- barrier:	0.1 micron
Intermetal dielectric 2 - glass 2:	0.6 micron
- glass 1 (multilayered glass):	0.4 micron
Metallization 2 - cap:	0.06 micron (approx.)
- aluminum:	0.6 micron
- barrier:	0.08 micron
Intermetal dielectric 1 - glass 2:	0.45 micron
- glass 1 (multilayered glass):	0.4 micron
Metallization 1 - cap:	0.07 micron (approx.)
- aluminum:	0.5 micron
- barrier:	0.1 micron
Pre-metal glass:	0.85 micron
Nitride layer:	0.04 micron (approx.)
Densified glass:	0.15 micron
Poly - silicide:	0.1 micron
- poly:	0.14 micron
Local oxide:	0.3 micron
N+ S/D:	0.12 micron
P+ S/D:	0.12 micron
P- well:	Could not delineate
N-well:	1.3 micron

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PACKAGE AND ASSEMBLY	Figures 1 - 5
DIE LAYOUT AND IDENTIFICATION	Figures 6 - 8
PHYSICAL DIE STRUCTURES	Figures 9 - 37
COLOR PROCESS DRAWING	Figure 29
MEMORY CELL STRUCTURES	Figure 30 - 35
GENERAL CIRCUIT LAYOUT	Figure 36
TYPICAL INPUT/OUTPUT LAYOUT	Figure 37

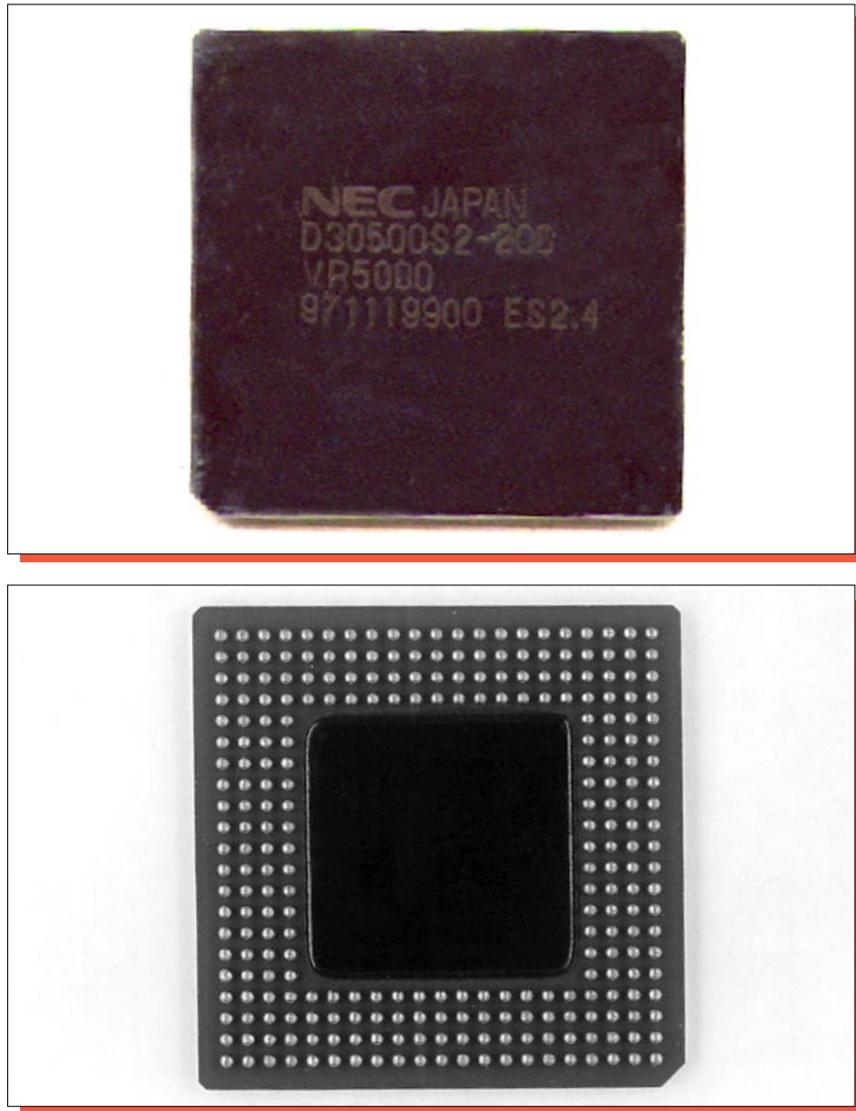


Figure 1. Package photographs of the NEC 79VR5000 RISC. Mag. 2x.

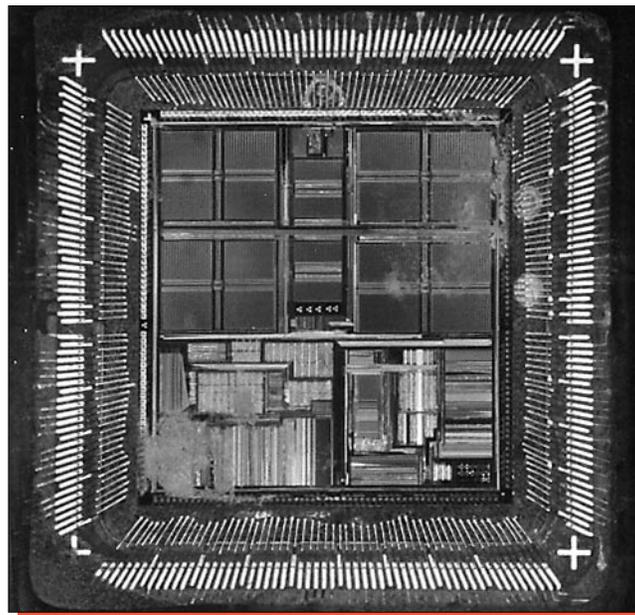


Figure 2. Optical view of the internal portion of the package. Mag. 5x.

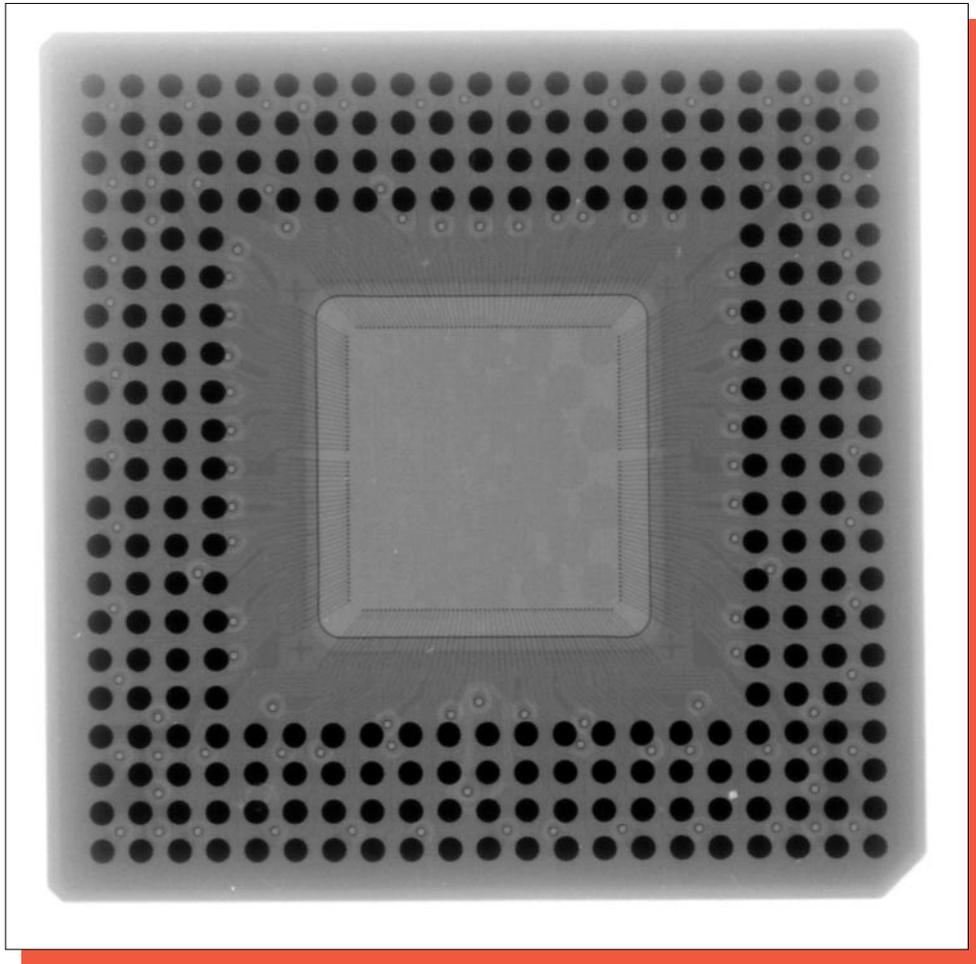
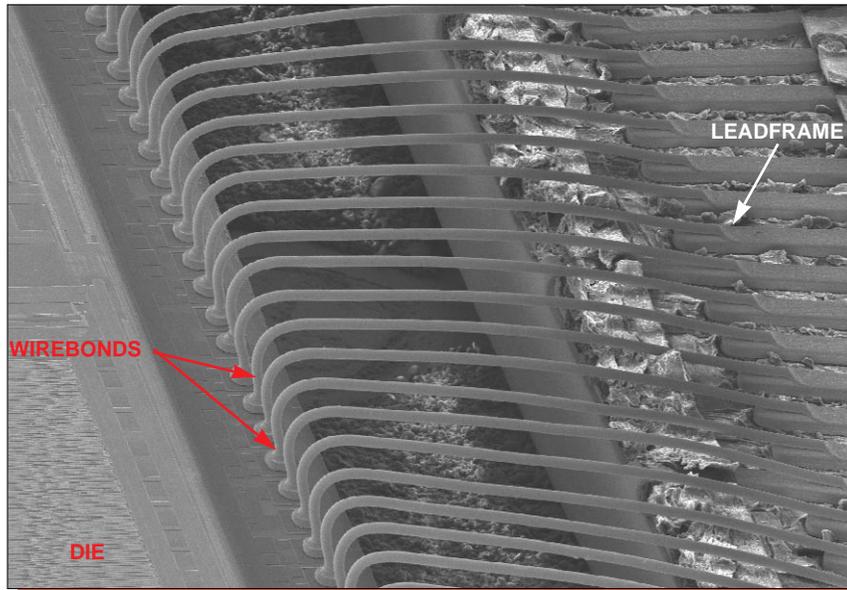
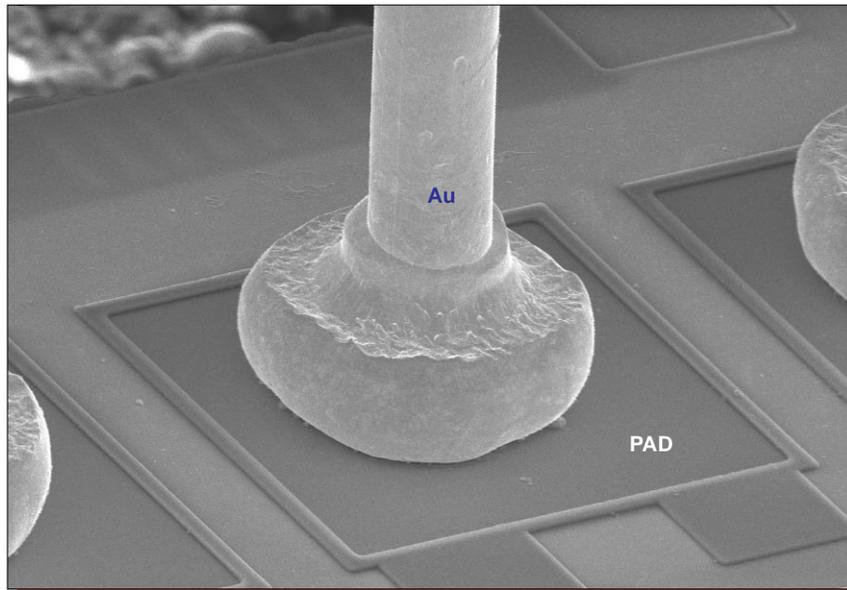


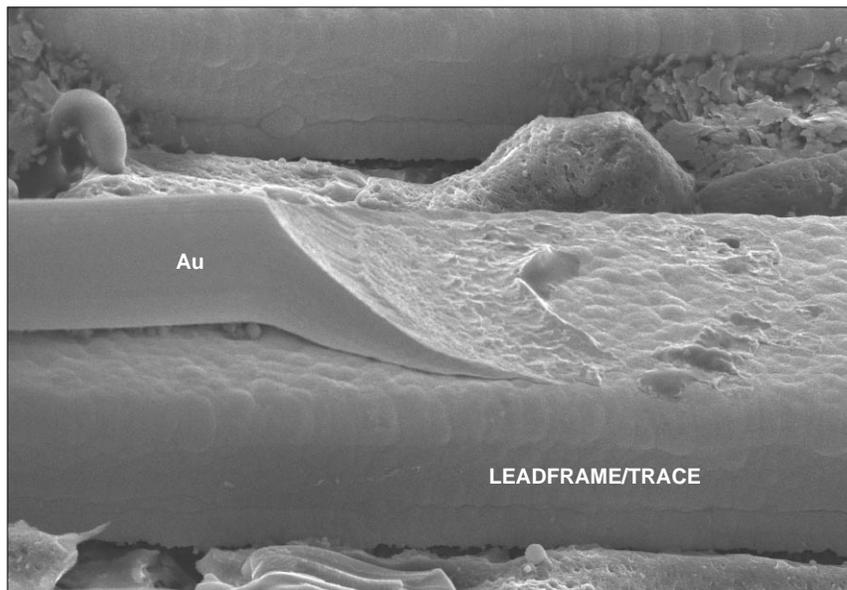
Figure 3. Package x-ray view. Mag. 4x.



Mag. 50x

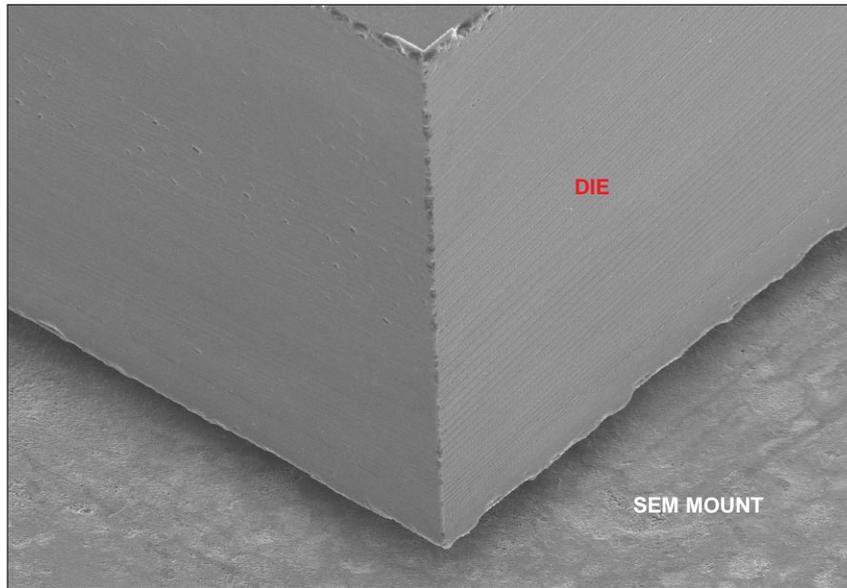


Mag. 600x

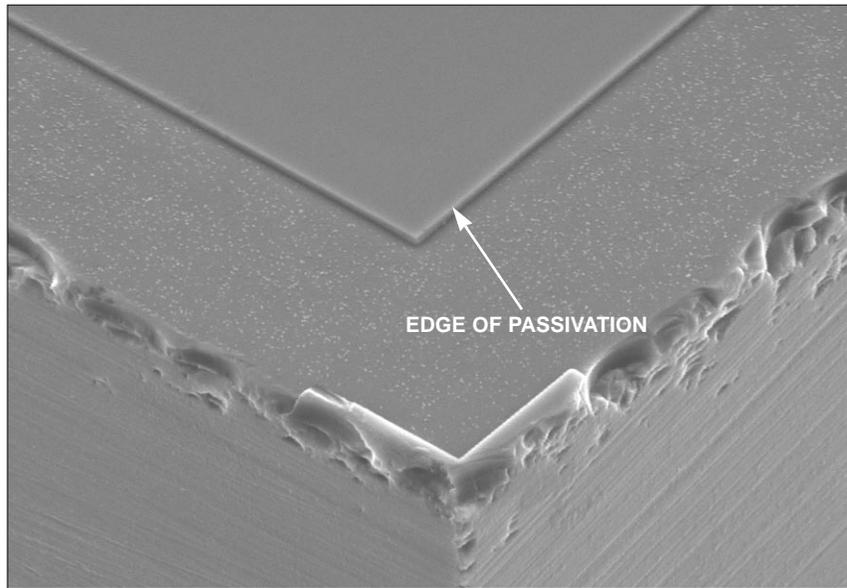


Mag. 600x

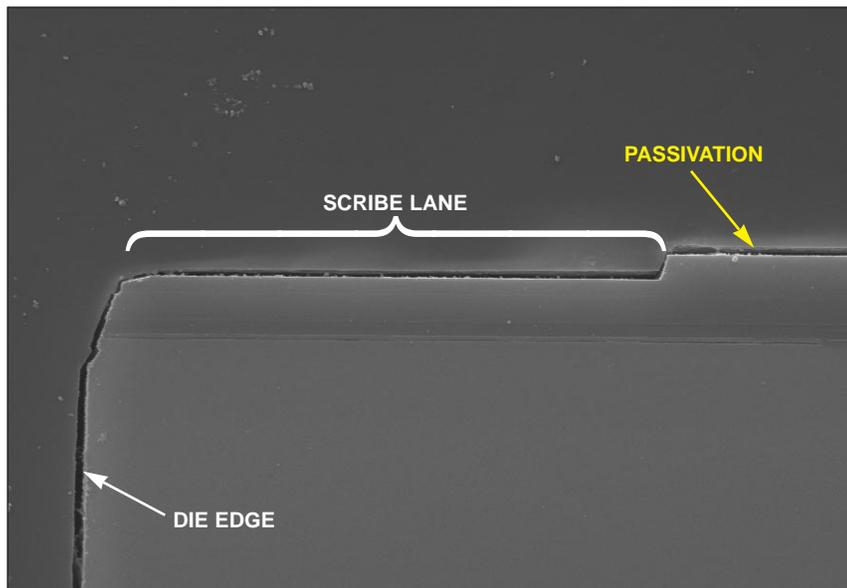
Figure 4. SEM views illustrating typical wirebonds. 60°.



Mag. 250x, 60°



Mag. 1000x, 60°



Mag. 2500x

Figure 5. SEM views illustrating a die corner and edge seal.

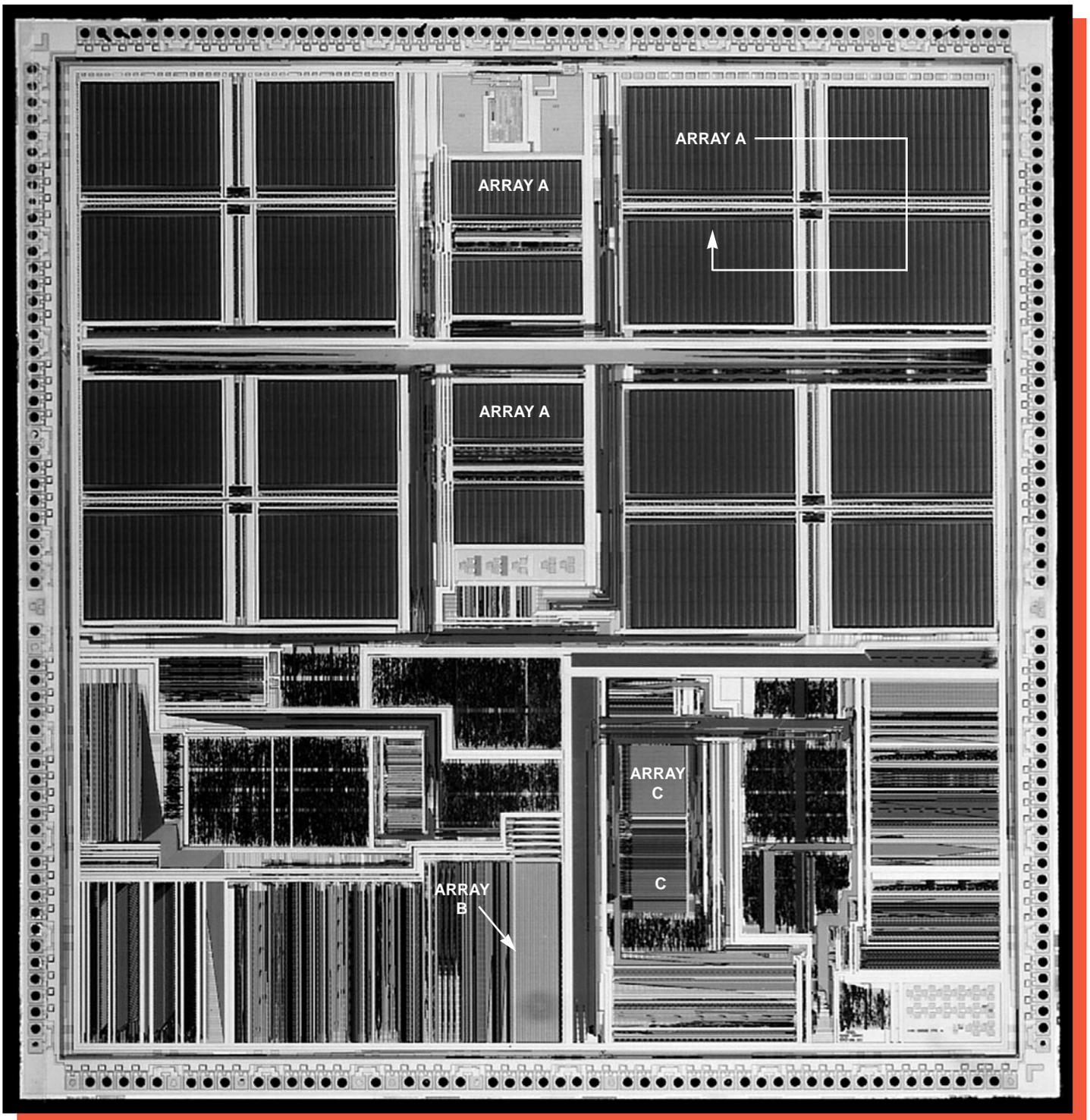


Figure 6. Whole die photograph of the NEC 79VR5000 RISC. Mag. 20x.

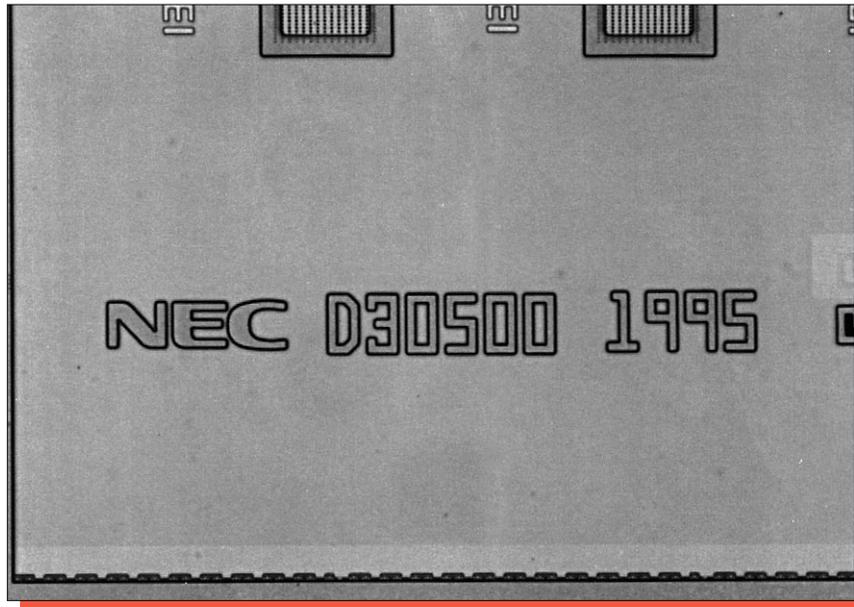


Figure 7. Die identification markings from the surface. Mag. 320x.

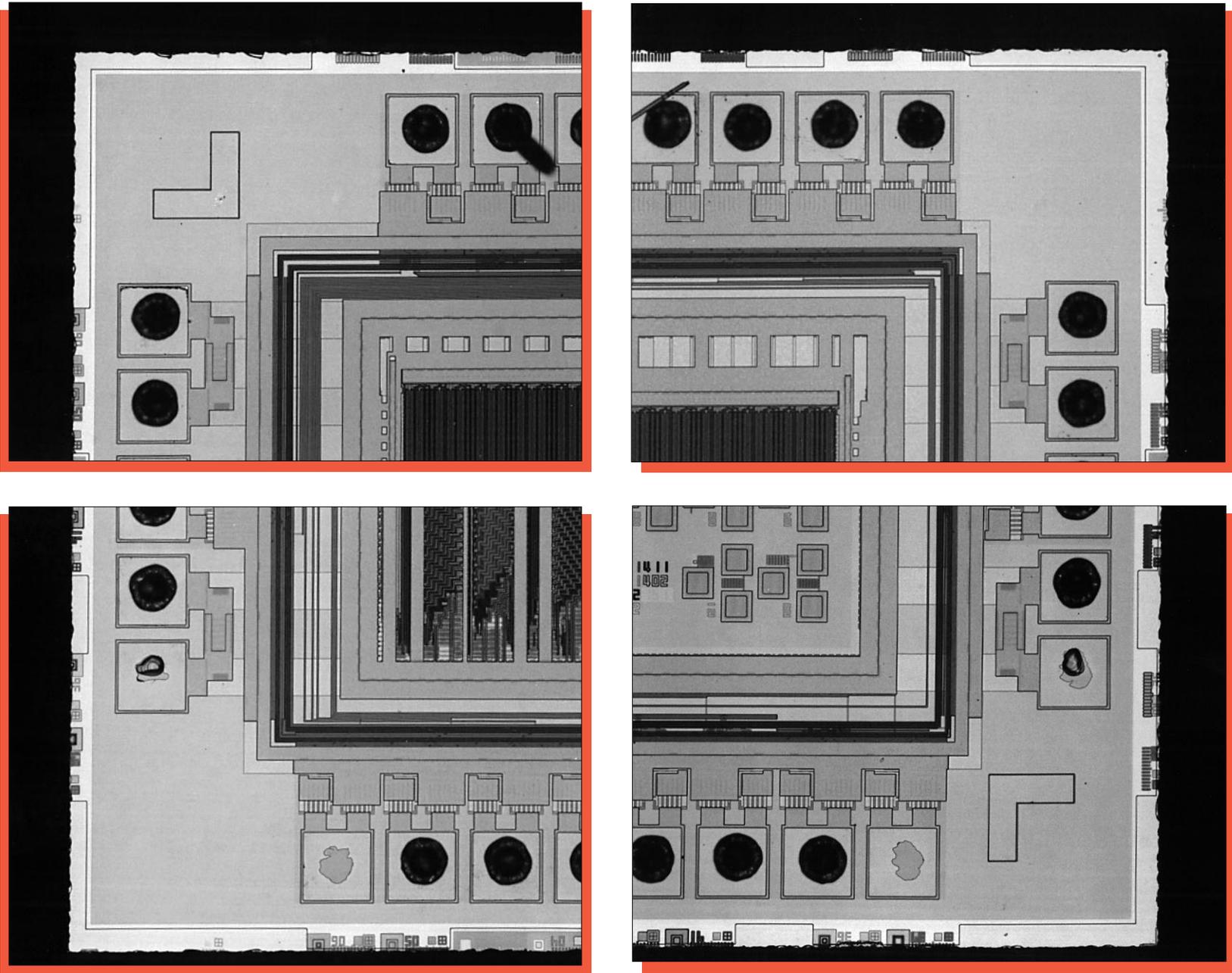
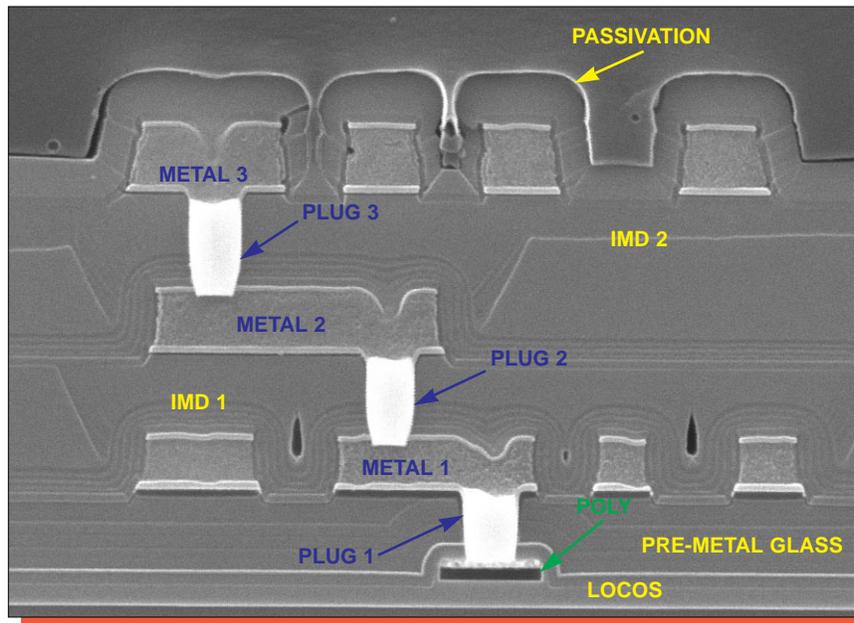
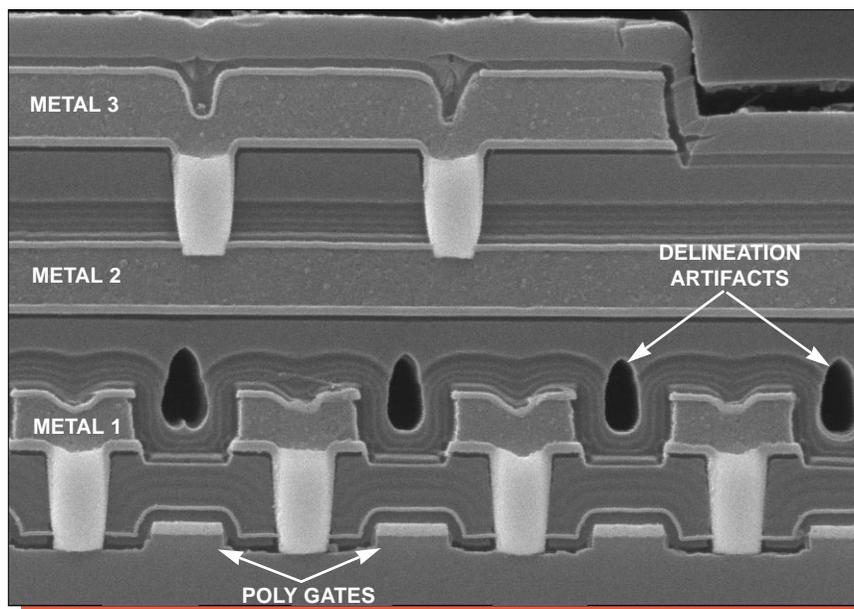


Figure 8. Optical views of the die corners on the NEC 79VR5000 RISC. Mag. 100x.

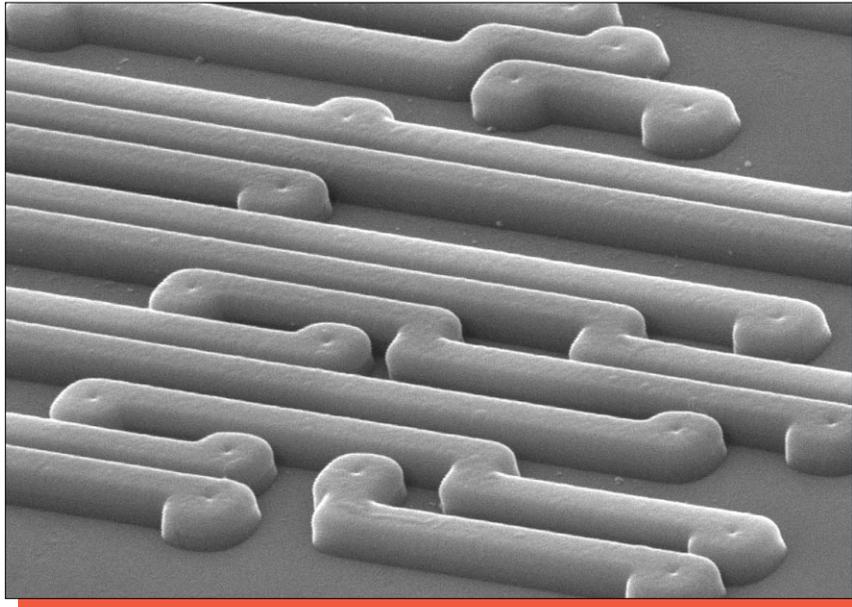


silicon-etch, Mag. 12,000x

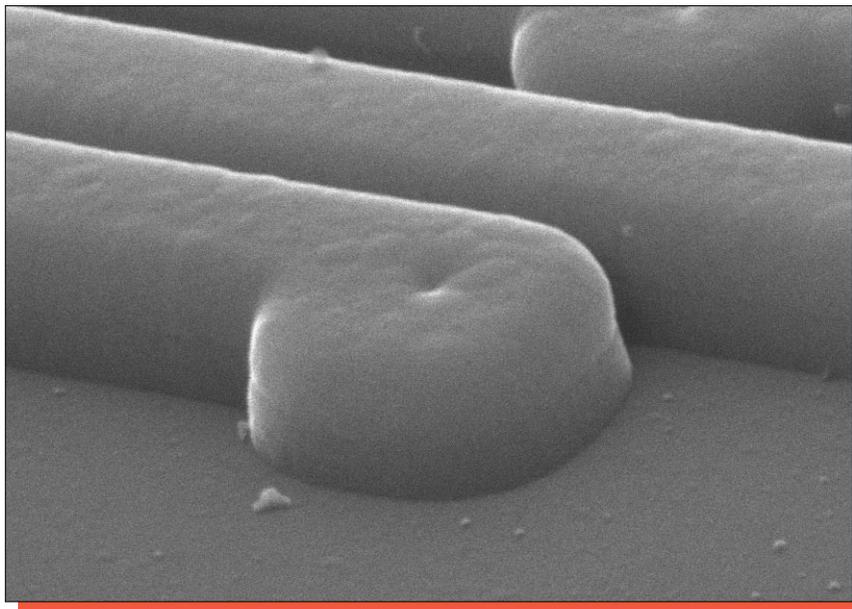


glass-etch, Mag. 13,000x

Figure 9. SEM section views illustrating general device structure.



Mag. 5000x



Mag. 20,000x

Figure 10. SEM views of passivation coverage. 60°.

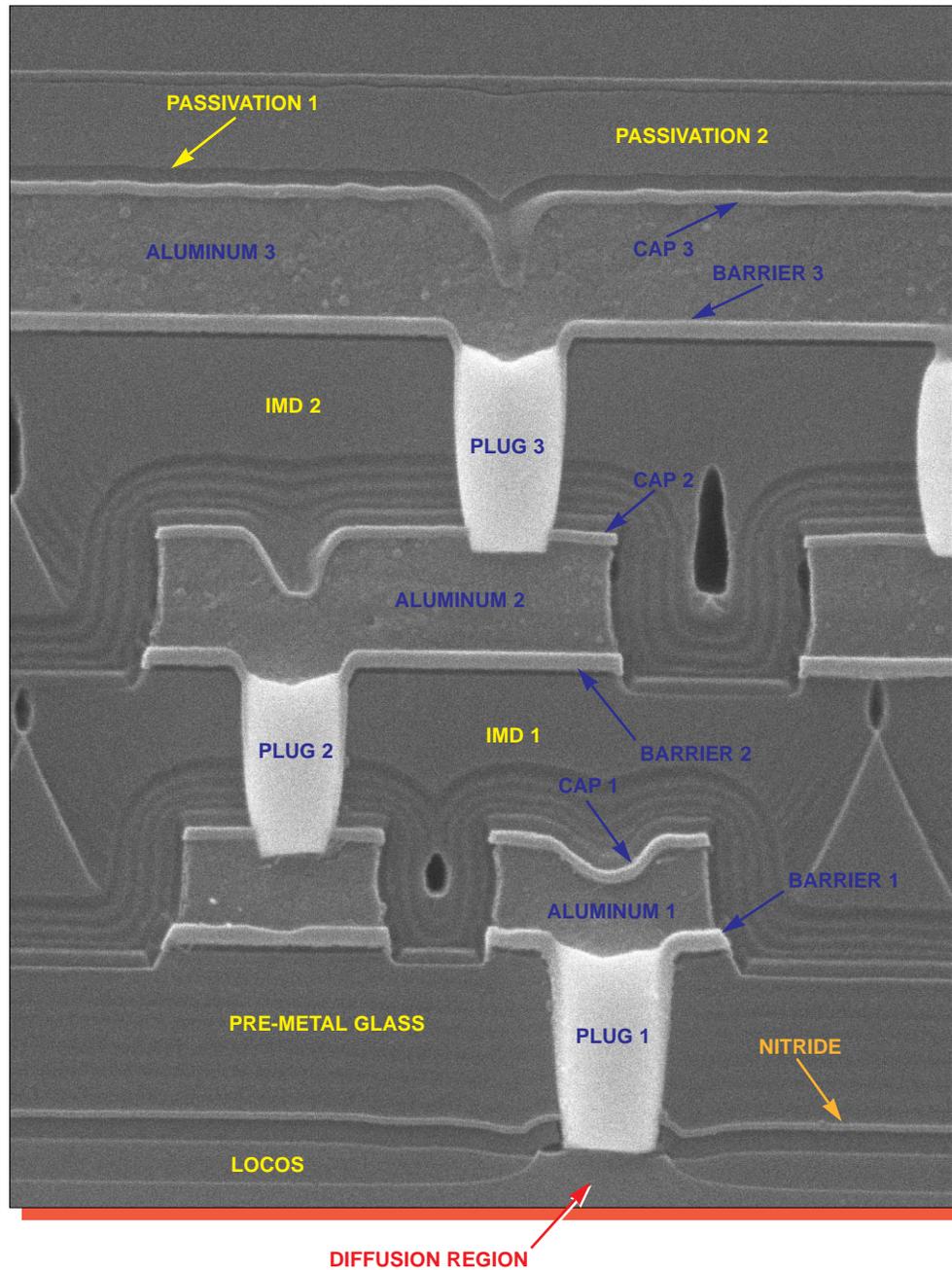
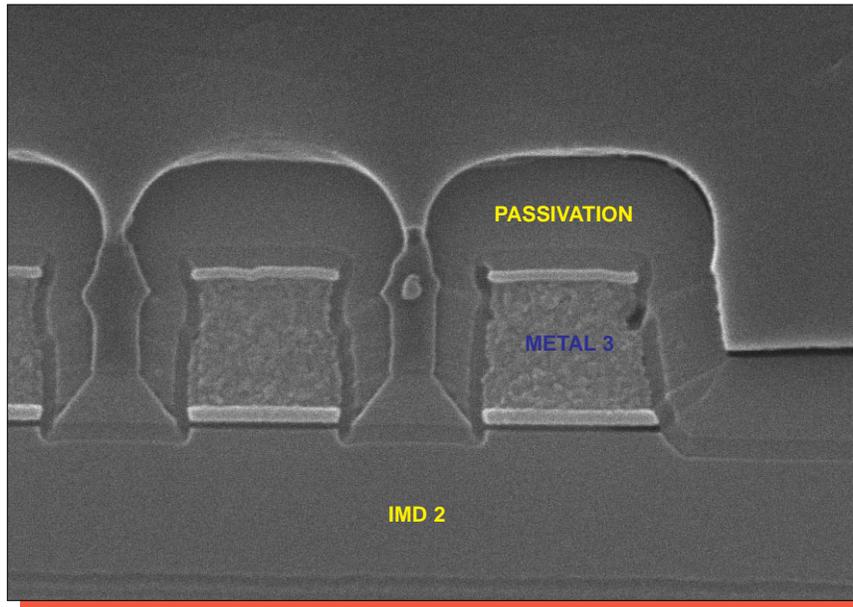
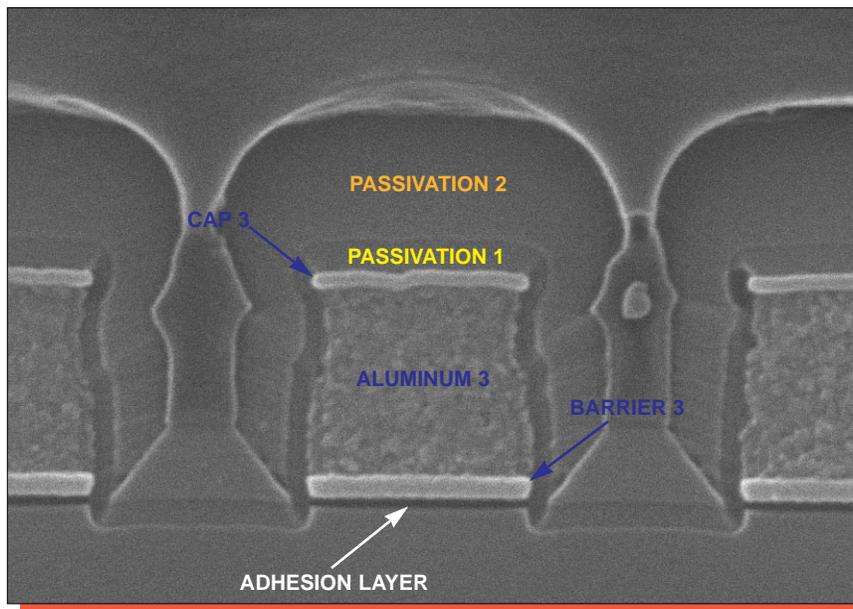


Figure 9a. Detailed SEM section view illustrating general device structure. Glass-etch. Mag. 26,000x.

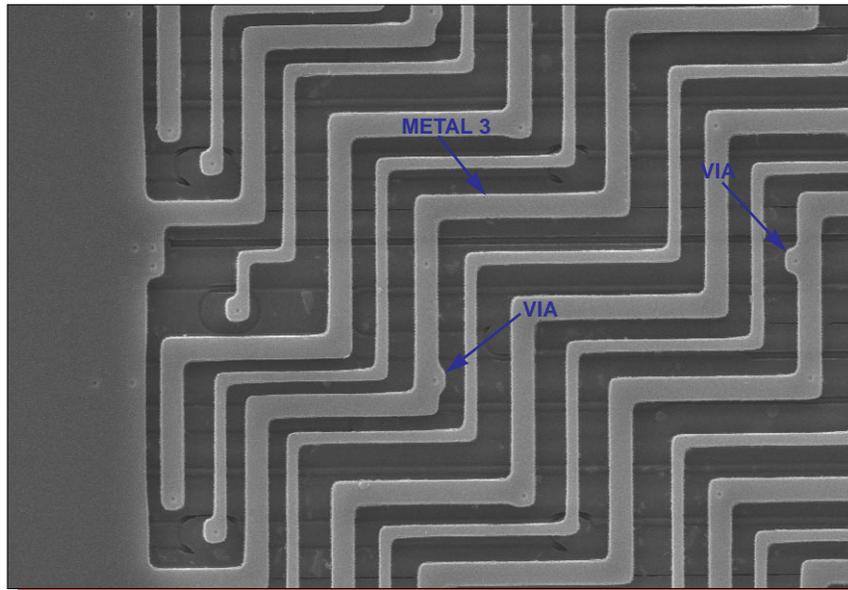


Mag. 26,000x

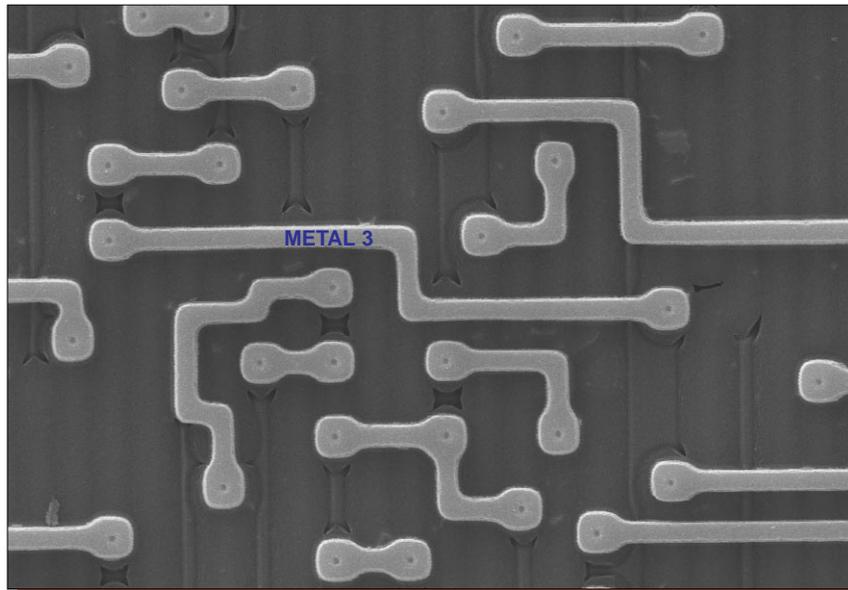


Mag. 40,000x

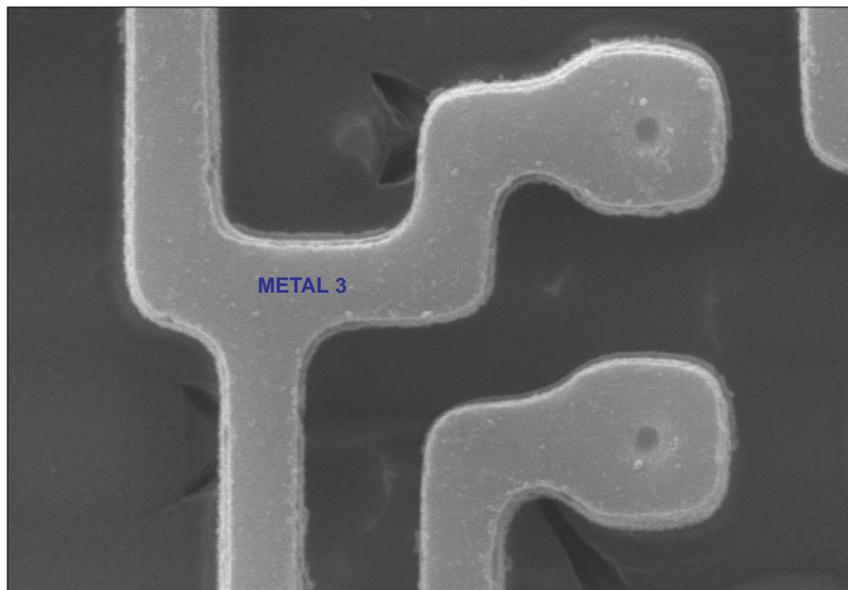
Figure 11. SEM section views of metal 3 line profiles.



Mag. 2000x

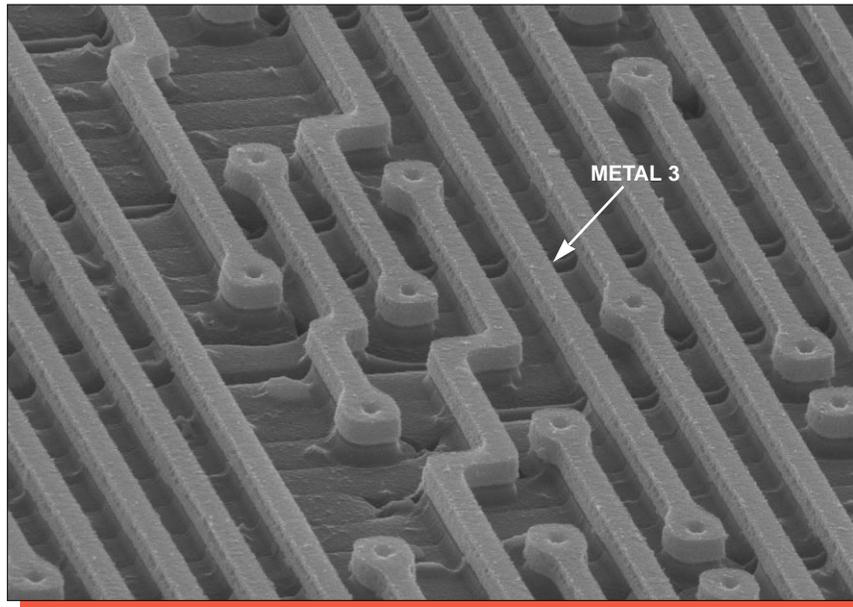


Mag. 3200x

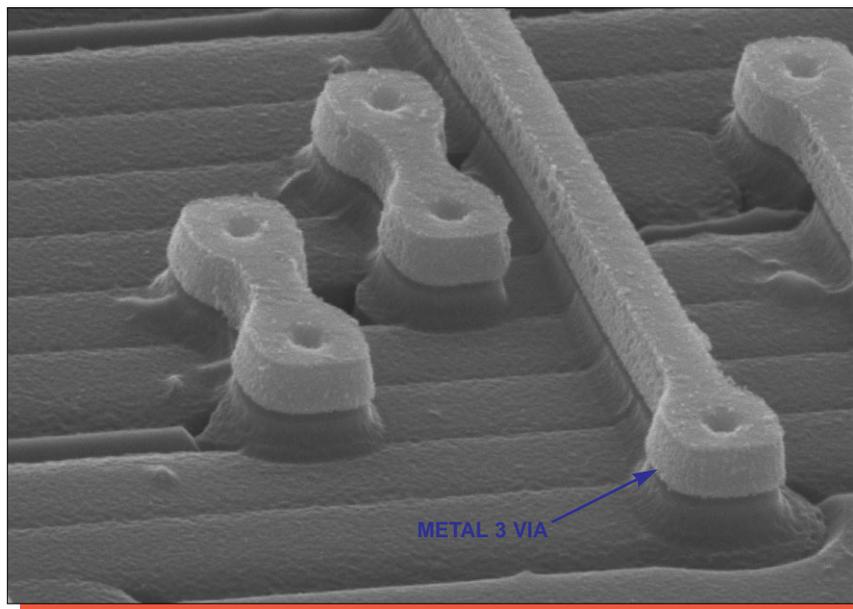


Mag. 13,000x

Figure 12. Topological SEM views illustrating metal 3 patterning. 0°.

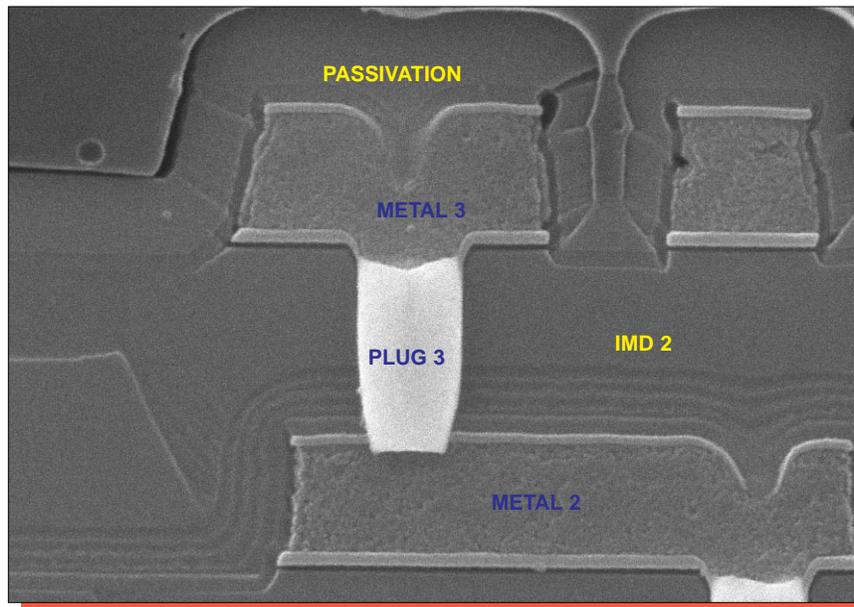


Mag. 5000x

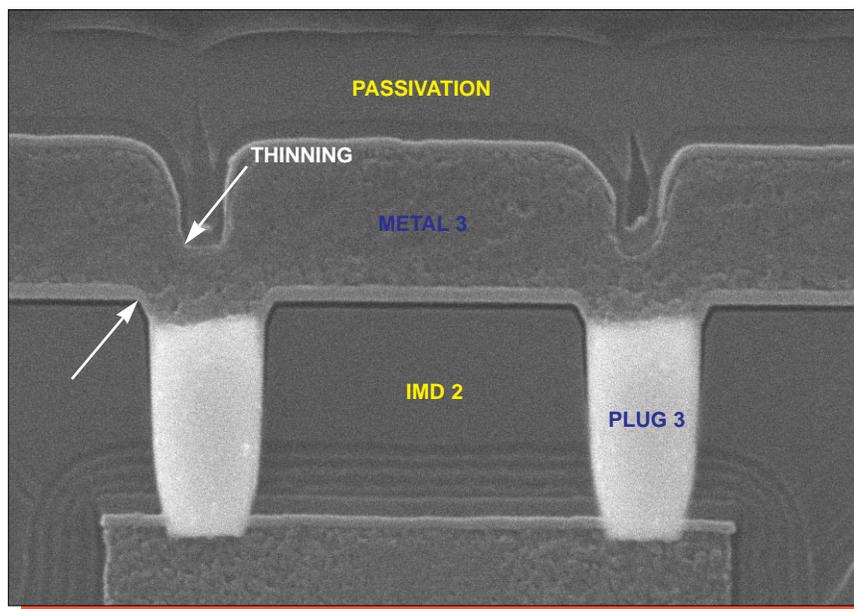


Mag. 10,000x

Figure 13. Perspective SEM views of metal 3 coverage. 60°.

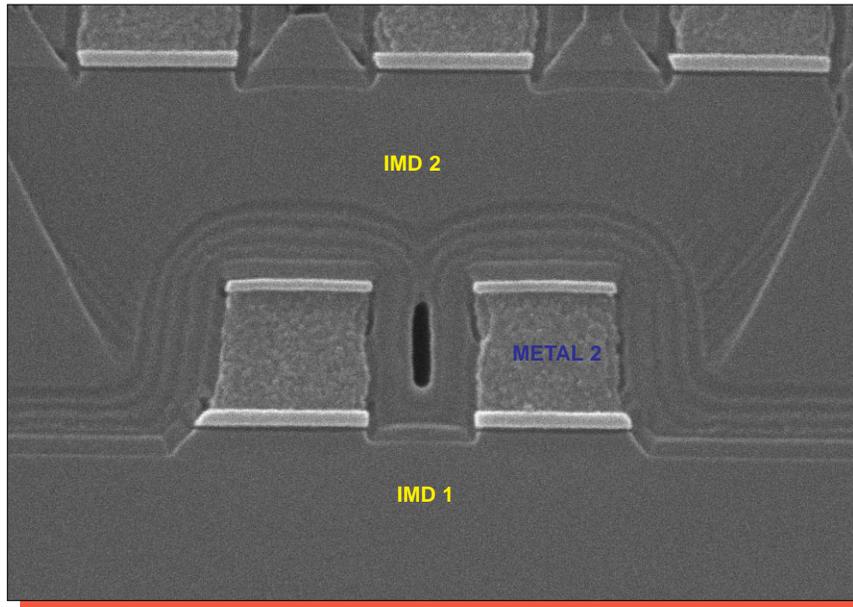


Mag. 24,000x

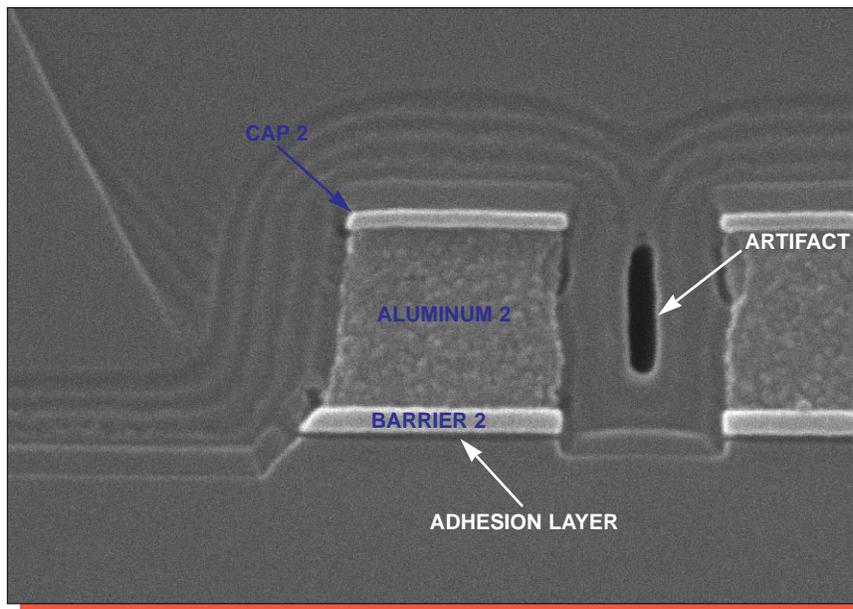


Mag. 26,000x

Figure 14. SEM section views of typical metal 3 vias.

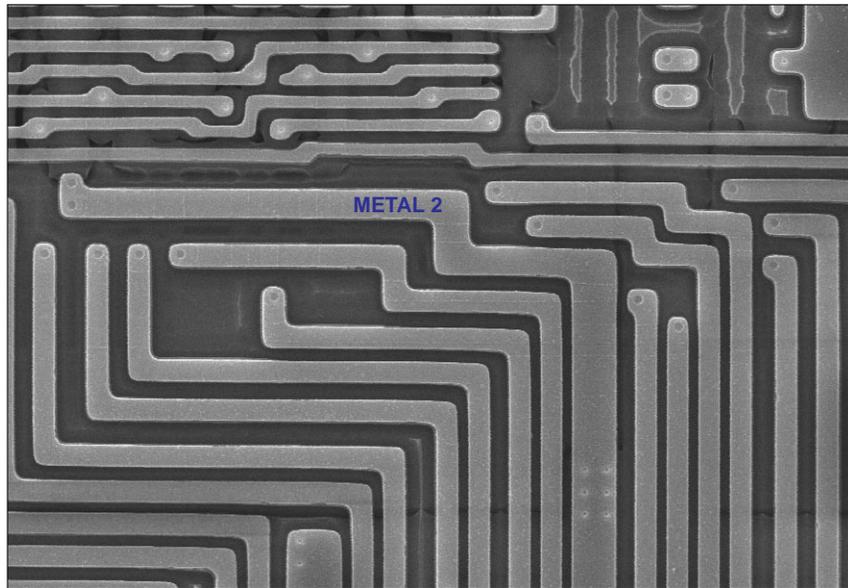


Mag. 26,000x

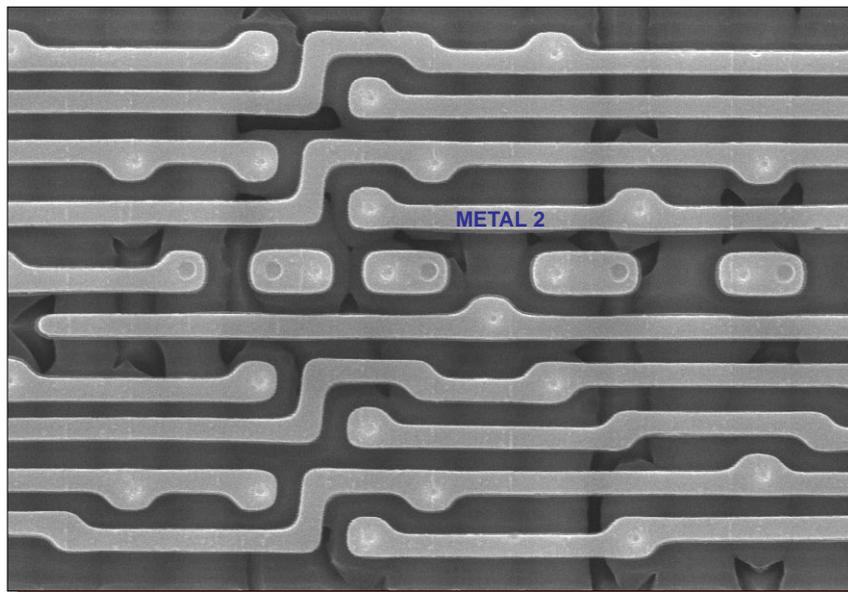


Mag. 40,000x

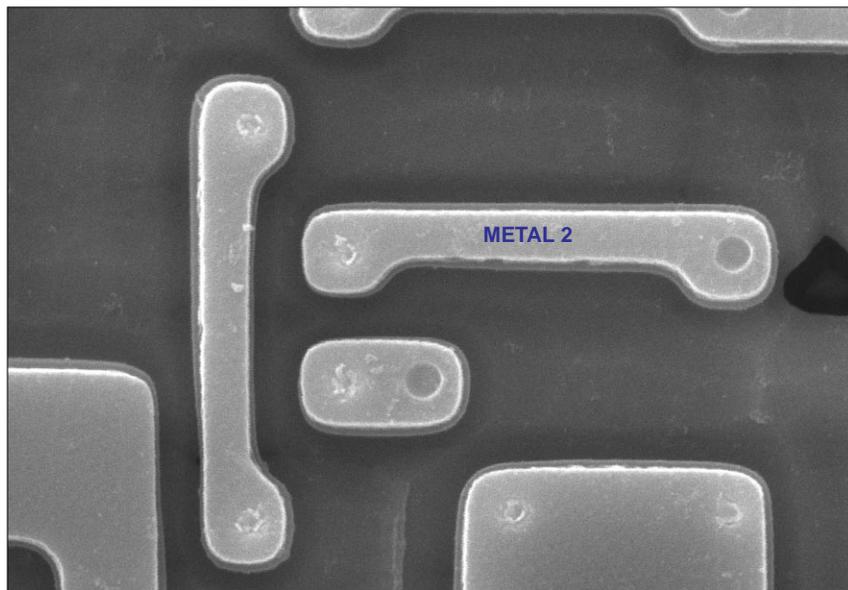
Figure 15. SEM section views of metal 2 line profiles.



Mag. 2500x

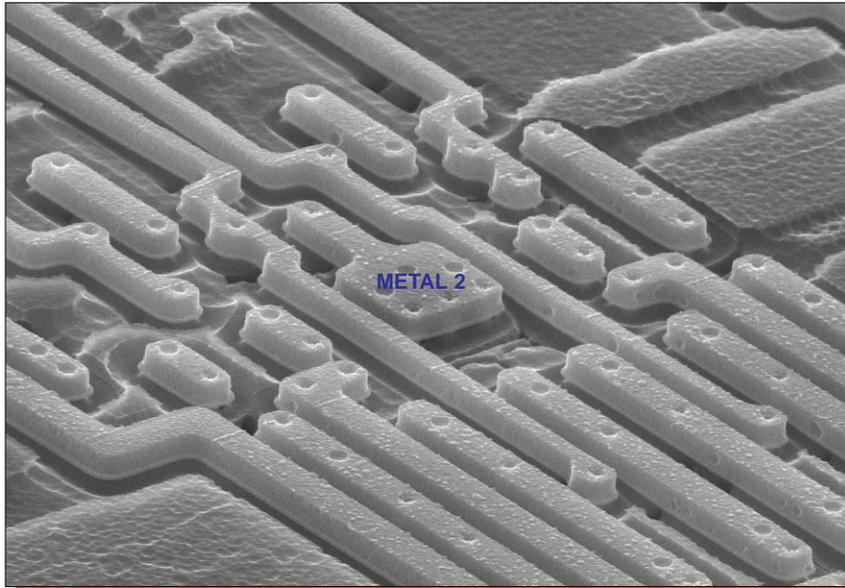


Mag. 5000x

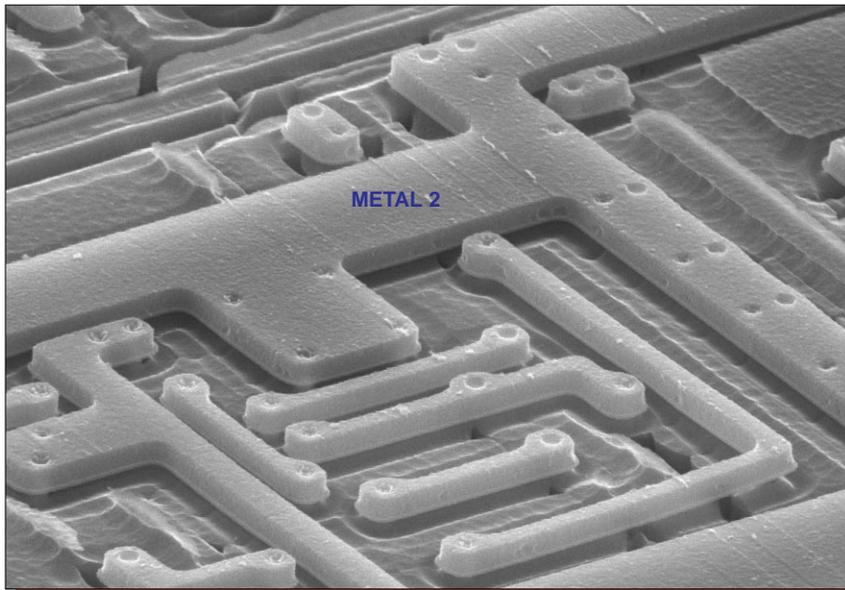


Mag. 10,000x

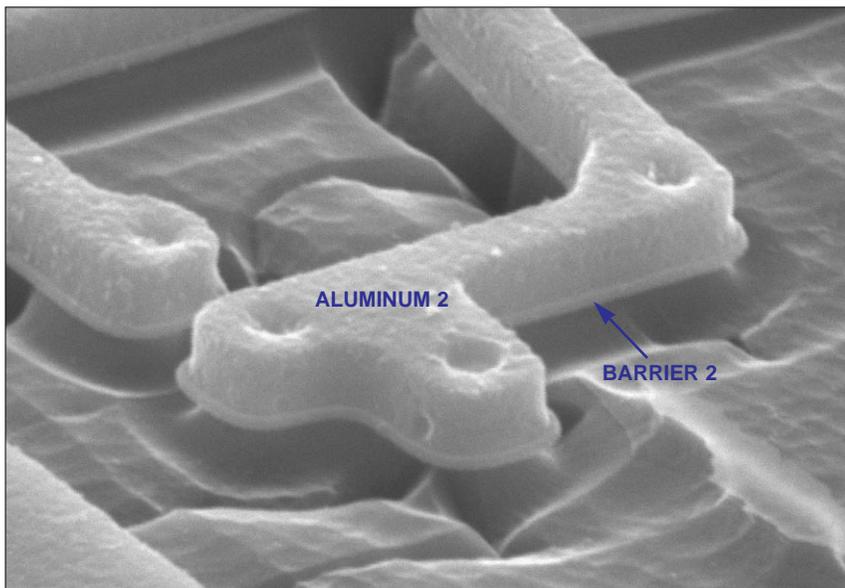
Figure 16. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 5000x

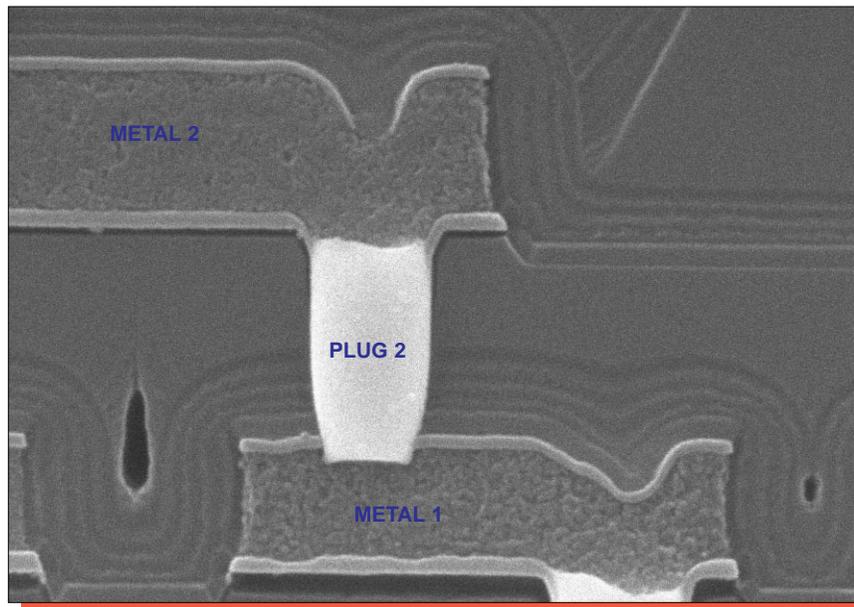


Mag. 5000x

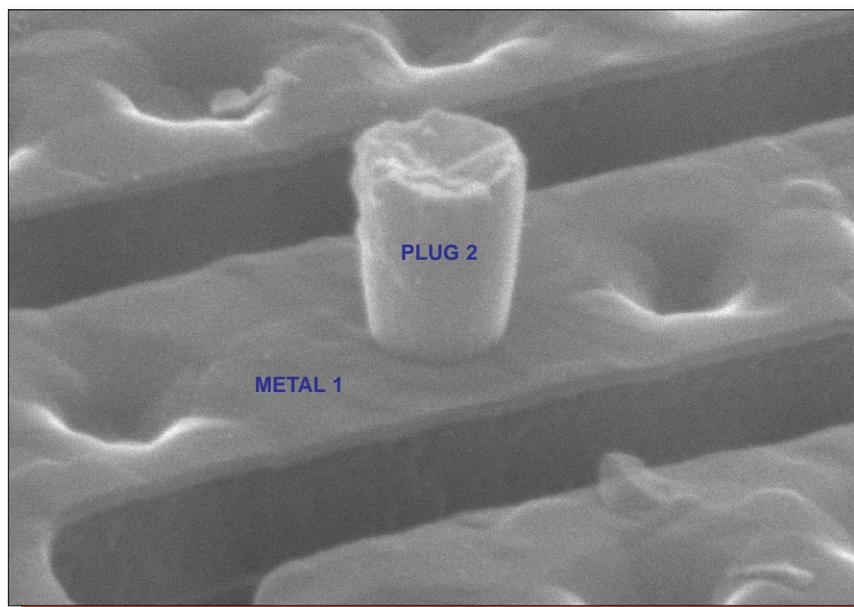


Mag. 16,000x

Figure 17. Perspective SEM views of metal 2 coverage. 60°.

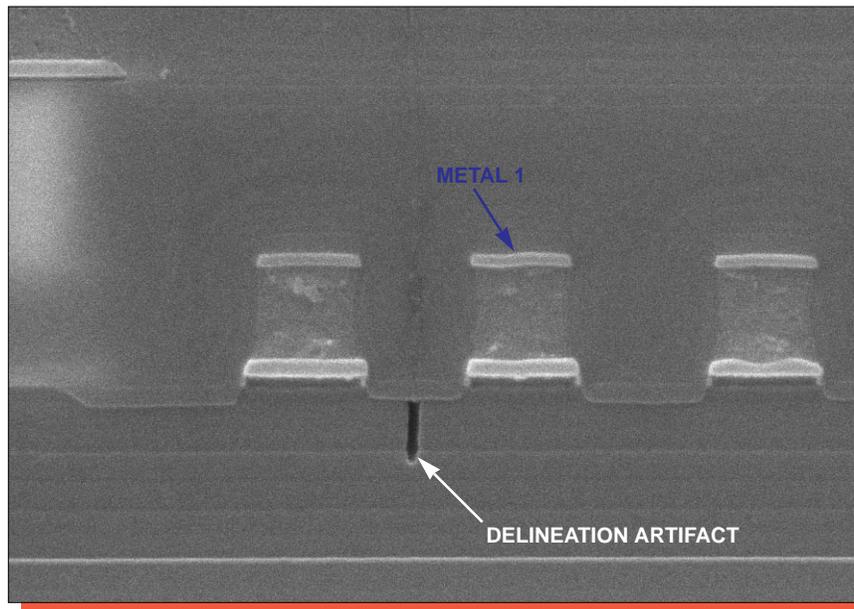


Mag. 30,000x

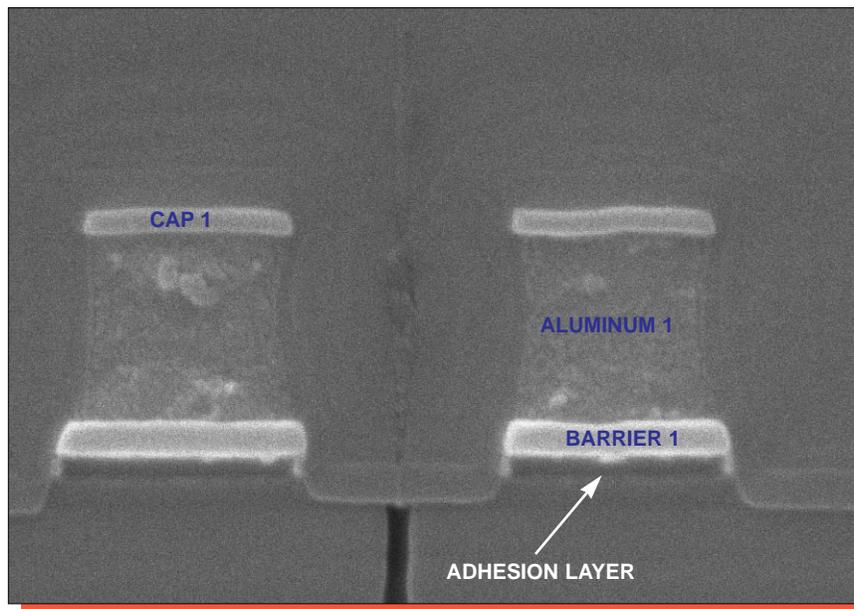


Mag. 40,000x, 60°

Figure 18. SEM views of a metal 2 via and plug.

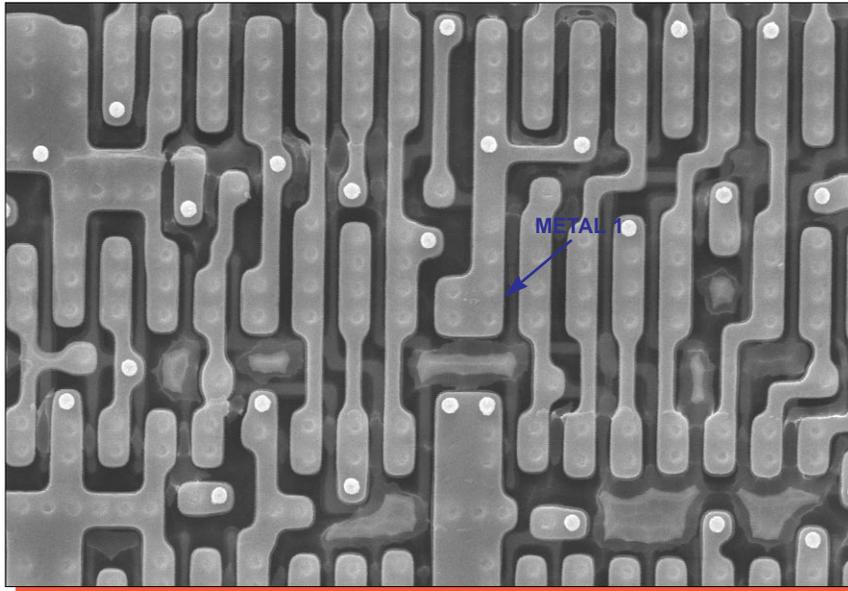


Mag. 26,000x

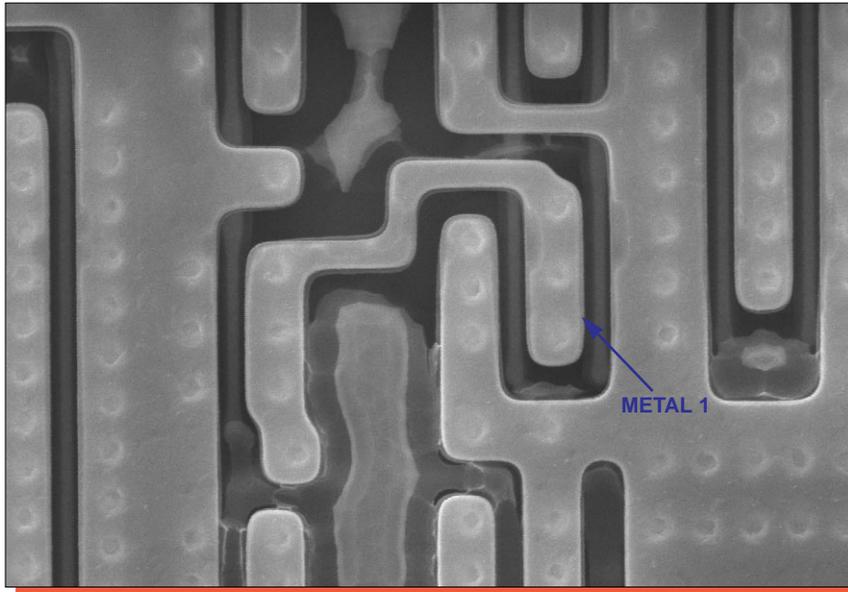


Mag. 52,000x

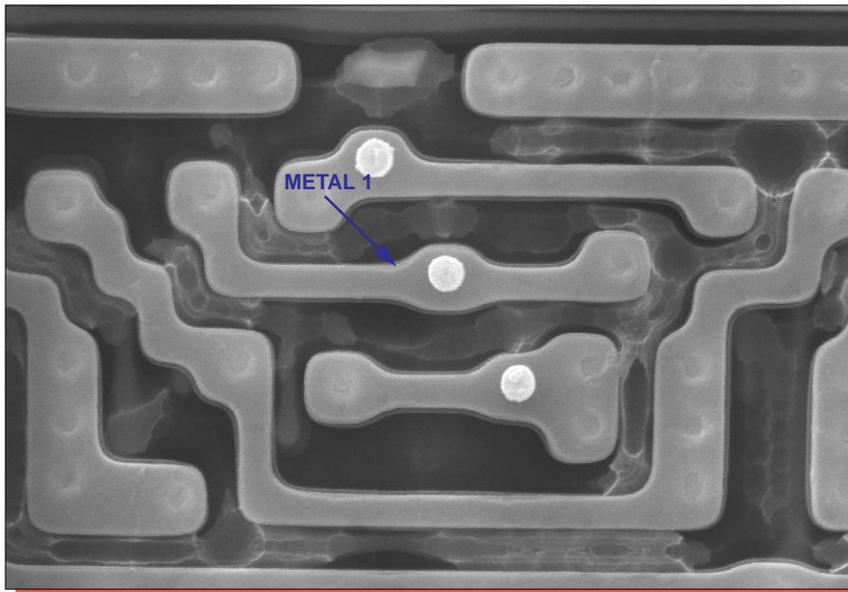
Figure 19. SEM section views of metal 1 line profiles.



Mag. 3500x

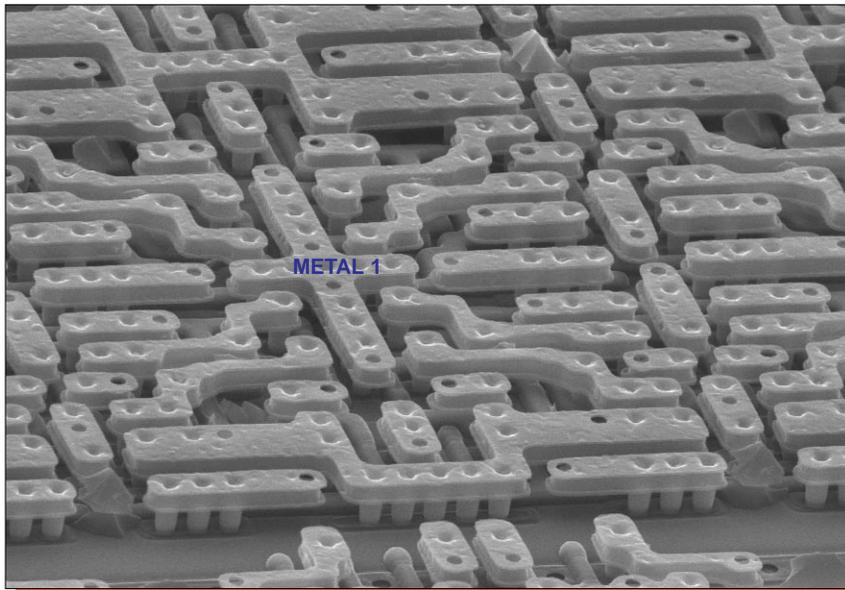


Mag. 6500x

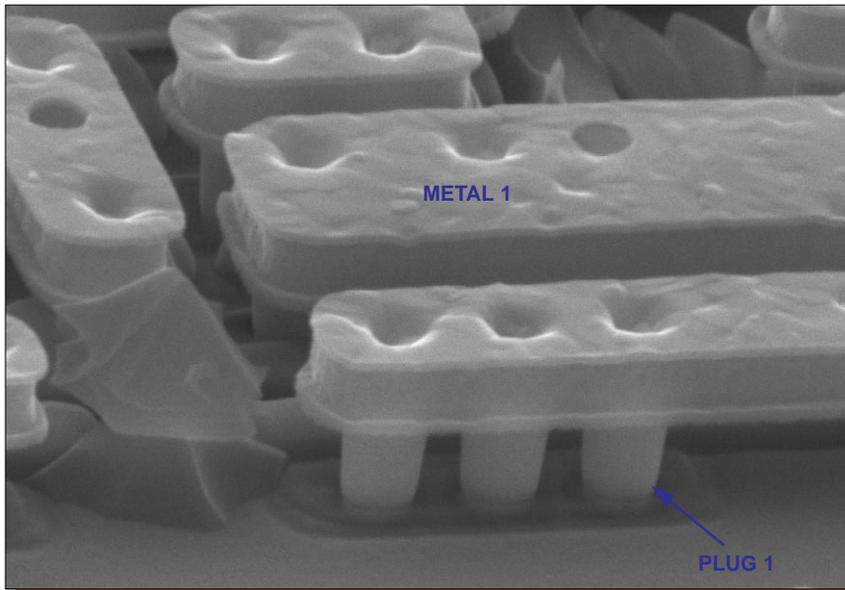


Mag. 8000x

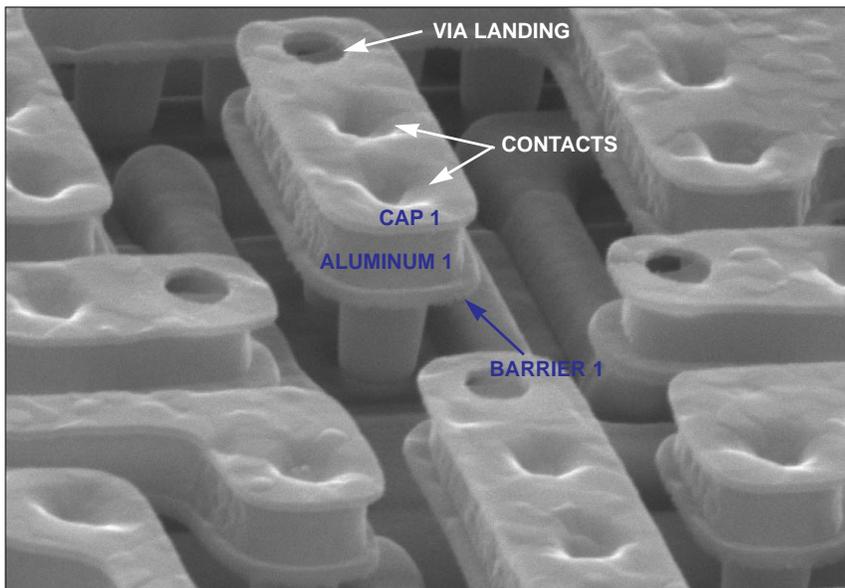
Figure 20. Topological SEM views illustrating metal 1 patterning. 0°.



Mag. 4500x

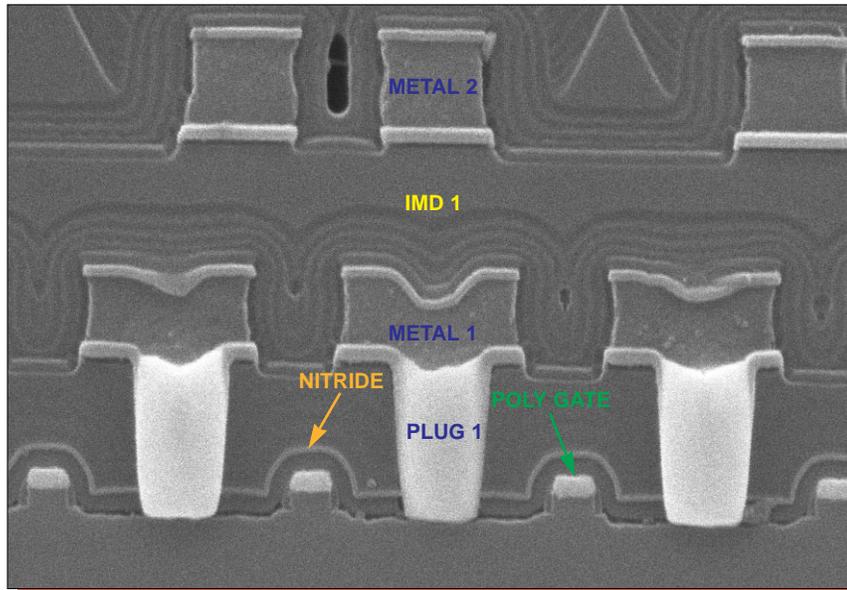


Mag. 18,000x

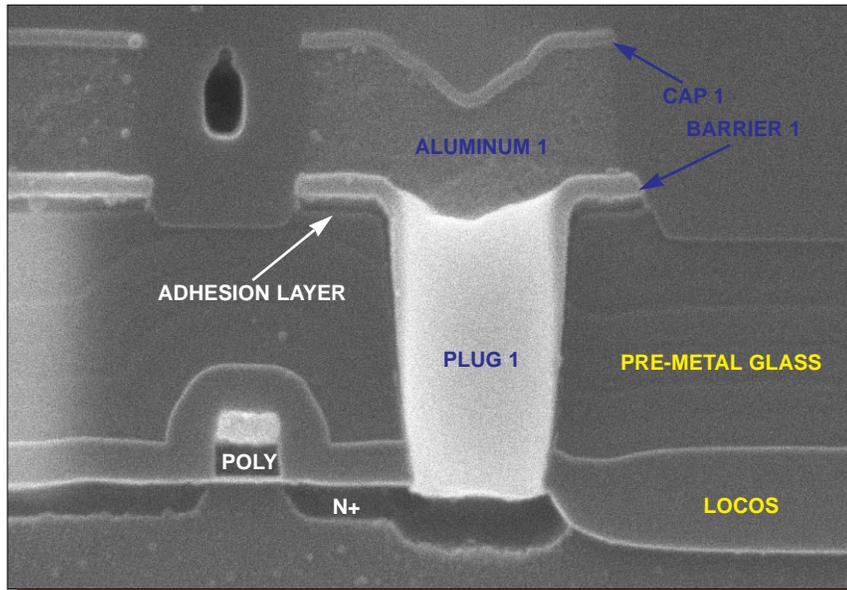


Mag. 18,000x

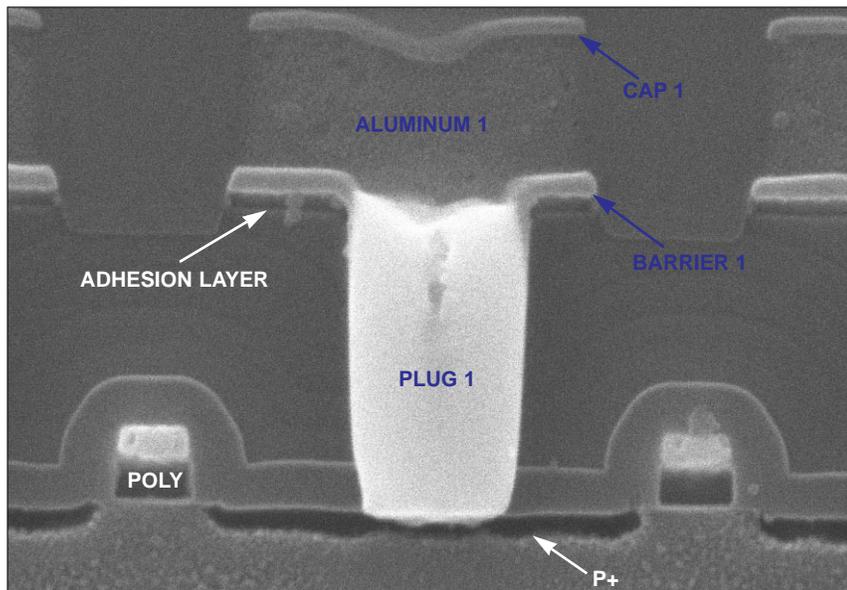
Figure 21. Perspective SEM views of metal 1 coverage. 60°.



glass-etch,
Mag. 20,000x

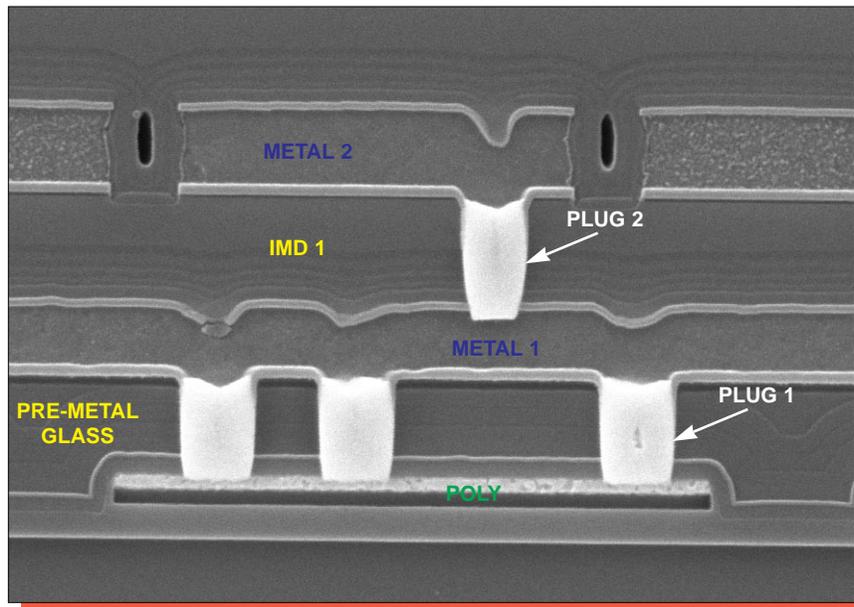


metal 1-to-N+,
silicon-etch,
Mag. 35,000x

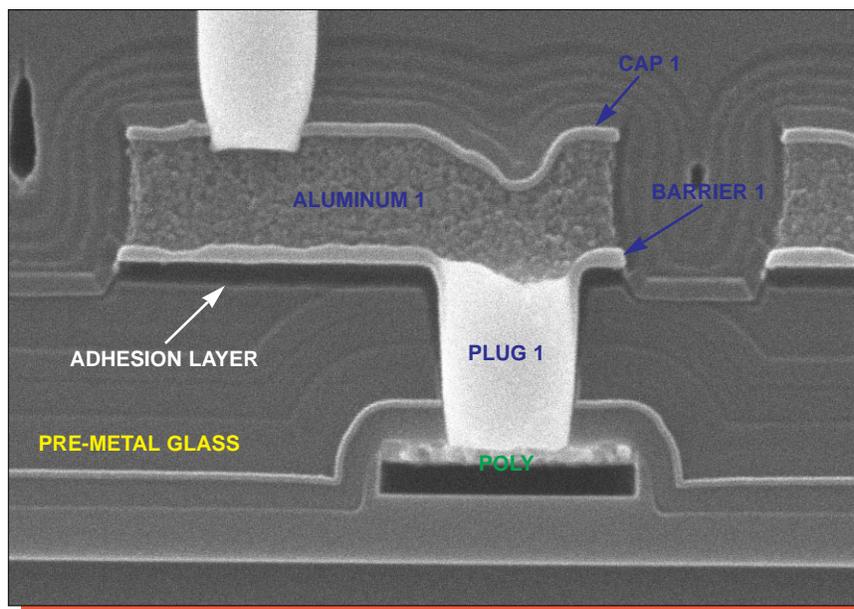


metal 1-to-P+,
silicon-etch,
Mag. 40,000x

Figure 22. SEM section views of typical metal 1-to-diffusion contacts.

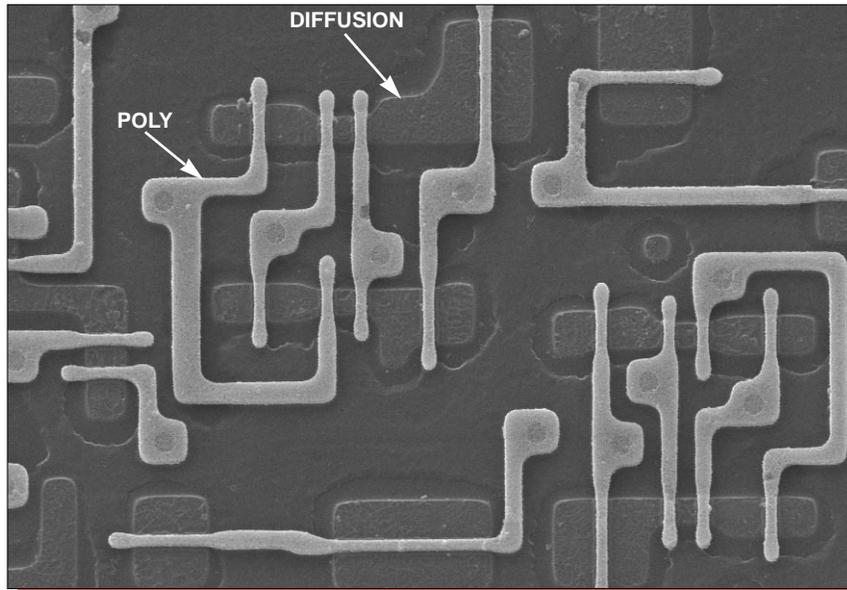


Mag. 16,000x

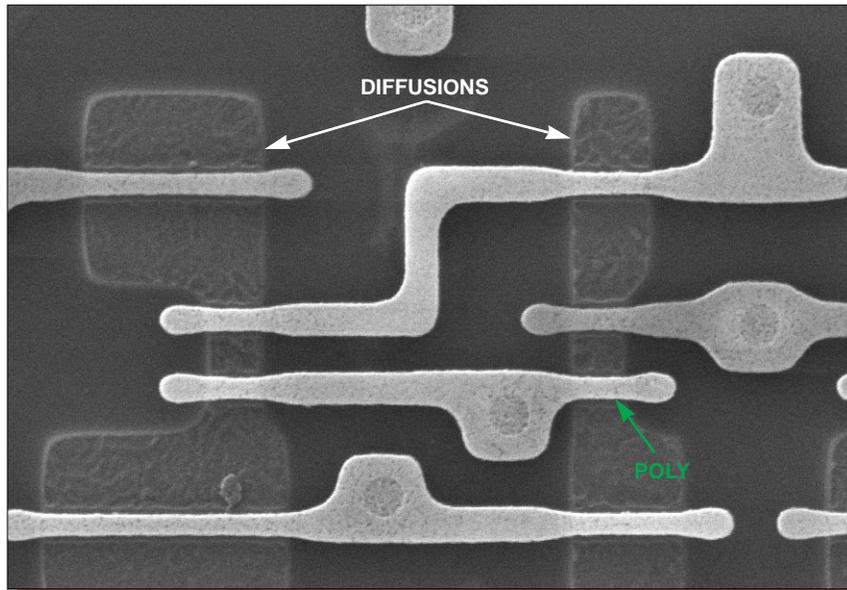


Mag. 30,000x

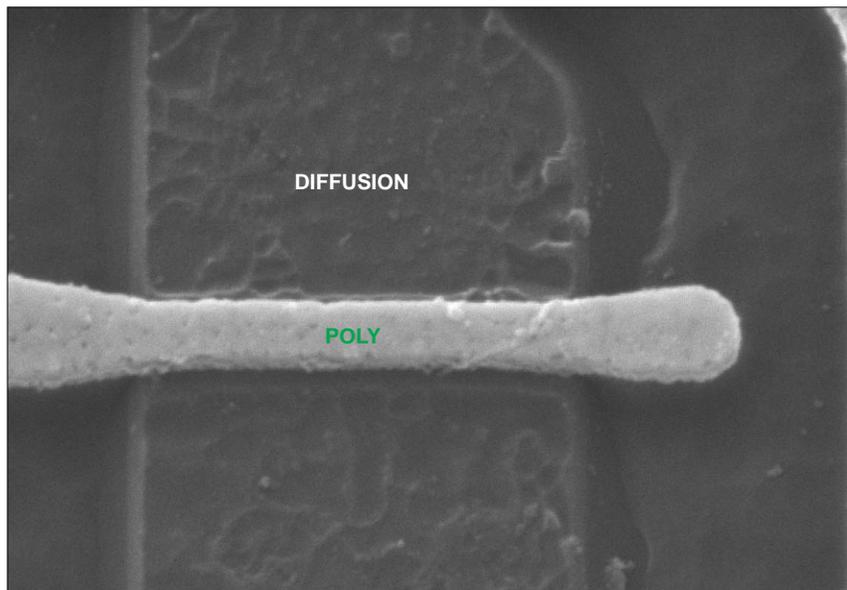
Figure 23. SEM section views of typical metal 1-to-poly contacts.



Mag. 5000x

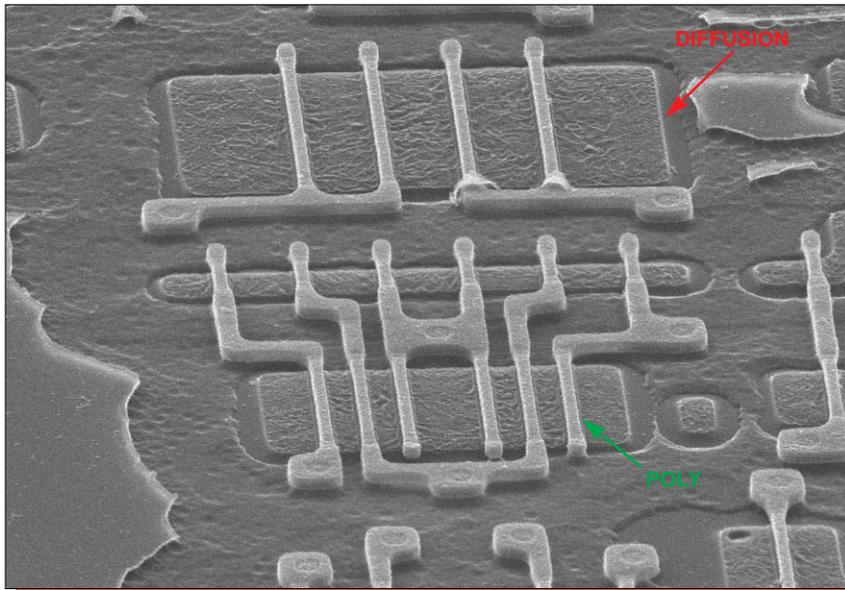


Mag. 10,000x

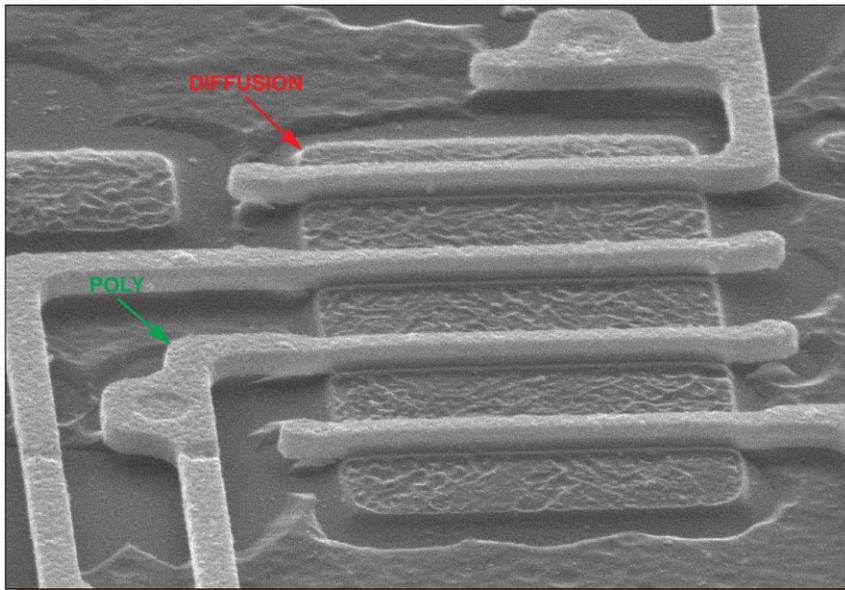


Mag. 30,000x

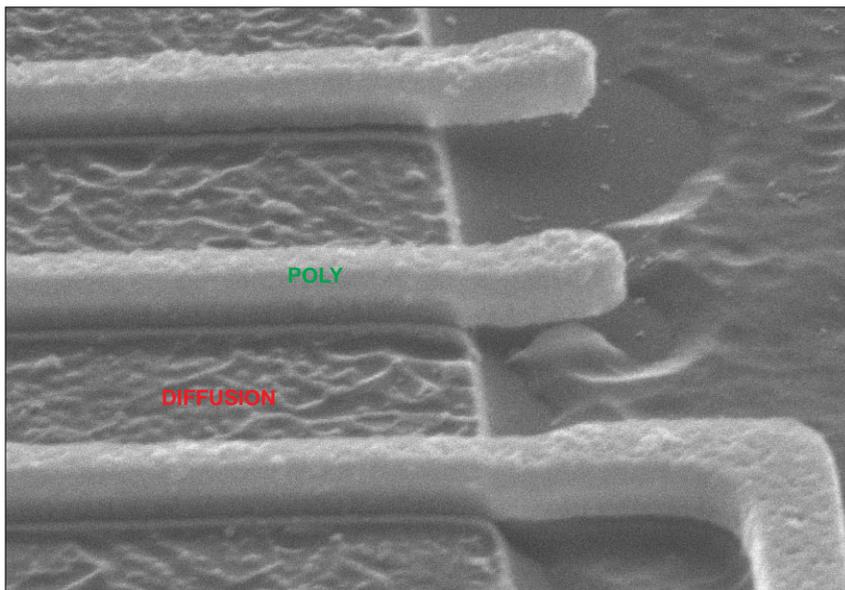
Figure 24. Topological SEM views of poly patterning. 0°.



Mag. 6500x



Mag. 13,000x



Mag. 30,000x

Figure 25. Perspective SEM views of poly coverage. 60°.

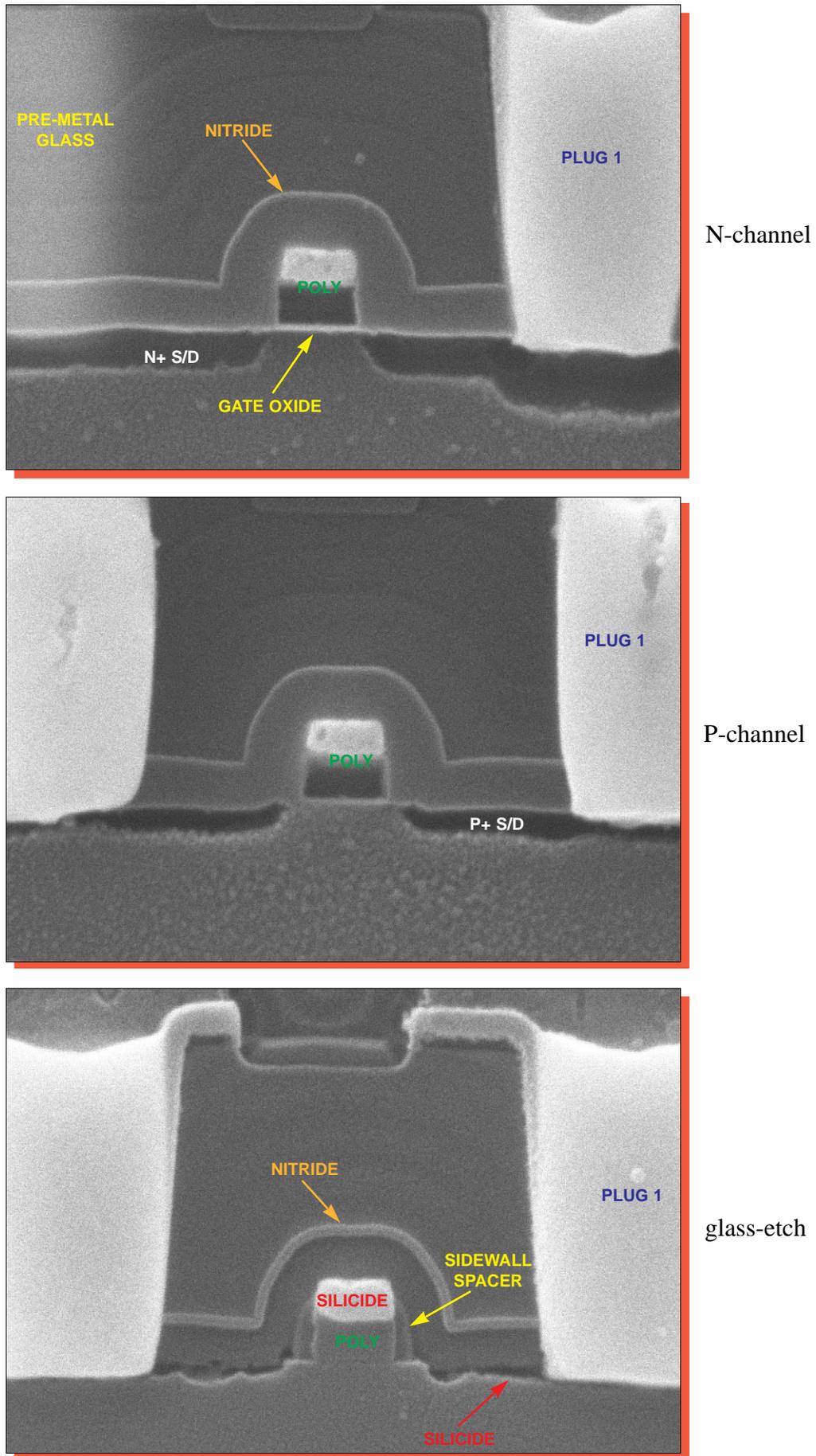


Figure 26. SEM section views of typical transistors. Mag. 52,000x.

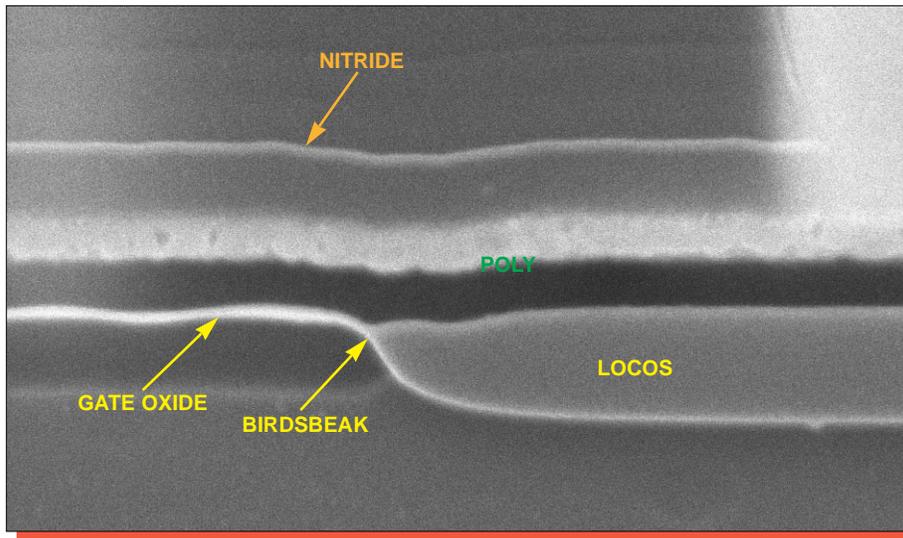
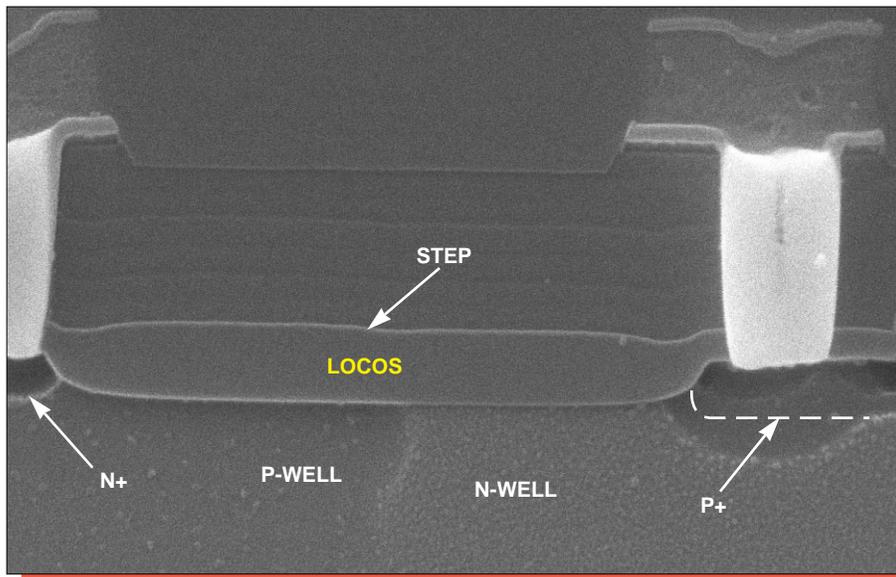
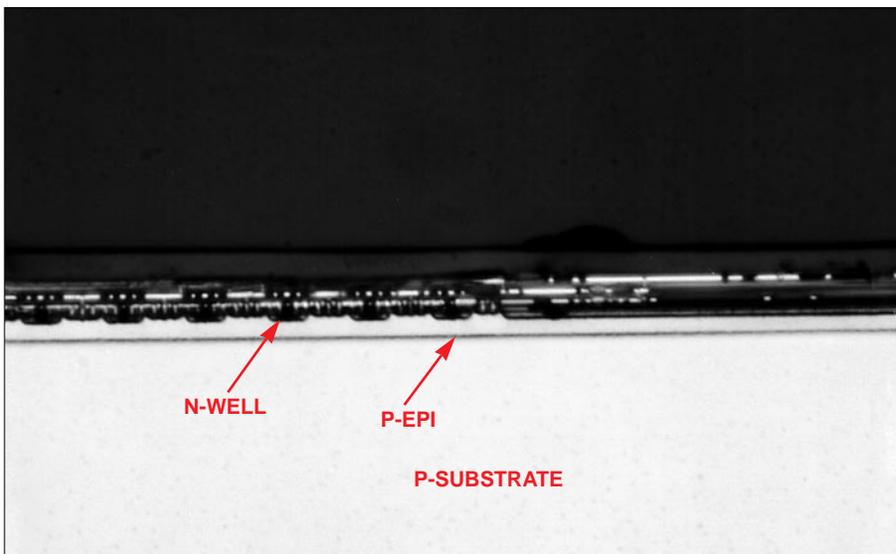


Figure 27. SEM section view of a local oxide birdsbeak. Mag. 52,000x.

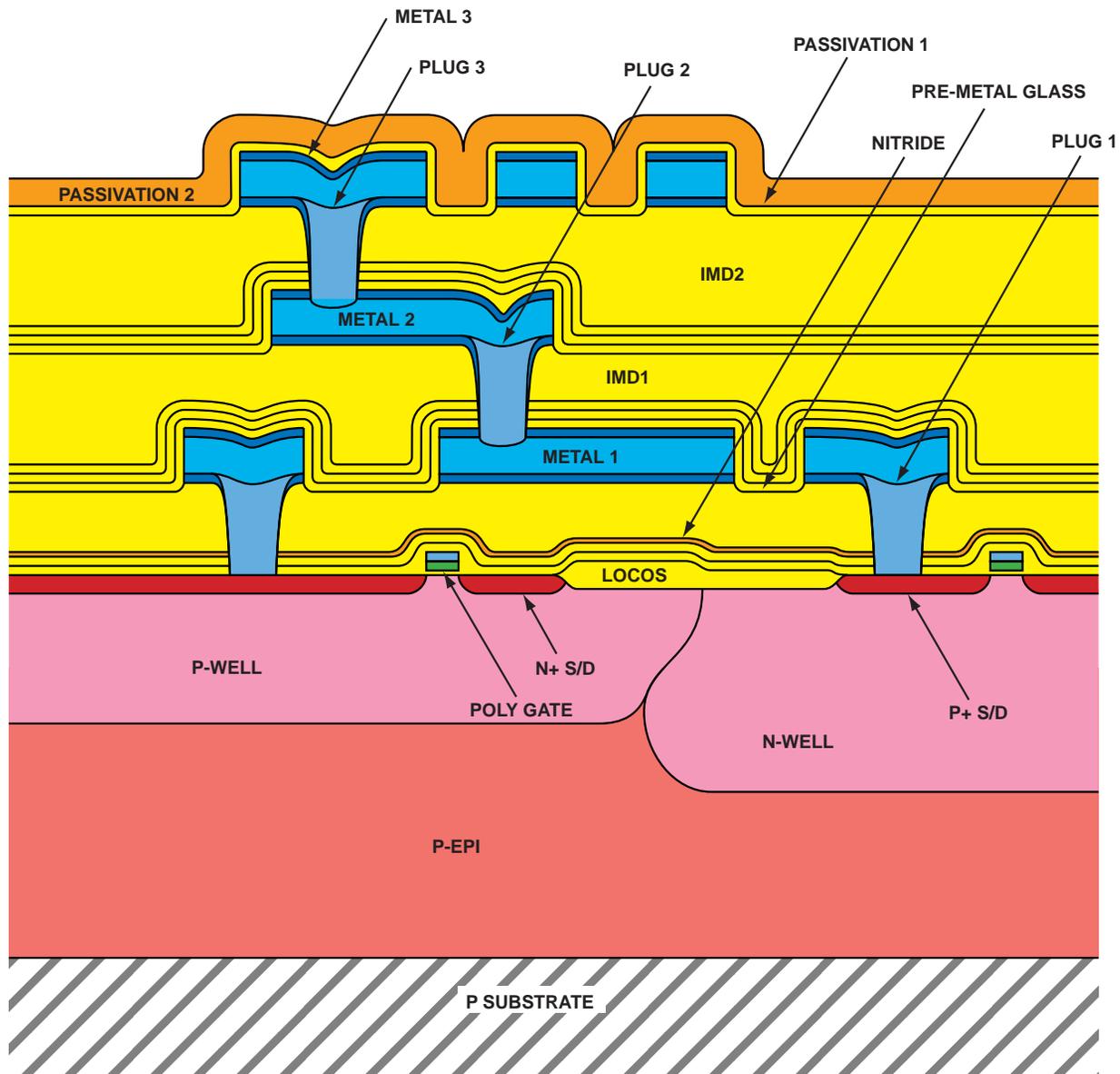


Mag. 26,000x



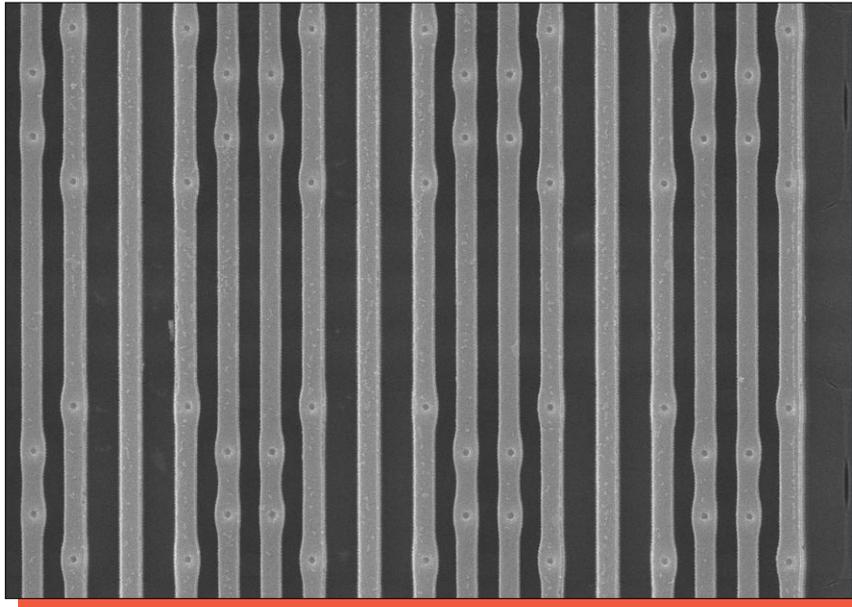
Mag. 800x

Figure 28. SEM and optical view of the well structure.

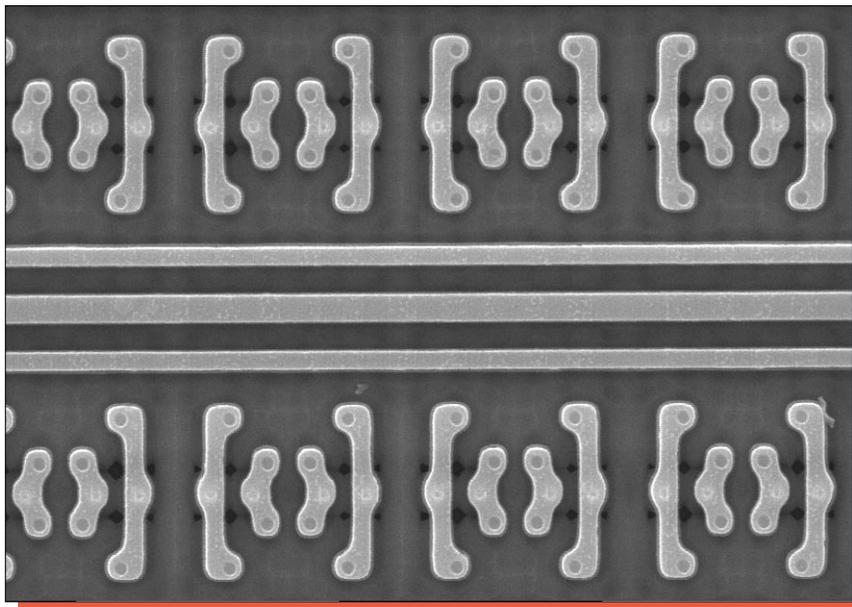


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

Figure 29. Color cross section drawing illustrating device structure.

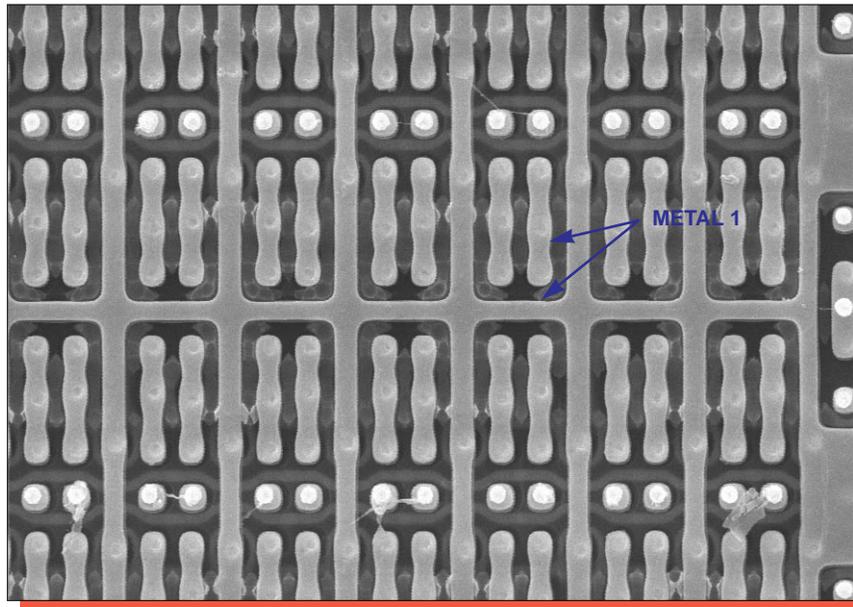


metal 3

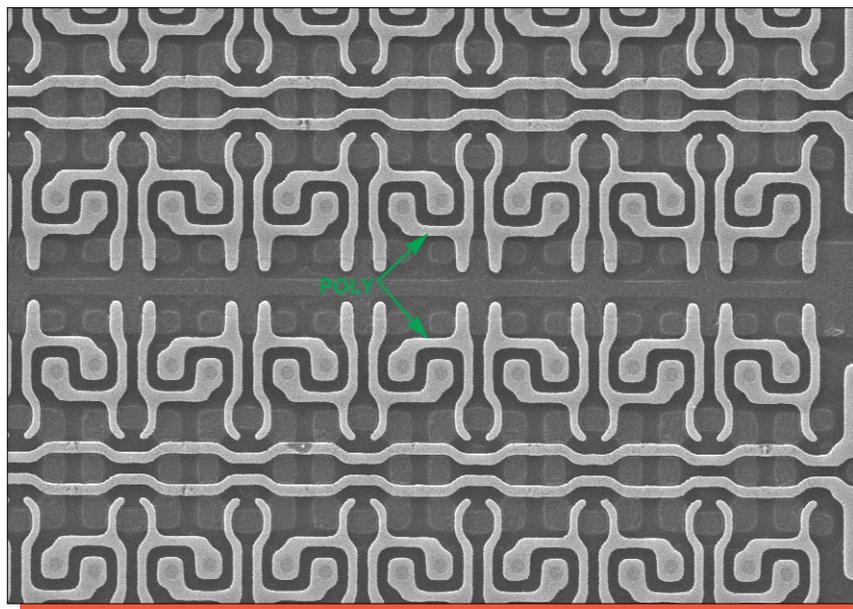


metal 2

Figure 30. Topological SEM views of the Cache memory array (Array A). Mag. 3500x, 0°.

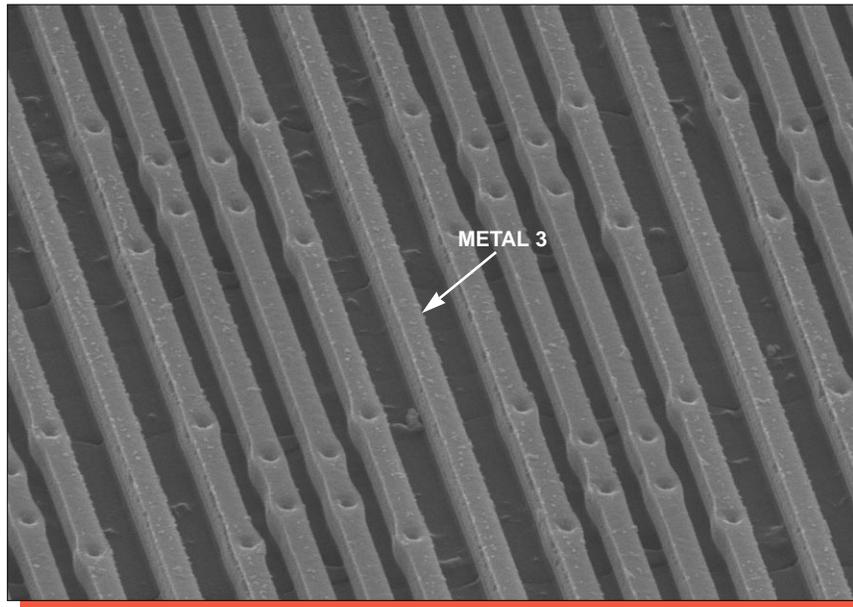


metal 1

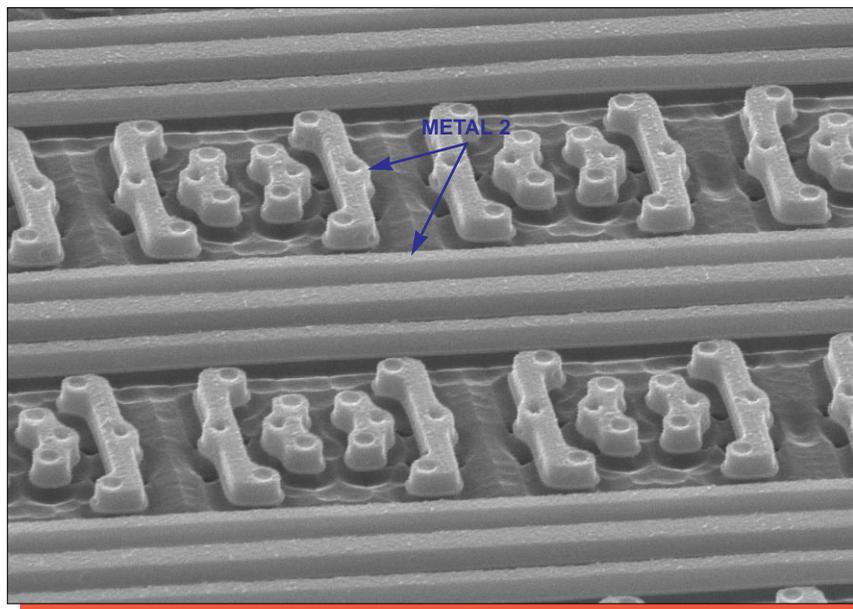


poly

Figure 30a. Topological SEM views of the Cache memory array (Array A).
Mag. 3500x, 0°.

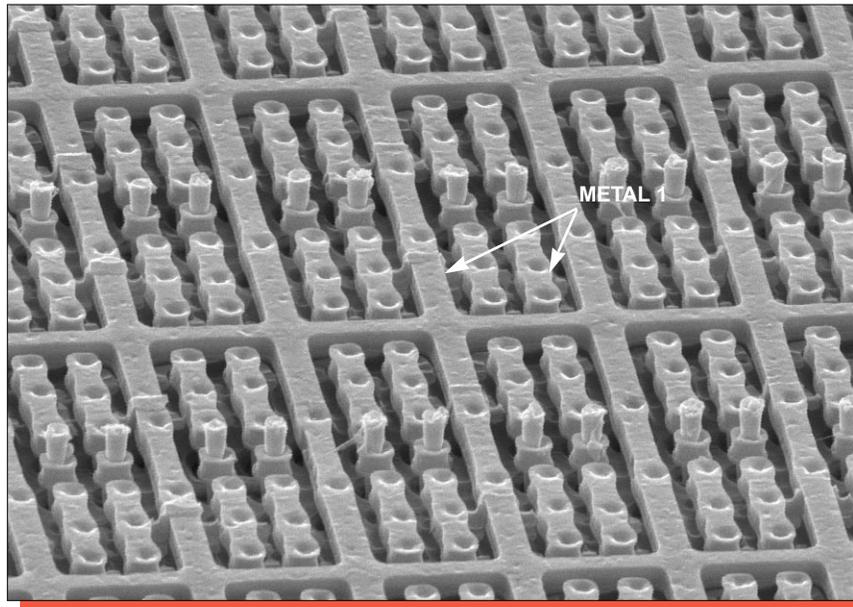


metal 3

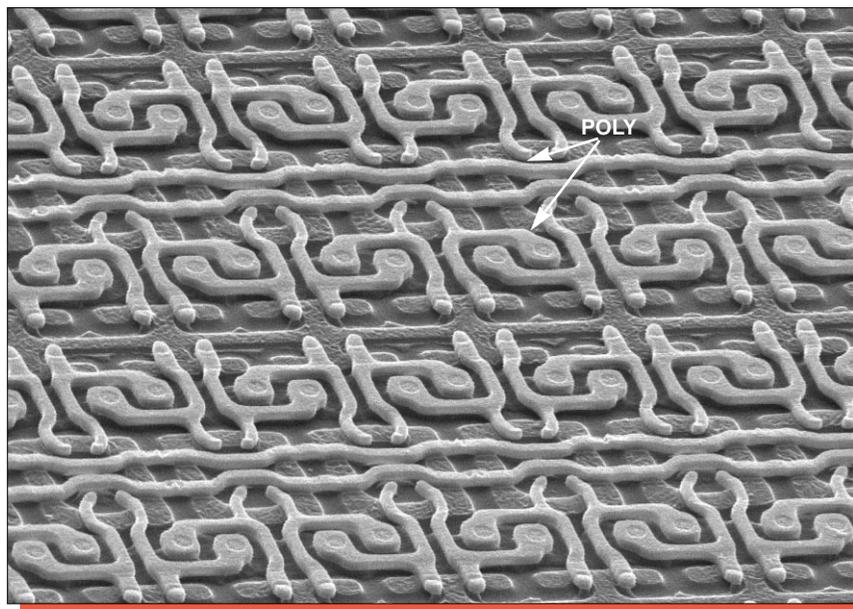


metal 2

Figure 31. Perspective SEM views of the Cache memory array (Array A).
Mag. 5000x, 60°.



metal 1



poly

Figure 31a. Perspective SEM views of the Cache memory array (Array A).
Mag. 5000x, 60°.

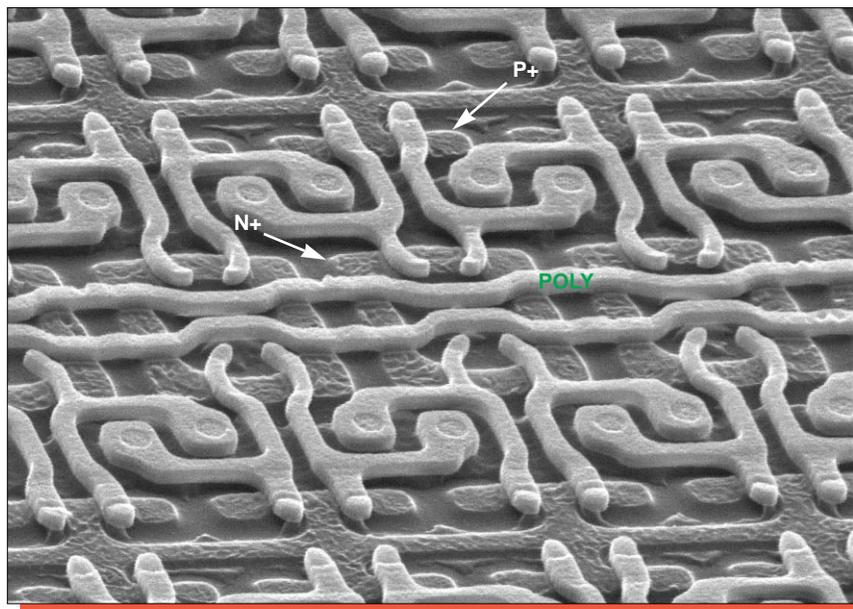
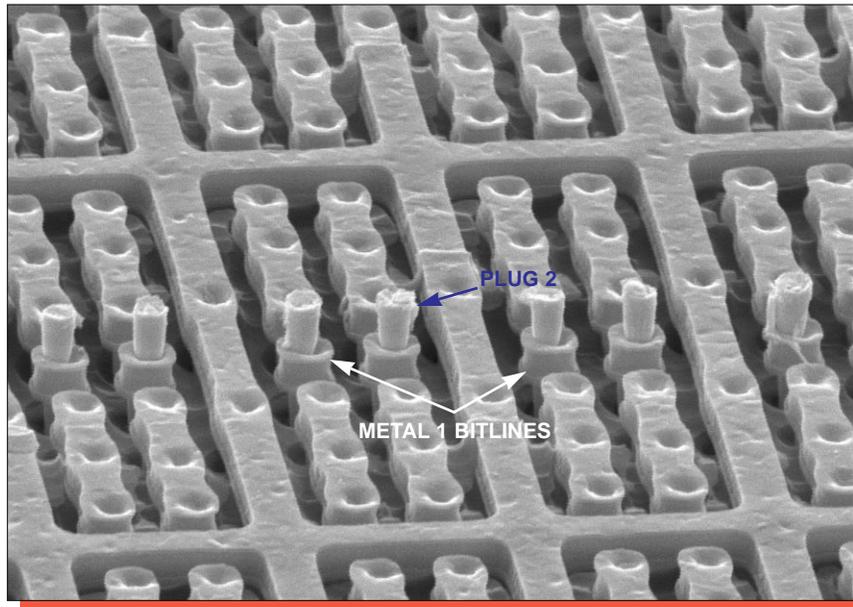
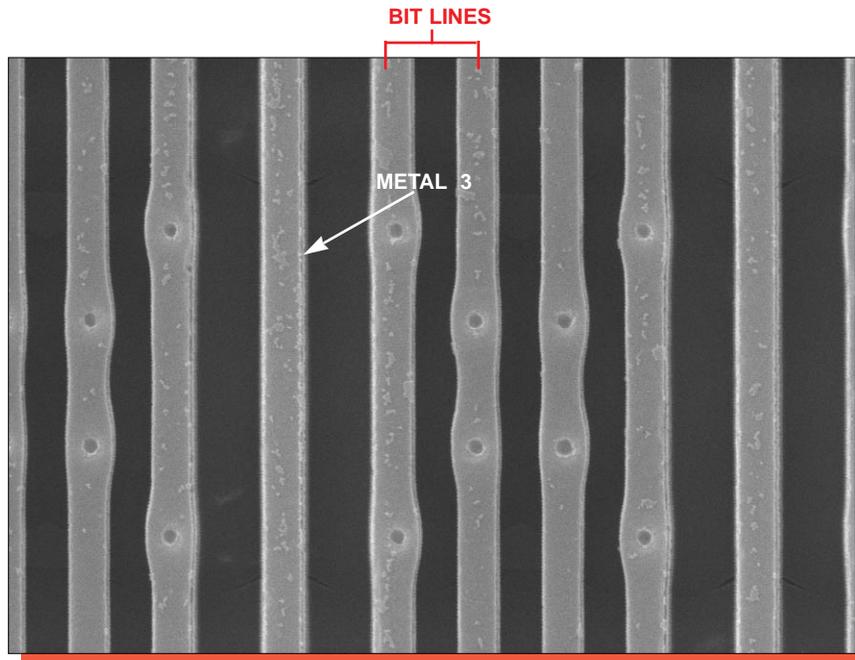
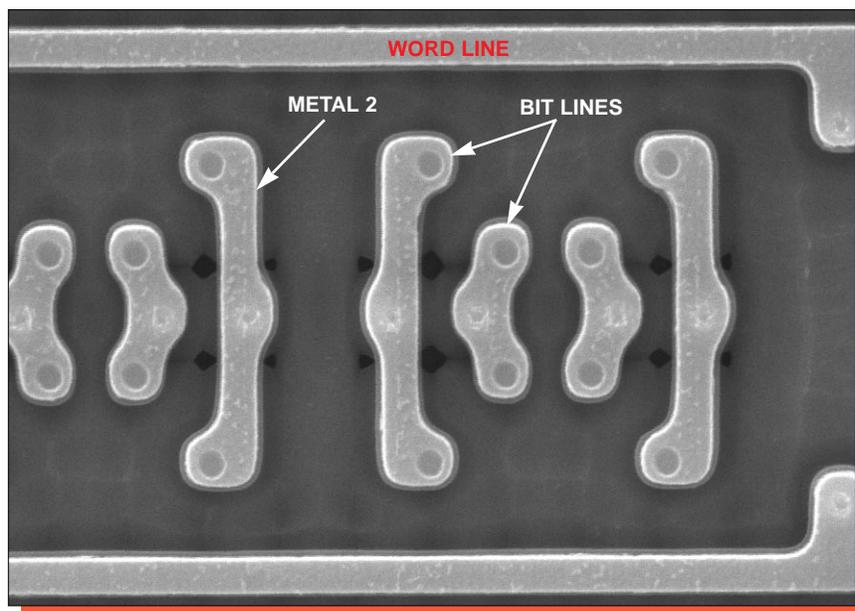


Figure 31b. Detailed SEM views of the Cache memory array (Array A). Mag. 8000x, 60°.

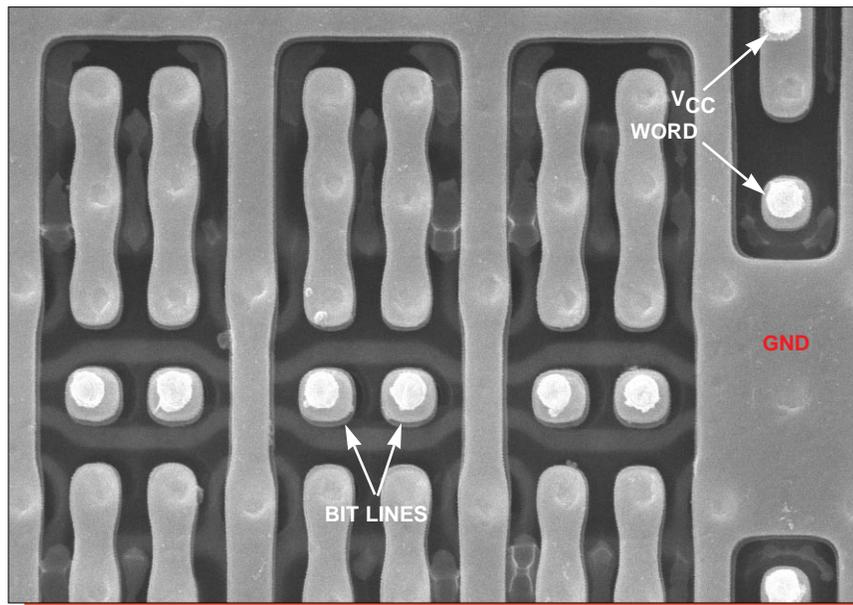


metal 3

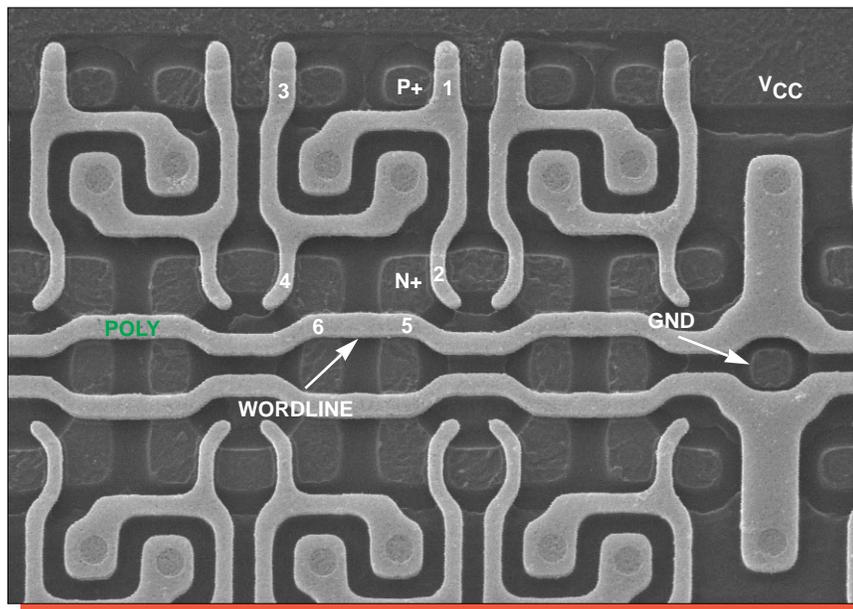


metal 2

Figure 32. Topological SEM views of the cell (Array A). Mag. 7000x, 0°.



metal 1



poly

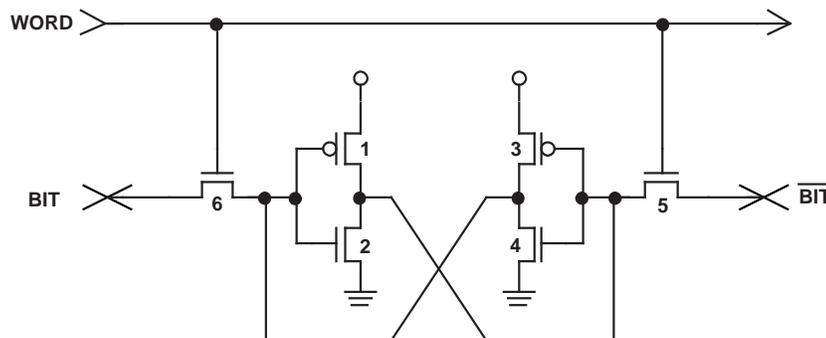
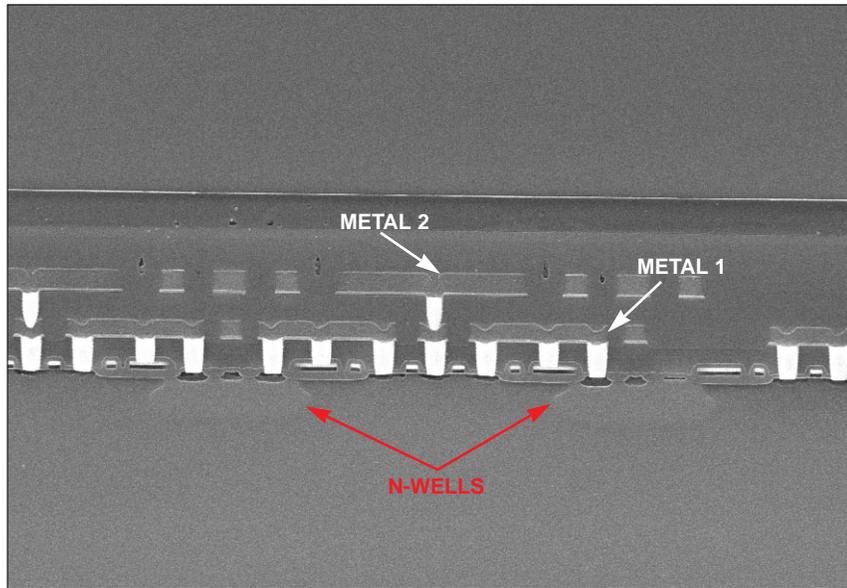
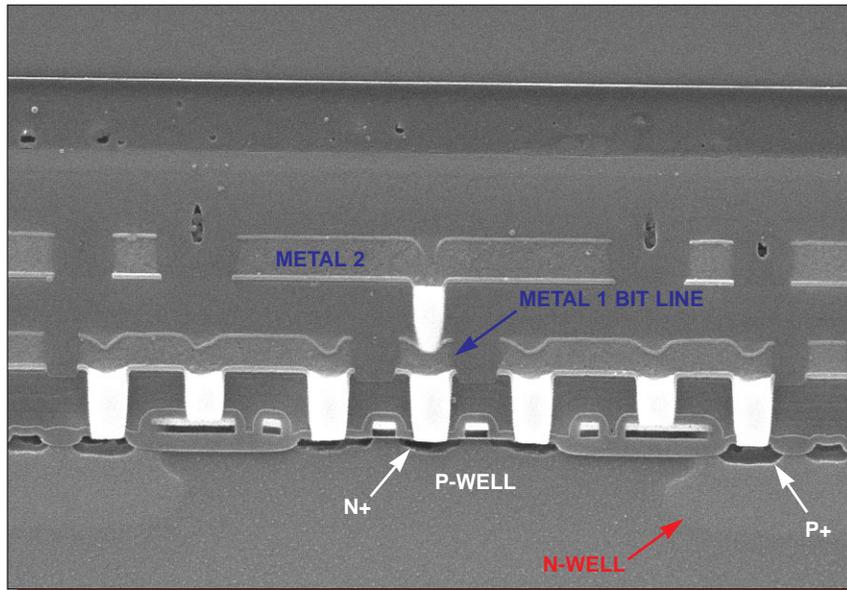


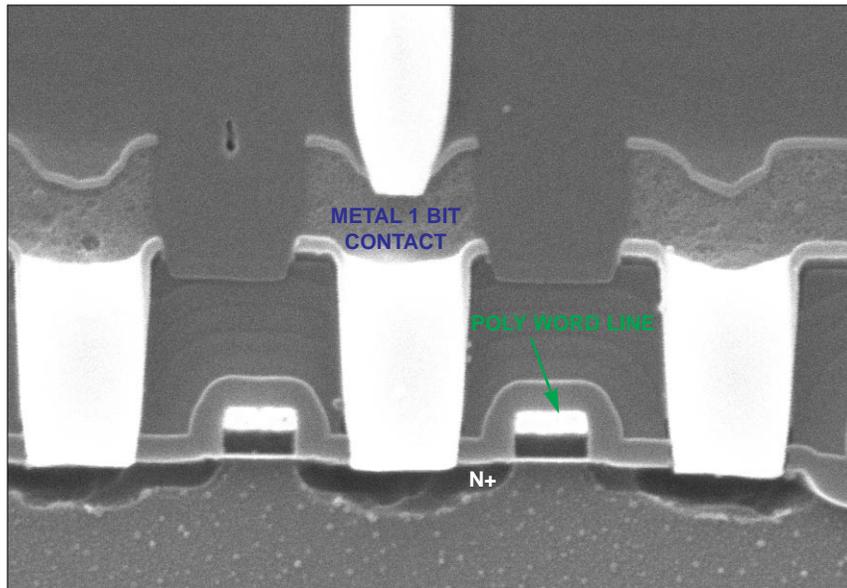
Figure 33. Topological SEM views of the cell along with the schematic (Array A).
Mag. 7000x, 0°.



Mag. 4000x

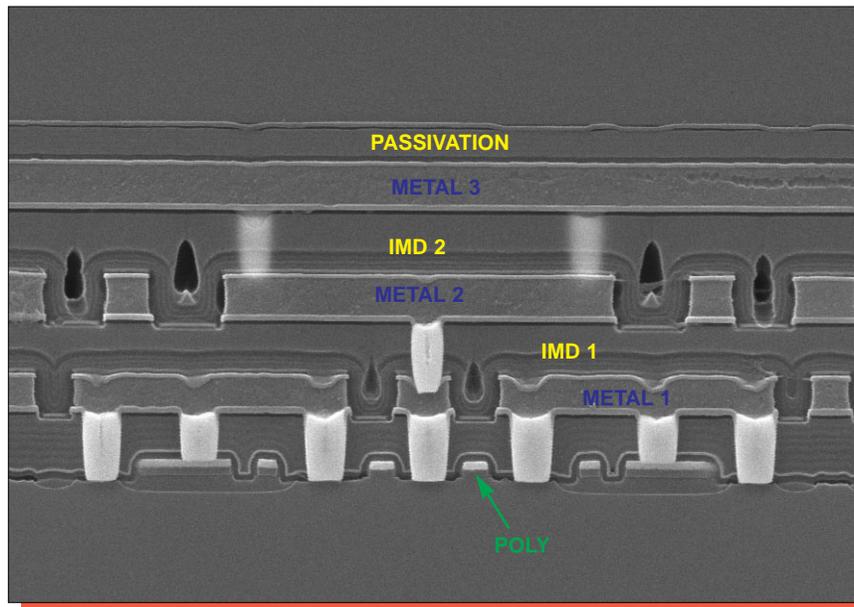


Mag. 8000x

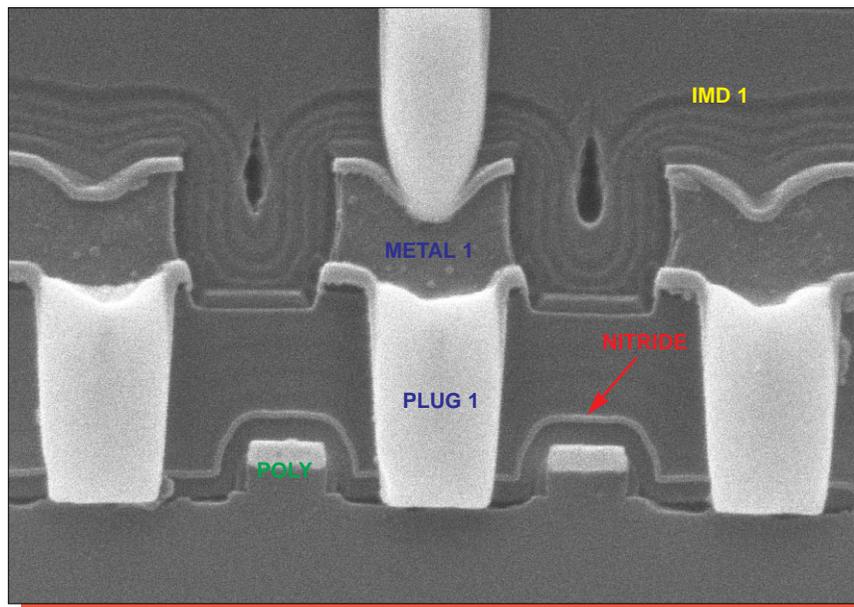


Mag. 26,000x

Figure 34. SEM section views of the Cache memory array (Array A).



Mag. 8000x



Mag. 26,000x

Figure 34a. SEM section views of the Cache memory cell (Array A). Glass-etch.

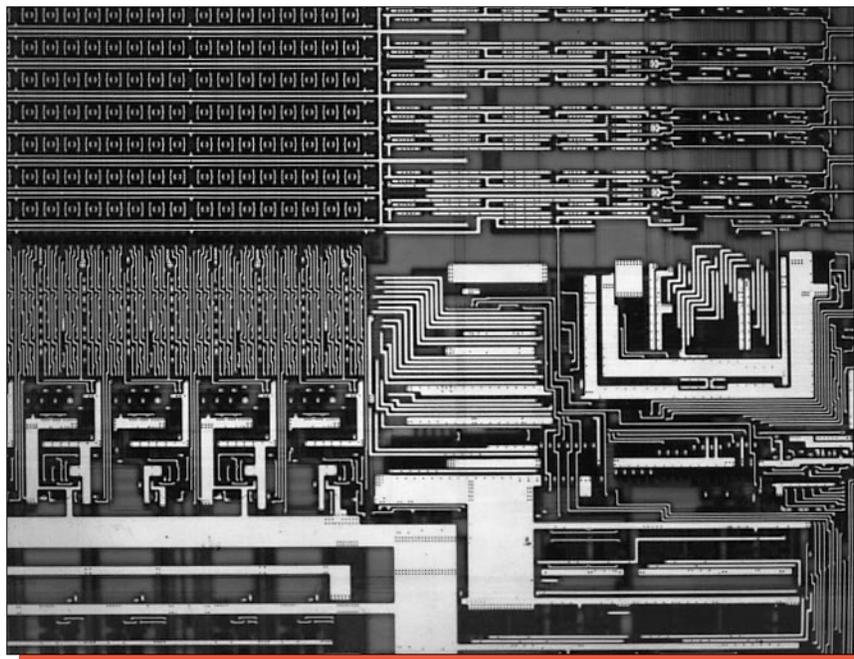
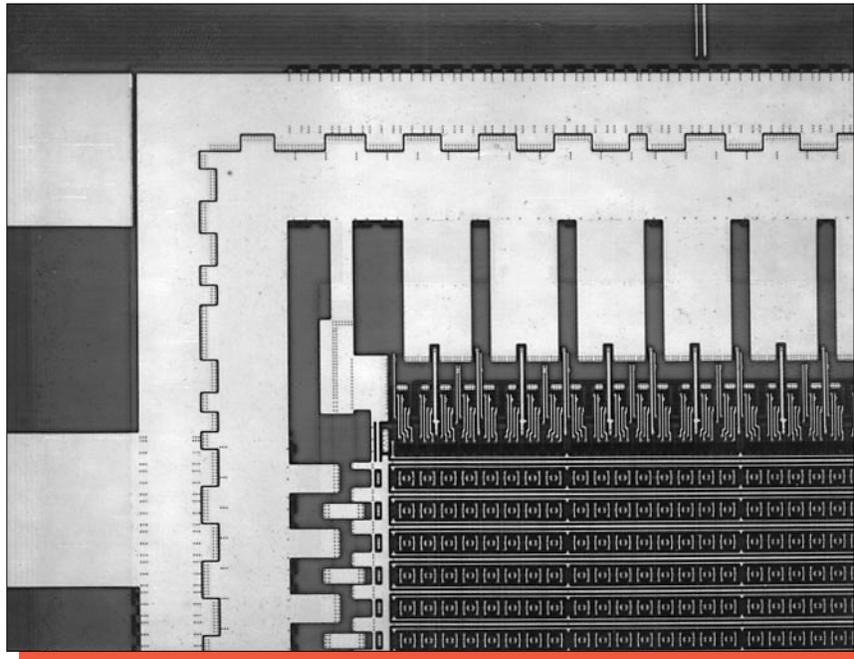
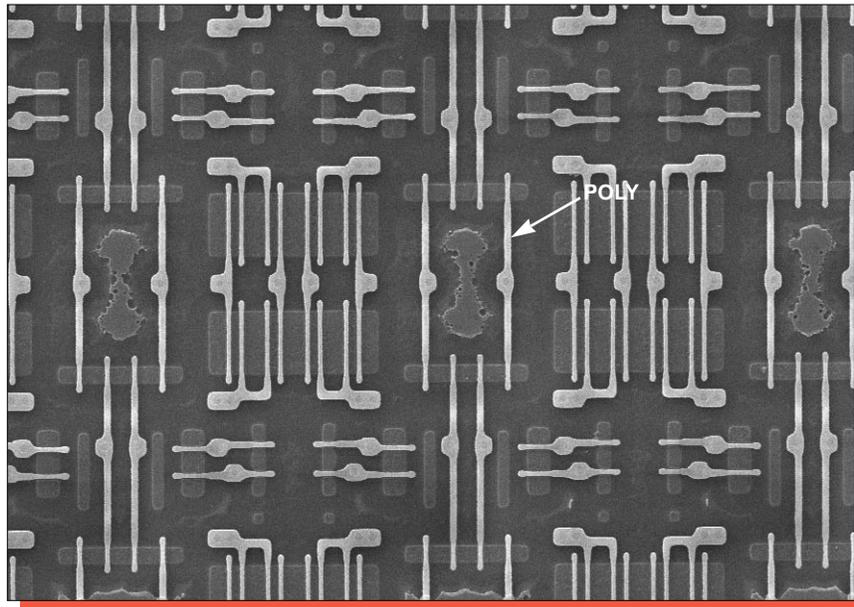
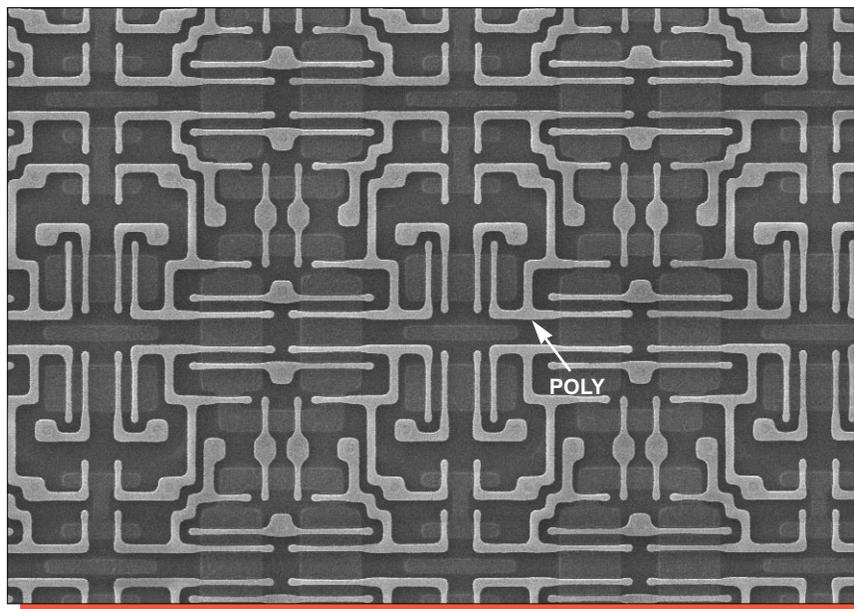


Figure 34b. Optical photographs illustrating metal 2 patterning along the edge of the Cache memory array (Array A). Mag. 320x.

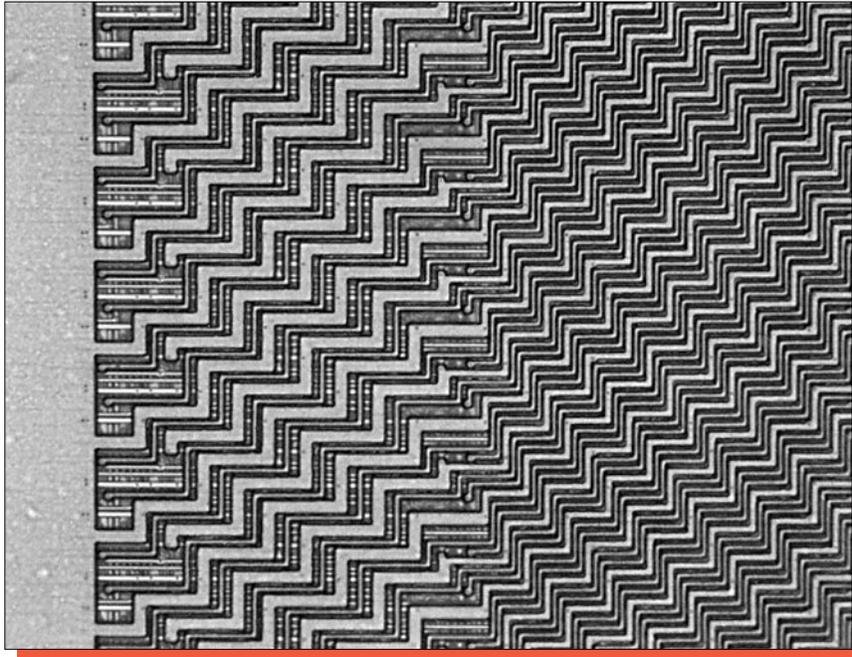


Mag. 2000x, Array B

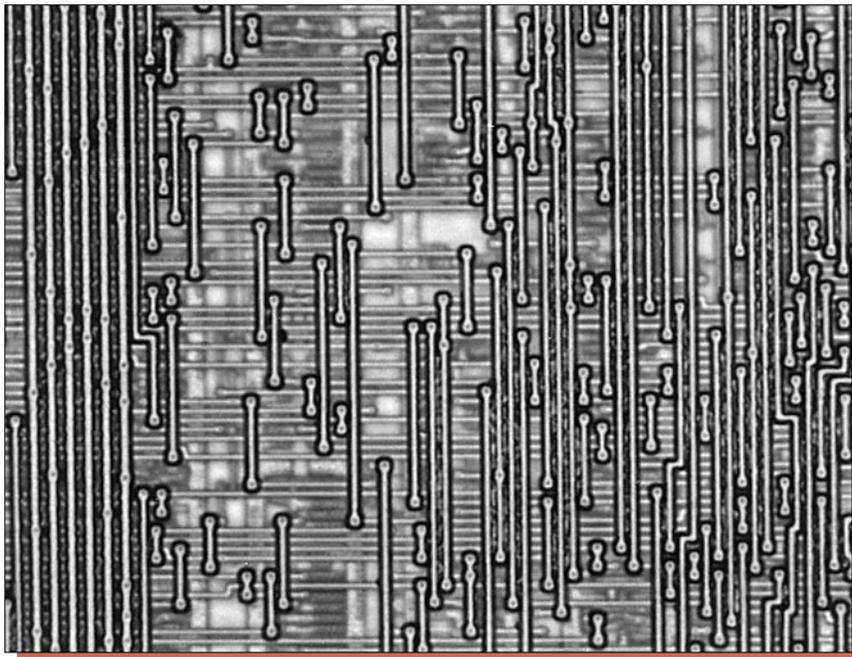


Mag. 2500x, Array C

Figure 35. Topological SEM views of additional cell arrays located on the NEC 79VR5000 RISC device.

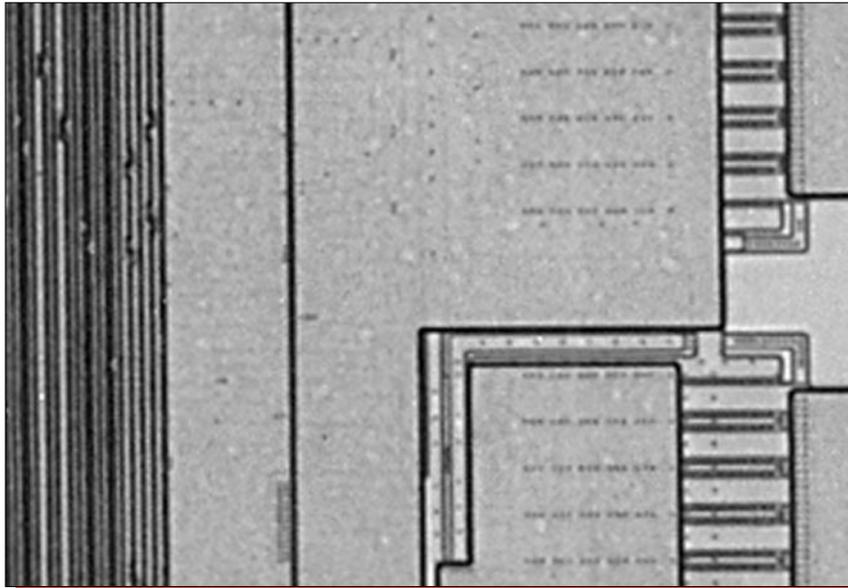


Mag. 500x

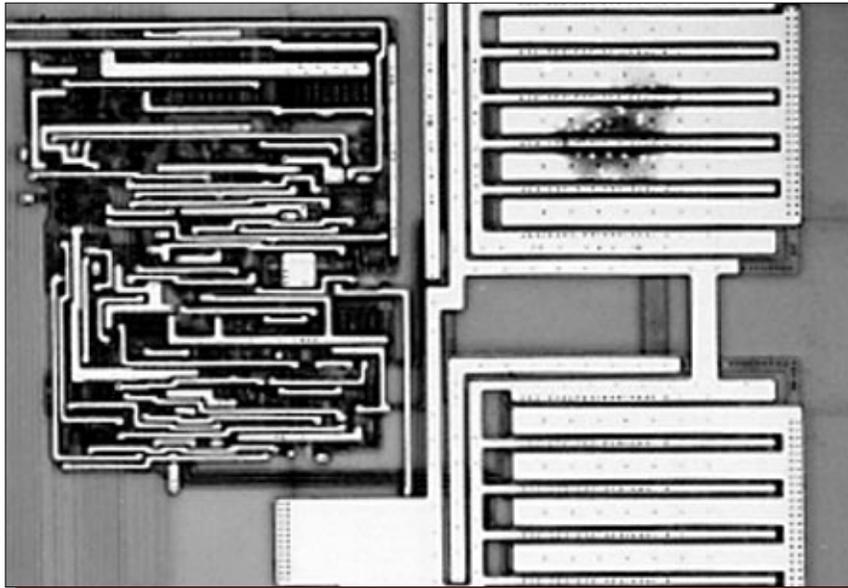


Mag. 800x

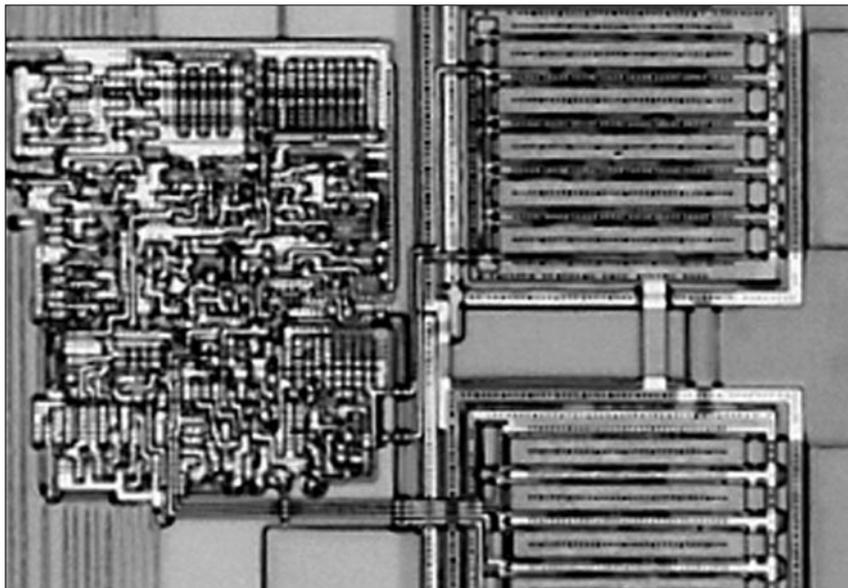
Figure 36. Optical photographs illustrating general circuitry layout. Intact.



intact



metal 2



metal 1

Figure 37. Optical views of typical input/output layout. Mag. 480x.