

## Construction Analysis

# Motorola MC68360EM25VC Communication Controller

Report Number: SCA 9711-562



**INTEGRATED CIRCUIT ENGINEERING**

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## **INTRODUCTION**

This report describes a construction analysis of the Motorola MC68360EM25VC Communication Controller. Four samples were supplied for the analysis. The devices were received in 240-pin PQFPs (Plastic Quad Flat Packs) date coded 9710.

## **MAJOR FINDINGS**

### **Questionable Items:<sup>1</sup>**

- Metal 2 thinned up to 80 percent<sup>2</sup> at vias (Figure 22).

**Special Features:** None.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## **TECHNOLOGY DESCRIPTION**

### **Assembly**

- The devices were packaged in 240-pin Plastic Quad Flat Packs (PQFP) with gull-wing leads.
- The leadframe was constructed of copper and externally tinned with lead-tin solder.
- The die was mounted cavity down on a dimpled header. The edges (and a portion on top) of the header and the internal leadframe were plated with silver.
- Die attach was by silver-epoxy.
- Thermosonic ball bonds using 1.2 mil gold wire. Four pins were not connected.
- Sawn dicing (full depth).

### **Die Process:**

- Fabrication process: Selective oxide isolation, CMOS process employing twin wells in P substrate.
- Die coat: No die coat was used.
- Final passivation: A layer of silicon-nitride over a layer of glass.
- Metallization: Three levels of metal defined by dry-etch techniques. All metals consisted of aluminum with titanium-nitride caps. Metal 1 also employed a titanium-nitride barrier. Standard vias and contacts were employed (no plugs).
- Interlevel dielectrics: Interlevel dielectrics 1 and 2 used the same dielectric structure. A thick glass was deposited first, followed by another layer of glass. The first layer of deposited glass was subjected to an etchback. No spin on glass or CMP planarization was used.

## **TECHNOLOGY DESCRIPTION (continued)**

- Pre-metal glass: A thick layer of BPSG over densified oxides. This glass was reflowed prior to contact cuts.
- Polysilicon: A single layer of dry-etched poly. This layer was used to form all gates on the die. Nitride sidewall spacers were used to provide the LDD spacing. No buried contacts were employed.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. No silicide was used on the diffusions.
- Isolation: Local oxide isolation. A step was noted in the oxide at well boundaries.
- Wells: Twin-wells in a P substrate. The step in the oxide at the well boundaries indicates a twin-well process was employed.
- Memory cells: Two types of MROMs were present on the device (see Figures 34-37). Metal 1 formed the bit lines and poly formed the word lines. Both were programmed at the LOCOS level; however, Array B also appeared to be programmed at the contact cut level. A 6T SRAM array was employed as well as a 8T SRAM array (see Figures 38-40). Metal 2 formed the bit lines and distributed GND throughout the 6T cells. Metal 1 distributed Vcc and provided cell interconnect. Poly formed the word lines. Documentation of the metal layout on the 8T cell was not available for SEM photography.
- No redundancy fuses were found.

## ANALYSIS RESULTS

**Assembly:**

**Figures 1 - 9**

**Questionable Items:**<sup>1</sup> None.

**Special Features:** None.

**General Items:**

- Overall package quality: The devices were packaged in 240-pin Plastic Quad Flat Packs (PQFP) with gull-wing leads. No defects were noted on the external or internal portions of the package.
- Leadframe: The leadframe was constructed of copper. The gull-wing leads were well formed and the external tin-lead solder tinning was complete. No gaps were noted at lead exits. The die was mounted cavity down on a dimpled leader. The internal leadframe and the edges (and a portion of the top) of the header were plated with silver.
- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. Bond pad pitch was relatively tight (136 microns); however, wire spacing was good and no problems were seen. Intermetallic formation was adequate at ball bonds. Wire pull strengths were normal; however, one bond lift was noted on each sample. Both bond lifts had part of the pad metal still adhered to the bond which indicates good adhesion (intermetallic) between the bond and the pad, so no problems are foreseen.
- Die attach: The die was mounted to the underside of the header with silver-epoxy die attach. Some excessive epoxy was noted at the edges of the attach; however, overall quality was normal with no voids noted.
- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## ANALYSIS RESULTS II

### Die Process and Design:

Figures 10 - 40

#### **Questionable Items:**<sup>1</sup>

- Metal 2 thinned up to 80 percent<sup>2</sup> at vias (Figure 22).

**Special Features:** None.

#### **General Items:**

- Fabrication process: Selective oxide isolation, CMOS process employing twin-wells in P substrate. No problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A layer of nitride over a layer of glass. Coverage was good and no defects were noted. Edge seal was also good as the passivation extended to the scribe lane to seal the metallization. A cutout was present at the die edge to prevent cracks from radiating inward over the active circuitry.
- Metallization: Three levels of metal interconnect. All metals consisted of aluminum with titanium-nitride caps. Metal 1 also employed a titanium-nitride barrier. Standard vias and contacts were used (no plugs).

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## **ANALYSIS RESULTS II (continued)**

- Metal patterning: All metal levels were defined by a dry etch of good quality. Metal lines were widened at via and contact connections (all levels).
- Metal defects: None. No voiding, notching or cracking of the metal layers. No silicon nodules were found following removal of the metal layers.
- Metal step coverage: Metal 3 (including cap) thinned up to 75 percent at vias and metal 2 (including cap) thinned up to 80 percent at vias. Although the thinning exceeds MIL-STDs (70 percent) it is probably not considered a serious reliability concern. Metal 1 (including cap and barrier) thinning was 65 percent at contacts.
- Vias and contacts: All via and contact cuts were defined by a two step etch. The cap metal was cleared at via sites for adhesion purposes and no significant over etching of the contacts was noted. Vias and contacts were completely surrounded by metal.
- Metal patterning: All metal levels were defined by a dry etch of good quality. Metal lines were widened at via and contact connections (all levels).
- Interlevel dielectrics: Interlevel dielectrics 1 and 2 consisted of the same type of oxide structure. A very thick glass was deposited first, followed by another layer of glass. The first layer was subjected to an etchback. No SOG or CMP planarization was used. No problems were found with any of these layers.
- Pre-metal glass: A thick layer of BPSG over densified oxides. The BPSG was reflowed prior to contact cuts. No problems were found.
- Polysilicon: A single layer of dry etched poly was used. It formed all gates and word lines in the arrays. Definition was by dry etch of good quality. It appears that the poly was deposited in two layers which is evident by the small oxide remnants when the poly was etched out in cross section (see Figures 29 and 30). Nitride sidewall spacers were used throughout and left in place. No problems were found.
- Isolation: The device used local oxide isolation. No problems were present at the birdsbeaks or elsewhere.

## **ANALYSIS RESULTS II (continued)**

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Diffusions were not silicided (salicide process). As mentioned, an LDD process was used employing nitride sidewall spacers.
- Wells: Twin-wells were used in a P substrate. Definition was normal. We could not delineate the P-well in section; however, the step in the oxide indicates a twin-well process was employed.
- Buried contacts: Direct poly to diffusion contacts were not used.
- Memory cells: Two types of MROM arrays were present on the device (see Figures 34-37). Metal 1 formed the bit lines and poly formed the word lines. Both were programmed at the LOCOS level; however, Array B also appeared to be programmed at the contact cut level. A 6T SRAM array was employed as well as a 8T SRAM array (see Figures 38-40). Metal 2 formed the bit lines and distributed GND throughout the 6T cells. Metal 1 distributed Vcc and provided cell interconnect. Poly formed the word lines. Documentation of the metal layout on the 8T cell was not available for SEM photography.
- No redundancy fuses were noted.

### **Special Items:**

- ESD sensitivity test: One sample was subjected to an ESD test which revealed all pins tested pass  $\pm 4000V$  pulses.

## **PROCEDURE**

The devices were subjected to the following analysis procedures:

External inspection

X-ray

ESD test

Package section and EDX

Die optical inspection

SEM assembly features and passivation

Passivation integrity test

Wirepull test

Delayer to metal 3 and inspect

Delayer to metal 2 and inspect

Delayer to metal 1 and inspect

Delayer to poly substrate and inspect

Die sectioning (90° for SEM)

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wirebond spacing	G
Wirebond quality	N
Dicing quality	N
Die attach quality	N
Die attach method	Silver epoxy
Dicing method	Sawn
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Via/contact registration	N

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

*\*Metal 2 thinning up to 80 percent.*

## PACKAGE MARKINGS

### TOP

(Logo)  
MC68360EM25VC  
2E68C 1EAD9710 Korea

### BOTTOM

Molded markings

## WIREBOND STRENGTH

Wire material: 1.2 mil diameter

Die pad material: Aluminum

Material at package land: Silver

Sample #	<u>1</u>	<u>2</u>
# of wires tested:	55	30
Bond lifts:	1	1
Force to break		
- high:	13.5 g	13 g
- low:	9 g	10 g
- average:	11.2 g	10.9 g
- std. dev.:	1.3	0.9

## **DIE MATERIAL ANALYSIS**

Final passivation:	Single layer of silicon-nitride* over a glass layer.
Metals 2 and 3:	Aluminum with a titanium-nitride cap.
Interlevel dielectrics 1 and 2:	A thick layer of glass followed by another layer of glass.
Metal 1:	Aluminum with a titanium-nitride cap and barrier.
Pre-metal glass:*	A CVD glass containing 7.6 wt. percent phosphorus and 3.2 wt. percent boron.

\**WDX analysis*

## **PACKAGE MATERIALS**

Leadframe:	Copper (Cu)
External tinning:	Tin-lead (SnPb) solder
Internal plating:	Silver (Ag)
Die attach:	Silver (Ag) epoxy



## VERTICAL DIMENSIONS

Die thickness: 0.3 mm (13 mils)

### Layers:

Passivation 2:	0.65 micron
Passivation 1:	0.35 micron
Metal 3 - cap:	0.05 micron
- aluminum:	1.0 micron
Interlevel dielectric 2 - glass 2:	0.25 - 0.4 micron
- glass 1:	0.5 - 1.4 micron
Metal 2 - cap:	0.05 micron
- aluminum:	0.8 micron
Interlevel dielectric 1 - glass 2:	0.4 micron
- glass 1:	0.4 - 1.5 micron
Metal 1 - cap:	0.05 micron
- aluminum:	0.55 micron
- barrier:	0.1 micron
Pre-metal glass:	0.8 micron
Poly:	0.25 micron
Oxide over poly:	0.2 micron
Local Oxide:	0.55 micron
N+ S/D:	0.2 micron
P+ S/D:	0.2 micron
N-well:	6.5 micron

## INDEX TO FIGURES

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PHYSICAL DIE STRUCTURES	Figures 13 - 40
COLOR DRAWING OF DIE STRUCTURE	Figure 33
MEMORY CELLS	Figures 34 - 40

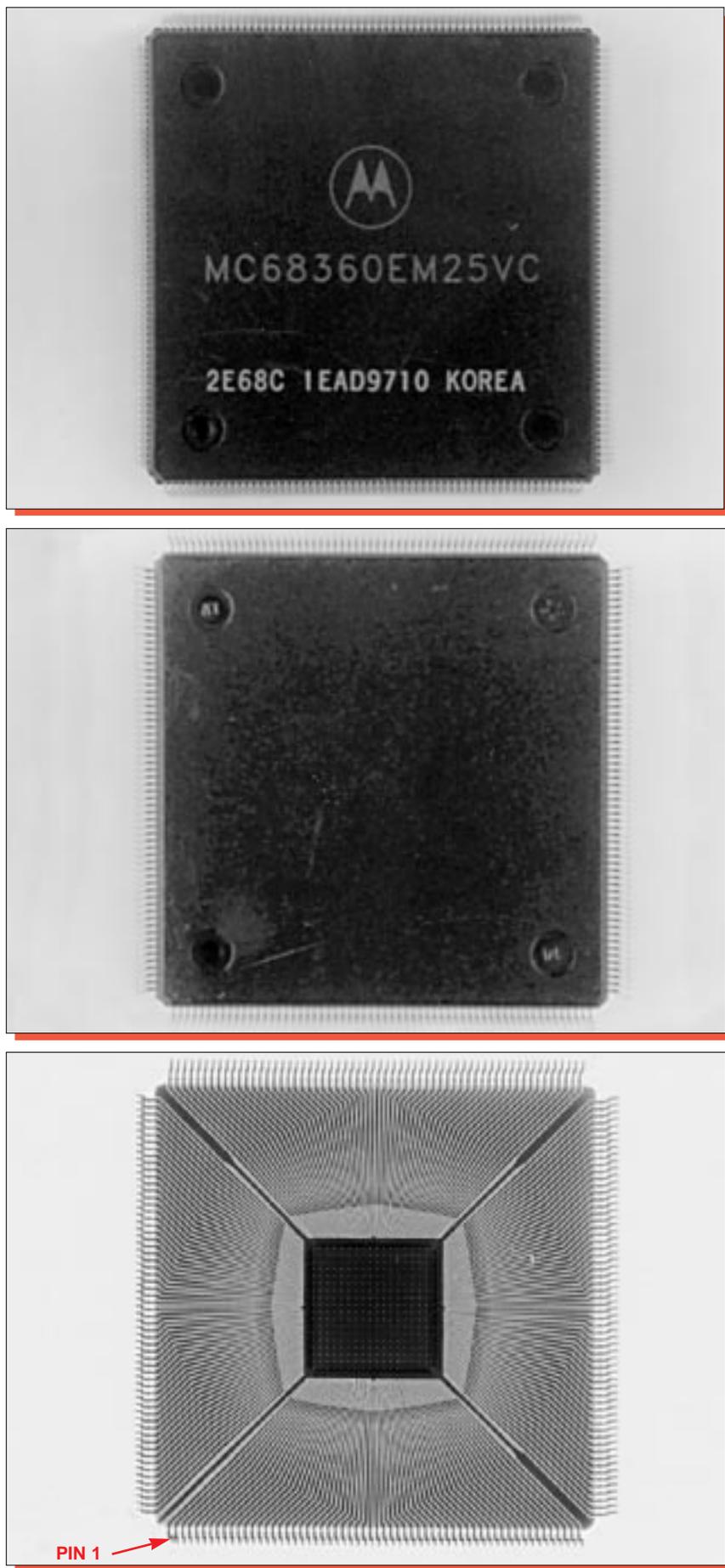
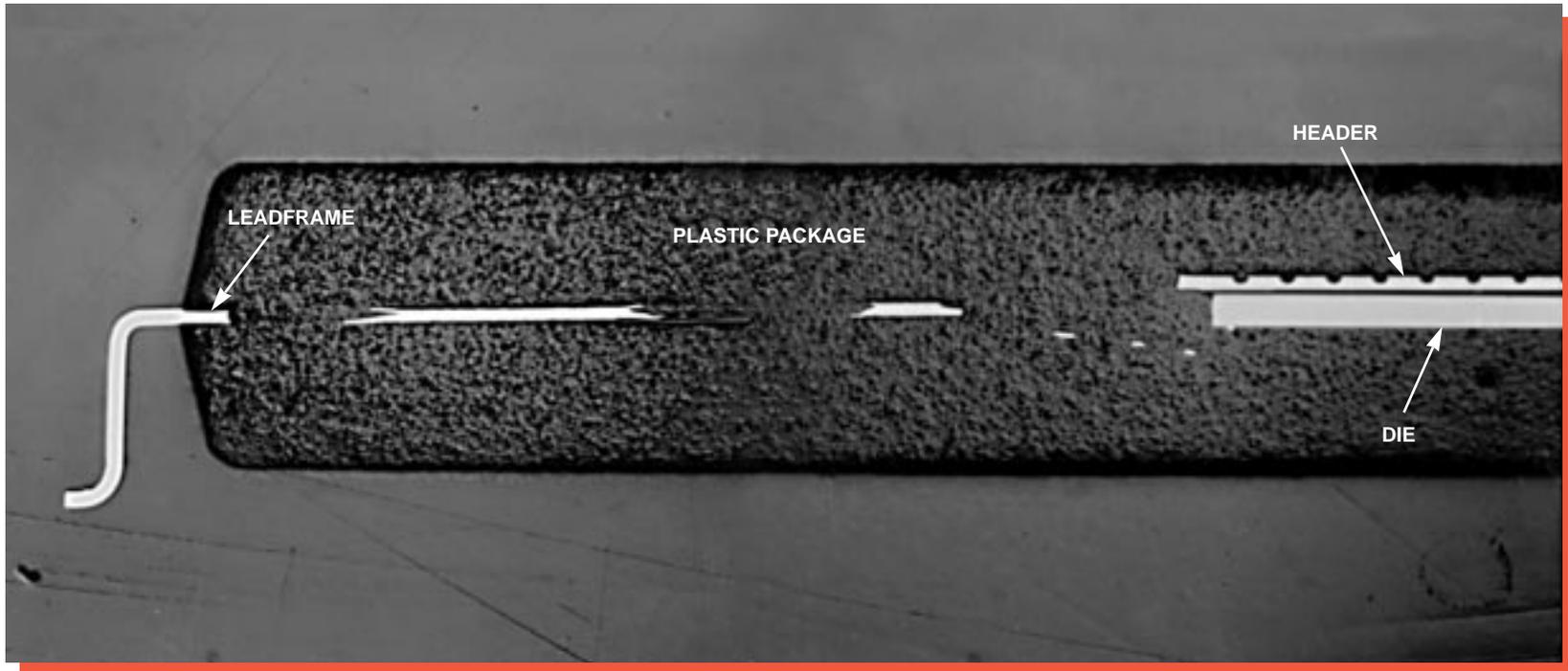
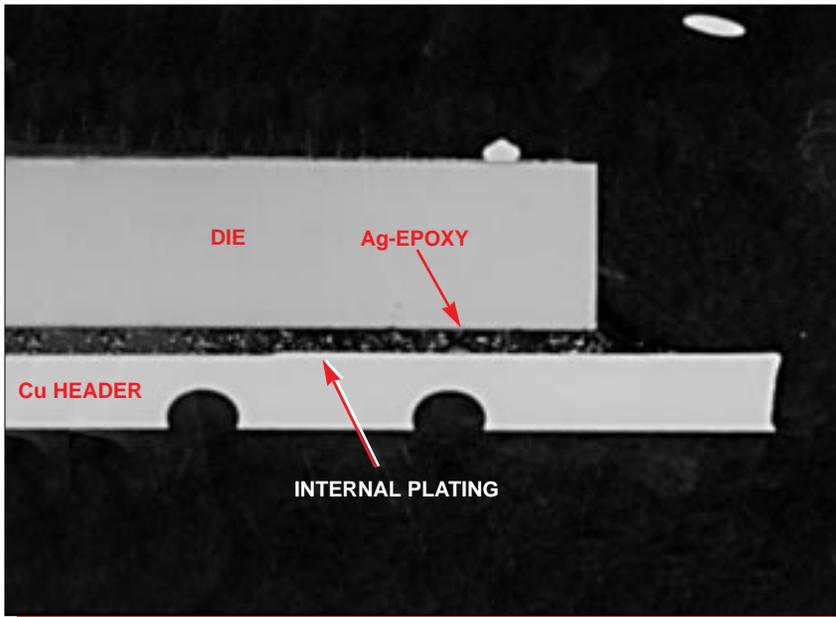


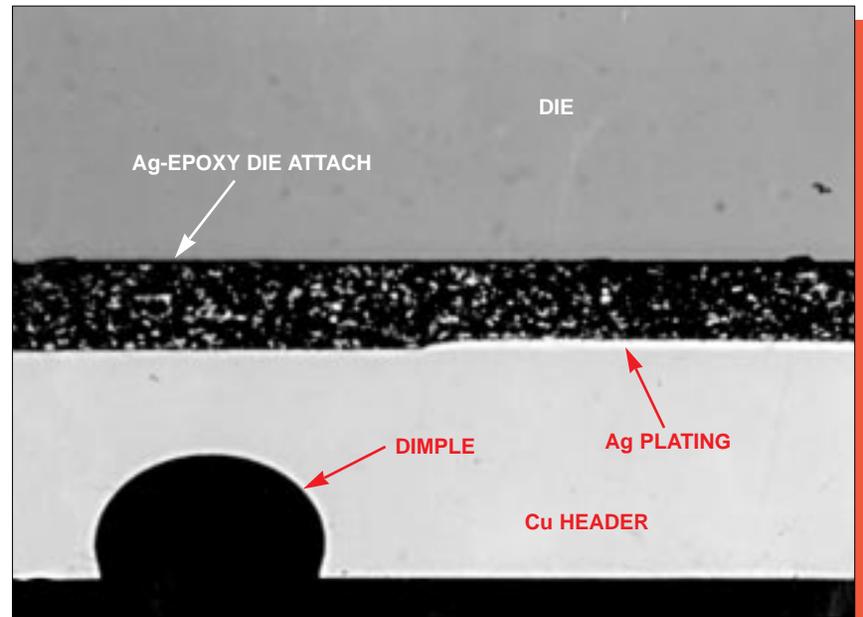
Figure 1. Package photographs and x-ray of the Motorola MC68360. Mag. 2.2x.



Mag. 12x

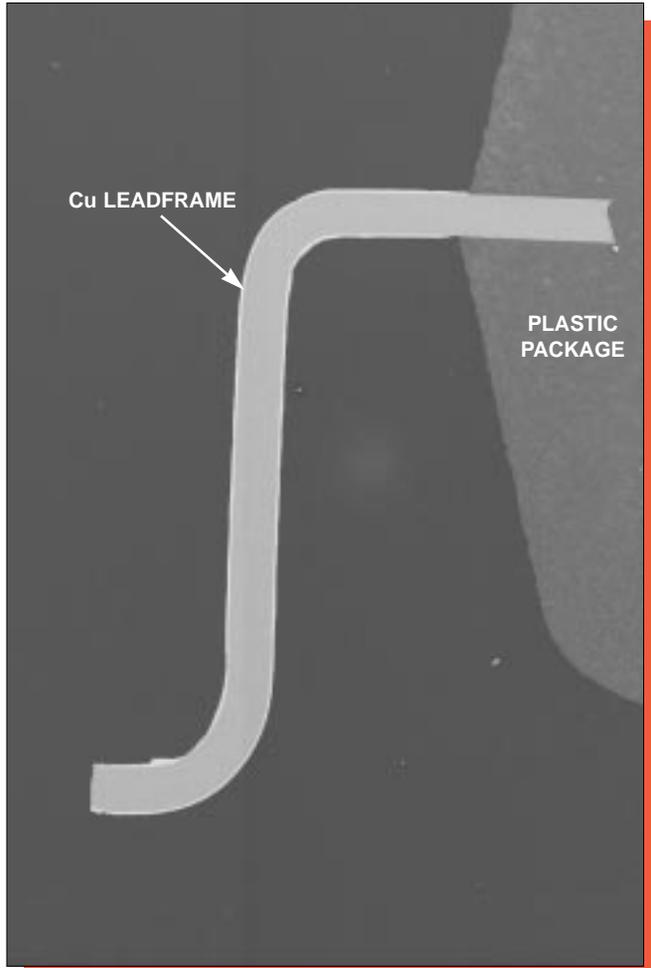


Mag. 65x

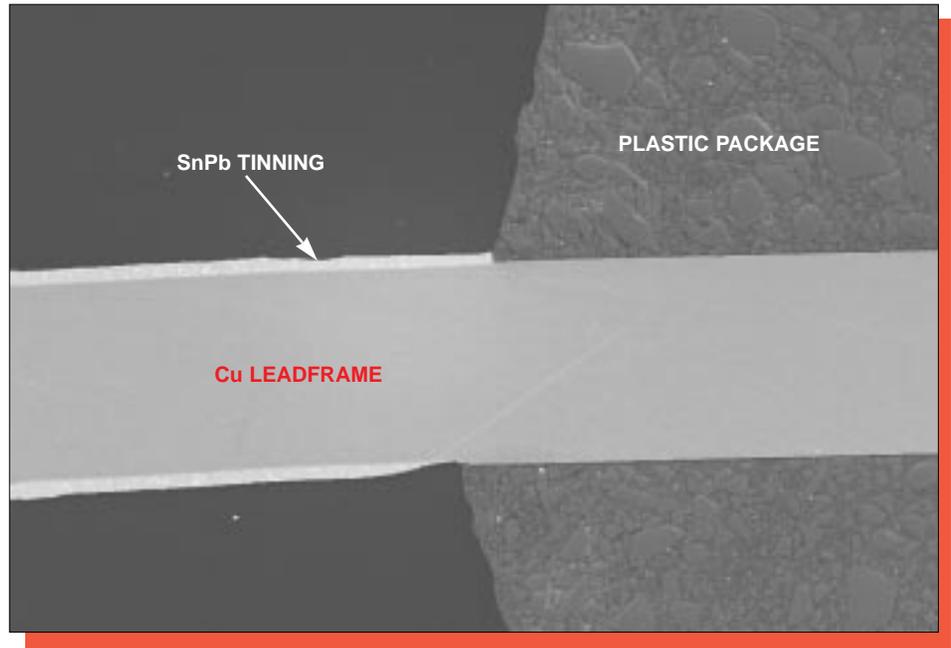


Mag. 200x

Figure 2. Optical section views illustrating general package construction.



Mag. 40x



Mag. 185x

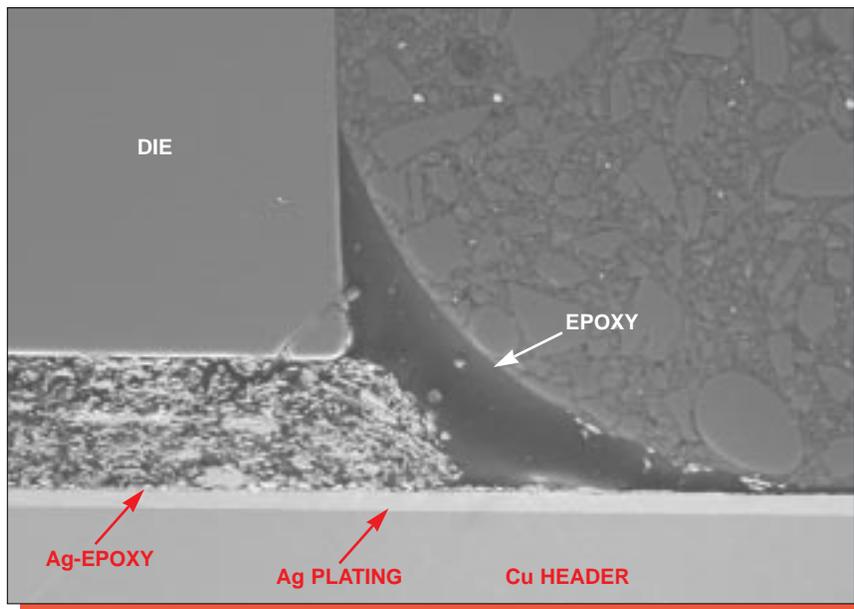


Mag. 750x

Figure 3. SEM section views illustrating lead forming and lead exit.

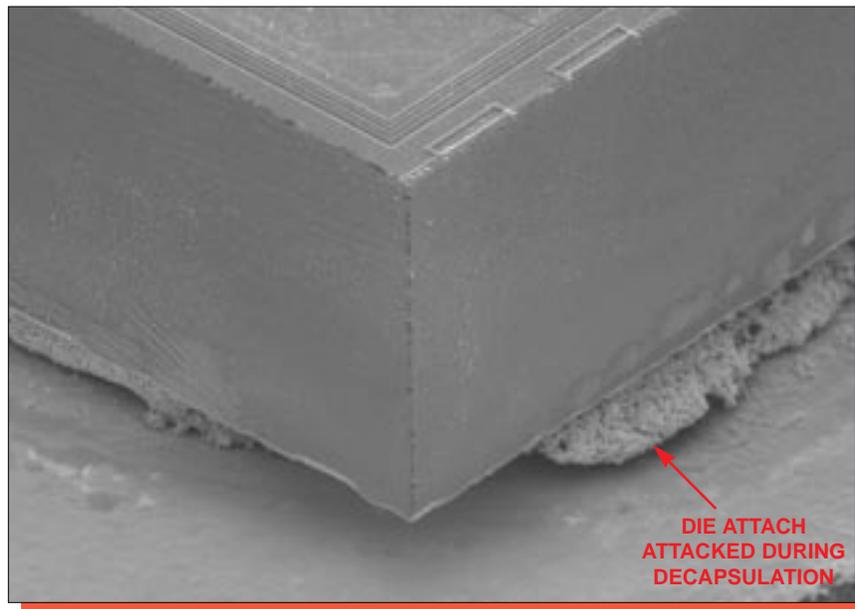


Mag. 500x

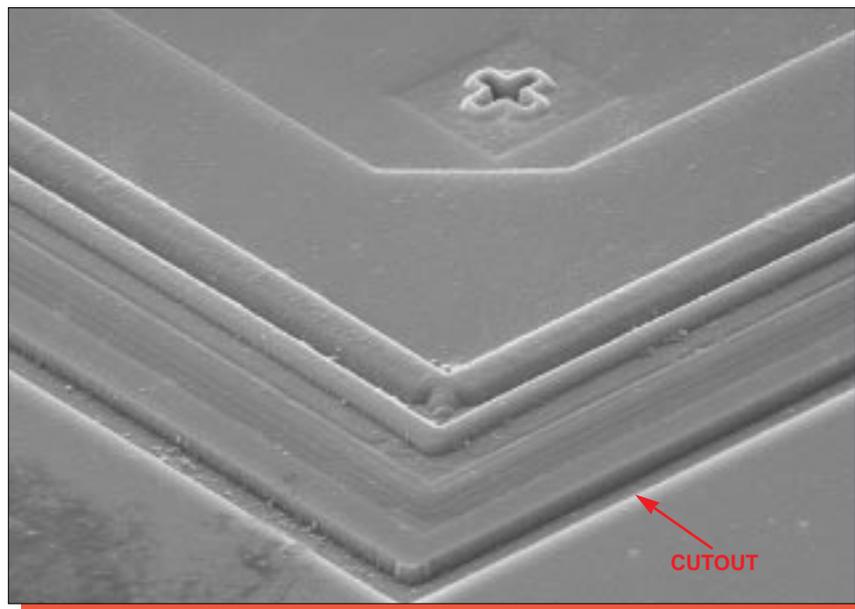


Mag. 350x

Figure 4. Detailed section views of internal plating and die attach quality.

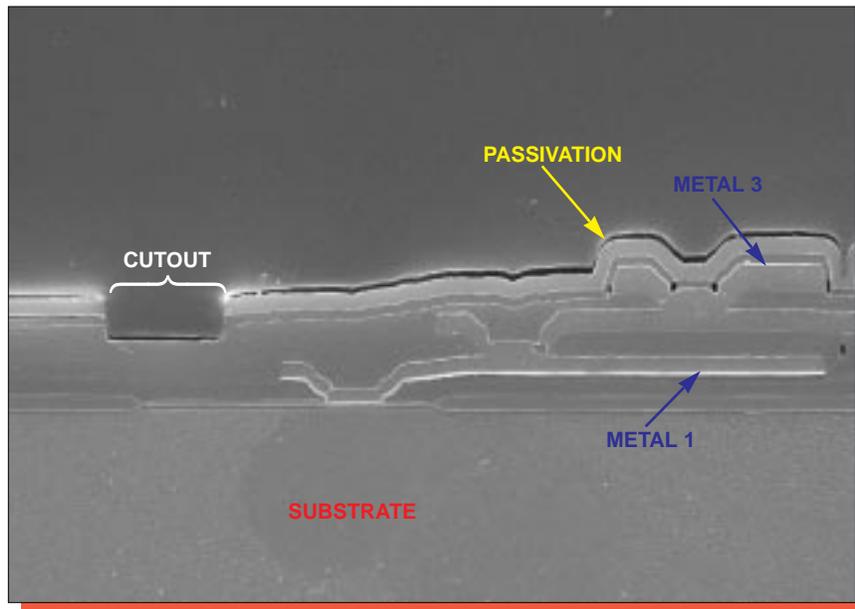


Mag. 150x

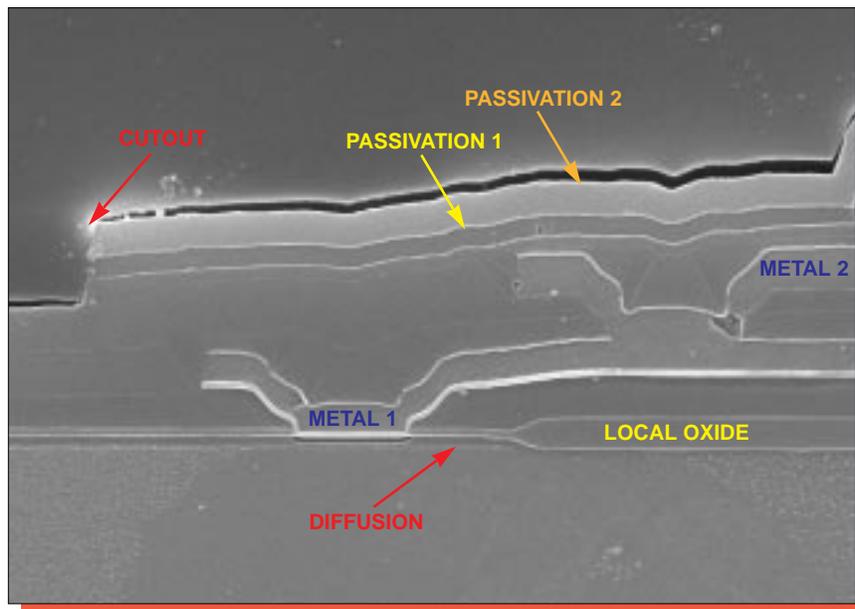


Mag. 1350x

Figure 5. SEM views of a die corner and edge seal. 60°.

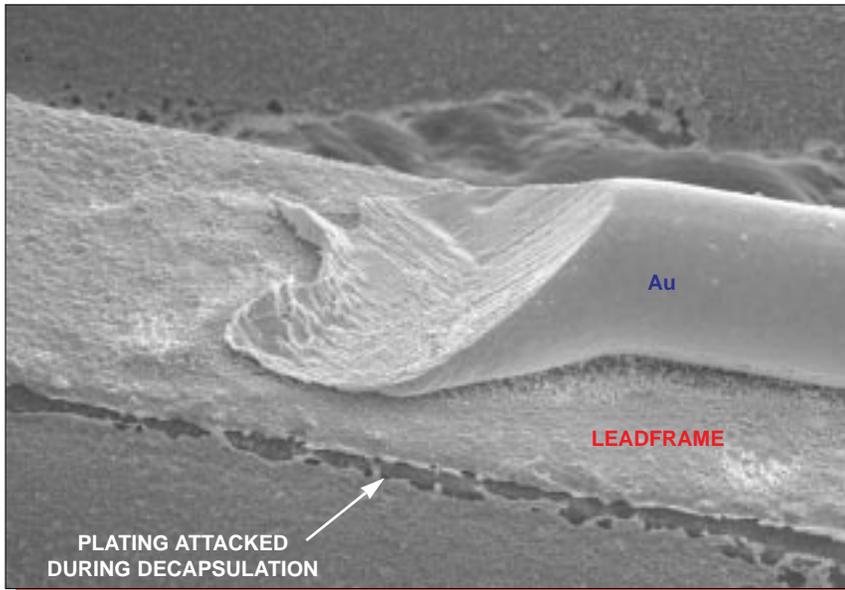


Mag. 3500x

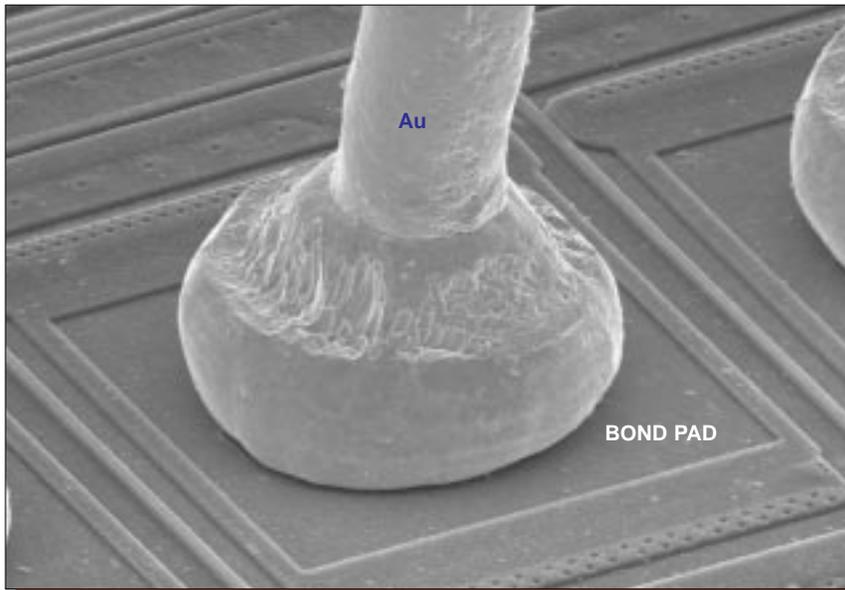


Mag. 7000x

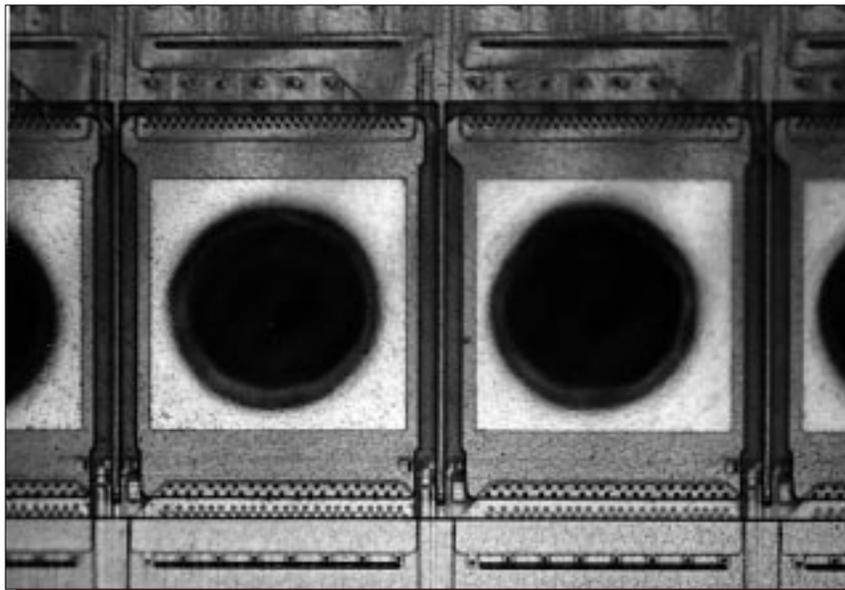
Figure 6. SEM section views of edge seal structure.



Mag. 750x, 60°



Mag. 750x, 60°

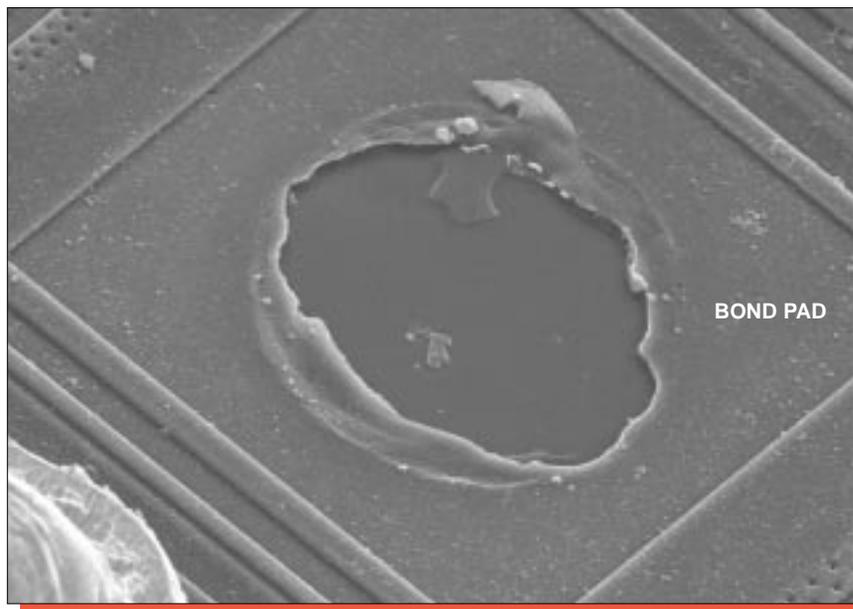


Mag. 320x

Figure 7. Optical and SEM views illustrating wirebonding.

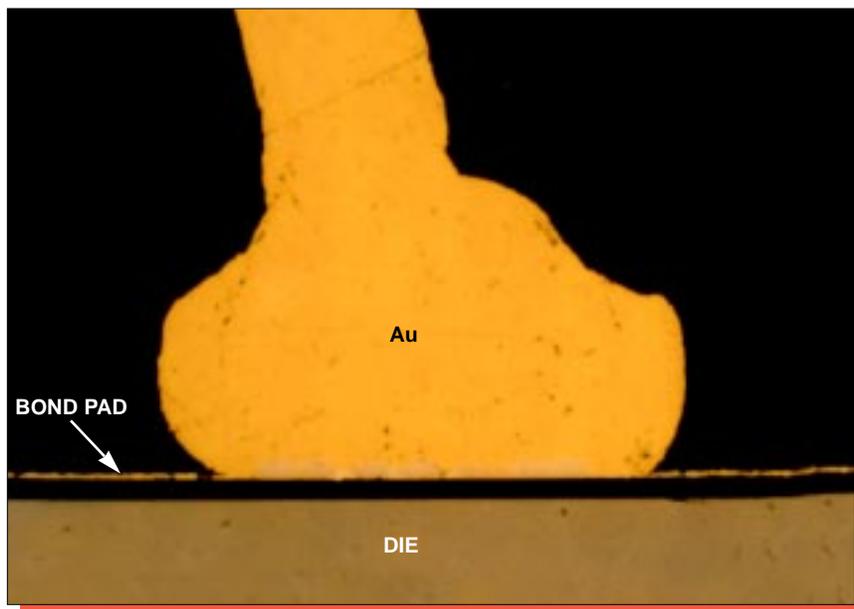


Mag. 885x

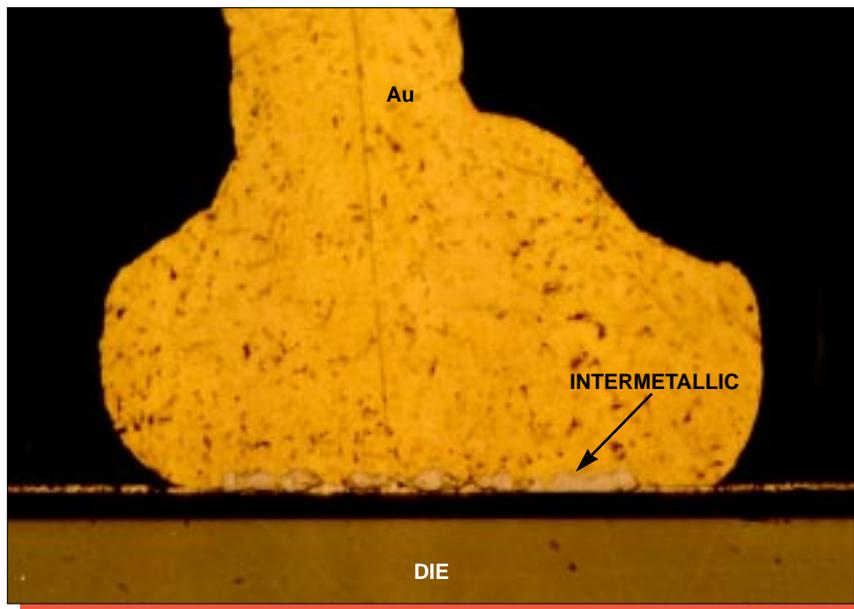


Mag. 850x

Figure 7a. SEM views of a lifted ball bond (following wirepull). 50°.

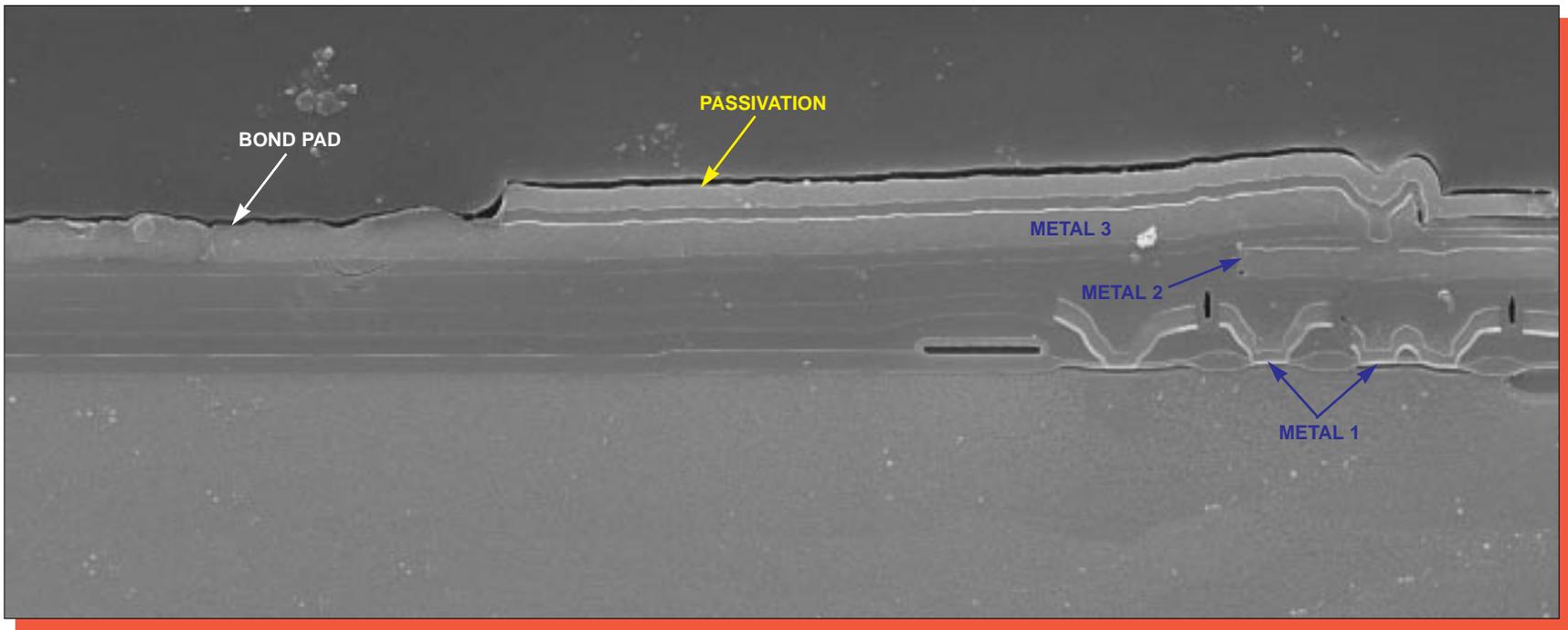


as polished, Mag. 800x

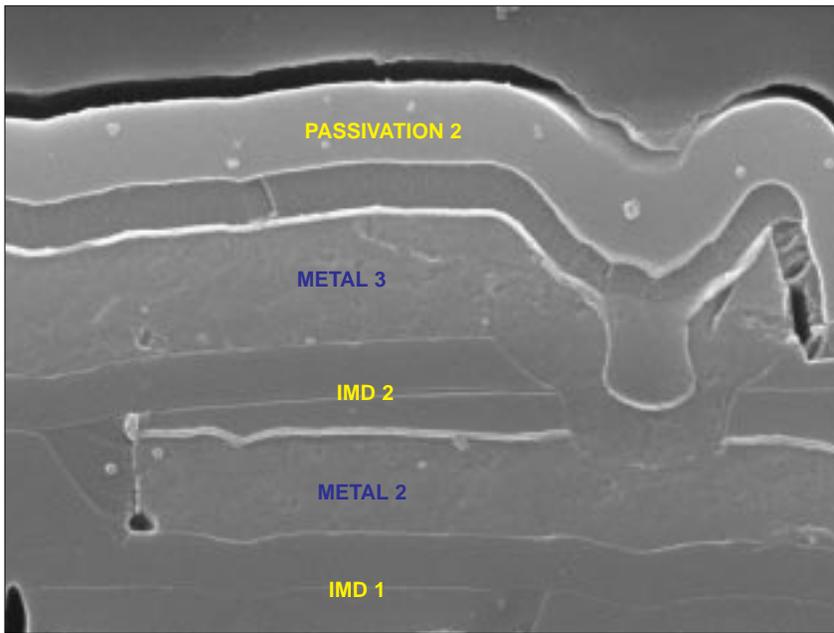


delineation etch, Mag. 1000x

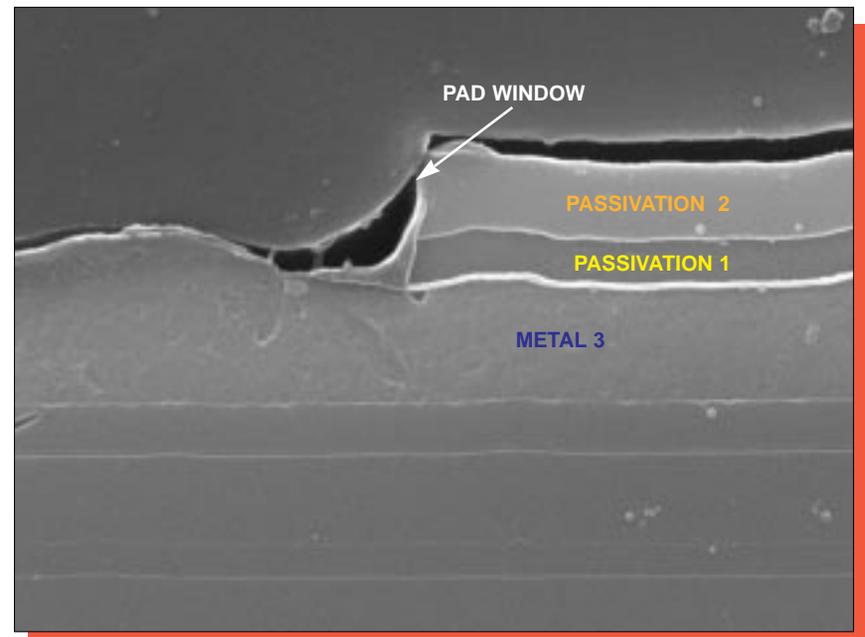
Figure 8. Section views of a typical ball bond.



Mag. 5000x



Mag. 17,000x



Mag. 15,500x

Figure 9. SEM section views illustrating bond pad structure.

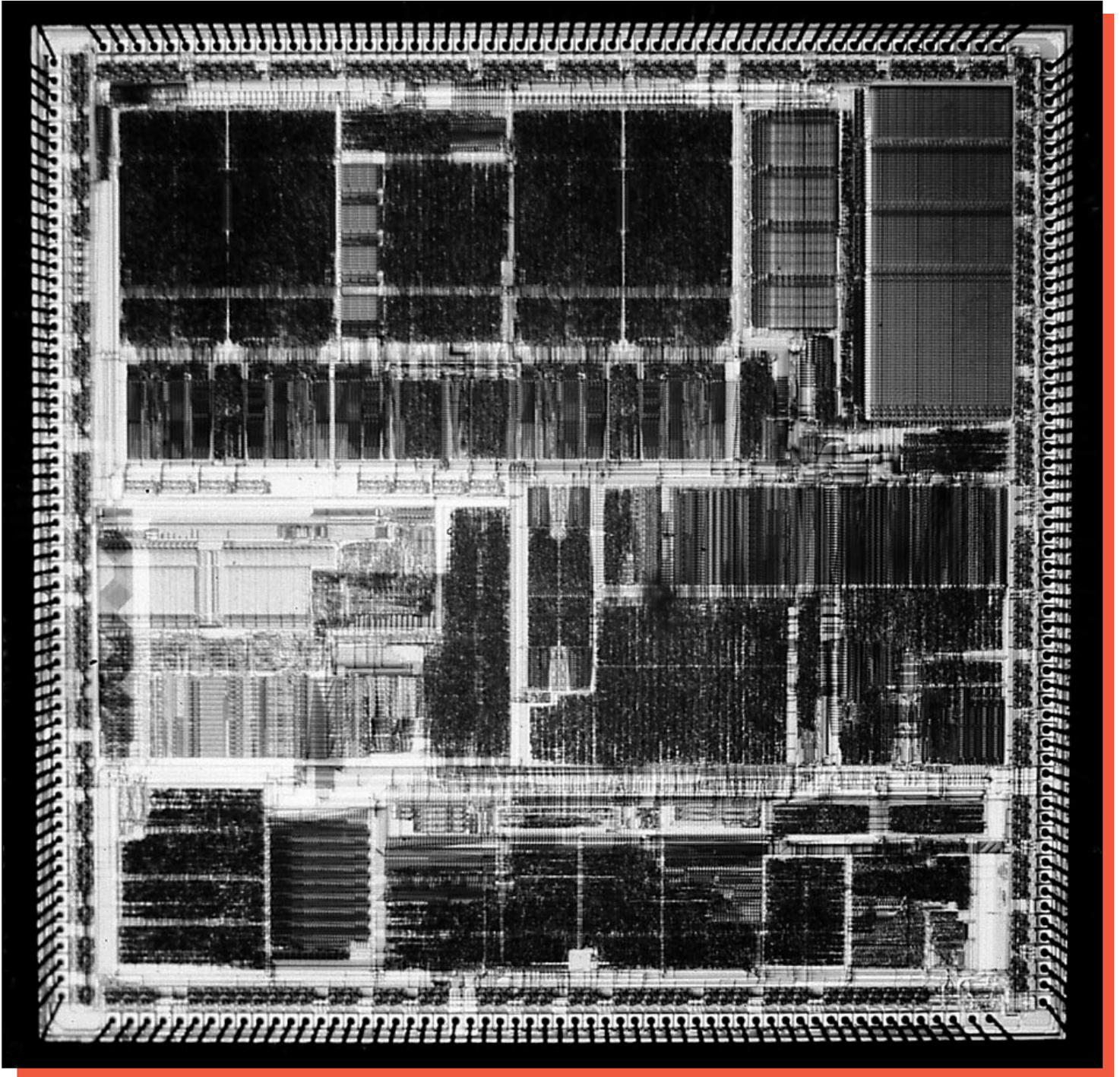


Figure 10. Whole die photograph of the Motorola MC68360. Mag. 19x.

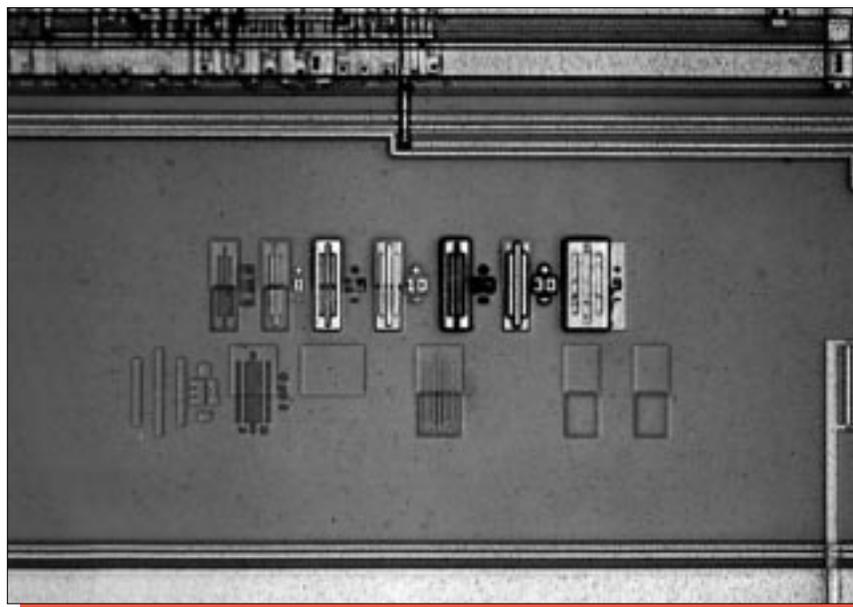


Figure 11. Die identification markings. Mag. 400x.

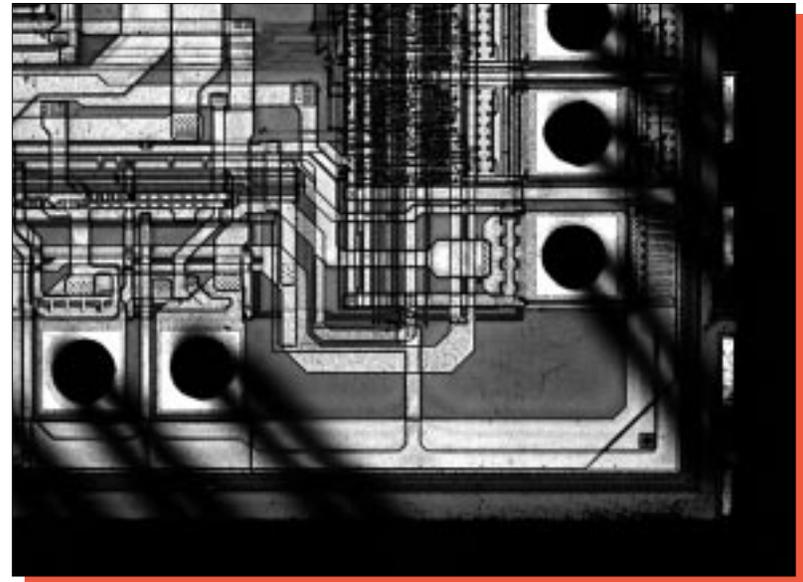
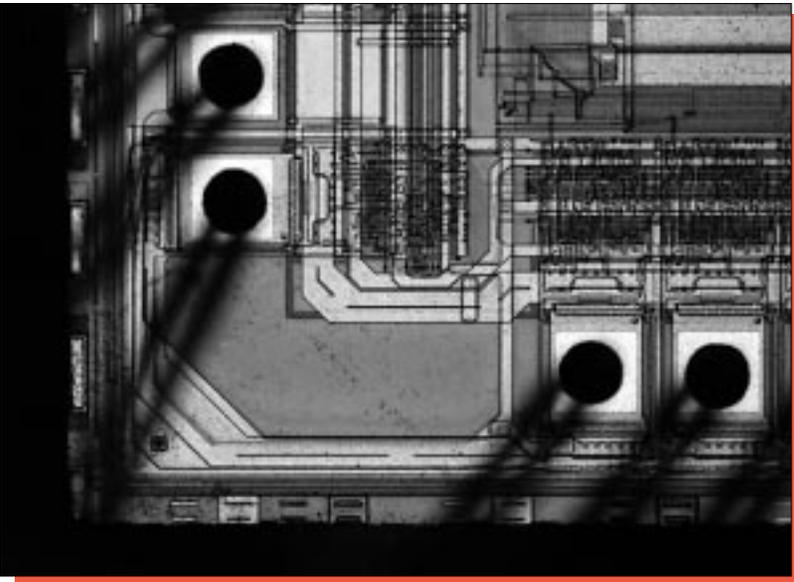
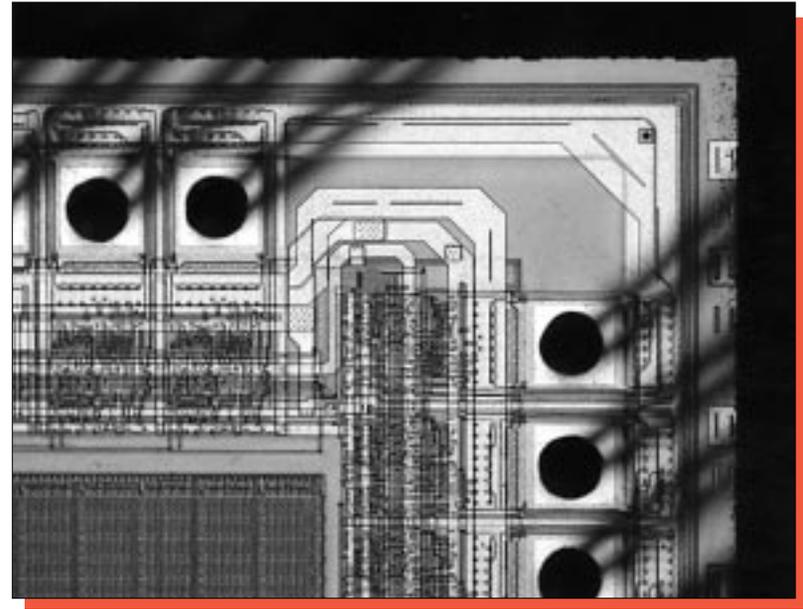
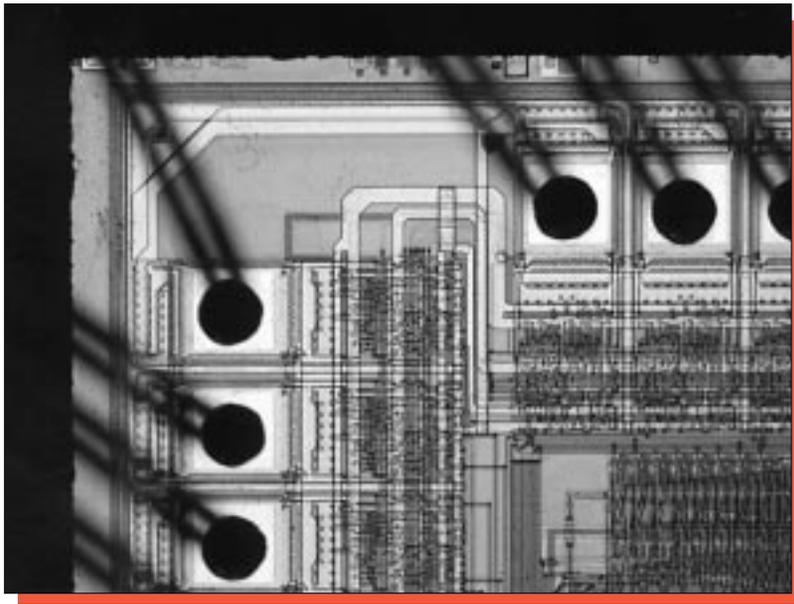
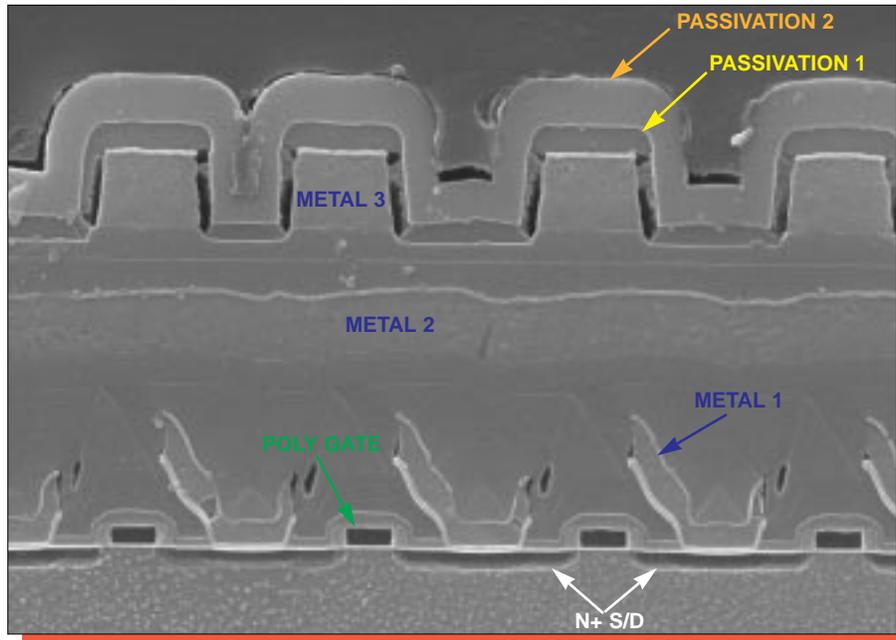
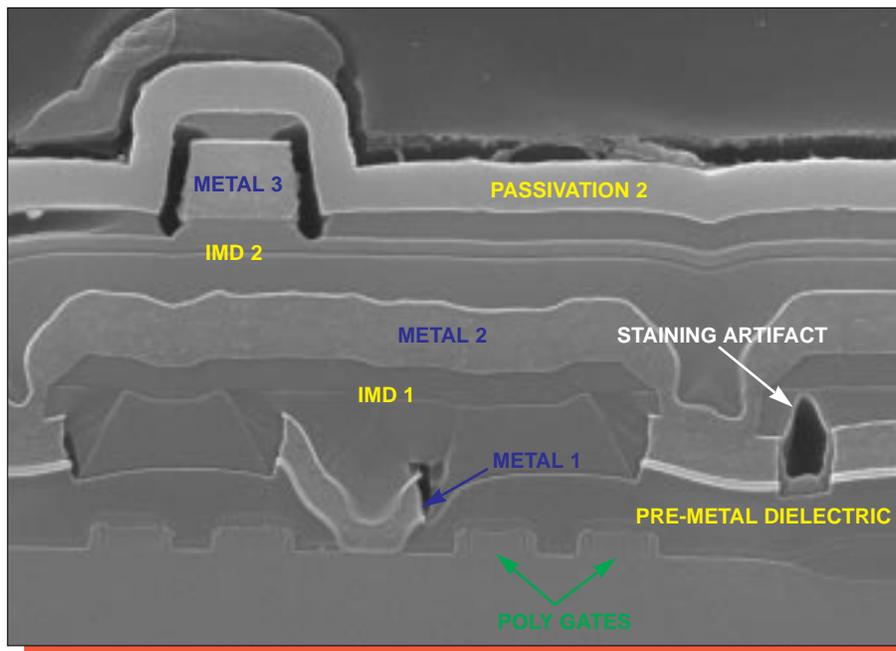


Figure 12. Optical views of the die corners. Mag. 100x.

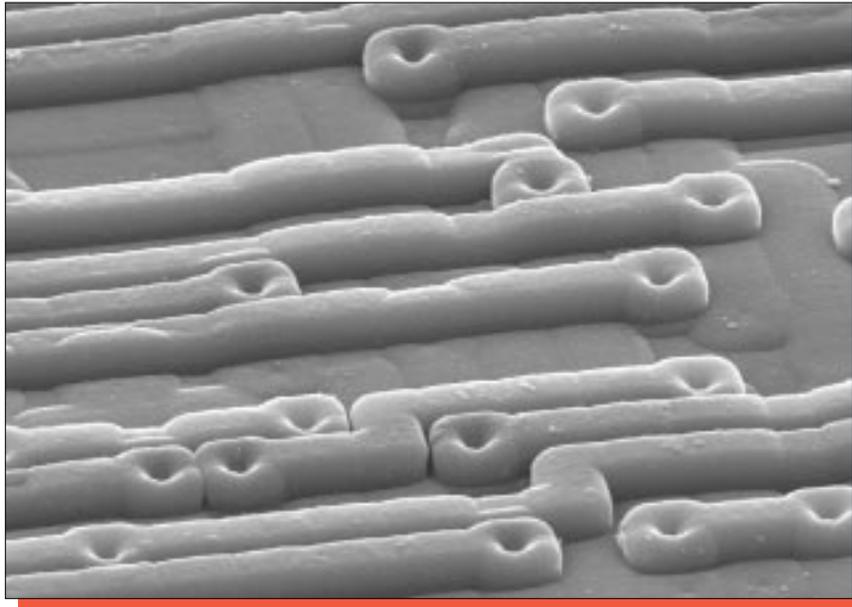


silicon etch

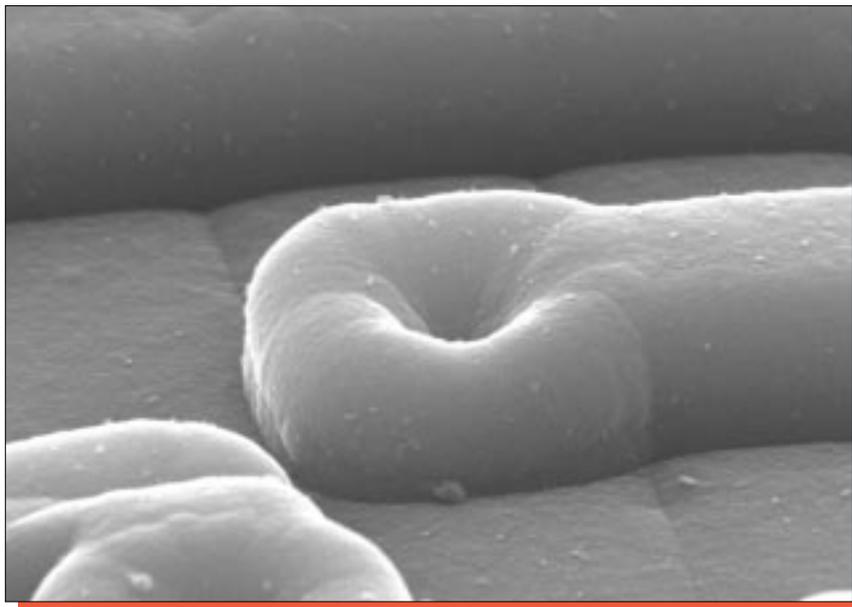


glass etch

Figure 13. SEM section views illustrating general device structure. Mag. 10,000x.

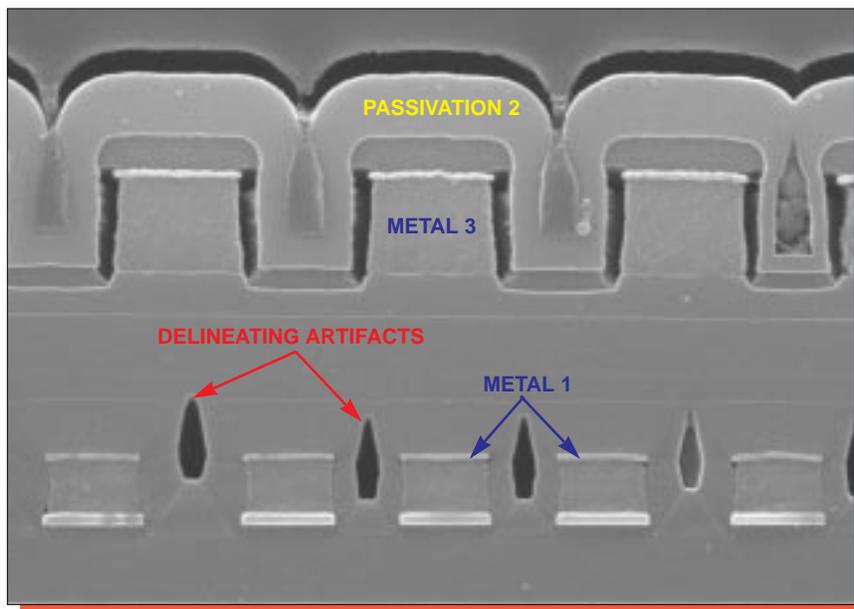


Mag. 3500x

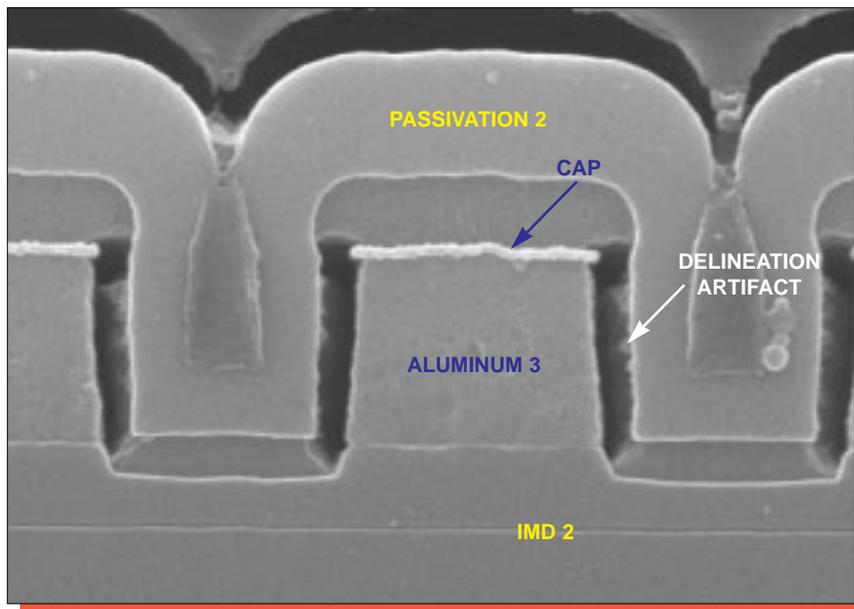


Mag. 15,000x

Figure 14. SEM views of overlay passivation coverage. 60°.



Mag. 13,000x



Mag. 26,000x

Figure 15. SEM section views of metal 3 line profiles.

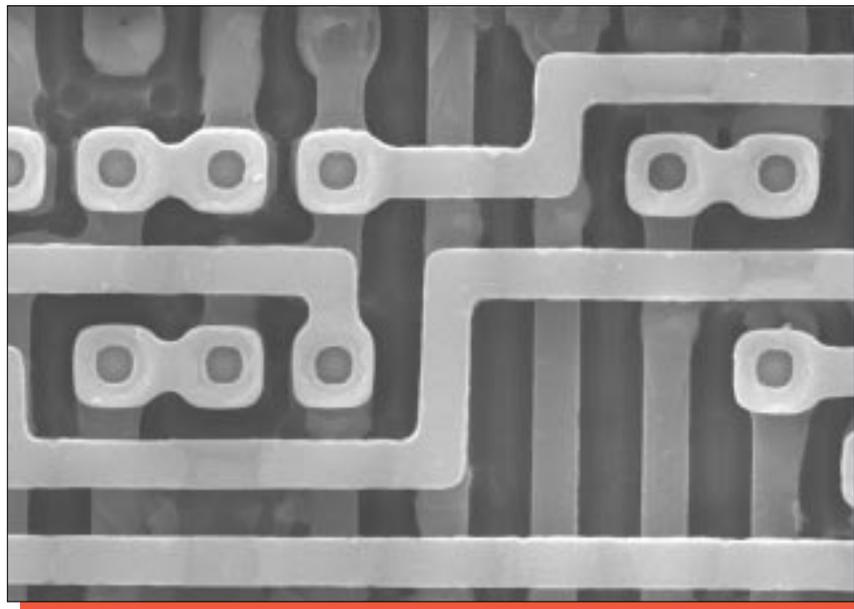
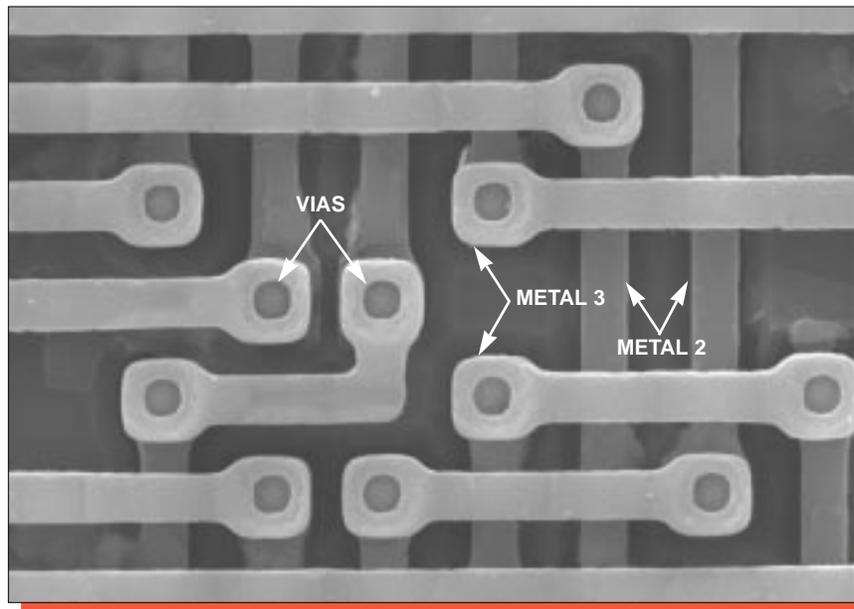
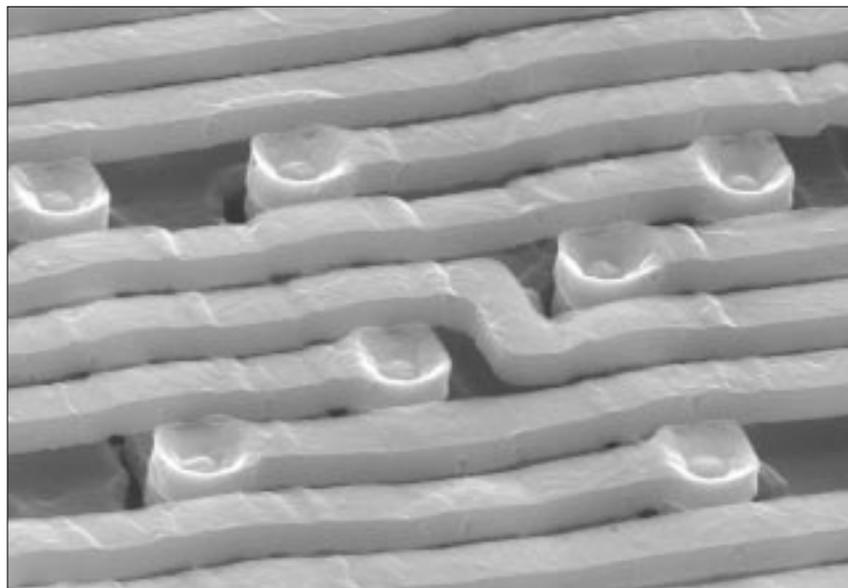
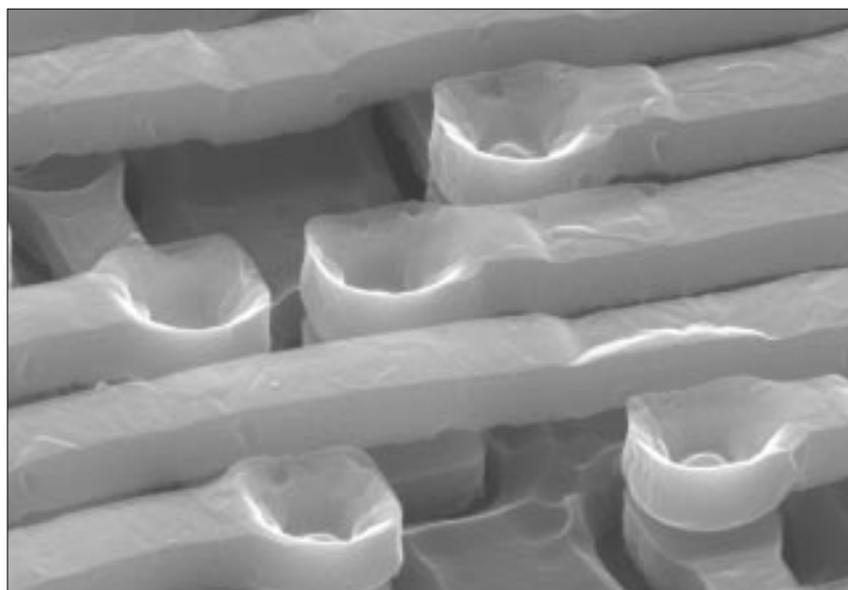


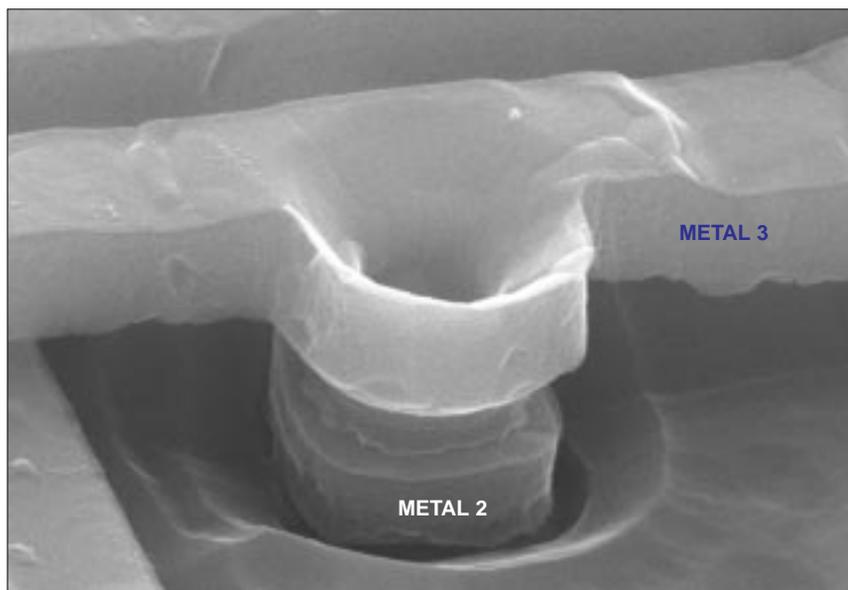
Figure 16. Topological SEM views illustrating metal 3 patterning. Mag. 5000x, 0°.



Mag. 6000x



Mag. 10,000x



Mag. 18,000x

Figure 17. SEM views of general metal 3 integrity. 55°.

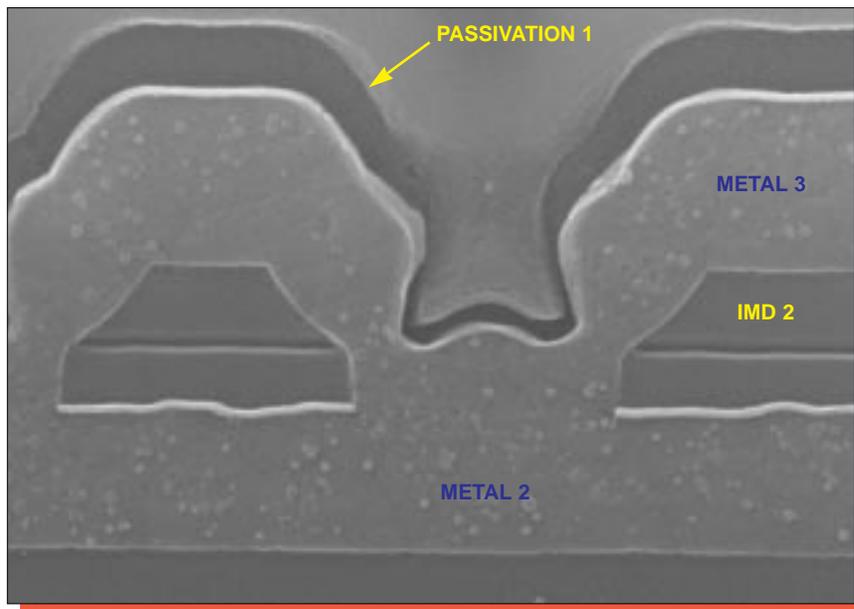
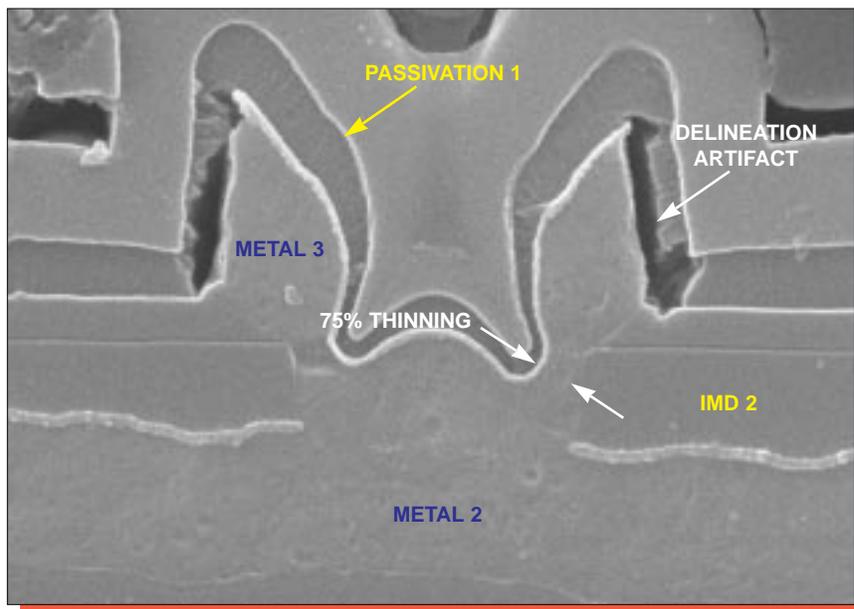
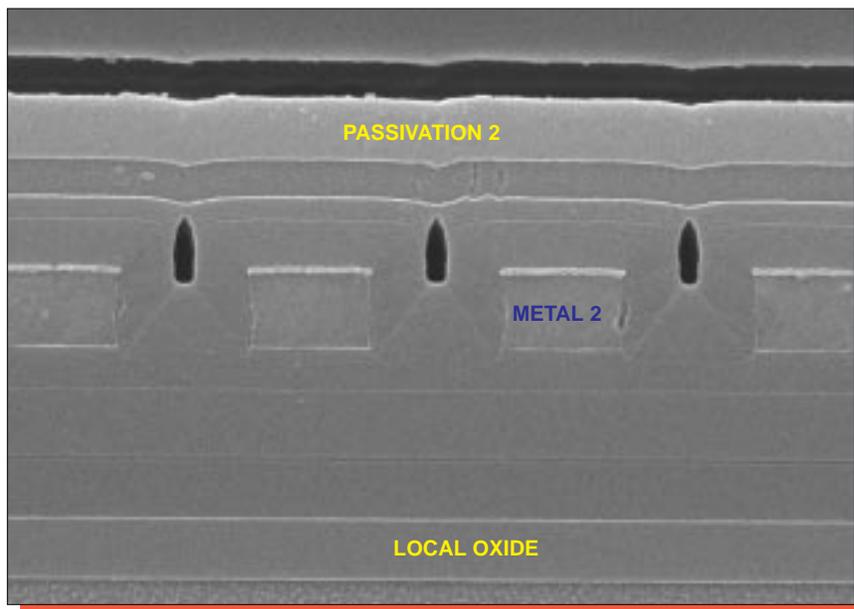
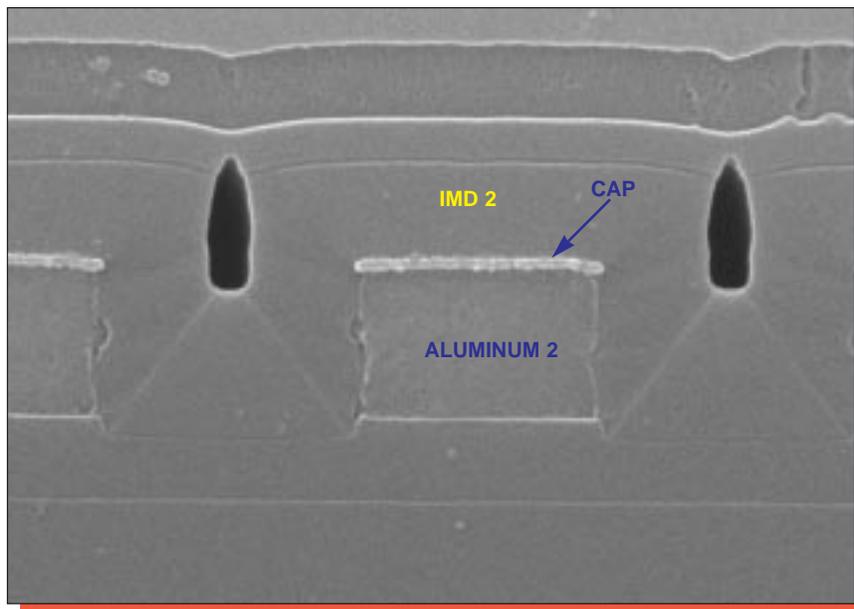


Figure 18. SEM section views of metal 3-to-metal 2 vias. Mag. 25,000x.

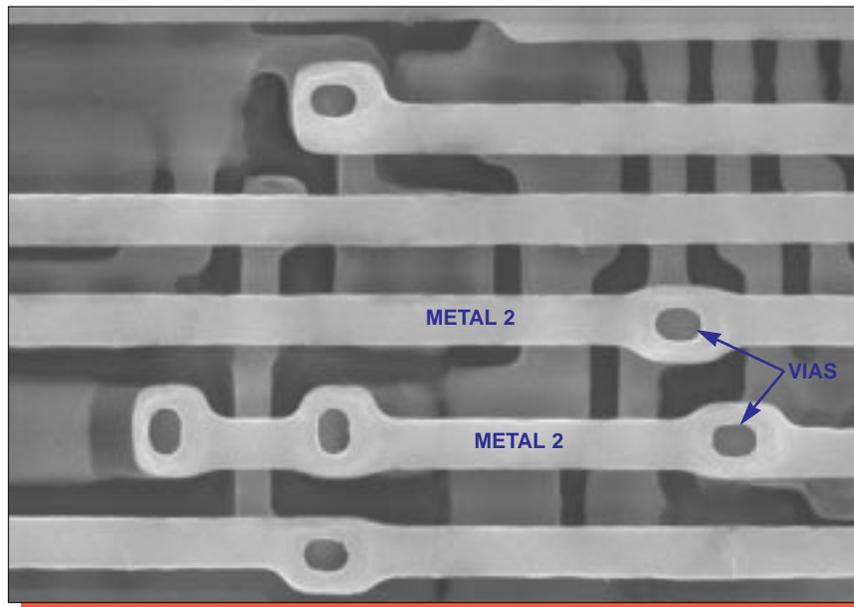


Mag. 13,000x

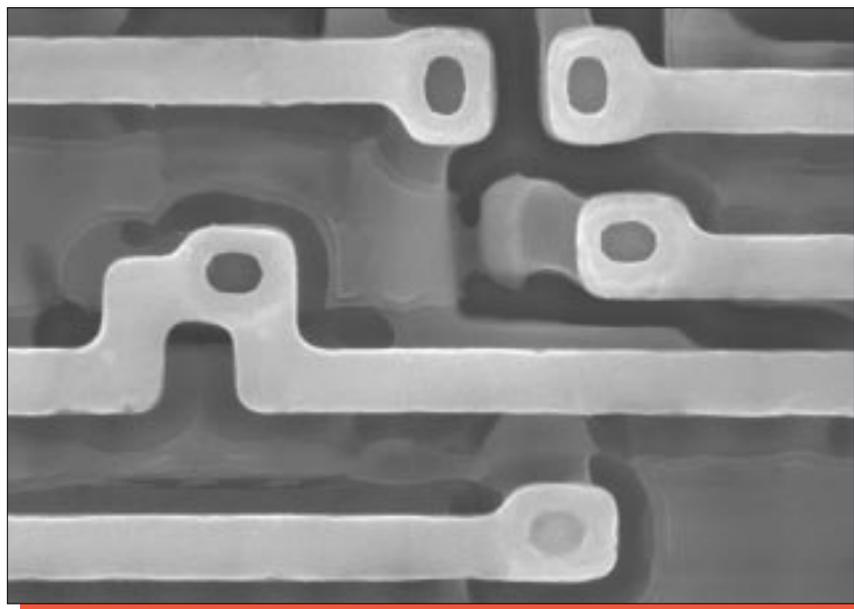


Mag. 26,000x

Figure 19. SEM section views of metal 2 line profiles.

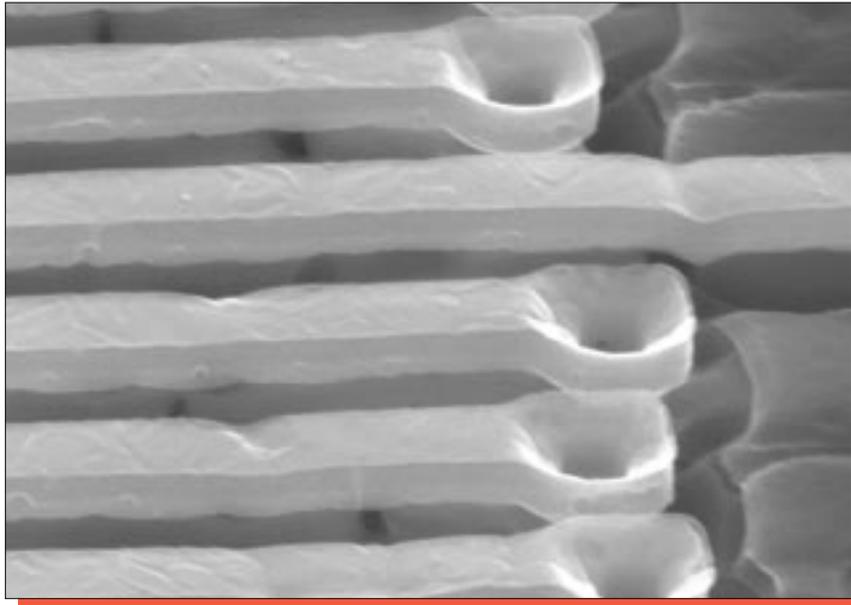


Mag. 5500x

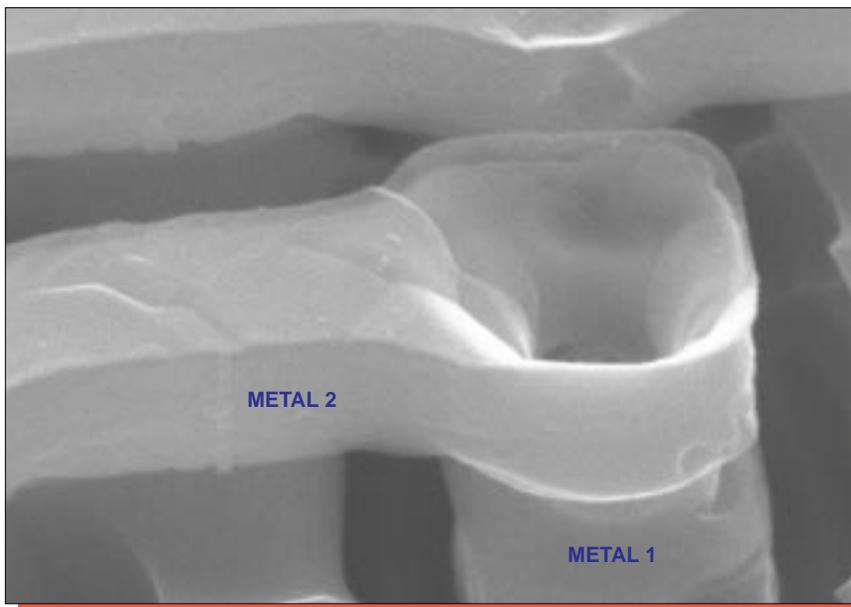


Mag. 7000x

Figure 20. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 10,000x



Mag, 26,000x

Figure 21. SEM views of general metal 2 integrity. 55°.

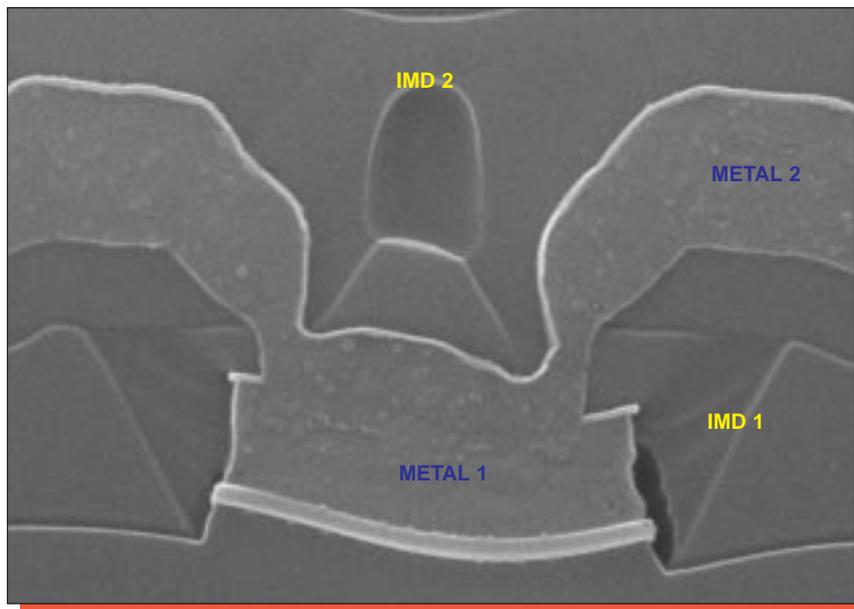
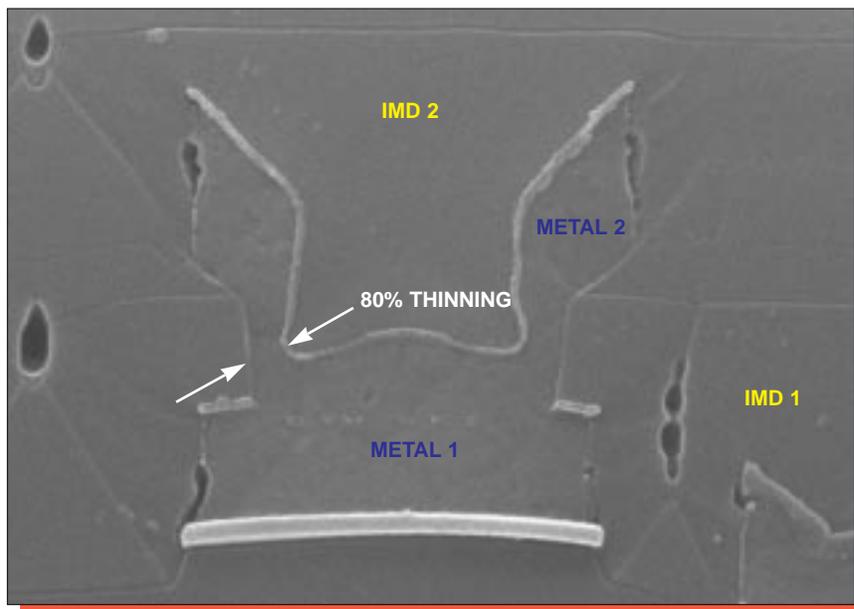
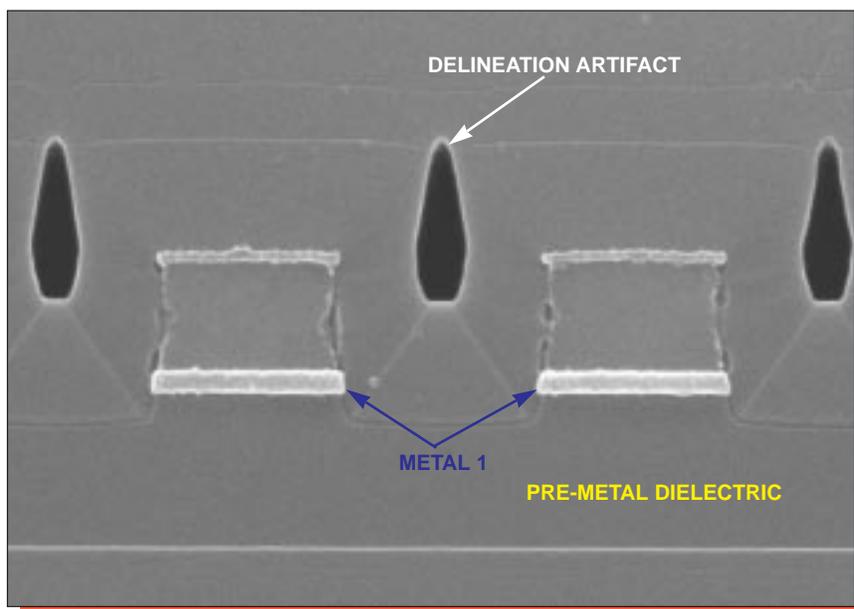
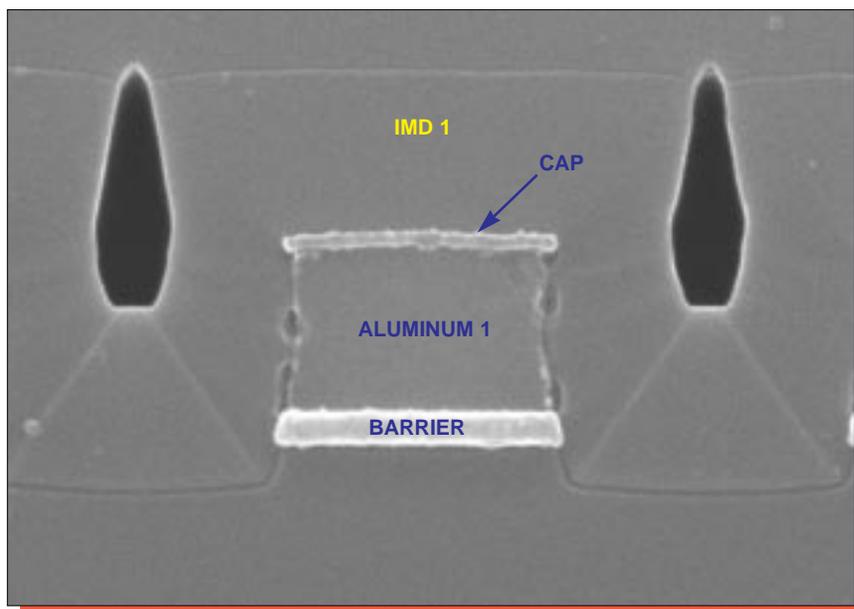


Figure 22. SEM section views of metal 2-to-metal 1 vias. Mag. 26,000x.



Mag. 26,000x



Mag. 40,000x

Figure 23. SEM section views of metal 1 line profiles.

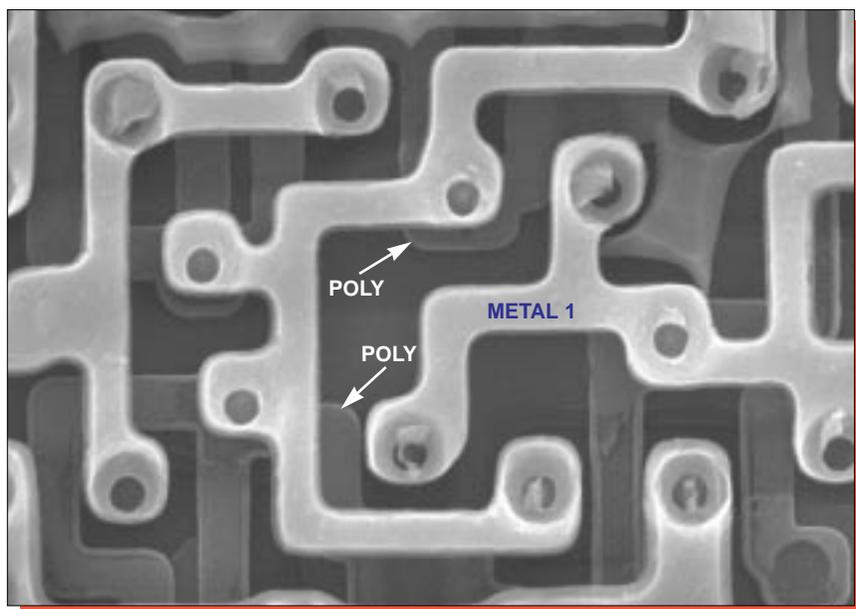
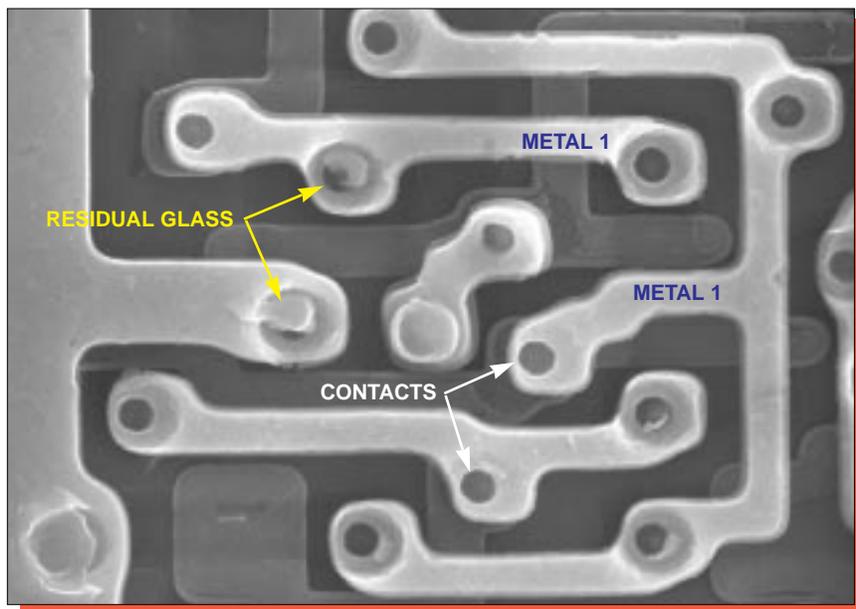
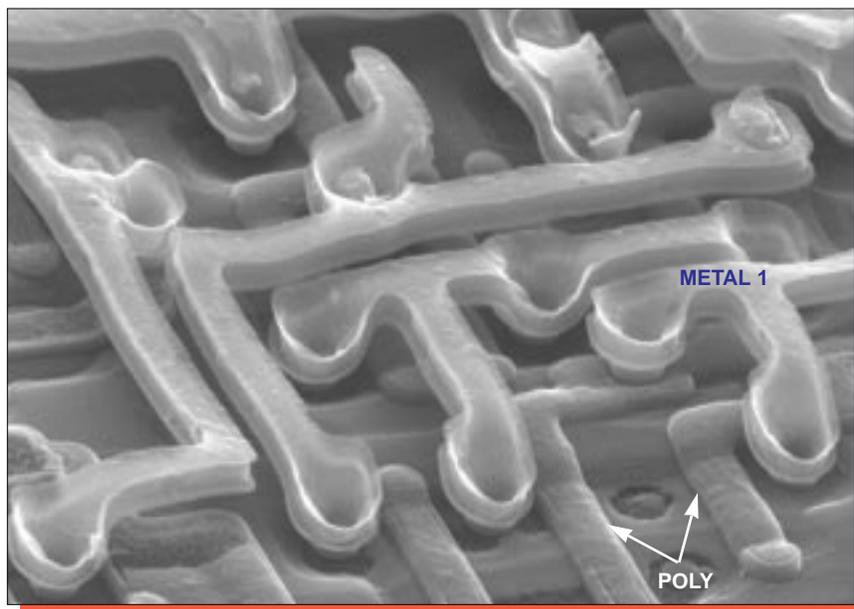
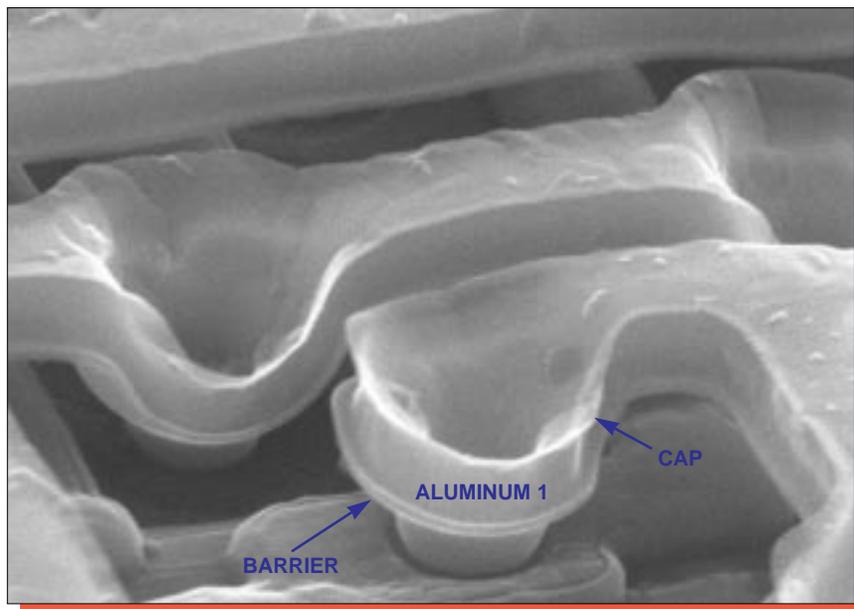


Figure 24. Topological SEM views illustrating metal 1 patterning. Mag. 6500x, 0°.

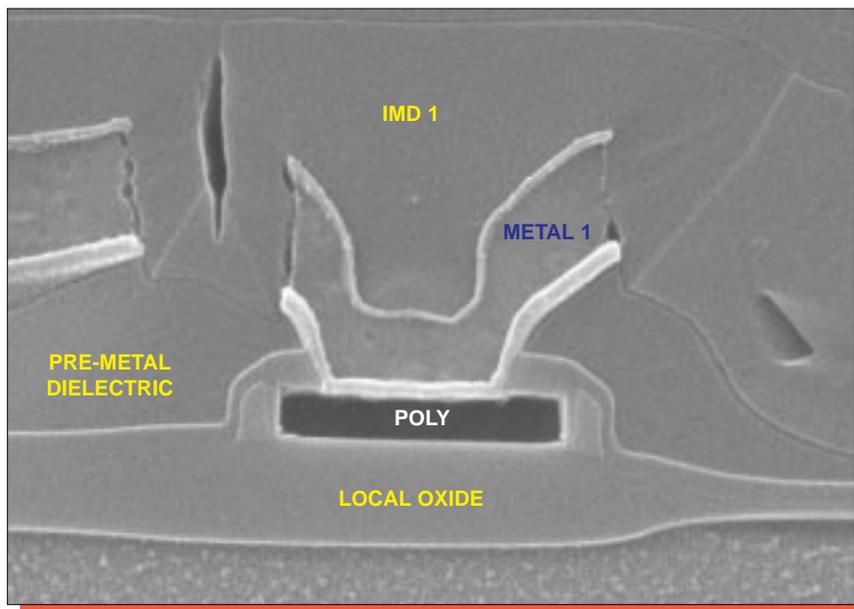


Mag. 7000x

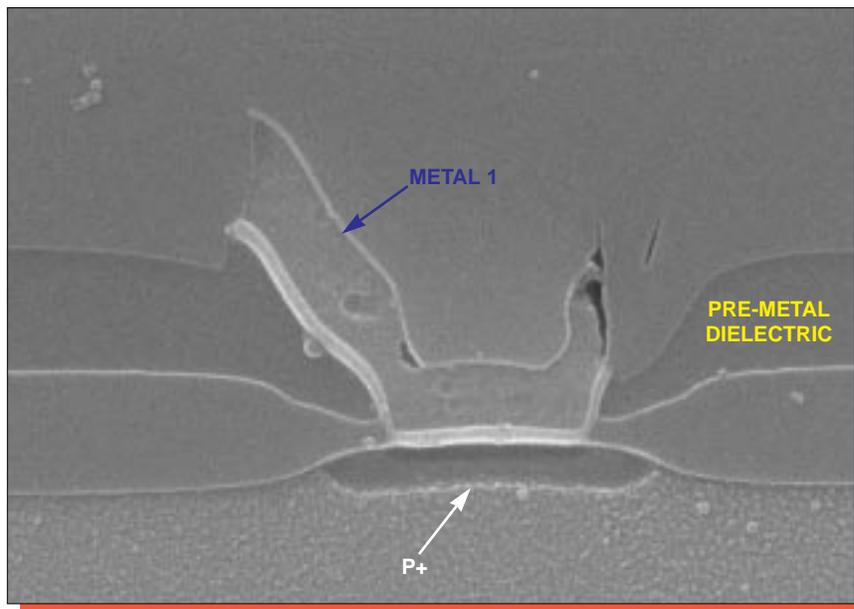


Mag. 20,000x

Figure 25. SEM views of general metal 1 integrity. 55°.



metal 1-to-poly



metal 1-to-P+

Figure 26. SEM section views of metal 1 contacts. Mag. 26,000x.

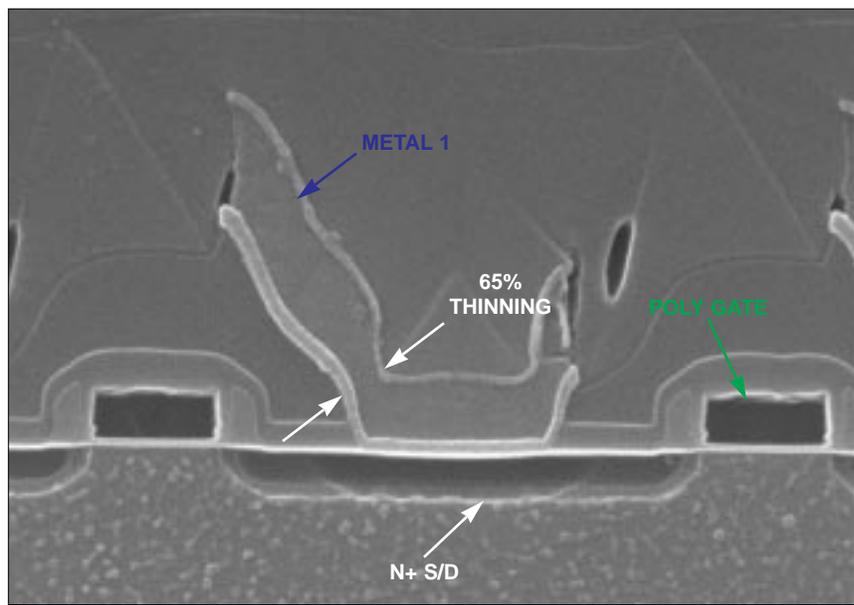
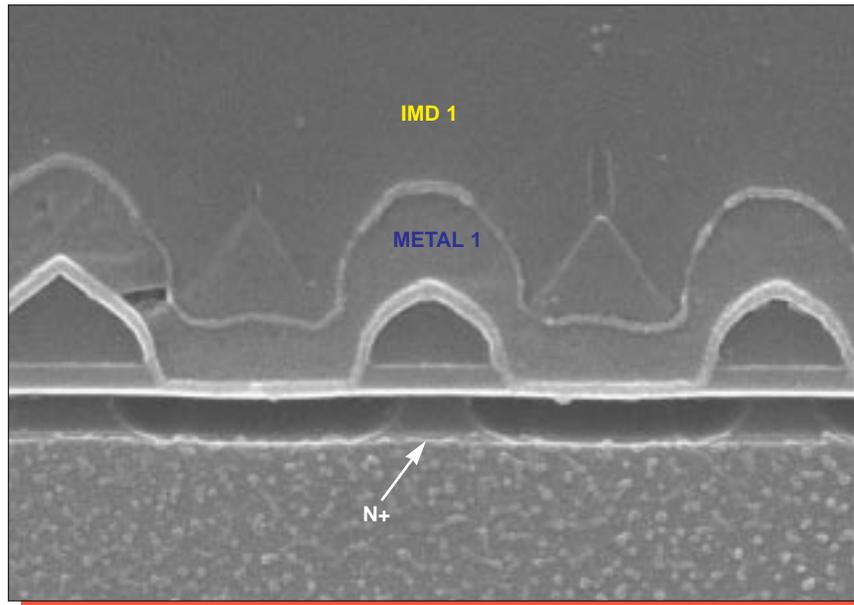
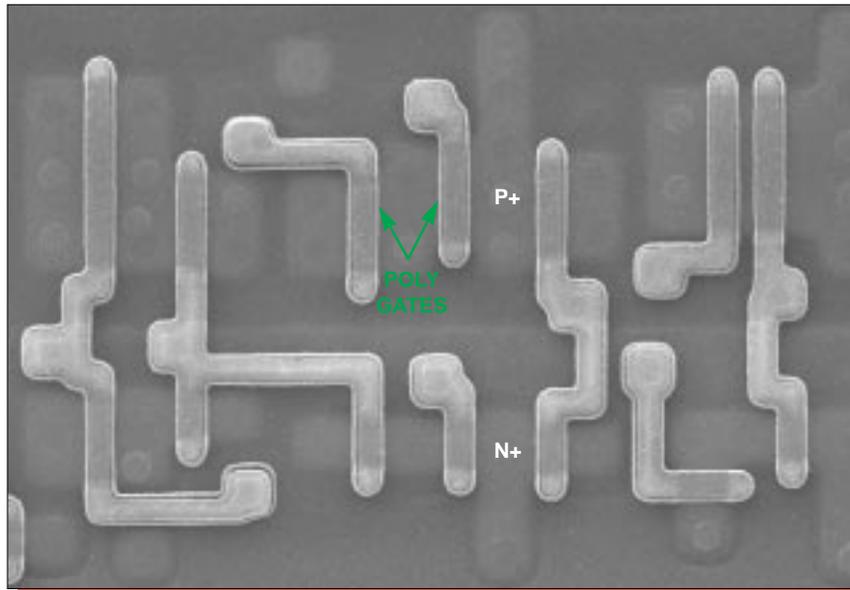
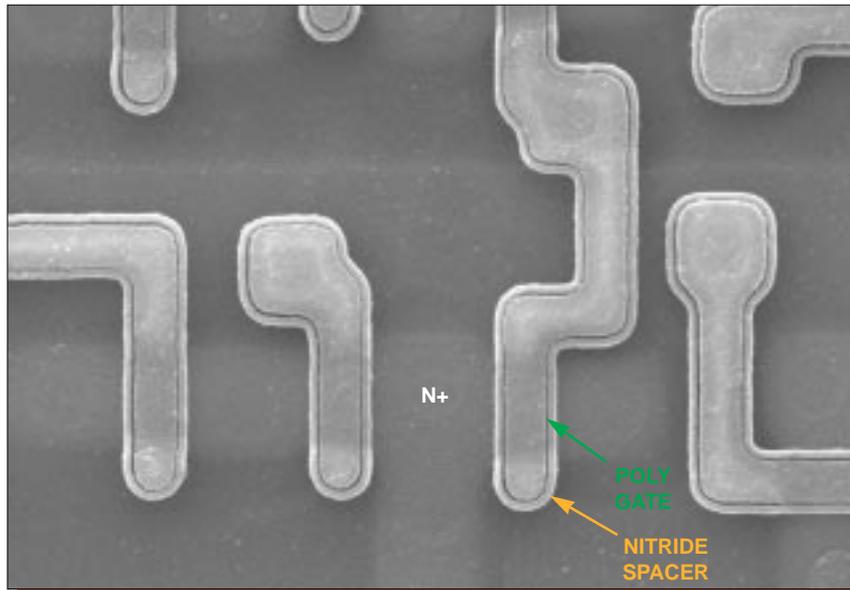


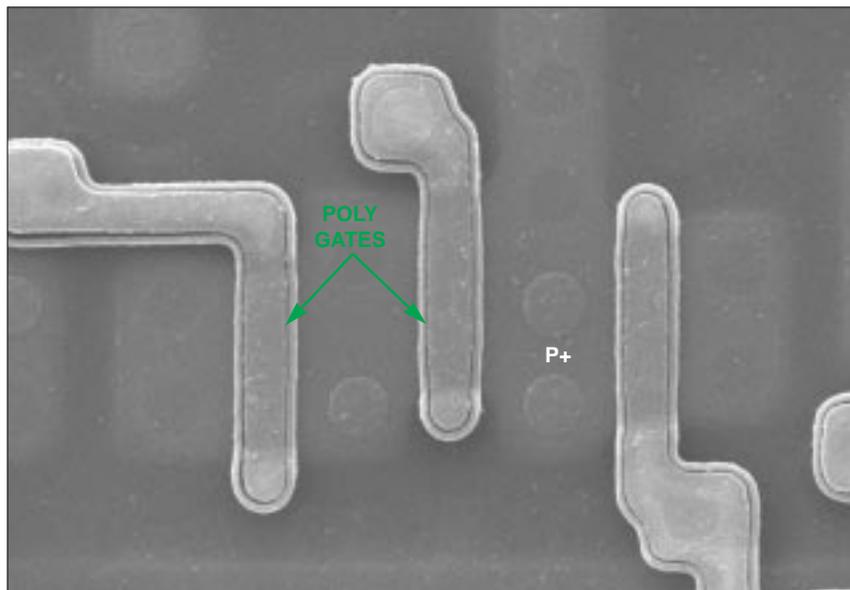
Figure 26a. SEM section views of metal 1-to-N+ contacts. Mag. 26,000x.



Mag. 4000x

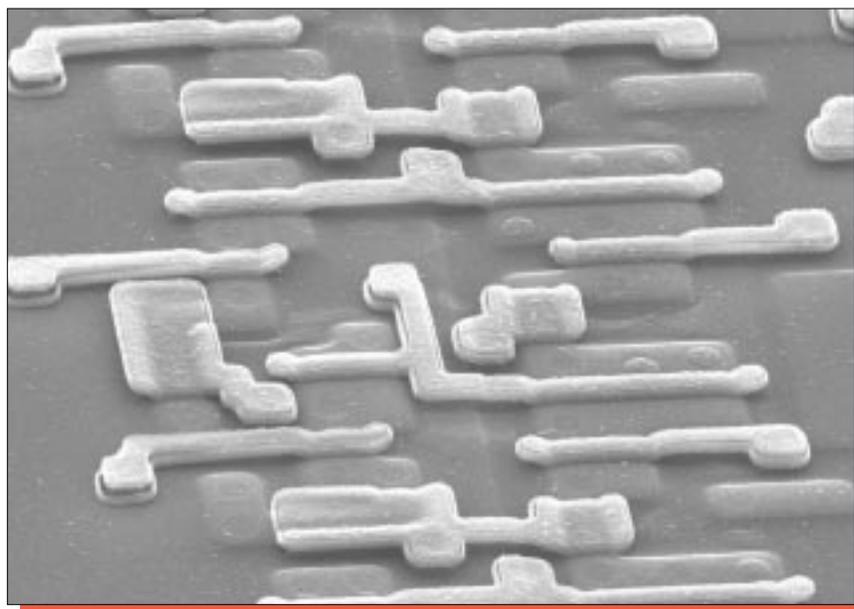


Mag. 8000x

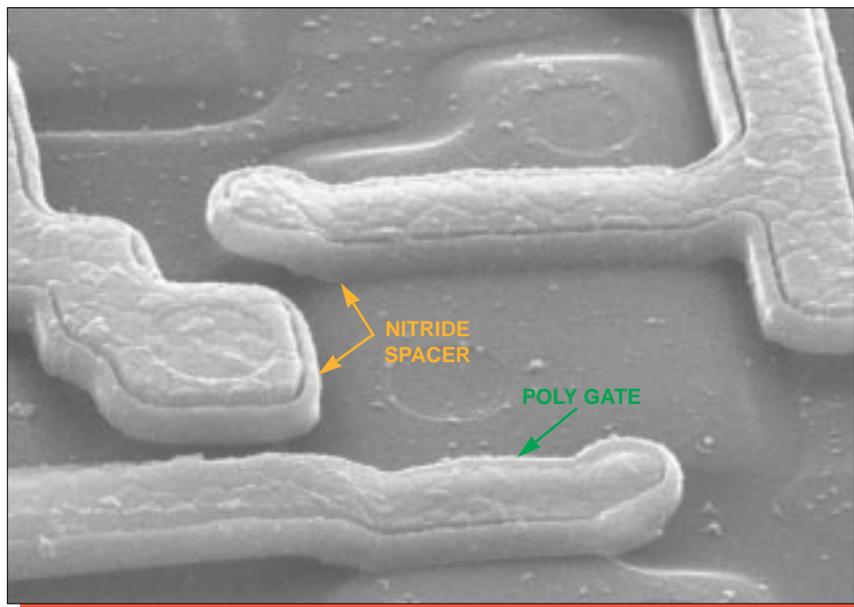


Mag. 8000x

Figure. 27. Topological SEM views illustrating poly patterning. 0°.

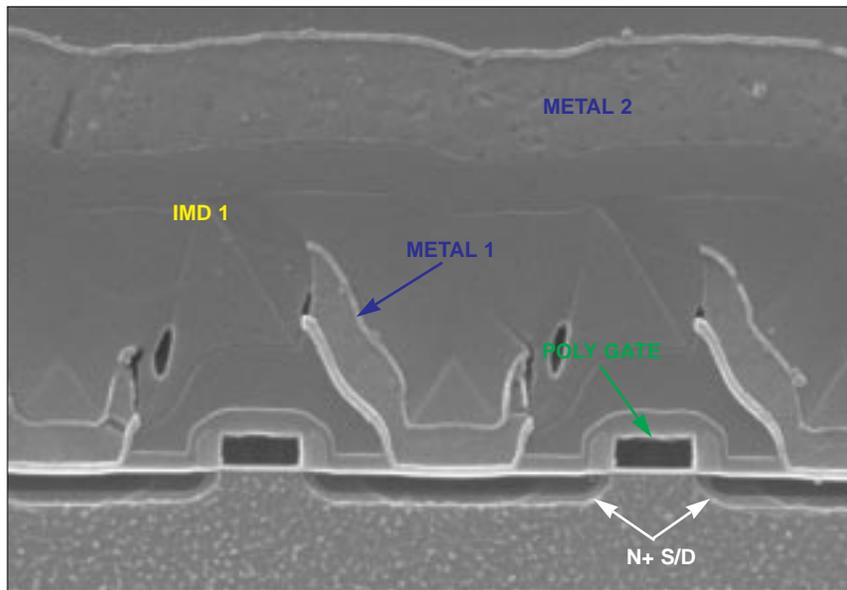


Mag. 4500x

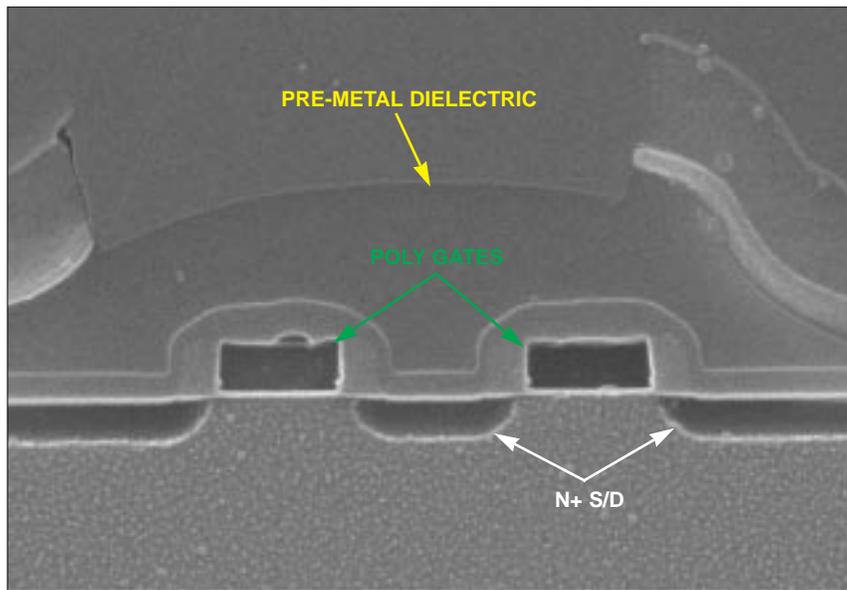


Mag. 16,000x

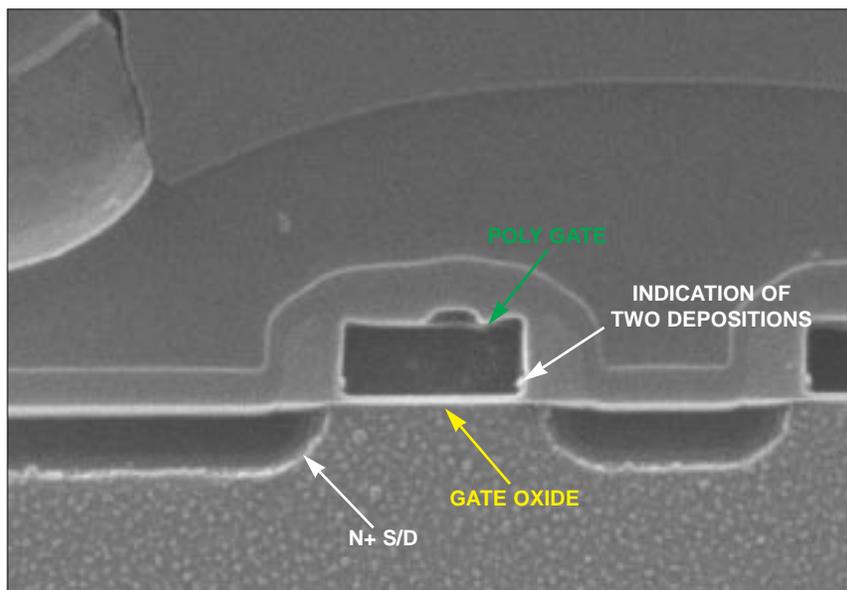
Figure 28. Perspective SEM views of poly coverage. 55°.



Mag. 17,000x

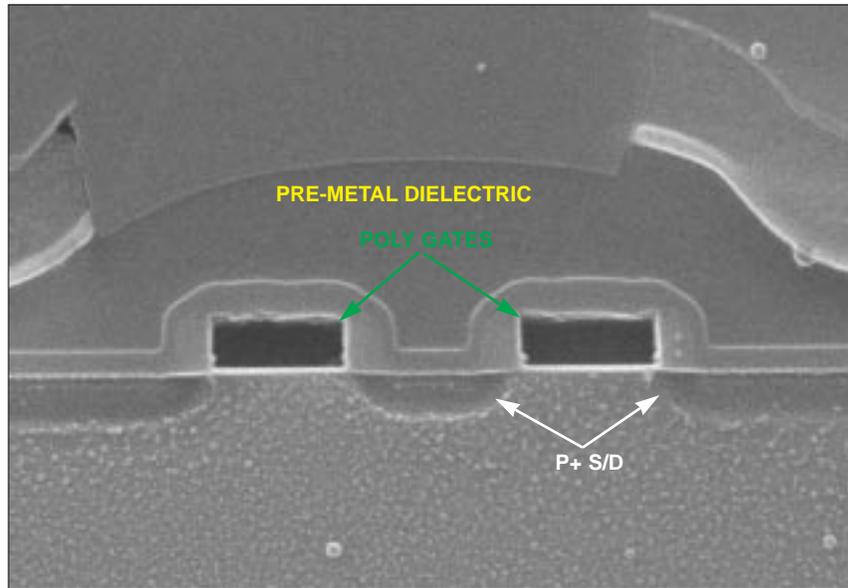


Mag. 26,000x

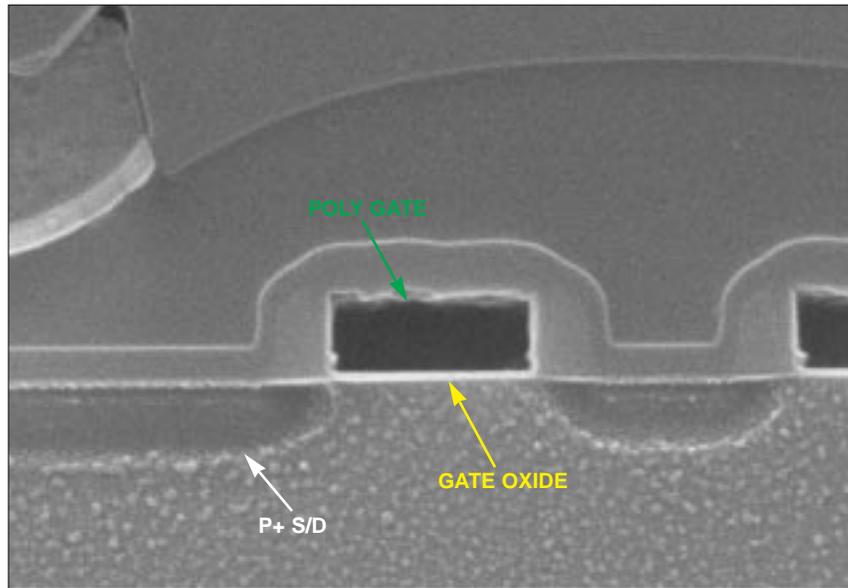


Mag. 40,000x

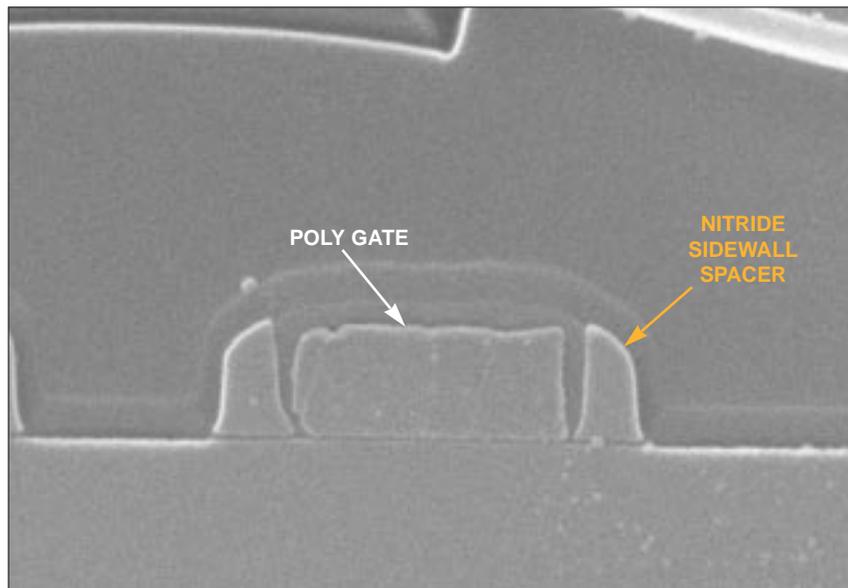
Figure 29. SEM section views of N-channel transistors.



Mag. 26,000x

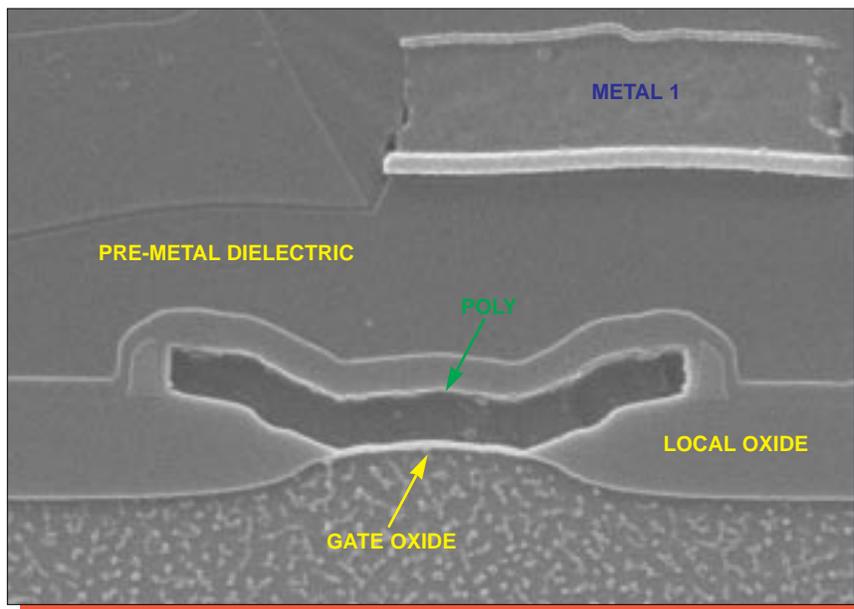


Mag. 40,000x

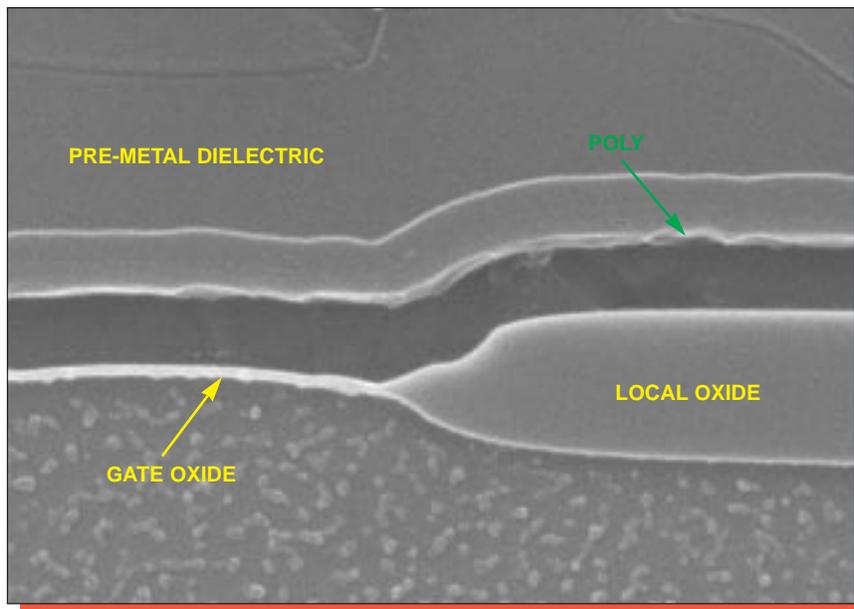


Mag. 52,000x

Figure 30. SEM section views of P-channel transistors.

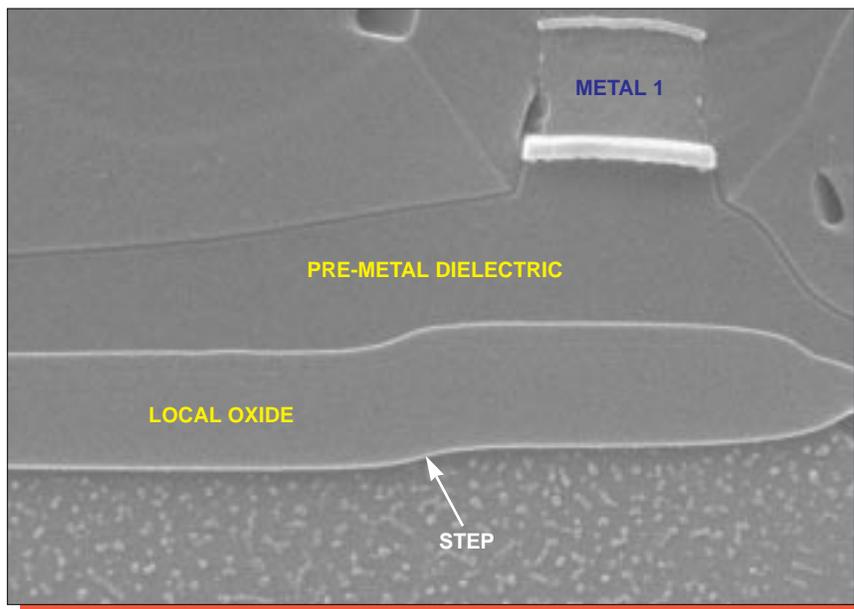


Mag. 26,000x

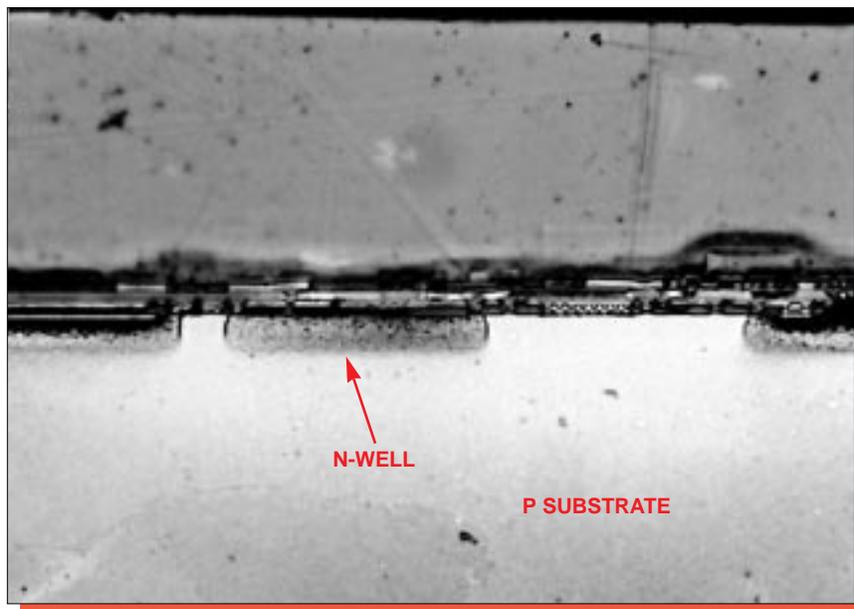


Mag. 40,000x

Figure 31. SEM section views of typical birdsbeak profiles.

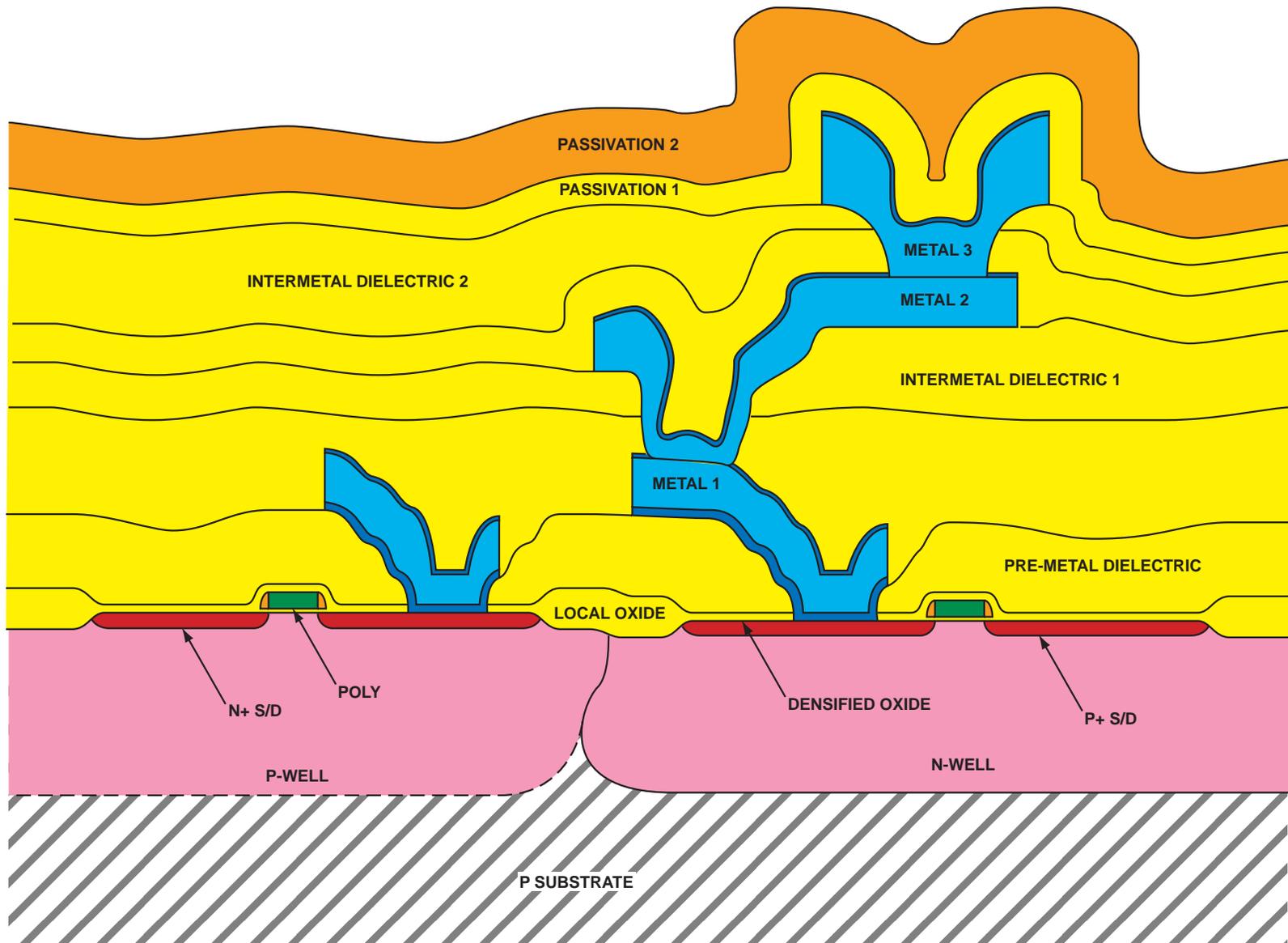


Mag. 26,000x



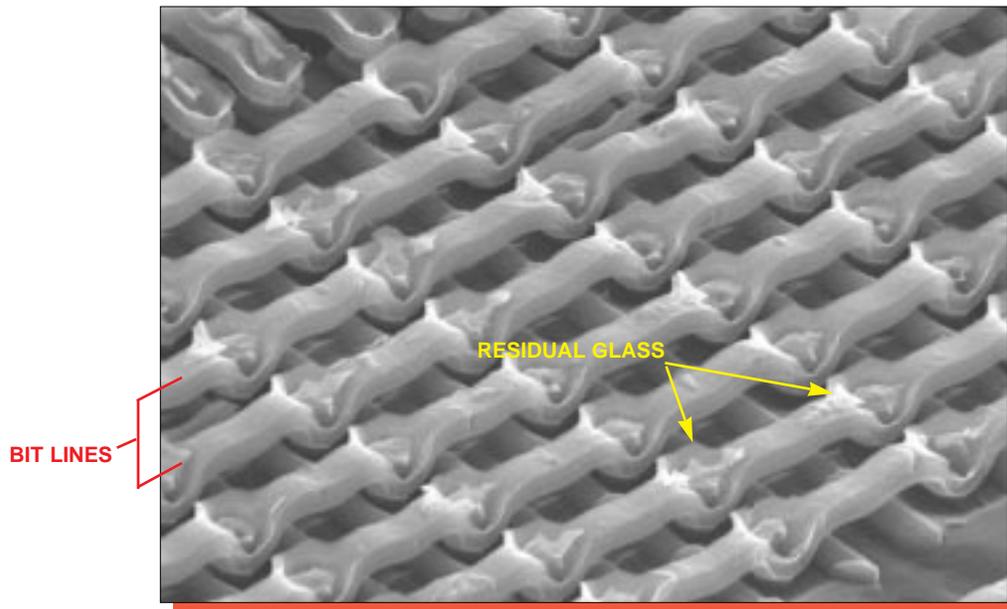
Mag. 800x

Figure 32. Section views of the well structure.

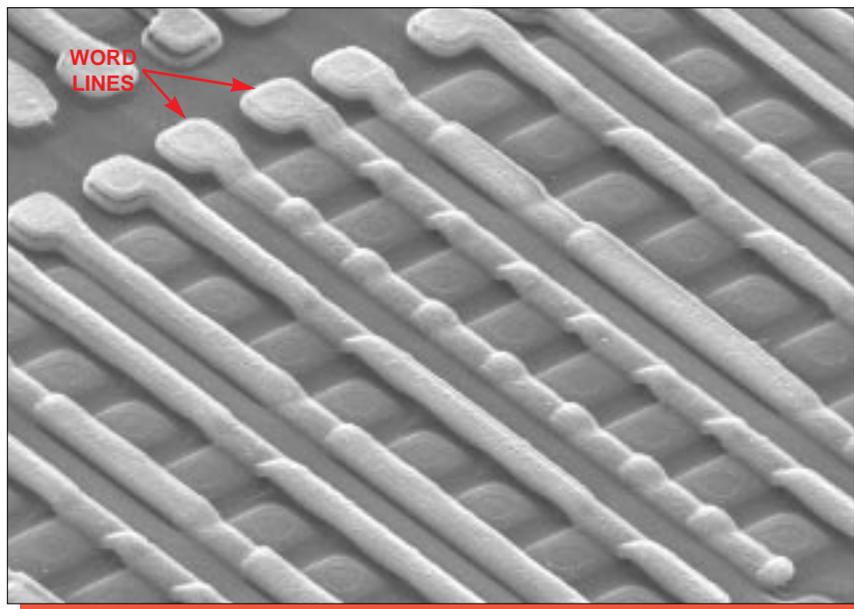


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
Red = Diffusion, and Gray = Substrate

Figure 33. Color cross section drawing illustrating device structure.



metal 1



poly

Figure 34. SEM views of an MROM array (array A). Mag. 5500x, 0°.

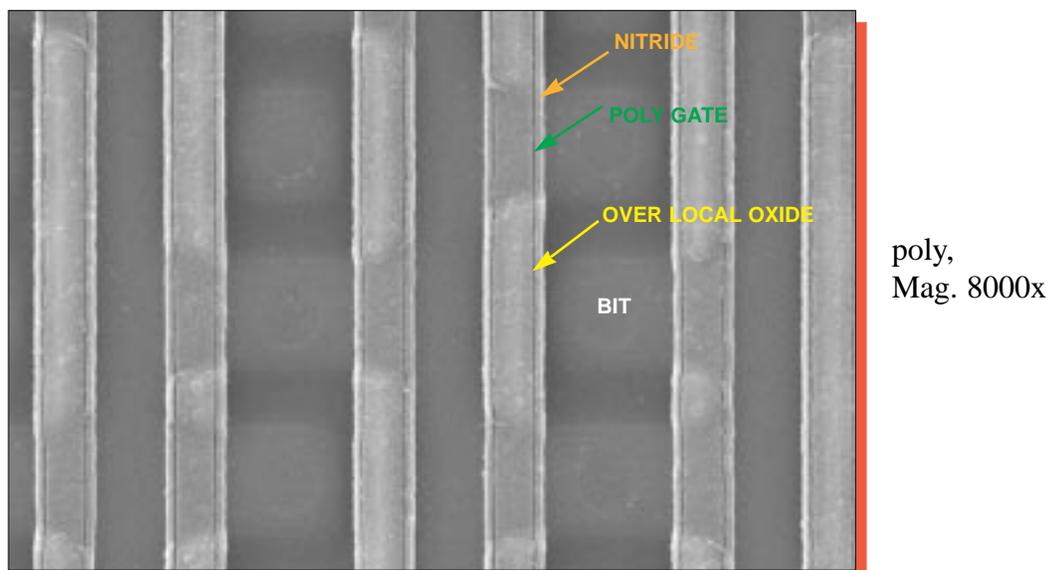
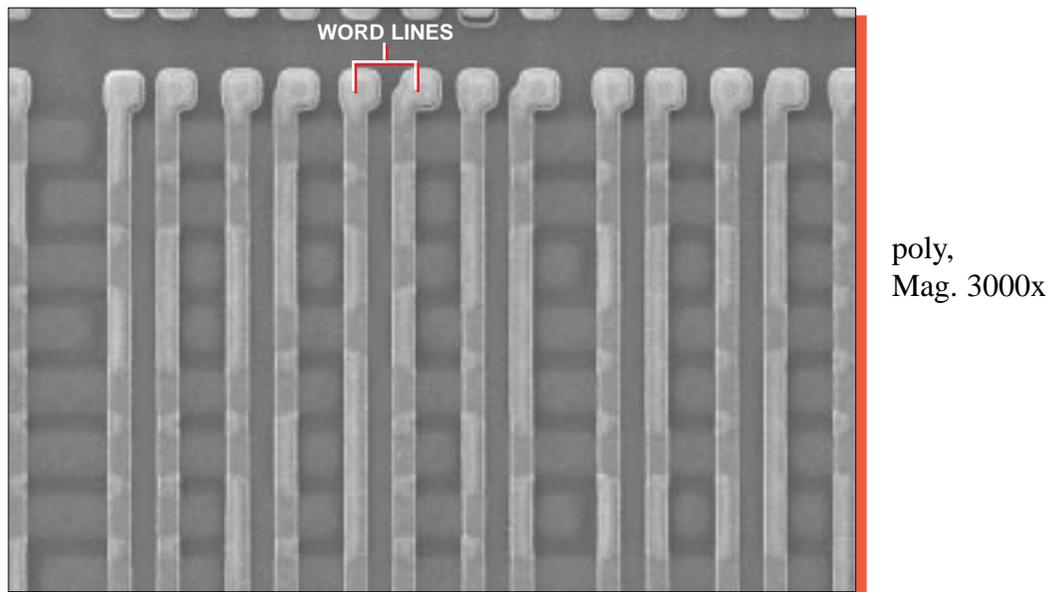
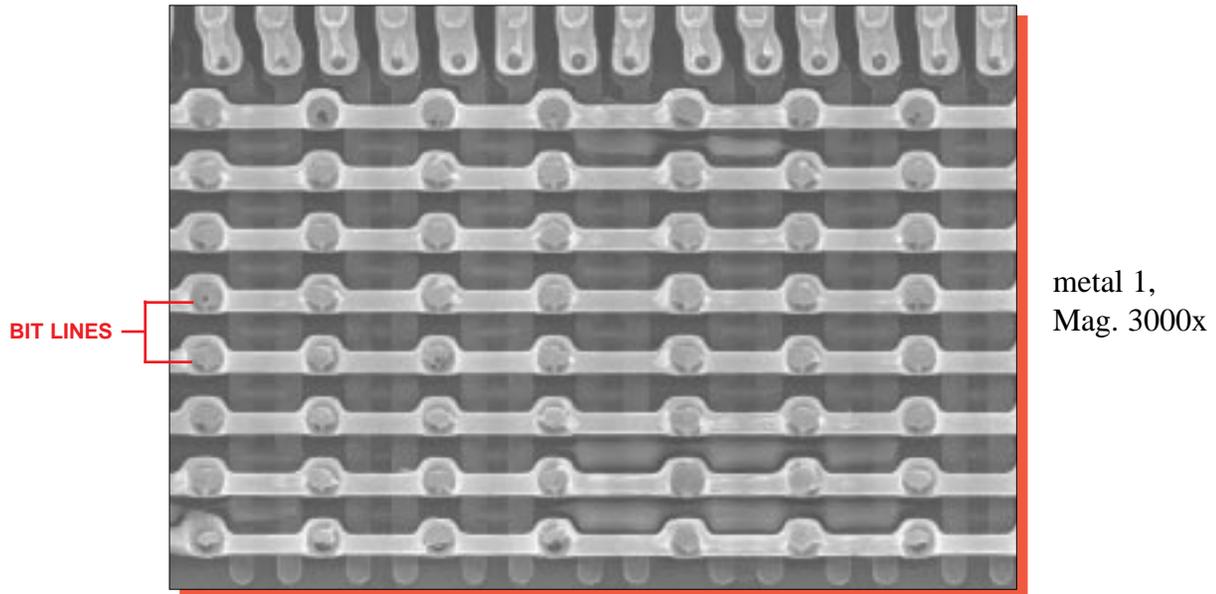
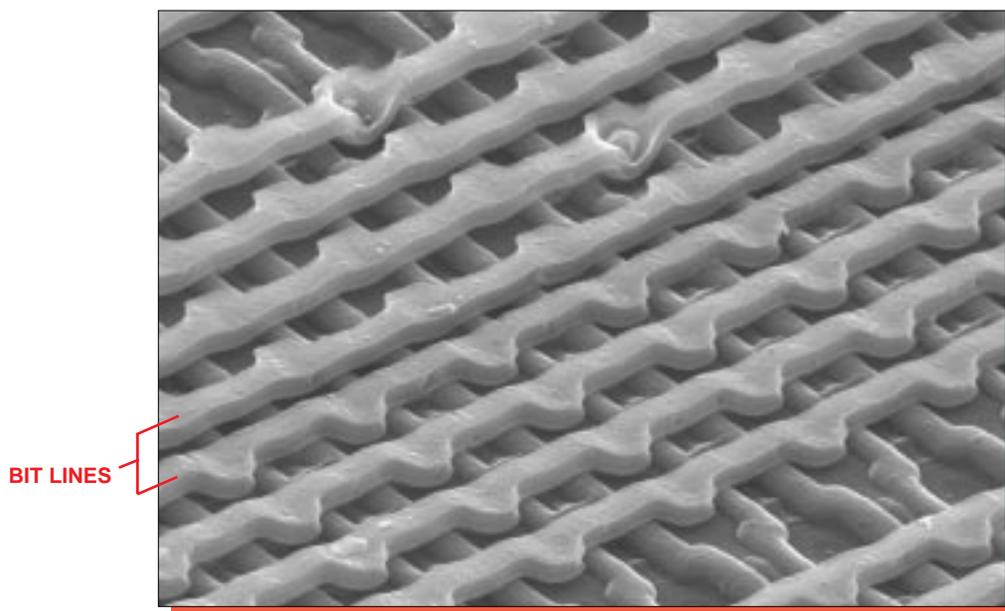
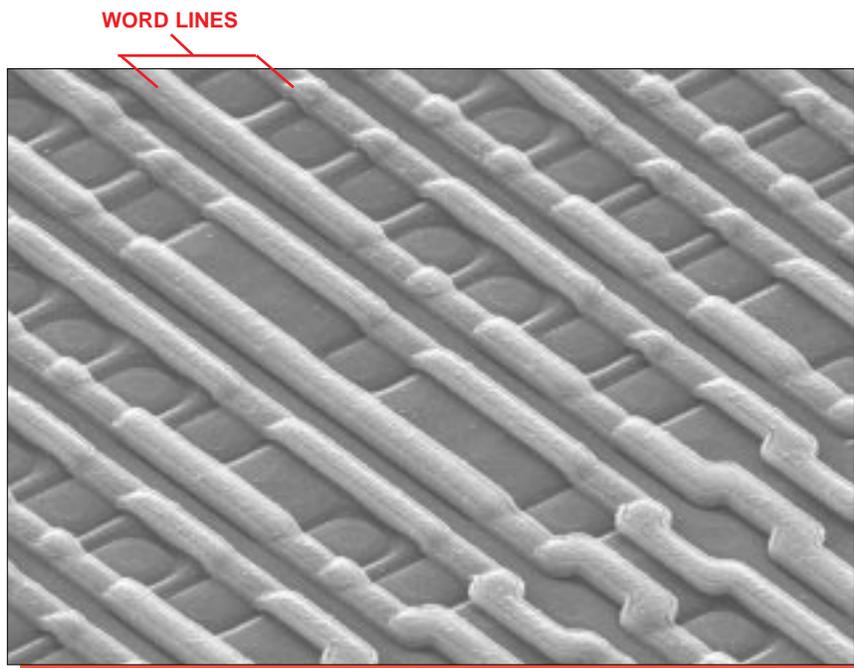


Figure 35. Topological SEM views of a MROM array (array A). 0°.



metal 1



poly

Figure 36. Perspective SEM views of an MROM array (array B). Mag. 5000x, 55°.

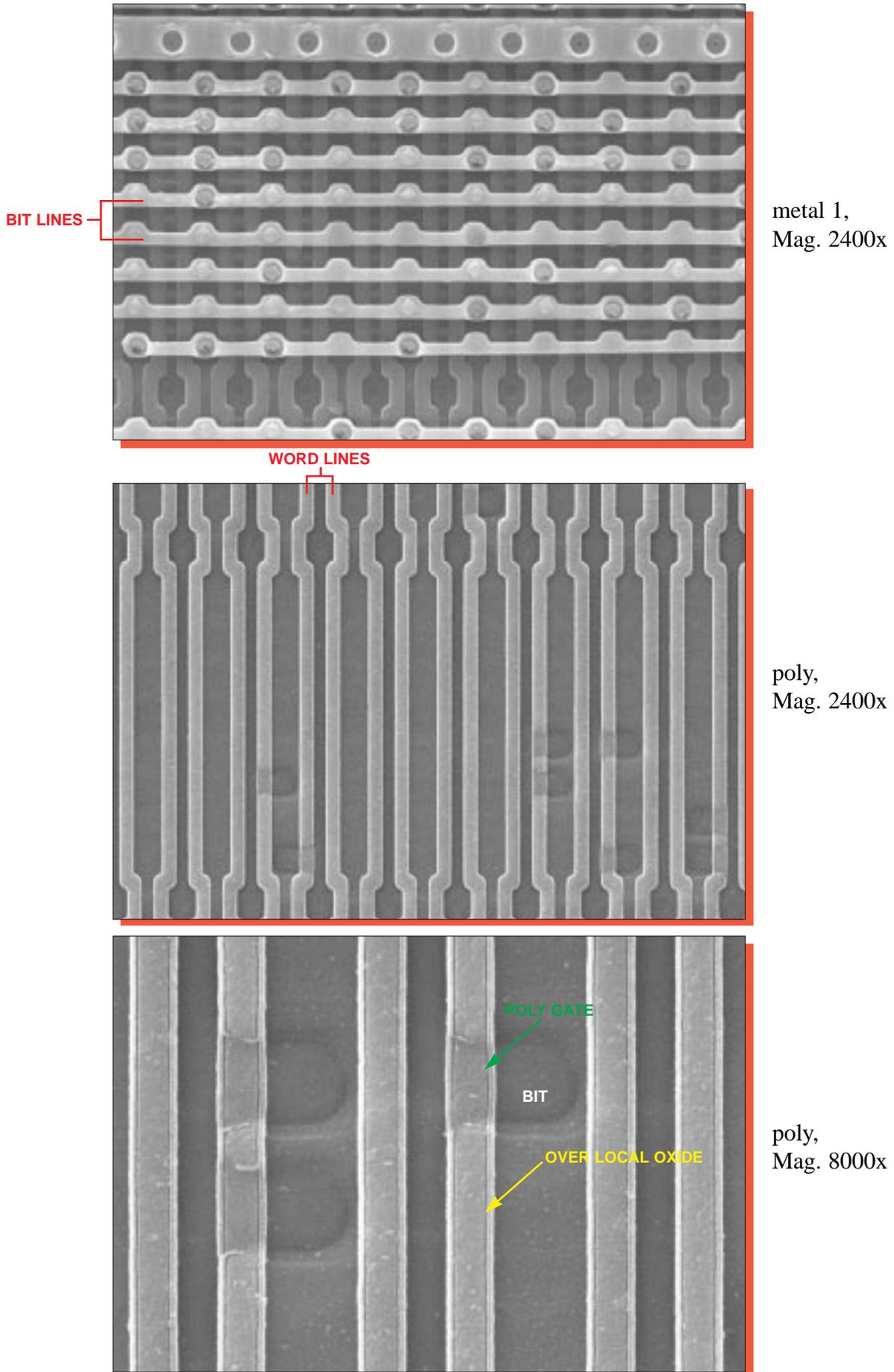
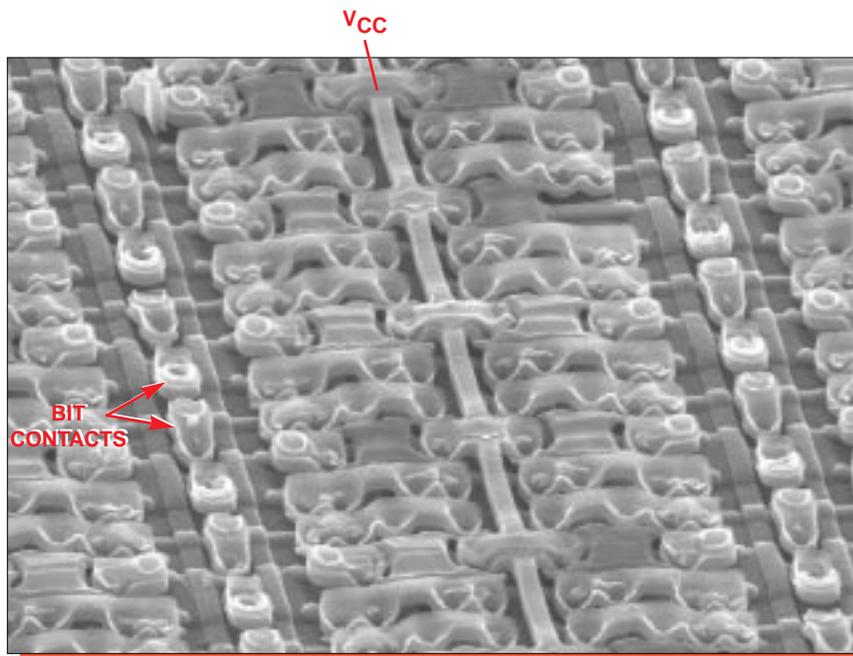
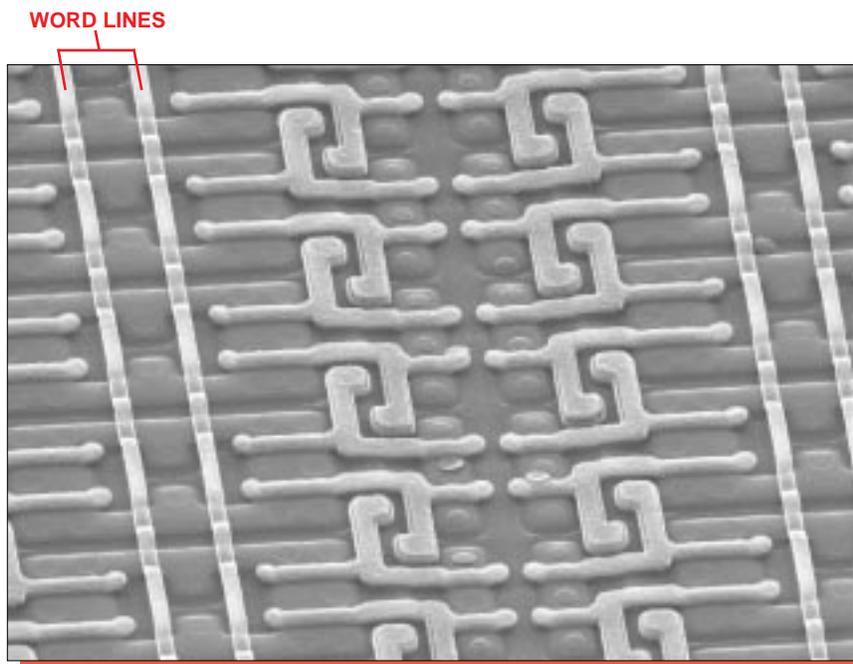


Figure 37. Topological SEM views of a MROM array (array B). 0°.



metal 1



poly

Figure 38. Perspective SEM views of the 6T SRAM array. Mag. 3000x, 55°.

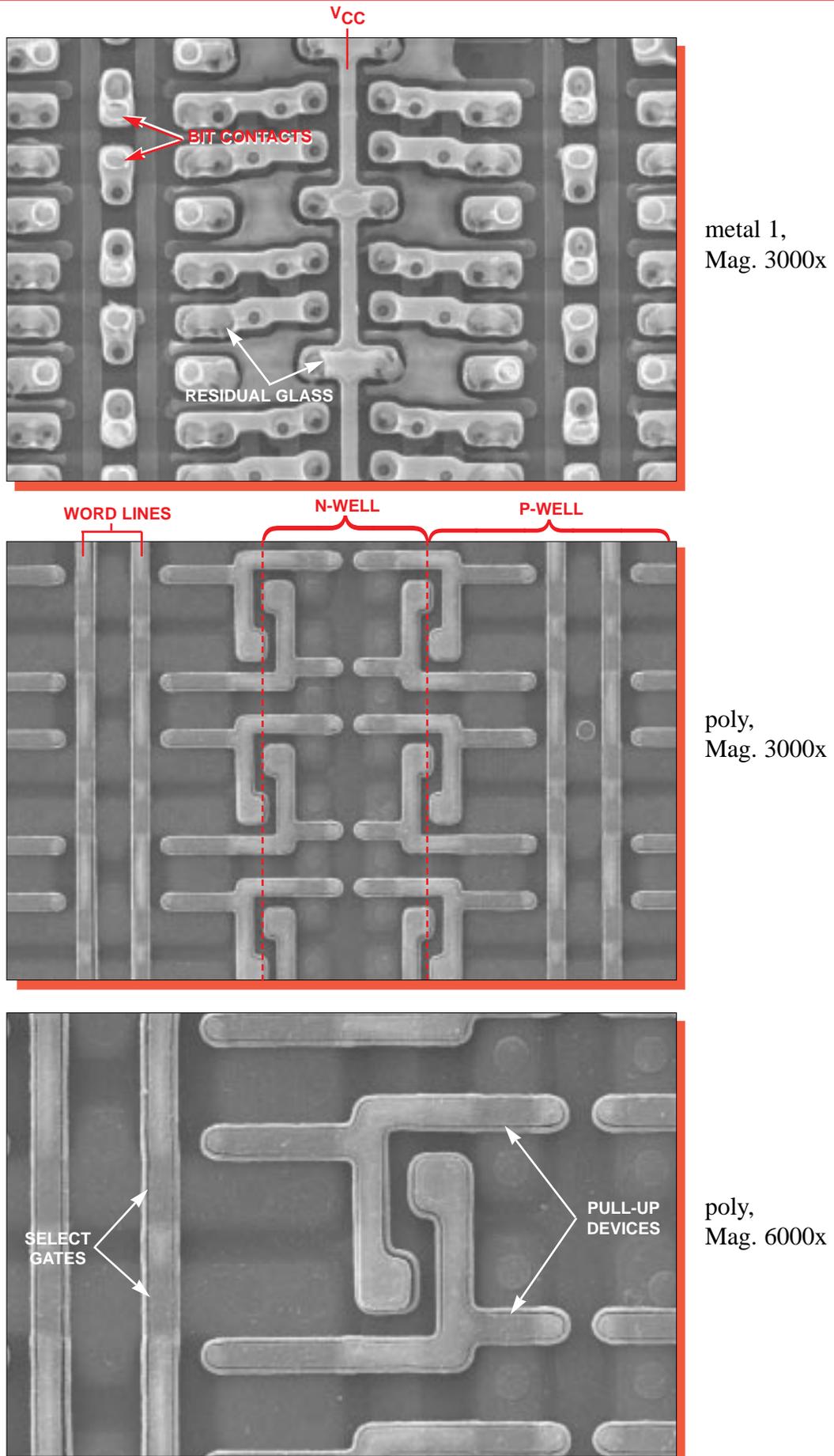
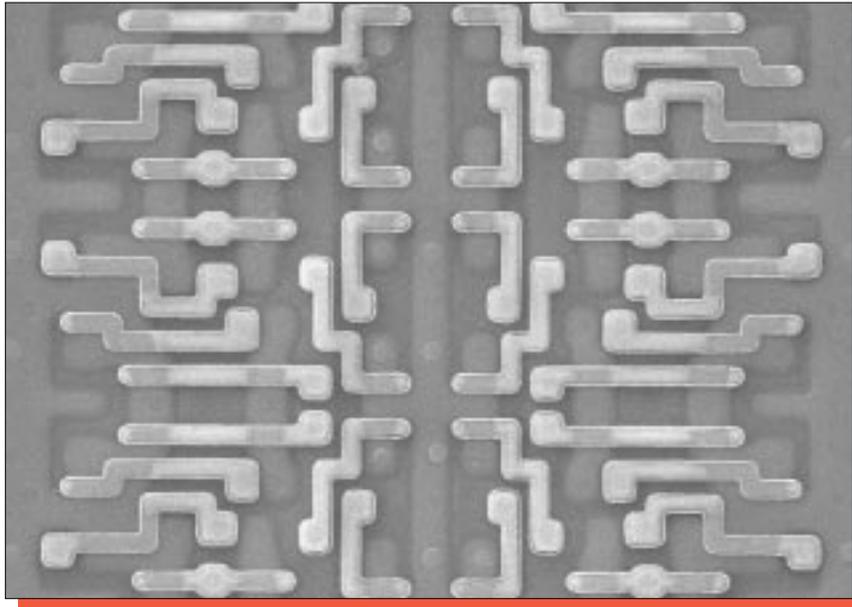
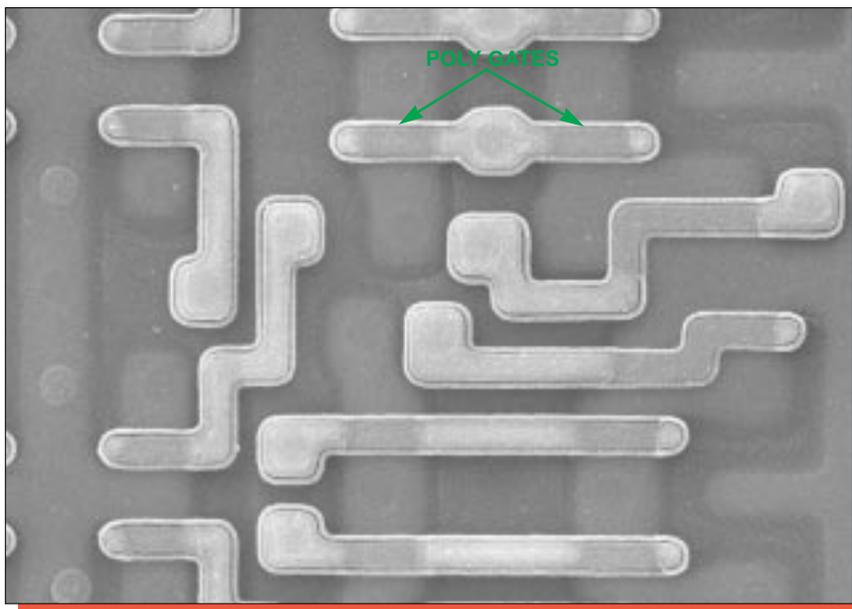


Figure 39. Topological SEM views of the 6T SRAM array. 0°.



Mag. 2500x



Mag. 5000x

Figure 40. Topological delayed views of the 8T SRAM array. 0°.