Construction Analysis

Motorola
MPA1016FN FPGA

Report Number: SCA 9711-561

INTEGRATED CIRCUIT ENGINEERING

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INDEX TO TEXT

INTRODUCTION

This report describes a construction analysis of the Motorola MPA1016FN FPGA. Two devices packaged in 84-pin Plastic Leaded Chip Carriers (PLCCs) and five scribed dice were received for the analysis. These devices were fabricated by Chartered Semiconductor Manufacturing. The packaged devices were date coded 9640.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Three levels of reflowed ("hot") aluminum.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were encapsulated in 84-pin Plastic Leaded Chip Carriers (PLCCs).
- The copper (Cu) leadframe was internally spot-plated with silver (Ag).
- External pins were tinned with tin-lead (SnPb) solder.
- Lead-locking provisions (anchors) at all pins.
- Thermosonic ball bonding using 1.2 mil O.D. gold wire.
- Sawn dicing (full-depth).
- Silver-filled epoxy die attach.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-substrate.
- Final passivation: A layer of nitride over a layer of glass.
- Metallization: Three levels of metal defined by standard dry-etch techniques. Metal 3 and metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and a titanium-nitride/titanium barrier. All three levels of aluminum were reflowed to fill contacts/vias (“hot aluminum”). Standard vias and contacts were used (no plugs).

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectrics: Interlevel dielectrics consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

- Polysilicon: A single layer of polycide (poly cap over titanium silicide on poly) was used to form all gates on the die. Definition was by a dry etch of normal quality. Direct poly-to-diffusion (buried) contacts were not used.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Wells: Twin-wells in a P-substrate. A step was present at well boundaries.

- Redundancy: Fuses were not used.

- Memory cells: Programming is achieved through a modified 6T CMOS SRAM cell. Metal 3 was used to form the bit lines (via metal 2 and metal 1). Metal 2 was used to distribute Vcc and GND (via metal 1). Metal 1 was used to provide cell interconnect. Polycide was used to form all gates and word lines.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 3**

Questionable Items: None.

General Items:

- The devices were encapsulated in 84-pin Plastic Leaded Chip Carriers (PLCCs).
- Overall package quality: Good. Internal spot-plating of the copper leadframe was silver. External pins were tinned with tin-lead (SnPb). No cracks or voids present. No gaps were noted at lead exits.
- Lead-locking provisions (anchors) were present at all pins.
- Wirebonding: Thermosonic ballbond method using 1.2 mil O.D. gold wire. No bond lifts occurred during wirepull tests and bond pull strengths were good.
- Die attach: Silver-filled epoxy of normal quality. No voids were noted in the die attach and no problems are foreseen.
- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

ANALYSIS RESULTS II

Die Process and Design: **Figures 4 - 33**

Questionable Items:[1] None.

Special Features:

- Three levels of reflowed ("hot") aluminum.

General items:

- Fabrication process: Devices were fabricated using selective oxidation CMOS process employing twin-wells in a P-substrate.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

- Die coat: No die coat was present.

- Final passivation: A layer of nitride over a layer of glass. Integrity tests indicated defect-free passivation. Edge seal was good as the passivation extended beyond the metal at the edge of the die.

- Metallization: Three levels of metal defined by standard dry-etch techniques. Metal 3 and metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and a titanium-nitride/titanium barrier. All three levels of aluminum were reflowed to provide excellent step coverage. Standard vias and contacts were used (no plugs).

- Metal patterning: All metal levels were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in any of the metal layers. No silicon nodules were noted following removal of the metal layers.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal step coverage: All three levels of aluminum were reflowed to provide excellent step coverage. No metal thinning occurred at any vias or contacts.

- Interlevel dielectrics: Interlevel dielectrics consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them. The SOG had been etched back.

- Pre-metal dielectric: A layer of reflow glass (BPSG) over densified oxide was used under metal 1. Reflow was performed prior to contact cuts only.

- Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of contacts was noted, but significant overetch was present at vias. This is not a problem in this case since the overetched aluminum is filled by the aluminum that fills the via. No problems were found.

- Polysilicon: A single layer of polycide (poly cap over titanium silicide on poly) was used to form all gates on the die. Definition was by a dry-etch of normal quality. Direct poly-to-diffusion (buried) contacts were not used.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Isolation: LOCOS (local oxide isolation). A step was present at the well boundaries, confirming the presence of twin-wells.

- Redundancy: Fuses were not present on the die.

- Memory cells: Programming is achieved through a modified 6T CMOS SRAM cell. Metal 3 was used to form the bit lines (via metal 2 and metal 1). Metal 2 was used to distribute Vcc and GND (via metal 1). Metal 1 was used to provide cell interconnect. Polycide was used to form all gates and word lines.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 3

Delayer to metal 2 and inspect

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity	G
Package markings	N
Die placement	N
Die attach quality	G
Wire spacing	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	G
Wirebond method	Thermosonic ball bond method using 1.2 mil O.D. gold wire.
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	G
Metal registration	G
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

(LOGO)
MPA1016FN
ZQUAL9640

WIREBOND STRENGTH

Wire material:	1.2 mil O.D. gold
Die pad material:	aluminum
Material at package lands:	silver

Sample #	**1**
# of wires tested:	20
Bond lifts:	0
Force to break - high:	15.0g
- low:	11.0g
- avg.:	13.0g
- std. dev.:	0.3

DIE MATERIAL ANALYSIS

Final passivation:	A layer of silicon-nitride over a layer of glass.
Metallization 3:	Aluminum (Al) with a titanium-nitride (TiN) cap and titanium (Ti) barrier.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and titanium (Ti) barrier.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and titanium-nitride/titanium barrier.
Polycide:	Polysilicon cap over Titanium (Ti) silicide on poly.

HORIZONTAL DIMENSIONS

Die size:	6.1 x 6.2 mm (241 x 245 mils)
Die area:	38 mm^2 (59,045 $mils^2$)
Min pad size:	0.1 x 0.1 mm (3.9 x 4.0 mils)
Min pad window:	0.09 x 0.09 mm (3.5 x 3.6 mils)
Min pad space:	0.04 mm (1.4 mils)
Min metal 3 width:	1.0 micron
Min metal 3 space:	1.2 micron
Min metal 3 pitch:	2.2 microns
Min metal 2 width:	0.9 micron
Min metal 2 space:	1.2 micron
Min metal 2 pitch:	2.1 microns
Min metal 1 width:	0.6 micron
Min metal 1 space:	0.8 micron
Min metal 1 pitch:	1.5 micron
Min via (M3-to-M2):	0.6 micron (round)
Min via (M2-to-M1):	0.6 micron (round)
Min contact:	0.8 micron (round)
Min polycide width:	0.5 micron
Min polycide space:	1.0 micron
Min gate length* - (N-channel):	0.5 micron
- (P-channel):	0.5 micron

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (19 mils)

Layers

Passivation 2:	0.6 micron
Passivation 1:	0.4 micron
Metal 3 - cap:	0.05 micron (approx.)
- aluminum:	0.8 micron
- barrier:	0.12 micron
Intermetal dielectric 2 - glass 2:	0.4 micron (average)
- SOG:	0 - 0.8 micron
- glass 1:	0.4 micron (average)
Metal 2 - cap:	0.05 micron (approx.)
- aluminum:	0.5 micron
- barrier:	0.1 micron
Intermetal dielectric 1 - glass 2:	0.4 micron (average)
- SOG:	0 - 0.8 micron
- glass 1:	0.4 micron (average)
Metal 1 - cap:	0.05 micron (approx.)
- aluminum:	0.5 micron
- TiN/ Ti barrier:	0.17 micron
Pre-metal glass:	0.4 micron (avg.)
Poly - poly cap:	0.02 micron (approx.)
- silicide:	0.15 micron
- poly:	0.2 micron
Local oxide:	0.4 micron
N+ S/D diffusion:	0.25 micron
P+ S/D diffusion:	0.25 micron
N-well:	2.5 microns (approx.)

INDEX TO FIGURES

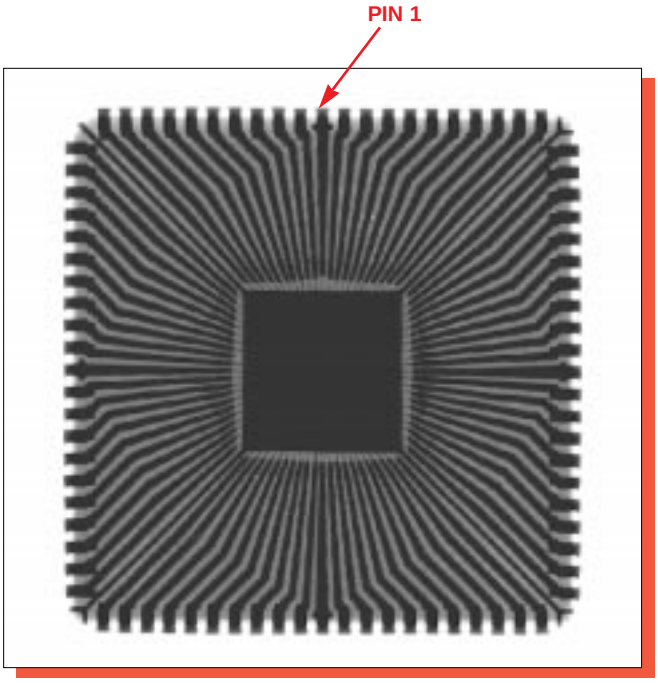
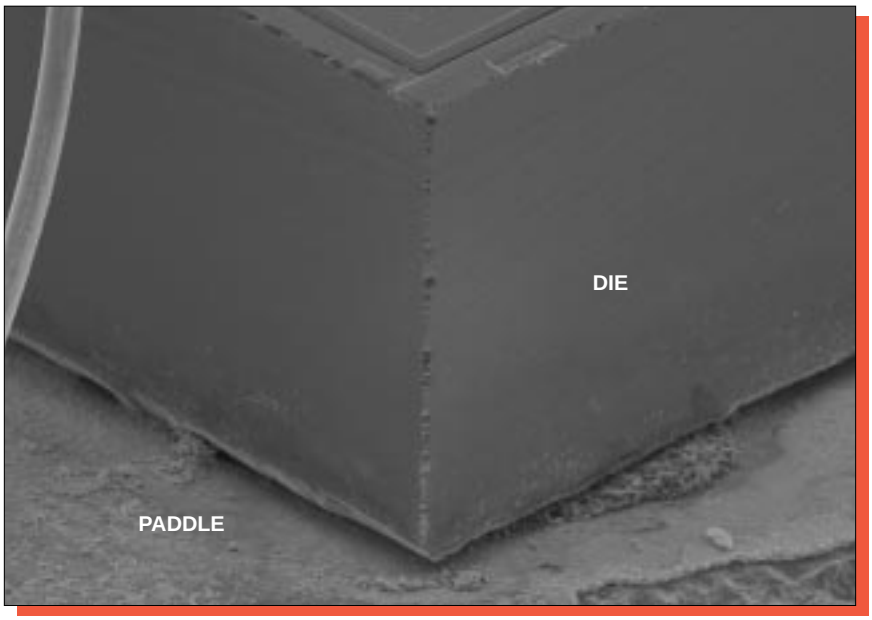


Figure 1. Package photograph and x-ray of the Motorola MPA1016FN FPGA.
Mag. 2.3x.



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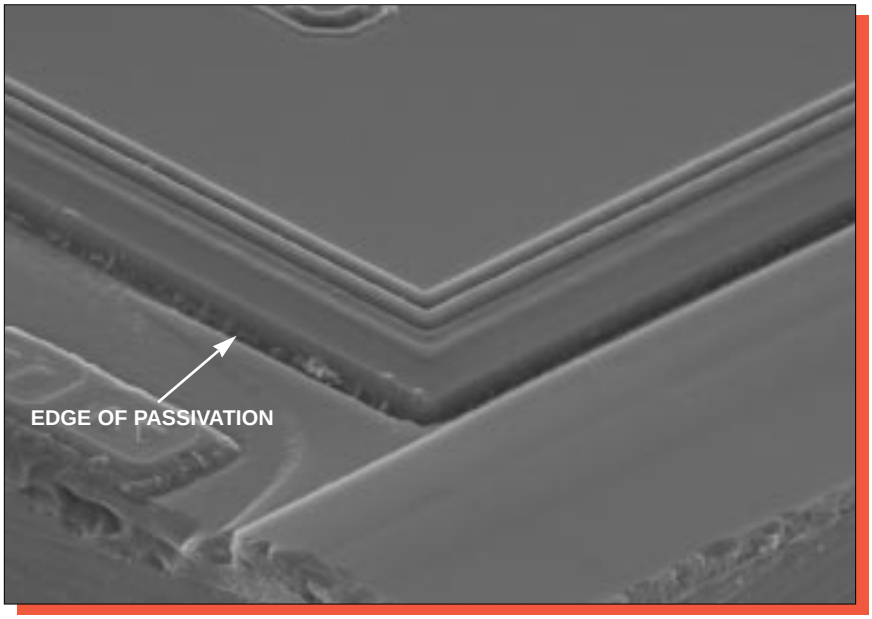
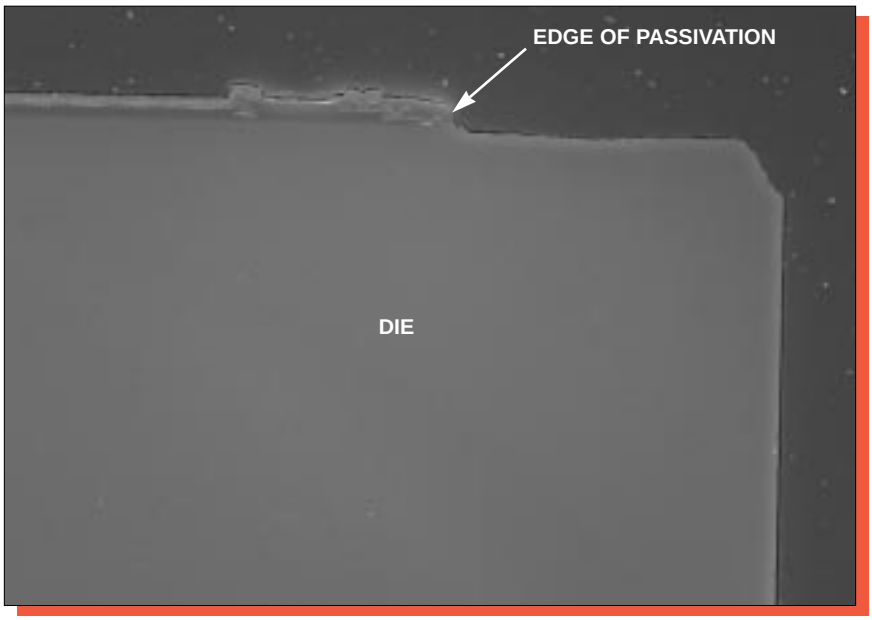
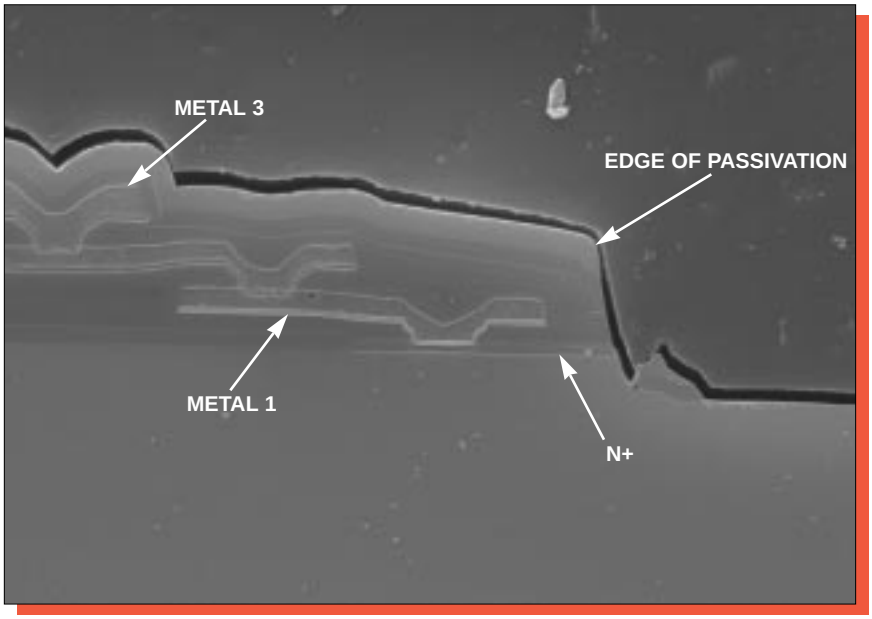


Mag. 1000x

Figure 2. SEM views illustrating dicing and edge seal. 60°.



Mag. 810x



Mag. 5000x

Figure 3. SEM section views of the edge seal.

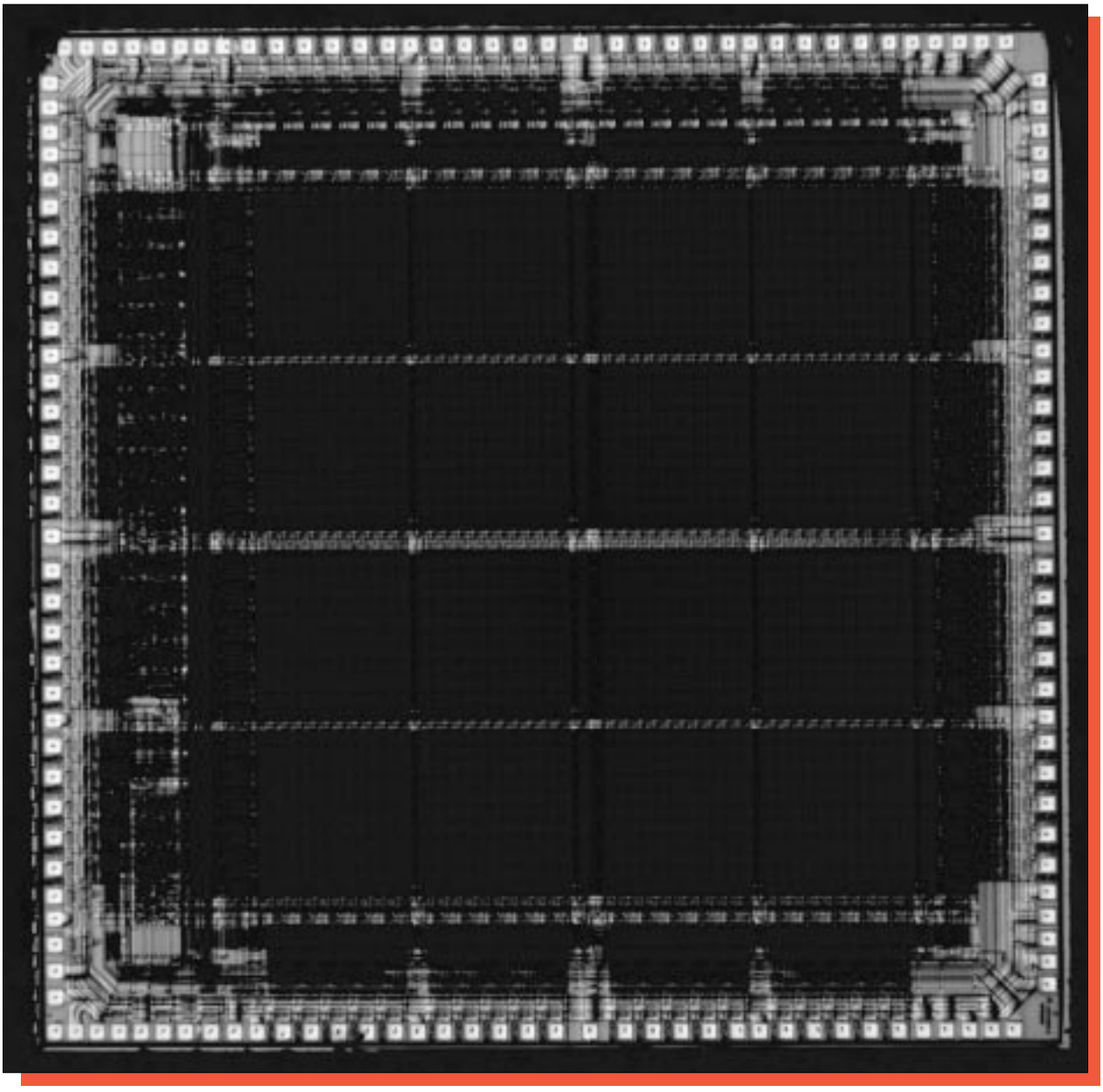
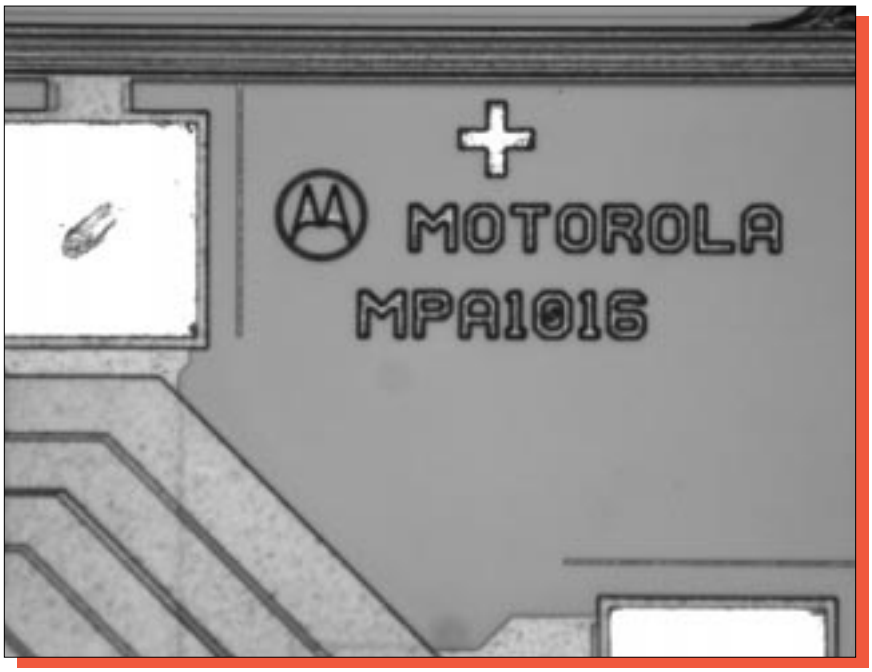


Figure 4. Whole die photograph of the Motorola MPA1016FN FPGA. Mag. 26x.



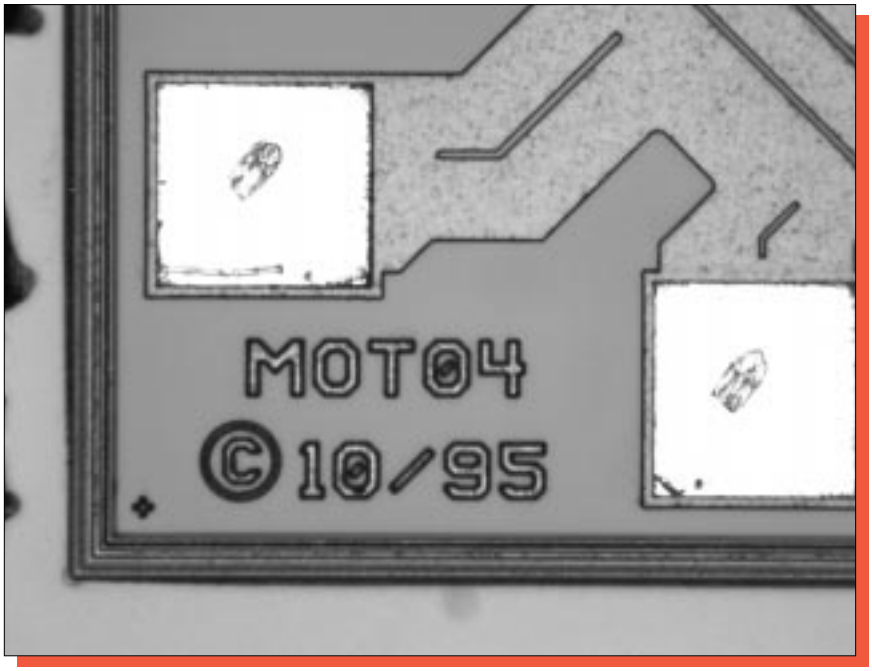


Figure 5. Optical views of die markings. Mag. 300x.

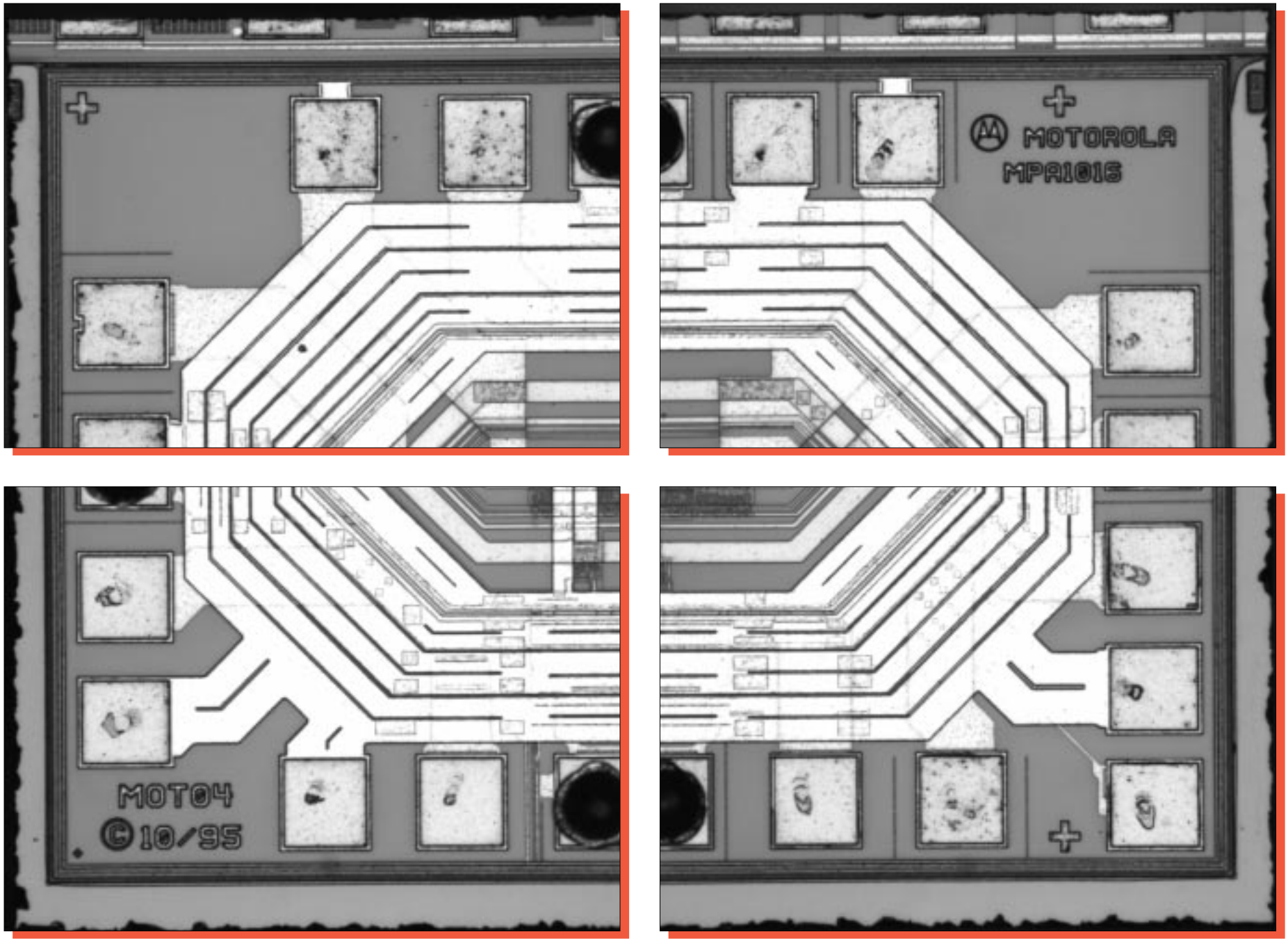
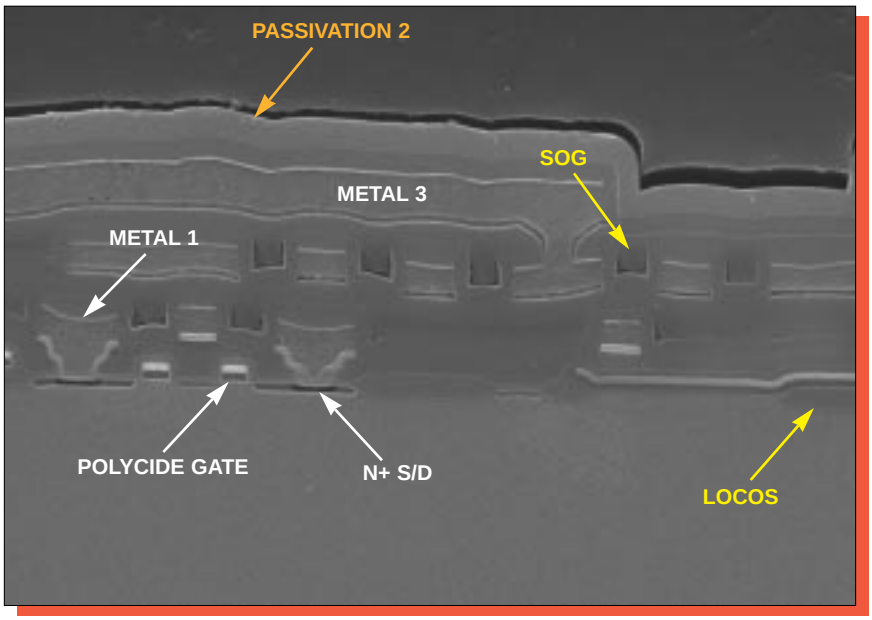
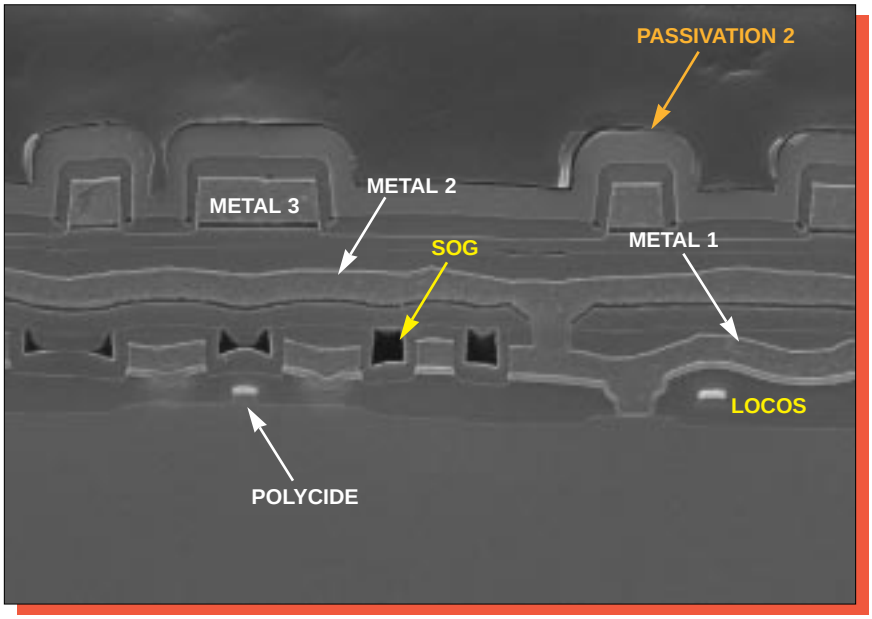


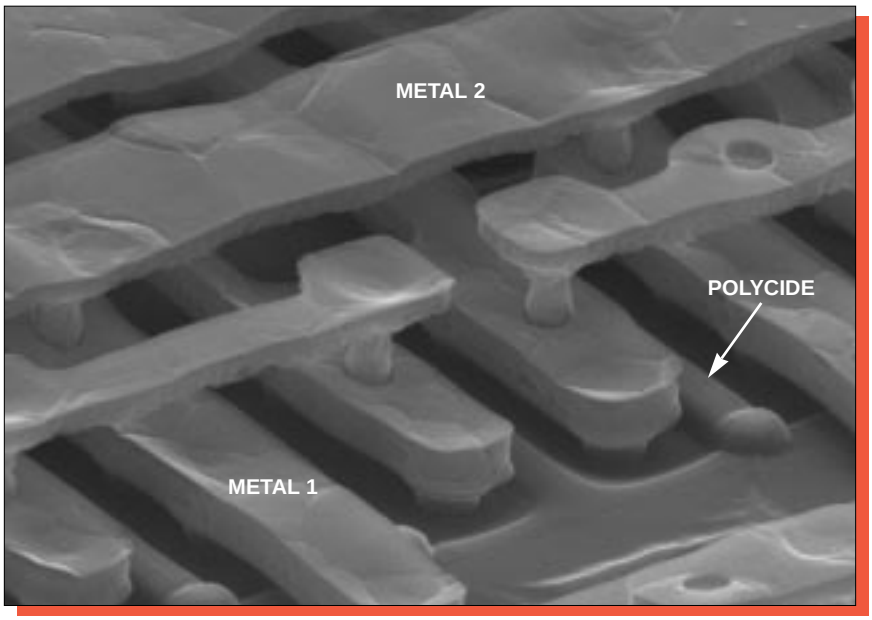
Figure 6. Optical views of die corners. Mag. 170x.





glass etch

Figure 7. SEM section views illustrating general structure. Mag. 6500x



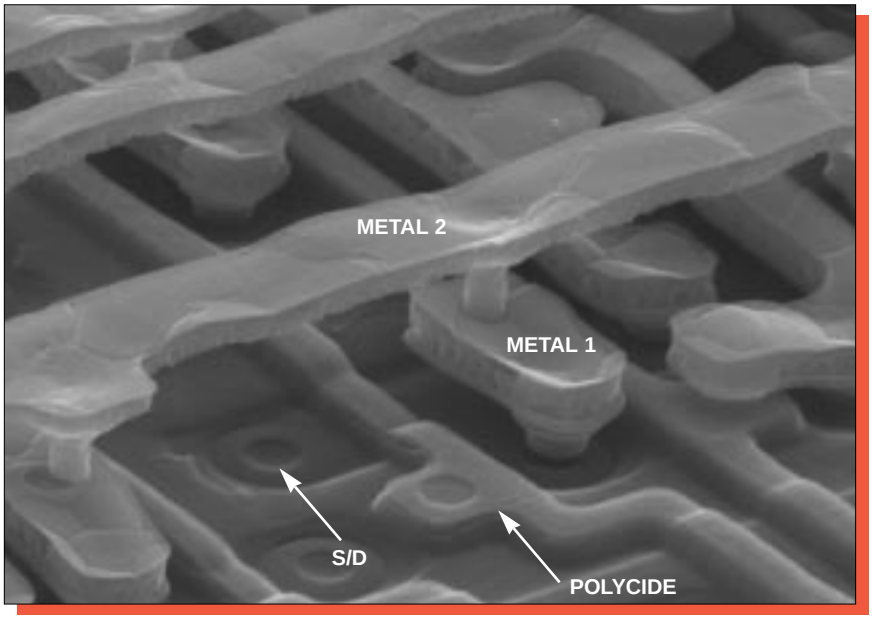
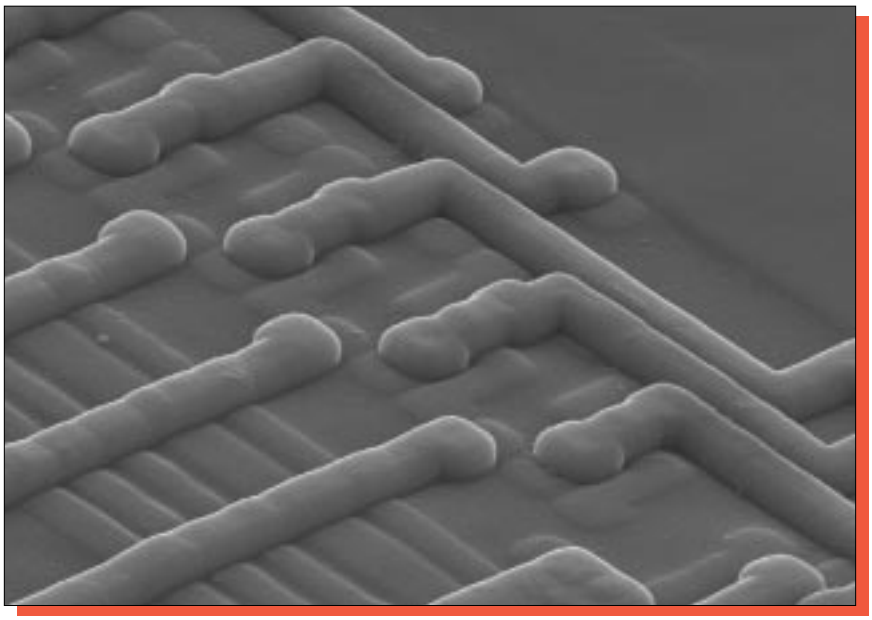
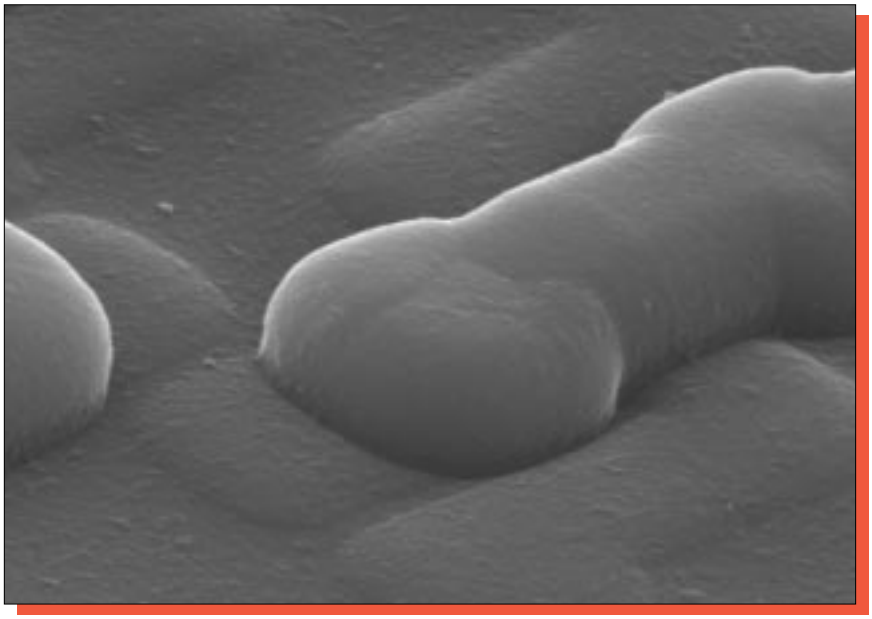


Figure 8. Perspective SEM views illustrating general structure. Mag. 10,000x, 60°.

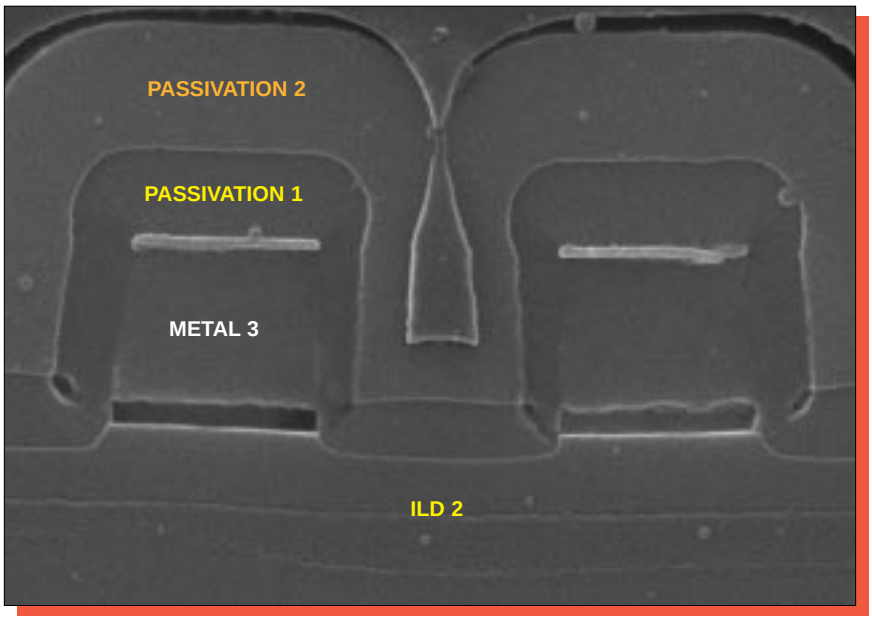


Mag. 3,200x

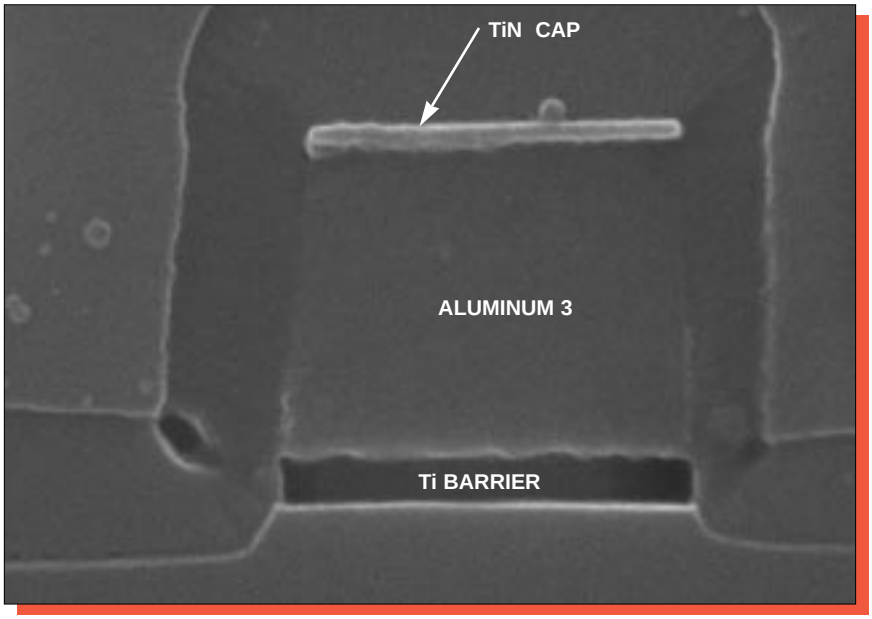


Mag. 13,000x

Figure 9. SEM views illustrating final passivation. 60°.



Mag. 26,000x



Mag. 52,000x

Figure 10. SEM section views of metal 3 line profiles.

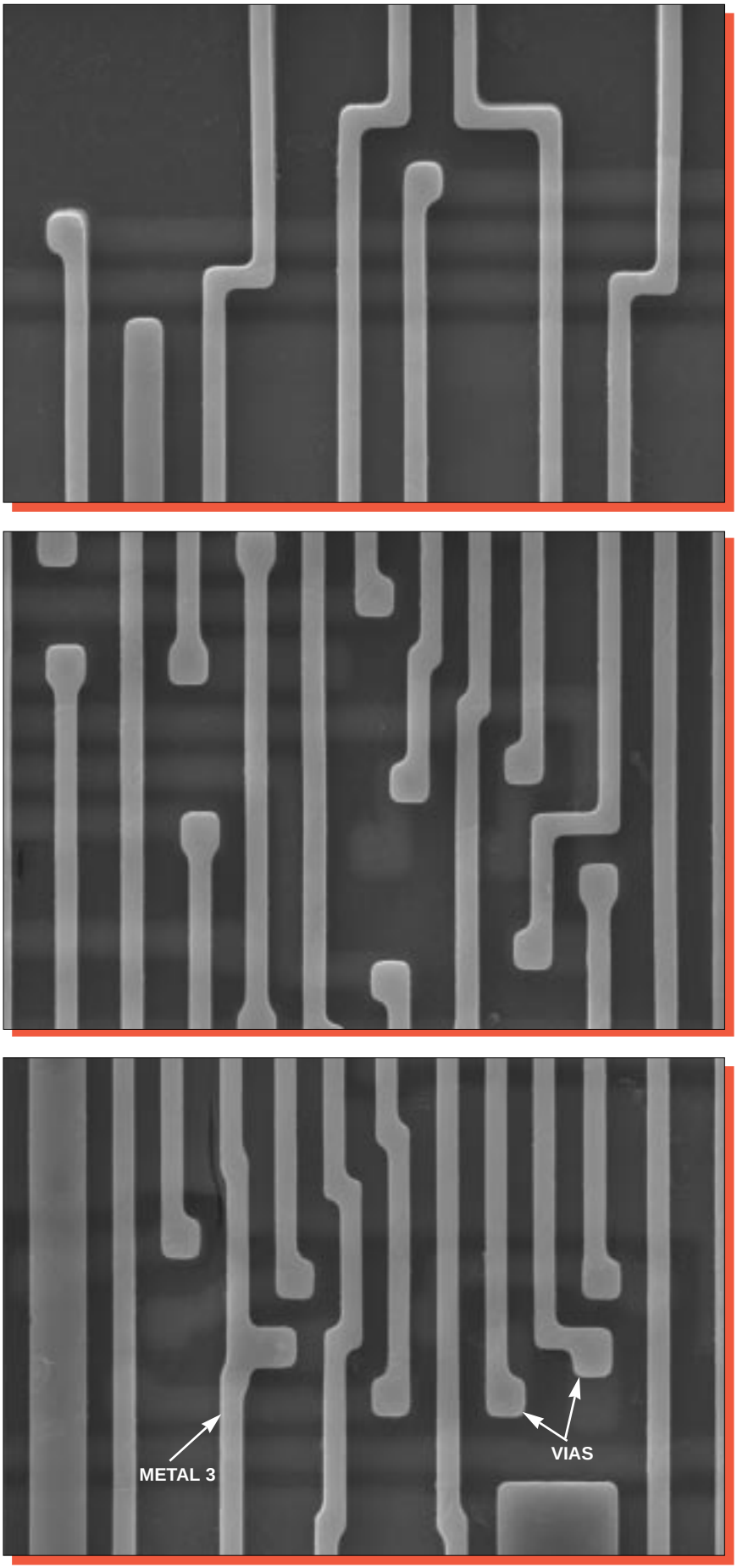
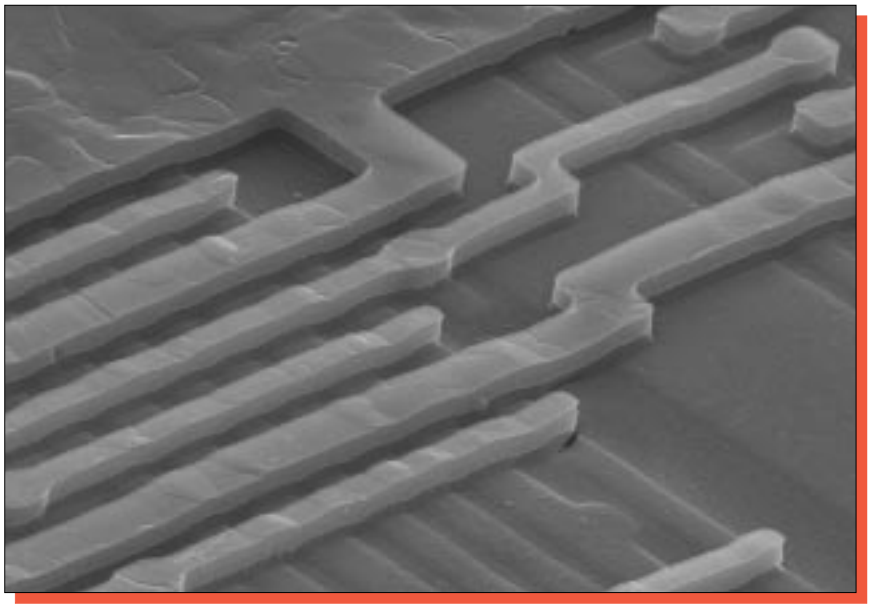
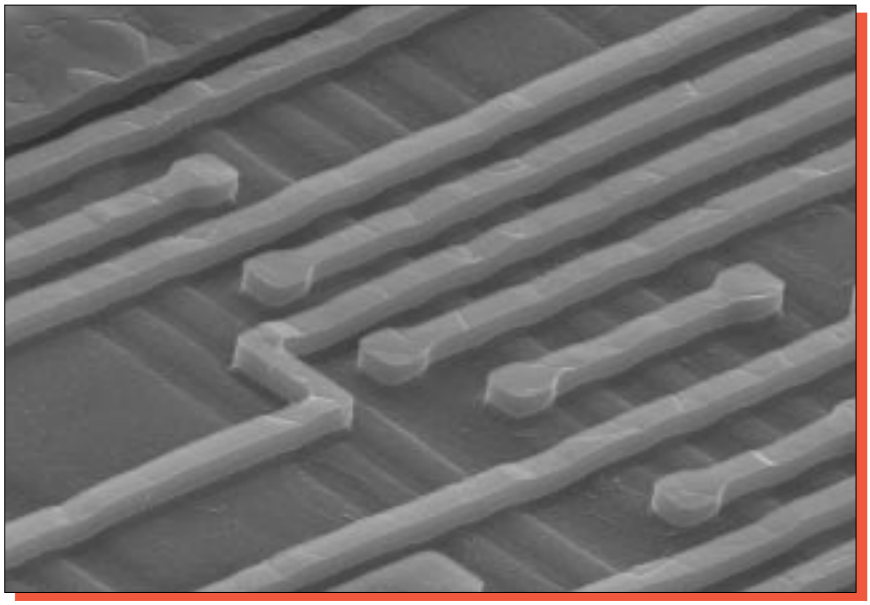


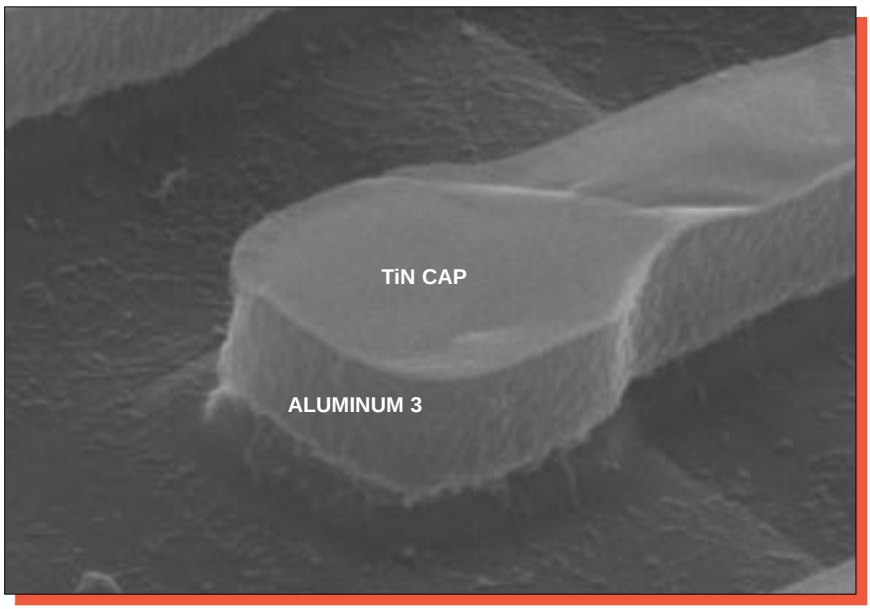
Figure 11. Topological SEM views of metal 3 patterning. Mag. 3200x, 0°.



Mag. 4200x

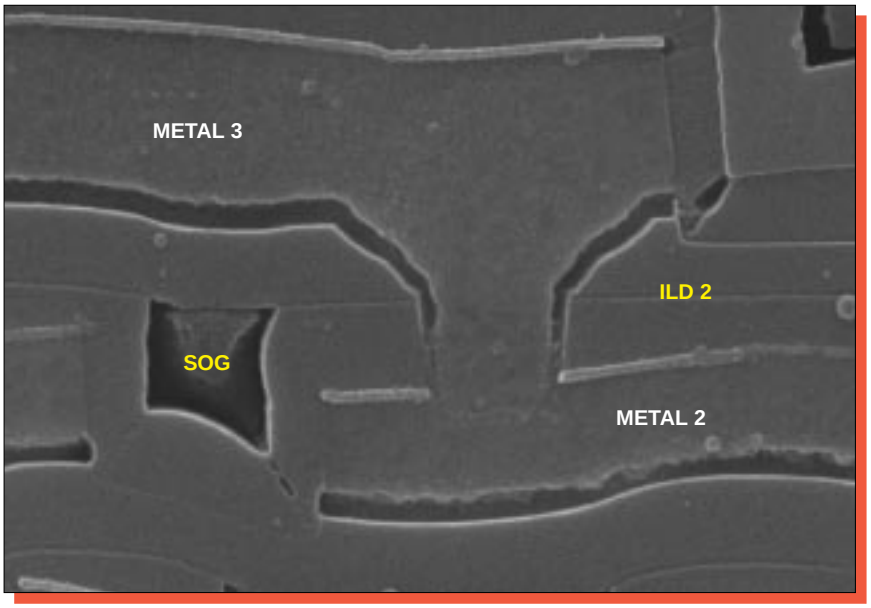


Mag. 4200x

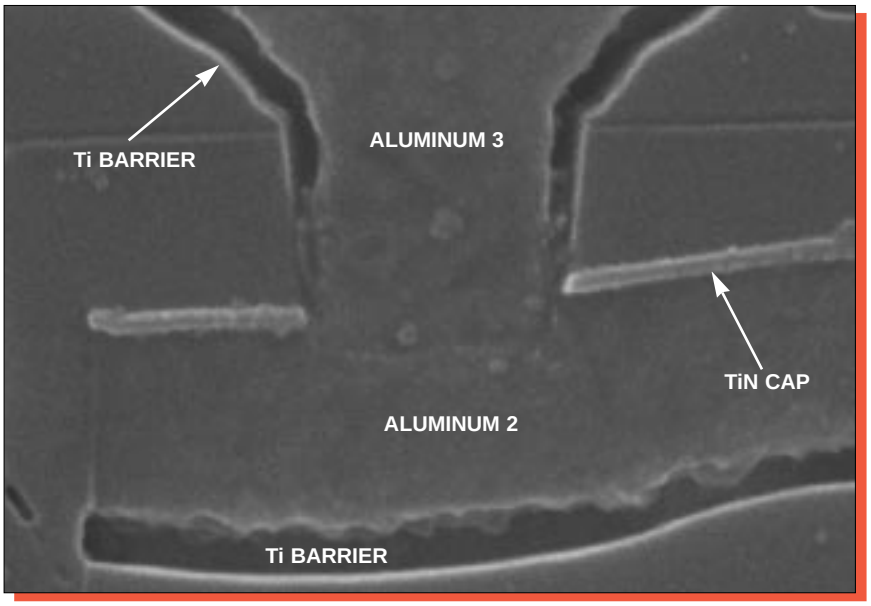


Mag. 26,000x

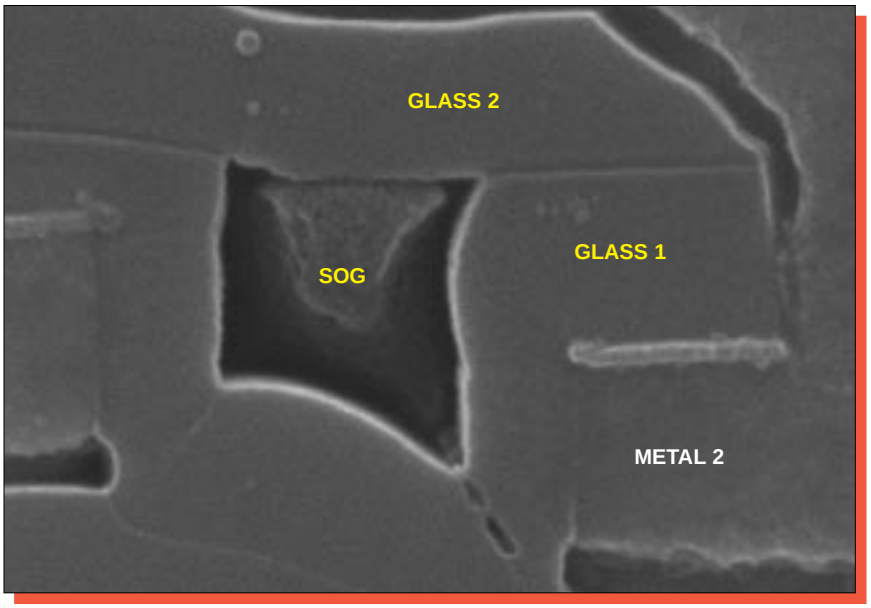
Figure 12. Perspective SEM views of metal 3 step coverage. 60°.



Mag. 26,000x

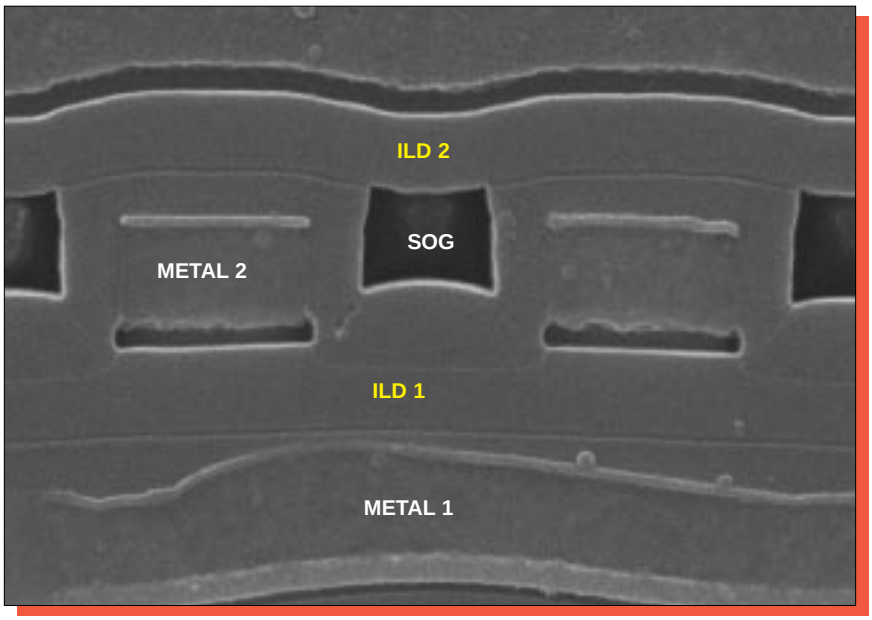


Mag. 52,000x



Mag. 52,000x

Figure 13. SEM section views illustrating a typical M3-to-M2 via and interlevel dielectric 2 composition.



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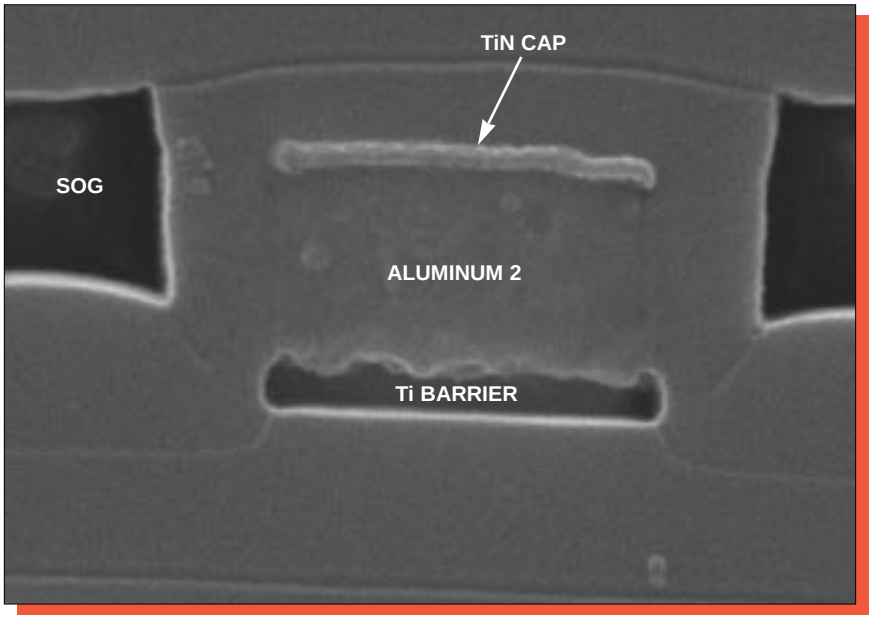
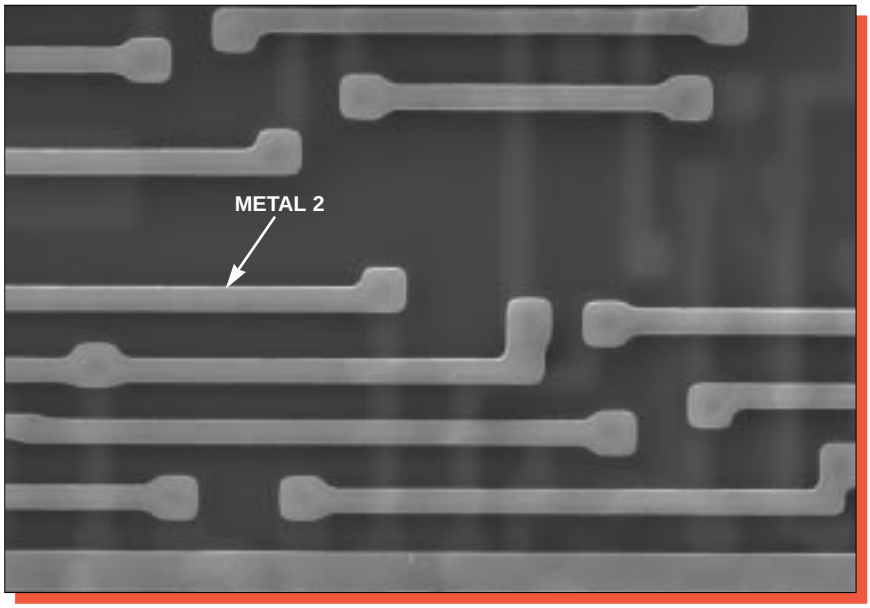
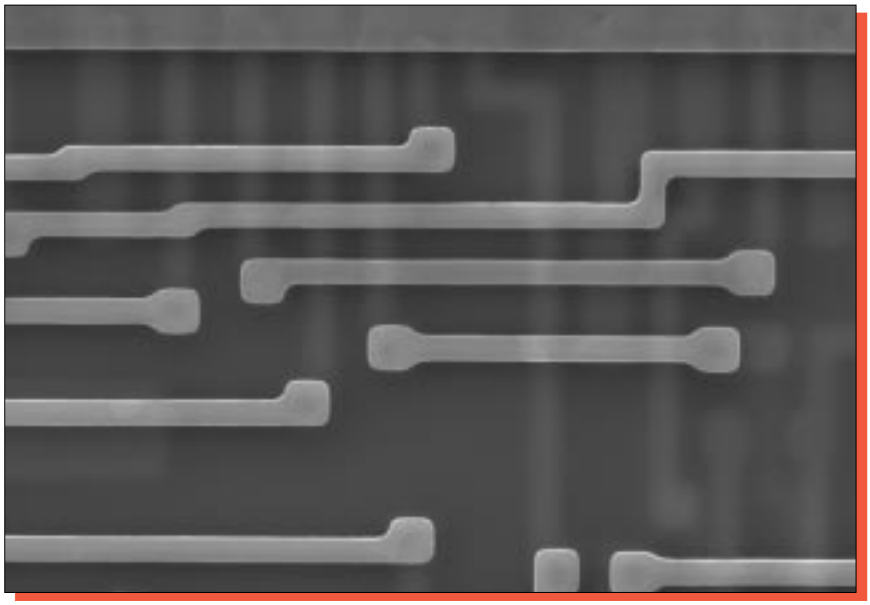


Mag. 52,000x

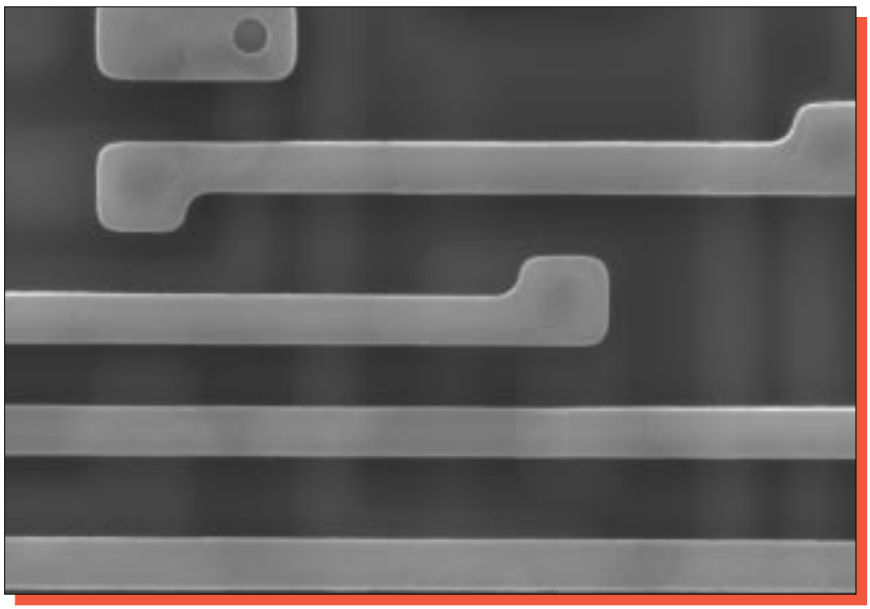
Figure 14. SEM section views of metal 2 line profiles.



Mag. 3200x

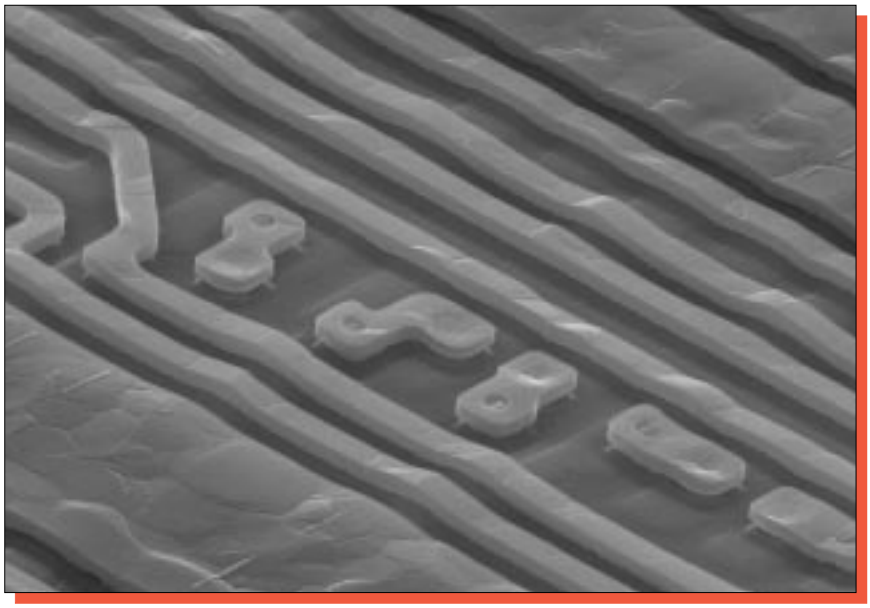


Mag. 3200x

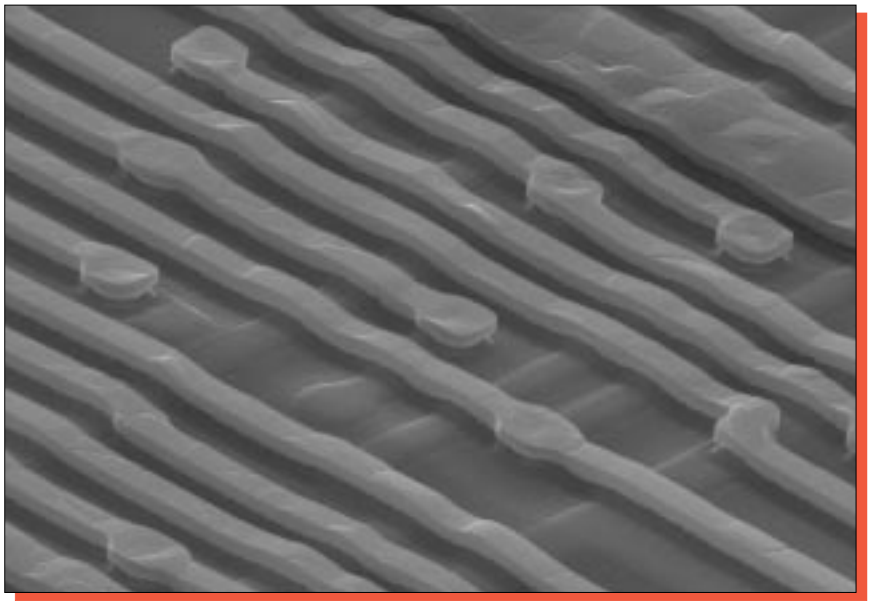


Mag. 6500x

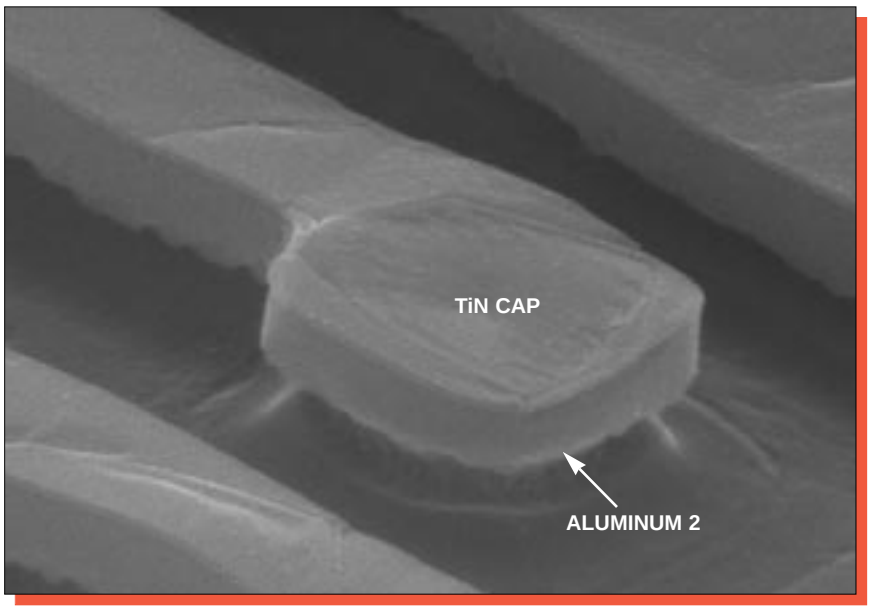
Figure 15. Topological SEM views of metal 2 patterning. 0°.



Mag. 5000x

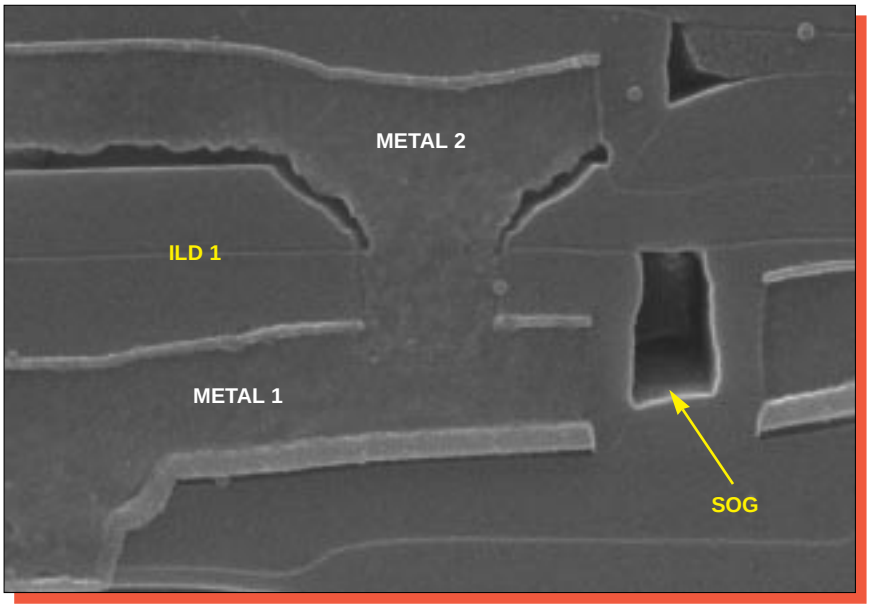


Mag. 5000x

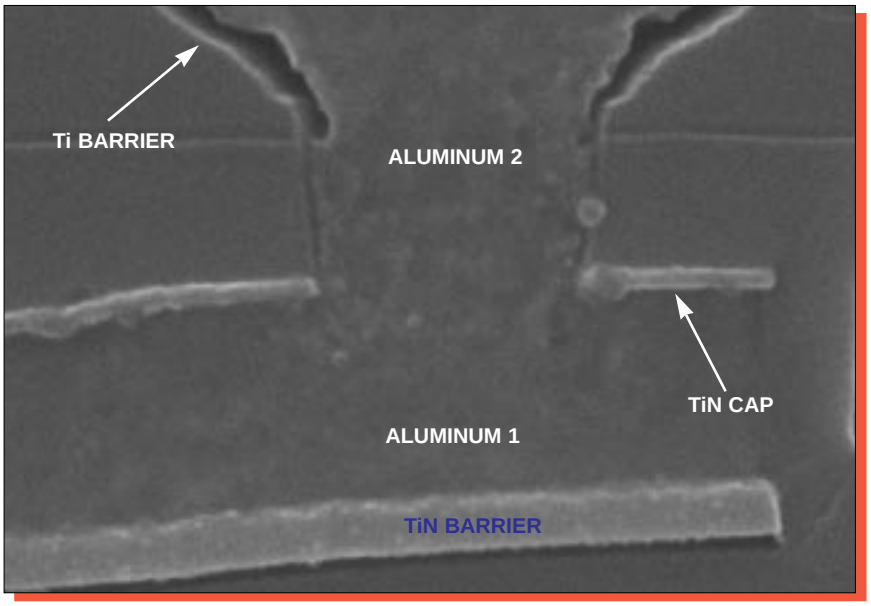


Mag. 30,000x

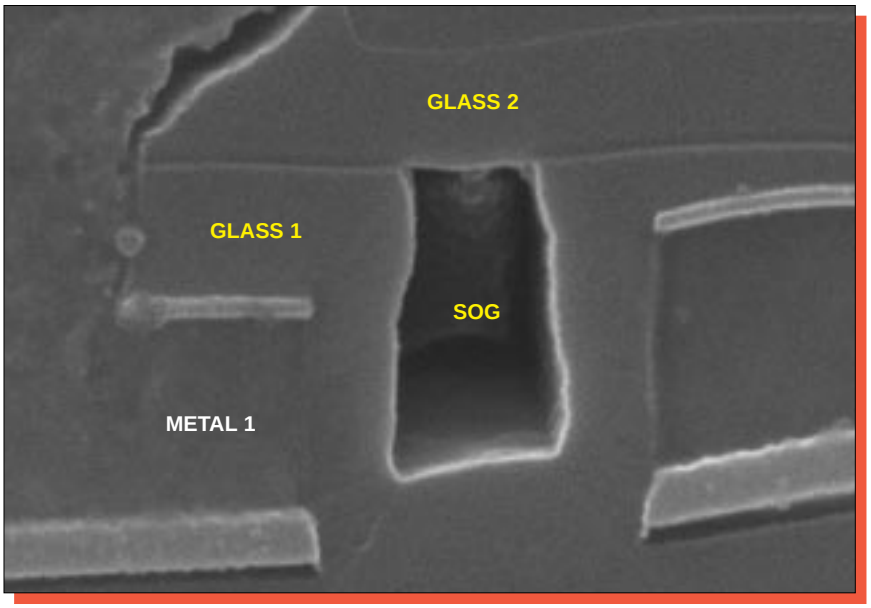
Figure 16. Perspective SEM views of metal 2 step coverage. 60°.



Mag. 26,000x

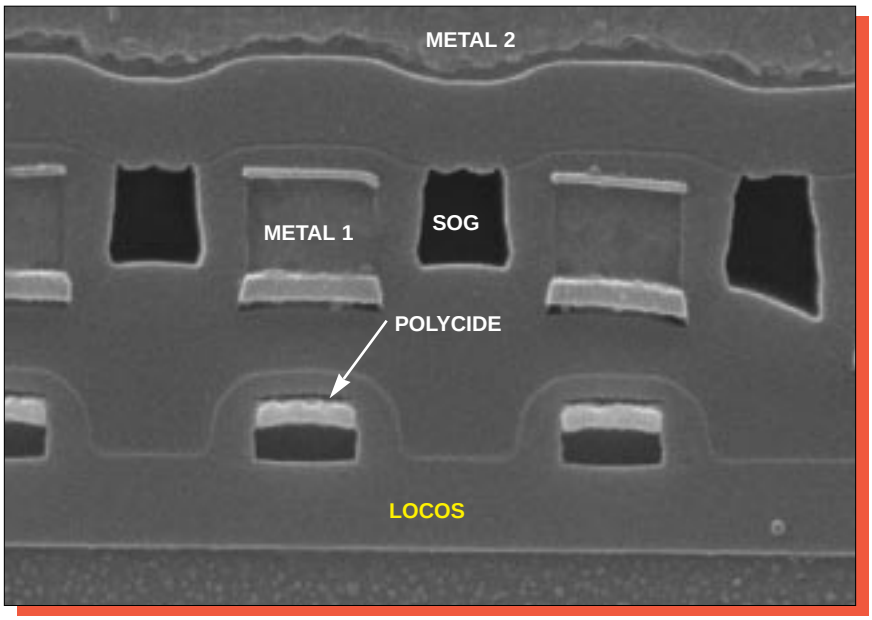


Mag. 52,000x

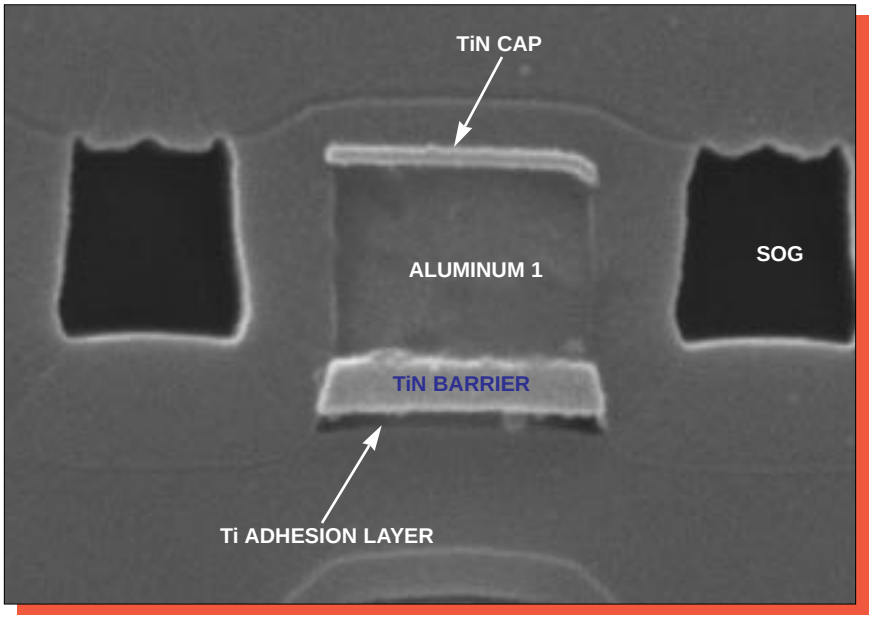


Mag. 52,000x

Figure 17. SEM section views illustrating a typical M2-to-M1 via and interlevel dielectric 1 composition.

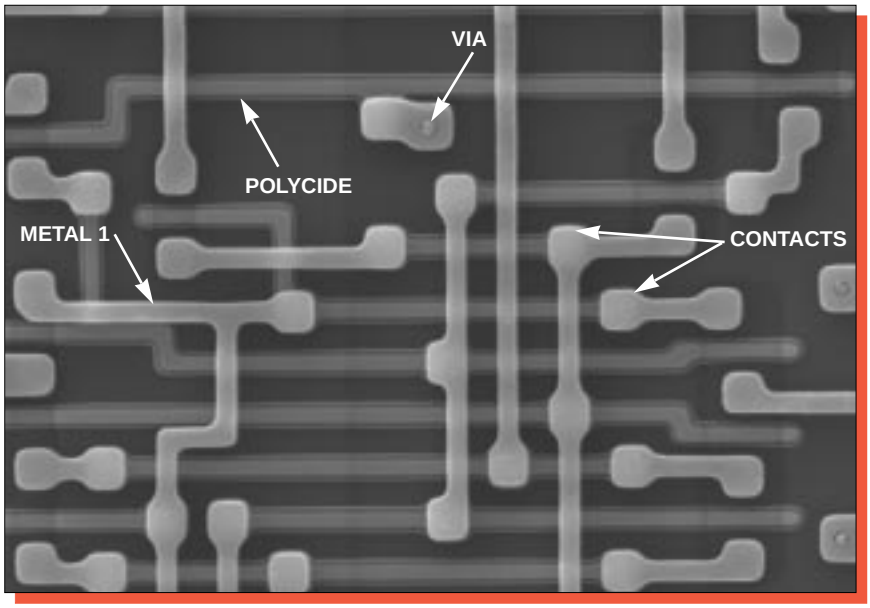


Mag. 26,000x

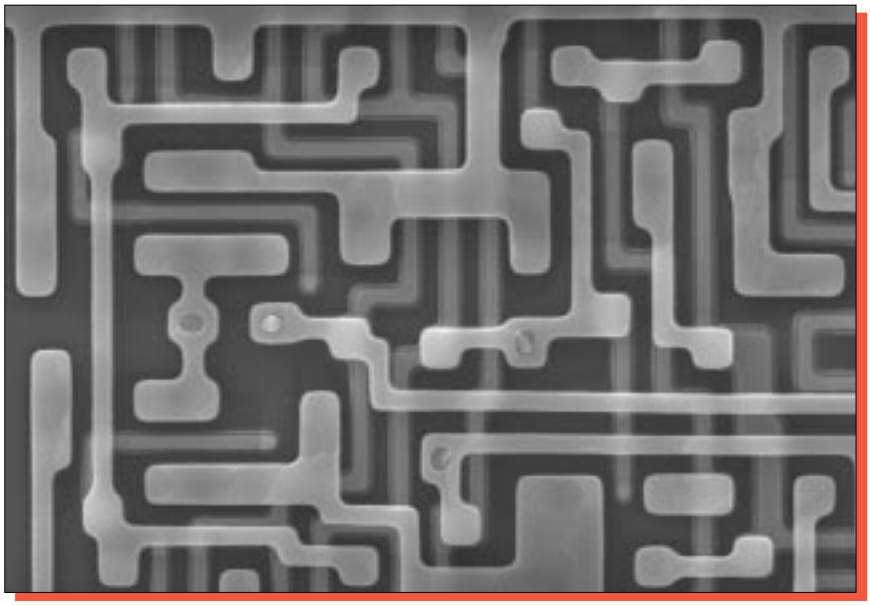


Mag. 52,000x

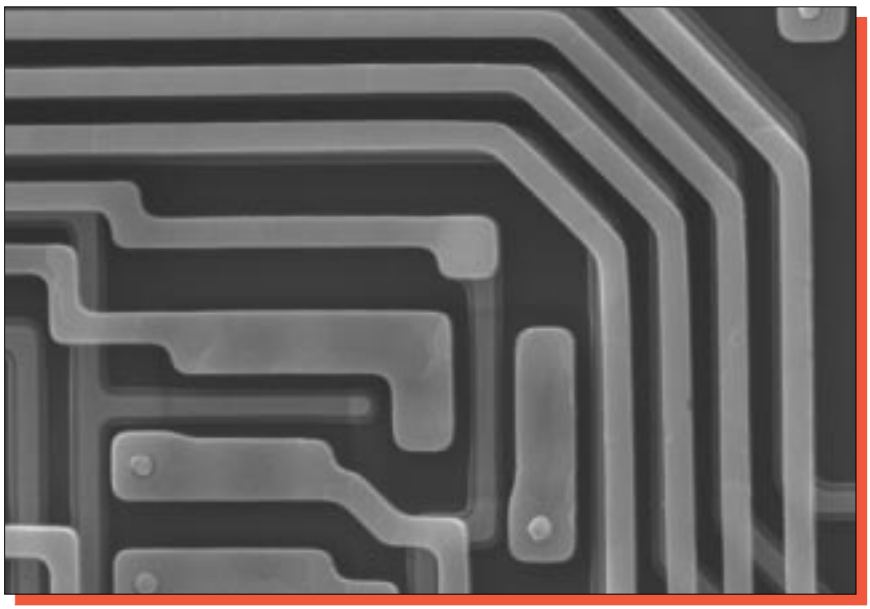
Figure 18. SEM section views of metal 1 line profiles.



Mag. 3200x

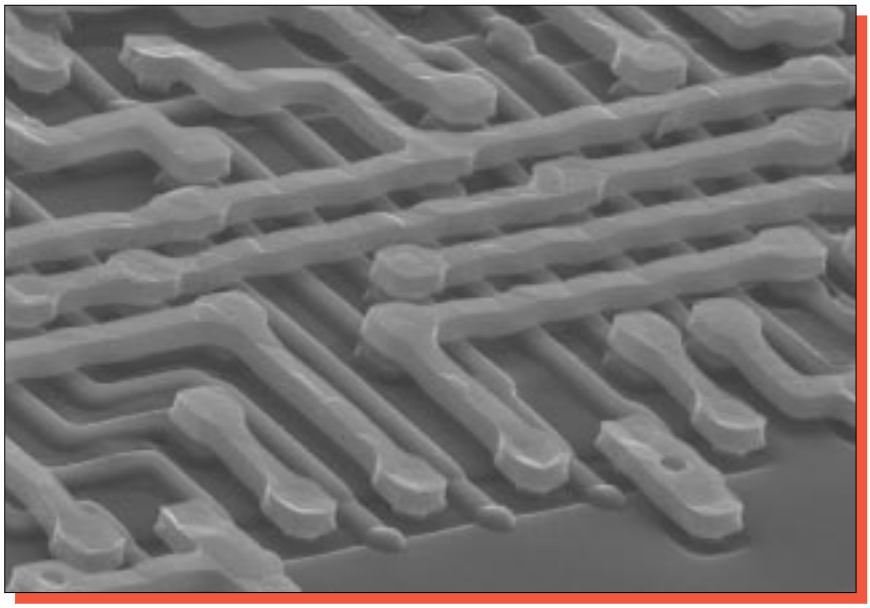


Mag. 3200x

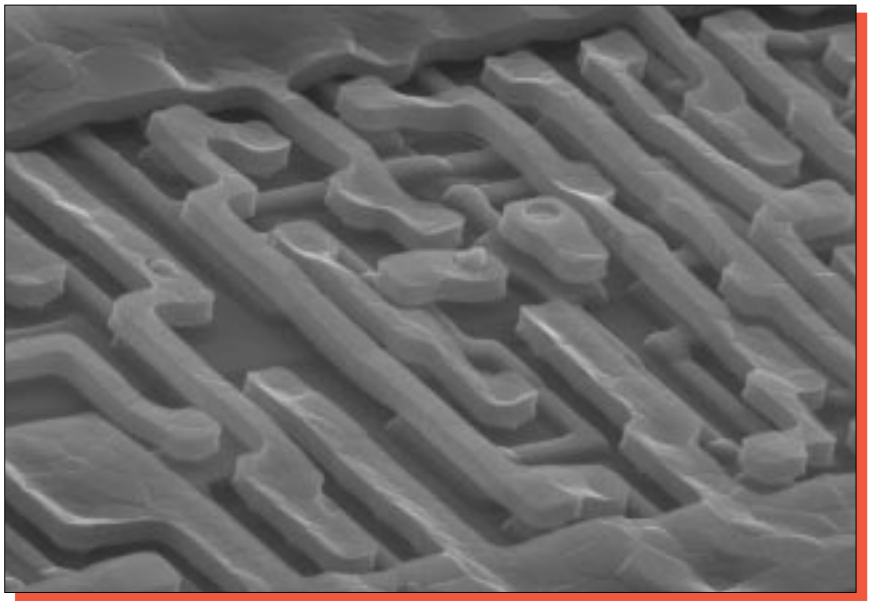


Mag. 5000x

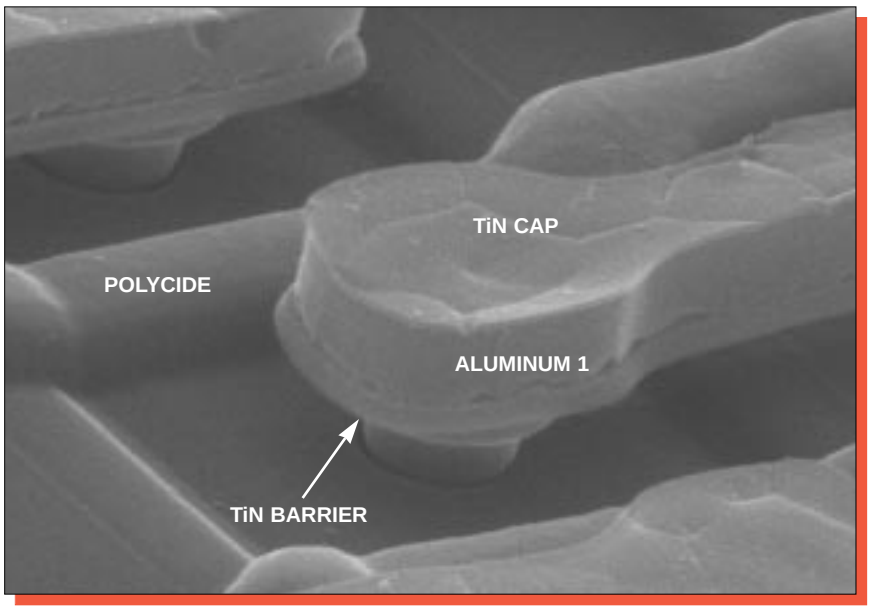
Figure 19. Topological SEM views of metal 1 patterning. 0°.



Mag. 5000x



Mag. 5000x



Mag. 25,000x

Figure 20. Perspective SEM views of metal 1 step coverage. 60°.

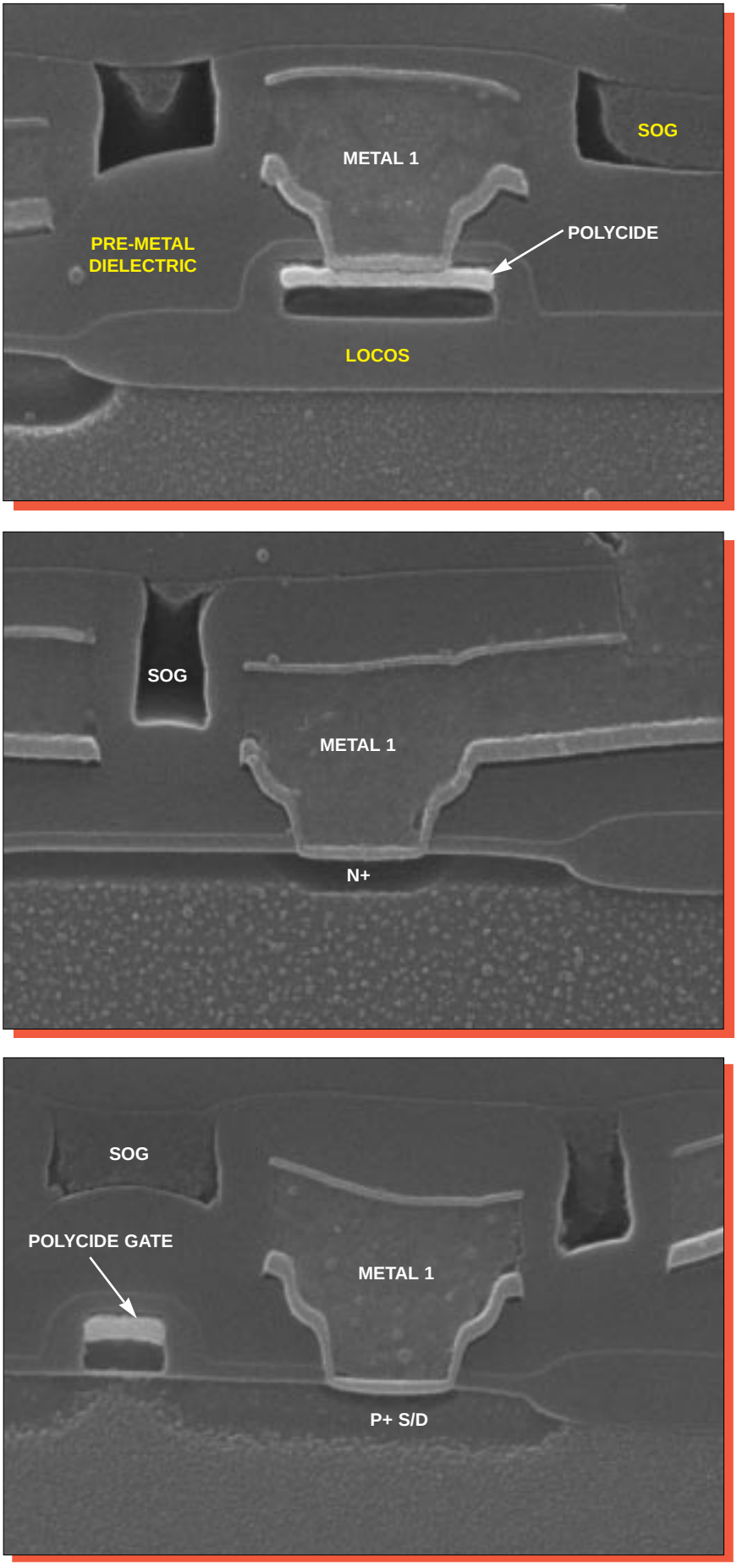


Figure 21. SEM section views of typical metal 1 contacts. Mag. 26,000x.

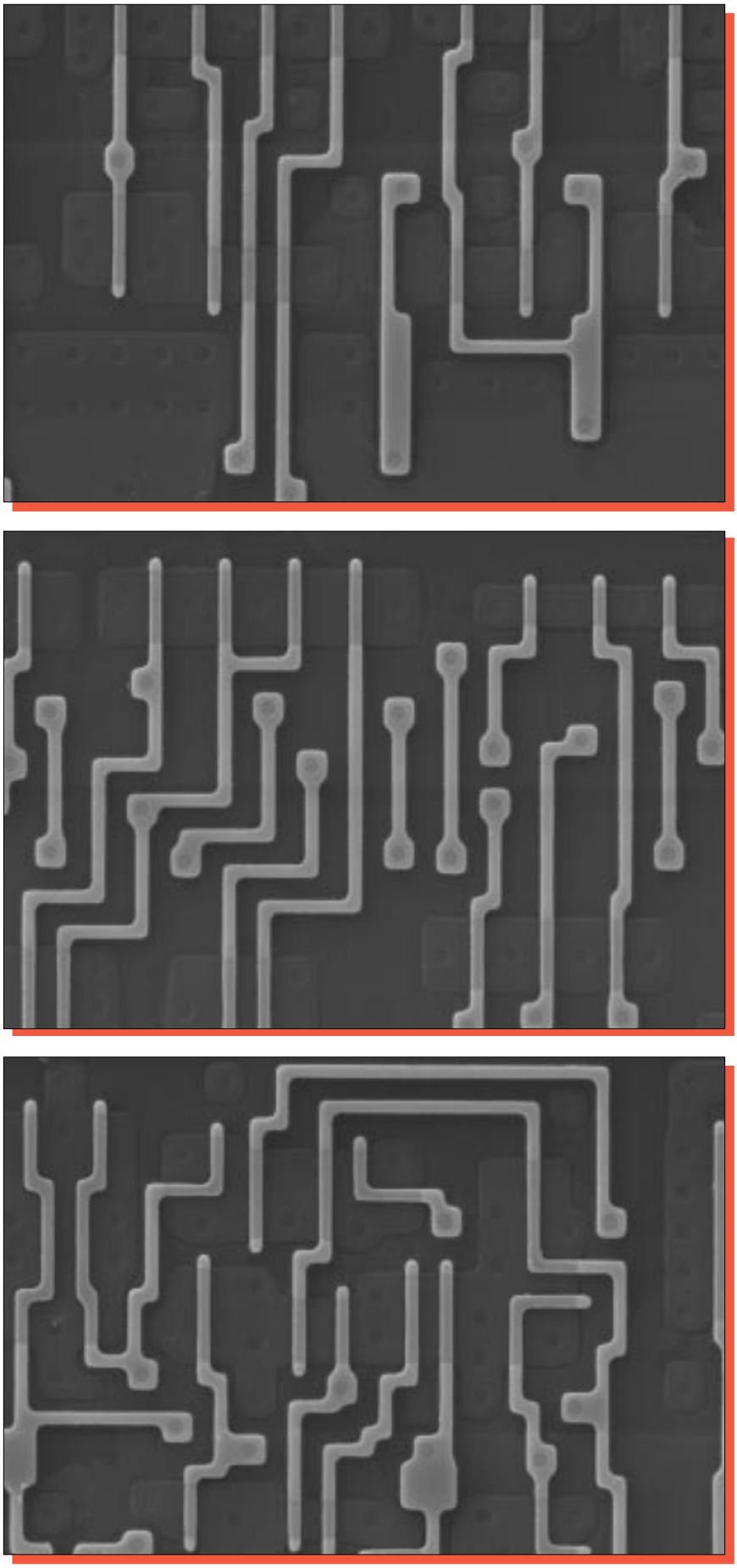
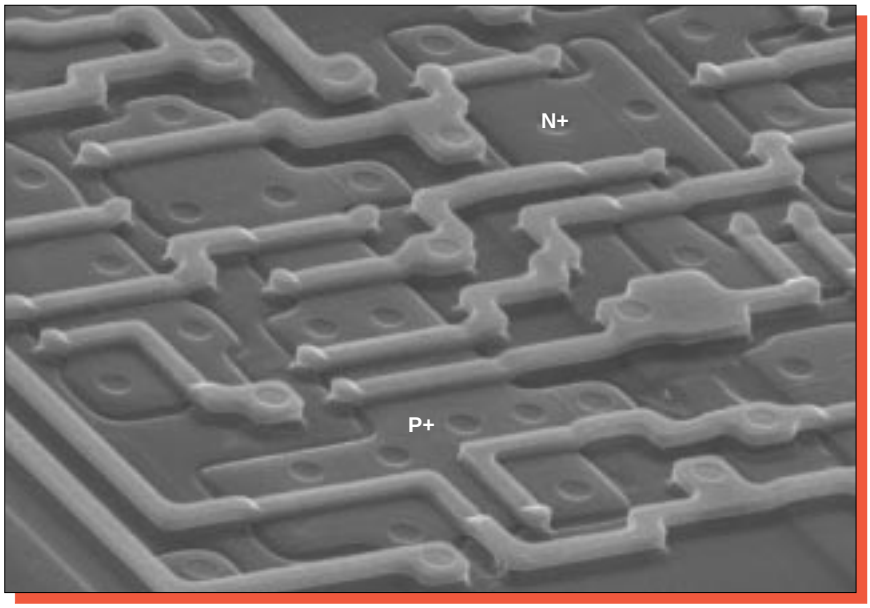
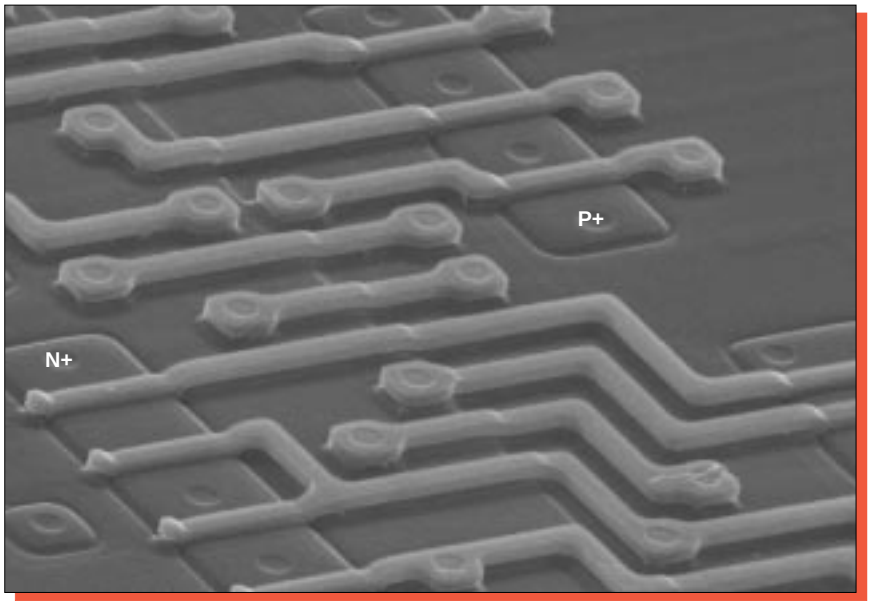


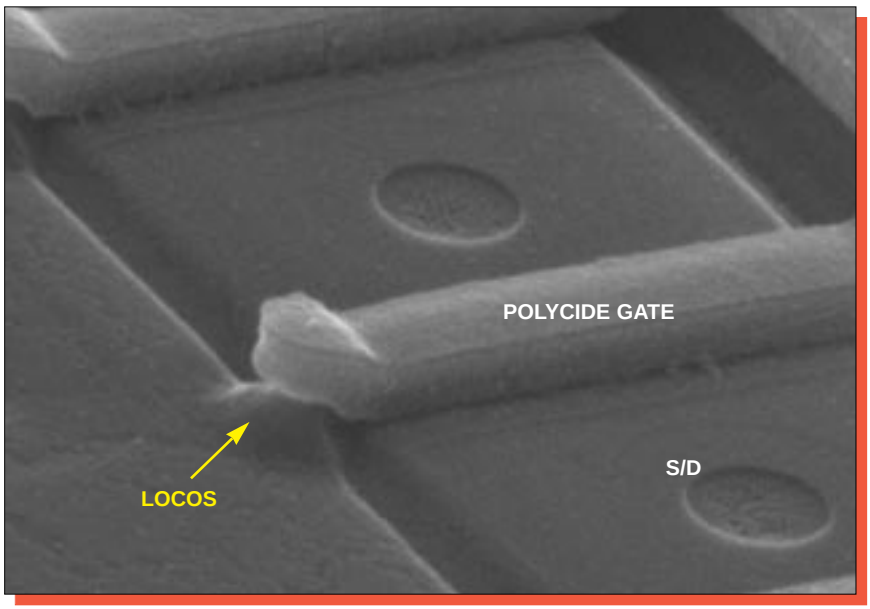
Figure 22. Topological SEM views of polycide patterning. Mag. 3200x, 0°.



Mag. 5700x

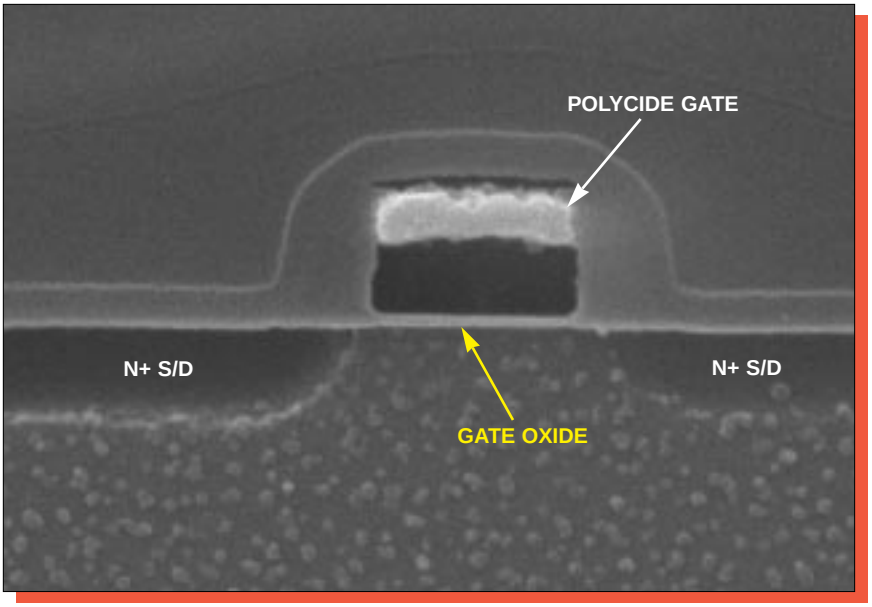


Mag. 5700x

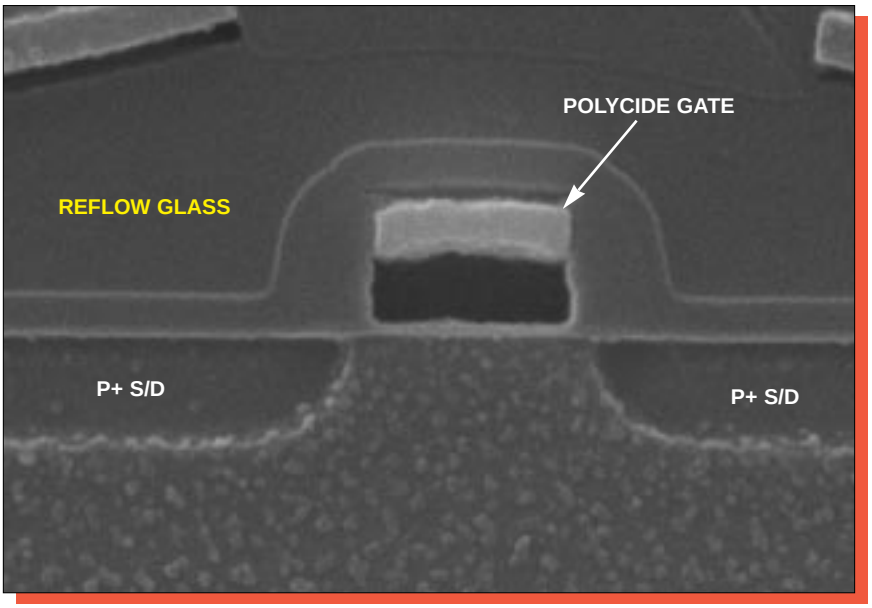


Mag. 26,000x

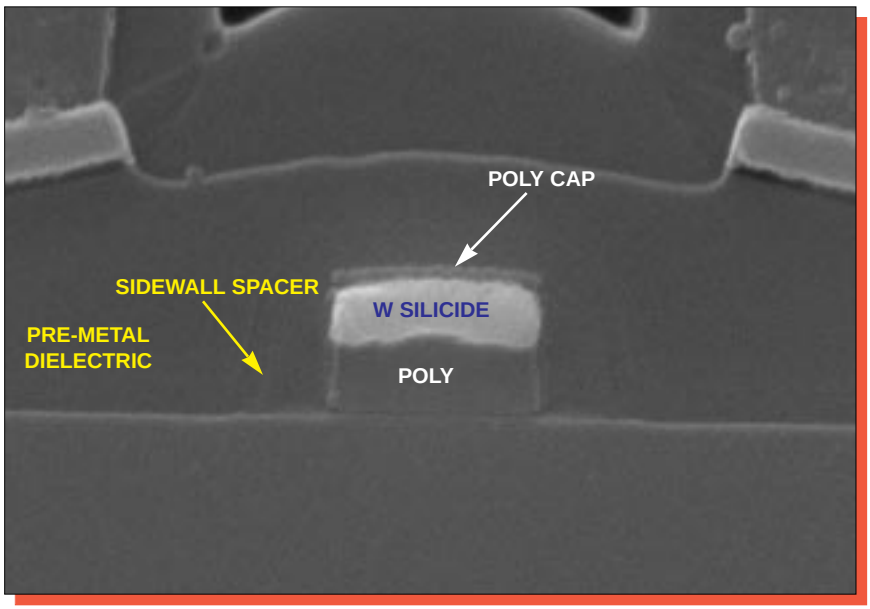
Figure 23. Perspective SEM views of polycide coverage. 60°.



N-channel

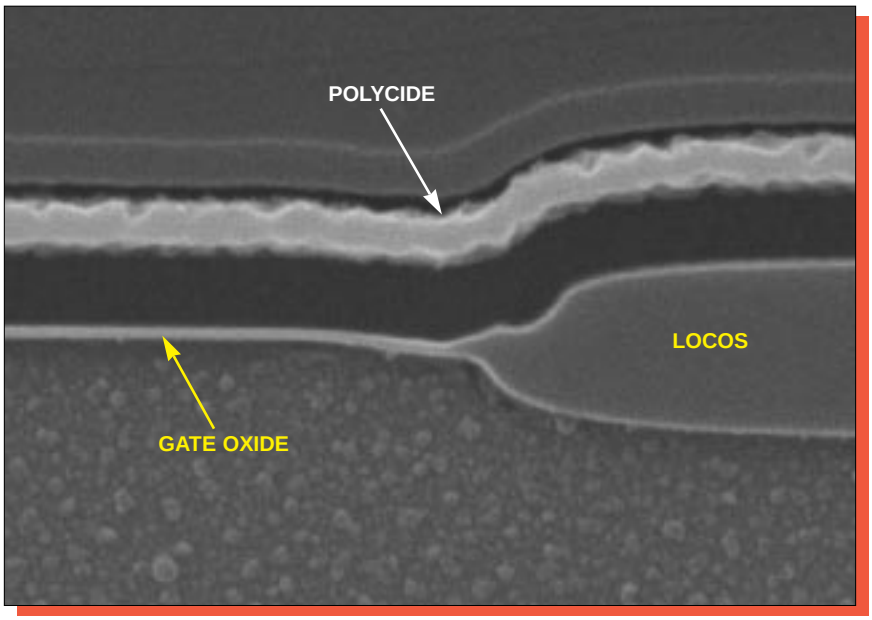


P-channel



glass etch

Figure 24. SEM section views of typical transistors. Mag. 52,000x.



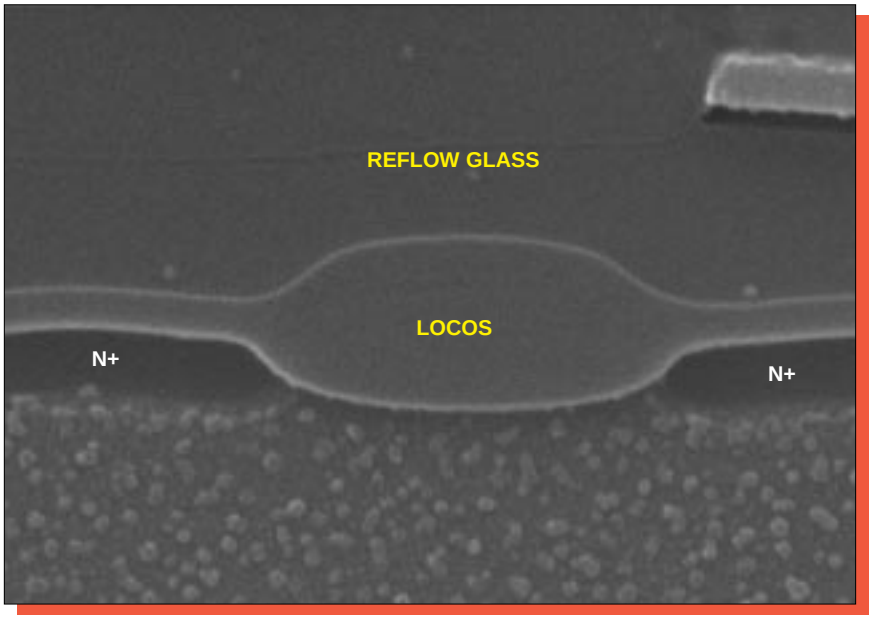
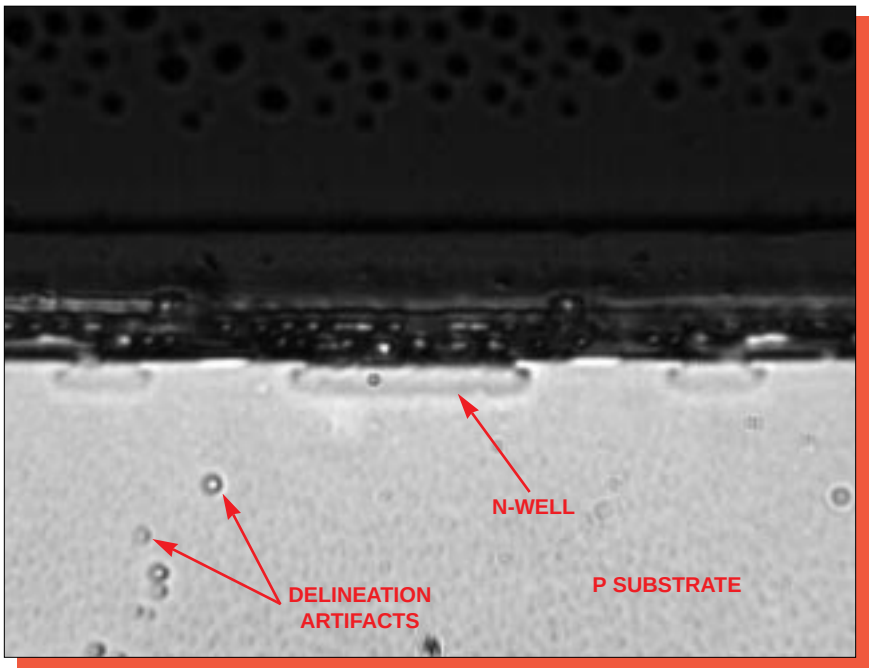
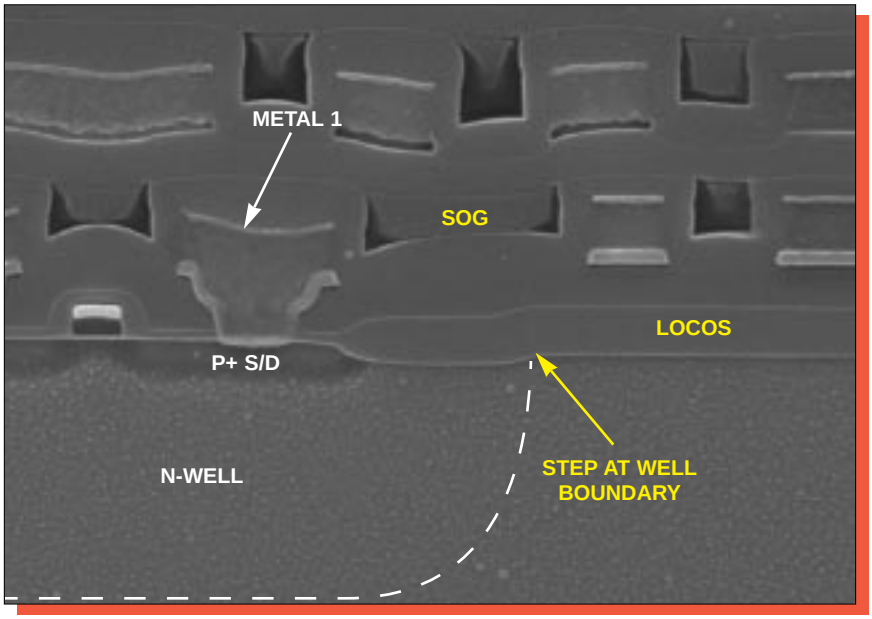


Figure 25. SEM section views illustrating a typical birdsbeak and local oxide isolation. Mag. 52,000x.

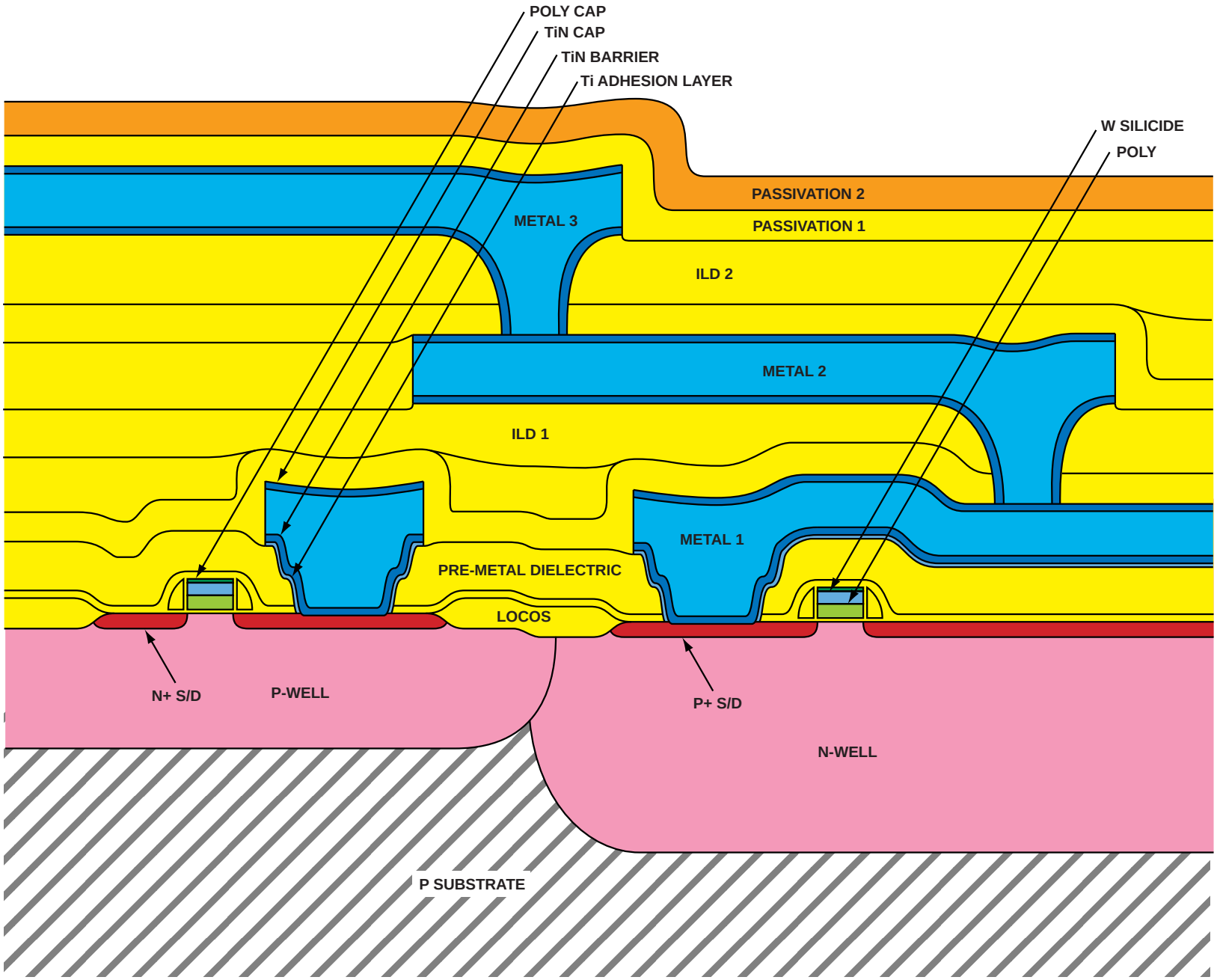


Mag. 1500x



Mag. 13,000x

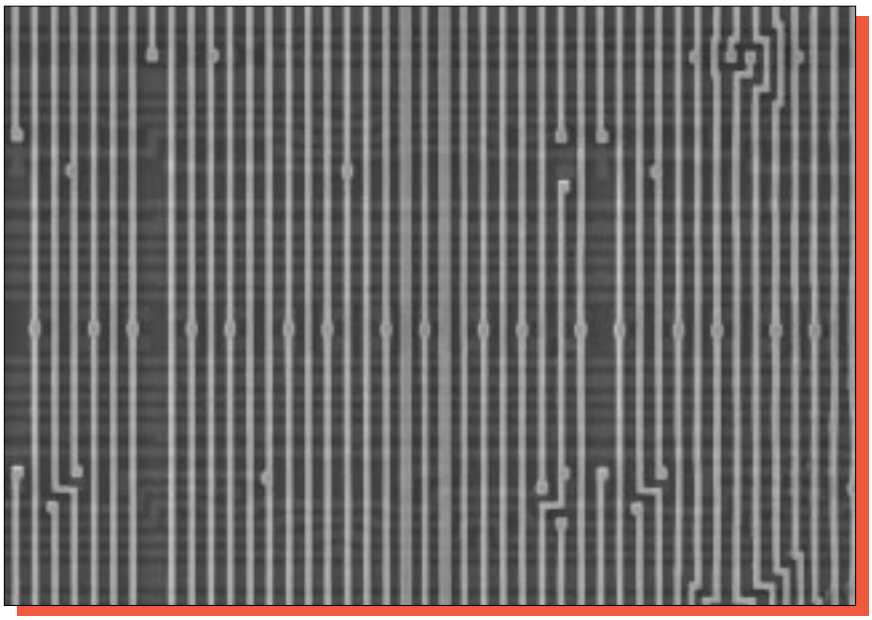
Figure 26. Section views illustrating well structure.



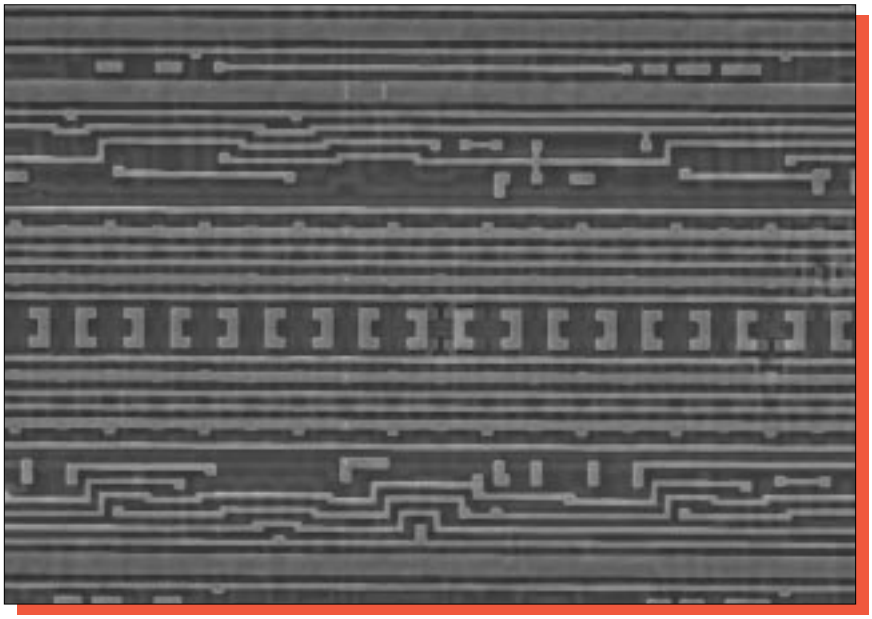
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 27. Color cross section drawing illustrating device structure.

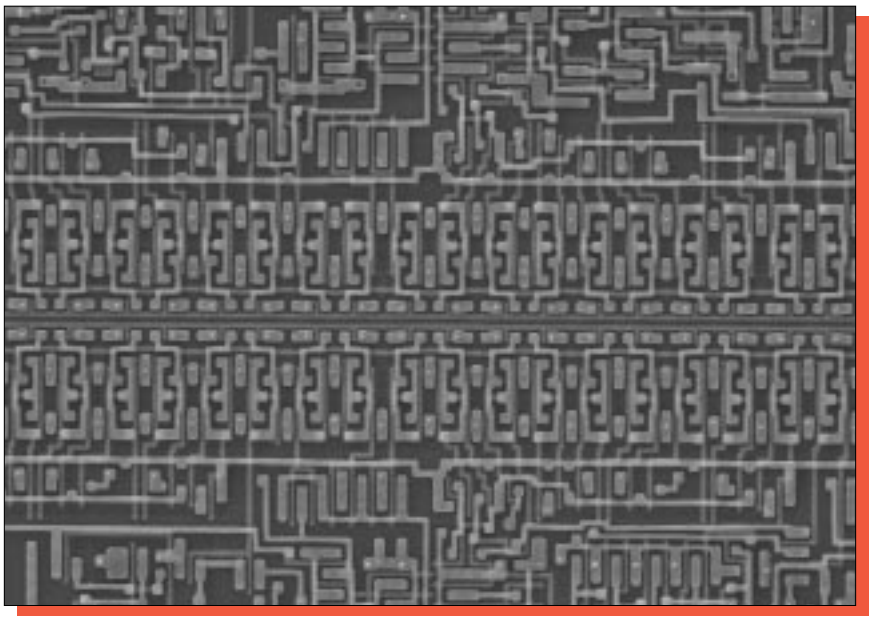


metal 3

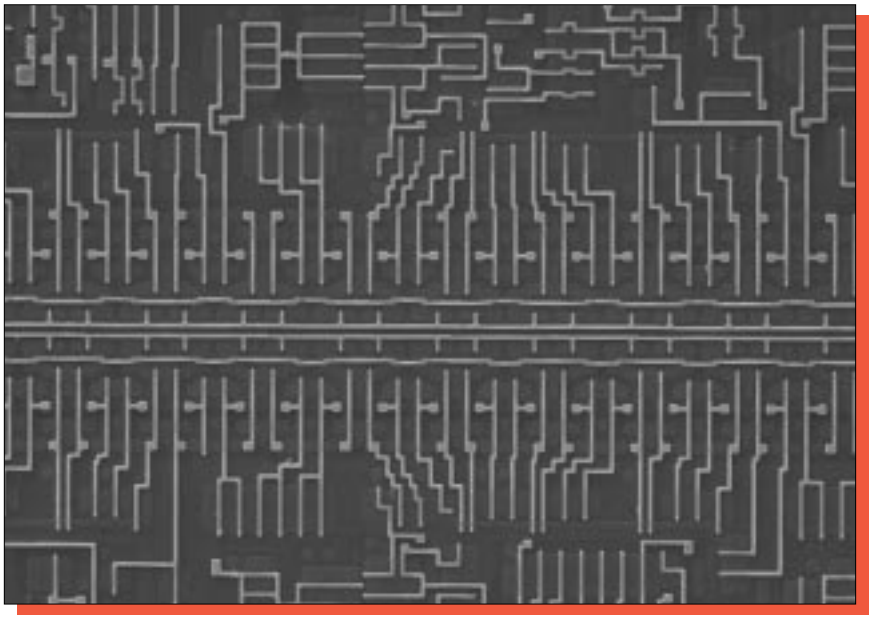


metal 2

Figure 28. Topological SEM views of the FPGA array area. Mag. 810x.

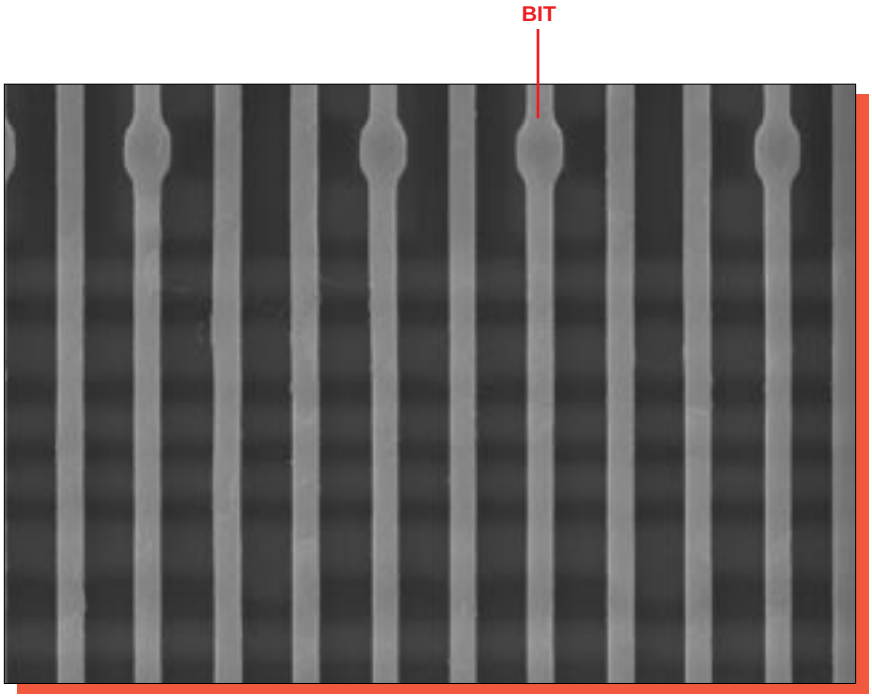


metal 1

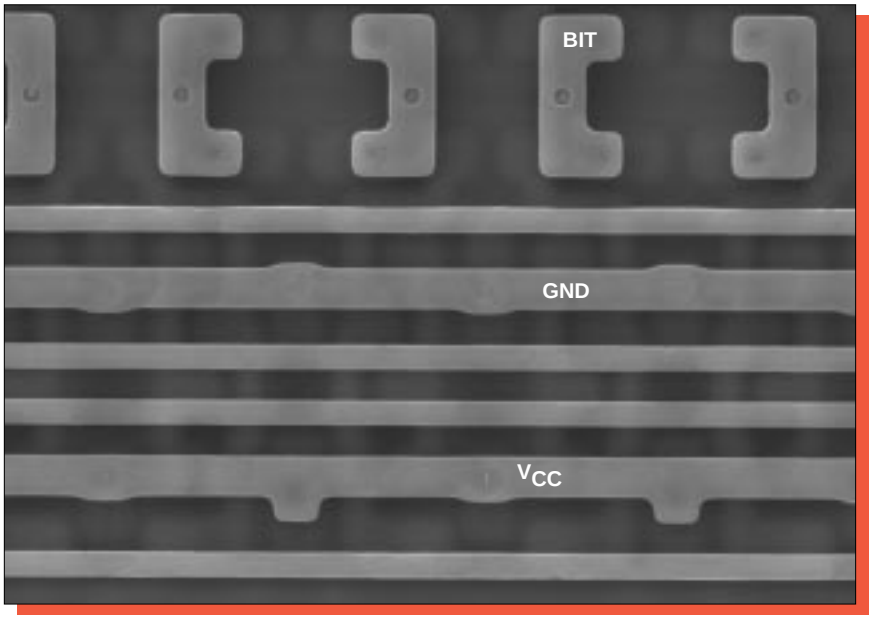


unlayered

Figure 29. Topological SEM views of the FPGA array area. Mag. 810x.

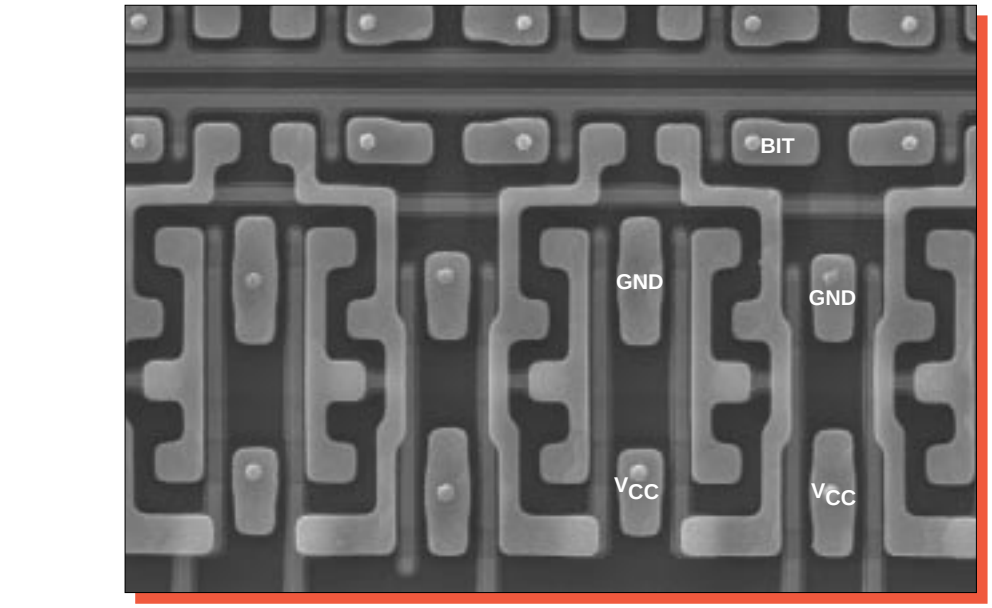


metal 3

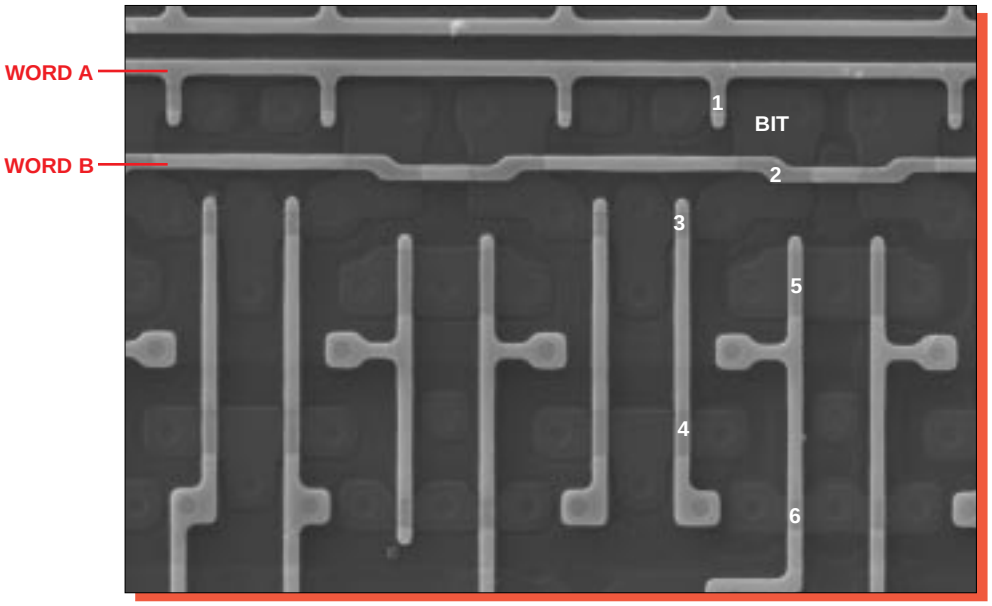


metal 2

Figure 30. Topological SEM views of the FPGA Base 6T-SRAM cell. Mag. 3200x.



metal 1



unlayered

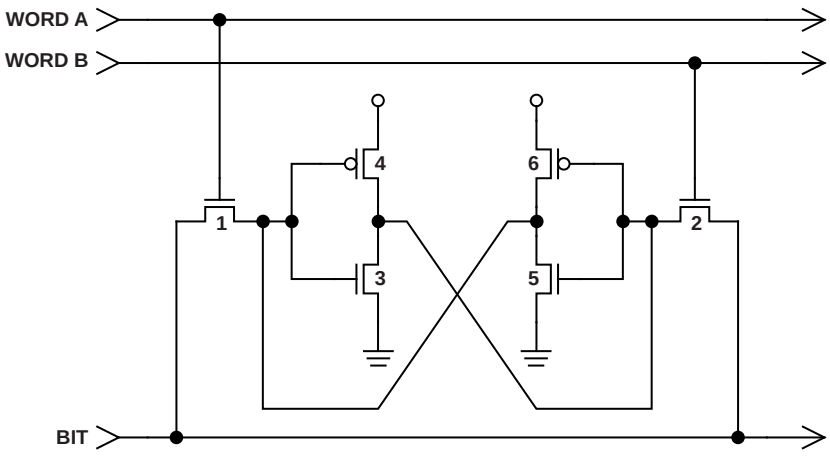
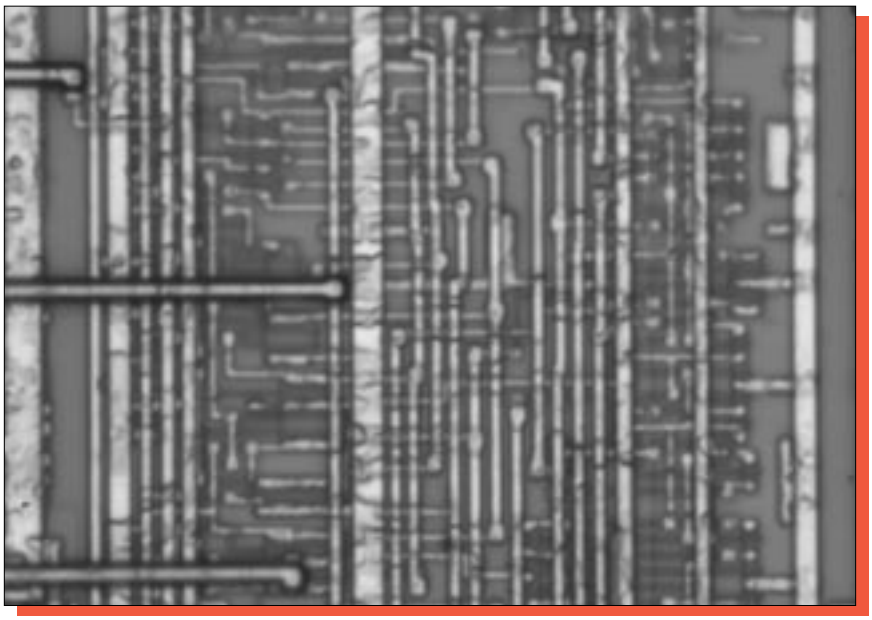
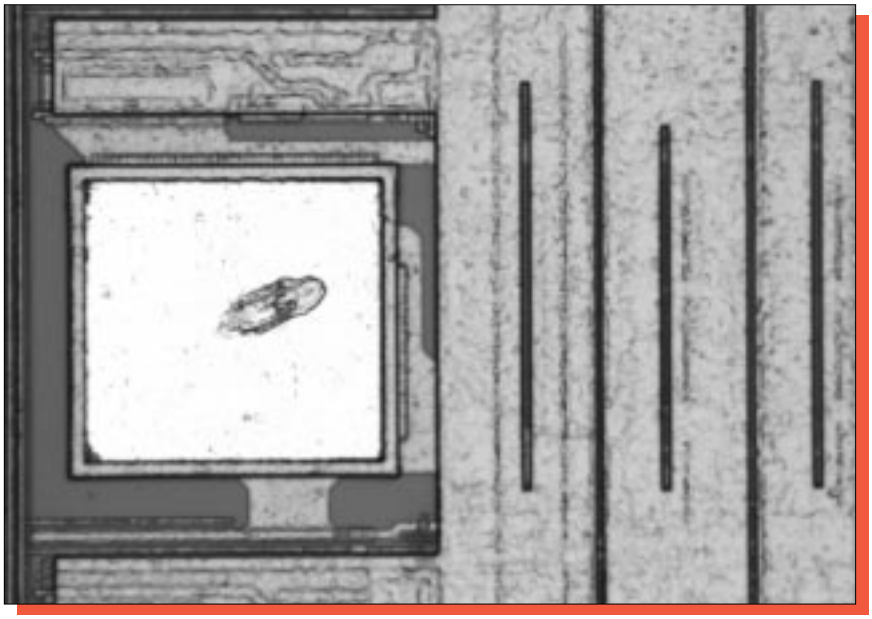


Figure 31. Topological SEM views and schematic of the FPGA Base 6T-SRAM cell. Mag. 3200x.



Mag. 1000x



Mag. 400x

Figure 32. Optical views of typical circuitry and input protection.

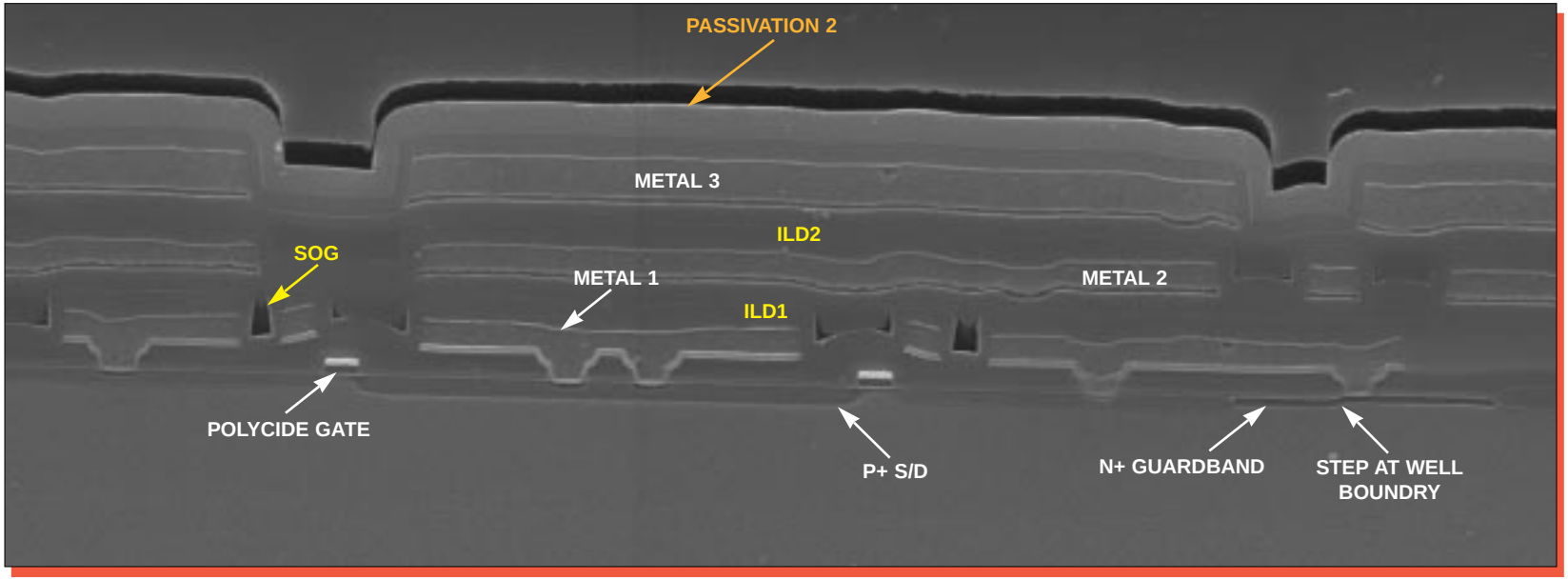


Figure 33. SEM section view of the I/O circuitry. Mag. 6500x.