Construction Analysis

SGS-Thomson M28C64-121
64K EEPROM

Report Number: SCA 9710-559

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the SGS-Thomson M28C64-121 64K EEPROM. Five devices packaged in 28-pin Dual In-Line Packages (DIPs) were received for the analysis. Devices were date coded 9621.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features: None.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 28-pin Dual In-Line Packages (DIPs).
- Lead-locking provisions (holes and anchors) at all pins.
- Wirebonding was by the thermosonic ball bond method using 1.2 mil O.D. gold wire.
- All pins except pin 26 were connected. No multiple bonding wires were noted.
- Die separation was by sawing (full depth).
- Silver-filled epoxy die attach.

Die Process:

- Devices were fabricated using a selective oxidation, N-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of two layers of silicon-dioxide (probably undoped).
- Metallization consisted of a single layer of dry-etched aluminum. The aluminum contained a titanium-nitride cap and barrier. There appeared to be a thin layer of titanium-aluminum (TiAl) precipitate or titanium (Ti) above the barrier (see Figure 11). A thin titanium adhesion layer was used under the barrier. Standard contacts were used (no plugs).

TECHNOLOGY DESCRIPTION (continued)

- Pre-metal dielectric consisted of a layer of CVD glass (probably BPSG) over various densified oxides. The glass appeared to be reflowed following contact cuts.

- A single layer of dry-etched polycide (poly and tungsten silicide) was used. This layer formed all gates on the die, and in the cell array it formed the capacitors, word lines, and tunnel oxide device.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the MOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. No step was present at the edge of the well boundaries.

- The memory cell consisted of a standard EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, capacitors, and the tunnel oxide devices.

- Redundancy fuses were not present.

ANALYSIS RESULTS I

Package and Assembly: **Figures 1 - 5**

Questionable Items:[1] None.

Special Features: None.

General Items:

- Devices were packaged in 28-pin Dual In-Line Packages (DIPs).
- Overall package quality: Good. No defects were noted externally or internally on the package. All pins were well formed.
- Lead-locking provisions (anchors and holes) were present.
- Wirebonding was by the thermosonic ball bond method using 1.2 mil O.D. gold wire. The clearance of the wires was normal. Bond pull strengths were normal (see page 9). No problems were noted.
- Die attach: A silver-epoxy was used to attach the die to the header. No significant voids were noted.
- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process: **Figures 6 - 26**

Questionable Items:[1] None.

Special Features: None.

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, N-well CMOS process in a P substrate. No epi was used.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.

- Die coat: No die coat was present.

- Overlay passivation: The passivation consisted of two layers of silicon-dioxide (probably undoped). Overlay integrity test indicated defect-free passivation. Edge seal was good.

- Metallization: A single layer of metal consisting of aluminum with a titanium-nitride cap and barrier. There appeared to be a thin layer of titanium-aluminum (TiAl) precipitate or titanium (Ti) above the barrier. A thin titanium adhesion layer was used under the barrier. Standard contacts were used (no plugs). No problems were noted.

- Metal patterning: The metal layer was patterned by a dry etch of normal quality. Contacts were completely surrounded by metal and metal lines were widened at contacts.

- Metal defects: No voiding, notching, or neckdown was noted in the metal layer.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal step coverage: Aluminum thinned up to 60 percent at contact edges. Total metal thinning was reduced to 40 percent with the addition of the cap and barrier. MIL-STD allows up to 70 percent metal thinning for contacts of this size.

- Pre-metal dielectric: A layer of CVD glass (probably BPSG) over various densified oxides was used under the metal. Reflow appeared to be performed following contact cuts. No problems were found.

- Contact defects: None. Contact cuts were well rounded. No over-etching of the contacts was noted.

- Polysilicon: A single layer of polycide (poly and tungsten silicide) was used to form all the gates on the die and in the cell. The poly formed the word/select lines, capacitors, and the tunnel oxide device.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the MOS transistors. An LDD process was used with oxide sidewall spacers left in place. Diffusions were not silicided. No problems were noted.

- Isolation: Local oxide (LOCOS) isolation was used. No step was present in the oxide at the well boundary.

- EEPROM array: Memory cell consisted of a standard EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, capacitors, and the tunnel oxide device. Cell pitch was 7.8 x 15.0 microns.

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM of passivation

Passivation integrity test

Wirepull test

Passivation removal

SEM inspection of metal

Metal removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis (EDX)

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal/Good

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (TOP)

(LOGO) M28C64-121
4H8AA627F
KOREA

BOTTOM

XOP641FA
M6119621

WIREBOND STRENGTH

Wire material: 1.2 mil O.D. gold
Die pad material: Aluminum

Sample #	**1**
# of wires pulled:	9
Bond lifts:	0
Force to break - high:	15g
- low	14g
- avg.	14.5g
- std. dev.:	0.5

DIE MATERIAL ANALYSIS (EDX)

Overlay passivation:	A layer of nitride over a layer of silicon-dioxide.
Metallization:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier. There appeared to be a layer of titanium-aluminum (TiAl) precipitate or titanium (Ti) above the barrier. A thin layer of titanium (Ti) was used under the barrier.
Poly:	Tungsten (W) silicide.

HORIZONTAL DIMENSIONS

Die size:	3.2 x 6.7 mm (125 x 265 mils)
Die area:	21.5 mm^2 (33,125 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.09 x 0.09 mm (3.8 x 3.8 mils)
Min pad space:	3.0 mils
Min metal width:	1.0 micron
Min metal space:	1.4 micron
Min metal pitch:	2.4 microns
Min contact:	0.8 micron
Min polycide width:	1.2 micron
Min polycide space:	1.1 micron
Min gate length - (N-channel):*	1.2 micron
- (P-channel):	1.3 micron
Cell pitch:	7.8 x 15.0 microns
Cell size:	117.0 microns

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (20 mils)

Layers:

Passivation 2:	0.65 micron
Passivation 1:	0.35 micron
Metal - cap:	0.07 micron (approximate)
- aluminum:	0.65 micron
- barrier:	0.15 micron
Pre-metal dielectric:	0.65 micron (average)
Oxide on poly:	0.15 micron
Poly - silicide:	0.15 micron
- poly:	0.15 micron
Local oxide:	0.55 micron
N+ S/D:	0.25 micron
P + S/D:	0.4 micron
N-well:	4.0 microns (approximate)

**Physical gate length*

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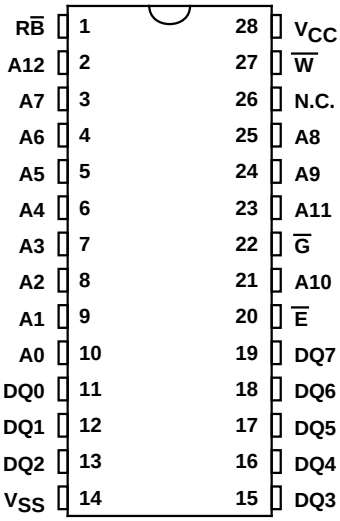
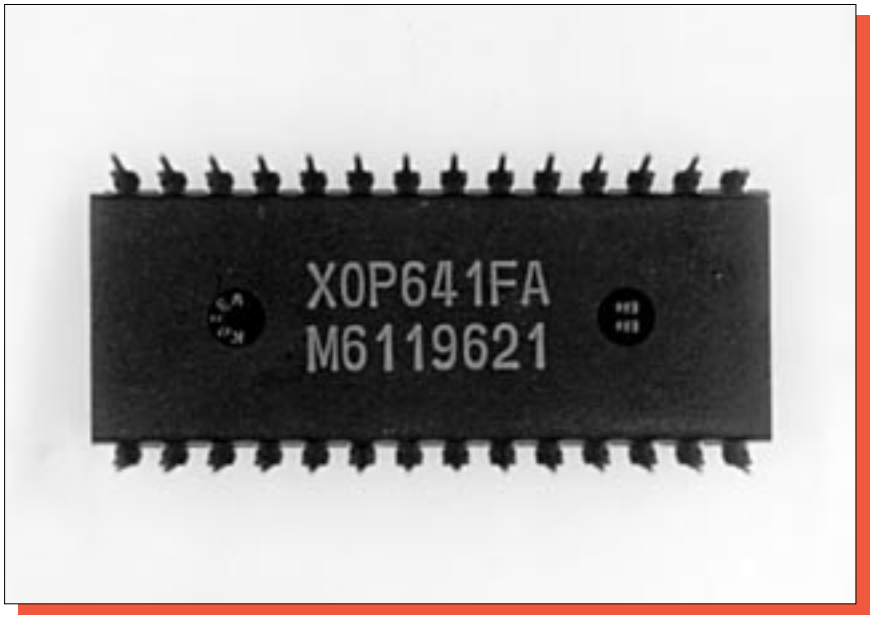
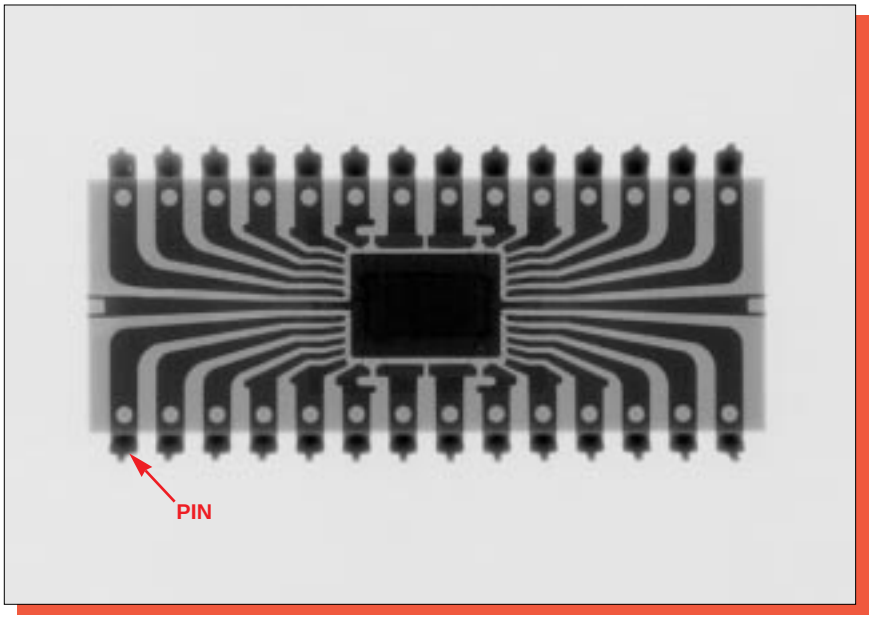




bottom

Figure 1. Package photographs and pinout of the SGS-Thomson M28C64-121 EEPROM. Mag. 2.5x.



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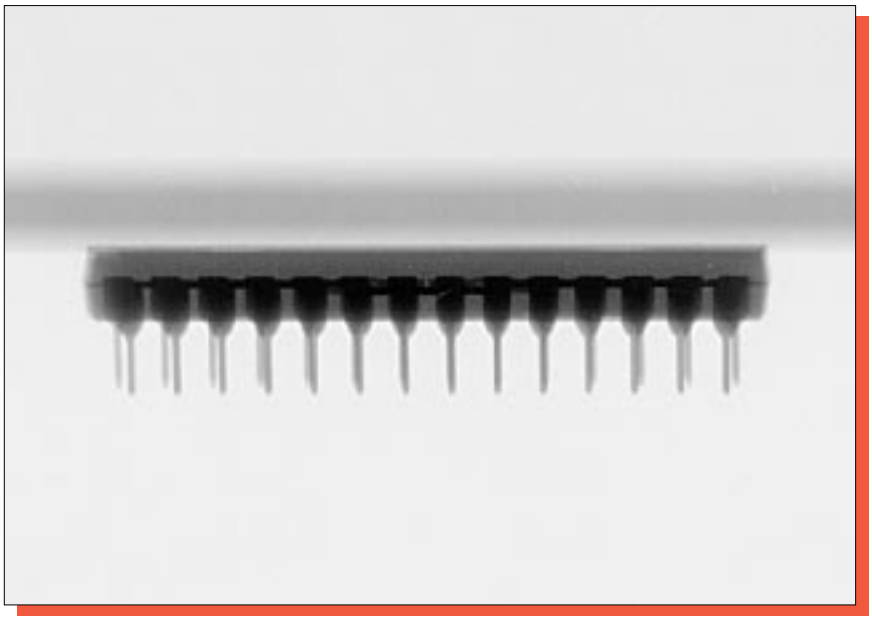
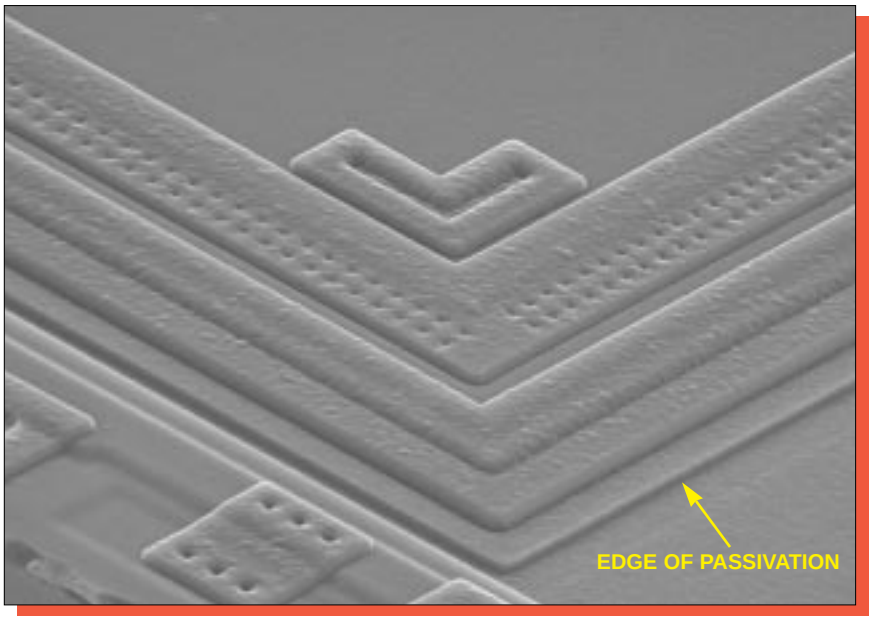


side

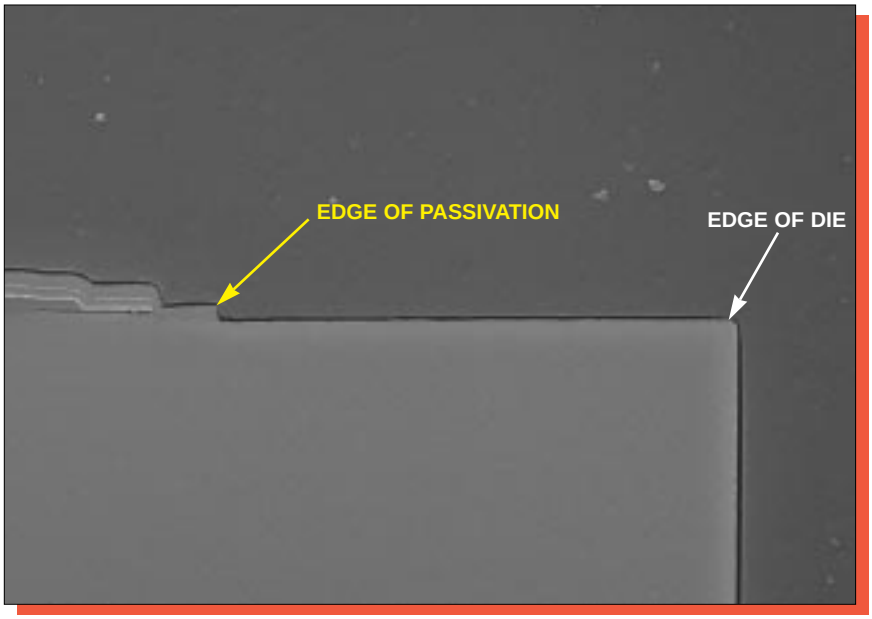
Figure 2. X-ray views of the package. Mag. 2.5x.

Mag. 250x

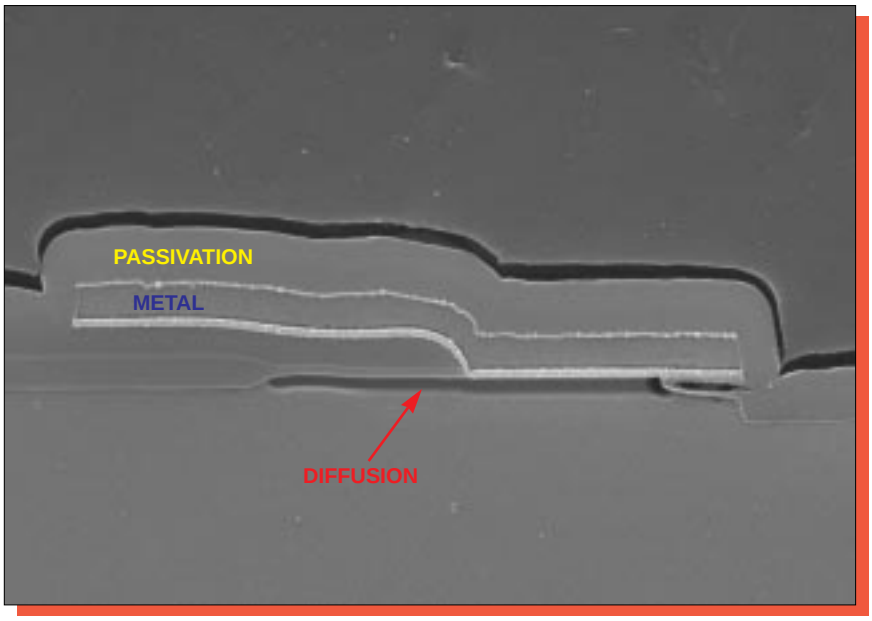


Mag. 1300x

Figure 3. Perspective SEM views of dicing and edge seal. 60°.

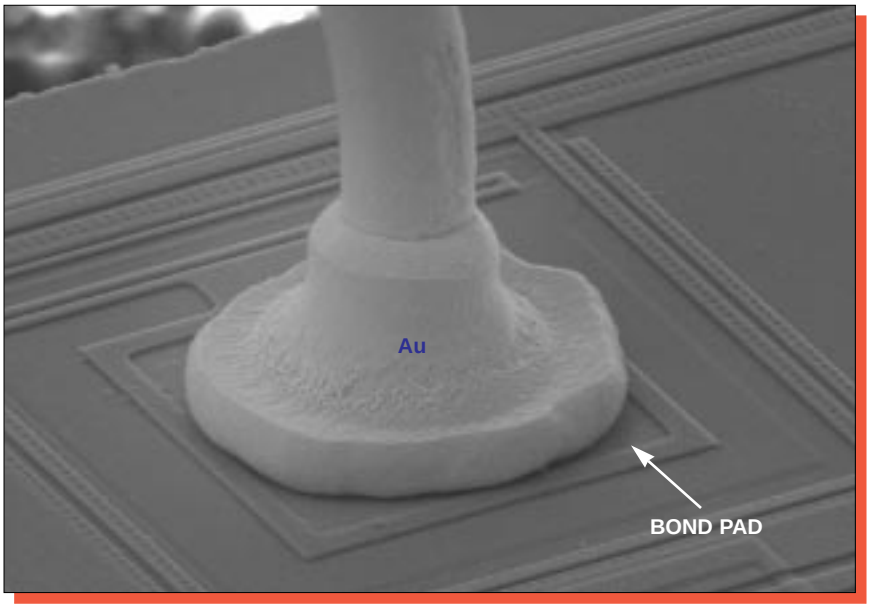


Mag. 1600x

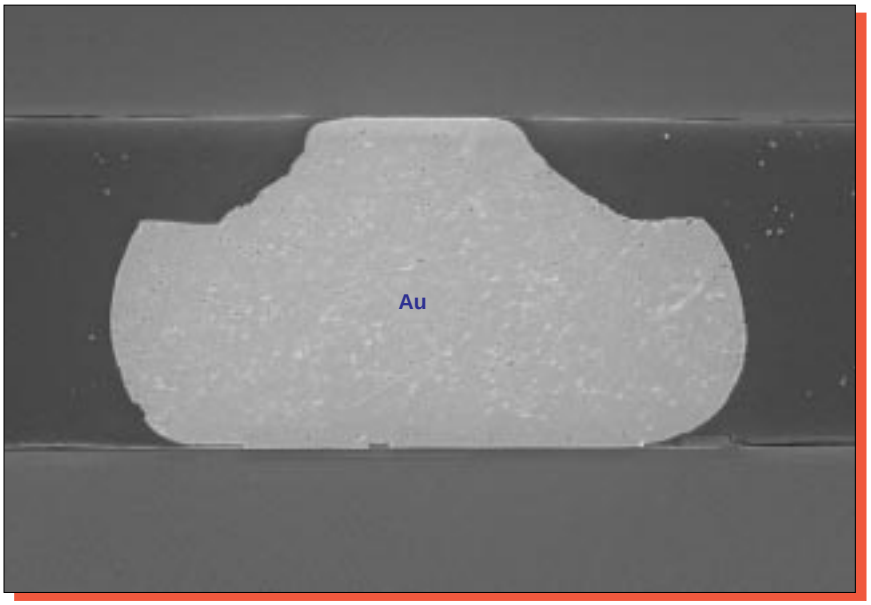


Mag. 6500x

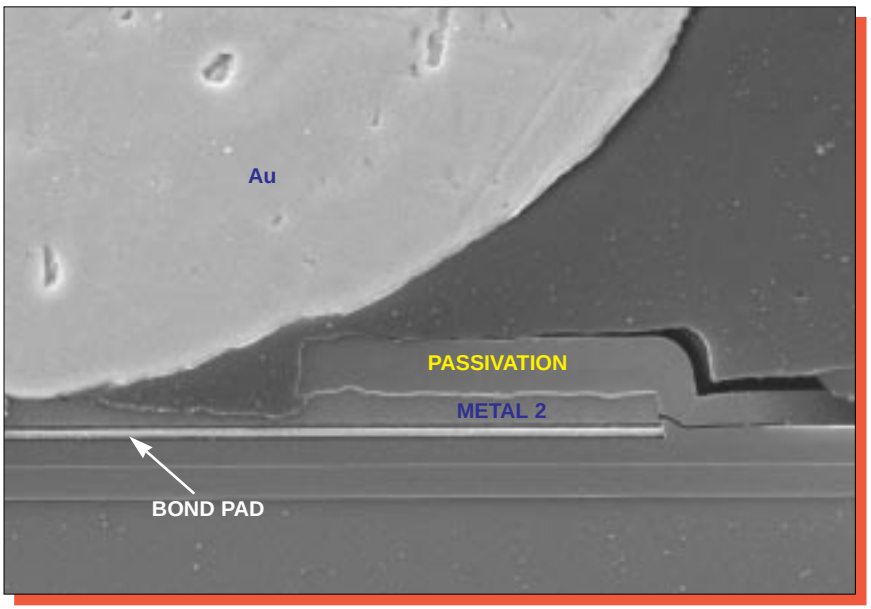
Figure 4. SEM section views of the edge seal.



Mag. 550x, 60°



Mag. 810x



Mag. 6500x

Figure 5. SEM views of typical ball bonds.

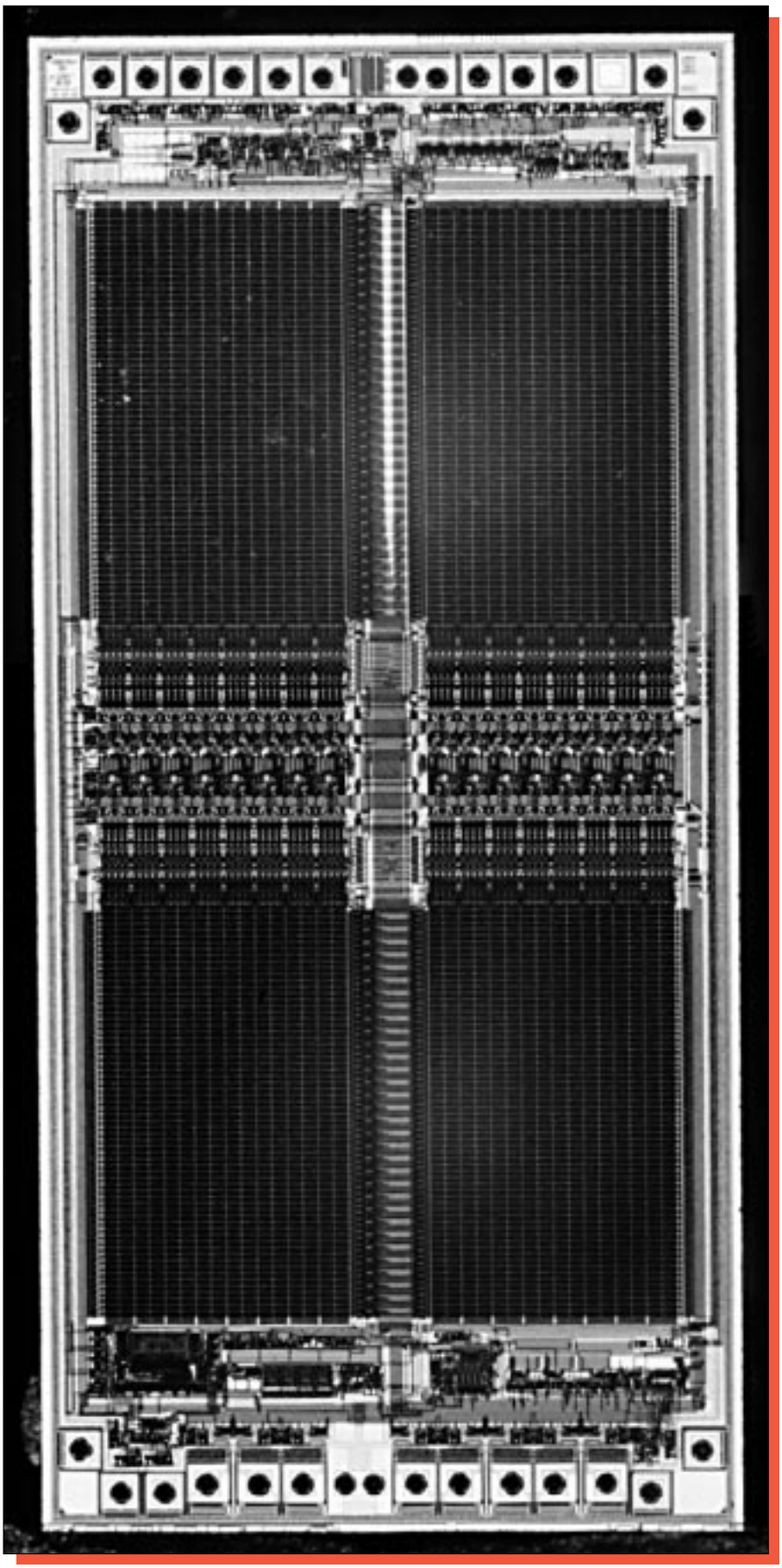
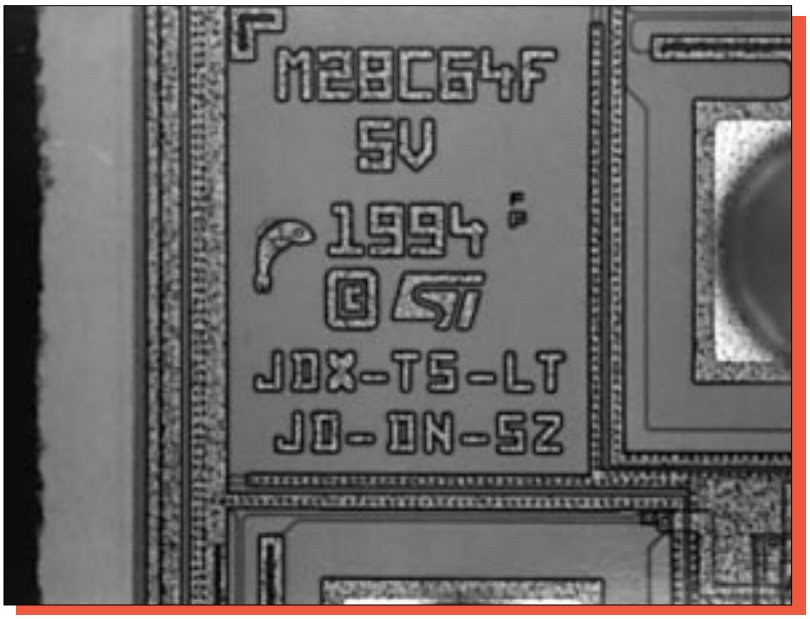
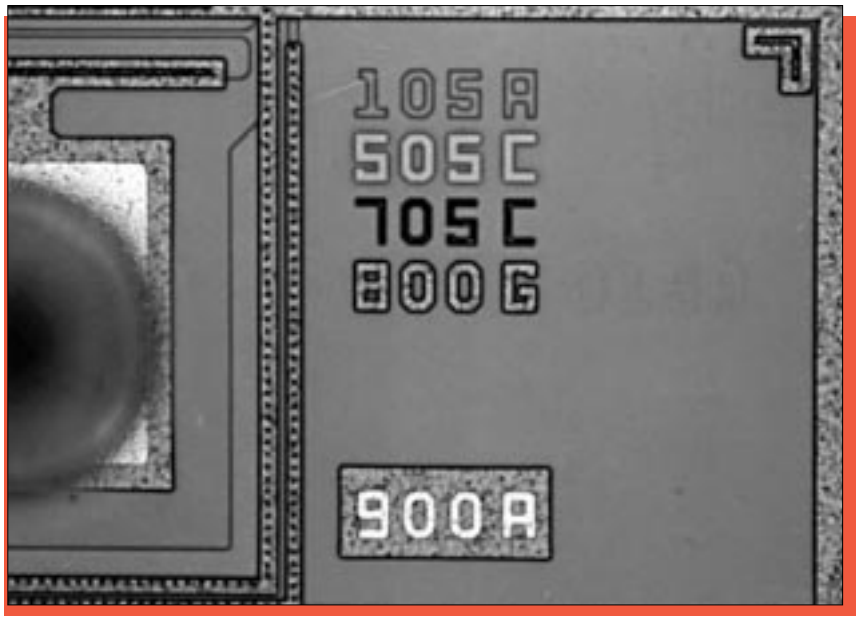


Figure 6. Whole die photograph of the M28C64-121 EEPROM. Mag. 34x.



Mag. 320x



Mag. 400x

Figure 7. Optical views of markings on the die surface.

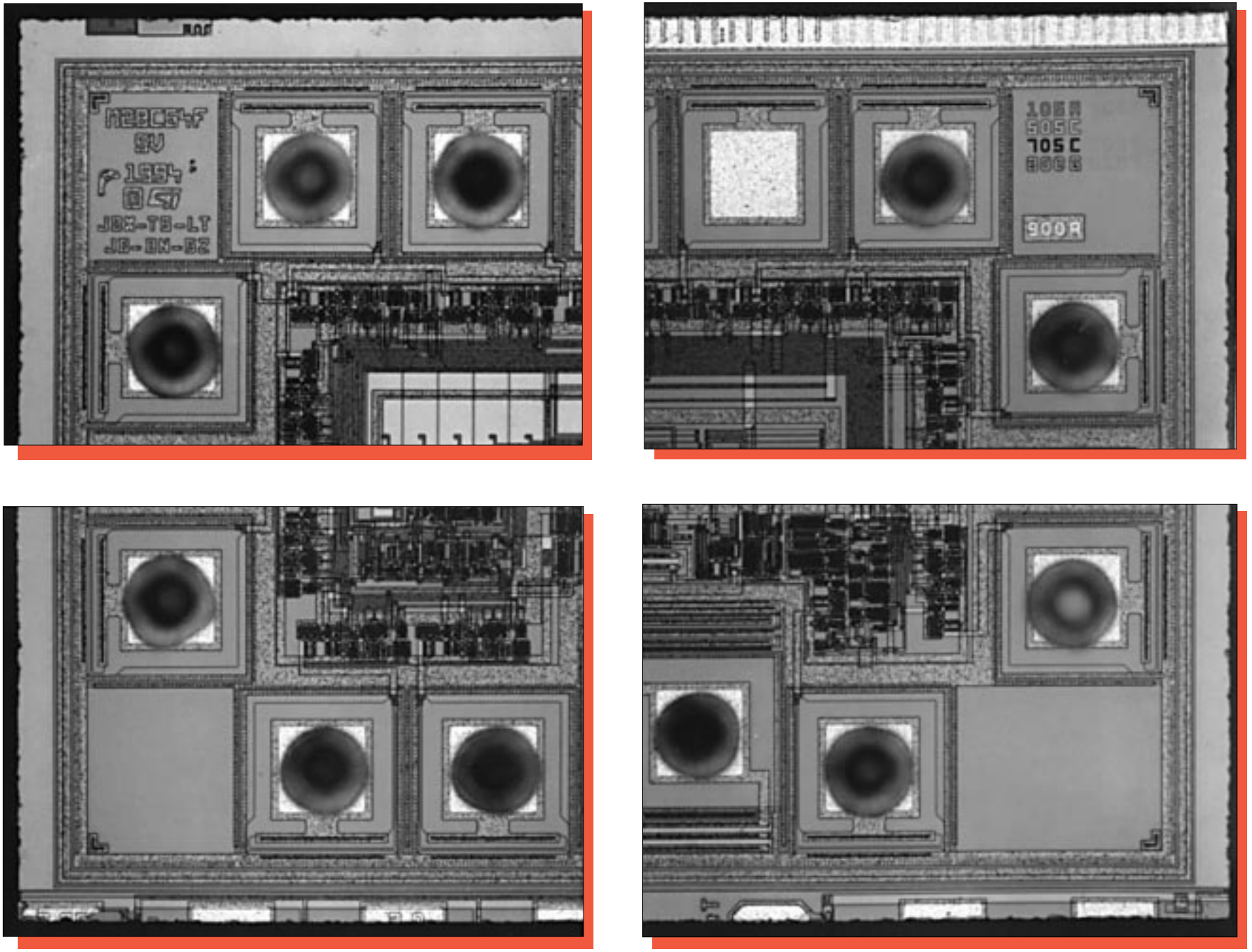
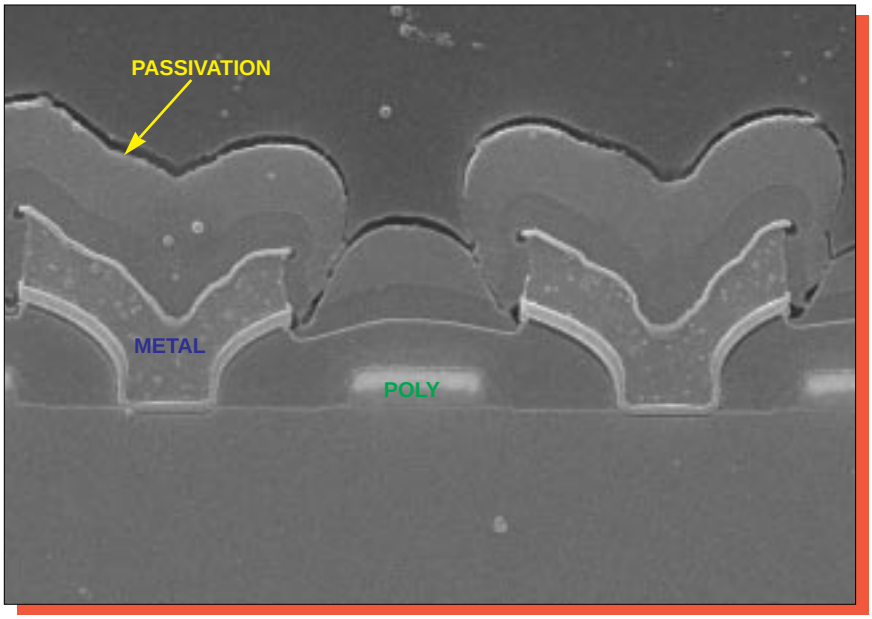
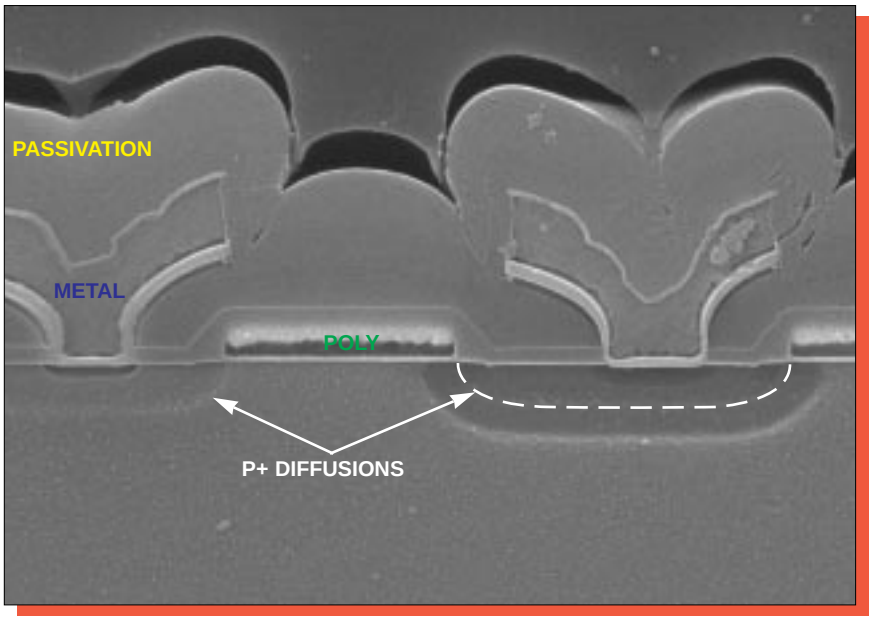


Figure 8. Optical views of the die corners. Mag. 160x.

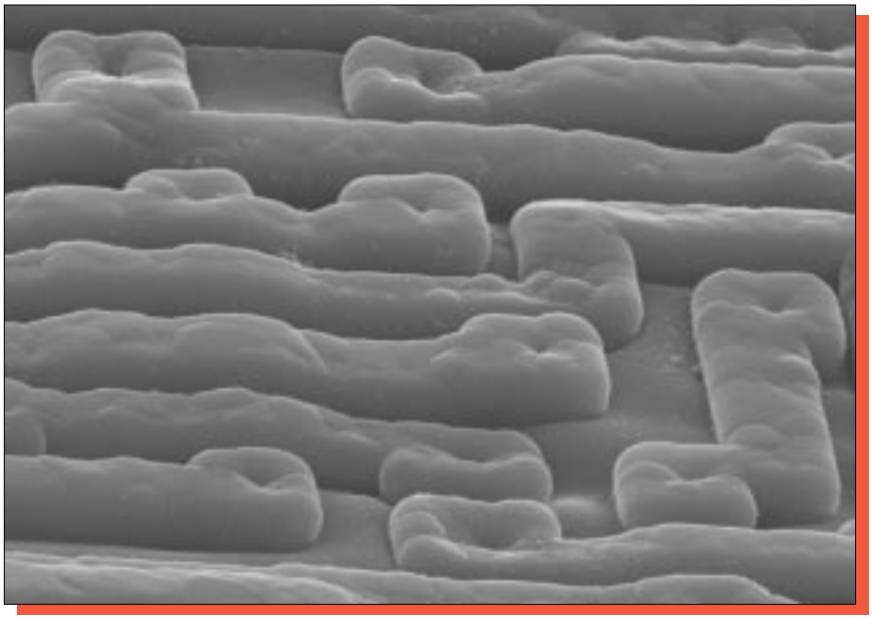


glass-etch

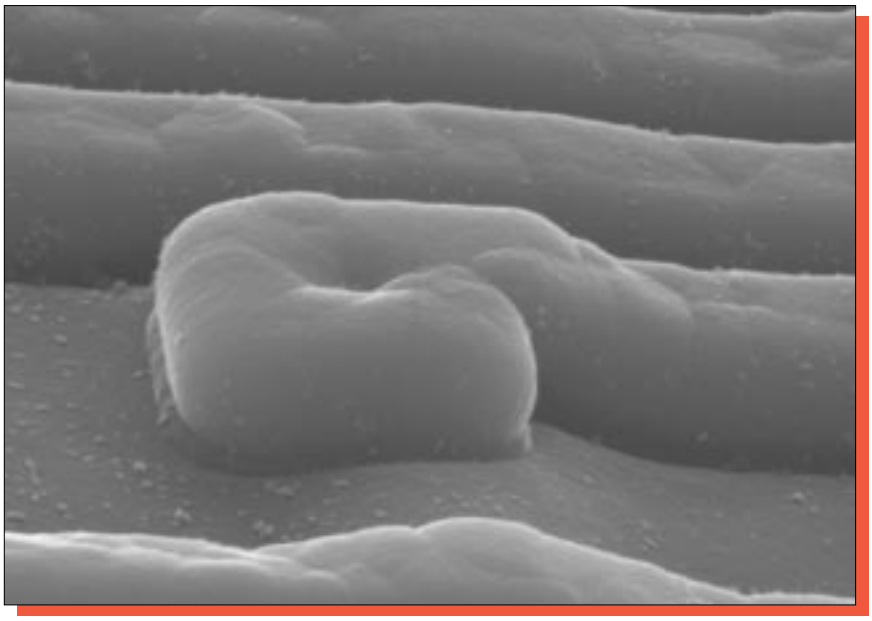


silicon-etch

Figure 9. SEM section views of general circuitry. Mag. 13,000x.

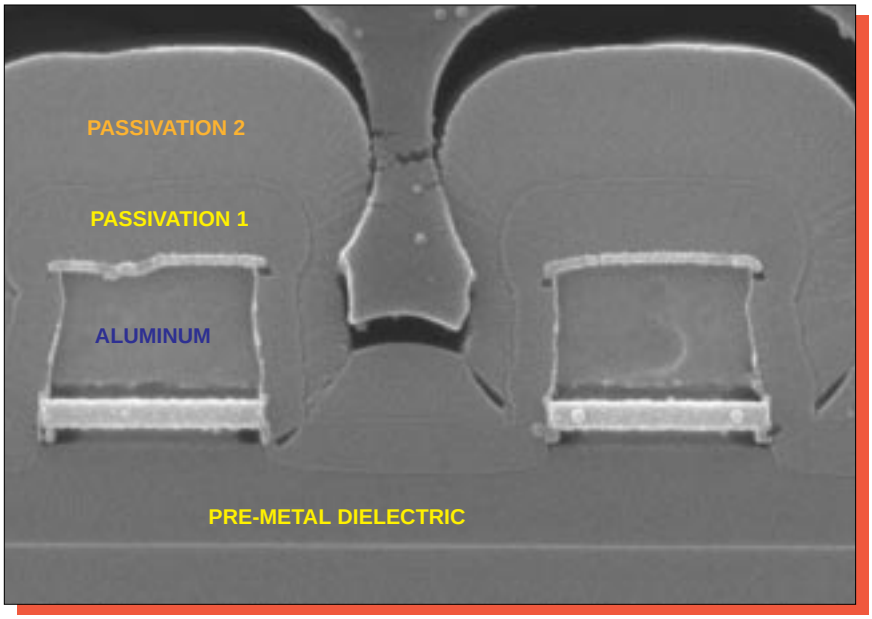


Mag. 5000x

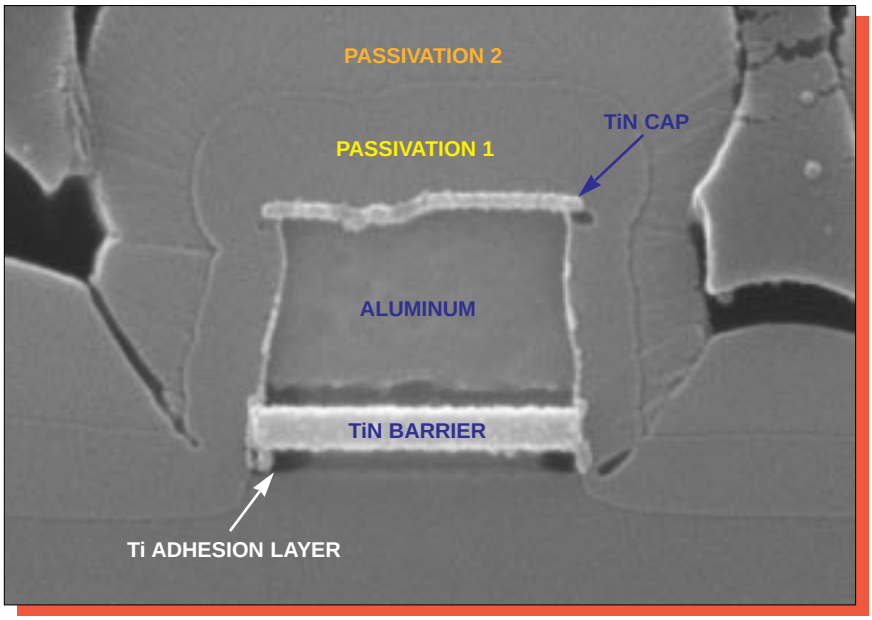


Mag. 12,500x

Figure 10. Perspective SEM views illustrating overlay passivation coverage. 60°.

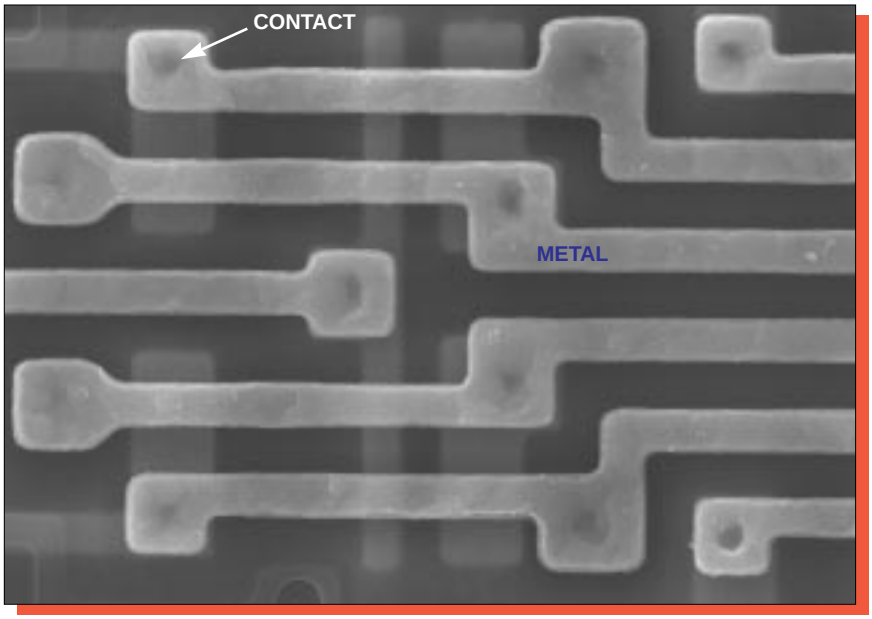


Mag. 26,000x

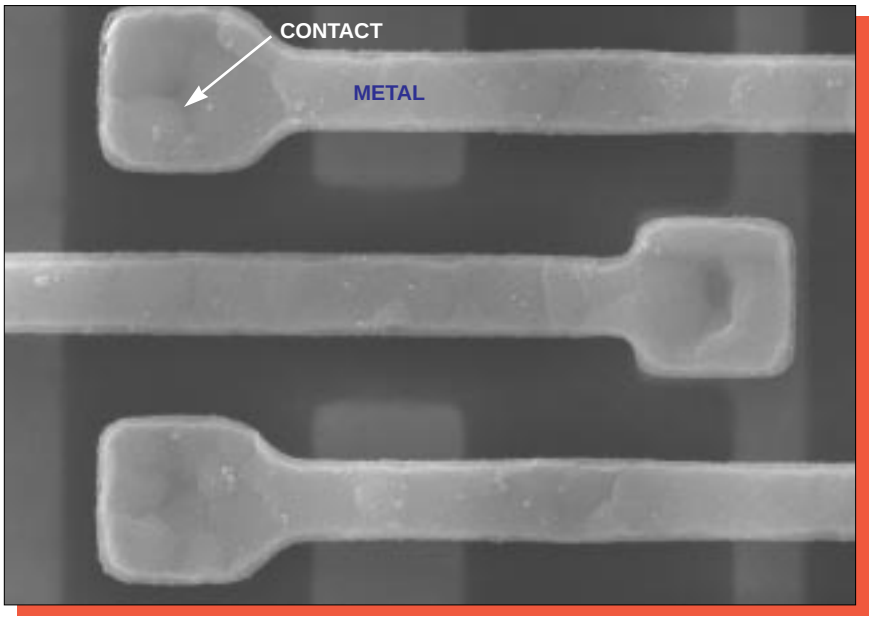


Mag. 40,000x

Figure 11. SEM section views of metal line profiles.

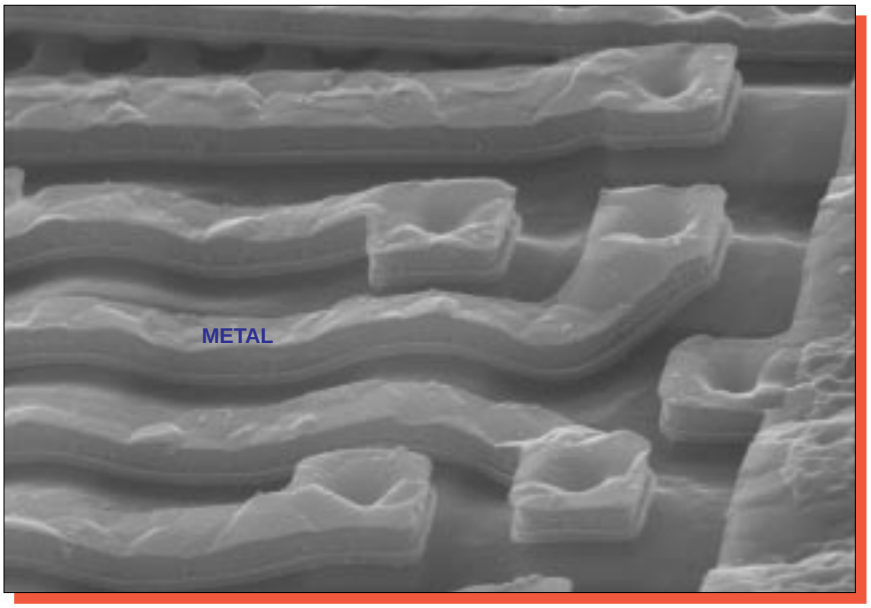


Mag. 4400x

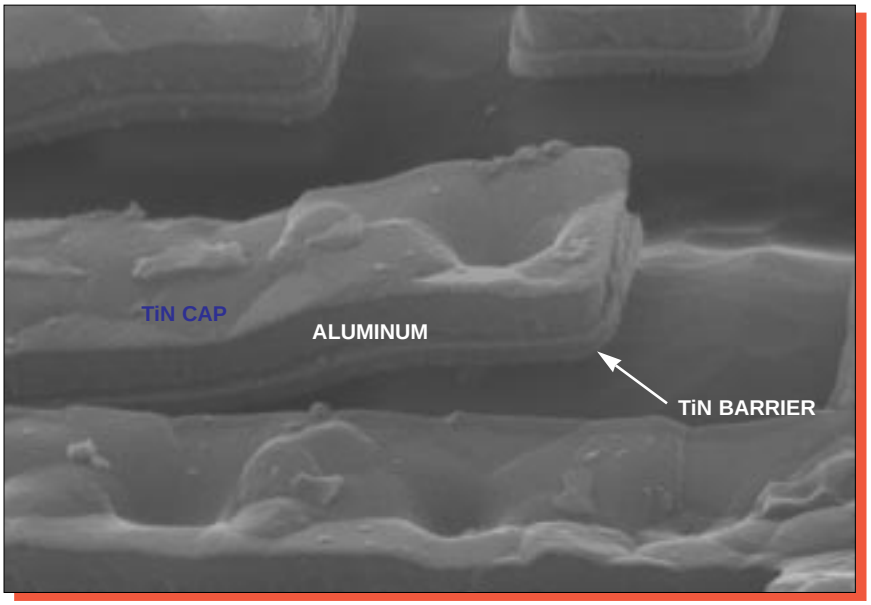


Mag. 7700x

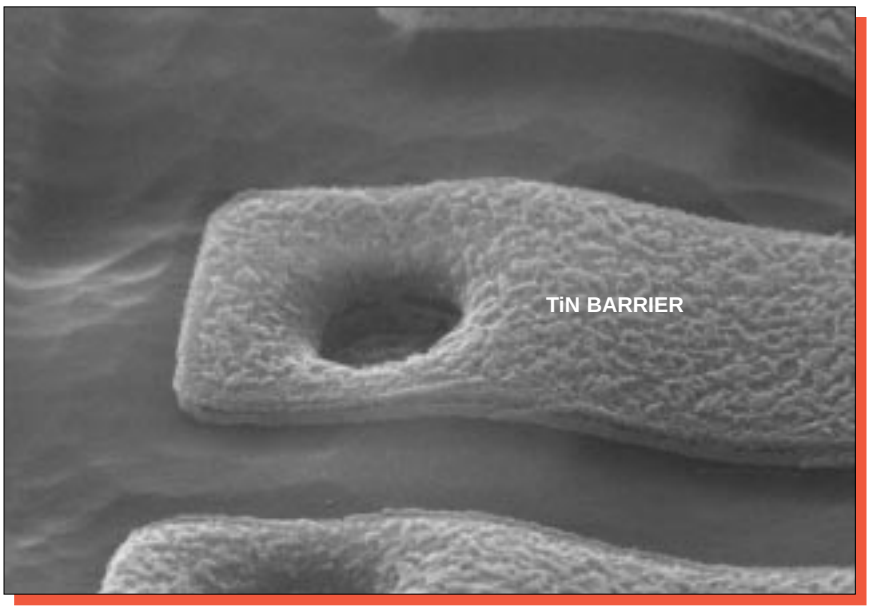
Figure 12. Topological SEM views illustrating metal patterning. 0°.



Mag. 6500x

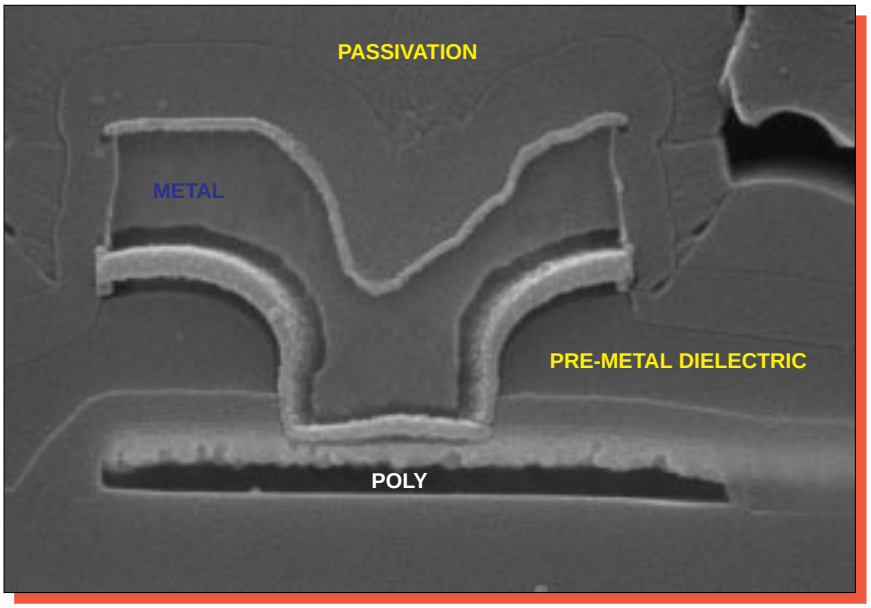


Mag. 13,000x

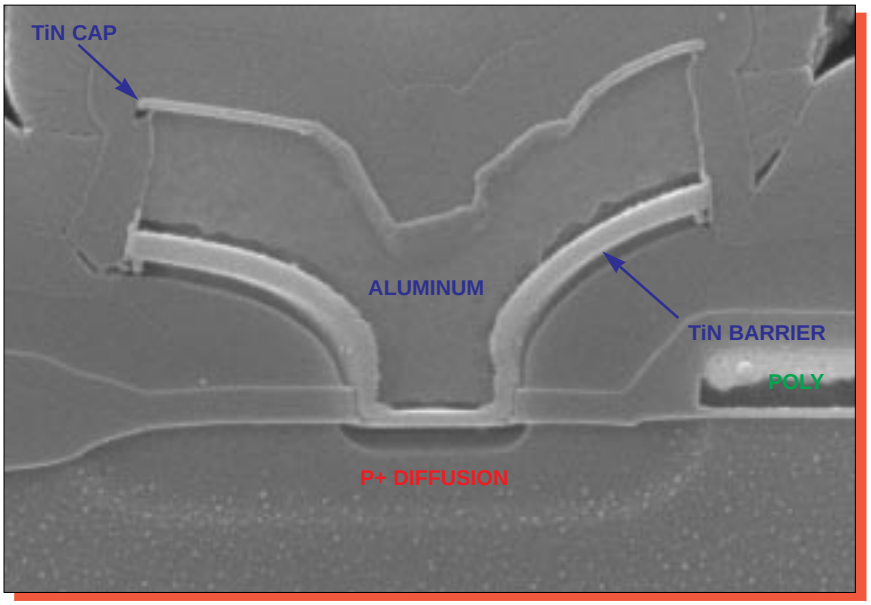


Mag. 20,000x

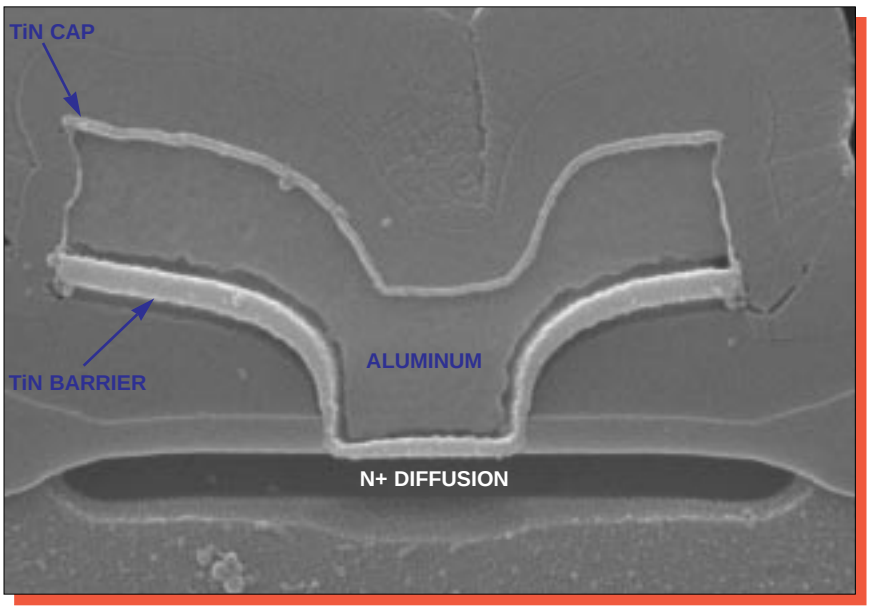
Figure 13. SEM views illustrating metal step coverage and barrier coverage. 60°.



metal 1-to-poly

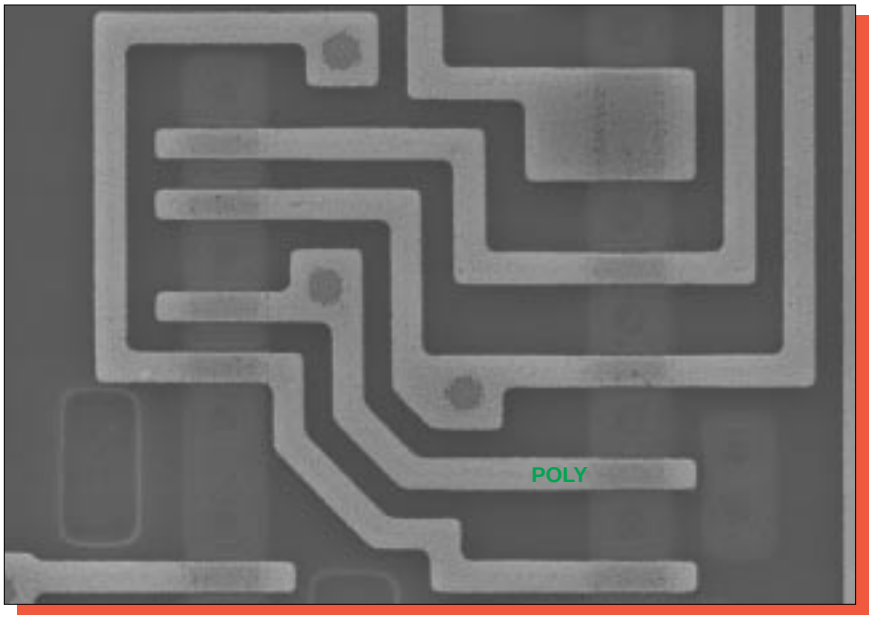


metal 1-to-P+

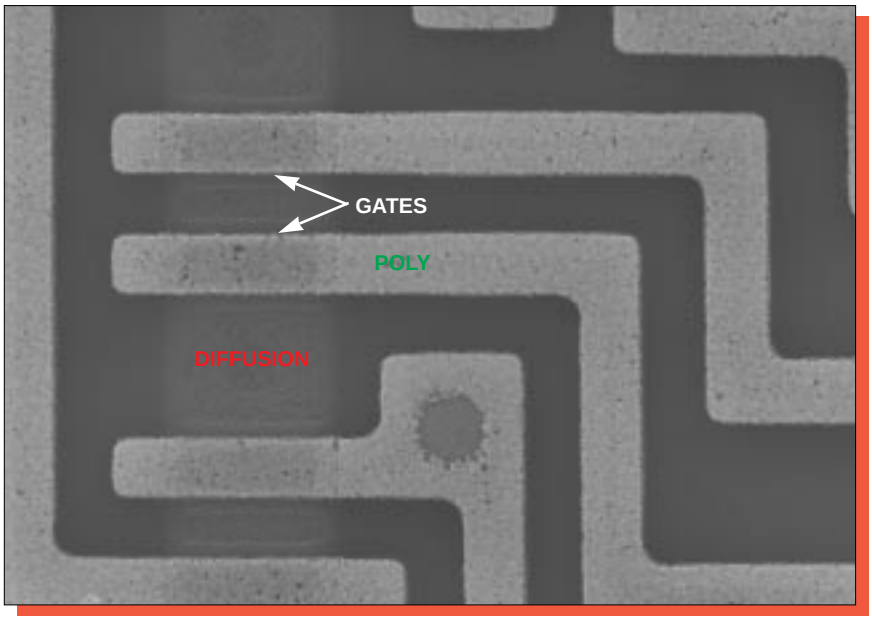


metal 1-to-N+

Figure 14. SEM section views of metal contacts (silicon etch). Mag. 26,000x.

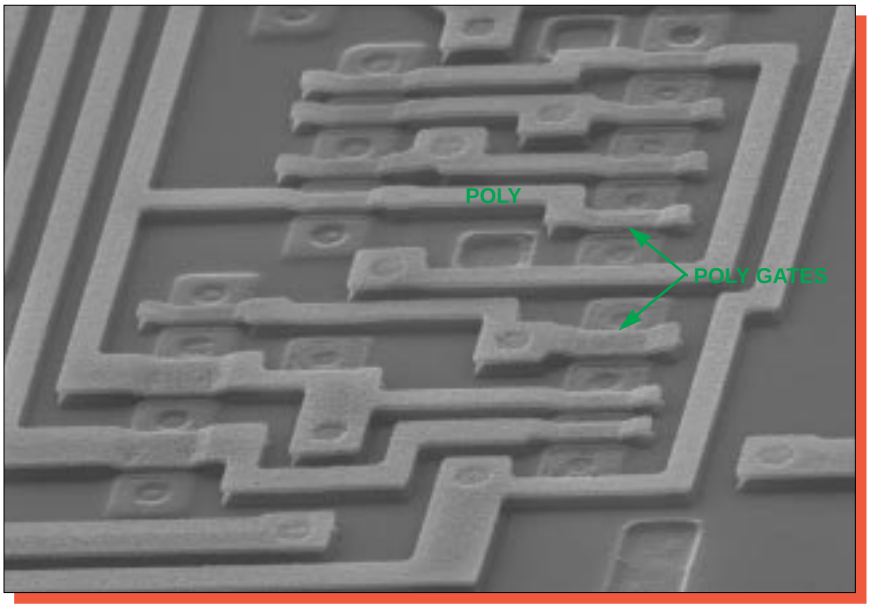


Mag. 3200x

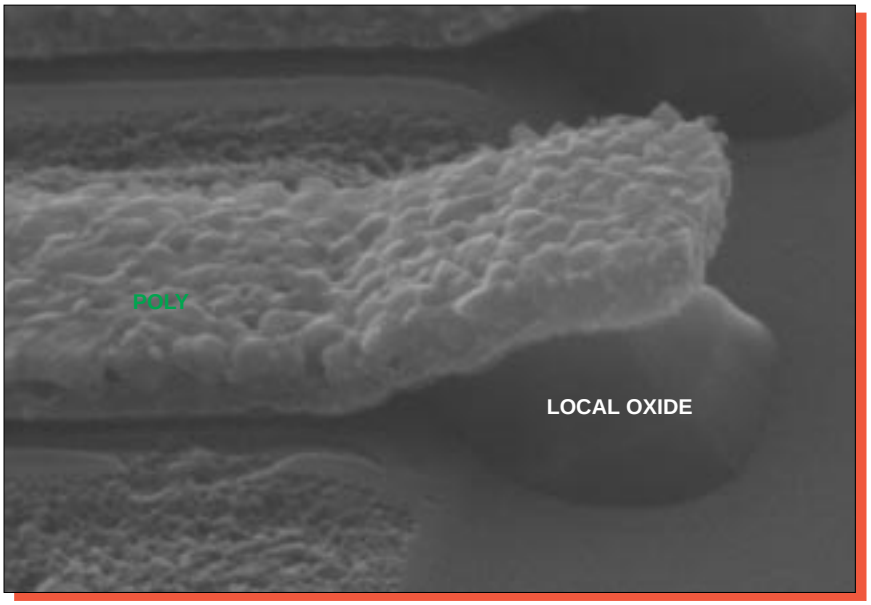


Mag. 6500x

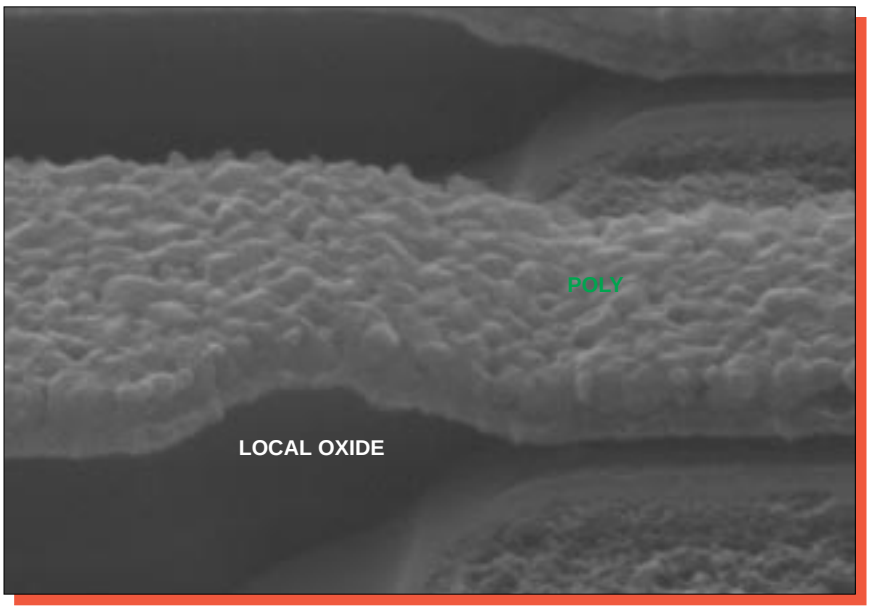
Figure 15. Topological SEM views of poly patterning. 0°.



Mag. 3200x

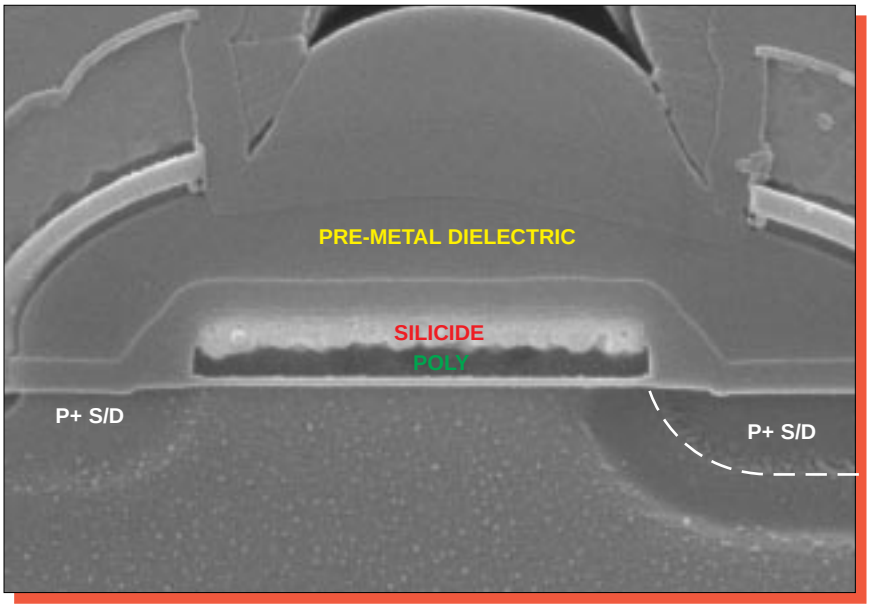


Mag. 40,000x

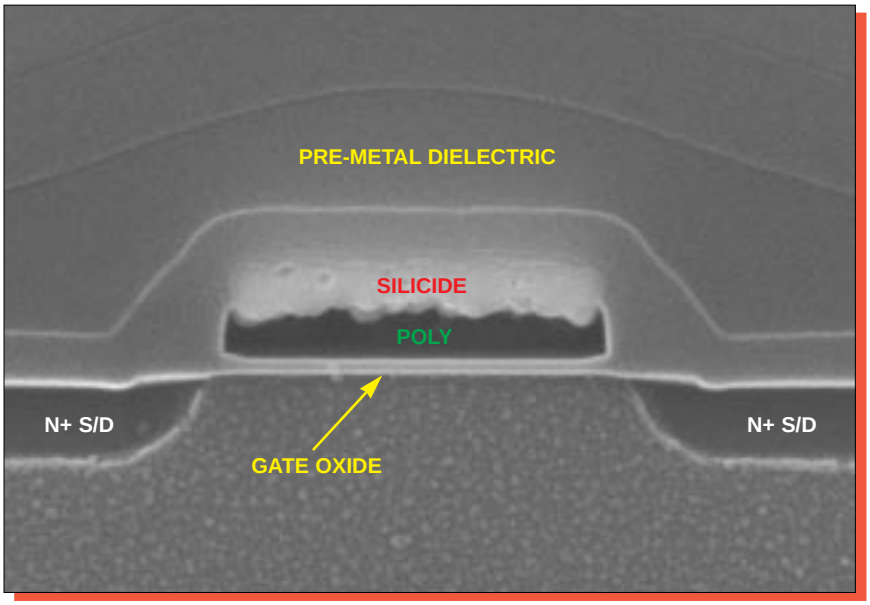


Mag. 40,000x

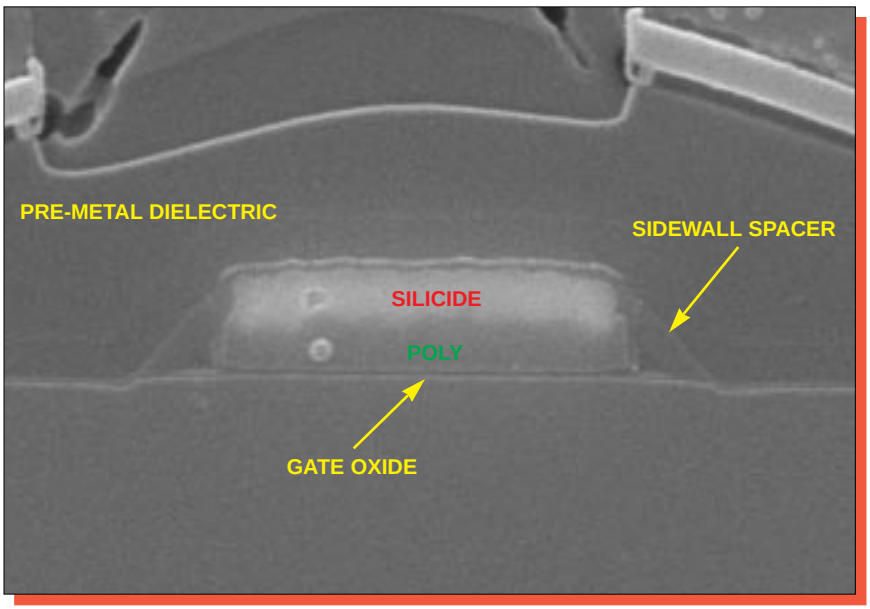
Figure 16. Perspective SEM views of poly coverage. 60°.



P-channel,
Mag. 26,000x



N-channel,
Mag. 40,000x



glass-etch,
Mag. 40,000x

Figure 17. SEM section views of typical transistors.

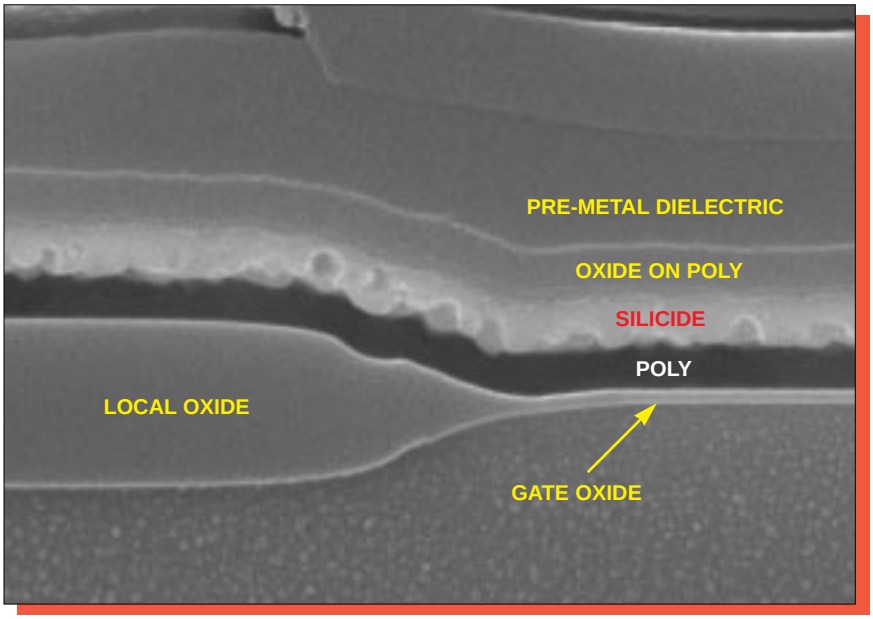


Figure 18. SEM section view of a typical local oxide birdsbeak. Mag. 40,000x.

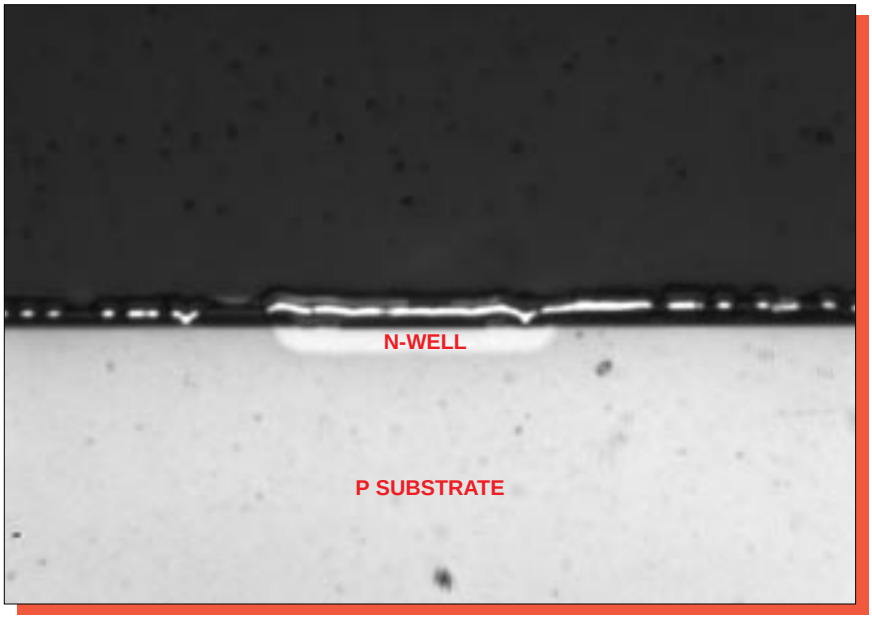
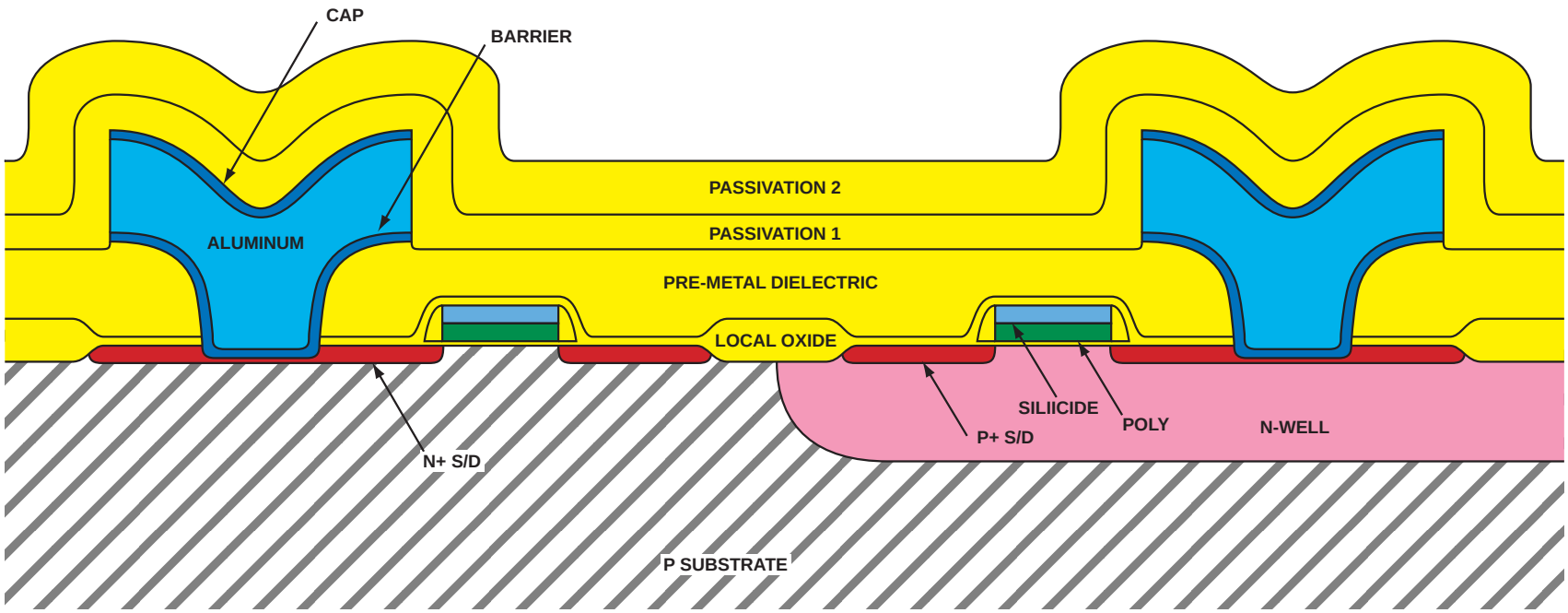


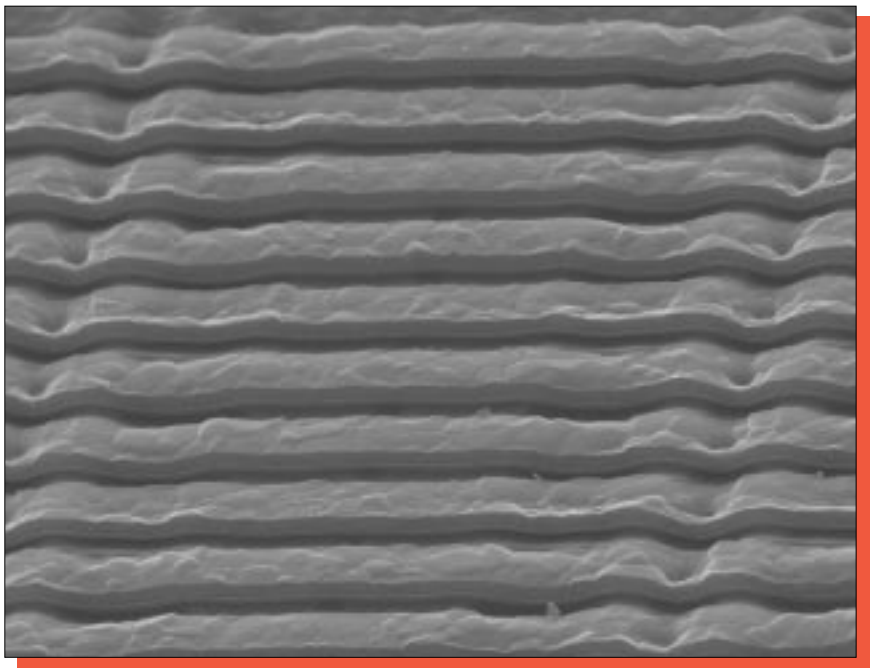
Figure 19. Optical section view illustrating the well structure. Mag. 800x.



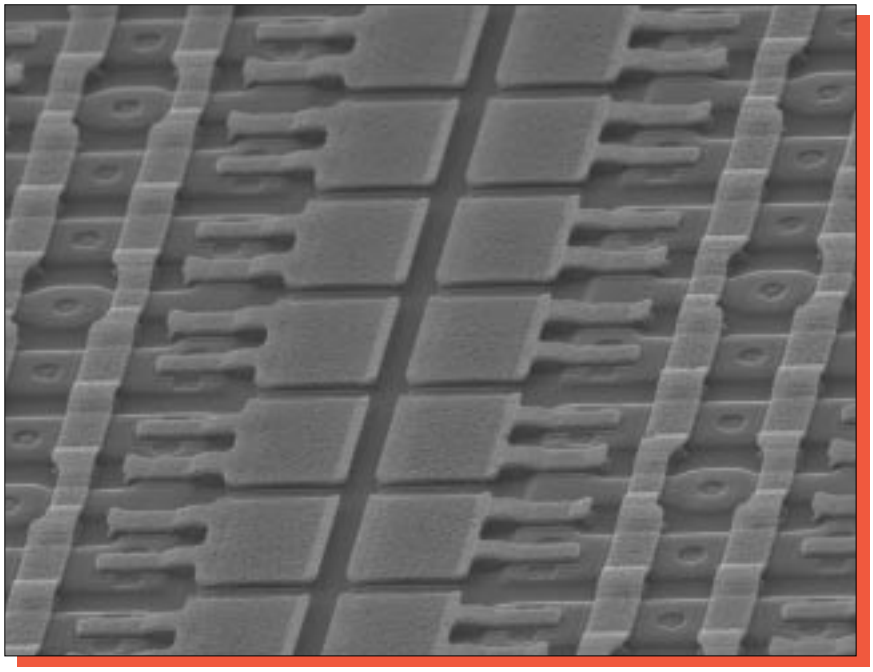
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 20. Color cross section drawing illustrating device structure.

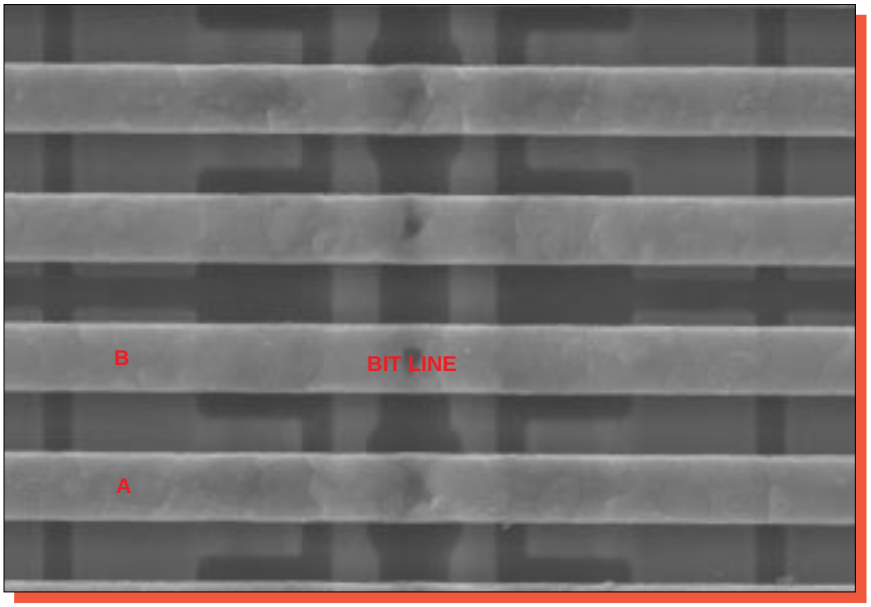


metal 1

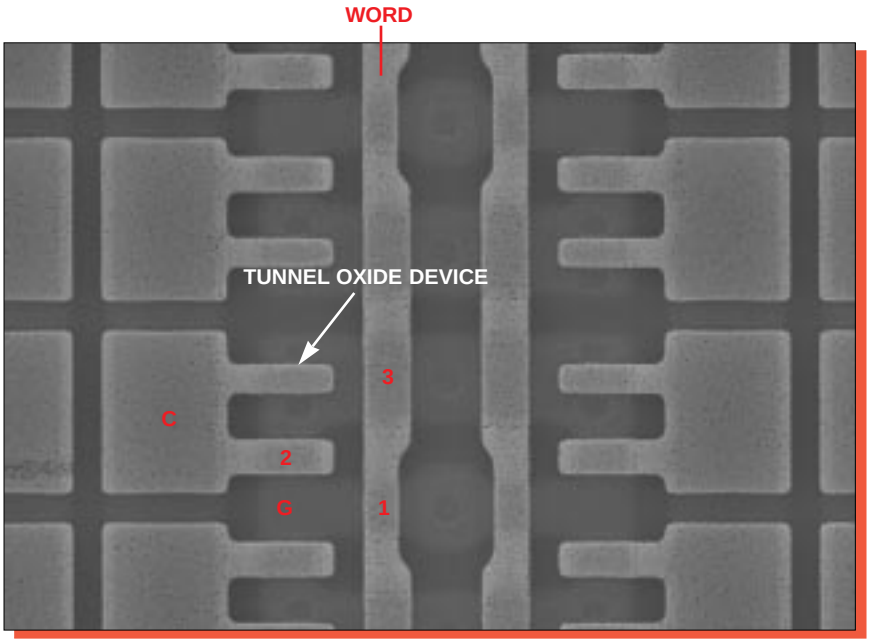


poly

Figure 21. Perspective SEM views of the EEPROM cell array. Mag. 3200x, 60°.



metal 1



poly

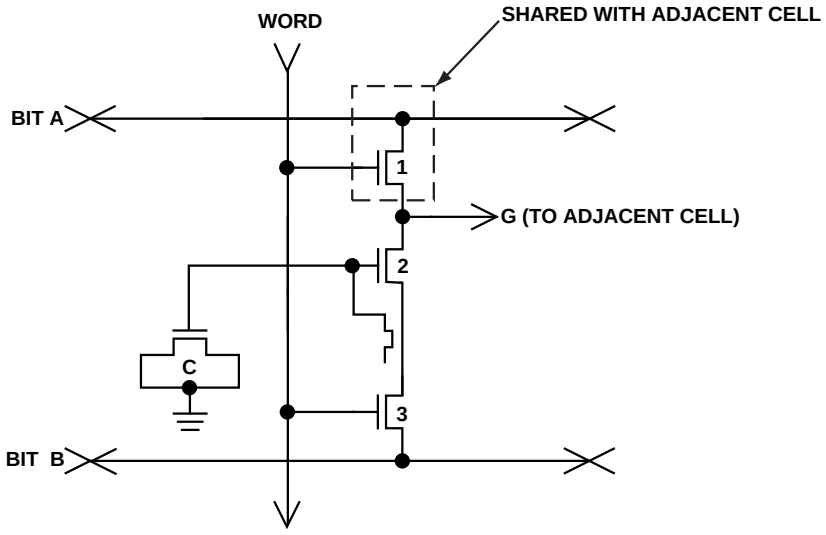
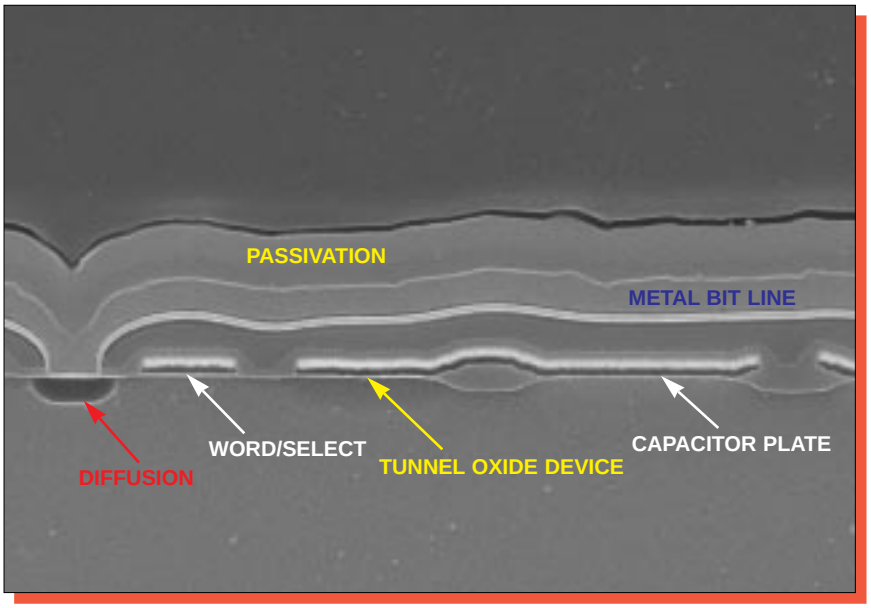
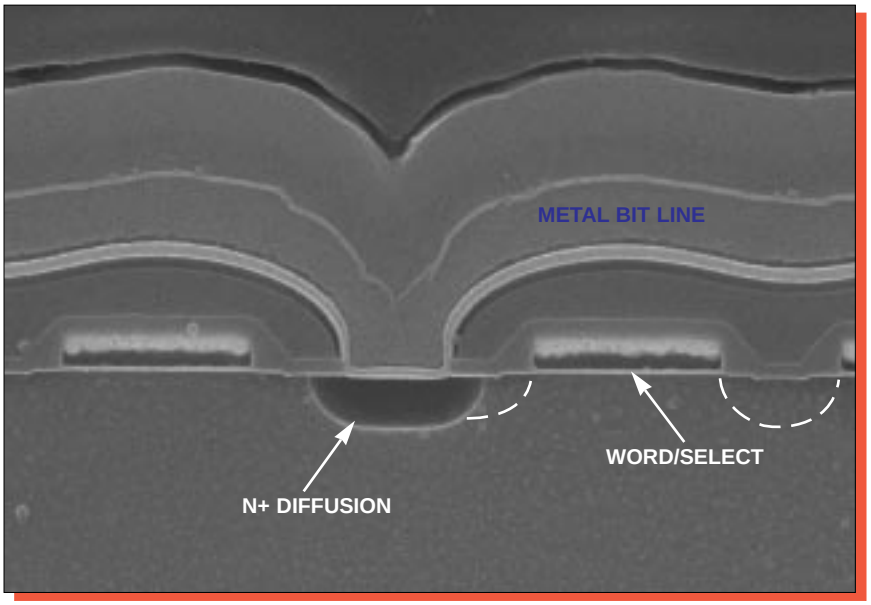


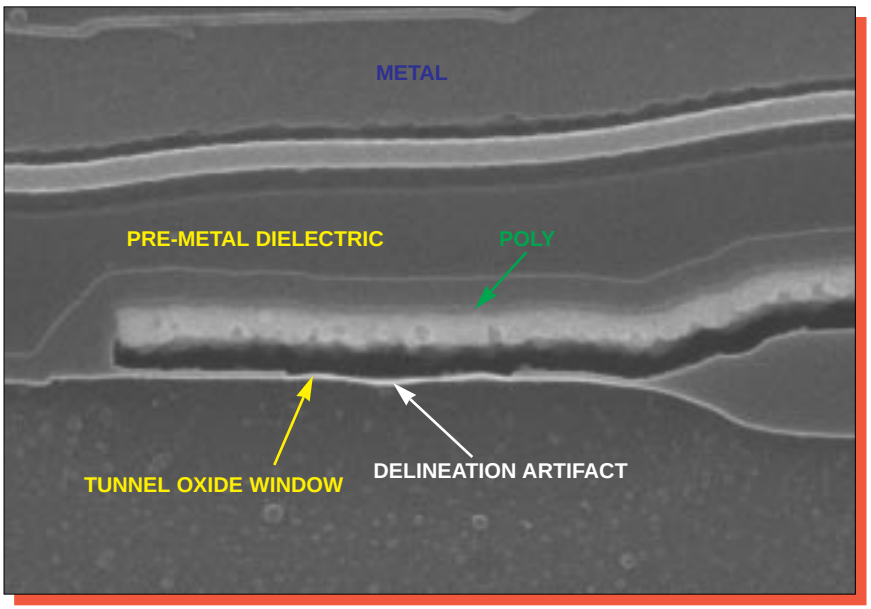
Figure 22. Topological SEM views and schematic of the EEPROM cell. Mag. 3200x, 0°.



Mag. 6500x

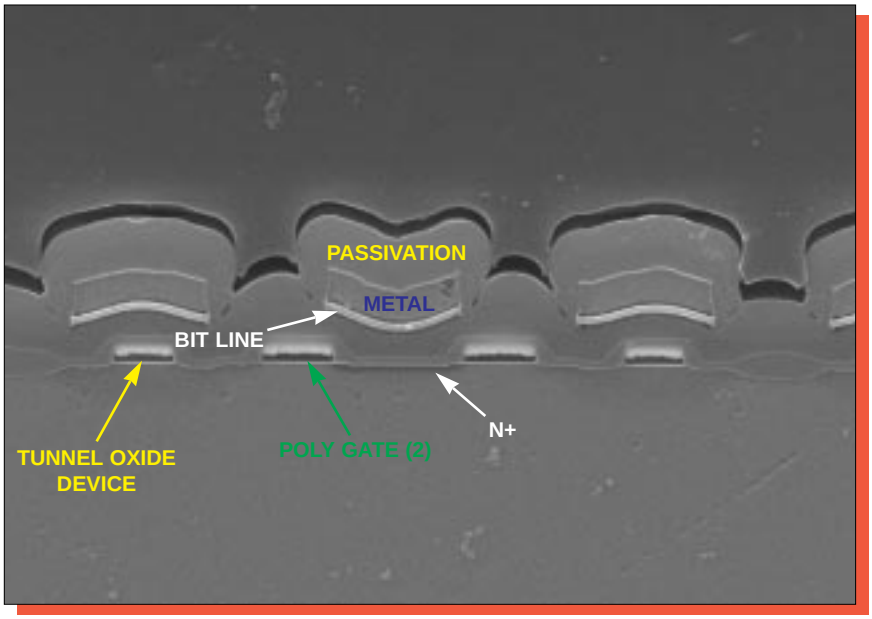


Mag. 13,000x

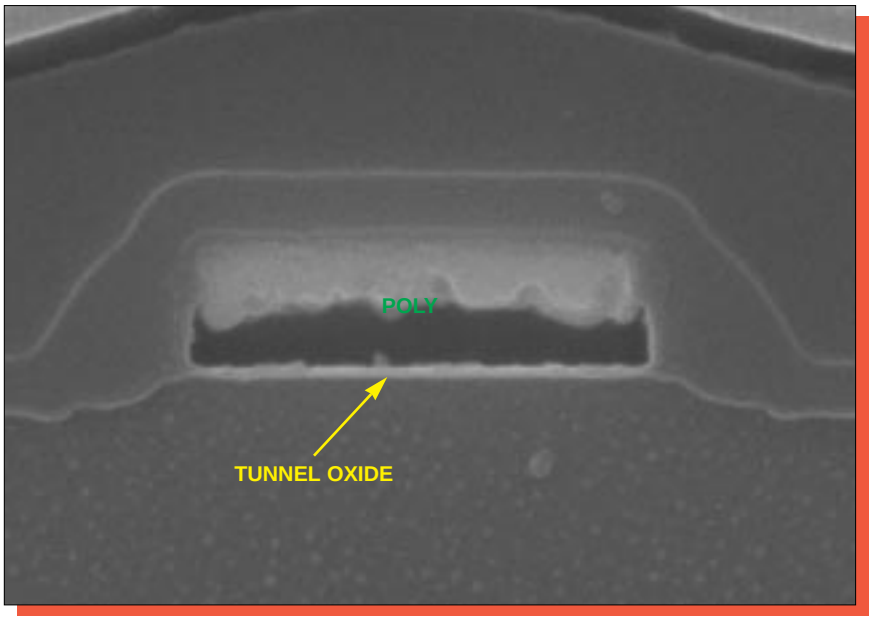


Mag. 26,000x

Figure 23. SEM section views of the EEPROM cell (parallel to bit line).

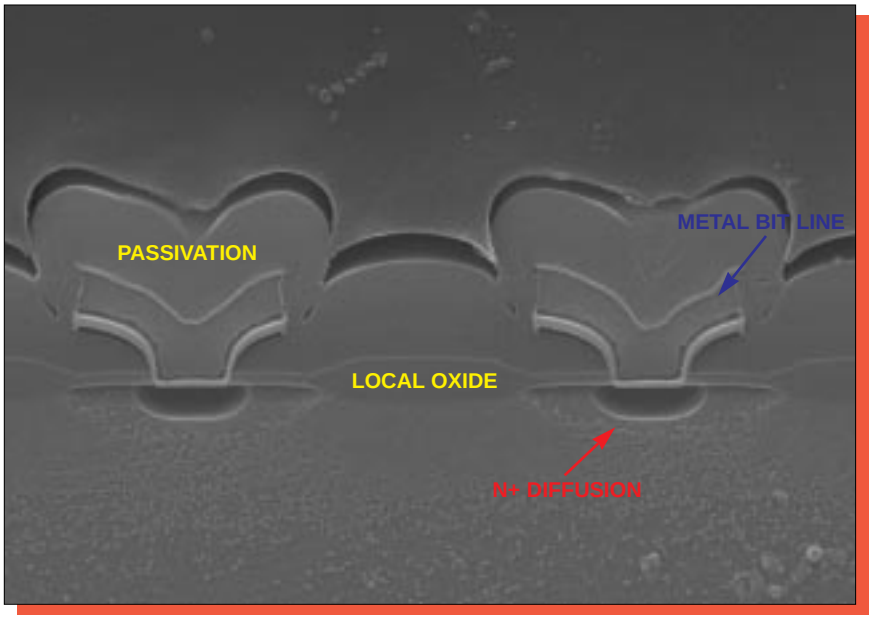


Mag. 6500x

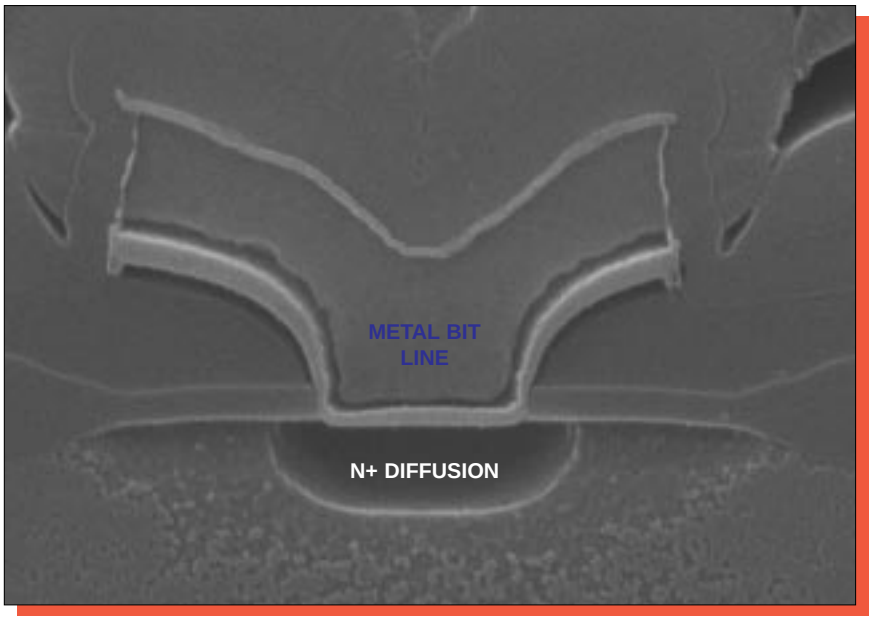


Mag. 52,000x

Figure 24. SEM section views of the EEPROM cell (perpendicular to bit lines).

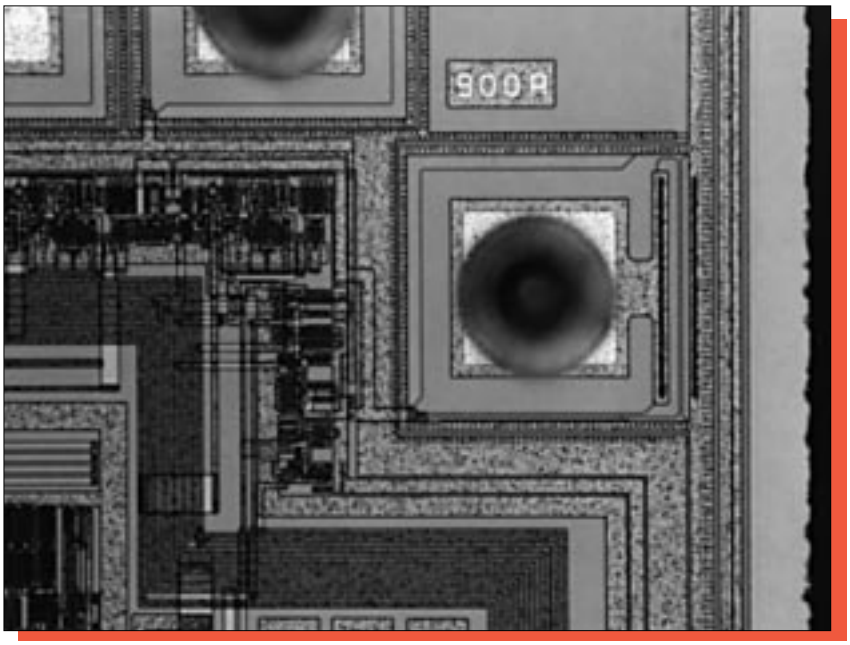


Mag. 10,000x

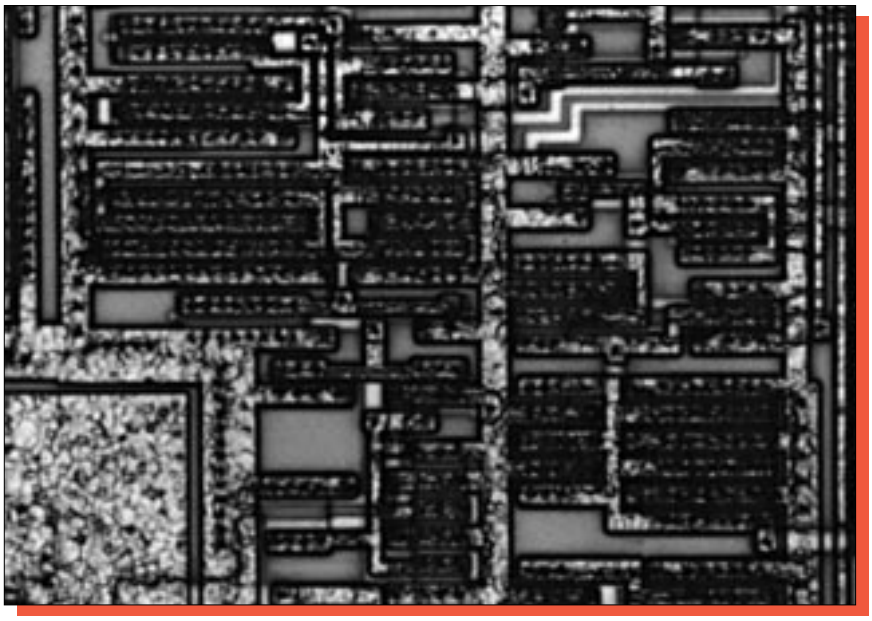


Mag. 26,000x

Figure 25. SEM section views of the EEPROM cell (perpendicular to bit line).



Mag. 200x



Mag. 800x

Figure 26. Optical views of an I/O structure and general circuitry.