Construction Analysis

AMD/Vantis MACHL V466-10
EEPLA

Report Number: SCA 9709-554

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the AMD (Vantis) MACHLV466-10 EEPLA. One decapped device was received for the analysis. It was date coded 9704.

MAJOR FINDINGS

- CMP planarization.
- Sub-micron gate lengths (0.4 micron N-channel and 0.45 micron P-channel).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Die Process:

- Devices were fabricated using a selective oxidation, P-well CMOS process in a N epi on a P substrate.

- Passivation consisted of a layer of nitride over a layer of silicon-dioxide.

- Metallization employed three layers of metal. All metal layers consisted of aluminum with titanium-nitride caps. Tungsten (W) plugs were used at all three layers for vias and contacts.

- Interlevel dielectric 2 (between metals 3 and 2) consisted of two layers of silicon-dioxide with a planarizing glass (SOG) layer in between. Interlevel dielectric 1 (between metals 2 and 1) also consisted of two layers of silicon-dioxide with a planarizing glass (SOG) layer in between.

- Pre-metal dielectric consisted of a thick layer of glass over a layer of low density glass over a thin (sealing) layer of nitride.

- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. No step was noted at the edge of the well, probably indicating a single polarity well process.

TECHNOLOGY DESCRIPTION (continued)

- Two EEPROM cell arrays were used on the device. Cell A in Figures 22 - 28 was the main cell design on the device. Both main portions of the cell were similar; however, Cell B in Figures 28 - 31 used nine additional transistors. Metal 3 was used to distribute GND. Metal 2 was used to form the select lines. Metal 1 was used to form Out 2, Out 1, and the PGM lines. Poly was used to form all the gates on both cells.

- Redundancy fuses were not present.

ANALYSIS RESULTS

Die Process: **Figures 7 - 34**

Questionable Items:[1] None.

Special Features:

- CMP planarization incorporating an SOG.
- Sub-micron gate lengths (0.4 micron N-channel and 0.45 micron P-channel).

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, N-well CMOS process in a P-epi on a P substrate.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Final passivation: Consisted of a layer of nitride over a layer of silicon-dioxide. The integrity test indicated defect-free passivation. Edge seal was good.
- Metallization: Three levels of metal. All layers consisted of aluminum with titanium-nitride caps. Tungsten (W) plugs were used under all three metal layers.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS (continued)

- Metal patterning: All metal layers were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in any of the metal layers. No silicon nodules were noted following the removal of any metal layer.

- Metal step coverage: Minimal metal thinning was noted due to the use of CMP planarization and tungsten (W) plugs.

- Interlevel dielectric 2 (between metals 3 and 2) consisted of two layers of silicon-dioxide with a planarizing glass (SOG) layer between. Interlevel dielectric 1 (between metals 2 and 1) also consisted of two layers of silicon-dioxide with a planarizing glass (SOG) layer between. As mentioned both of these were planarized by CMP. No problems were found in any of these layers.

- Pre-metal dielectric: A thick layer of glass over a low density glass over a thin (sealing) layer of silicon-nitride was used under metal 1. This structure was also planarized by CMP.

- Contact defects: Via and contact cuts were defined by a single step process. No over-etching of the contacts and vias was noted.

- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by dry-etch of normal quality.

- Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

ANALYSIS RESULTS (continued)

- Local oxide (LOCOS) isolation was used. No step was present at the well boundaries, probably indicating this is a single polarity well process.

- Two EEPROM cell arrays were used on the device. Cell A in Figures 22 - 28 was the main cell on the device. Both cell layouts were similar; however, Cell B in Figures 28 - 31 used nine additional transistors. Metal 3 was used to distribute GND. Metal 2 was used to form the select lines. Metal 1 was used to form Out 2, Out 1, and the PGM lines. Poly formed all the gates on both cell types. Cell "A" pitch was 5.5 x 10.5 microns. Cell "B" pitch was 17.5 x 18 microns.

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection

SEM of passivation

Passivation integrity test

Passivation removal

SEM inspection of metal 3

Metal 3 removal and inspect barrier

Delayer to metal 2 and inspect

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die attach quality	N
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	N
Contact coverage	N
Contact registration	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIAL ANALYSIS

Final passivation:	Consisted of a layer of nitride over a layer of silicon-dioxide.
Metallization 3:	Aluminum (Al) with a titanium-nitride (TiN) cap.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap.
Plugs:	Tungsten (W).

HORIZONTAL DIMENSIONS

Die size:	7.3 x 7.3 mm (285 x 285 mils)
Die area:	53 mm^2 (81,255 $mils^2$)
Min pad size:	0.11 x 0.13 mm (4.7 x 5.1 mils)
Min pad window:	0.09 x 0.09 mm (3.7 x 3.7 mils)
Min pad space:	10 microns
Min metal 3 width:	1.0 micron
Min metal 3 space:	0.5 micron
Min metal 3 pitch:	1.5 micron
Min metal 2 width:	1.0 micron
Min metal 2 space:	0.4 micron
Min metal 2 pitch:	1.4 micron
Min metal 1 width:	0.65 micron
Min metal 1 space:	0.45 micron
Min metal 1 pitch:	1.1 micron
Min via (M3-M2):	0.45 micron (diameter)
Min via (M2-M1):	0.5 micron (diameter)
Min contact:	0.55 micron
Min poly width:	0.4 micron
Min poly space:	0.55 micron
Min gate length - (N-channel):*	0.4 micron
- (P-channel):	0.45 micron
EEPROM cell size (cell A):	57.8 $microns^2$
EEPROM cell pitch (cell A):	5.5 x 10.5 microns
EEPROM cell size (cell B):	315 $microns^2$
EEPROM cell pitch (cell B):	17.5 x 18 microns

**Physical gate length*

VERTICAL DIMENSIONS

Die thickness:	0.4 mm (16.3 mils)

Layers:

Passivation 2:	0.8 micron
Passivation 1:	0.8 micron
Metal 3 - cap:	0.04 micron (approximate)
- aluminum:	0.8 micron
Interlevel dielectric 2 - glass 2:	0.8 micron
- glass 1:	0.06 - 0.12 micron
Metal 2 - cap:	0.10 micron
- aluminum:	0.85 micron
Interlevel dielectric 1- glass 2:	0.35 micron
- glass 1:	0.15 - 0.5 micron
Metal 1 - cap:	0.1 micron
- aluminum:	0.5 micron
Pre-metal dielectric:	0.75 - 1.2 micron
Sealing nitride:	0.05 micron
Poly:	0.22 micron
Local oxide:	0.35 micron
N+ S/D:	0.22 micron
P + S/D:	0.15 micron
N-well:	2 microns (approximate)

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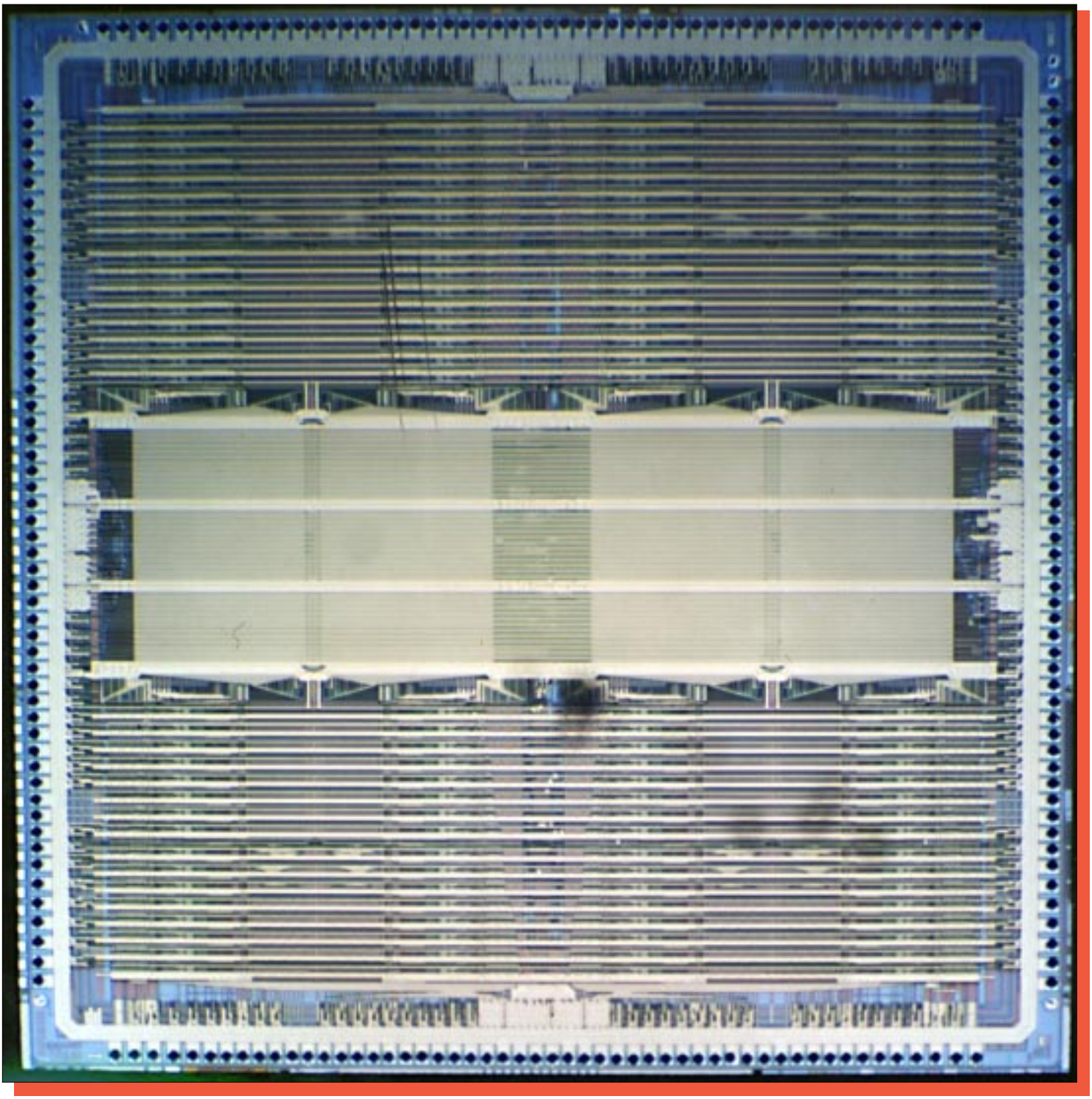


Figure 1. Whole die photograph of the AMD/Vantis MACHL V466-10. Mag. 10x.

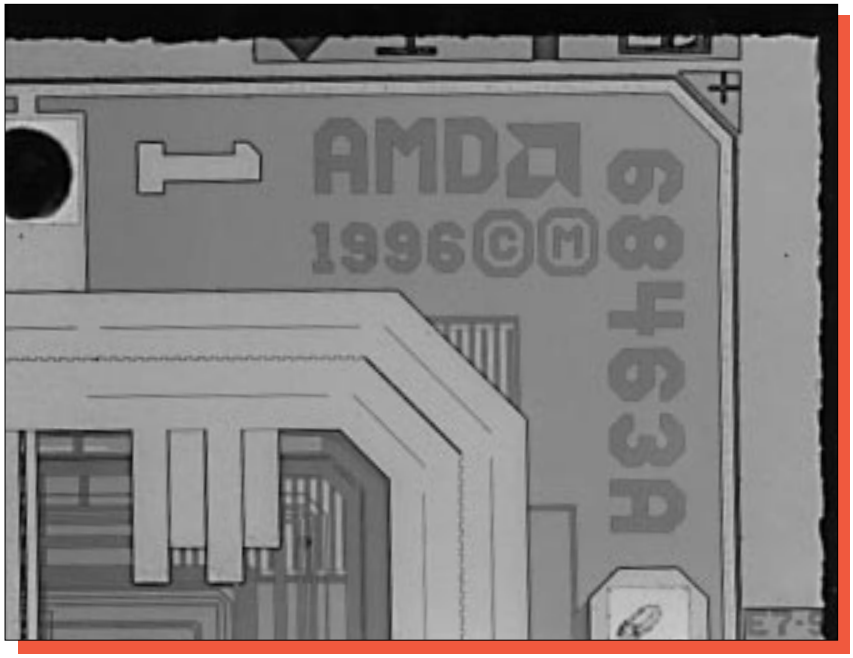
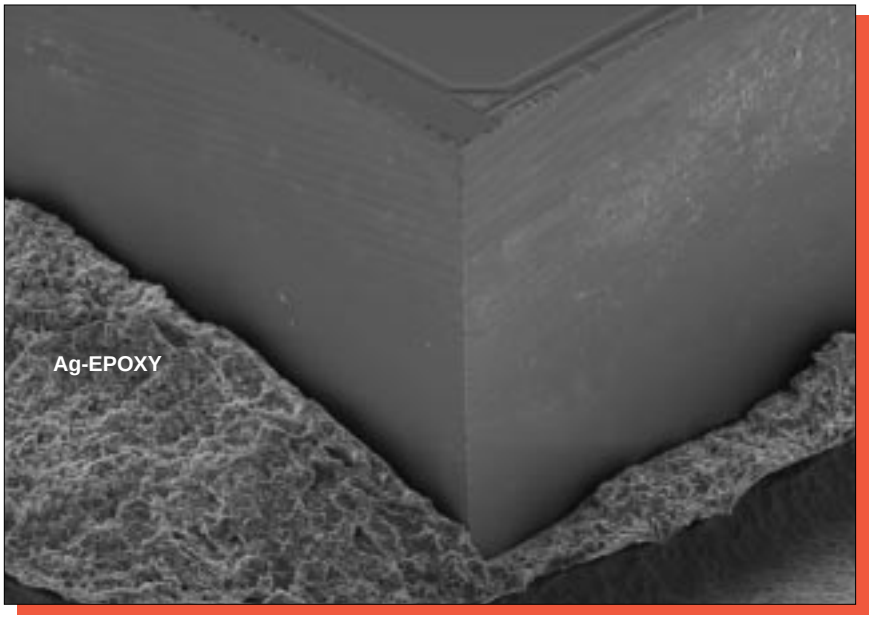
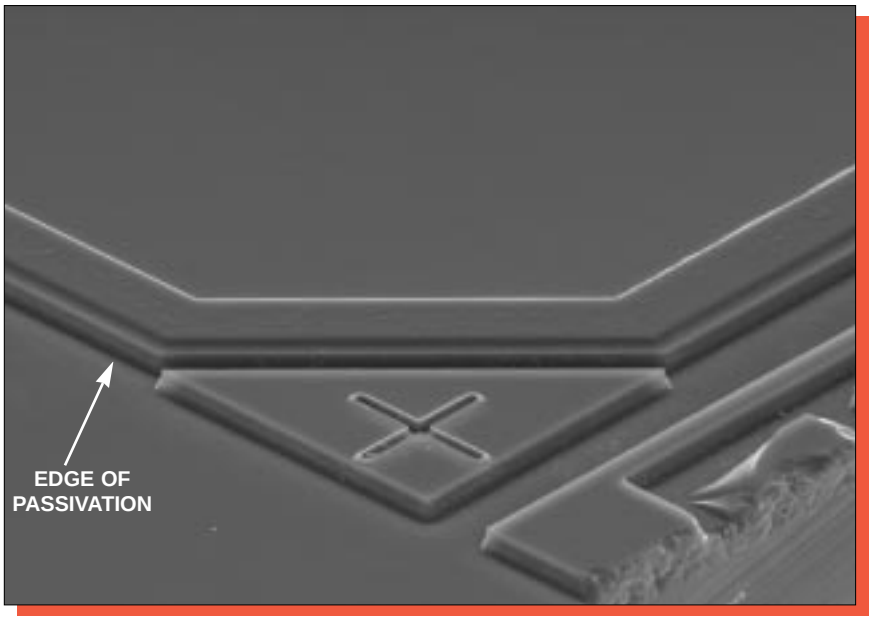


Figure 2. Markings from the die surface. Mag. 160x.

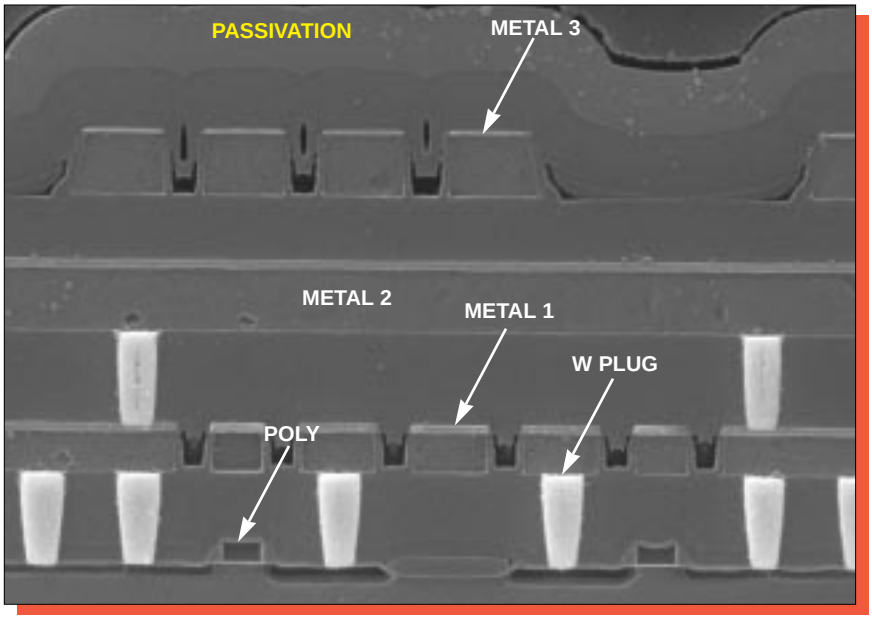


Mag. 130x

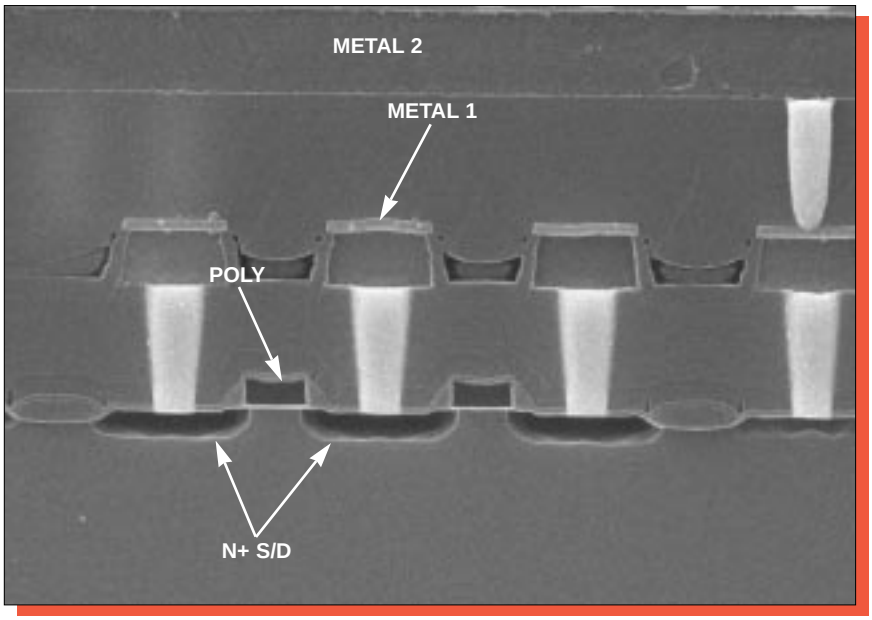


Mag. 1100x

Figure 3. Perspective SEM views of dicing and edge seal. 60°.

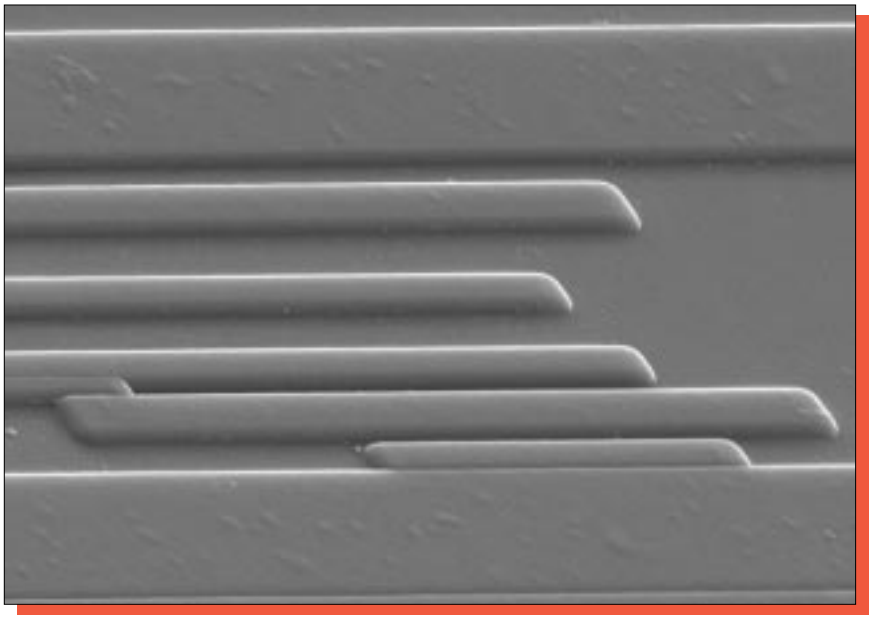


Mag. 10,000x

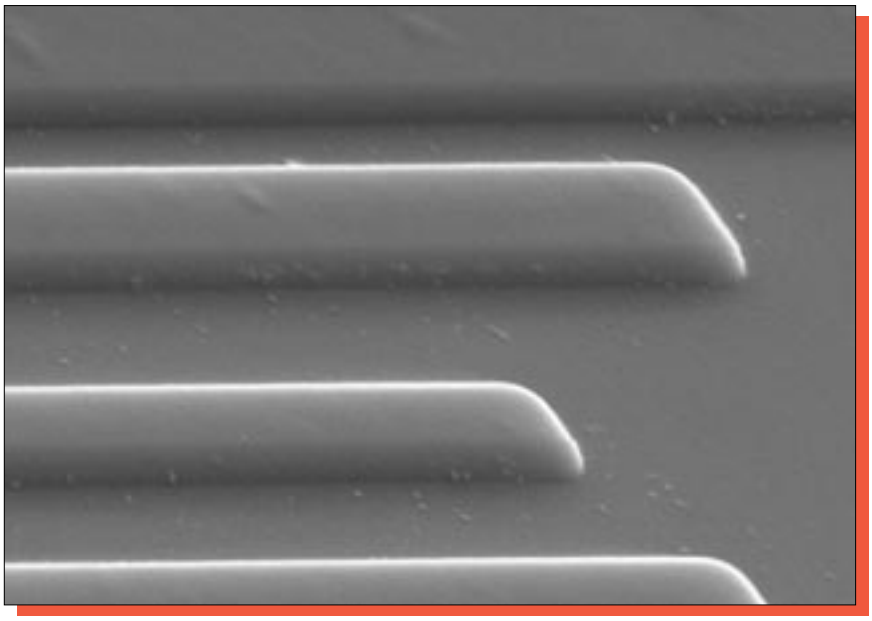


Mag. 13,000x

Figure 4. SEM section views of general device structure.

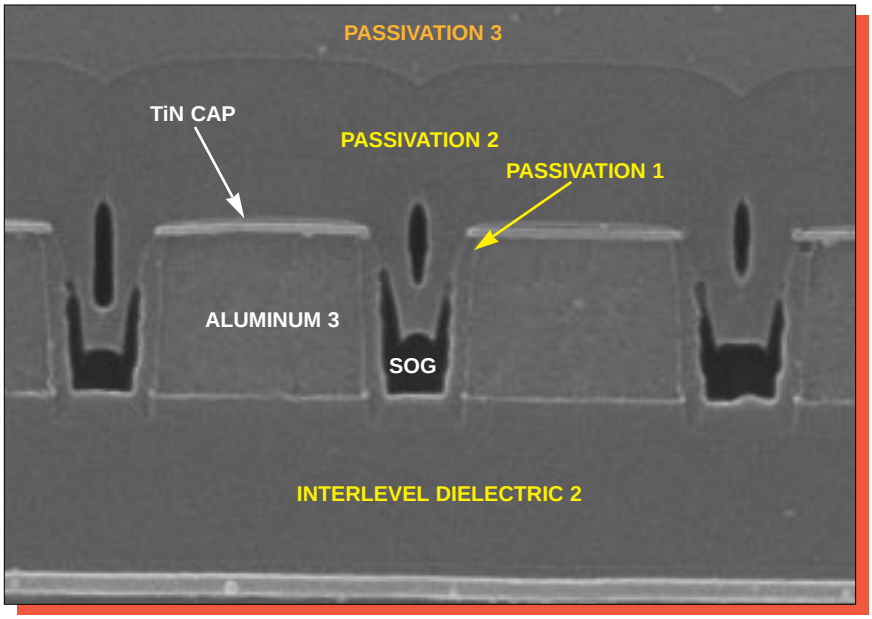


Mag. 2100x

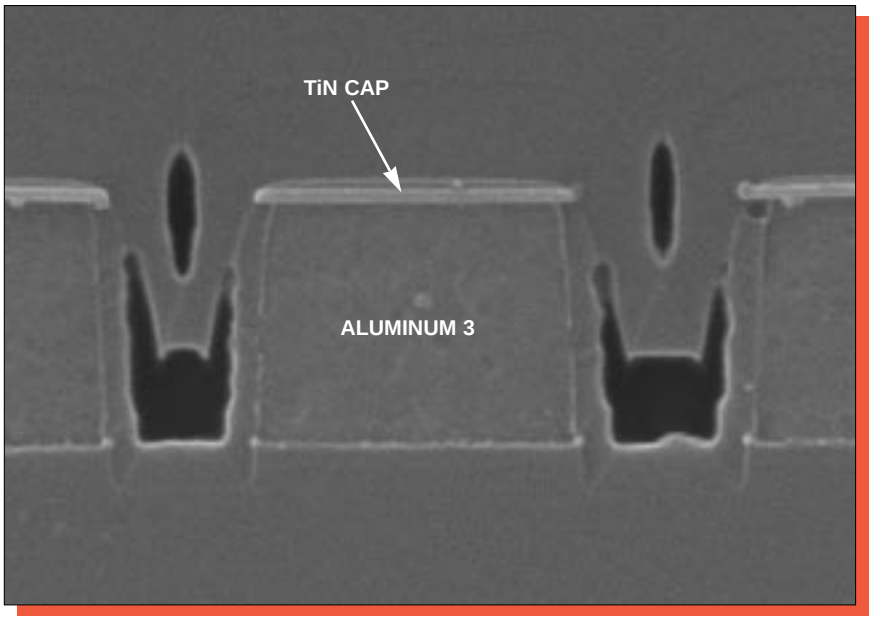


Mag. 4800x

Figure 5. Perspective SEM views illustrating overlay passivation coverage. 60°.

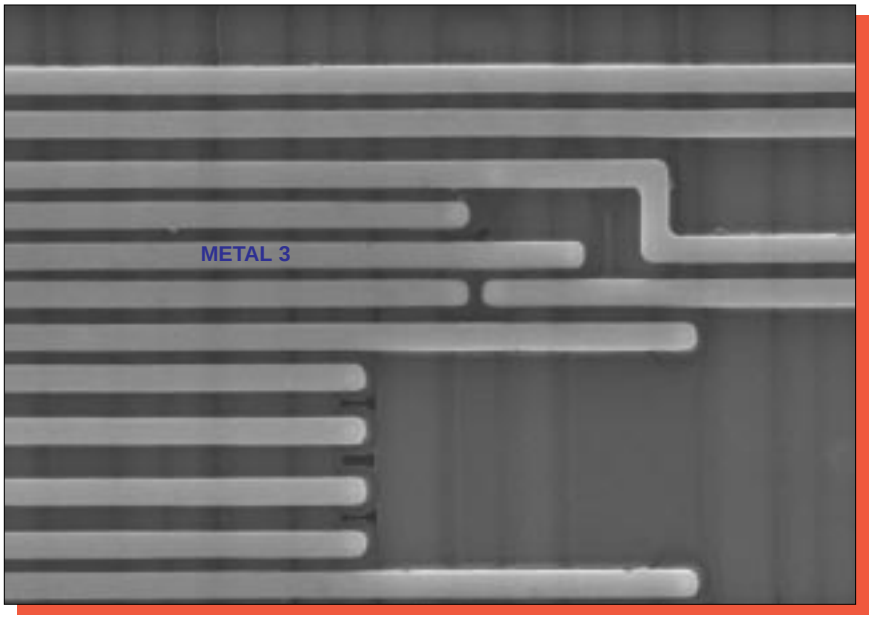


Mag. 26,000x

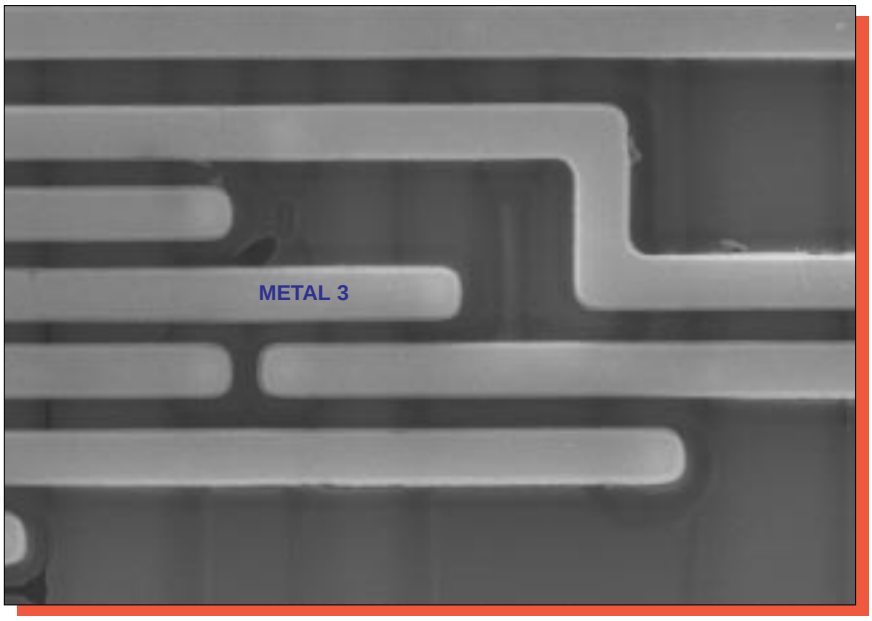


Mag. 40,000x

Figure 6. SEM section views of metal 3 line profiles.

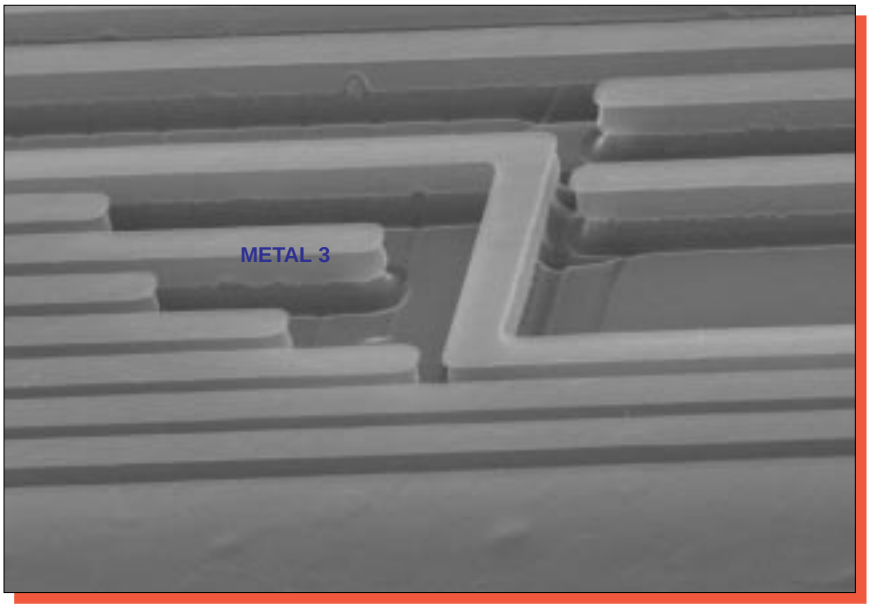


Mag. 3200x

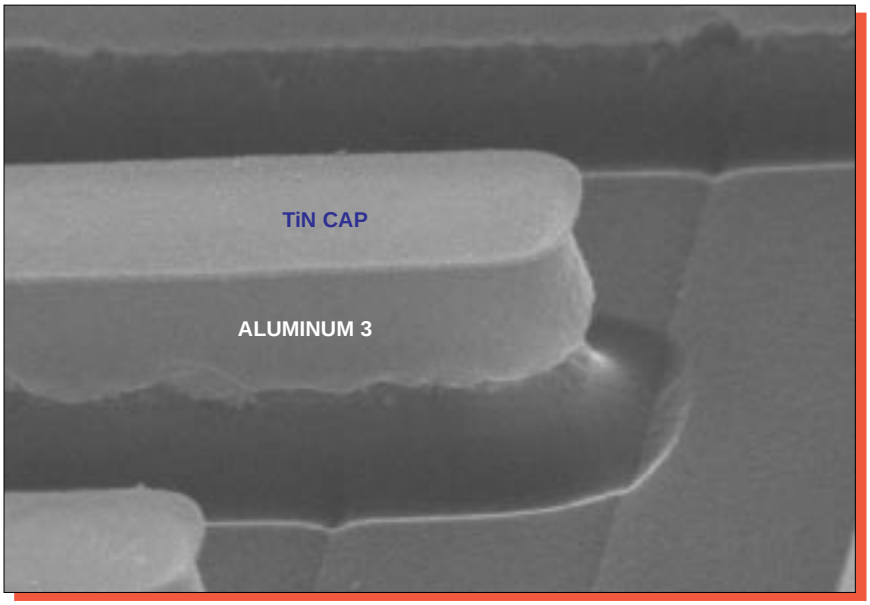


Mag. 6500x

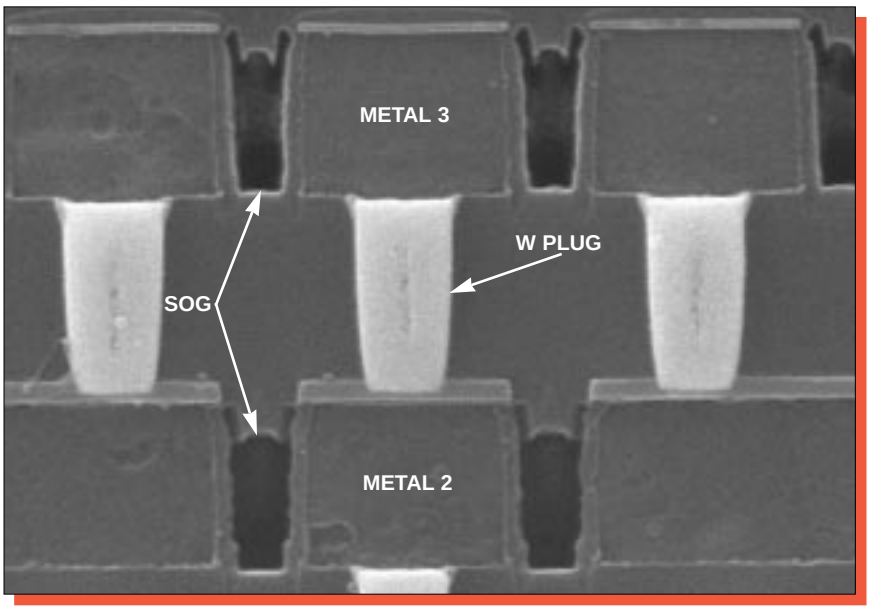
Figure 7. Topological SEM views of metal 3 patterning. 0°.



Mag. 6500x, 60°

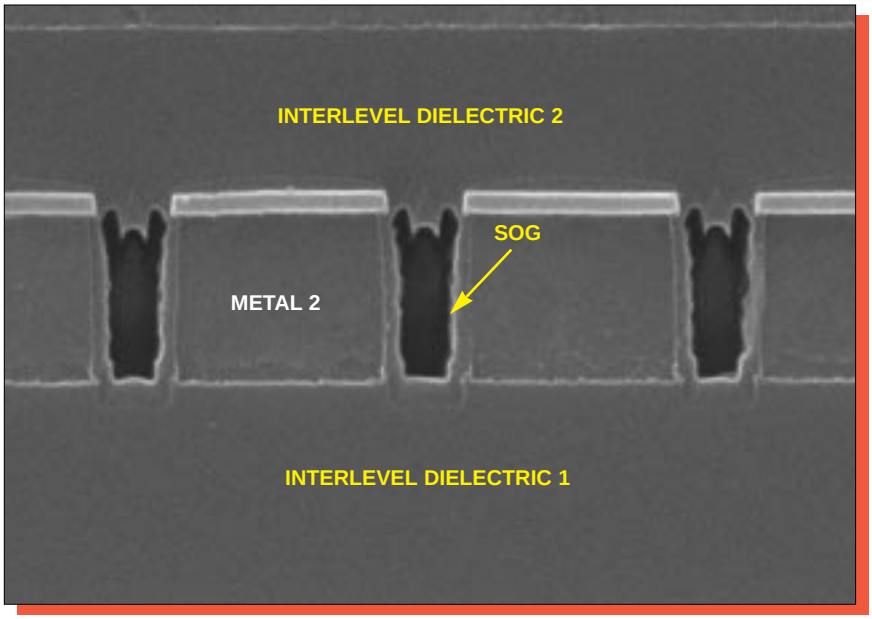


Mag. 26,000x, 60°

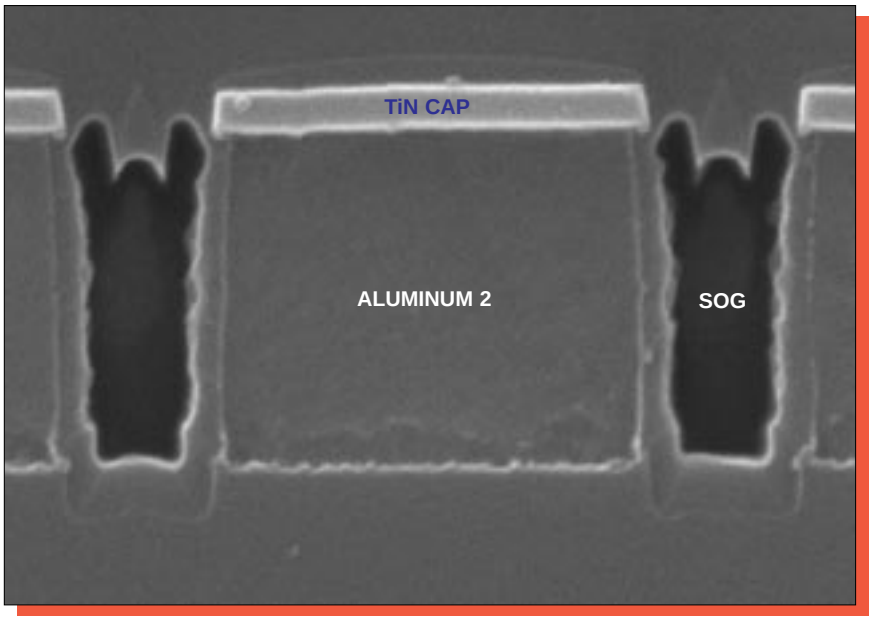


Mag. 26,000x

Figure 8. SEM views illustrating metal 3 step coverage and metal 3-to-metal 2 vias.

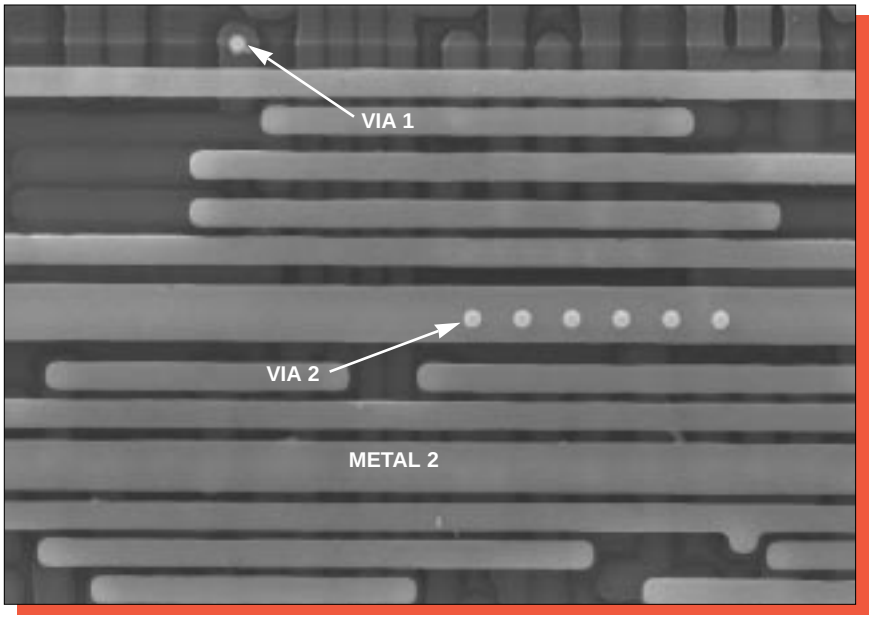


Mag. 26,000x

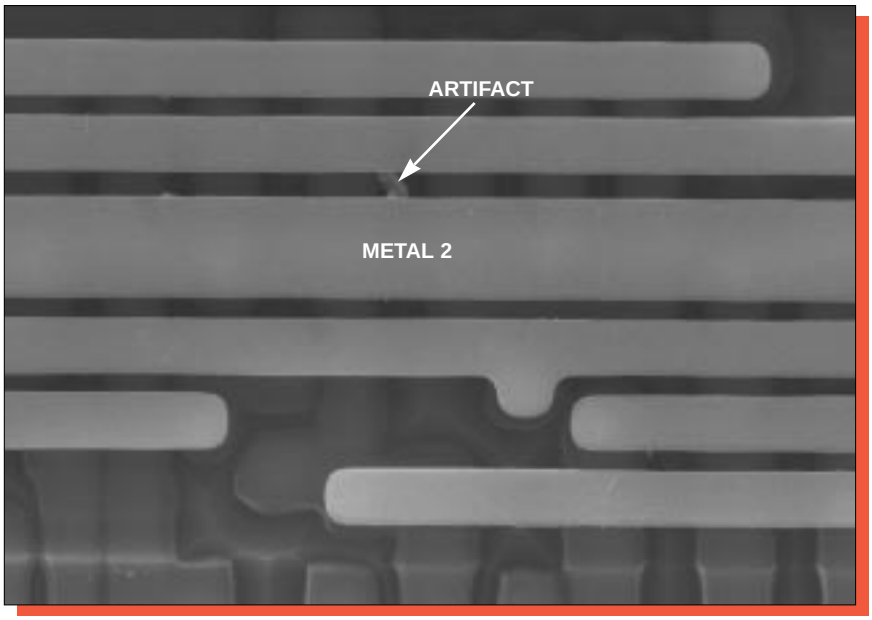


Mag. 52,000x

Figure 9. SEM section views of metal 2 line profiles.

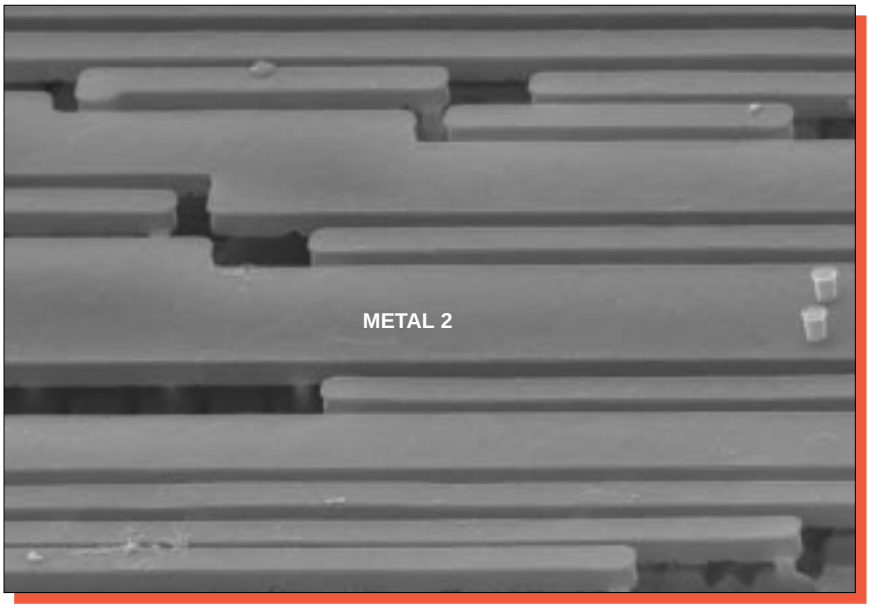


Mag. 3200x

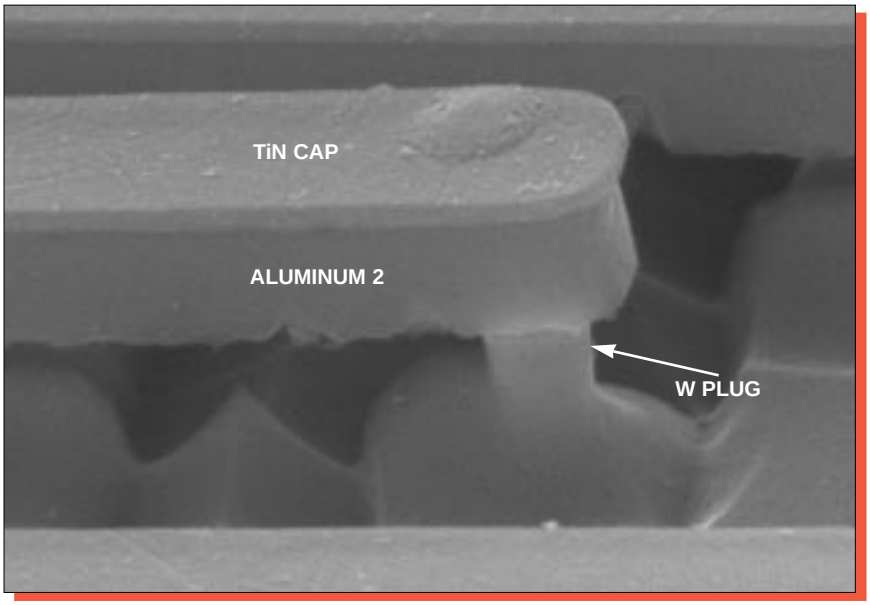


Mag. 6500x

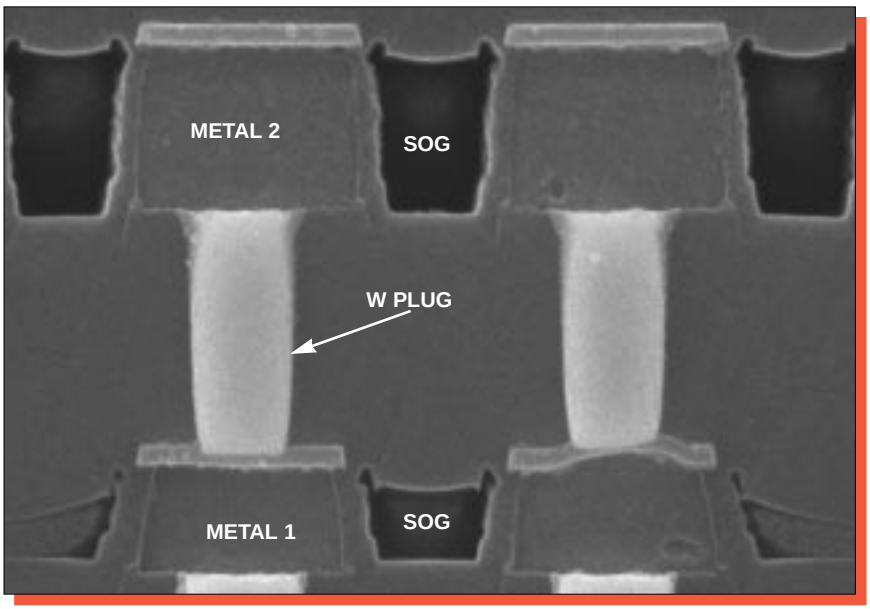
Figure 10. SEM section views of metal 2 patterning. 0°.



Mag. 5000x, 60°

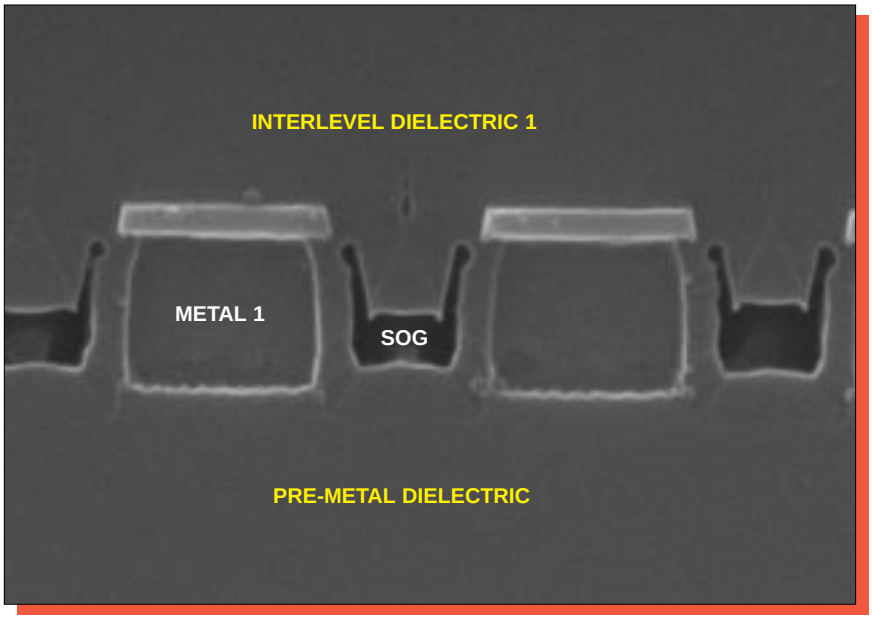


Mag. 26,000x, 60°

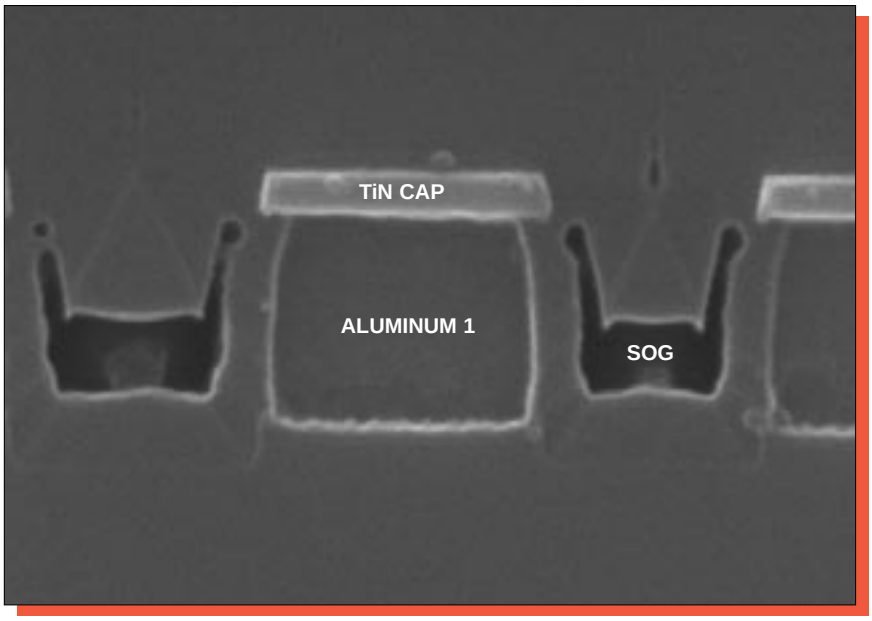


Mag. 26,000x

Figure 11. SEM views illustrating metal 2 step coverage and metal 2-to-metal 1 via.

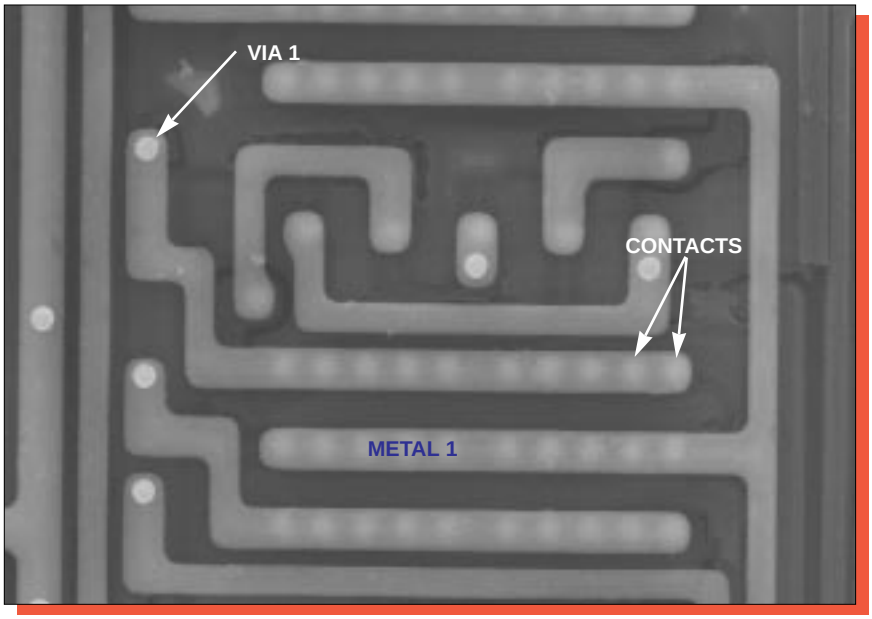


Mag. 40,000x

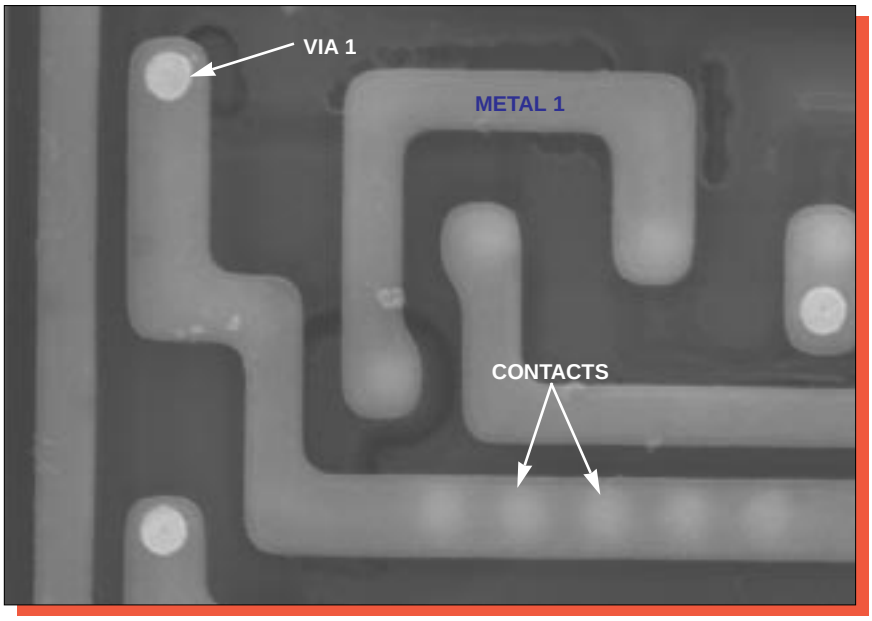


Mag. 52,000x

Figure 12. SEM section views of metal 1 line profiles.

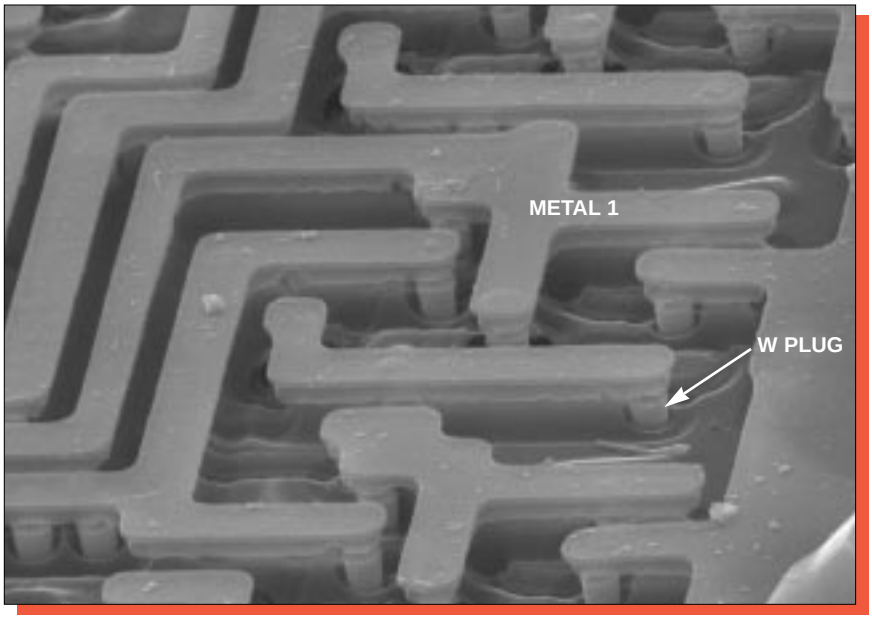


Mag. 5000x

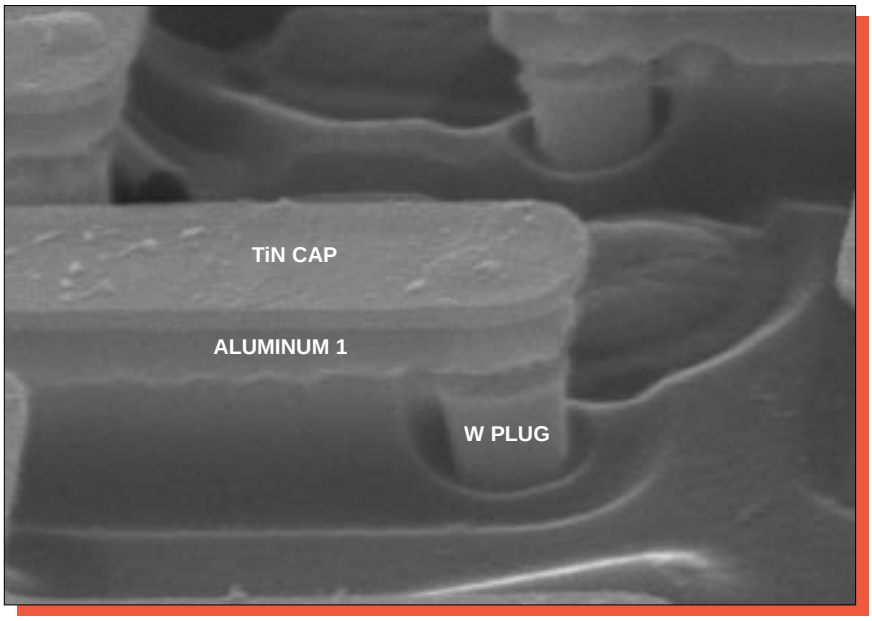


Mag. 10,000x

Figure 13. Topological SEM views of metal 1 patterning. 0°.

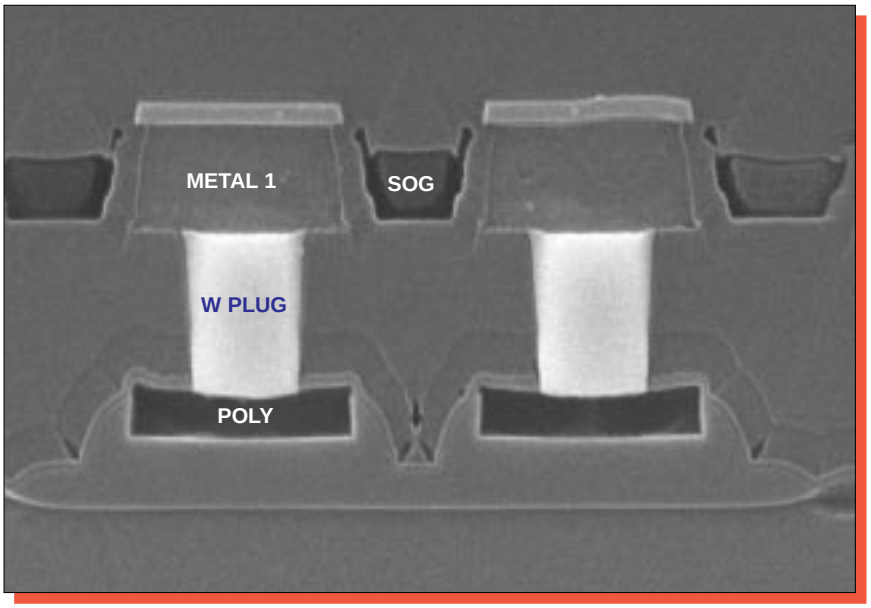


Mag. 8000x

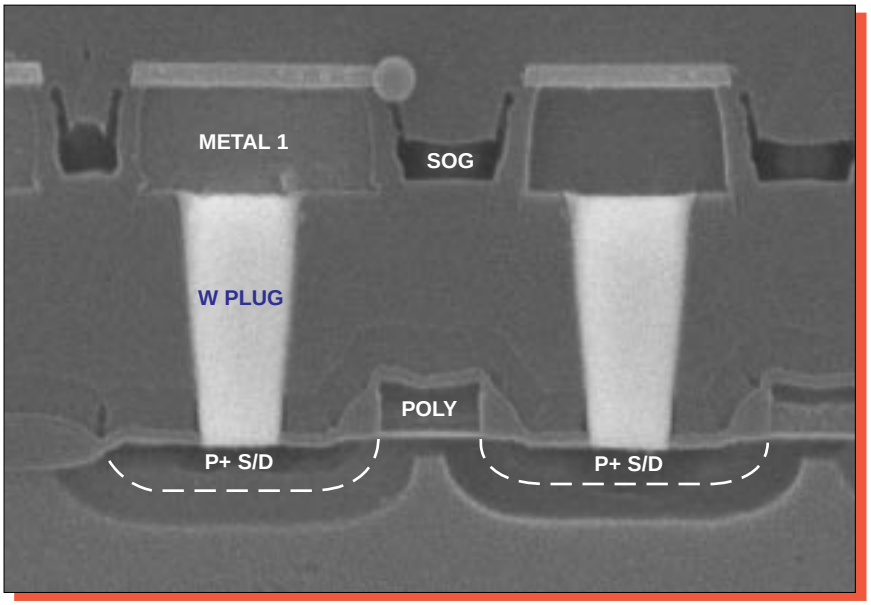


Mag. 26,000x

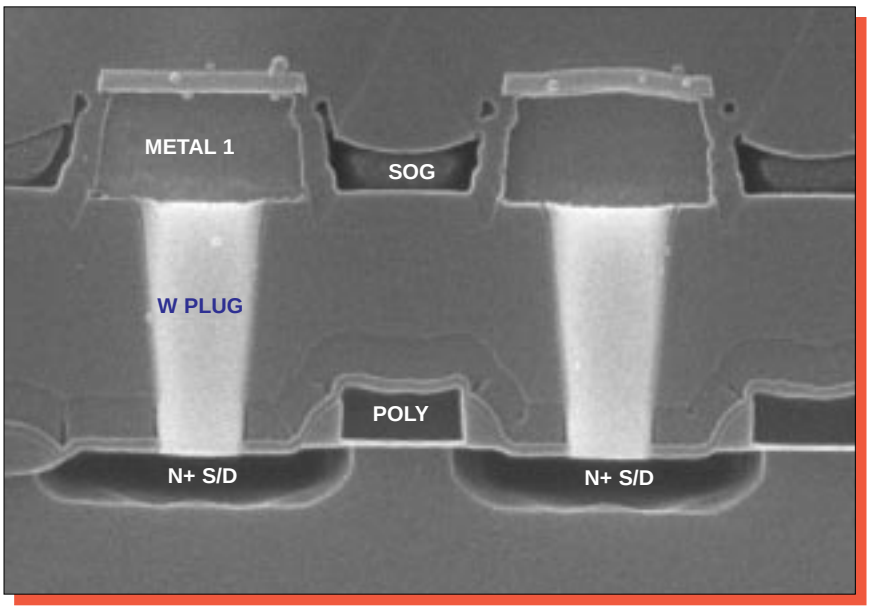
Figure 14. Perspective SEM views illustrating metal 1 step coverage. 60°.



metal 1-to-poly

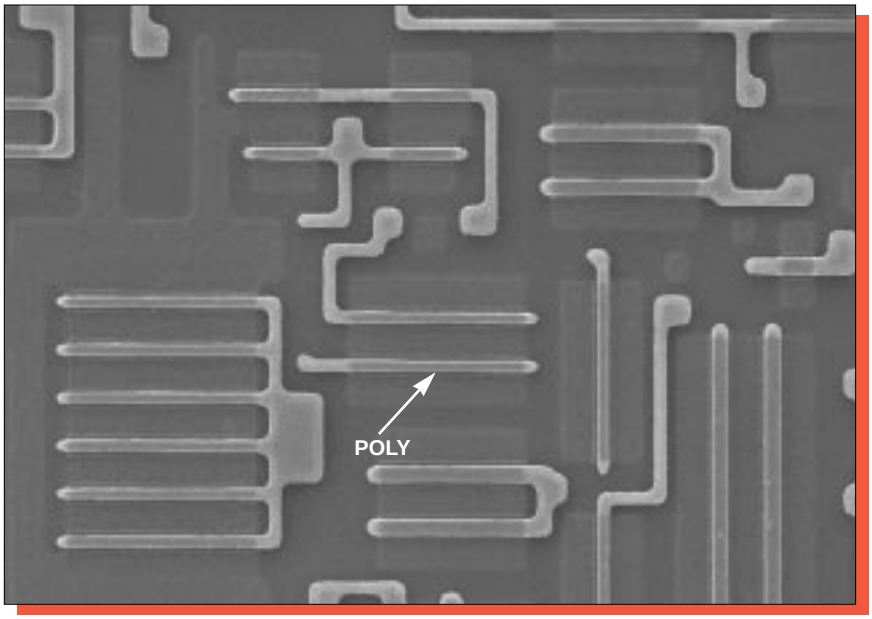


metal 1-to-P+

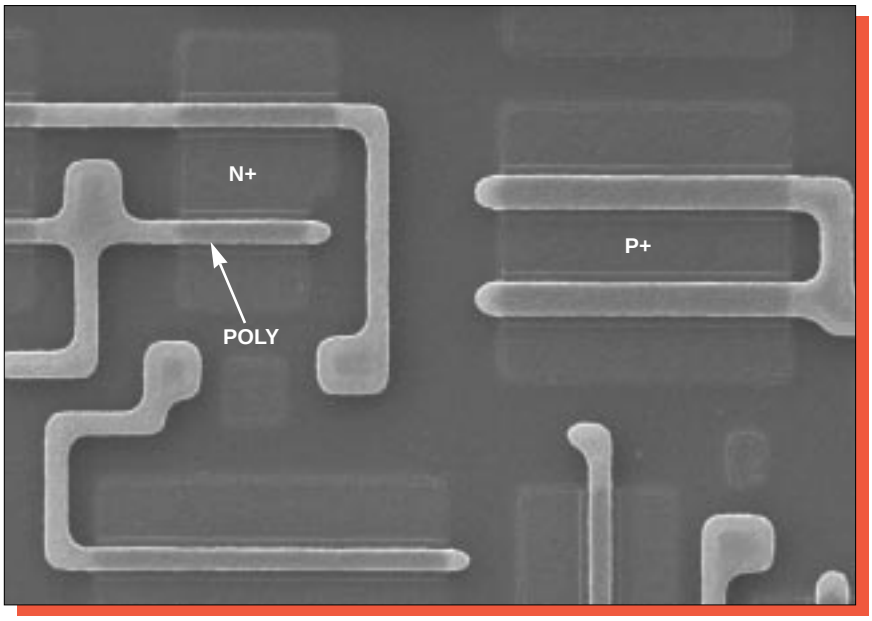


metal 1-to-N+

Figure 15. SEM section views of metal 1 contacts (silicon etch). Mag. 26,000x.

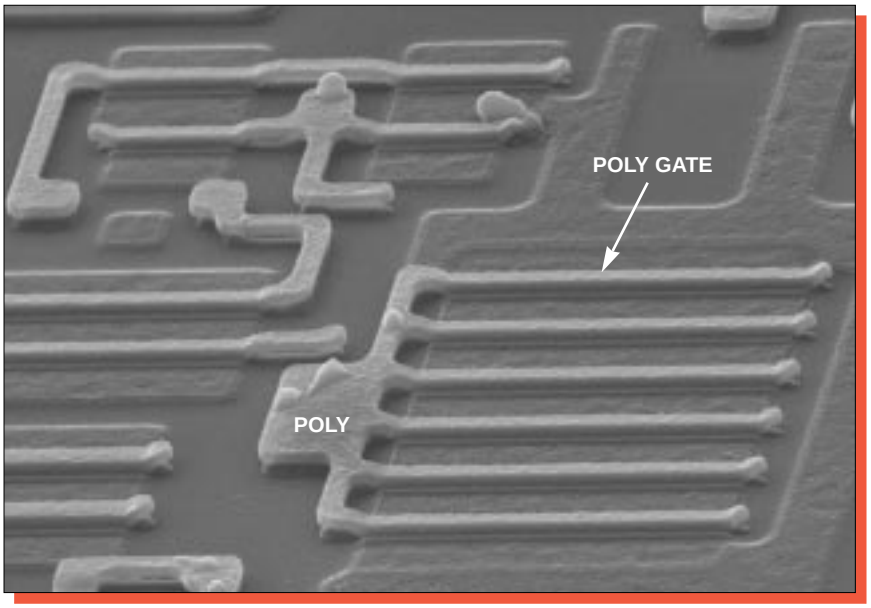


Mag. 3200x

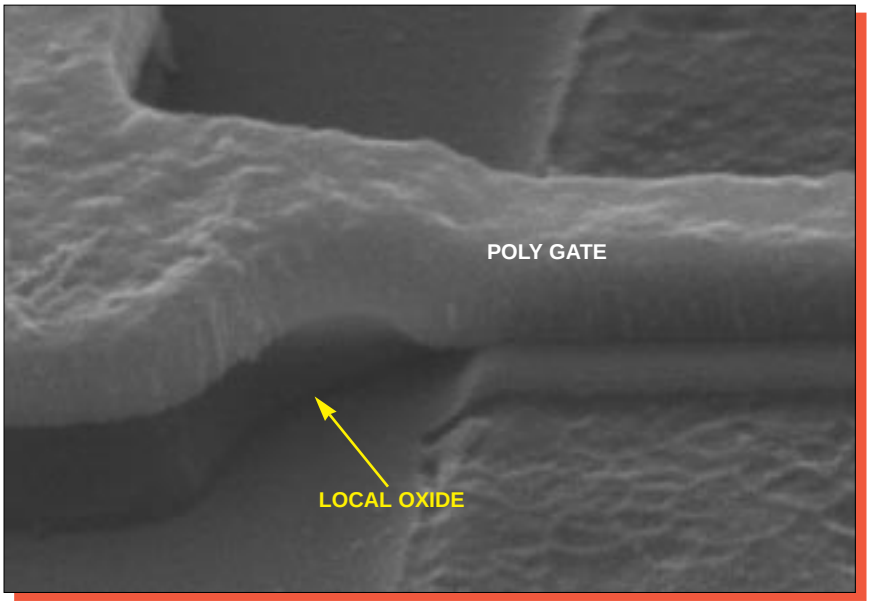


Mag. 6500x

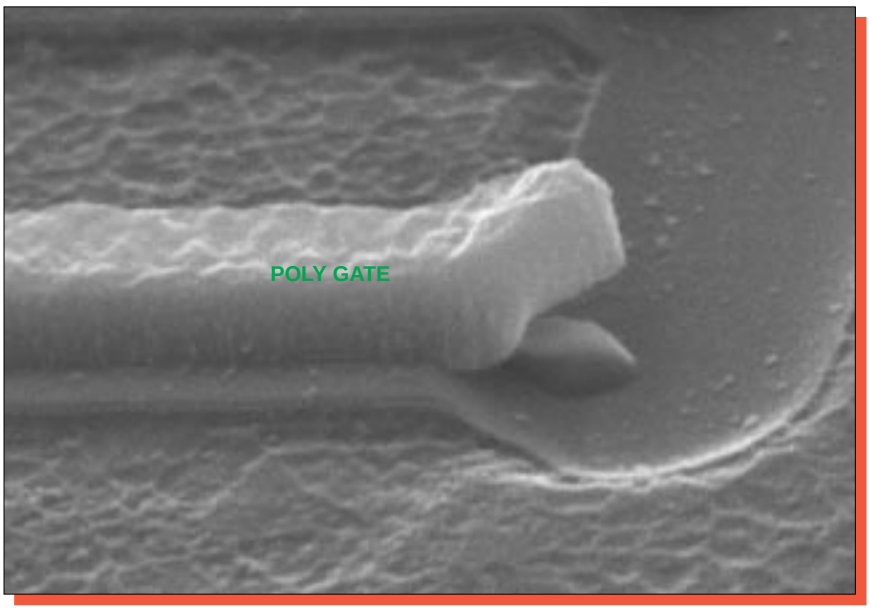
Figure 16. Topological SEM views of poly patterning. 0°.



Mag. 6500x

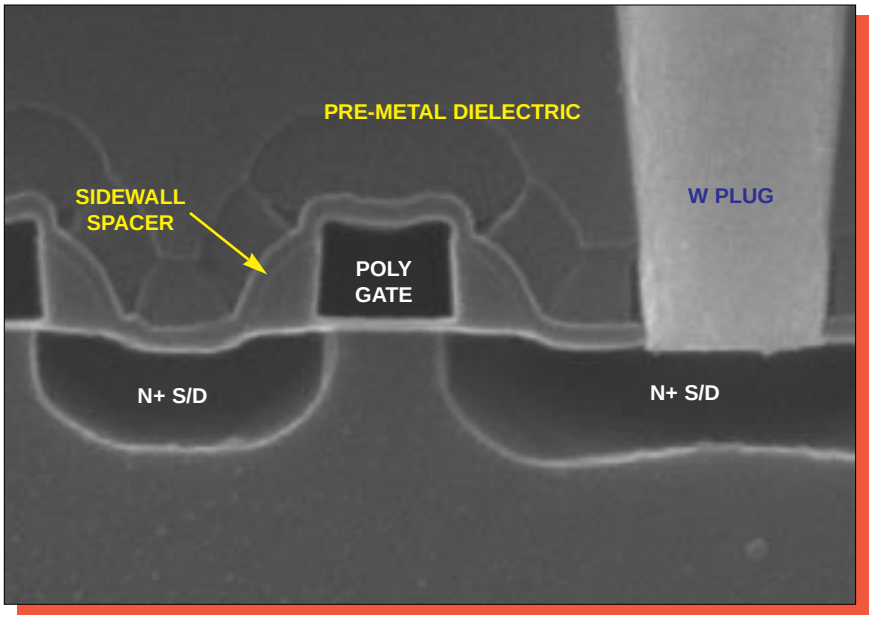


Mag. 52,000x

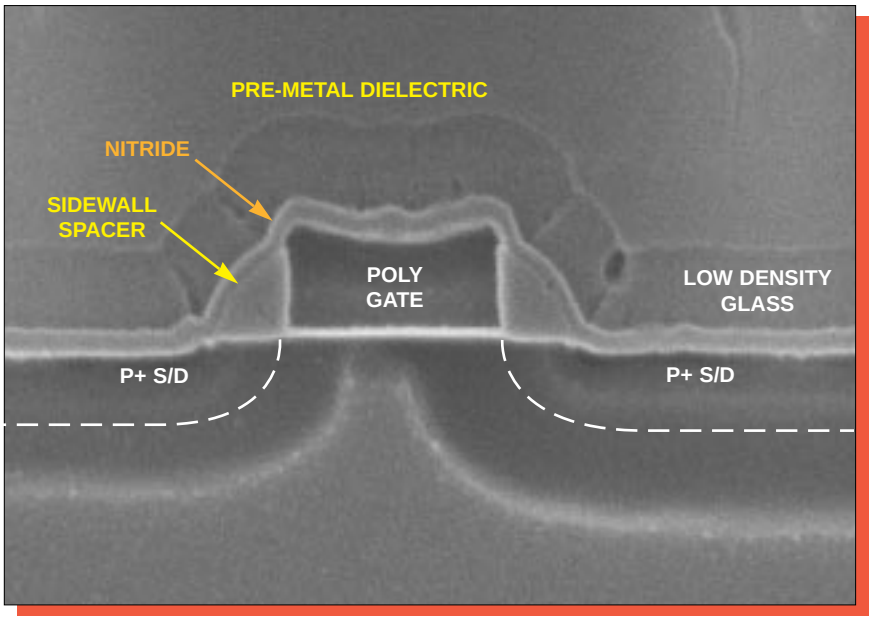


Mag. 52,000x

Figure 17. Perspective SEM views of poly coverage. 60°.



N-channel



P-channel

Figure 18. SEM section views of typical transistors. Mag. 52,000x.

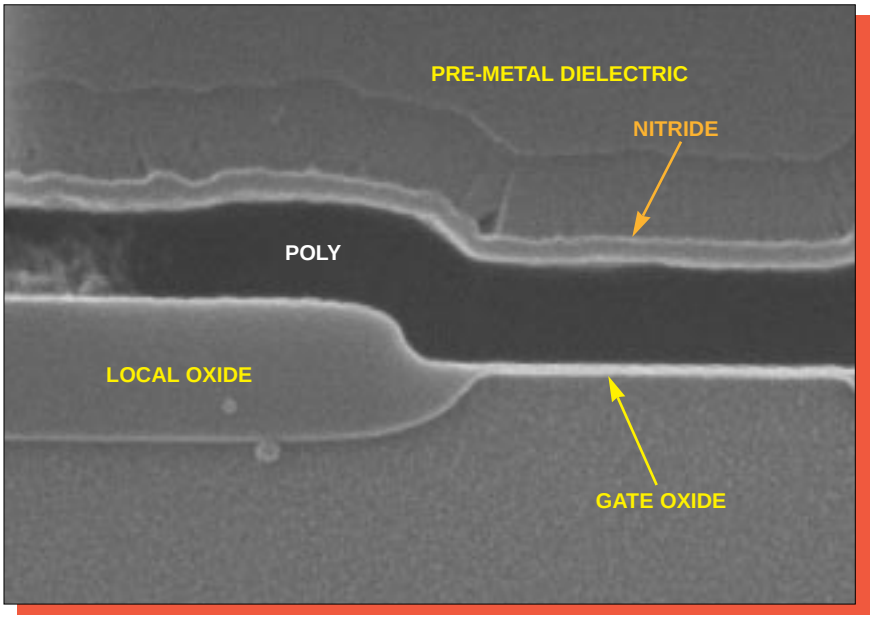


Figure 19. SEM section view of a typical local oxide birdsbeak. Mag. 52,000x.

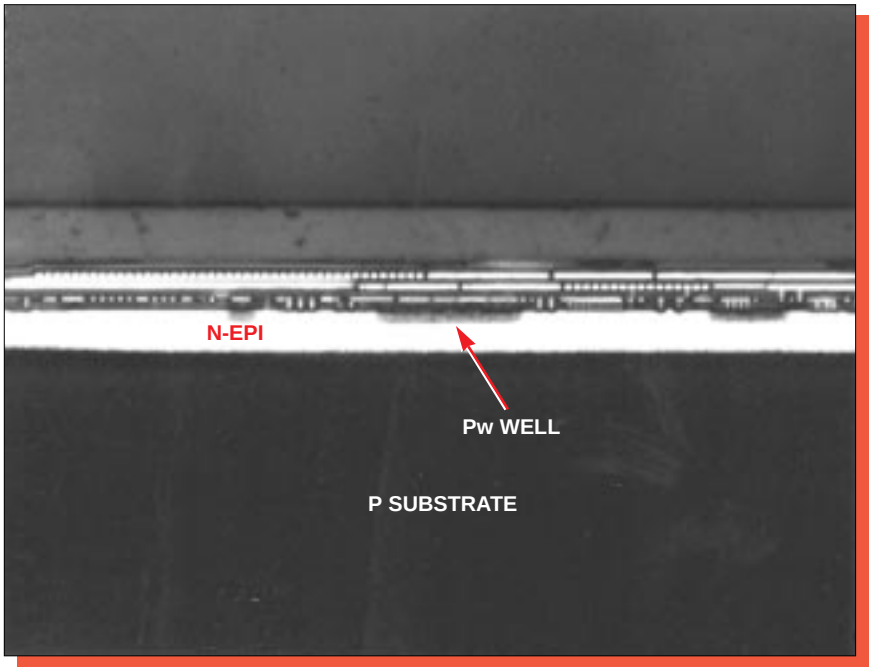
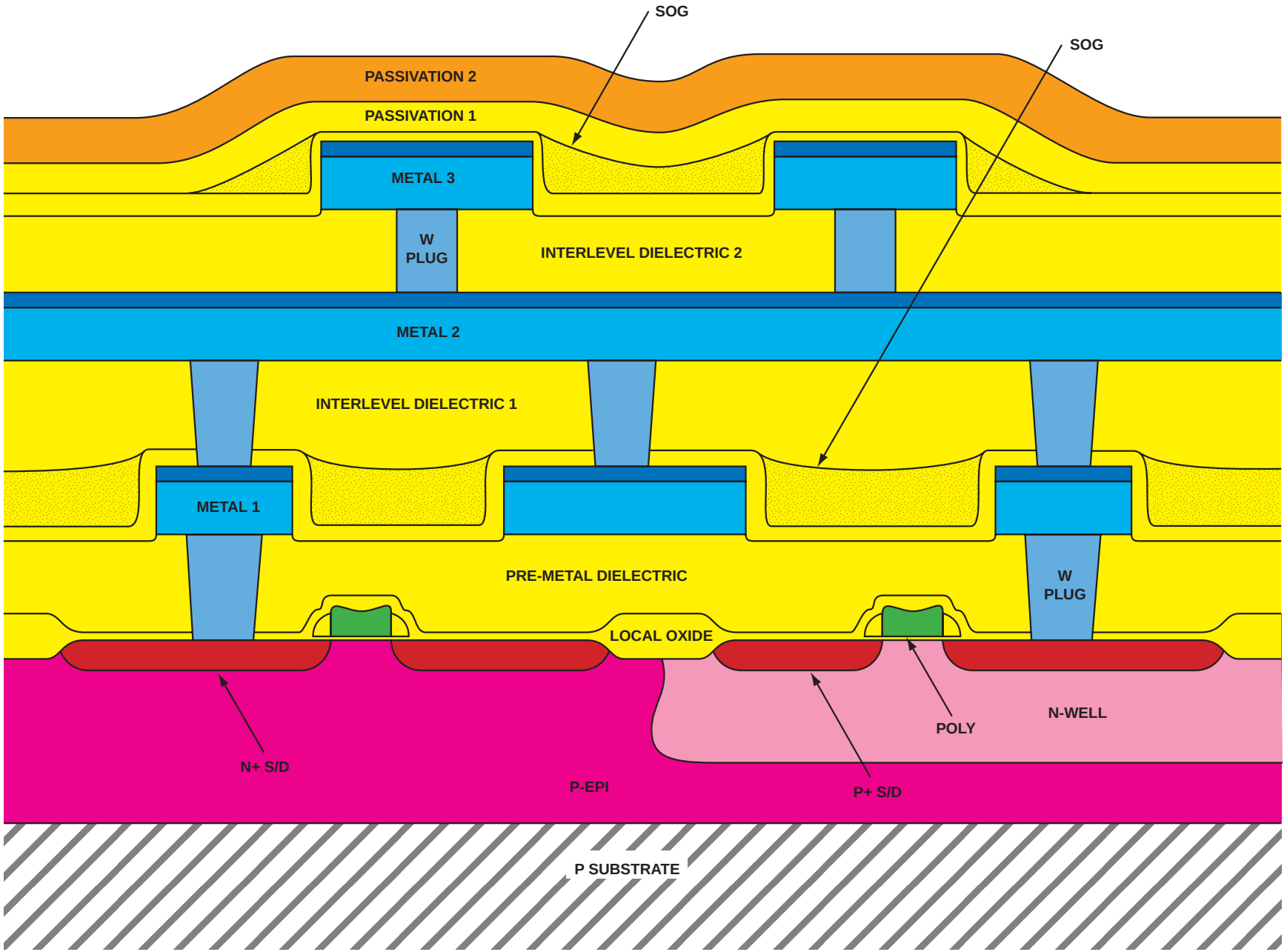


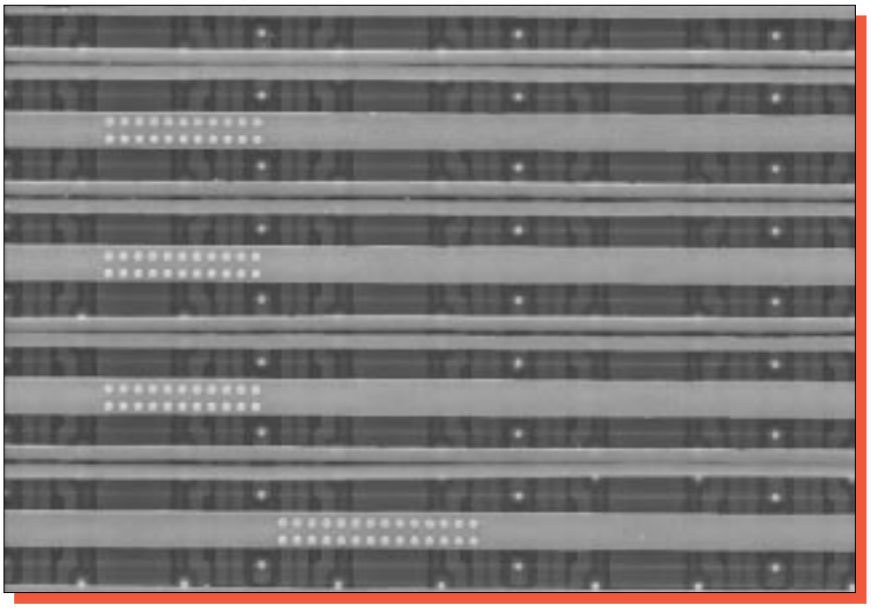
Figure 20. Section view illustrating the well structure. Mag. 800x.



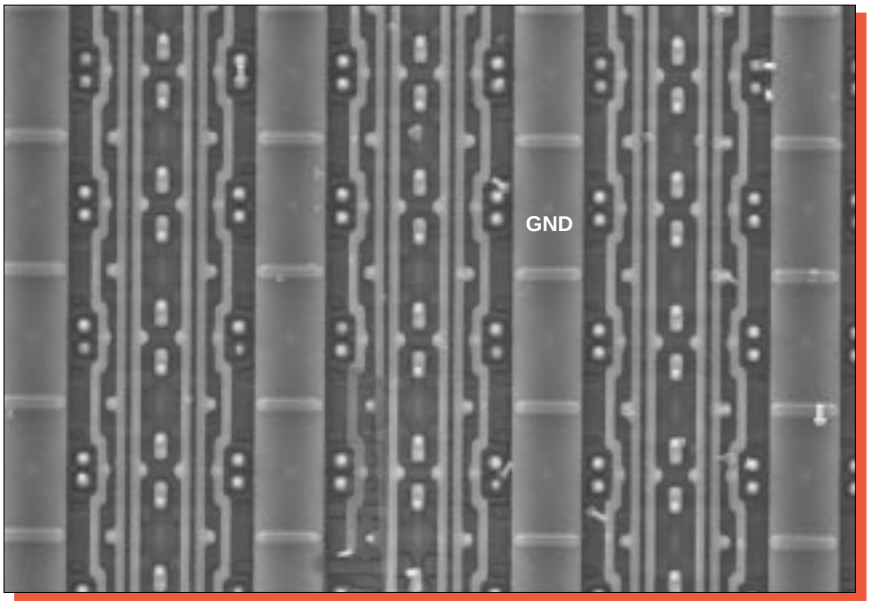
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

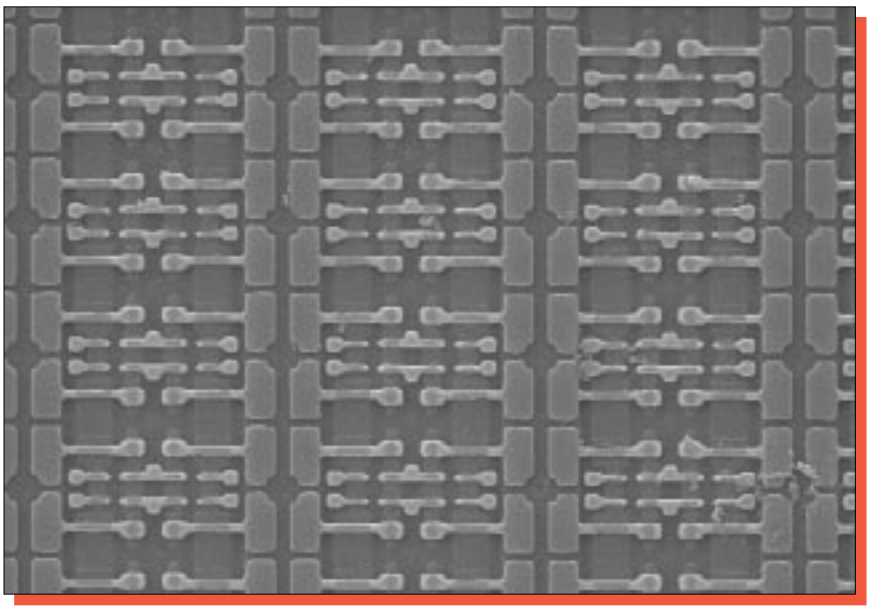
Figure 21. Color cross section drawing illustrating device structure.



metal 2

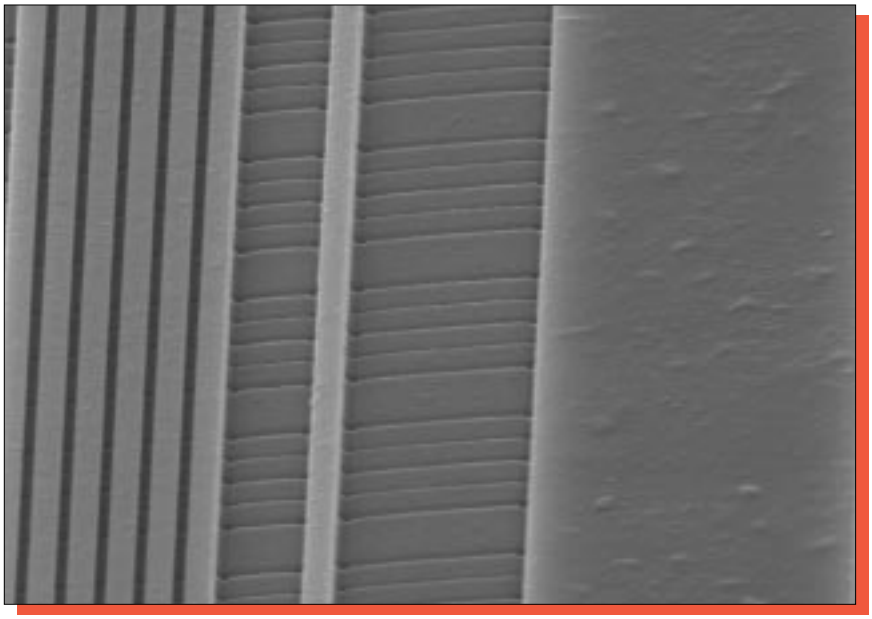


metal 1

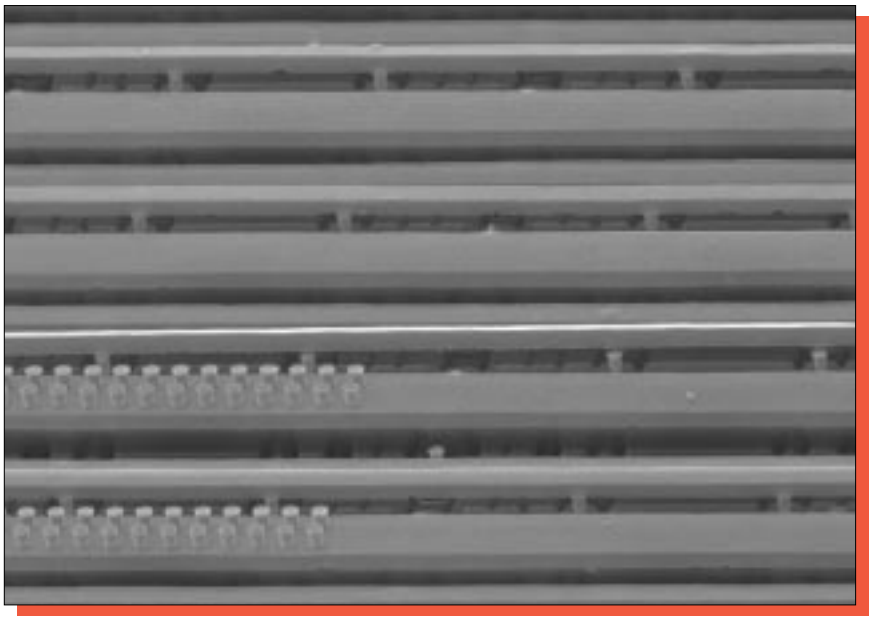


poly

Figure 22. SEM views of the EEPROM cell array (cell A). Mag. 1600x.

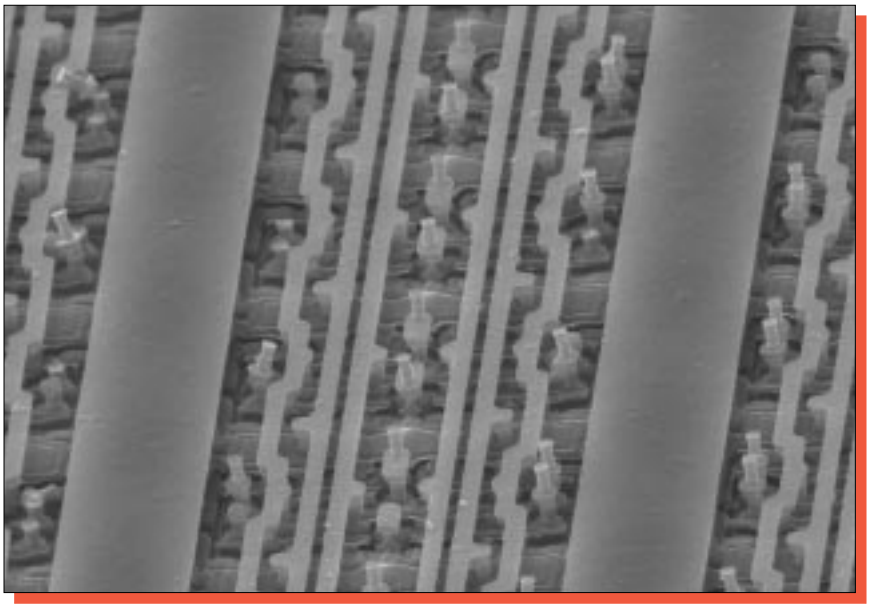


metal 3

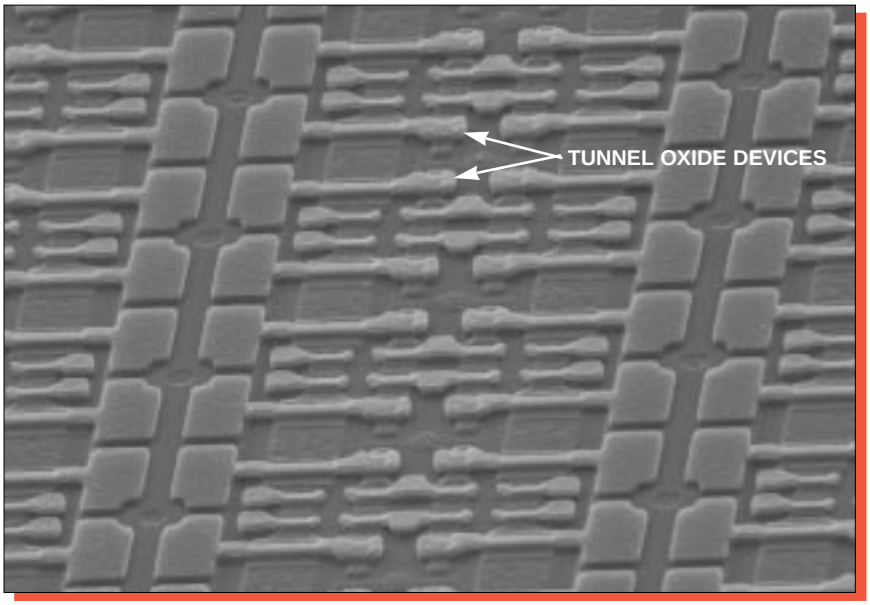


metal 2

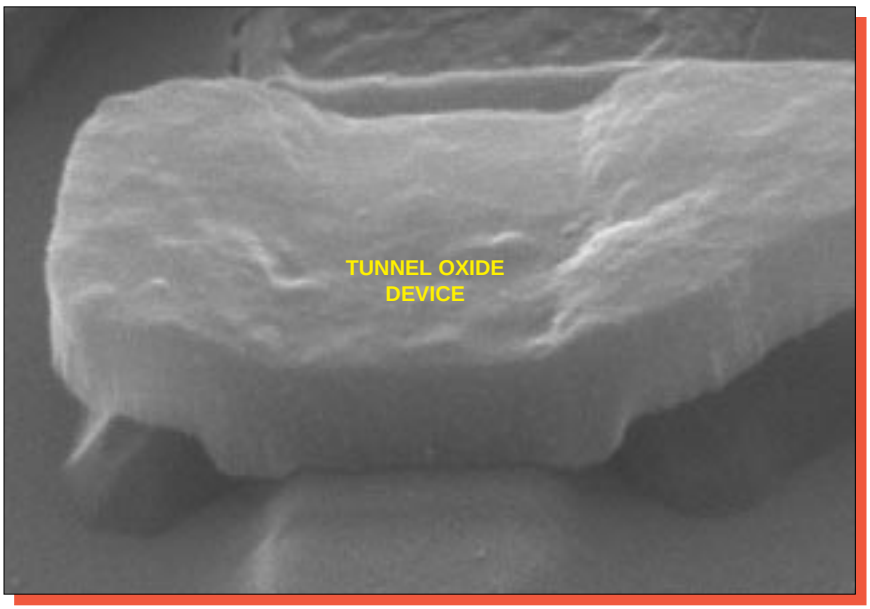
Figure 23. Perspective SEM views of the EEPROM cell (cell A). Mag. 3200x, 60°.



metal 1,
Mag. 3200x

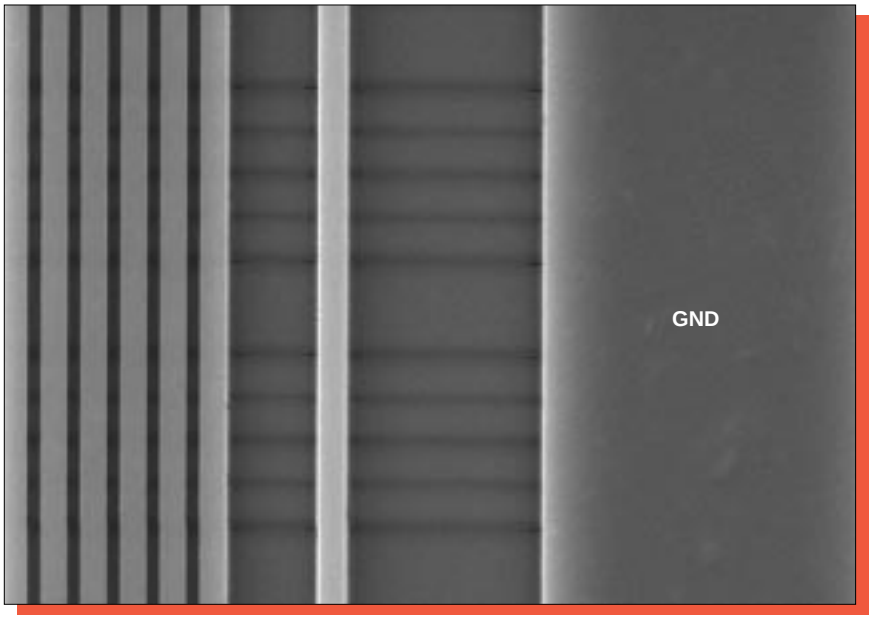


poly,
Mag. 3200x

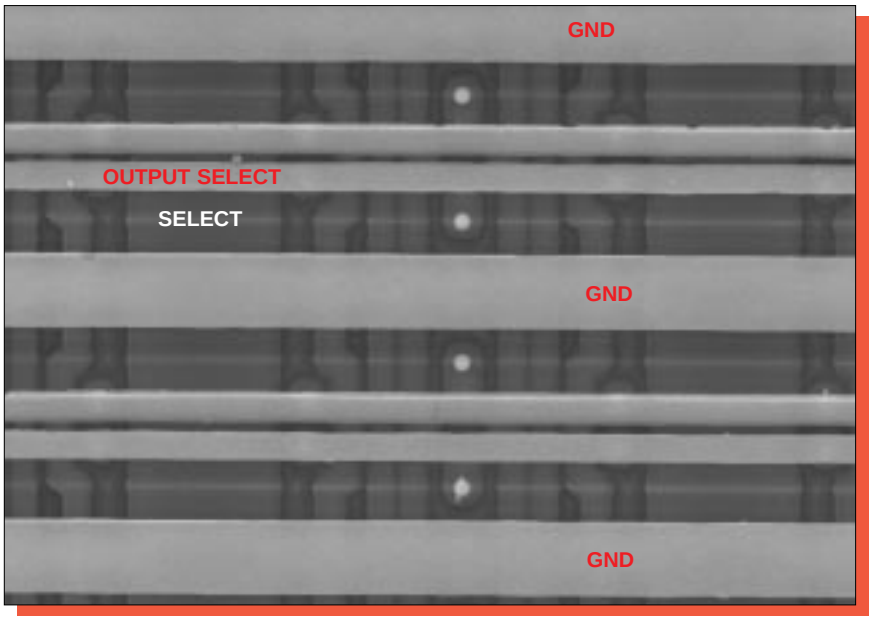


Mag. 52,000x

Figure 24. Perspective SEM views of the EEPROM cell array (cell A). 60°.



metal 3



metal 2

Figure 25. SEM views of the EEPROM cell array (cell A). Mag. 3200x, 0°.

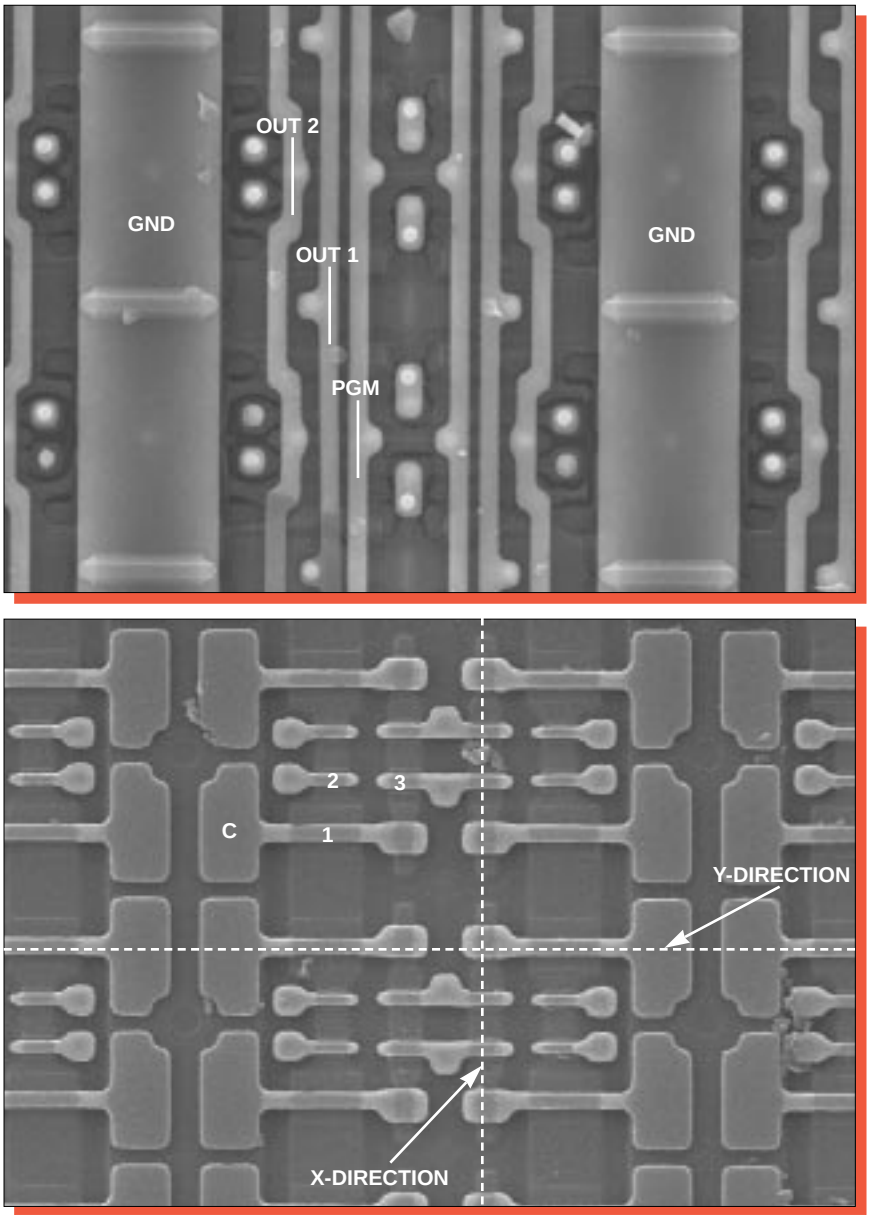
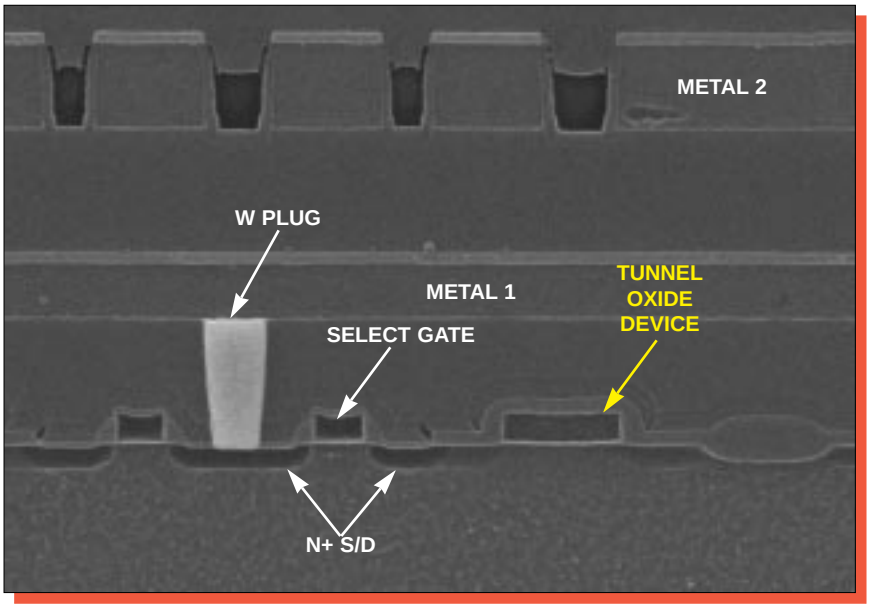
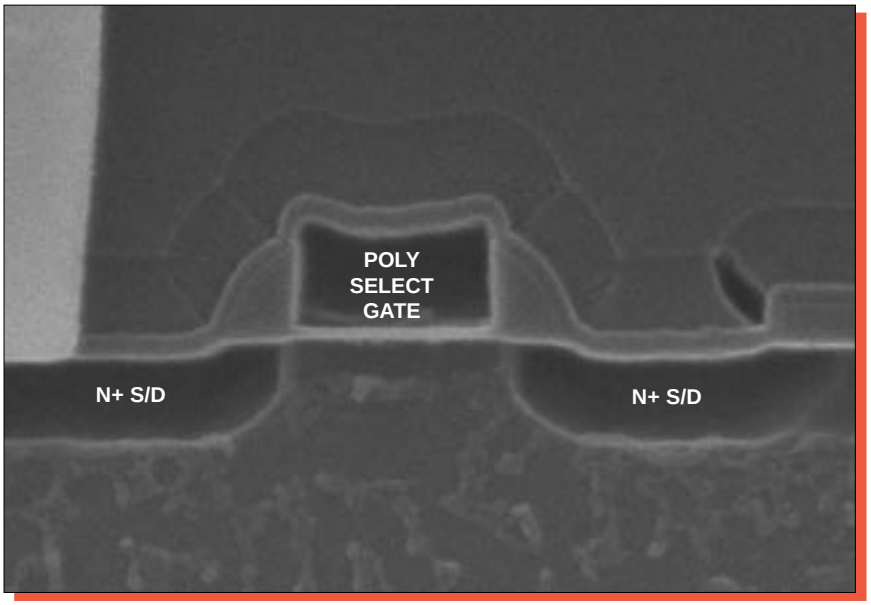


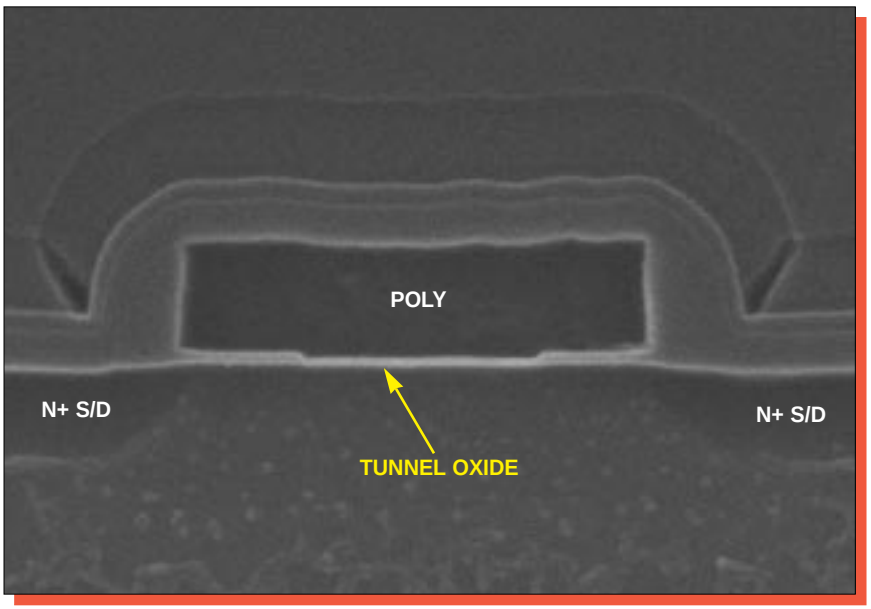
Figure 26. SEM section views and schematic of the EEPROM cell array (cell A).
Mag. 3200x, 0°.



Mag. 13,000x

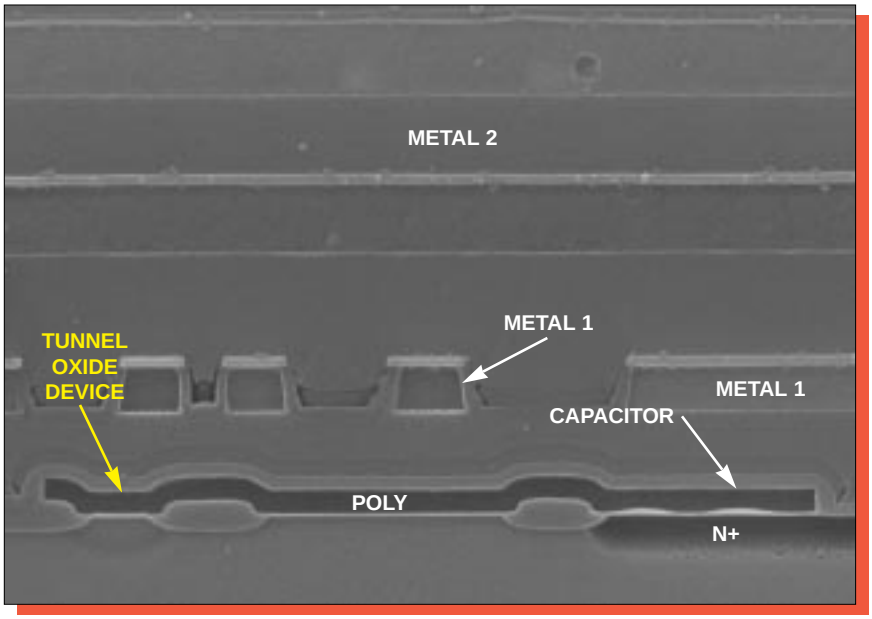


Mag. 52,000x

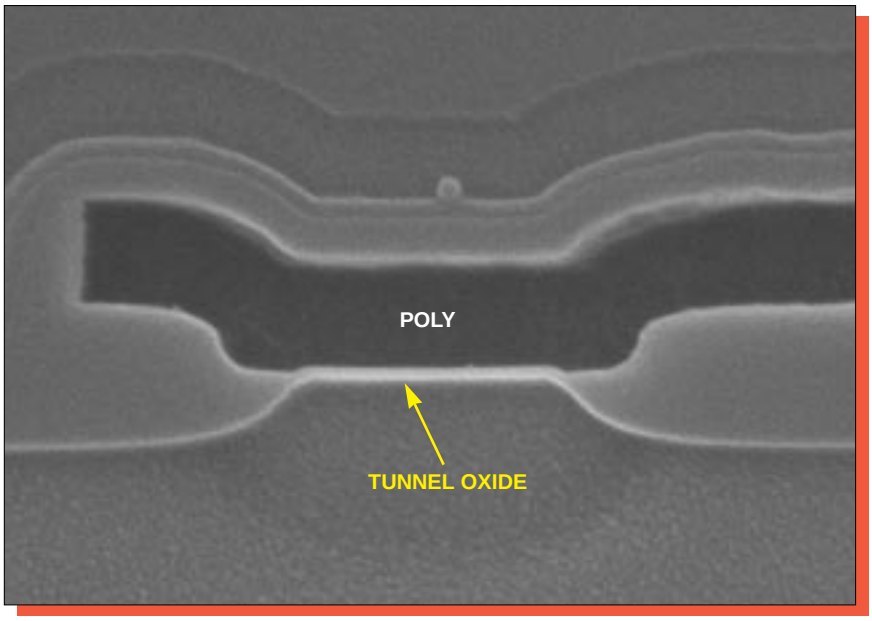


Mag. 52,000x

Figure 27. SEM section views of an EEPROM cell (cell A). X-direction.

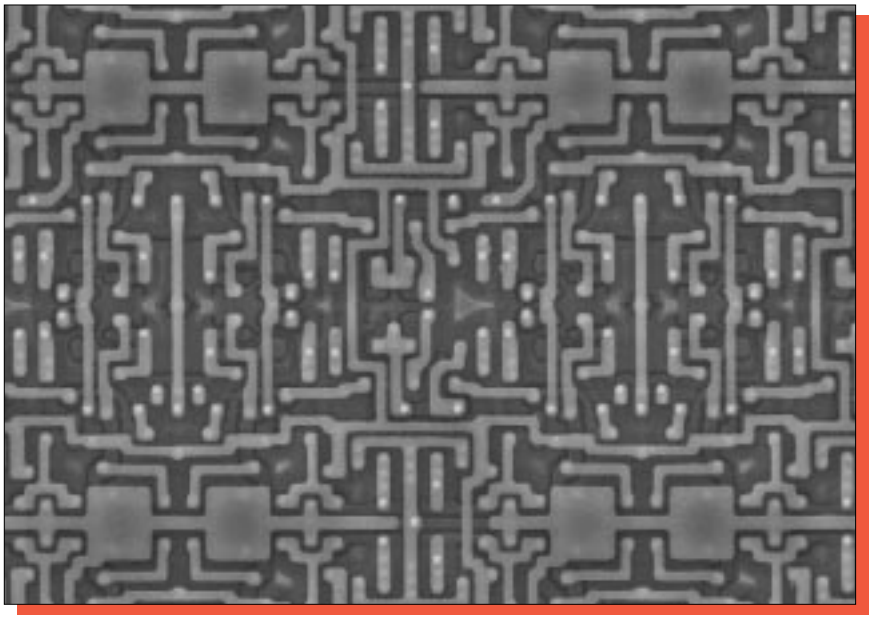


Mag. 11,000x

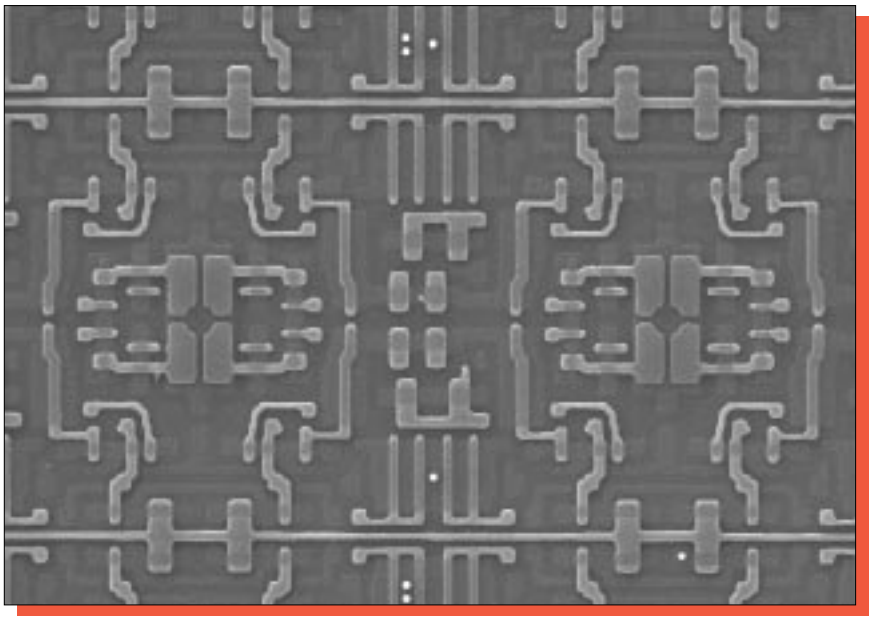


Mag. 52,000x

Figure 28. SEM section views of an EEPROM cell (cell A). Y-direction.

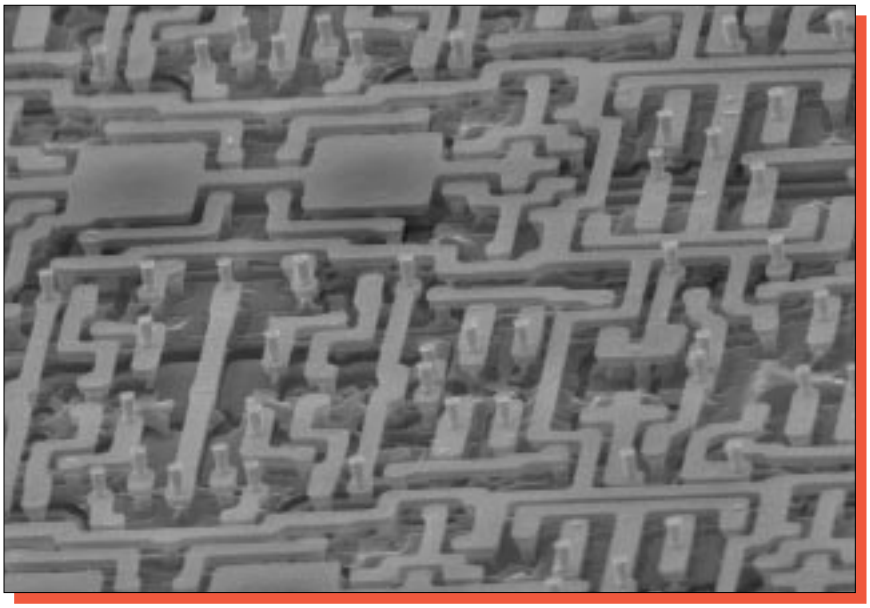


metal 1

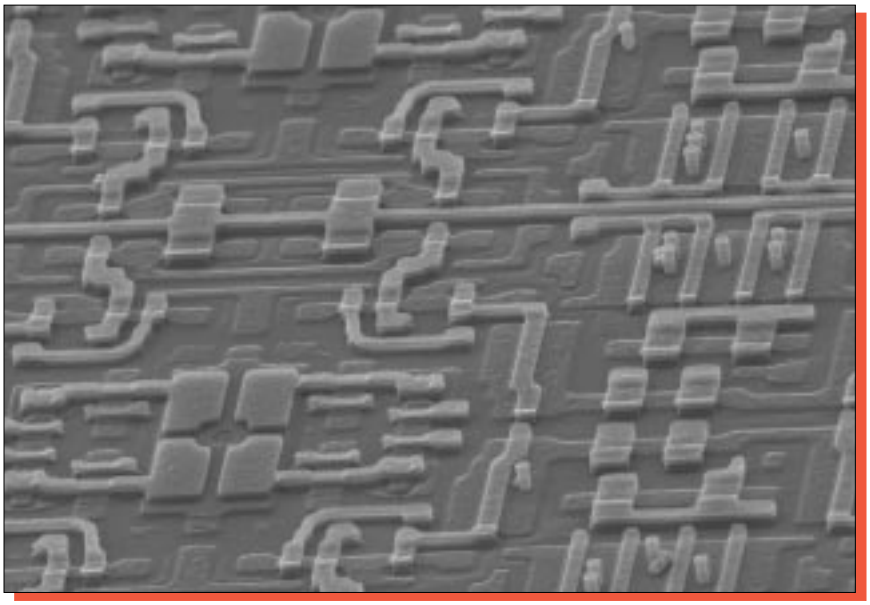


poly

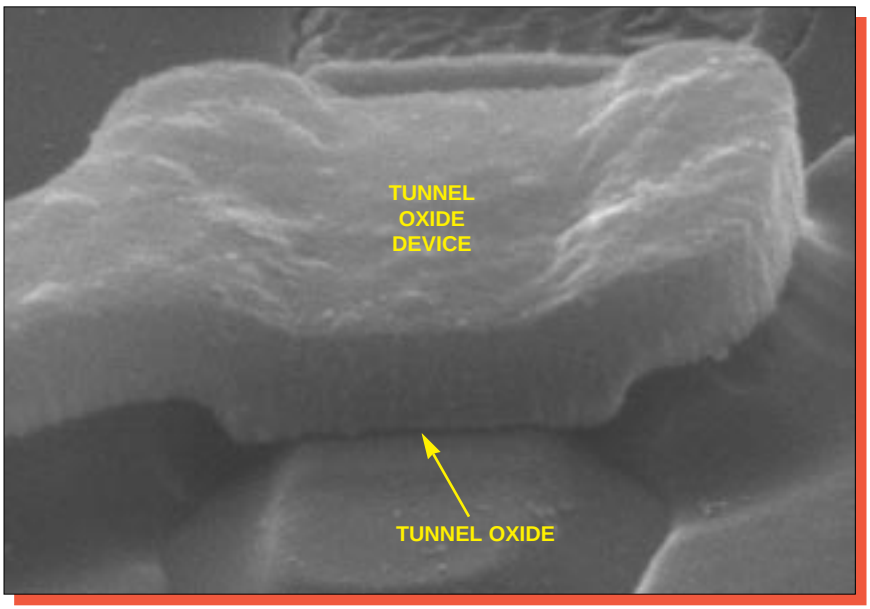
Figure 29. SEM views of the EEPROM cell (cell B). Mag. 1600x, 0°.



metal 1,
Mag. 3200x

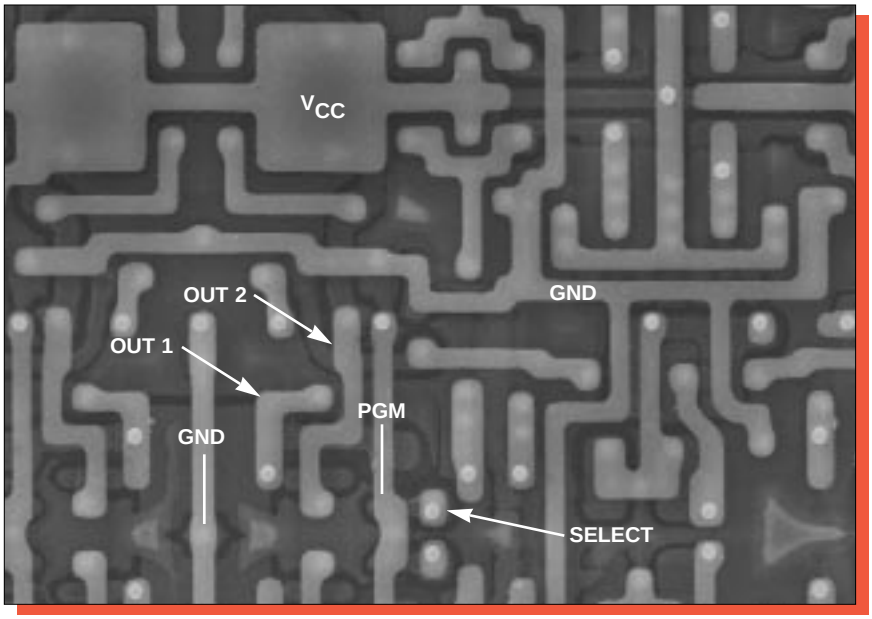


poly,
Mag. 3200x

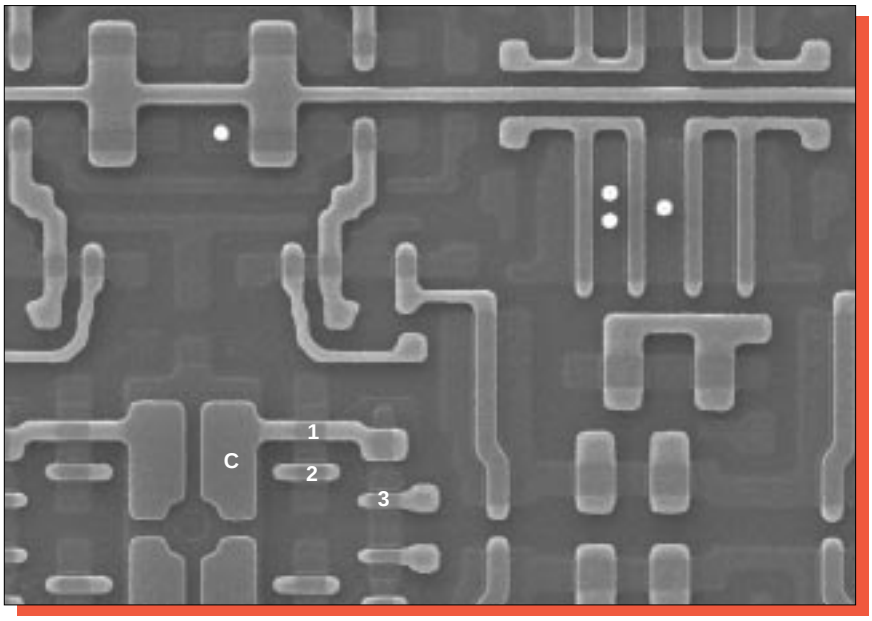


Mag. 52,000x

Figure 30. Perspective SEM views of the EEPROM cell array (cell B). 60°.



metal 1



poly

Figure 31. SEM views of the EEPROM cell (cell B). Mag. 3200x, 0°.