

## Construction Analysis

# Xilinx XC4036XL-1C FPGA

Report Number: SCA 9709-553



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## **INTRODUCTION**

This report describes a construction analysis of the Xilinx XC4036XL-1C FPGA. Only about half a die was available for this analysis. The device was date coded 9612.

## **MAJOR FINDINGS**

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Sub micron metal 1 pitch (0.95 micron).
- Tungsten (W) plugs were used for contacts and vias at all metal layers.
- Sub-micron gate lengths (0.35 micron N-channel and 0.3 micron P-channel).

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## TECHNOLOGY DESCRIPTION

### Die Process:

- Devices were fabricated using a selective oxidation, N-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of a layer of nitride over a layer of silicon-dioxide.
- Metal interconnect used three levels of metal. All consisted of aluminum with titanium-nitride caps and barriers, with a titanium (Ti) adhesion layer beneath the barrier. Tungsten (W) plugs were used at all levels for contacts and vias.
- Both interlevel dielectric 2 (between metals 3 and 2) and interlevel dielectric 1 (between metals 2 and 1) consisted of two layers of silicon-dioxide with a planarizing glass (probably SOG) in between.
- Pre-metal dielectric consisted of a layer of reflow glass (probably BPSG) over various densified oxides. The glass was reflowed prior to contact cuts only.
- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.
- Standard implanted N<sup>+</sup> and P<sup>+</sup> diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.
- Local oxide (LOCOS) isolation. No step was present at the edge of the well.
- Programming is achieved through a modified 5T CMOS SRAM cell. Metal 3 was used to form the word lines (via metal 2 and metal 1). Metal 2 was used to form the bit lines and distribute V<sub>cc</sub> and GND (via metal 1). Metal 1 was used to provide cell interconnect. Poly was used to form all gates.
- Redundancy fuses were not present.

## ANALYSIS RESULTS

### Die Process:

Figures 1 - 25

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Sub micron metal 1 pitch (0.95 micron).
- Tungsten (W) plugs were used for the contacts and vias.
- Sub-micron gate lengths (0.35 micron N-channel and 0.3 micron P-channel).

### **General Items:**

- Fabrication process: Devices were fabricated using a selective oxidation, N-well CMOS process in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. The die portion used for the analysis had some mechanical damage at the corners but the middle of the die had very little damage.
- Die coat: No die coat was present.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS (continued)**

- Final passivation consisted of a layer of nitride over a layer of silicon-dioxide. Integrity test was not performed because the die was damaged.
- Metallization: Three levels of metal. All consisted of aluminum with titanium-nitride caps and barriers with a titanium (Ti) layer beneath the barrier for adhesion purposes. Tungsten (W) plugs were used for all contacts and vias.
- Metal patterning: All metal layers were patterned by a dry etch of normal quality.
- Metal defects: No voiding, notching, or neckdown was noted in any of the metal layers. No silicon nodules were noted following the removal of any metal layer.
- Metal step coverage: Virtually no metal thinning was noted due to the use of tungsten (W) plugs for the contacts and vias, and general good planarization.
- Interlevel dielectric 2 (between metals 3 and 2) consisted of two layers of silicon-dioxide with a planarizing glass (probably SOG) layer in between. Interlevel dielectric 1 (between metals 2 and 1) also consisted of two layers of silicon-dioxide with a planarizing glass (probably SOG) layer in between. It is believed that CMP was used under metals 3 and 2. No problems were found in any of these layers.
- Pre-metal dielectric: A layer of reflow glass (probably BPSG) over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.

## **ANALYSIS RESULTS (continued)**

- Contact defects: Via and contact cuts were defined by step process. No over-etching of the contacts and vias was noted.
- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by dry-etch of normal quality.
- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.
- Local oxide (LOCOS) isolation was used. No step was present at the well boundary and no other firm evidence of a twin-well process was found.
- Programming is achieved through a modified 5T CMOS SRAM cell. Metal 3 was used to form the word lines (via metal 2 and metal 1). Metal 2 was used to form the bit lines and distribute Vcc and GND (via metal 1). Metal 1 was used to provide cell interconnect. Poly was used to form all gates.
- Redundancy fuses were not present on the die.

## **PROCEDURE**

The devices were subjected to the following analysis procedures:

SEM of passivation  
Passivation removal  
SEM inspection of metal 3  
Metal 3 removal and inspect barrier  
Delayer to metal 2 and inspect  
Metal 2 removal and inspect barrier  
Delayer to metal 1 and inspect  
Metal 1 removal and inspect barrier  
Delayer to silicon and inspect poly/die surface  
Die sectioning (90° for SEM)\*  
Die material analysis  
Measure horizontal dimensions  
Measure vertical dimensions

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

Die surface integrity:

Toolmarks (absence)	*
Particles (absence)	*
Contamination (absence)	*
Process defects (absence)	G
General workmanship	N
Passivation integrity	*
Metal definition	N
Metal integrity	N
Metal registration	N
Contact coverage	N
Contact registration	N

**DIE MATERIAL ANALYSIS**

Overlay passivation:	Consisted of a layer of nitride over a layer of silicon-dioxide.
Metallization 3:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier and titanium (Ti) adhesion layer.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier and titanium (Ti) adhesion layer.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier and titanium (Ti) adhesion layer.
Plugs:	Tungsten (W).

*\*The portion of the die that was available for the analysis was damaged so no meaningful analysis could not be performed.*

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*



## VERTICAL DIMENSIONS

Die thickness: 0.38 mm (15 mils)

### Layers:

Passivation 2:	0.55 micron
Passivation 1:	0.4 micron
Metal 3 - cap:	0.05 micron (approximate)
- aluminum:	0.85 micron
- barrier:	0.05 micron (approximate)
Interlevel dielectric 2 - glass 2:	0.8 micron
- glass 1:	0.1 micron
Metal 2 - cap:	0.05 micron (approximate)
- aluminum:	0.55 micron
- barrier:	0.05 micron (approximate)
Interlevel dielectric 1- glass 2:	0.8 micron
- glass 1:	0.1 micron (approximate)
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.08 micron (approximate)
Pre-metal dielectric:	0.08 - 0.45 micron
Oxide on poly:	0.15 micron
Poly:	0.25 micron
Local oxide:	0.35 micron
N+ S/D:	0.2 micron
P + S/D:	0.25 micron
N-well:	2.5 microns (approximate)

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DIE LAYOUT AND IDENTIFICATION

Figure 1

PHYSICAL DIE STRUCTURES

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COLOR PROCESS DRAWING

Figure 19

SRAM CELL STRUCTURE

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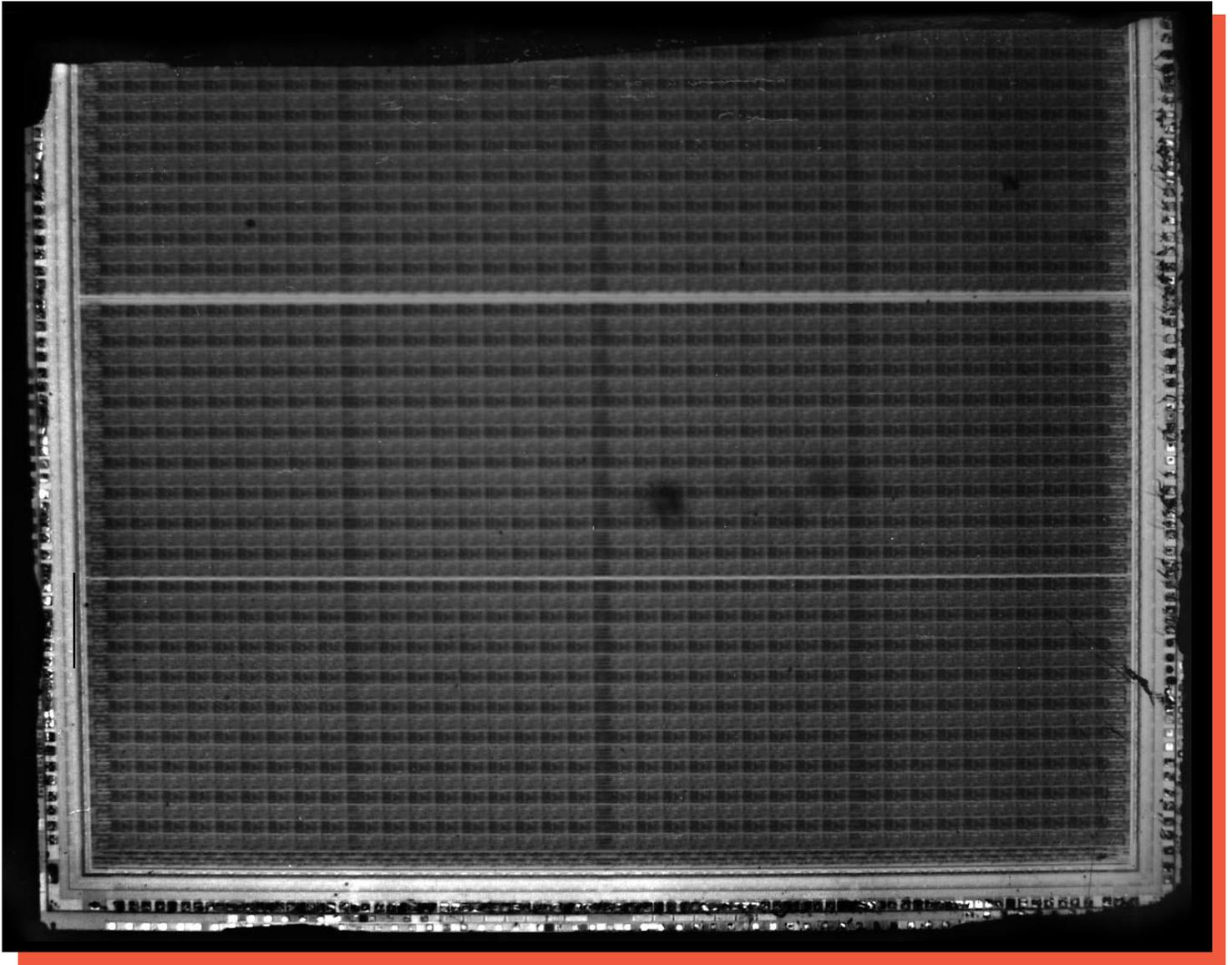
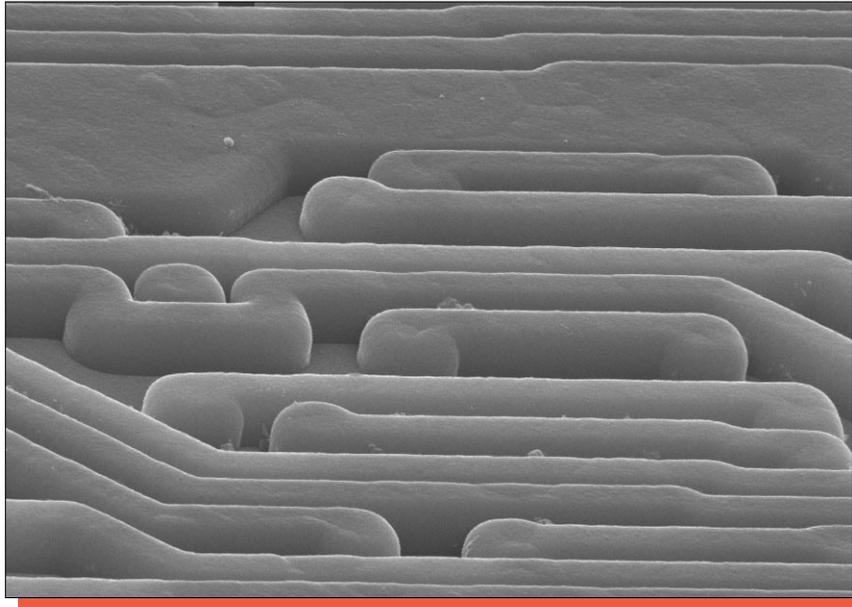
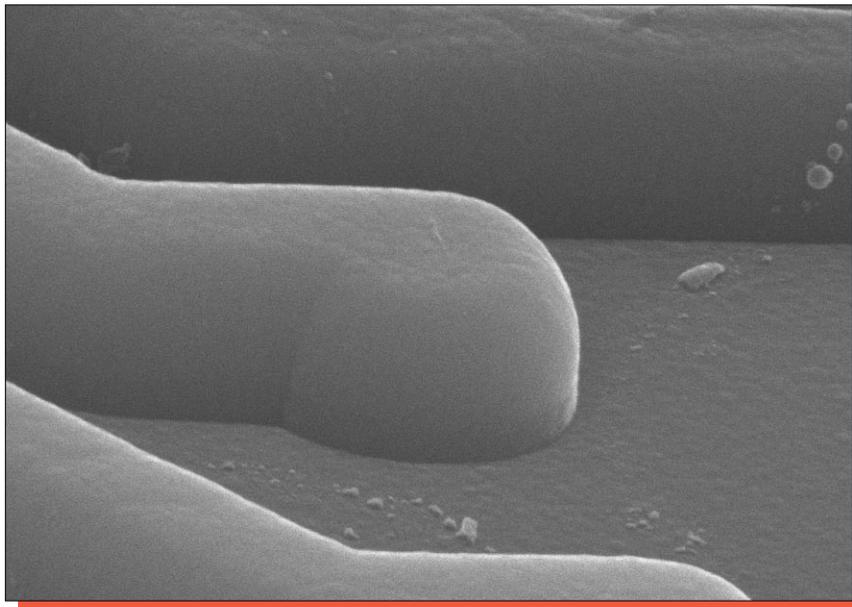


Figure 1. Die photograph of the Xilinx XC4036XL-1C. Mag. 14x.

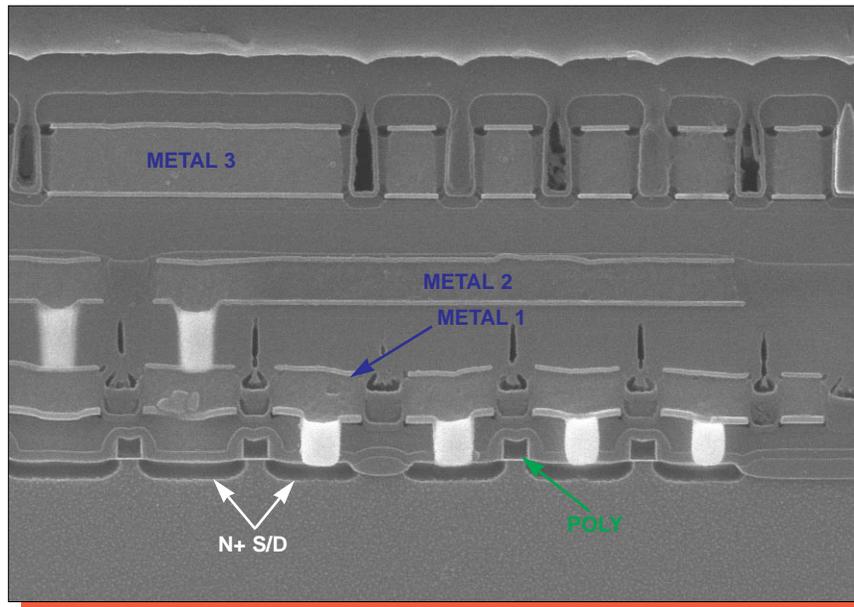


Mag. 5000x

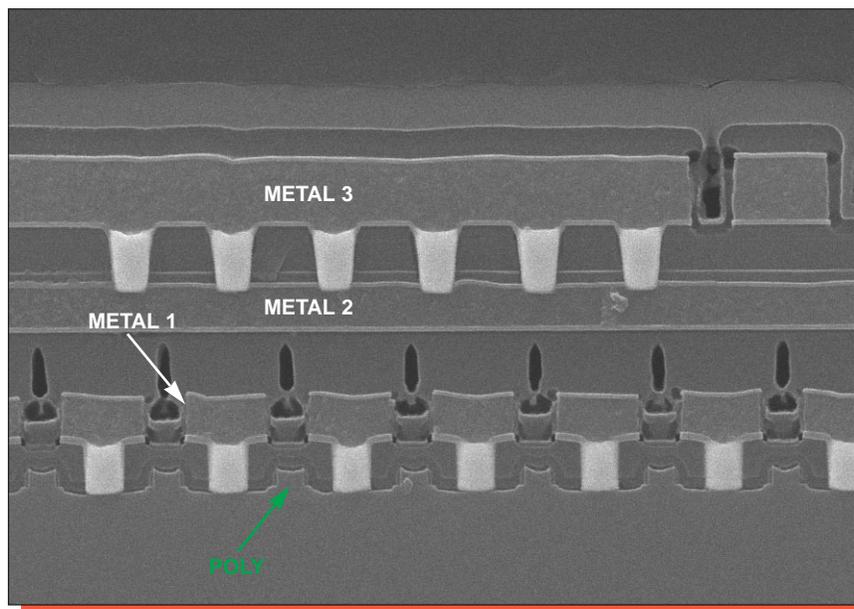


Mag. 16,000x

Figure 2. Perspective SEM views of the overlay passivation coverage. 60°.

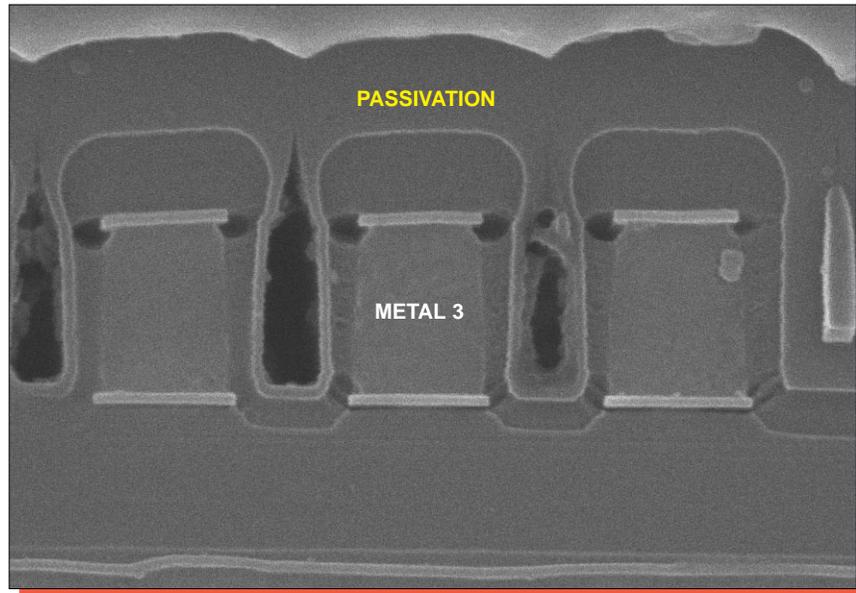


silicon etch

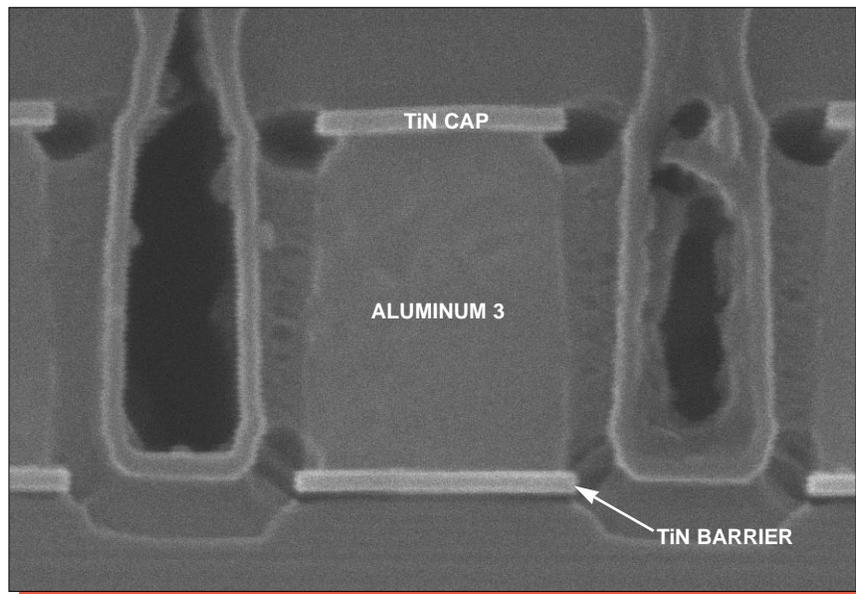


glass etch

Figure 3. SEM section views illustrating general device structure. Mag. 10,000x.

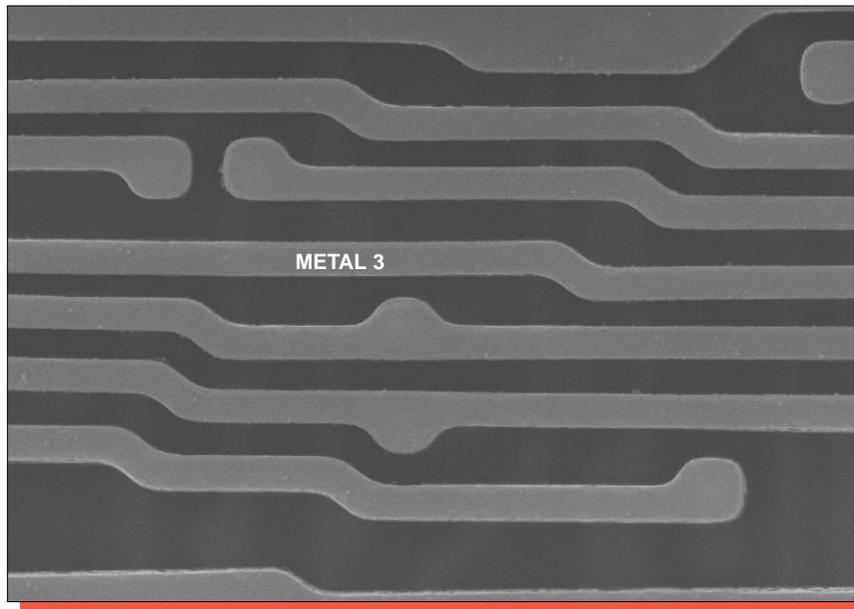


Mag. 26,000x

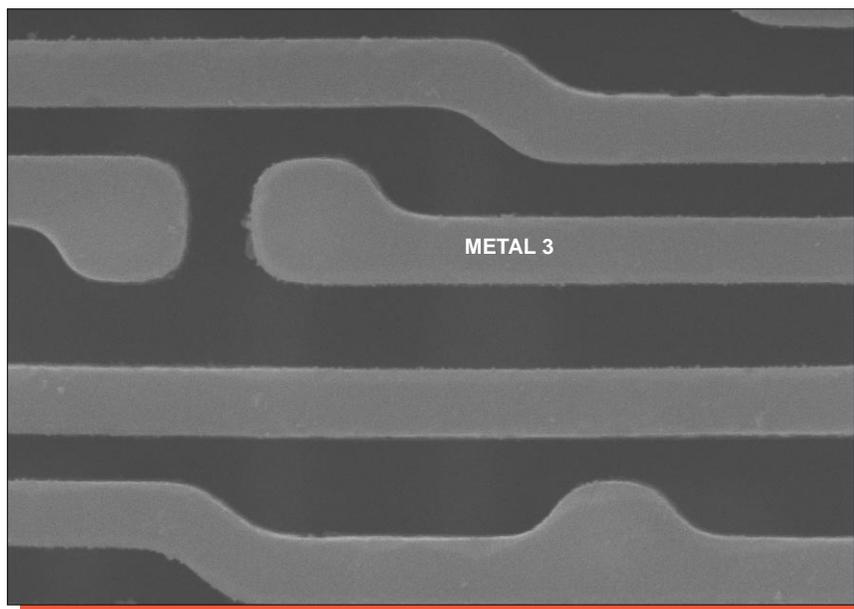


Mag. 52,000x

Figure 4. SEM section views of metal 3 profiles.

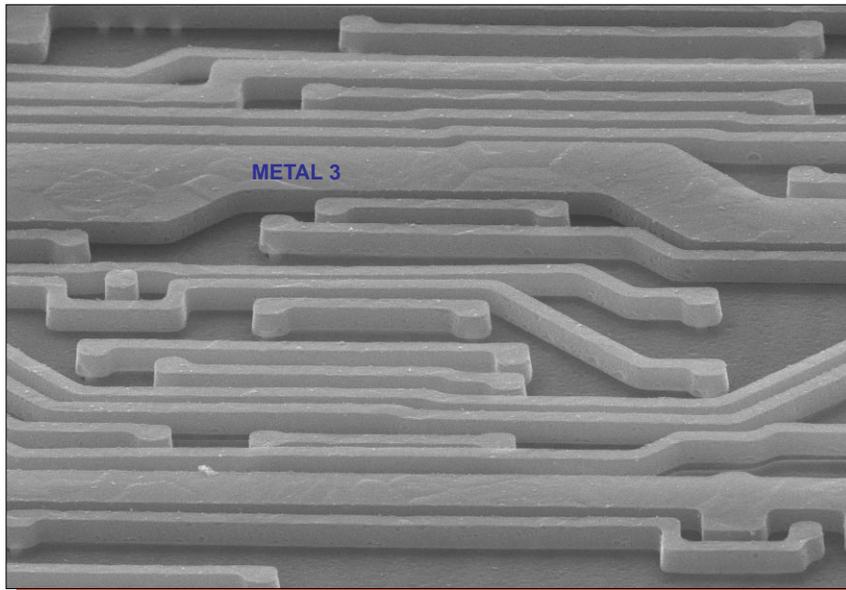


Mag. 6500x

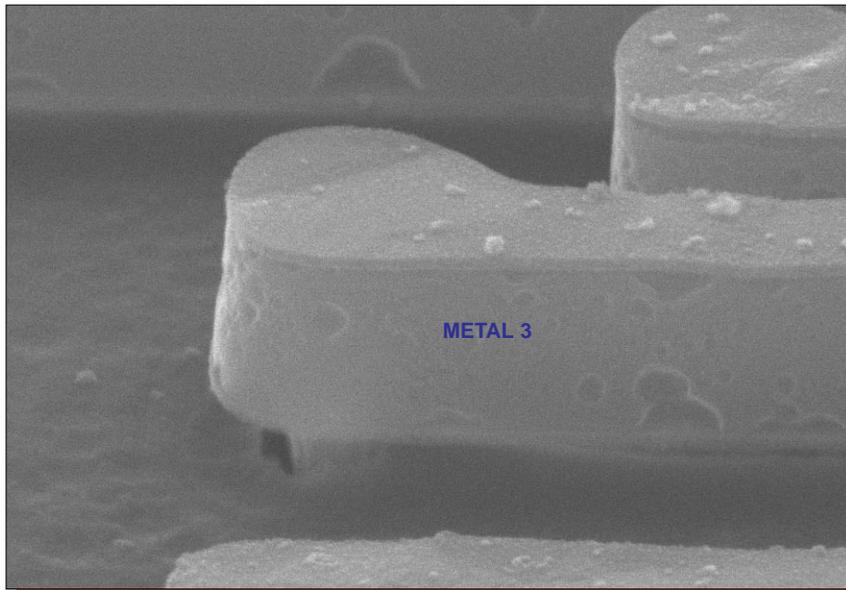


Mag. 13,000x

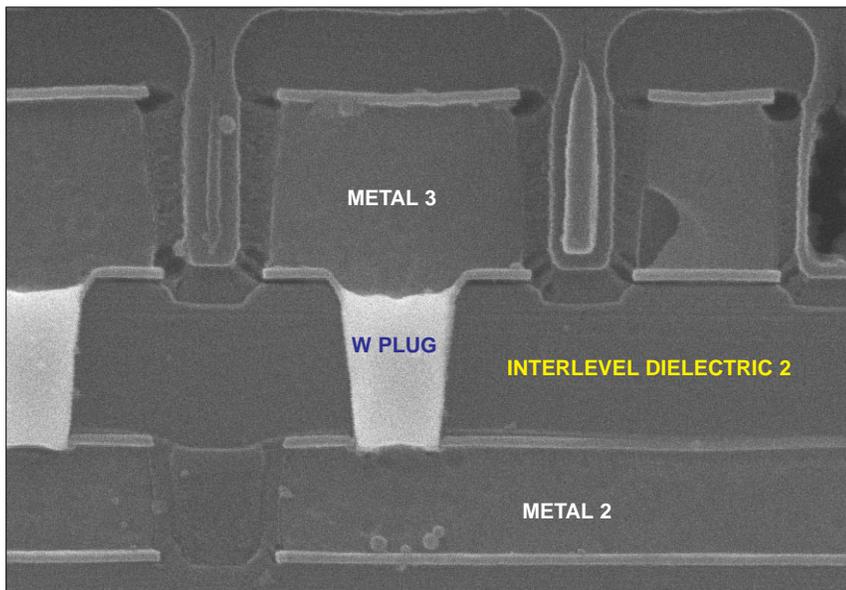
Figure 5. Topological SEM views of metal 3 patterning. 0°.



Mag. 3200x

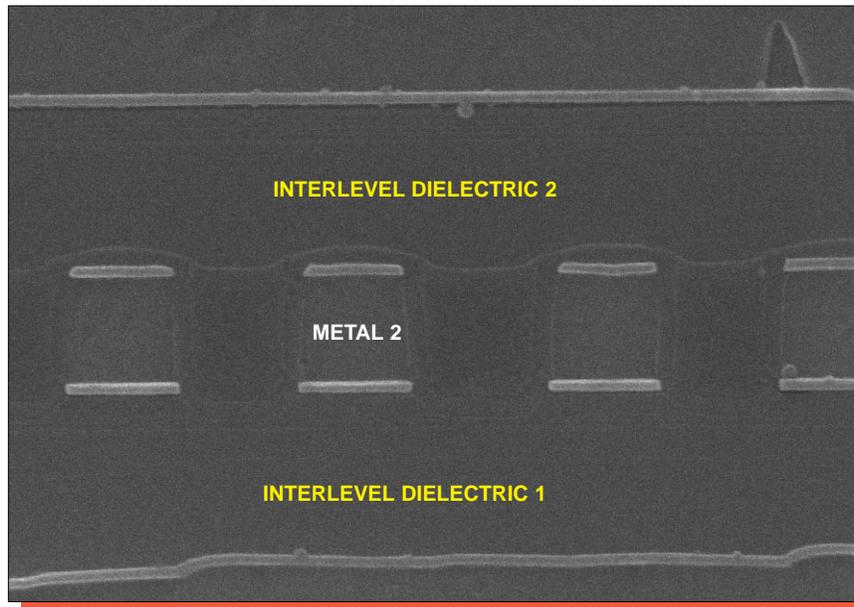


Mag. 26,000x

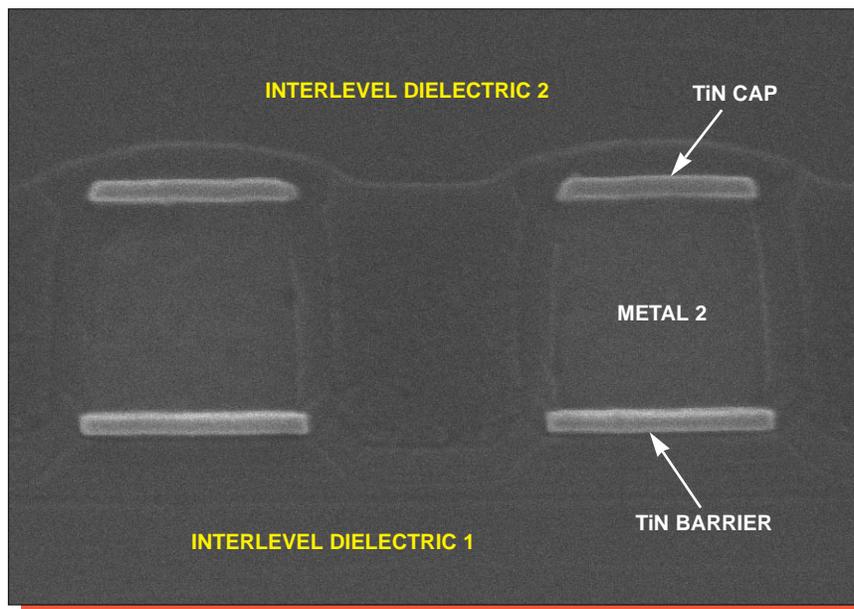


Mag. 26,000x

Figure 6. SEM views of metal 3 step coverage and metal 3-to-metal 2 via.

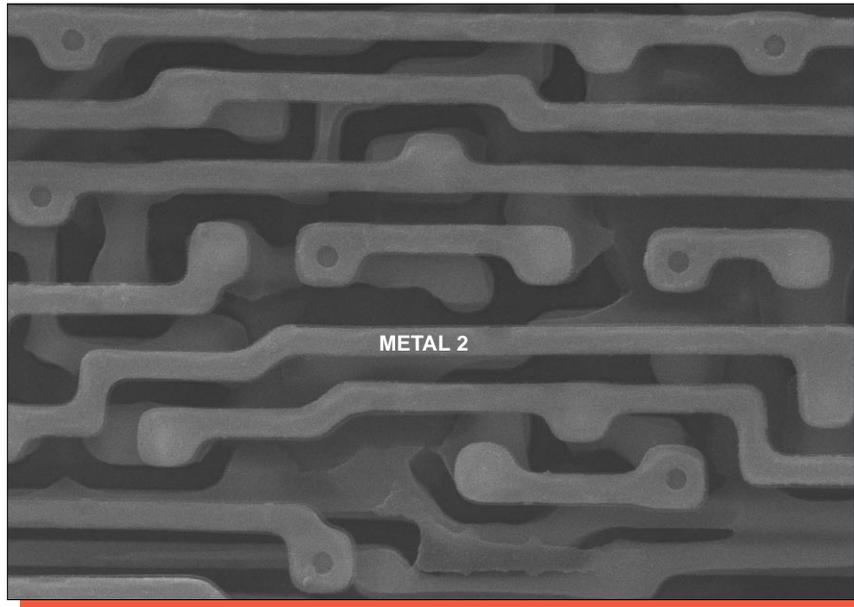


Mag. 26,000x

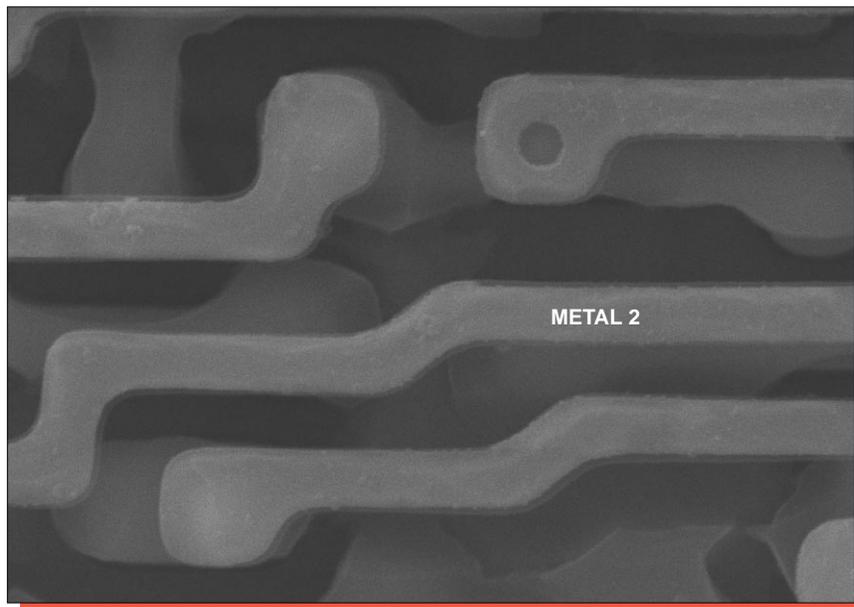


Mag. 52,000x

Figure 7. SEM section views of metal 2 line profiles.

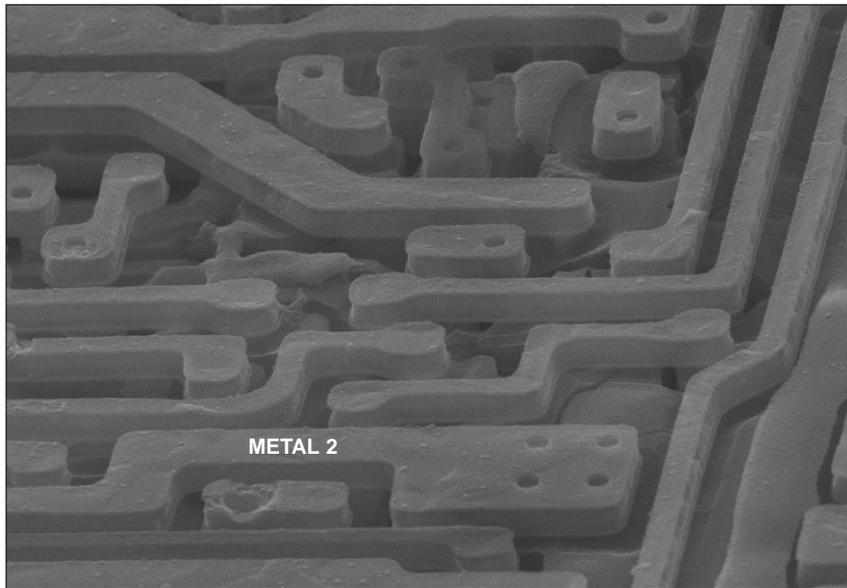


Mag. 6500x

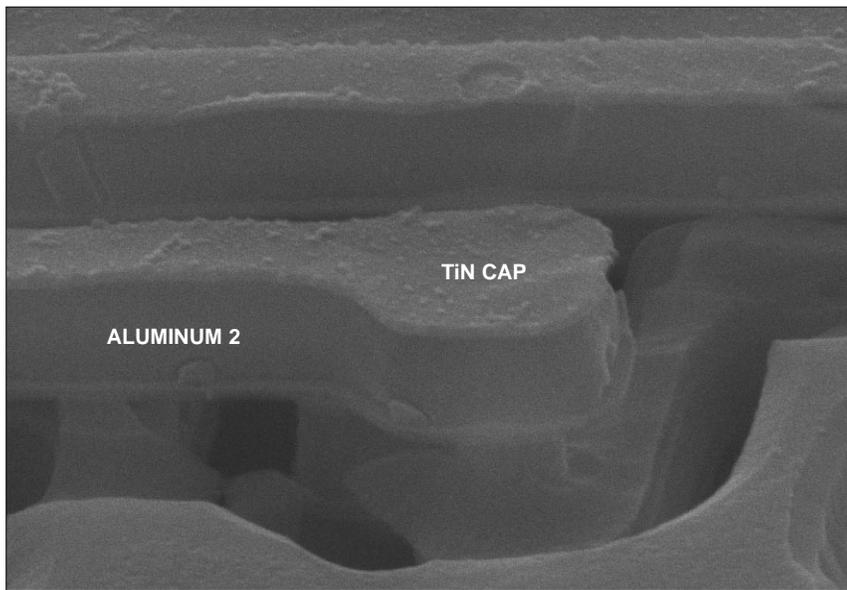


Mag. 13,000x

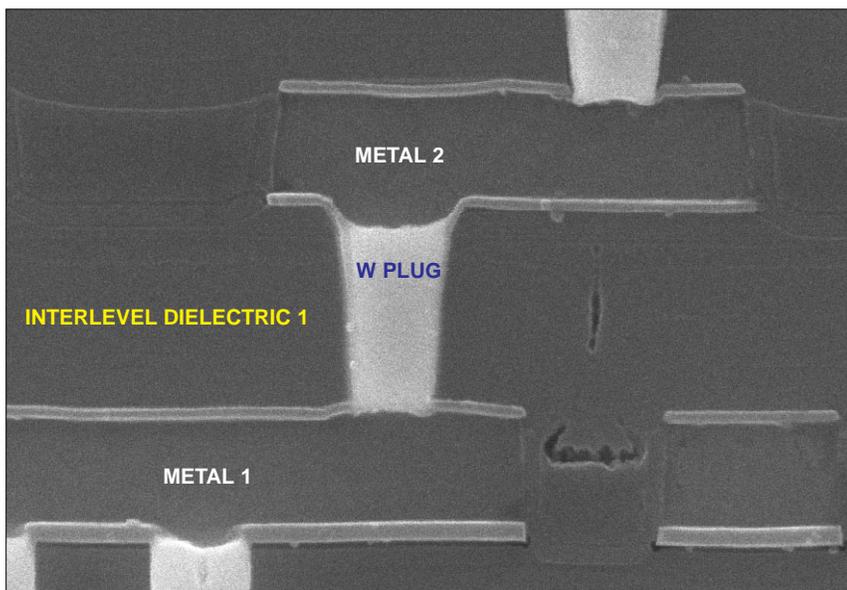
Figure 8. Topological SEM views of metal 2 patterning. 0°.



Mag. 6500x, 60°

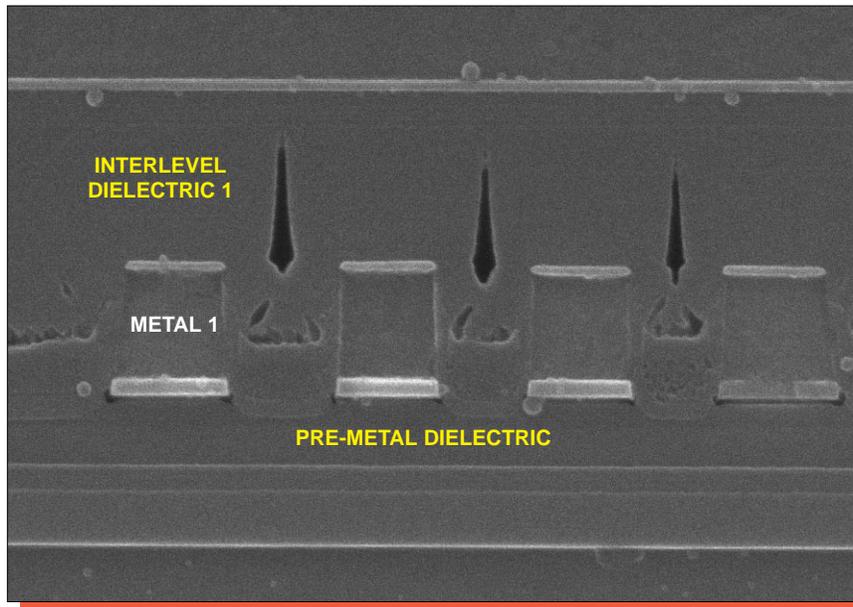


Mag. 26,000x, 60°

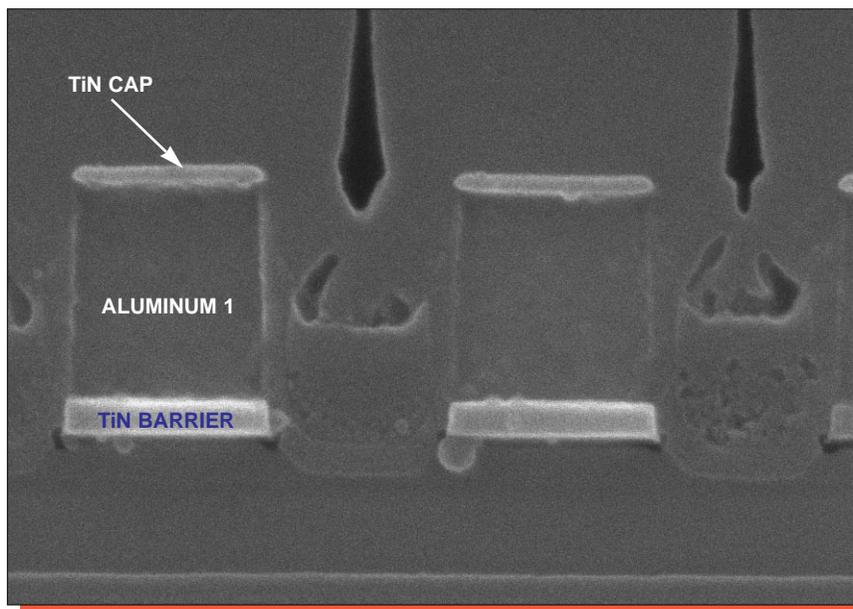


Mag. 26,000x, 60°

Figure 9. SEM views illustrating metal 2 step coverage and metal 2-to-metal 1 via.

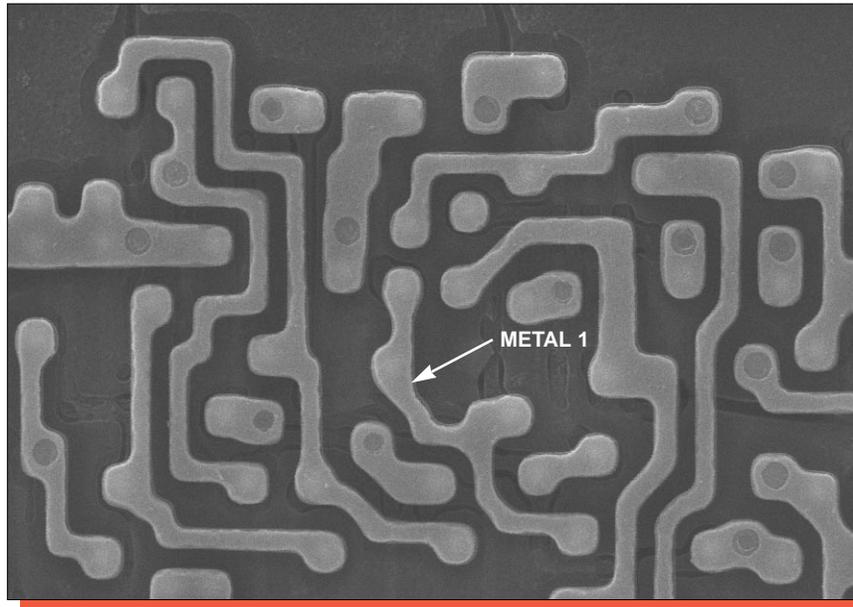


Mag. 26,000x

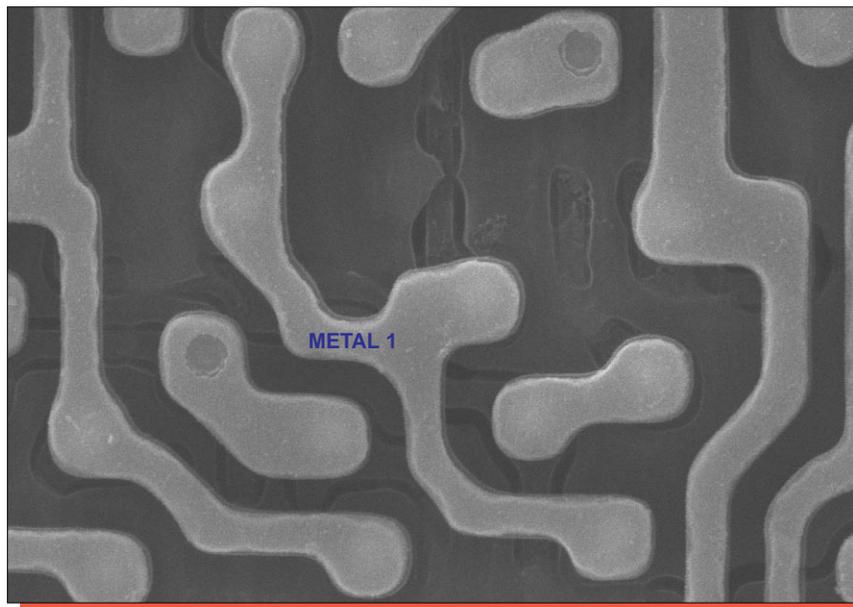


Mag. 52,000x

Figure 10. SEM section views of metal 1 line profiles.

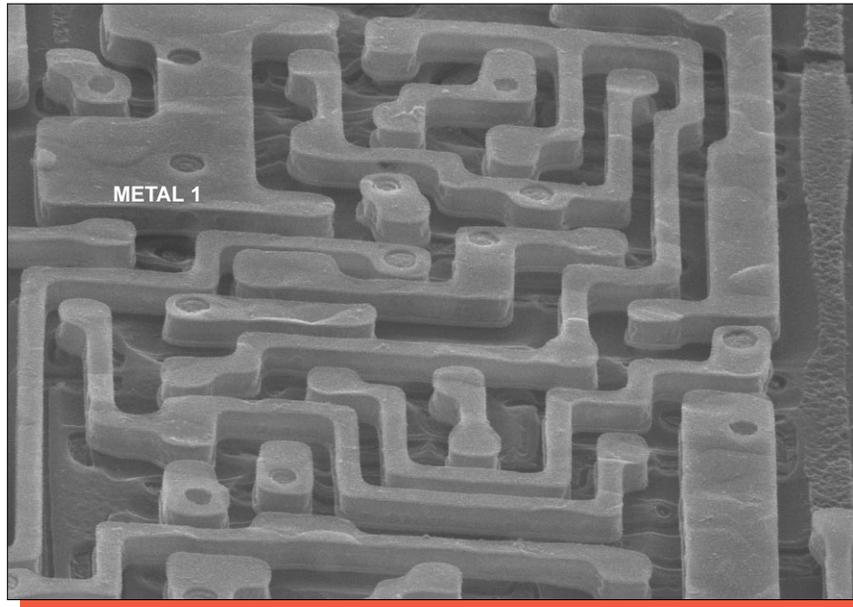


Mag. 5000x

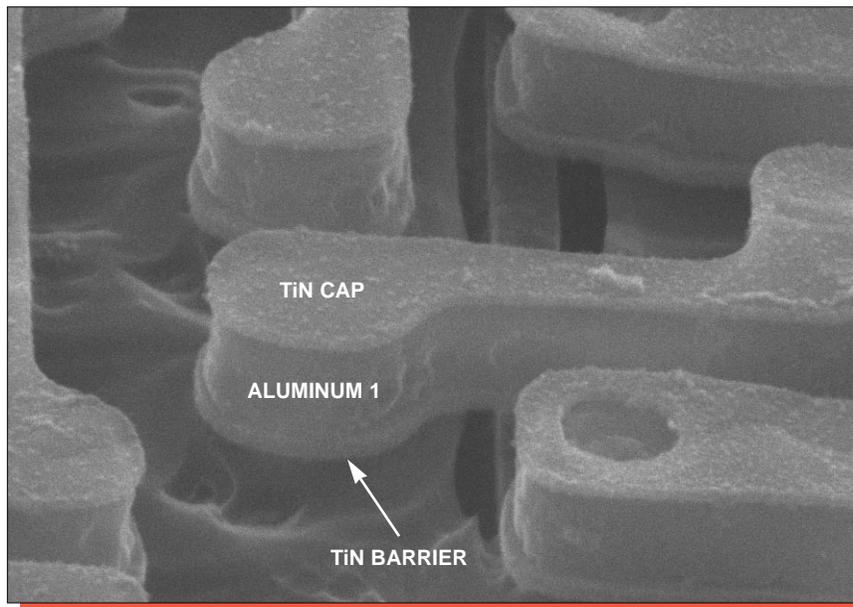


Mag. 10,000x

Figure 11. Topological SEM views of metal 1 patterning. 0°.

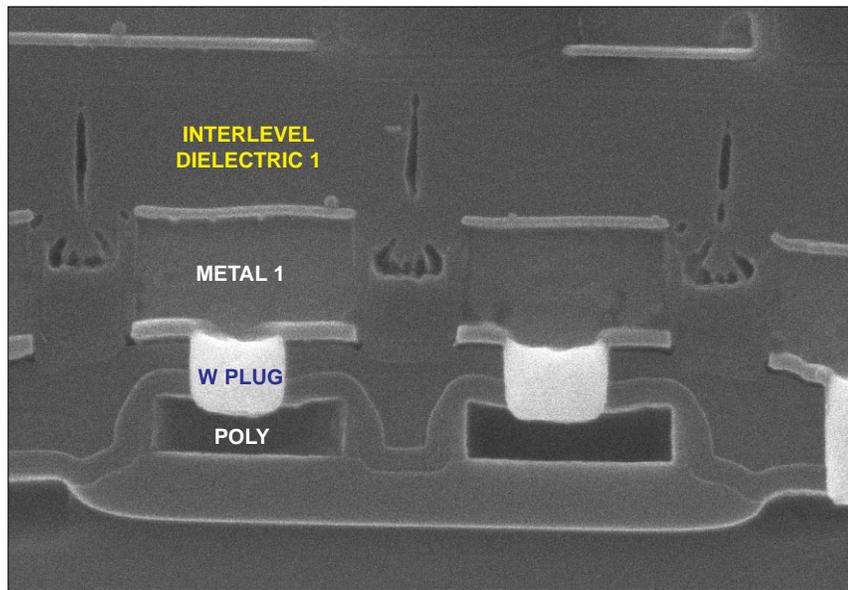


Mag. 6500x

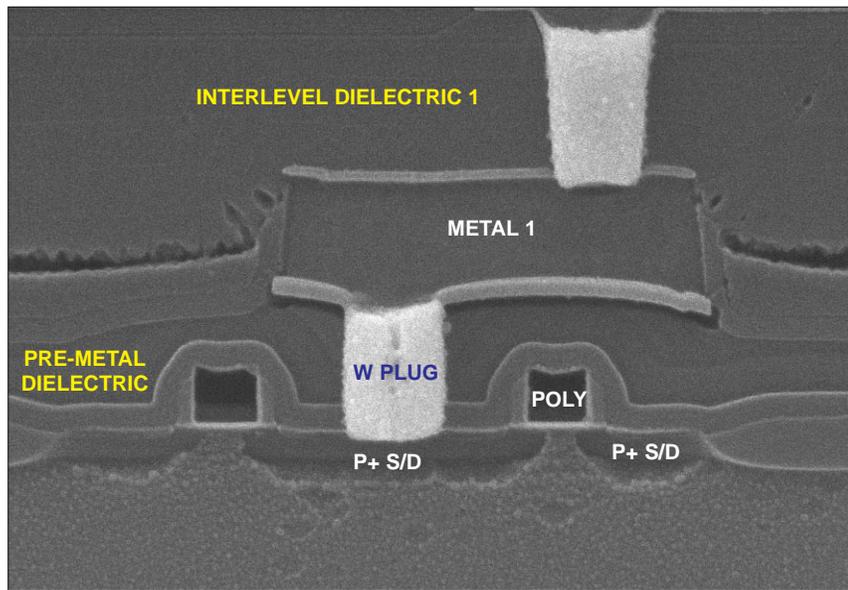


Mag. 26,000x

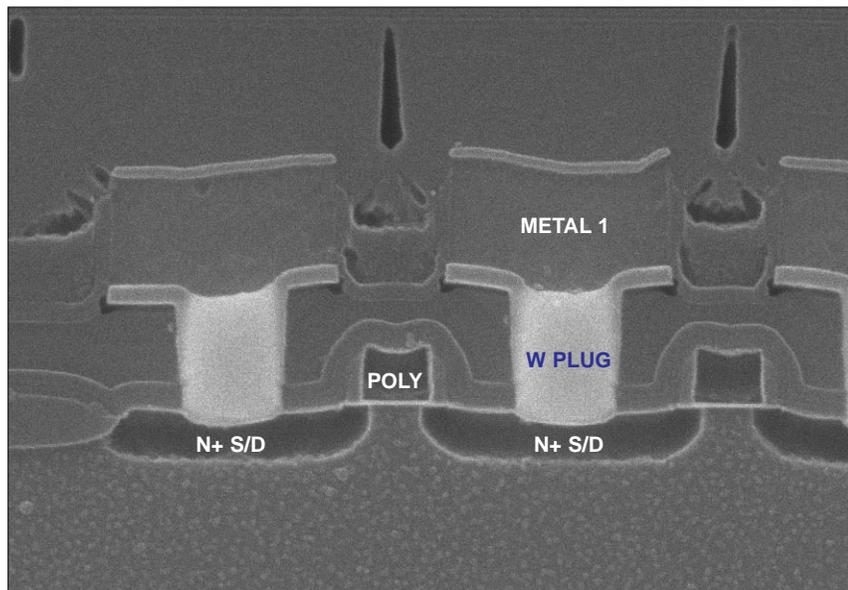
Figure 12. Perspective SEM views illustrating metal 1 step coverage. 60°.



metal 1-to-poly

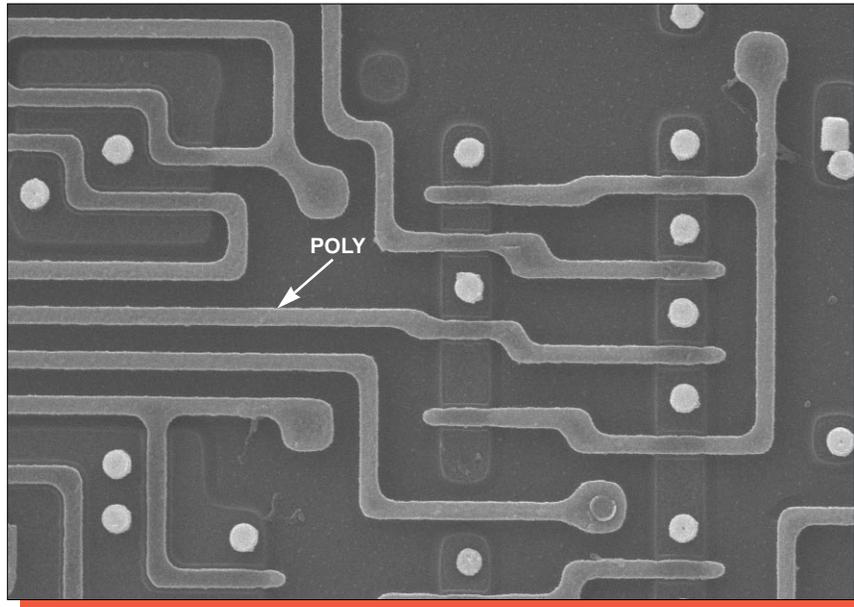


metal 1-to-P+

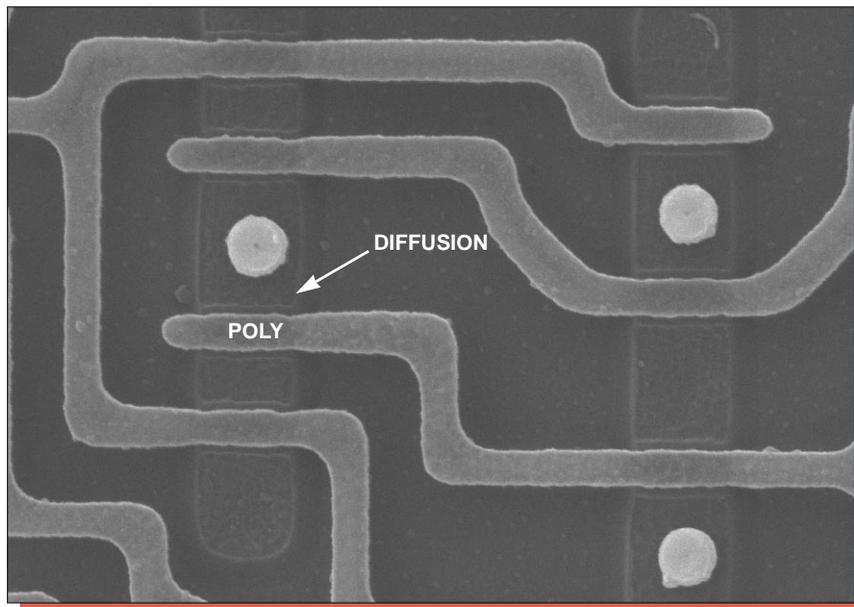


metal 1-to-N+

Figure 13. SEM section views of metal 1 contacts (silicon etch). Mag. 26,000x.

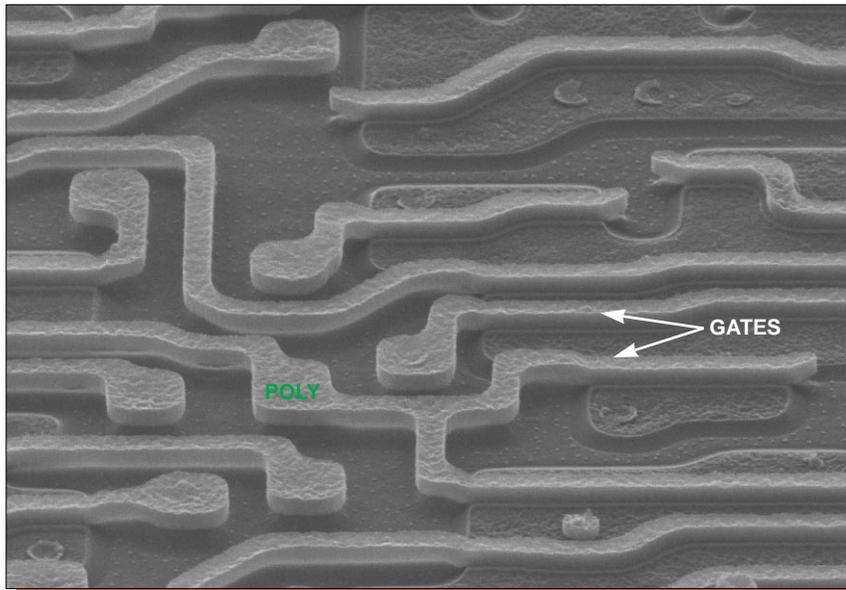


Mag. 6500x

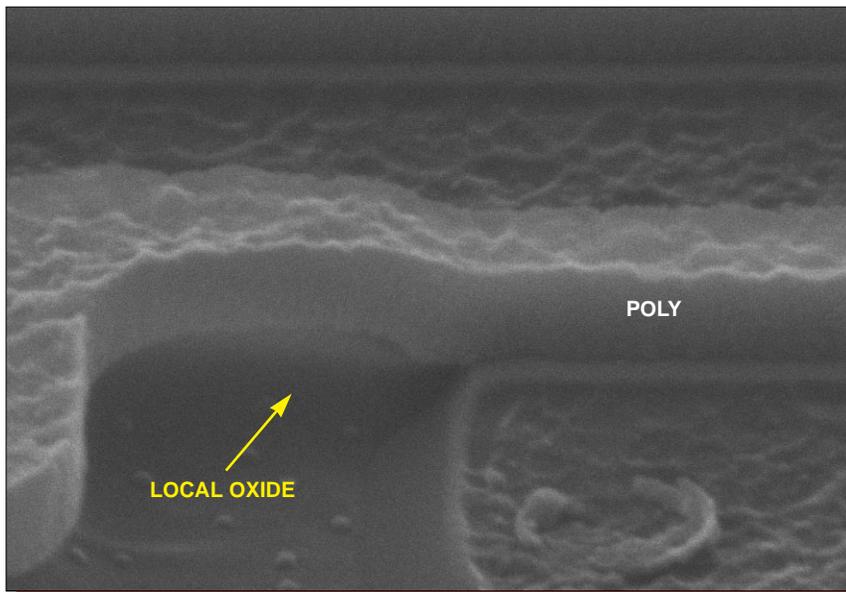


Mag. 13,000x

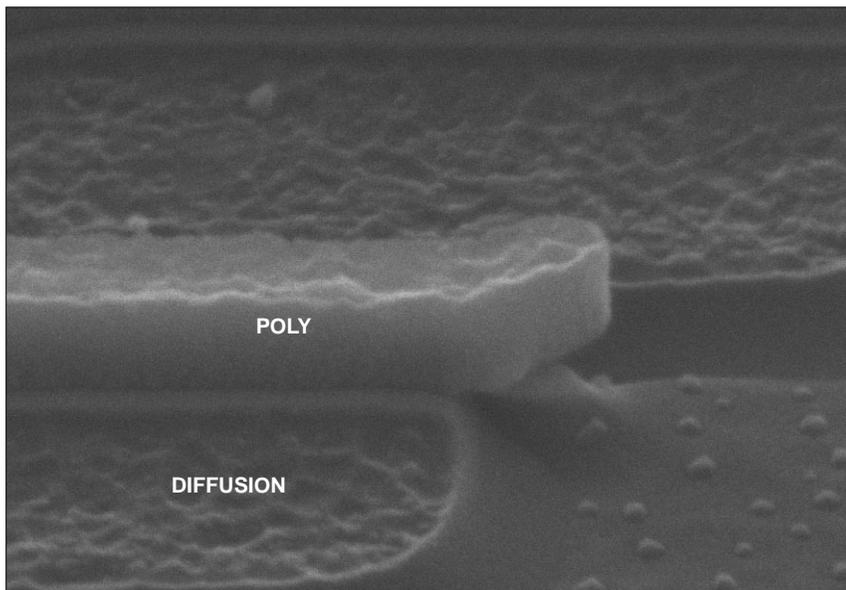
Figure 14. Topological SEM views of poly patterning. 0°.



Mag. 10,000x



Mag. 52,000x



Mag. 52,000x

Figure 15. SEM views of poly step coverage. 60°.

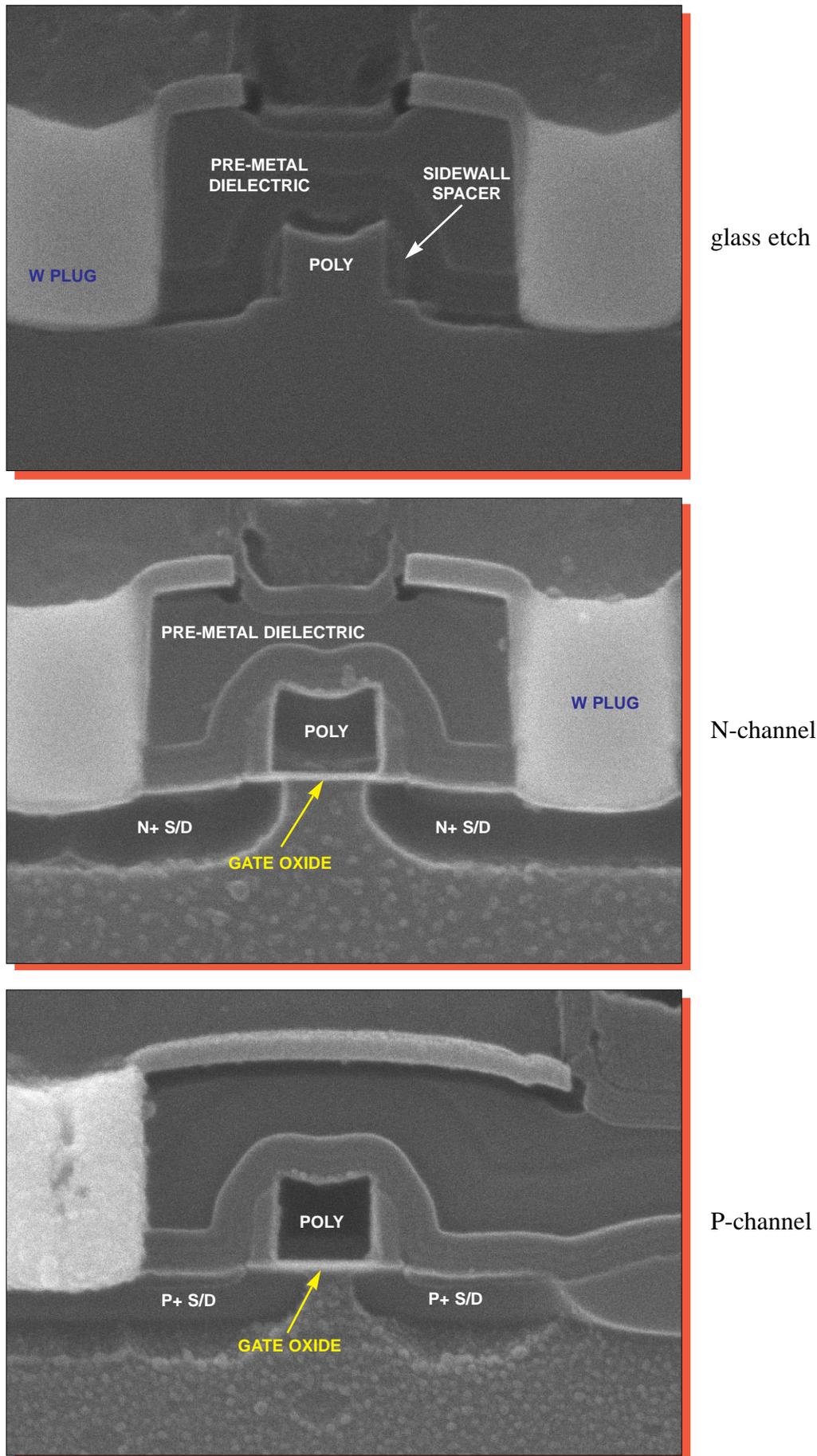


Figure 16. SEM section views of typical transistors. Mag. 52,000x.

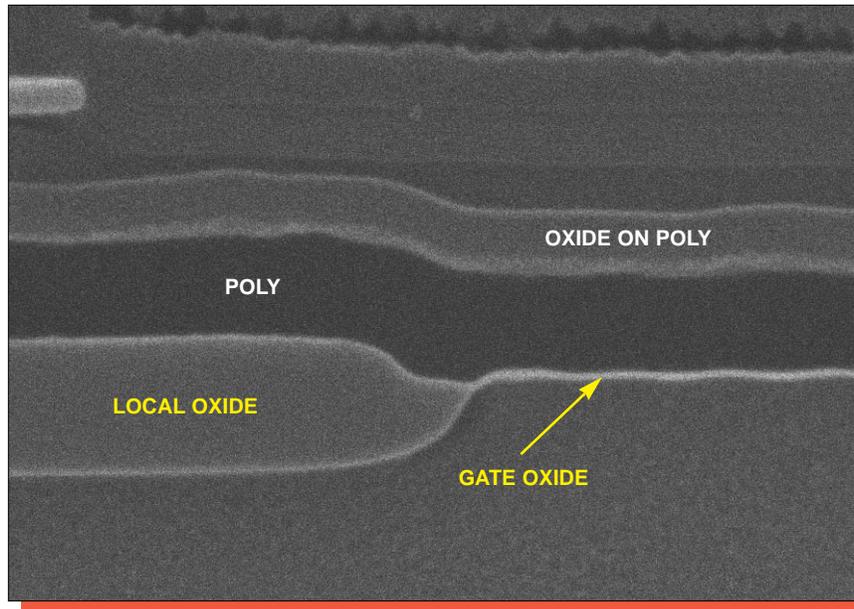


Figure 17. SEM section view of a typical local oxide birdsbeak. Mag. 52,000x.

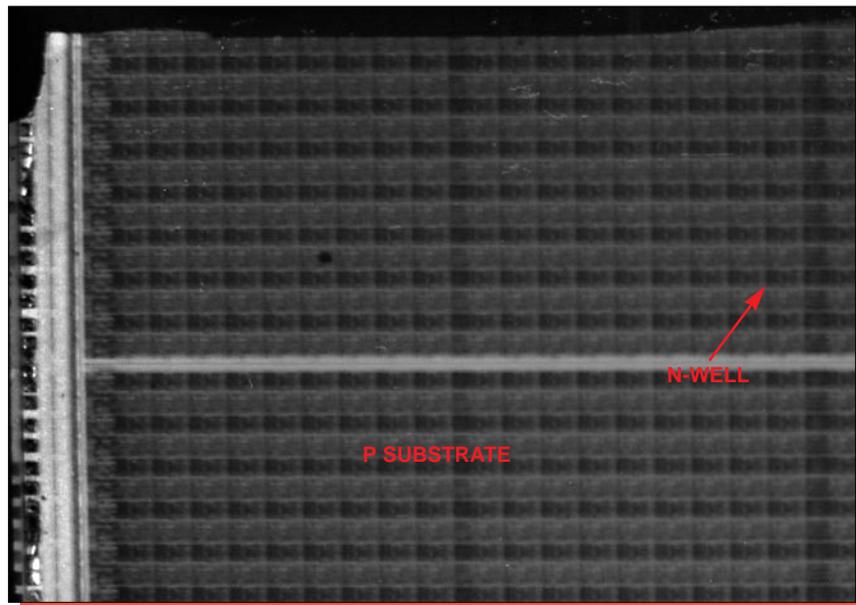
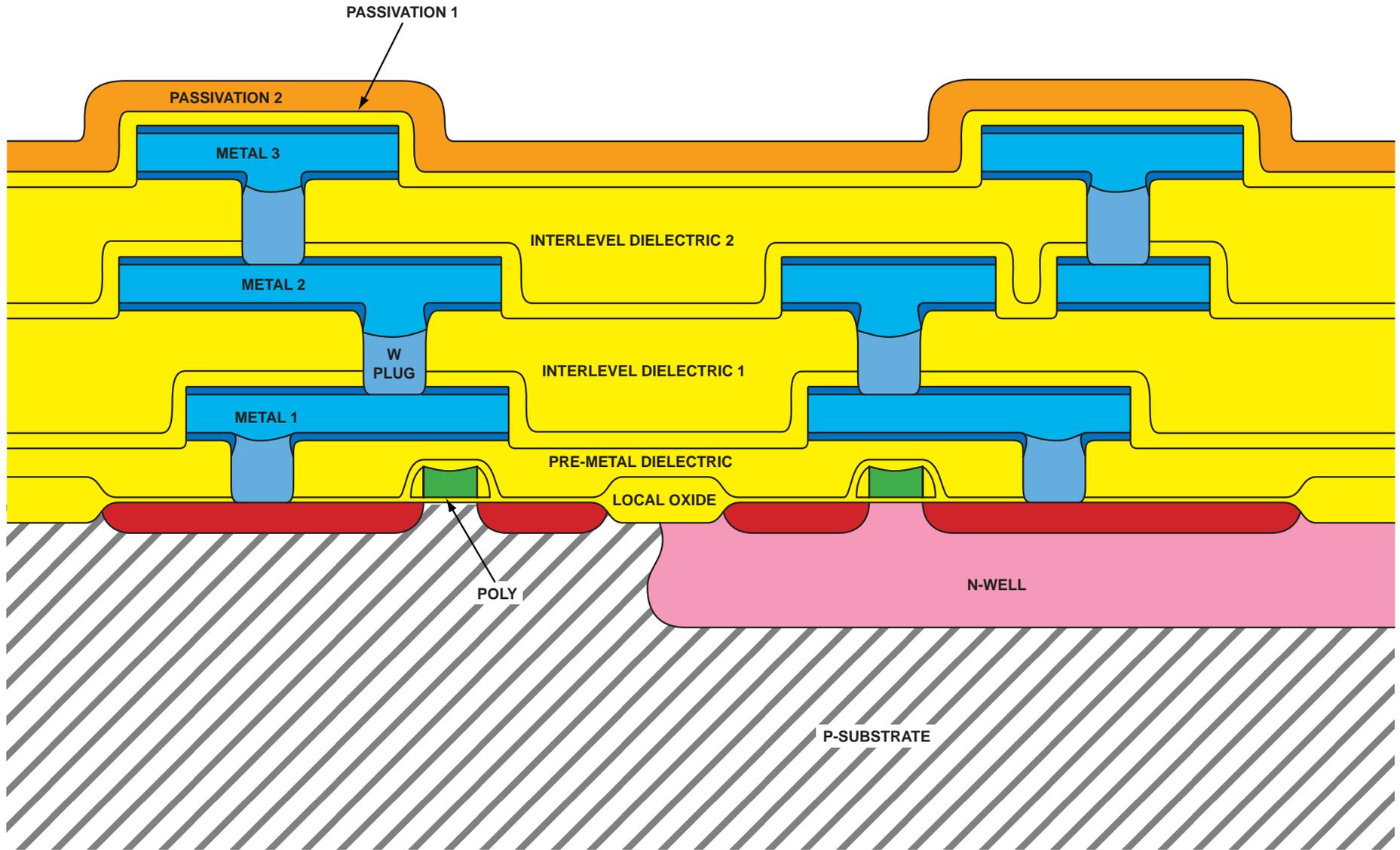
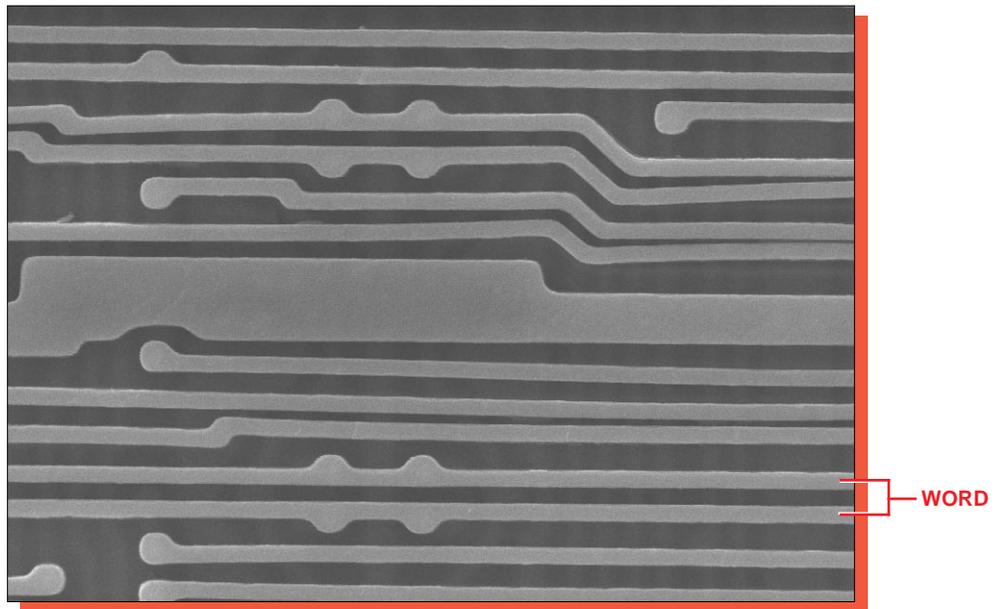


Figure 18. Section view illustrating the well structure. Mag. 800x.

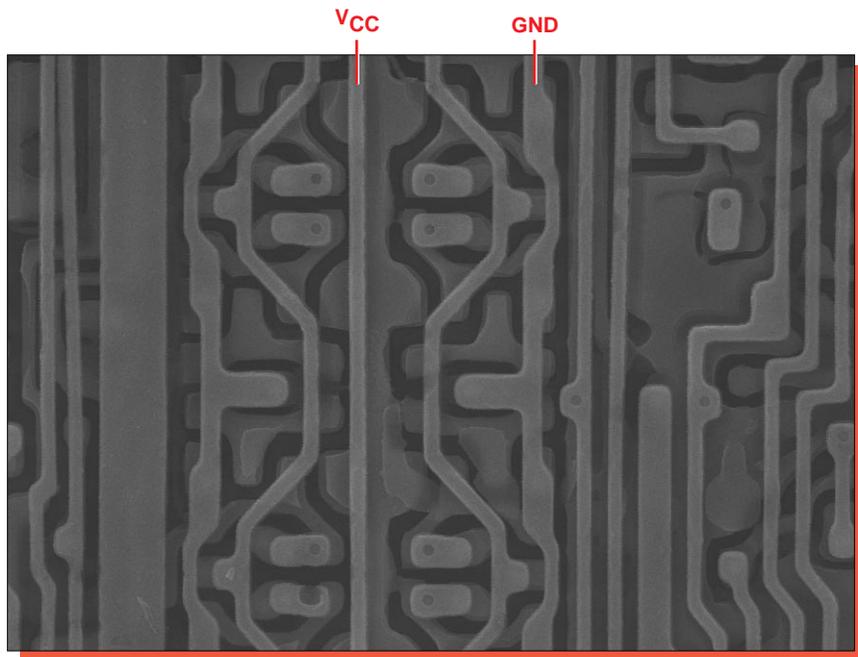


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
Red = Diffusion, and Gray = Substrate

Figure 19. Color cross section drawing illustrating device structure.

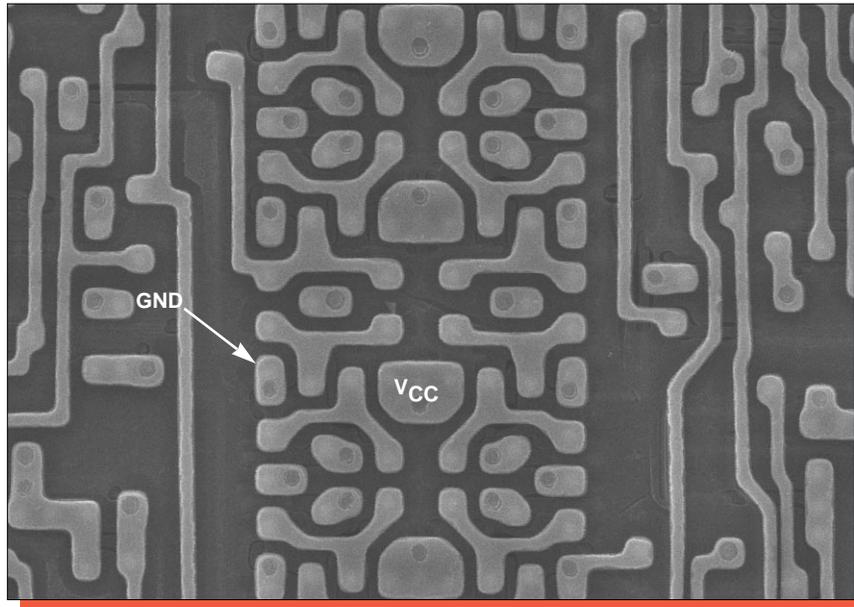


metal 3

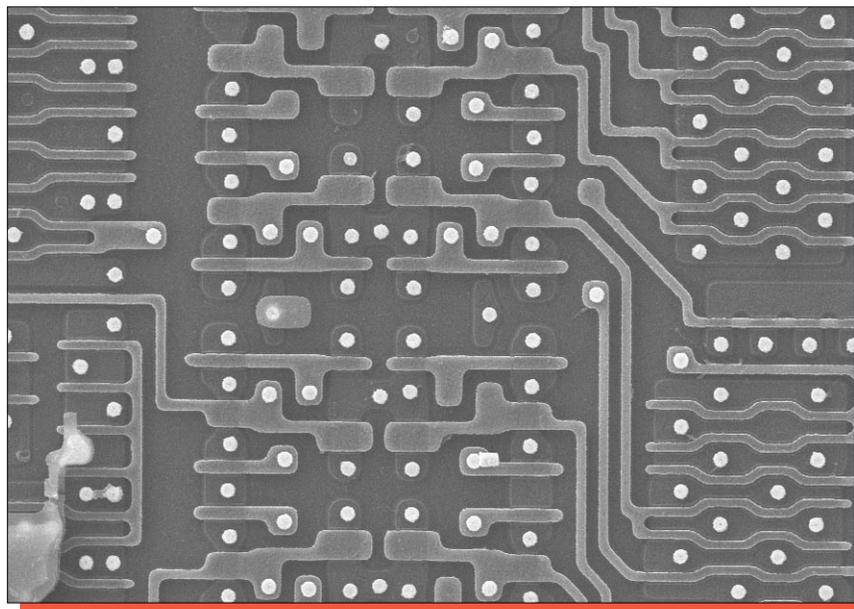


metal 2

Figure 20. Topological SEM views of the SRAM cell. Mag. 3200x, 0°.

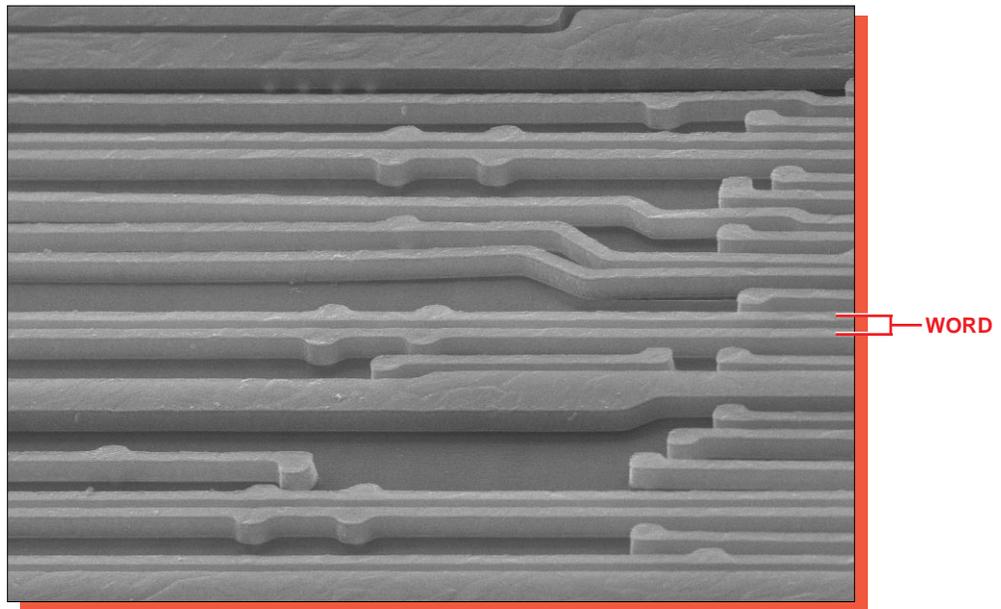


metal 1

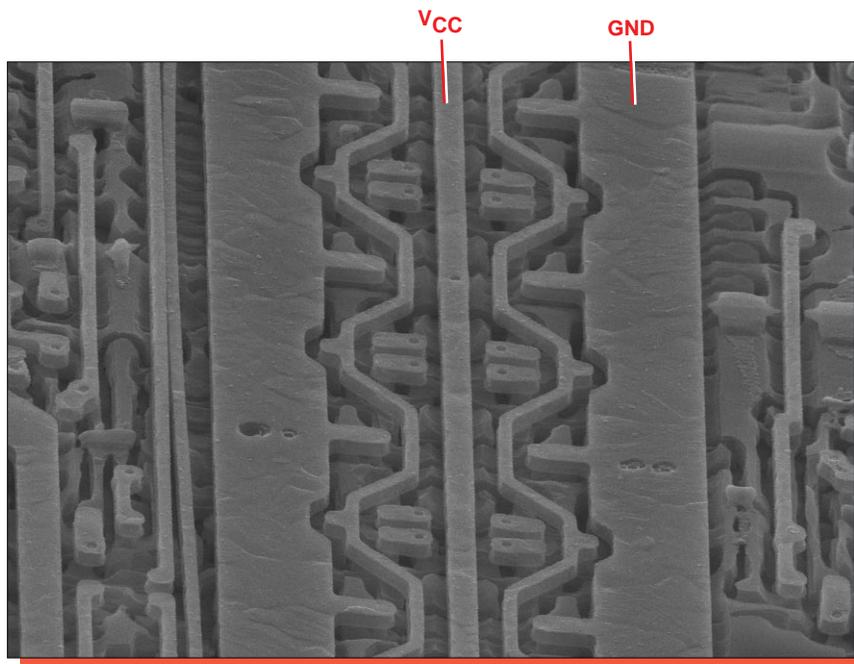


poly

Figure 21. Topological SEM views of the SRAM cell. Mag. 3200x, 0°.

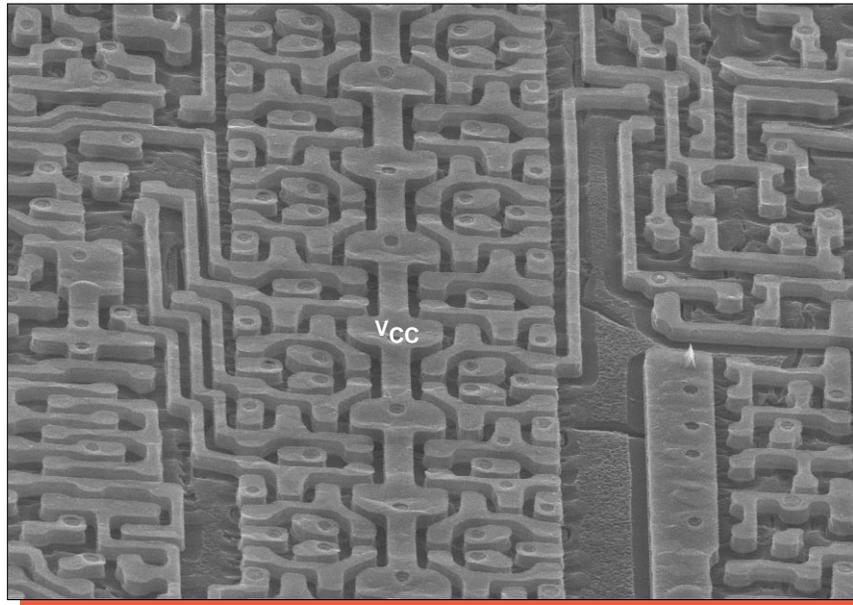


metal 3

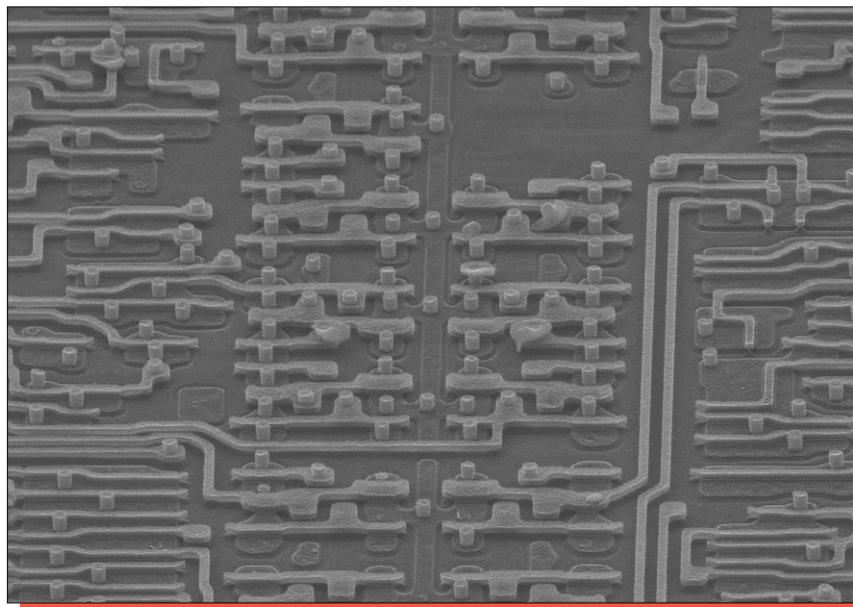


metal 2

Figure 22. Perspective SEM views of the SRAM cell. Mag. 3200x, 60°.

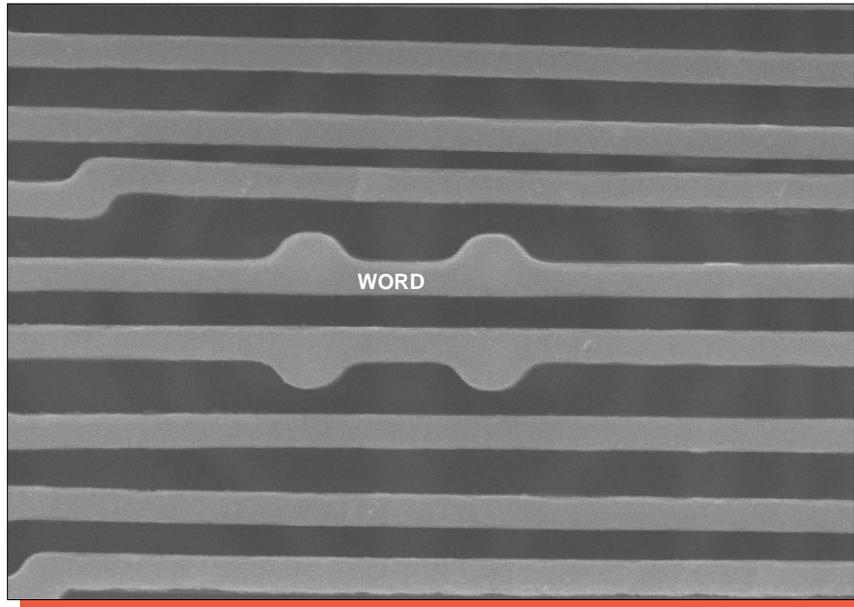


metal 1

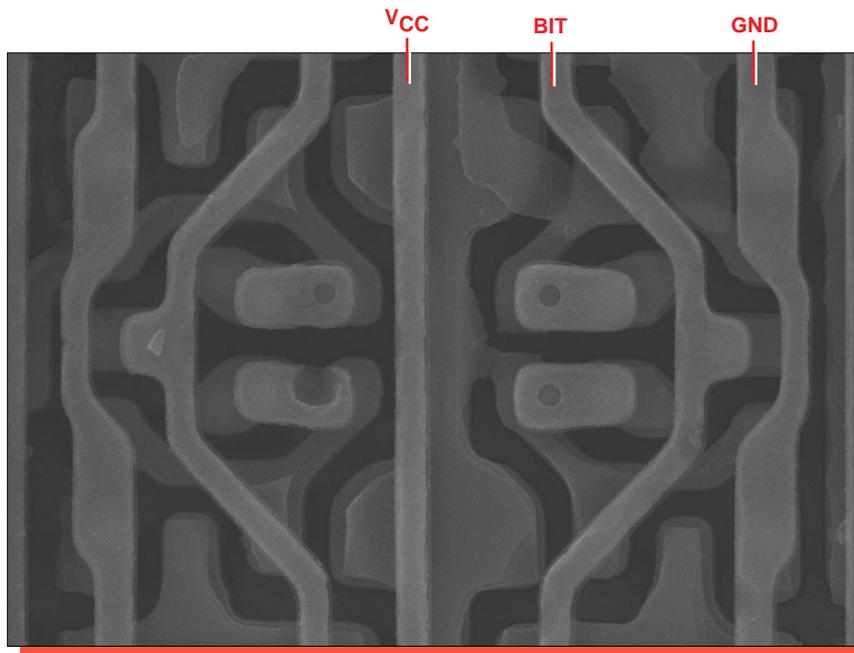


poly

Figure 23. Perspective SEM views of the SRAM cell. Mag. 3200x, 60°.



metal 3



metal 2

Figure 24. Detailed SEM views of the SRAM cell. Mag. 6500x, 0°.

