

Construction Analysis

Motorola PC603R Microprocessor

Report Number: SCA 9709-551



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INTRODUCTION

This report describes a construction analysis of the Motorola PC603R Microprocessor. Two engineering samples were supplied for the analysis. The devices were received in 256-pin Ball Grid Array (BGA) packages date coded 9713.

MAJOR FINDINGS

Questionable Items:¹

- Significant misalignment of metal 2 and 4 to the underlying plugs was noted (Figures 19 and 29)

Special Features:

- Six metal, P-epi, BiCMOS process.
- Metal 1 (tungsten) was defined by a damascene process. Stacked vias were employed.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.
- Aggressive design rule features (0.2 micron gates).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 256-pin (255 actual pins) Ball Grid Arrays (BGAs). The die was mounted surface down on the ceramic substrate (C4 flip-chip assembly).
- A blue colored underfill was present between the die surface and the ceramic substrate.
- Solder balls were employed for all connections to die metallization (C4 flip-chip process). There appeared to be space for standard bond pads around the die perimeter although used for protection diodes (?) in this case (see Figure 6).
- Sawn dicing (full depth).

Die Process:

- Fabrication process: Oxide-filled shallow-trench isolation, BiCMOS process employing twin-wells in an apparent P-epi on a P substrate.
- Die coat: A thin patterned polyimide die coat was present over the entire die.
- Final passivation: A layer of nitride over a layer of glass.
- Metallization: Six levels of metal defined by standard dry-etch techniques (except M1). Metal 1 (tungsten) was defined by a damascene process. Metals 2 - 6 consisted of aluminum. Metal 6 did not employ a cap or barrier metal. Metals 2 - 5 employed titanium-nitride caps and barriers. Tungsten plugs were employed for vias under metals 2 - 5. Metal 6 used standard vias. All tungsten plugs and tungsten metal 1 were lined with titanium-nitride. Stacked vias were employed at all levels. Elongated vias (M6 - M3) and contacts (M1) were also present.

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectrics: Interlevel dielectric 5 (between M5 and M6) consisted of two layers of glass. The first layer was subjected to an etchback. Interlevel dielectrics 2 - 4 used the same dielectric structure. A very thin glass was deposited first, followed by three separate layers of glass. The third layer of glass was planarized by CMP which left the surface very planar. The fourth layer appeared to have been similarly planarized during tungsten plug CMP. Interlevel dielectric 1 (between M1 and M2) consisted of a single thick layer of glass which had also been subjected to CMP.
- Pre-metal glass: A thin layer of glass over a thick layer of glass and a thin nitride. This dielectric was also planarized by CMP.
- Polysilicon: A single layer of dry-etched polycide (poly and titanium-silicide). This layer was used to form all gates on the die. Nitride sidewall spacers were used to provide the LDD spacing.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Titanium was sintered into the diffusions (salicide process).
- Isolation: Field oxide consisted of oxide-filled shallow-trench isolation. It was very planar with the diffused silicon surfaces. A small step was noted on top of the trench oxide at well boundaries.
- Wells: Twin-wells in a P-epi on a P substrate.
- SRAM: On-chip cache memory cell arrays were employed. The memory cells used a 6T CMOS SRAM cell design. Metal 3 formed the bit lines and metal 2 distributed GND and Vcc throughout the cells and was used as “piggyback” word lines and cell interconnect. Metal 1 also provided cell interconnect. Polycide formed the select and storage gates. Cell pitch was 3.5 x 5.1 microns (17.8 microns²).
- There appeared to be bipolar devices on the die; however, we could not verify them in cross-section due to our inability to see them before complete delayering.
- No redundancy fuses were found.

ANALYSIS RESULTS

Die Process and Design:

Figures 1 - 46

Questionable Items:¹

- Significant misalignment of metal 2 and 4 to the underlying plugs was noted (Figures 19 and 29)

Special Features:

- Six metal, P-epi, BiCMOS process.
- Metal 1 (tungsten) was defined by a damascene process. Stacked vias were employed.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.
- Aggressive design rule features (0.2 micron).

General items:

- Fabrication process: Oxide filled shallow-trench isolation, BiCMOS process employing twin-wells in an apparent P-epi on a P substrate. No problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was adequate at most levels; however, alignment of metals 2 and 4 to their respective underlying plugs was poor. Plug coverage was only 35-to-40 percent at some metal 2 and 4 vias. Some isolated metal 6 vias were noted on the die (see Figure 6).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS (continued)

- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Die coat: A patterned polyimide die coat was present over the entire die surface.
- Final passivation: A layer of nitride over a layer of glass. Coverage was good. Edge seal was also good as the passivation extended to the scribe lane to seal the metallization. A cutout was present in the passivation and ILD 5 around the die perimeter to prevent cracks from radiating over the circuitry.
- Metallization: Six levels of metal interconnect. Metals 2 - 6 consisted of aluminum. Metals 2 - 5 employed titanium-nitride caps and barriers. Metal 6 did not employ a cap or barrier metal. Tungsten plugs were employed with metals 2 - 5. All plugs were lined with titanium-nitride underneath and over top. Standard vias were employed under metal 6. Metal 1 consisted of tungsten defined by a damascene process. The metal 1 tungsten was also lined with titanium-nitride.
- Metal patterning: All aluminum metal levels were defined by a dry etch of good quality. Metal lines were only widened at metal 6 via connections.
- Metal defects: None (excluding misalignment). No voiding, notching or cracking of the metal layers was found. No silicon nodules were found following removal of the metal layers.
- Metal step coverage: Metal 6 thinned up to 75 percent at vias. Although the thinning exceeds MIL-STDs (70 percent) it is not considered a reliability concern. No metal thinning was present at the connections to the tungsten via plugs or metal 1. The absence of thinning is due to the good control of plug height and the planarization technique employed.
- Vias and contacts: All via and contact cuts were defined by a dry etch of good quality. Again there was significant misalignment of metal 2 and 4 to their respective plugs. This misalignment reduced metal spacing to adjacent plugs (see Figure 32). Some tungsten plugs “spilled over” one edge of the metal. IBM uses this “borderless” contact technique for improved contact resistance. Vias and contacts were placed directly over one another (stacked vias). No problems were noted.

ANALYSIS RESULTS (continued)

- Interlevel dielectrics: Interlevel dielectric 5 (between M5 and M6) consisted of two layers of glass. The first layer was subjected to an etchback. Interlevel dielectrics 2 - 4 consisted of the same type of oxide structure. A very thin glass was deposited first, followed by three separate layers of glass. The third and fourth layers of glass were subjected to CMP which left the surface very planar. No CMP was performed on ILD 5 (under M6). Interlevel dielectric 1 (between M2 and M1) consisted of a single thick layer of glass which had also been subjected to CMP. No problems were found with any of these layers.
- Pre-metal glass: A thin layer of silicon-dioxide over a thick layer of glass and a thin nitride. This layer was also planarized by chemical-mechanical-planarization. No problems were found.
- Polysilicon: A single level of polycide (poly and titanium-silicide) was used. It formed all gates and word lines in the array. Definition was by dry etch of good quality. Nitride sidewall spacers were used throughout and left in place. No problems were found.
- Isolation: The device used oxide-filled shallow-trench isolation which was quite planar with the silicon surface. A small step was noted on top of the trench oxide at well boundaries. No problems were present.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Titanium was sintered into the diffusions (salicide process) to reduce series resistance. An LDD process was used employing nitride sidewall spacers.
- Wells: Twin-wells were used in a P-epi on a P substrate. Definition was normal. We could not delineate the P-well in cross-section.
- Buried contacts: Direct poly to diffusion contacts were not used.
- SRAM: As mentioned, on-chip cache memory cell arrays were employed on the device. The SRAM cell array used a 6T CMOS SRAM cell design. Metal 3 formed the bit lines. Metal 2 distributed GND and Vcc throughout the cells and was used as “piggyback” word lines and cell interconnect. Metal 1 also provided cell interconnect. Polycide formed the word lines/select and storage gates. Cell pitch was 3.5 x 5.1 microns.

ANALYSIS RESULTS (continued)

- There appeared to also be bipolar devices on the die as observed from the surface. Since they could only be seen once the die was delayered we were unsuccessful in obtaining a cross section through one of these devices to observe the sectional structure.
- No redundancy fuses were noted.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Die optical inspection

Delayer to metal 6 and inspect

Aluminum removal (metal 6)

Delayer to metal 5 and inspect

Aluminum removal (metal 5) and inspect tungsten plugs

Delayer to metal 4 and inspect

Aluminum removal (metal 4) and inspect tungsten plugs

Delayer to metal 3 and inspect

Aluminum removal (metal 3) and inspect tungsten plugs

Delayer to metal 2 and inspect

Aluminum removal (metal 2) and inspect tungsten plugs

Delayer to metal 1 and inspect

Tungsten removal (metal 1)

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

OVERALL QUALITY EVALUATION: Overall Rating: Normal.

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Solder ball placement	G
Solder ball interconnect quality	G
Dicing quality	N
Die attach quality	G
Die attach method	C4 solder ball interconnect technique
Dicing method	Sawn
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	N
Metal registration	NP ¹
Contact coverage	NP ¹
Via/contact registration	N
Etch control (depth)	N

¹Misalignment of M2 and M4 to underlying plugs.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

(Logo) XPC603RRX250LA
70H92D DTC9713B
S23687 W001

DIE MATERIAL ANALYSIS

Final passivation:	Single layer of nitride over a single layer of glass.
Metallization 6:	Aluminum.
Interlevel dielectric 5:	Two layers of glass.
Metallization 2 - 5:	Aluminum with titanium-nitride caps and barriers.
Interlevel dielectrics 2 - 4:	A thin layer of glass followed by three layers of glass.
Interlevel dielectric 1:	Thick layer of glass.
Metallization 1:	Tungsten (damascene process) with titanium-nitride liner.
Vias (M2 - M5):	Tungsten (lined with titanium-nitride).
Pre-metal glass:	Thin layer of glass over a thick layer of silicon-dioxide and a thin nitride.
Polycide:	Titanium-silicide on polysilicon.
Salicide on diffusions:	Titanium-silicide.

INDEX TO FIGURES

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DIE LAYOUT AND IDENTIFICATION	Figures 2 - 6
PHYSICAL DIE STRUCTURES	Figures 7 - 46
COLOR DRAWING OF DIE STRUCTURE	Figure 43
MEMORY CELL	Figures 44 - 46

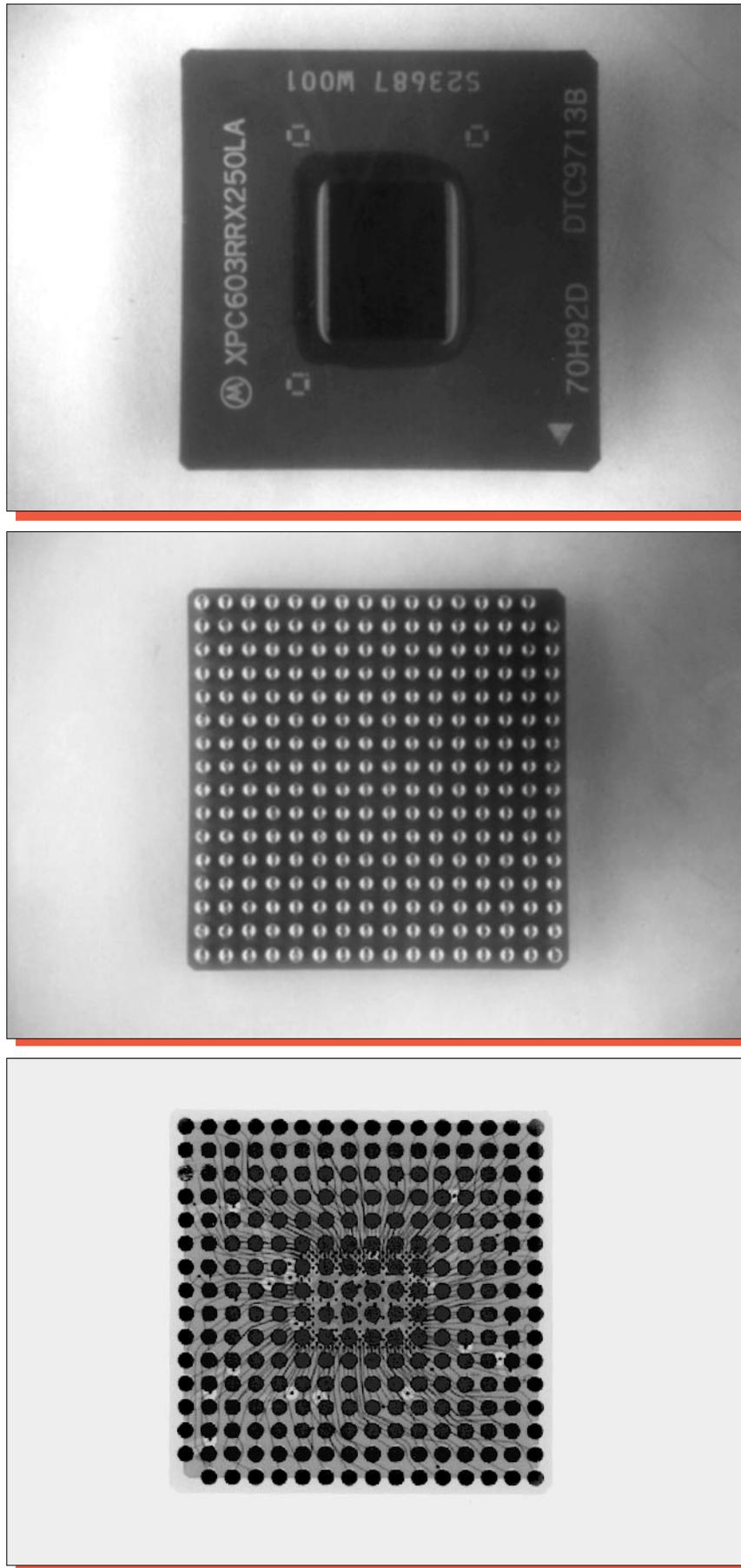


Figure 1. Package photographs and x-ray view of the Motorola PC603R Microprocessor. Mag. 2.8x.

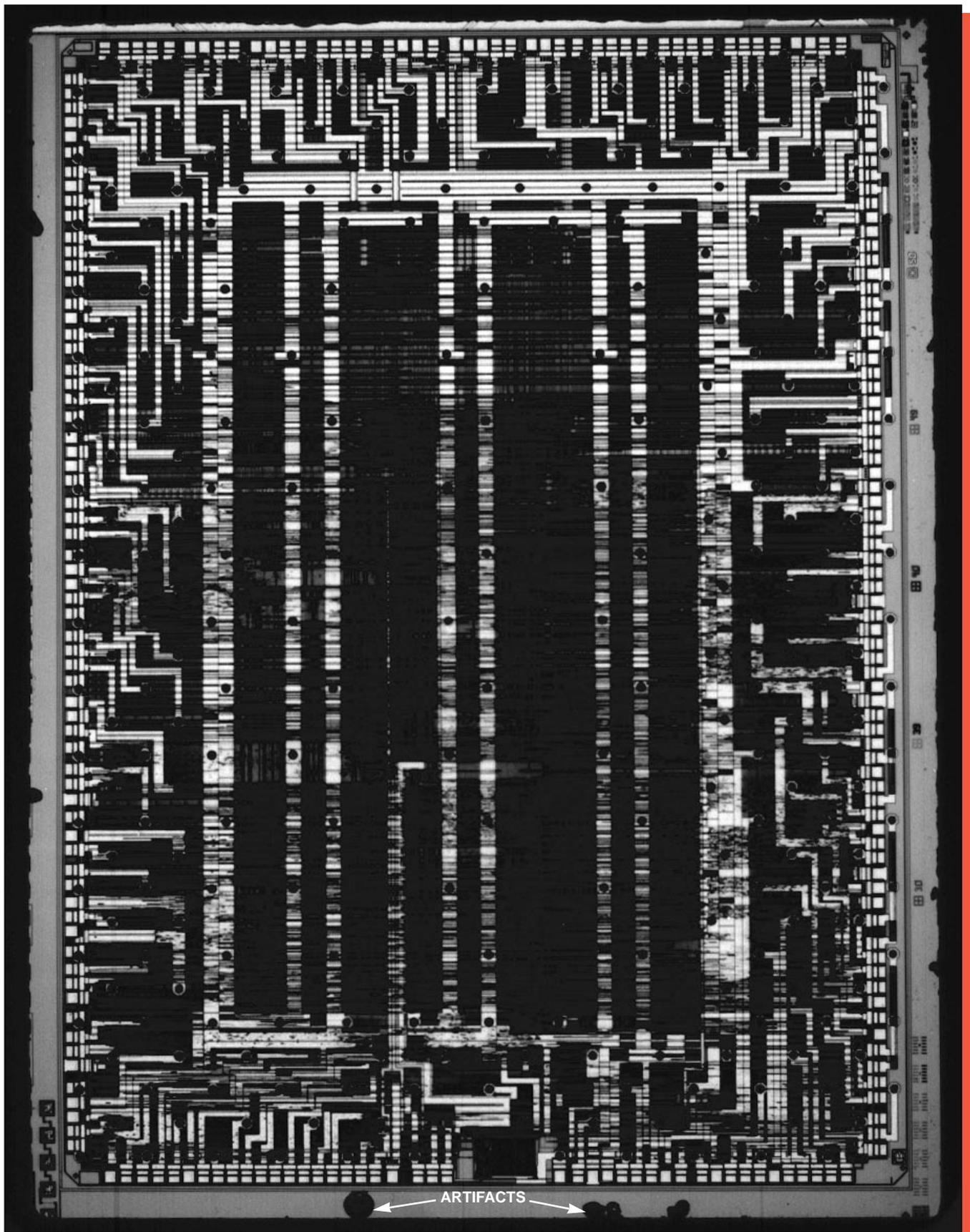


Figure 2. Whole die photograph of the Motorola PC603R Microprocessor. Mag. 28x.

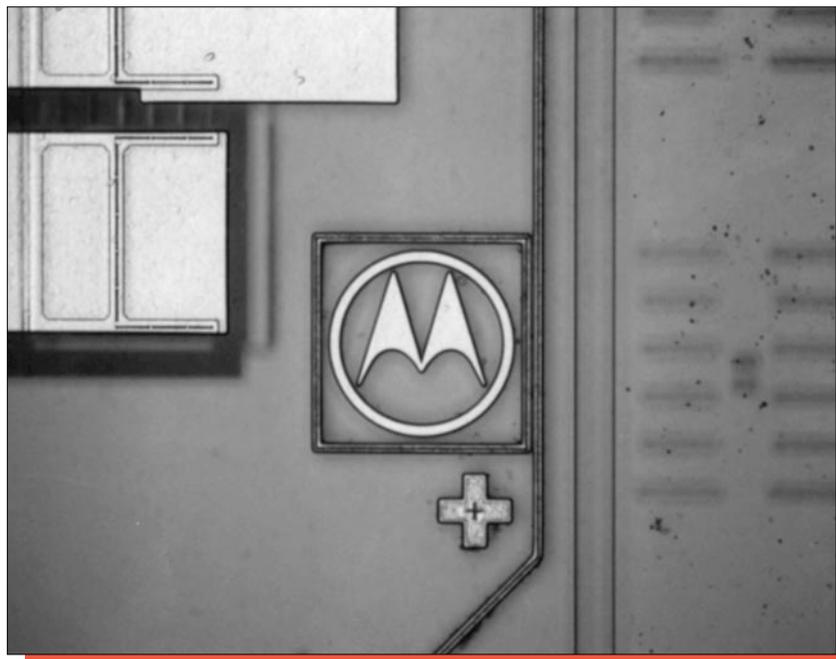


Figure 3. Die markings from the surface. Mag. 320x.

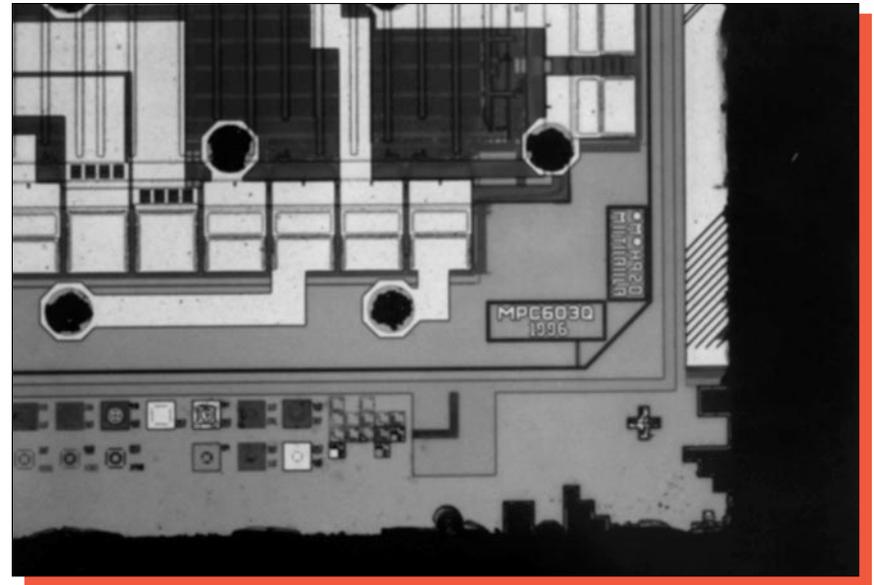
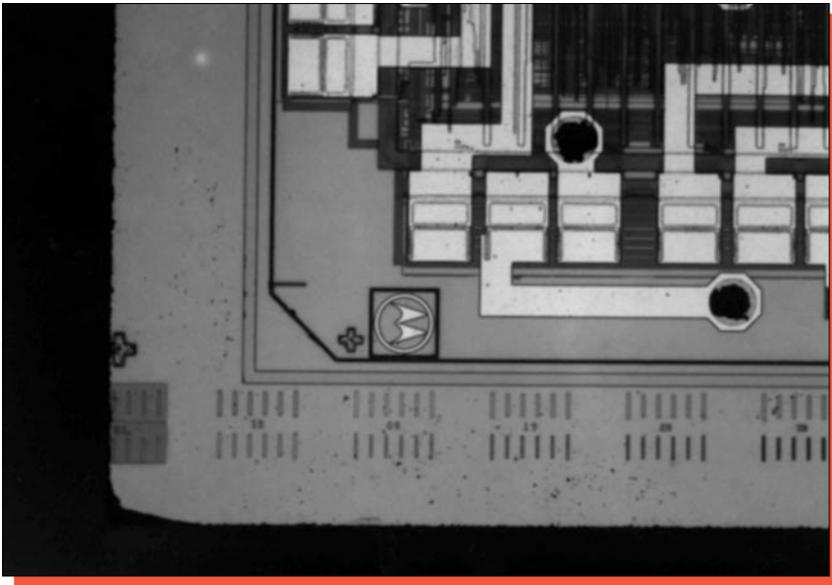
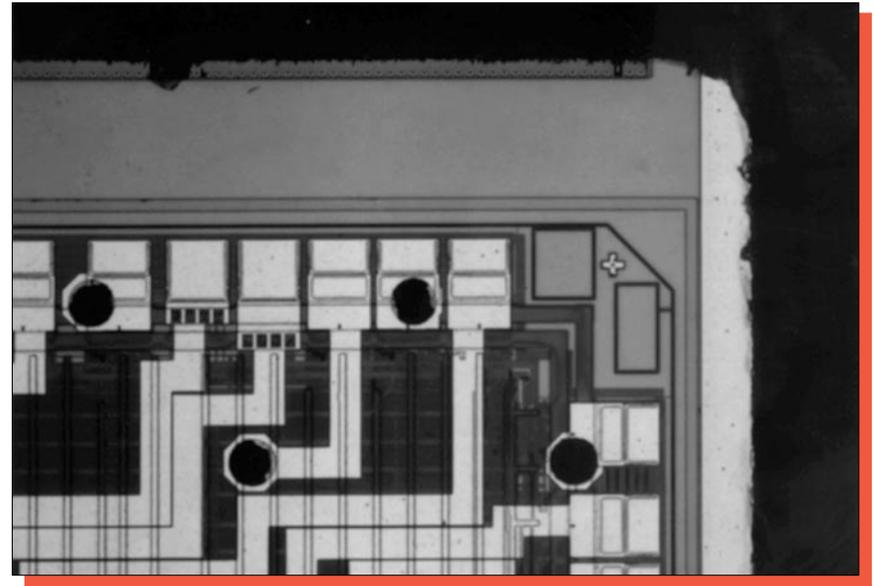
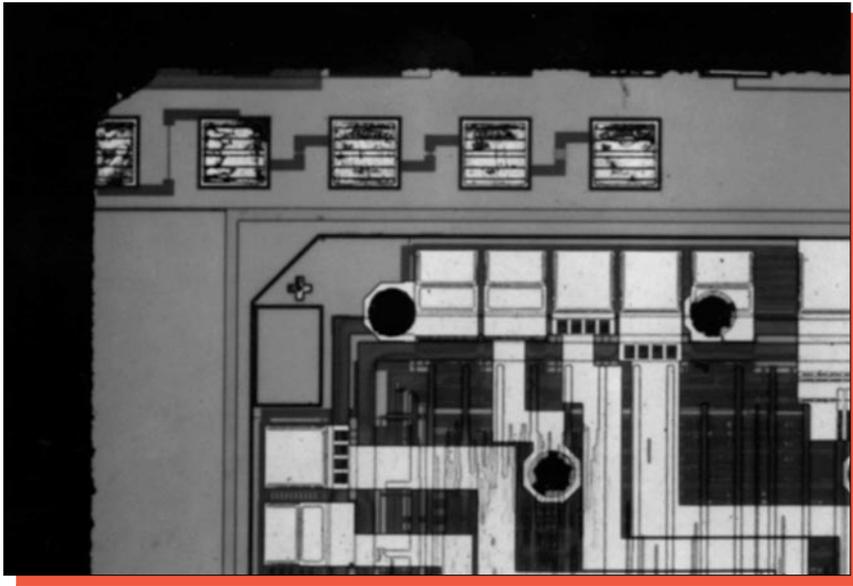
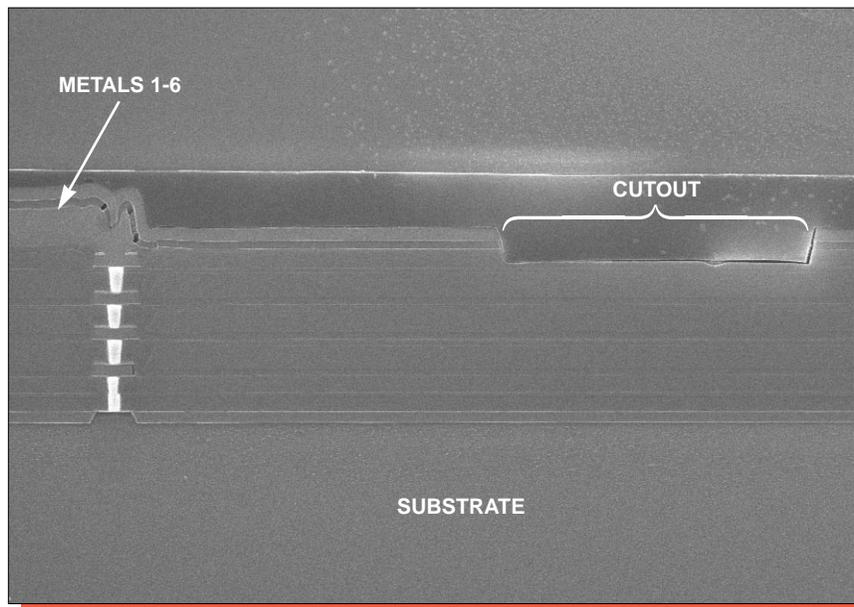
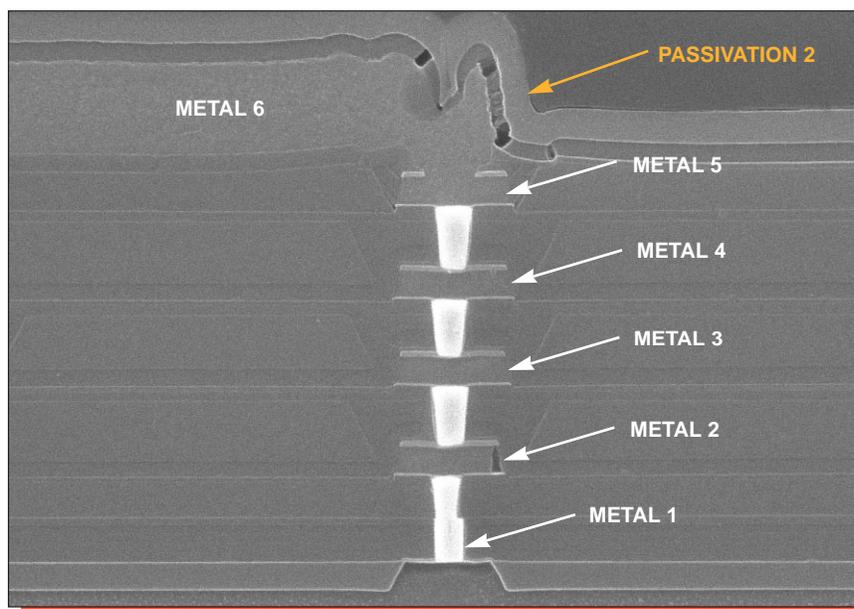


Figure 4. Optical views of the die corners. Mag. 100x.

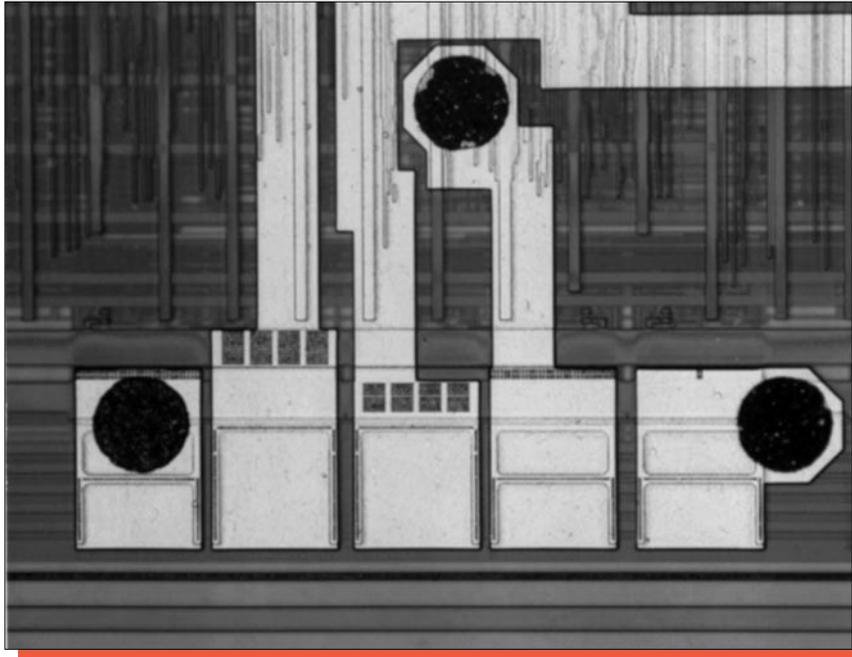


Mag. 2700x

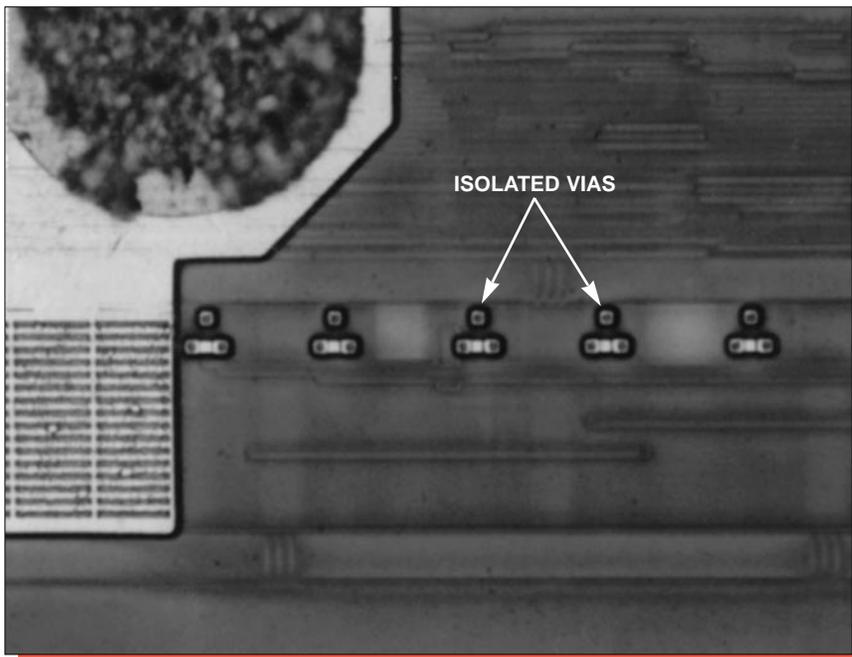


Mag. 6750x

Figure 5. SEM section views of the edge seal structure.

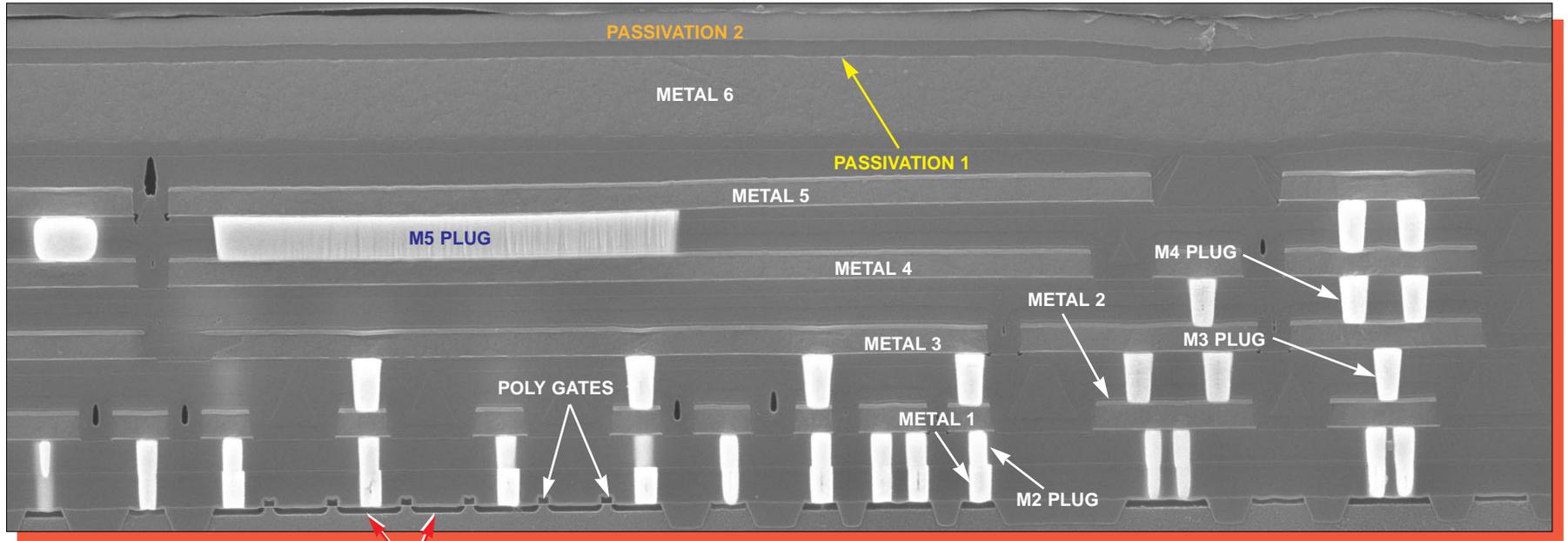


Mag. 200x

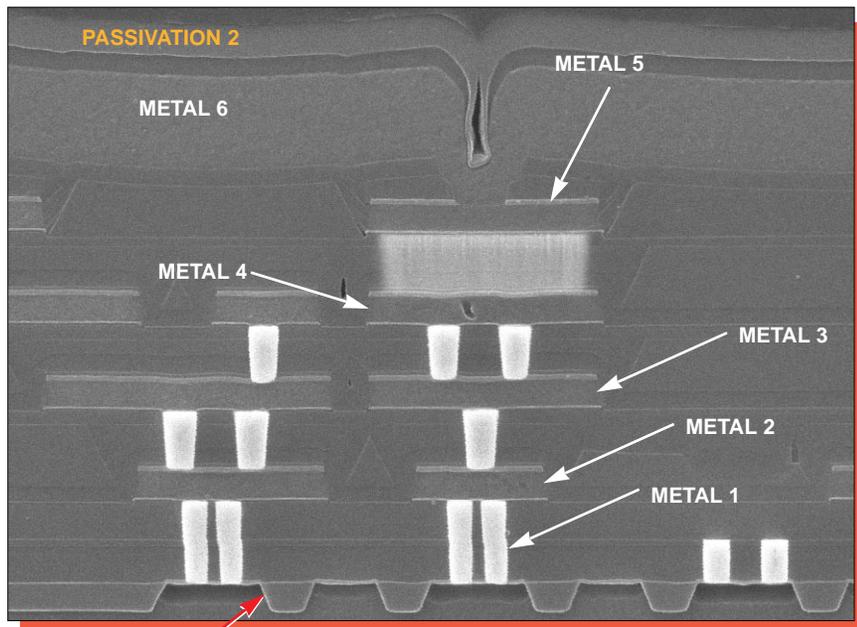


Mag. 800x

Figure 6. Optical views of layout features.

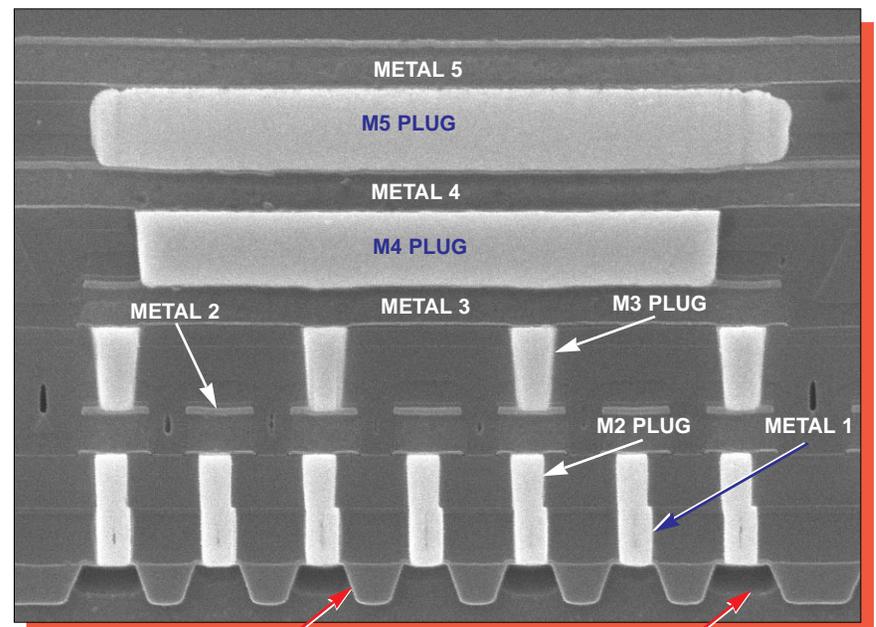


Mag. 6750x



TRENCH OXIDE

Mag. 7000x



TRENCH OXIDE

Mag. 9000x

N+

Figure 7. SEM section views of general device structure.

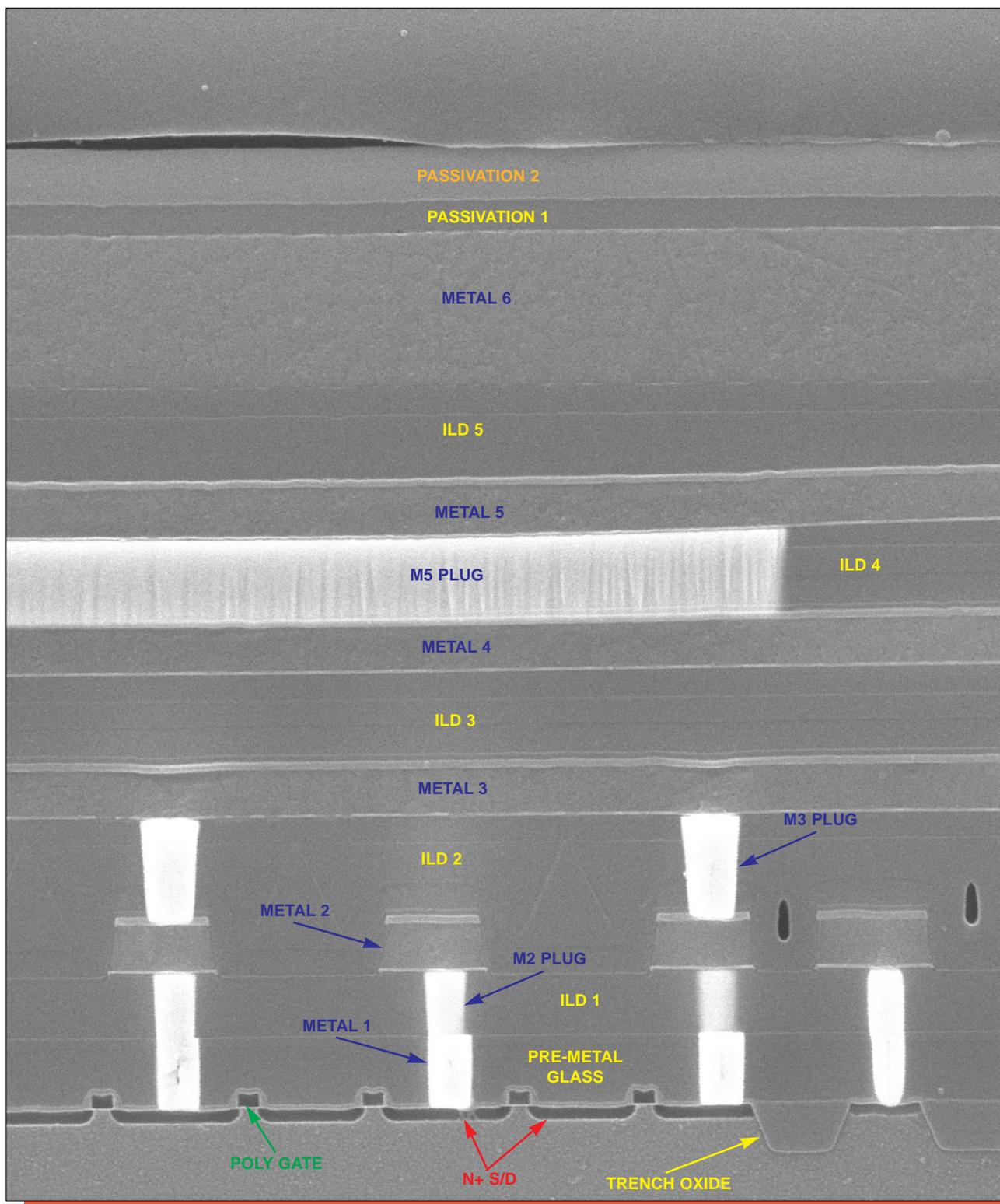
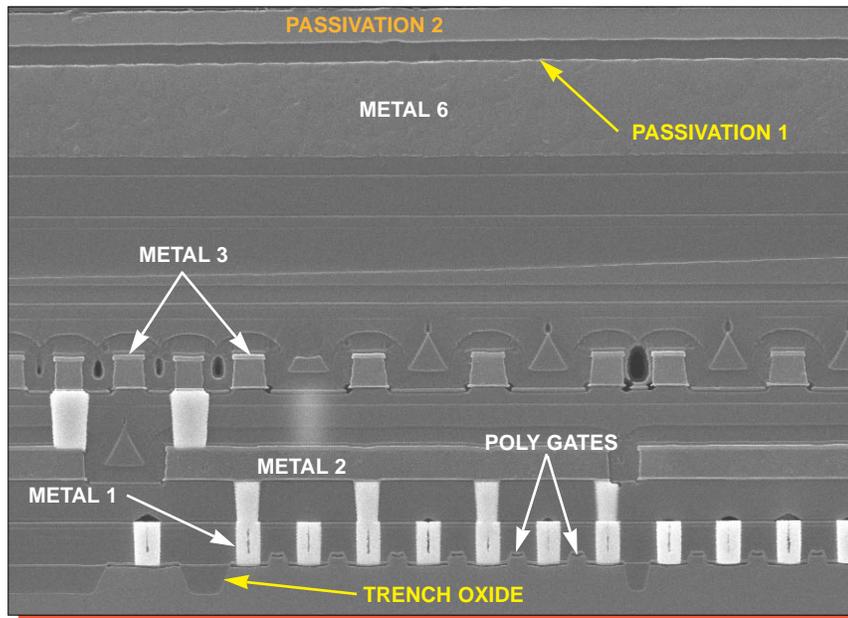
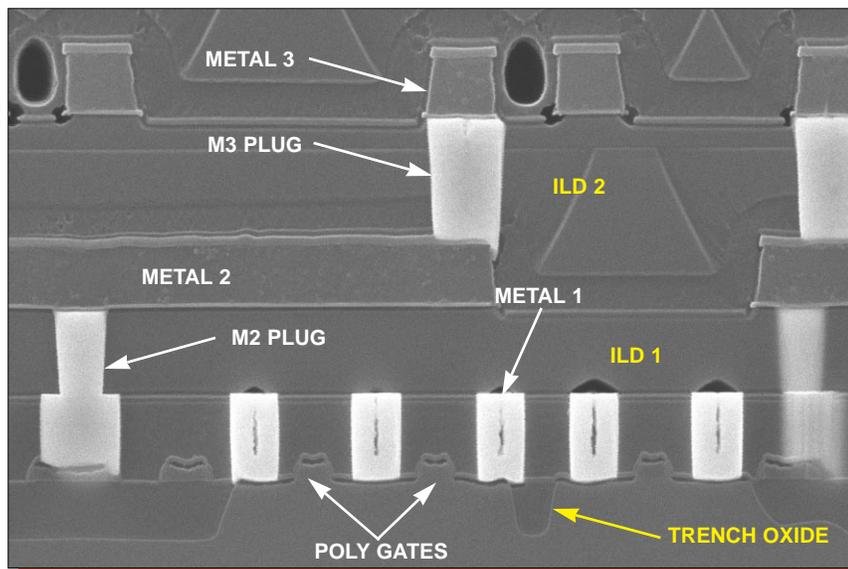


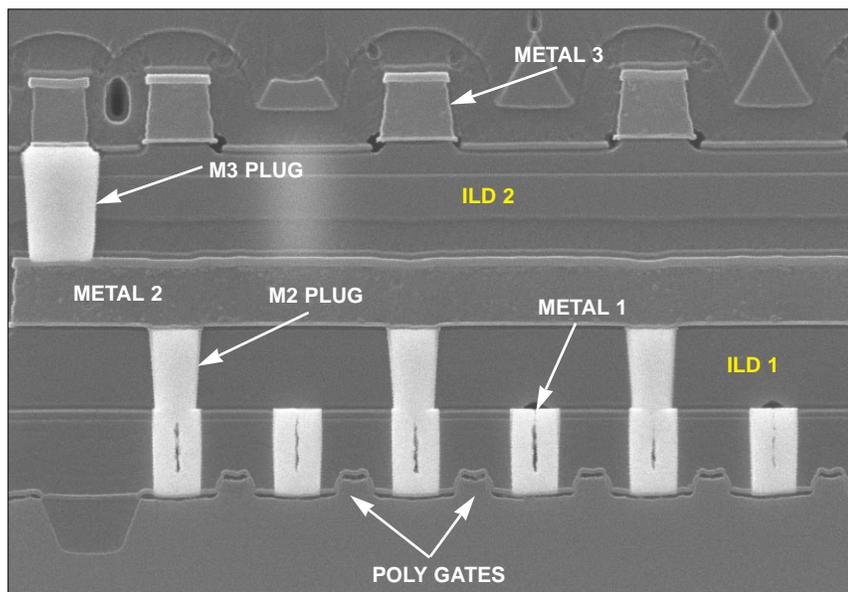
Figure 7a. Detailed SEM section view of general device structure. Mag. 14,300x.



Mag. 6500x



Mag. 13,000x



Mag. 13,000x

Figure 8. Glass etch section views illustrating general structure.

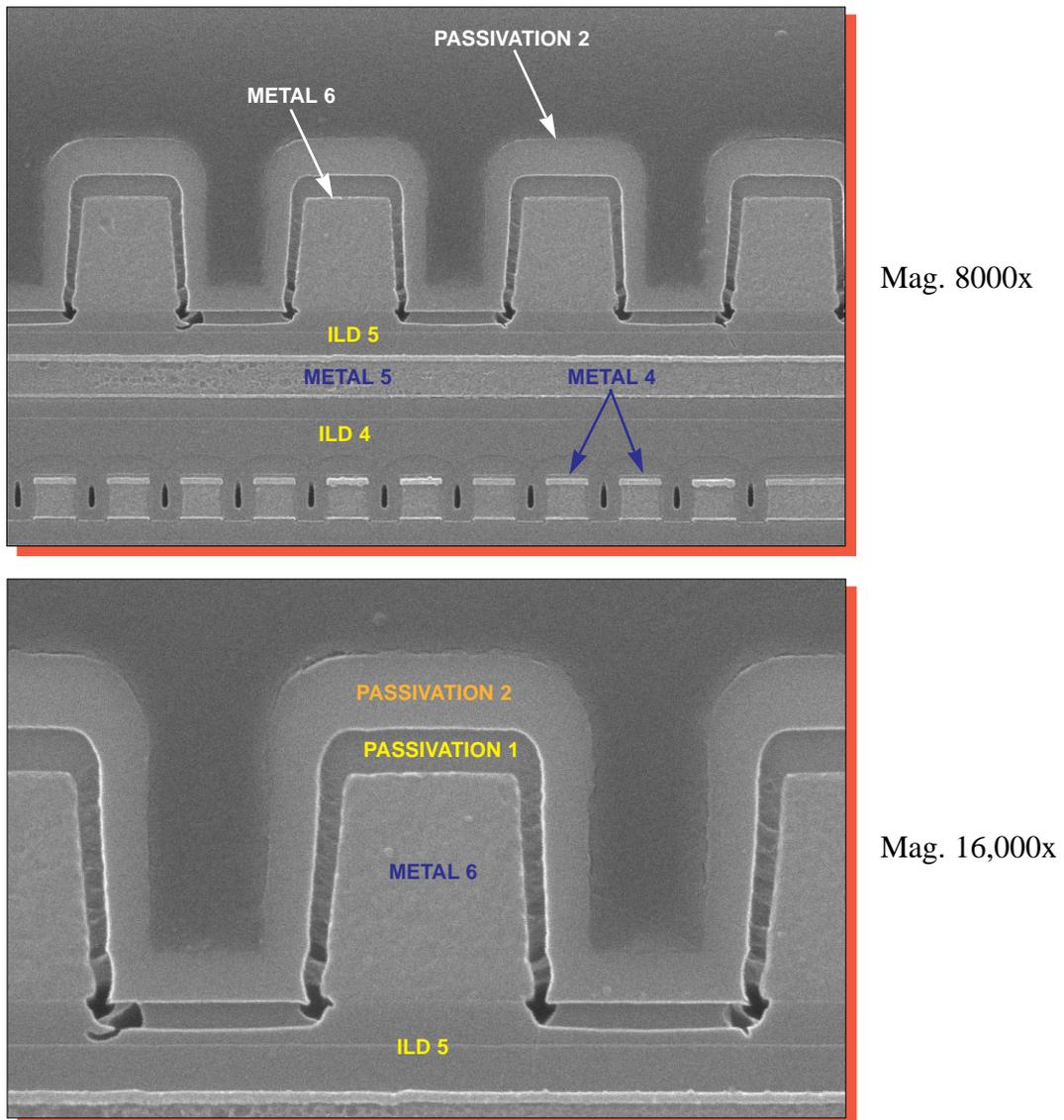


Figure 9. SEM section views of metal 6 line profiles.

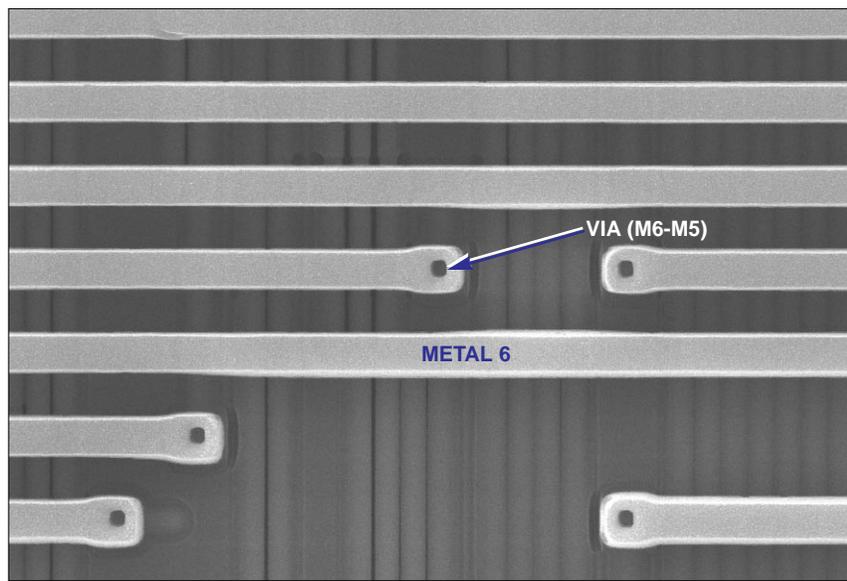
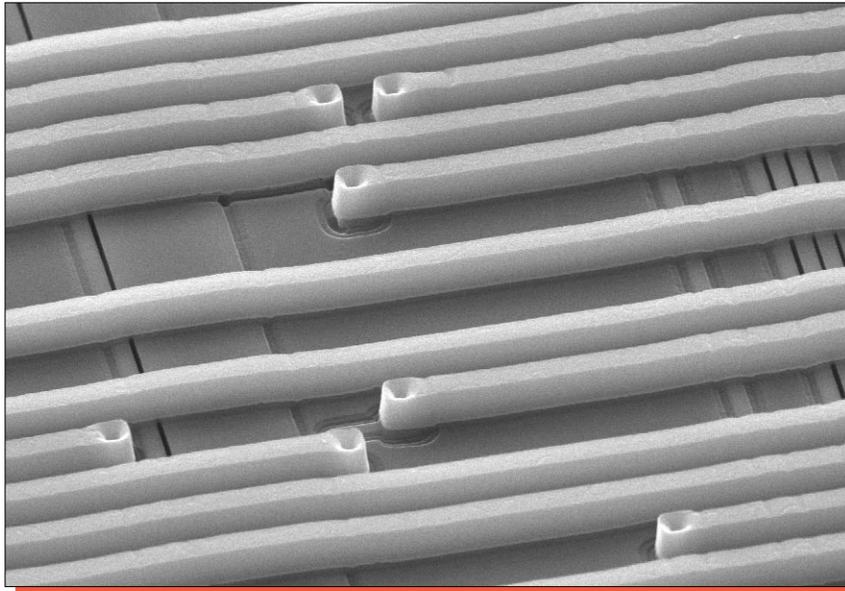
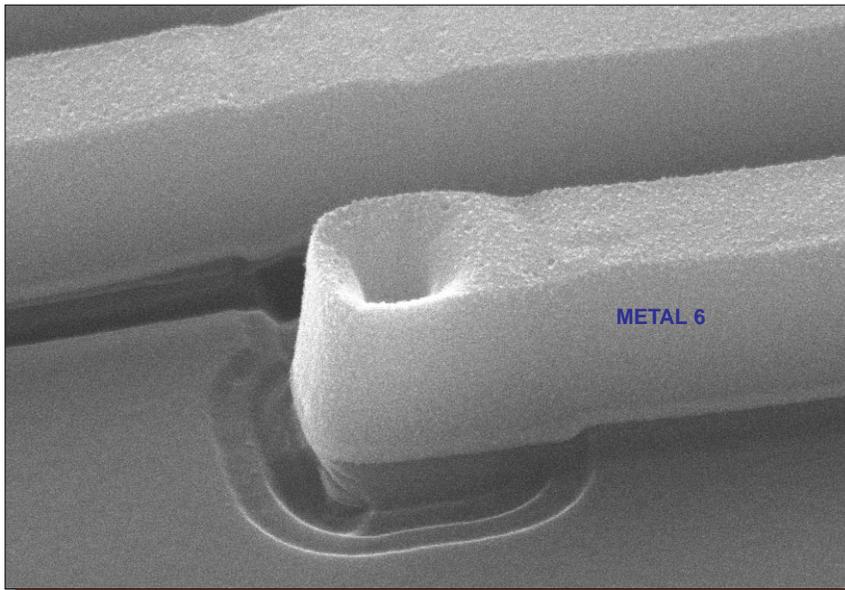


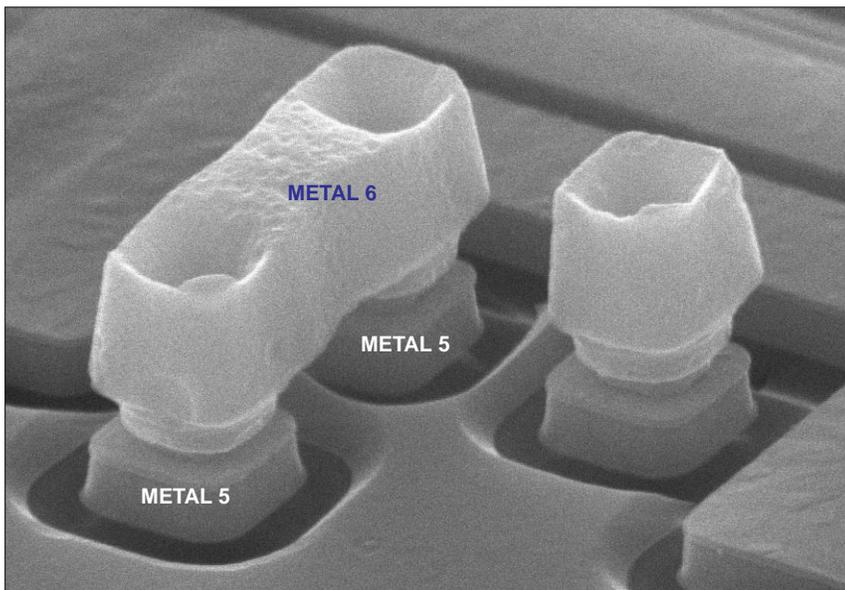
Figure 10. Topological SEM view of metal 6 patterning. Mag. 3000x, 0°.



Mag. 2500x

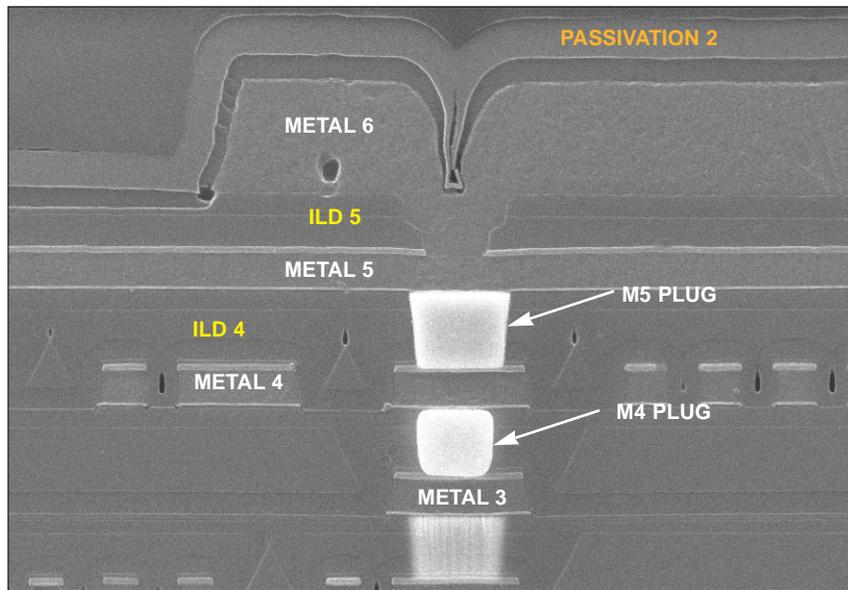


Mag. 12,400x

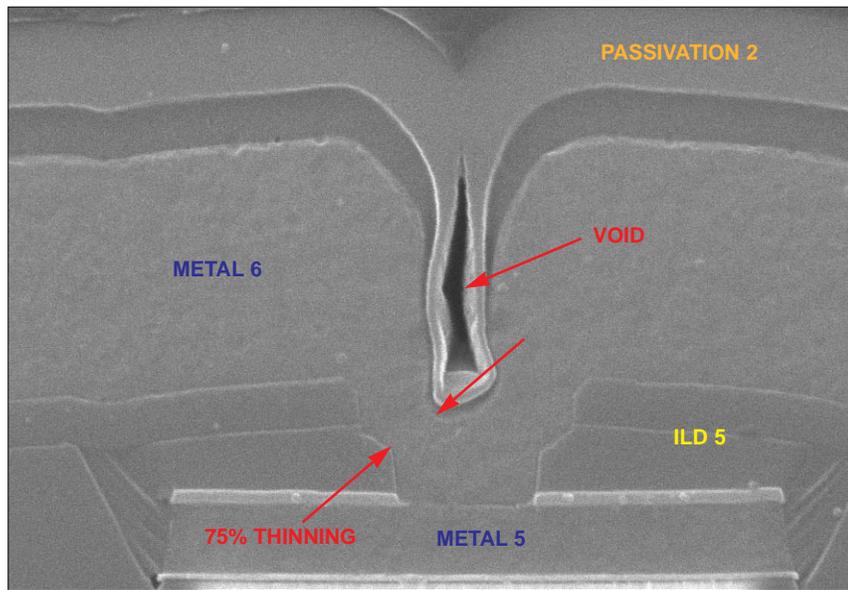


Mag. 12,000x

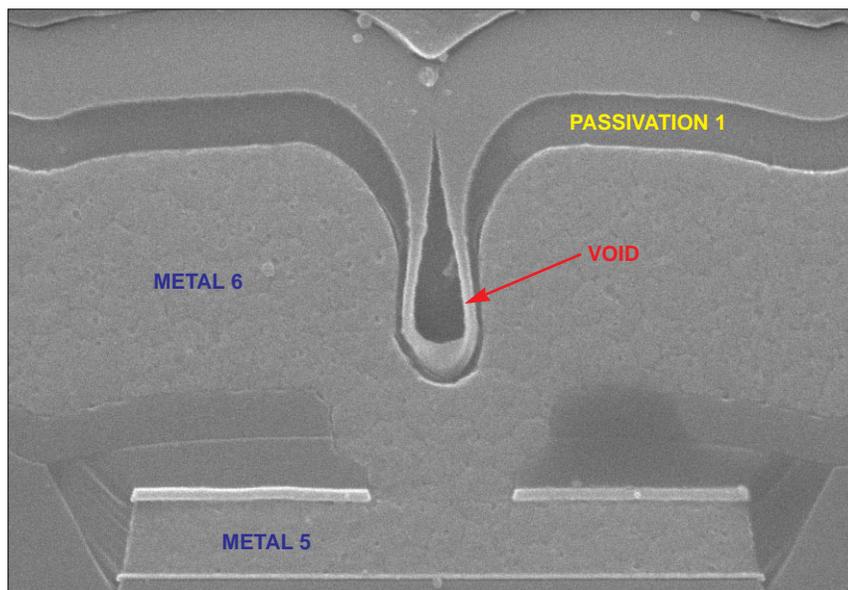
Figure 11. SEM views of general metal 6 integrity. 55°.



Mag. 8000x



Mag. 17,600x



Mag. 17,600x

Figure 12. SEM section views of metal 6-to-metal 5 vias.

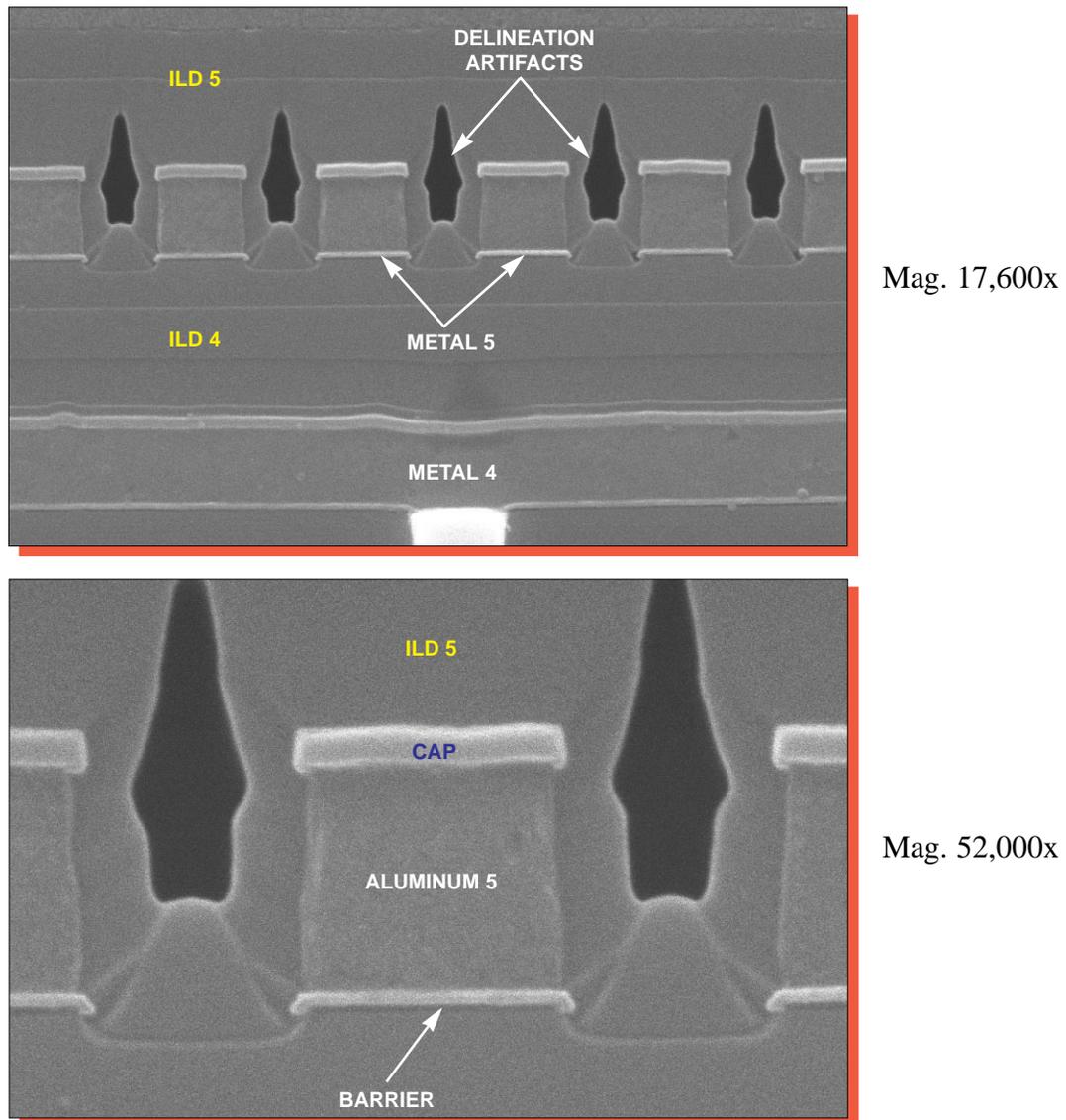


Figure 13. SEM section views of metal 5 line profiles.

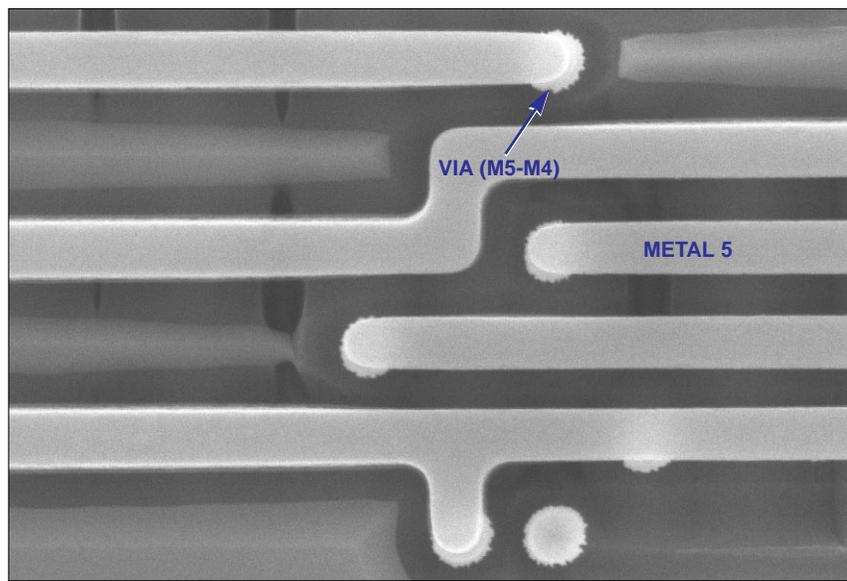
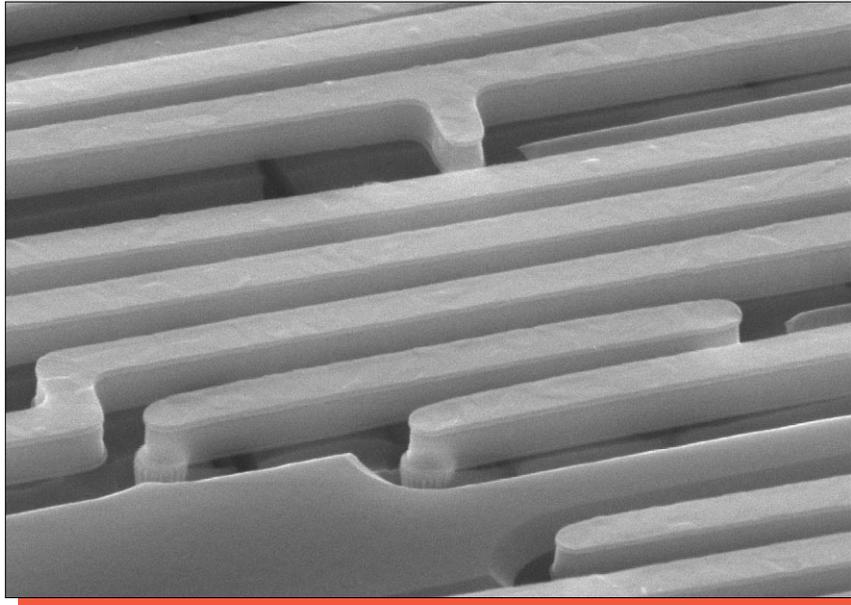
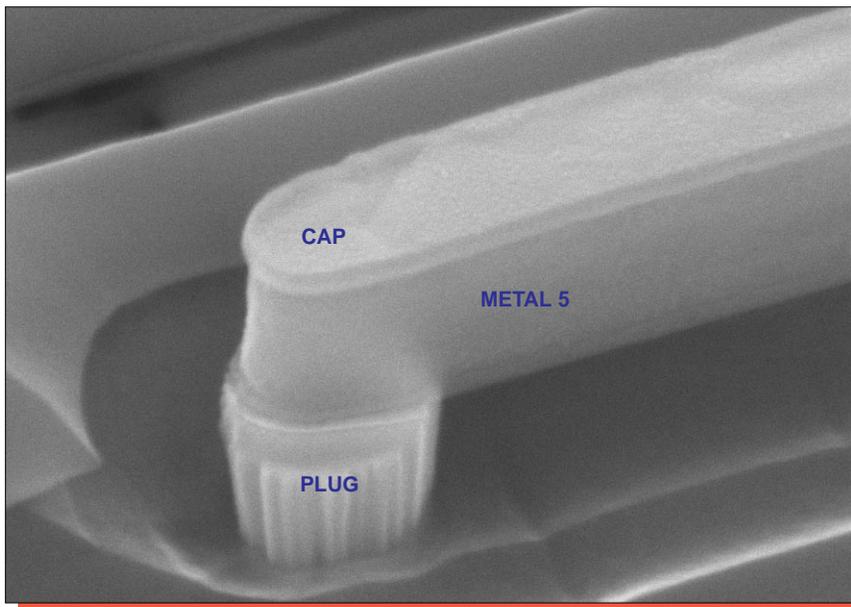


Figure 14. Topological SEM view of metal 5 patterning. Mag. 10,000x, 0°.

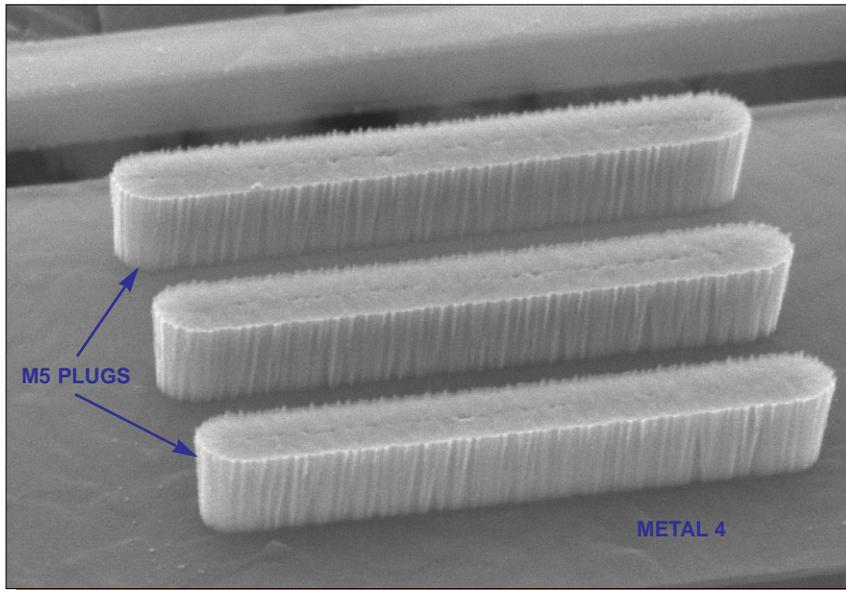


Mag. 9000x

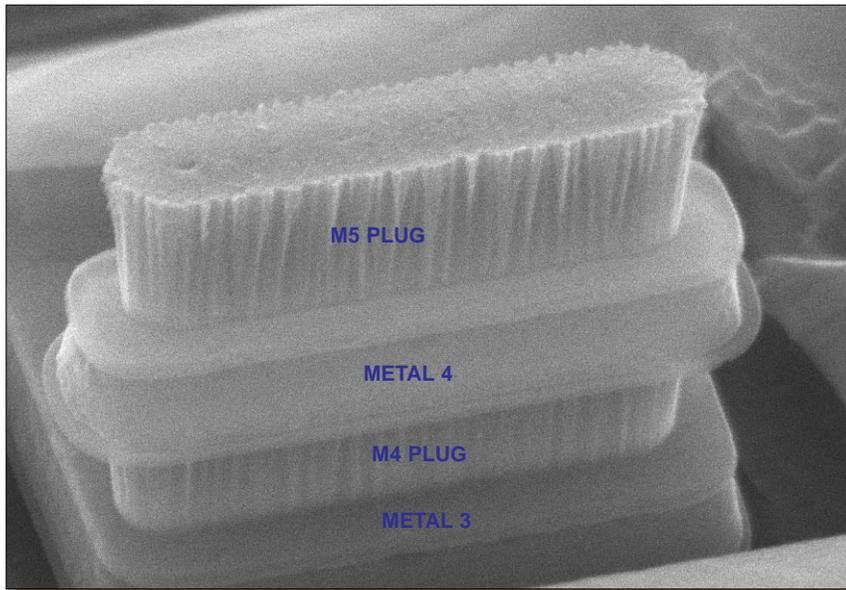


Mag. 35,000x

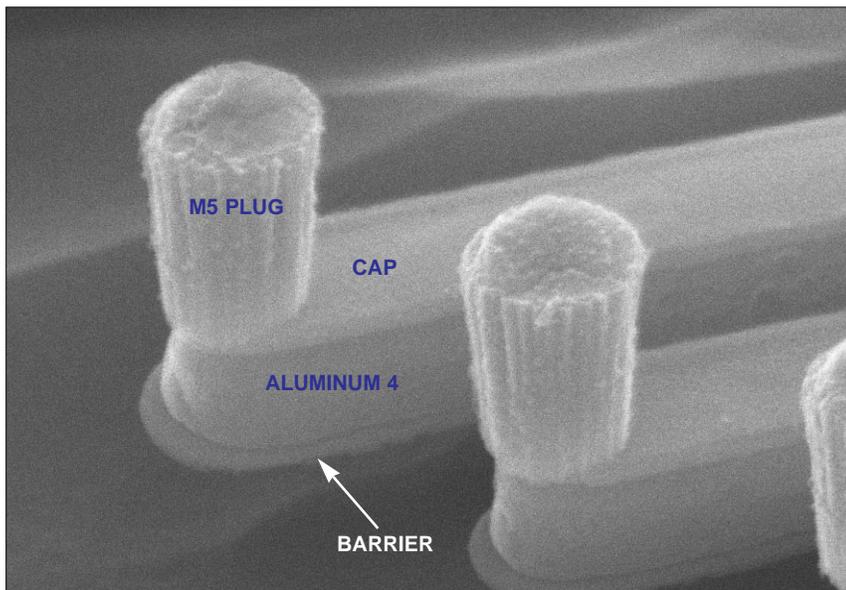
Figure 15. SEM views of general metal 5 integrity. 55°.



Mag. 13,500x



Mag. 22,000x



Mag. 30,000x

Figure 16. SEM views of metal 5 tungsten plugs. 55°.

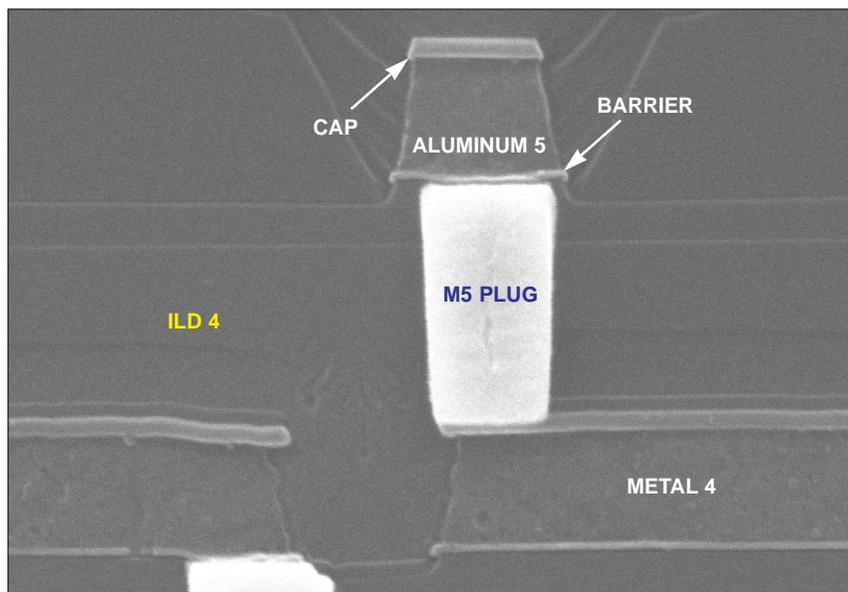
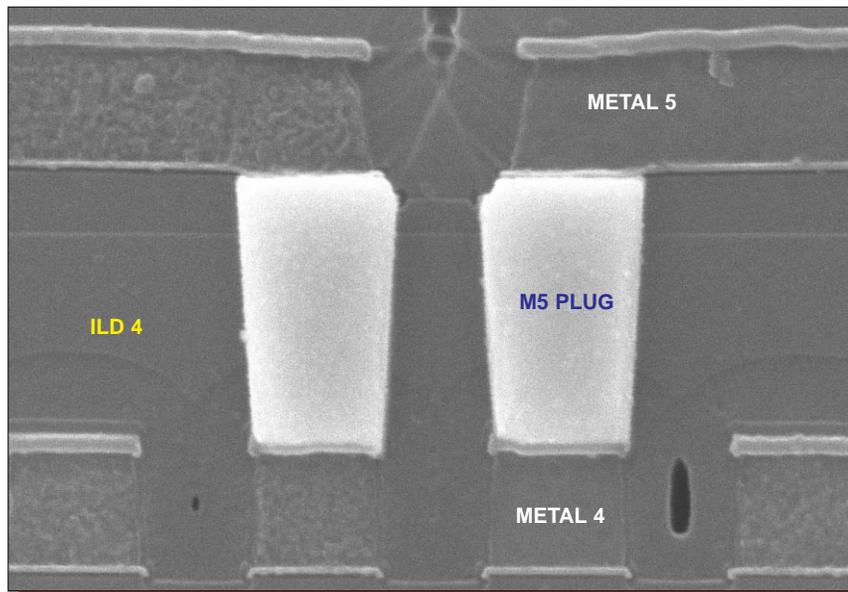
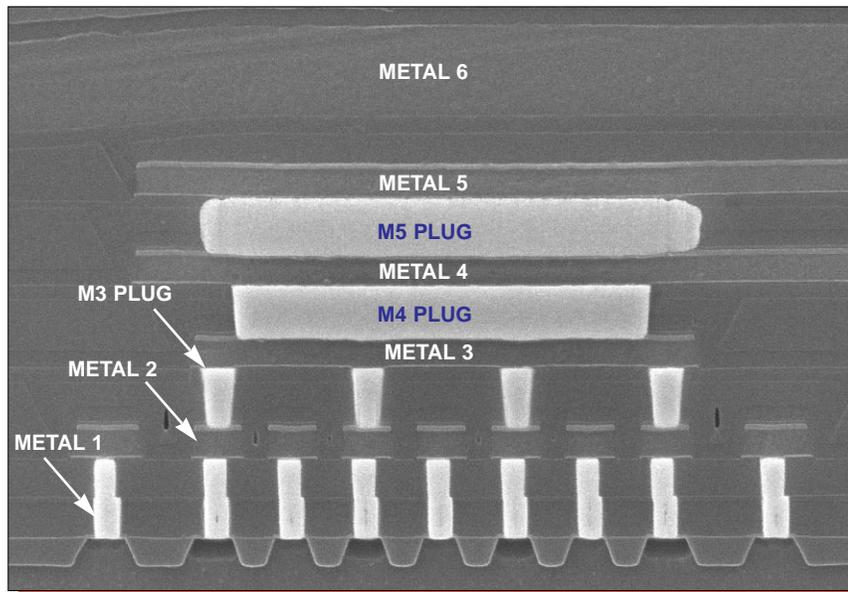
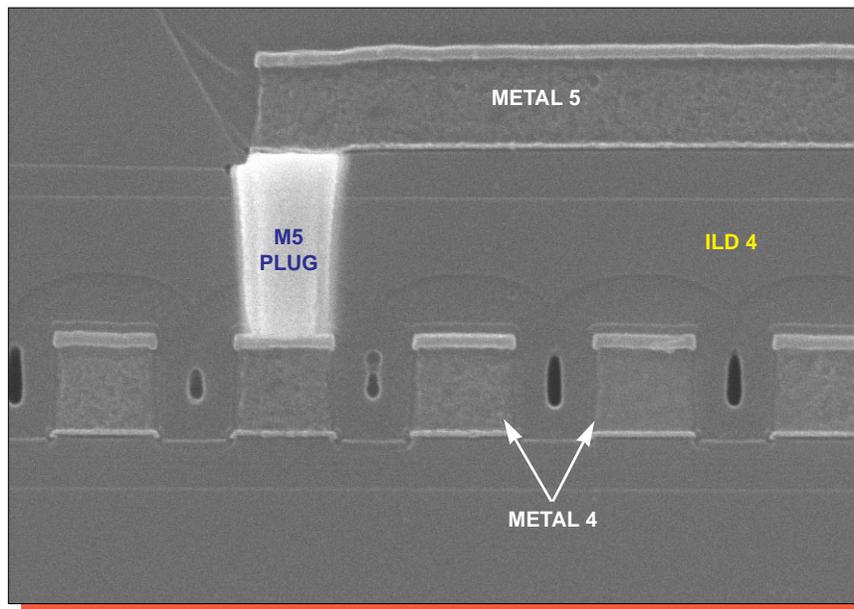
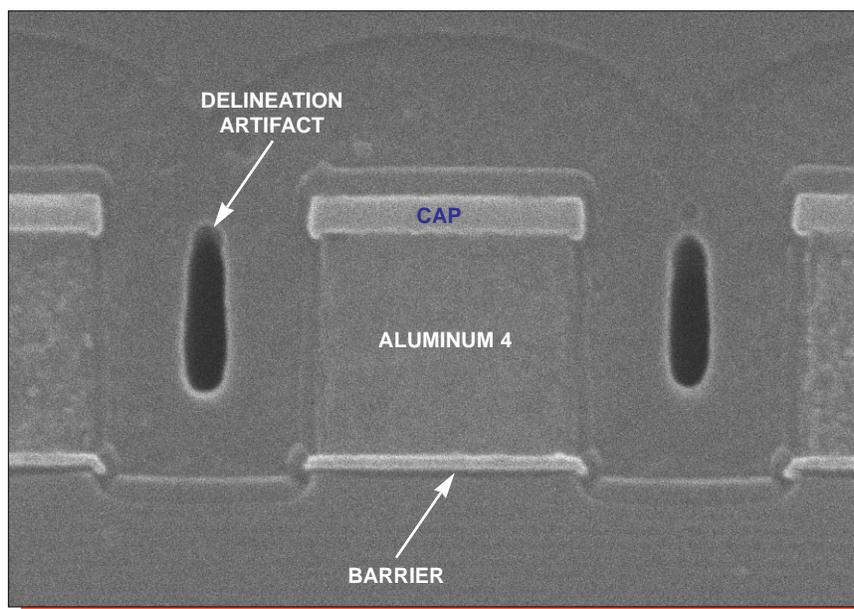


Figure 17. SEM section views of metal 5-to-metal 4 vias.

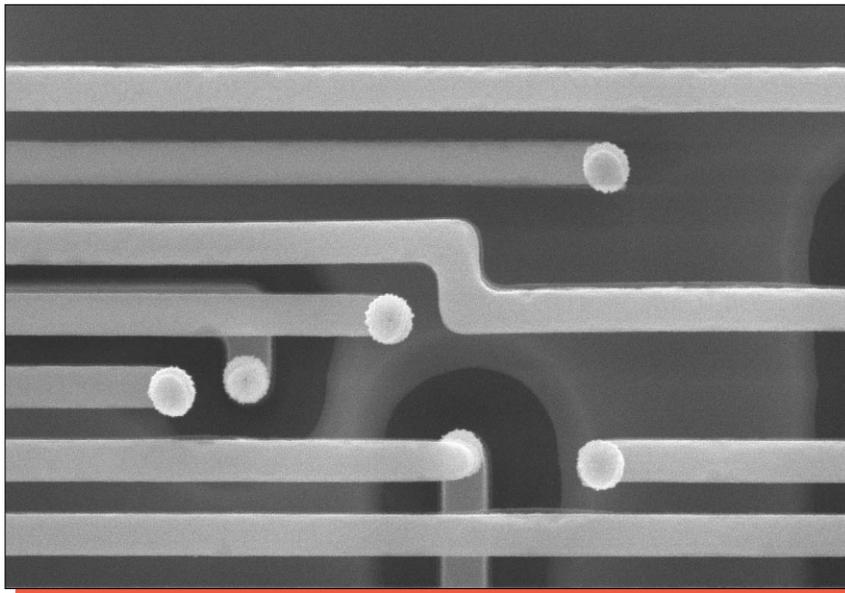


Mag. 20,000x

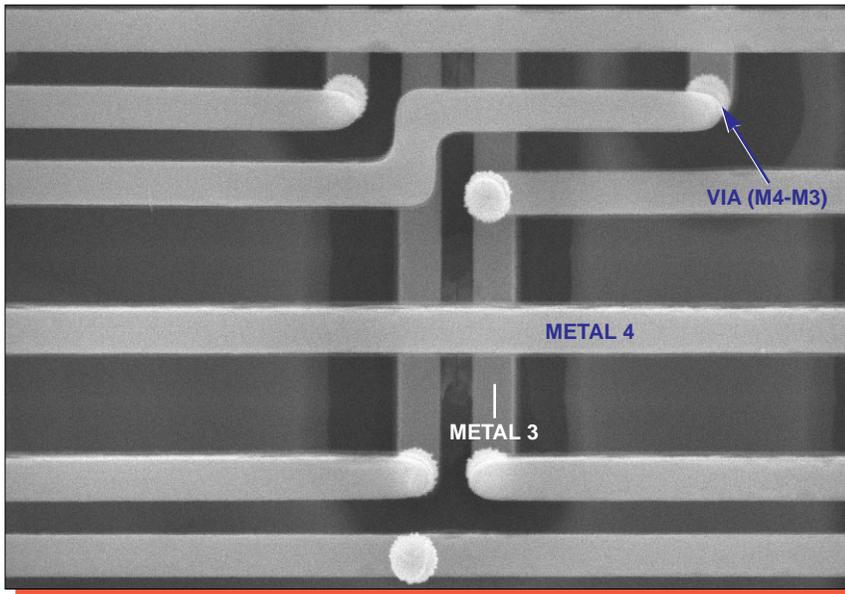


Mag. 52,000x

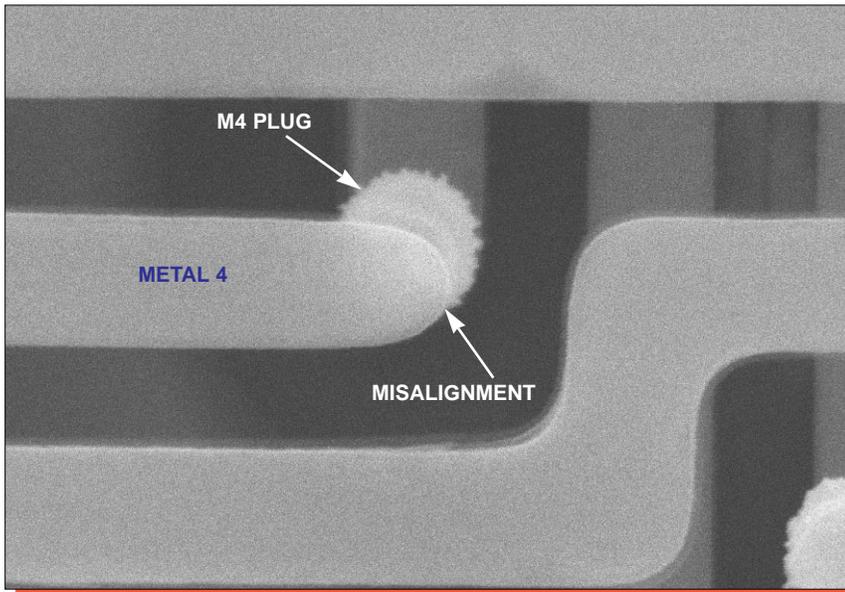
Figure 18. SEM section views of metal 4 line profiles.



Mag. 8000x

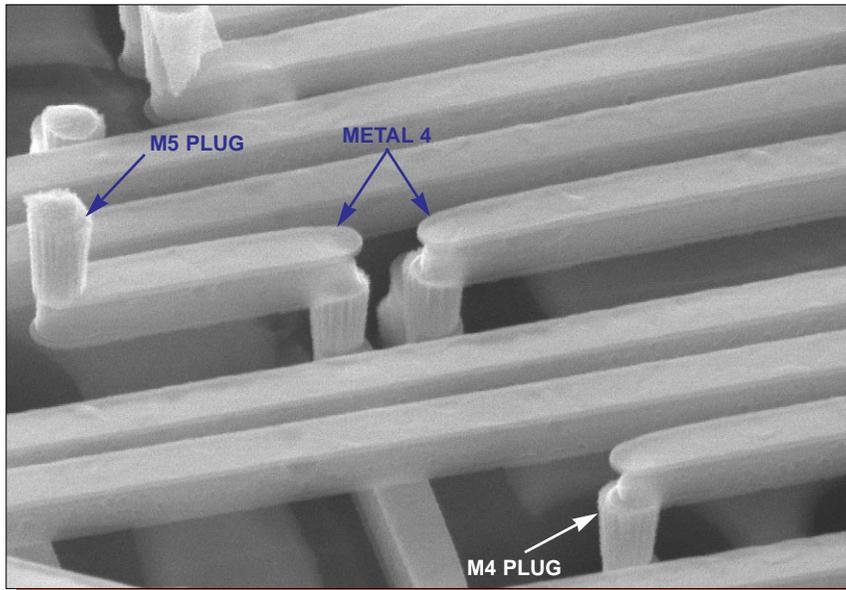


Mag. 8000x

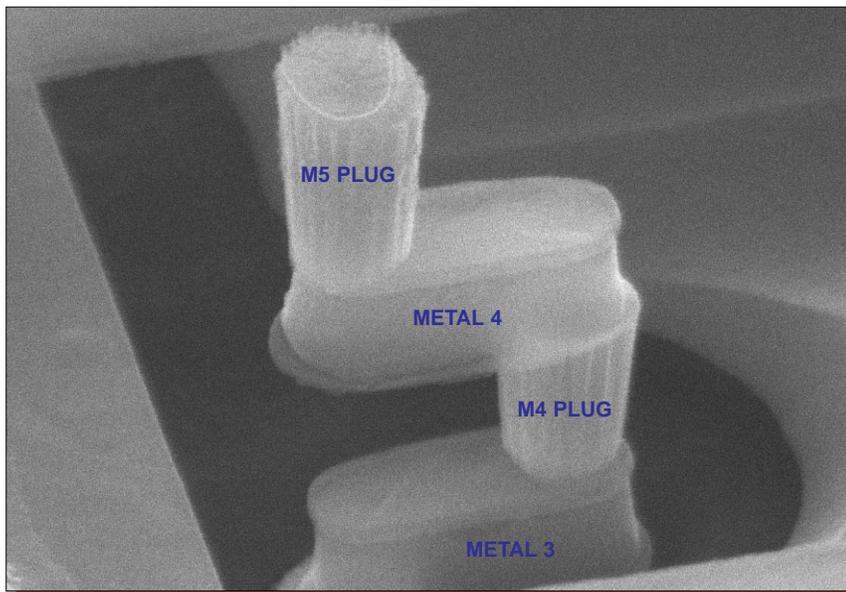


Mag. 25,000x

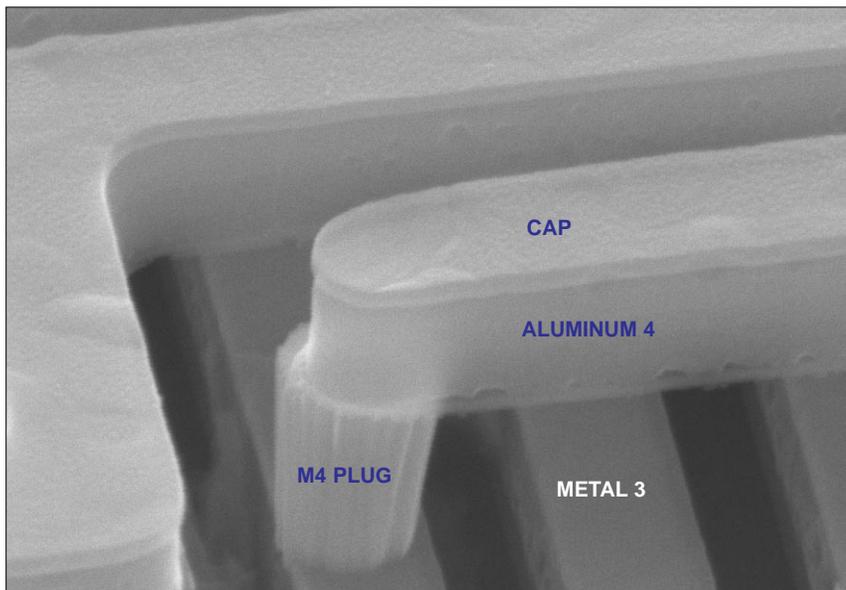
Figure 19. Topological SEM views of metal 4 patterning. 0°.



Mag. 11,000x

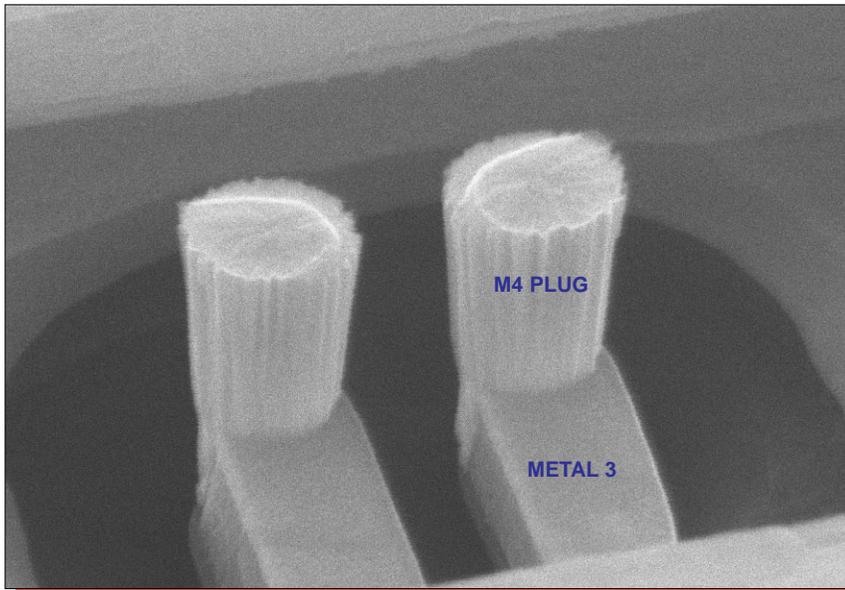


Mag. 25,000x

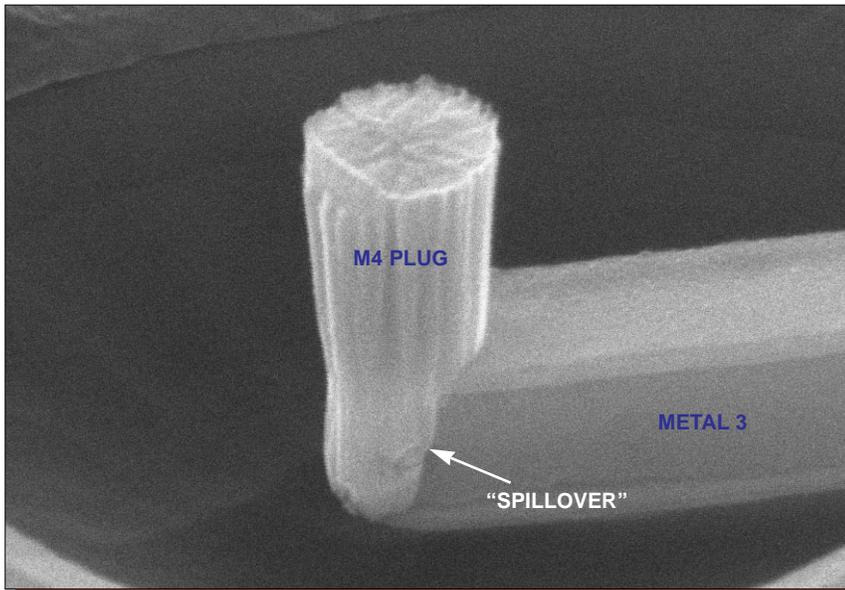


Mag. 30,000x

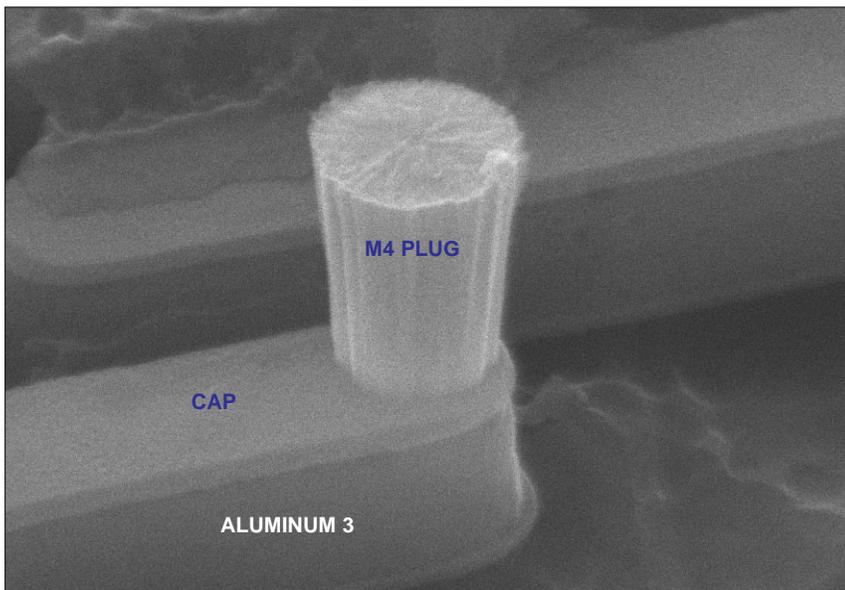
Figure 20. SEM views of general metal 4 integrity. 55°.



Mag. 30,000x

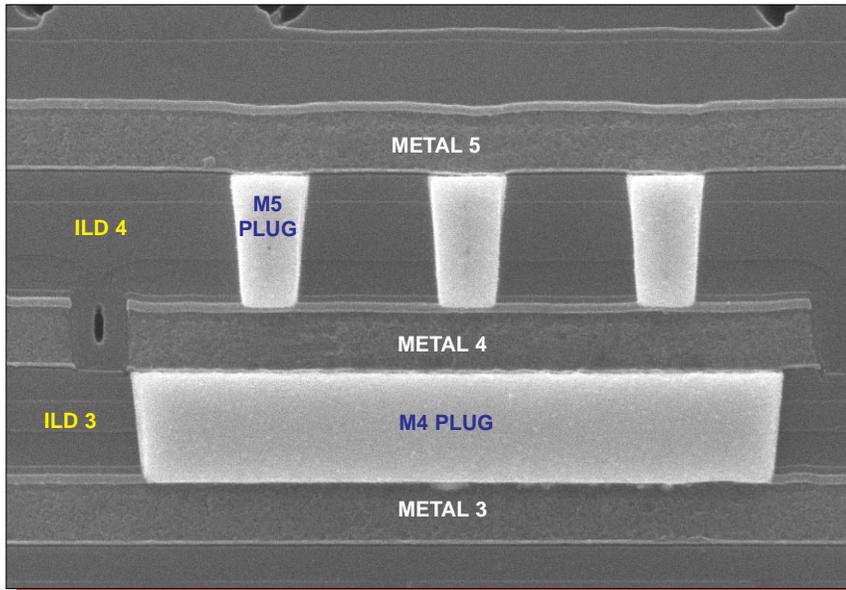


Mag. 32,000x

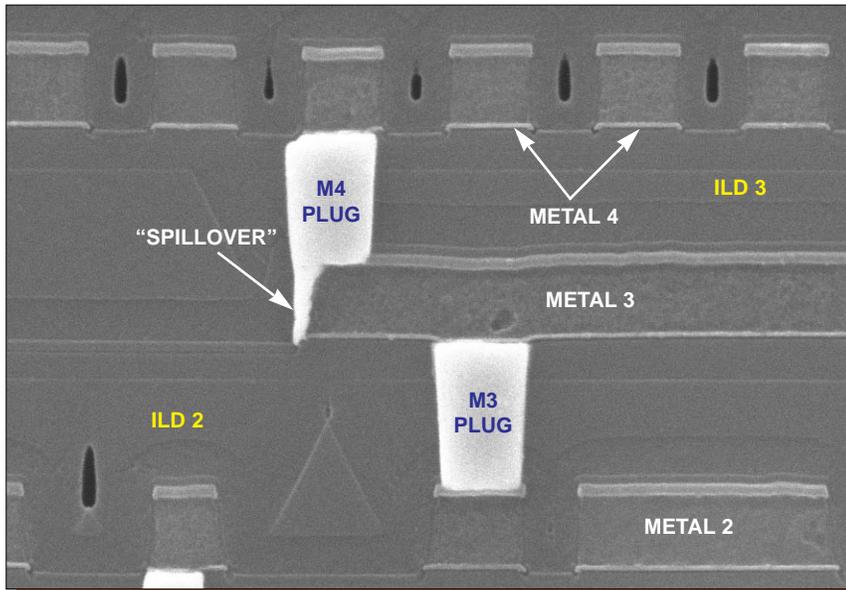


Mag. 35,000x

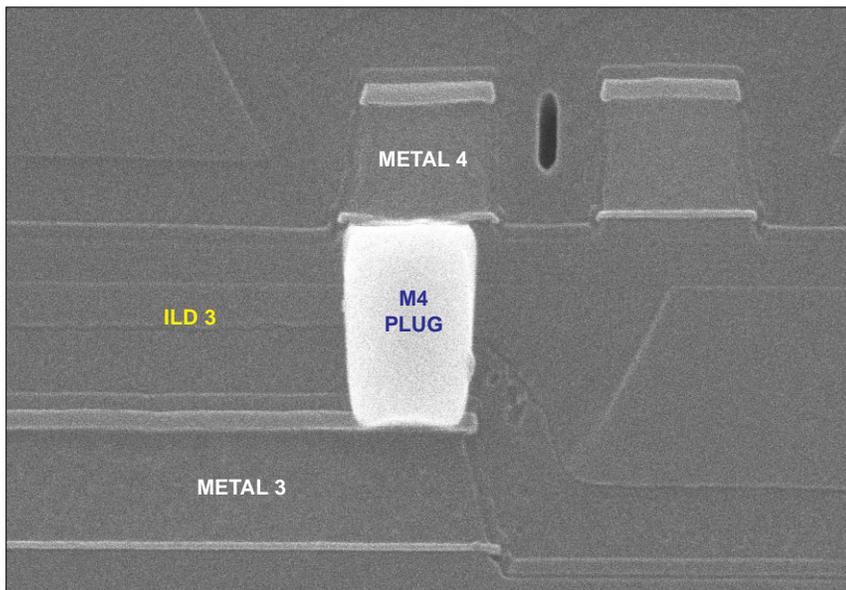
Figure 21. SEM views of metal 4 tungsten plugs. 55°.



Mag. 13,000x



Mag. 16,000x



Mag. 26,000x

Figure 22. SEM section views of metal 4-to-metal 3 vias.

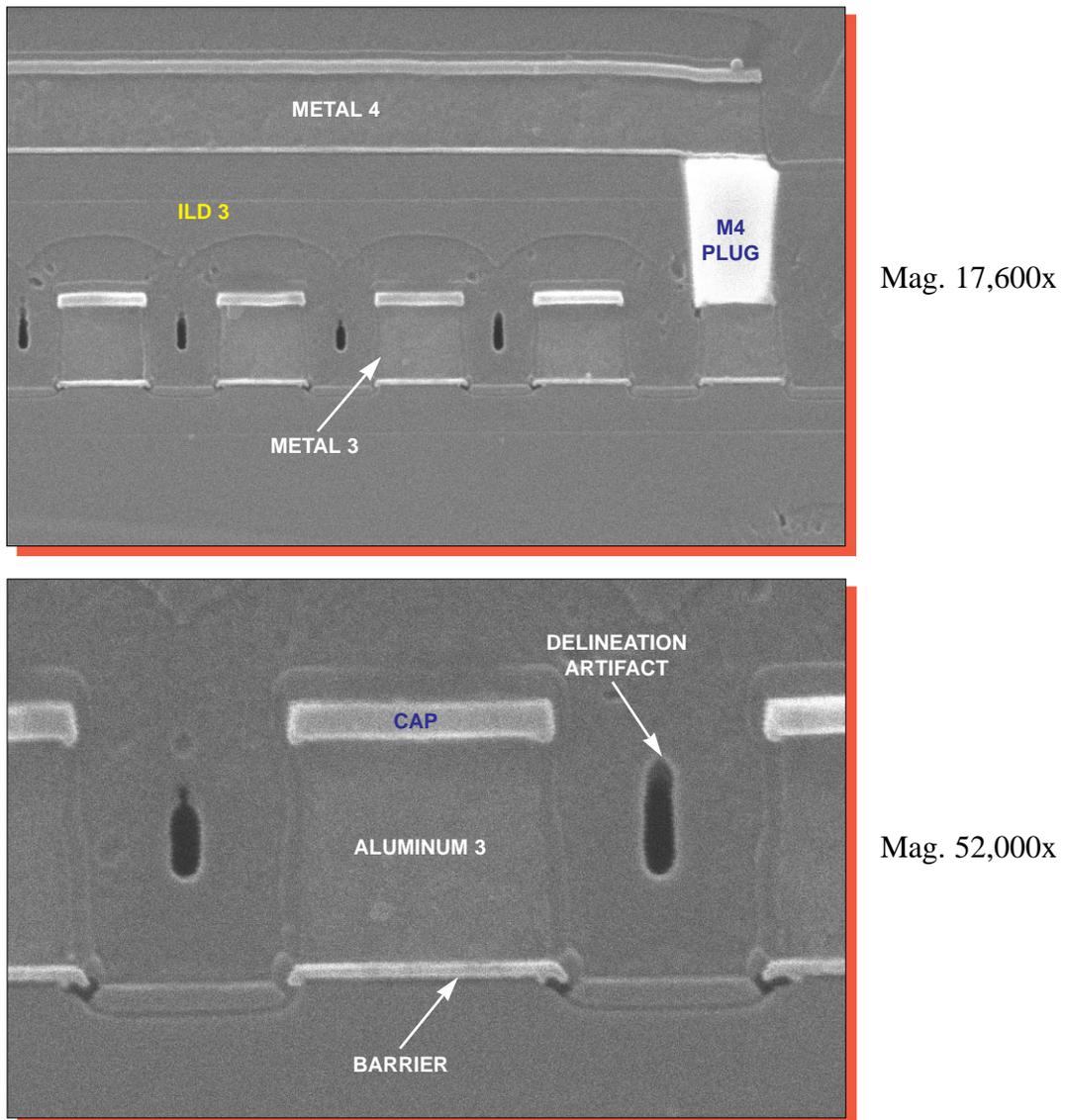


Figure 23. SEM section views of metal 3 line profiles.

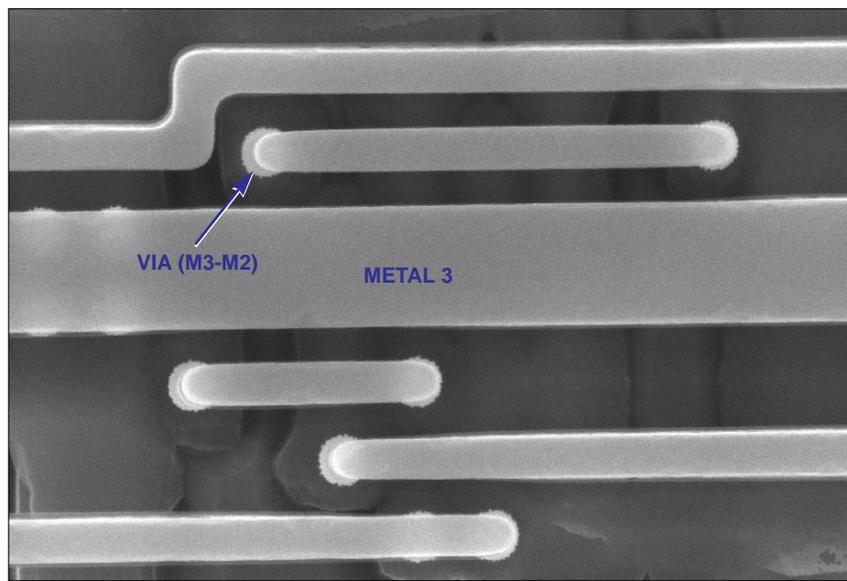
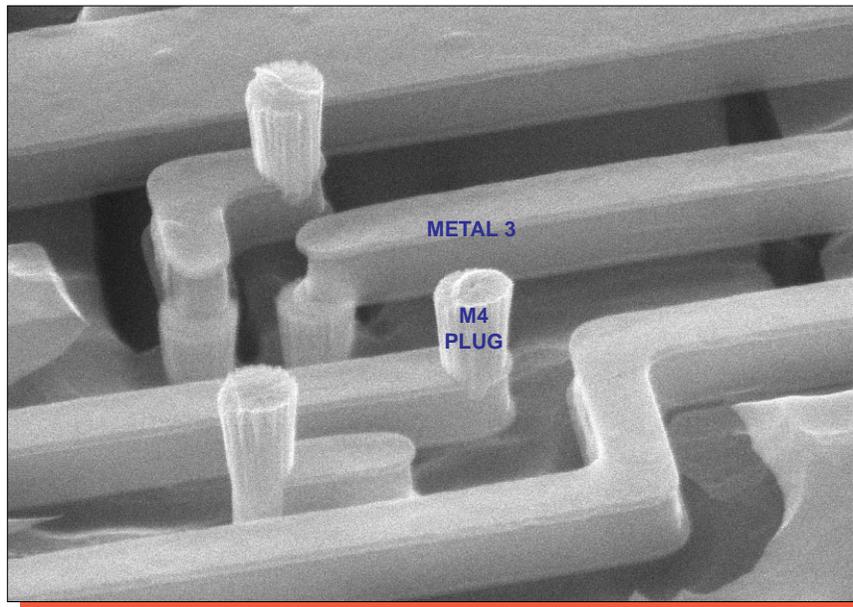
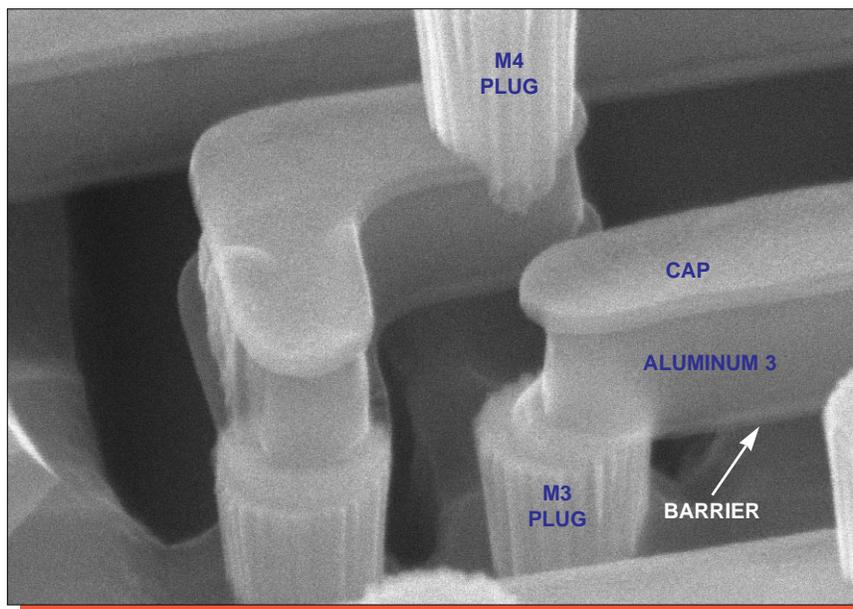


Figure 24. Topological SEM view of metal 3 patterning. Mag. 8000x, 0°.

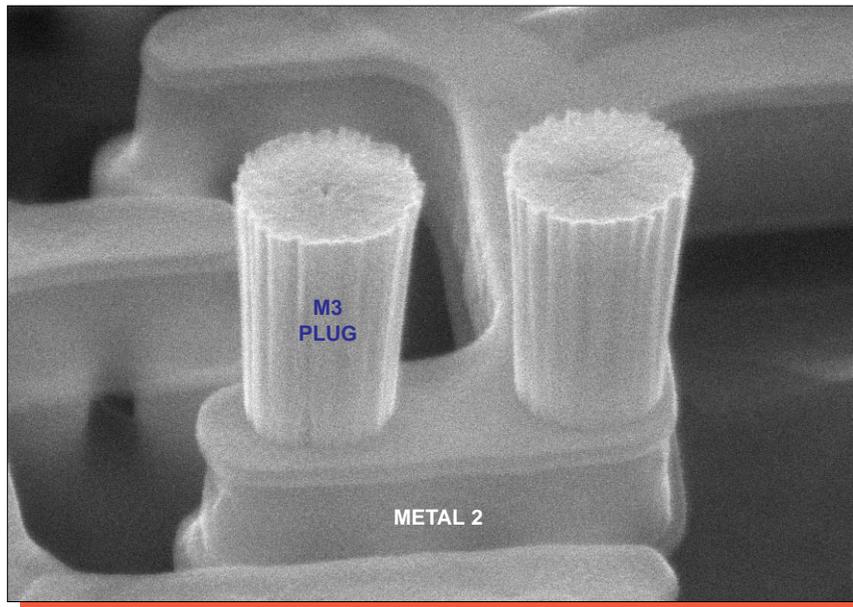


Mag. 13,000x

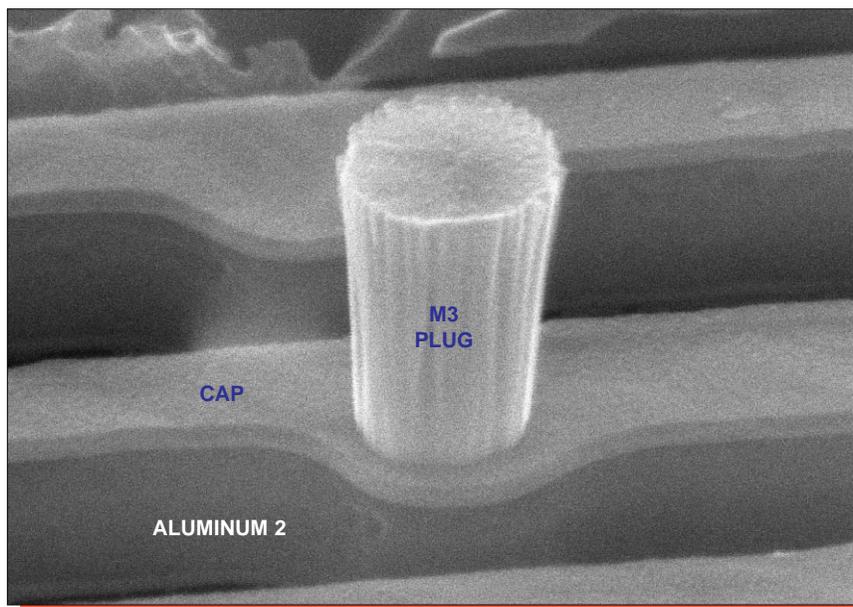


Mag. 30,000x

Figure 25. SEM views of general metal 3 integrity. 55°.

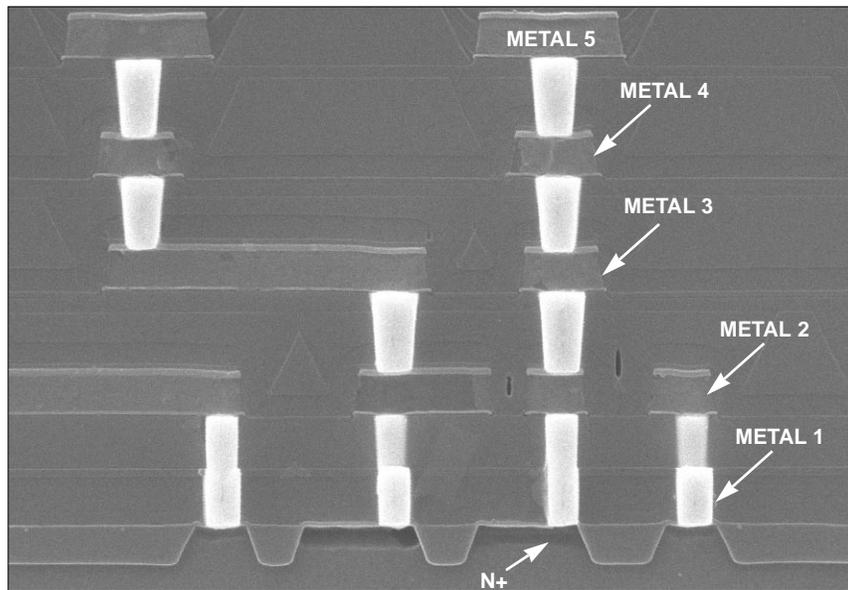


Mag. 30,000x

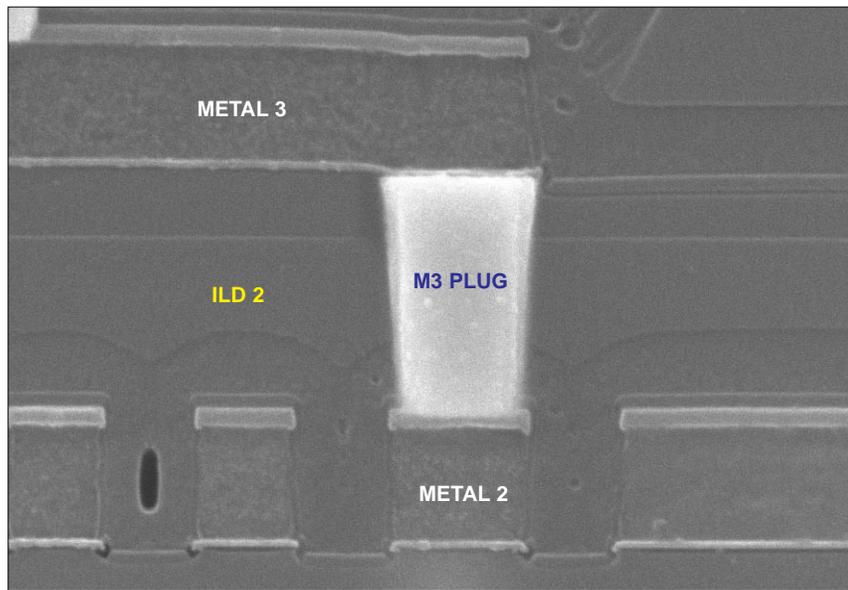


Mag. 35,000x

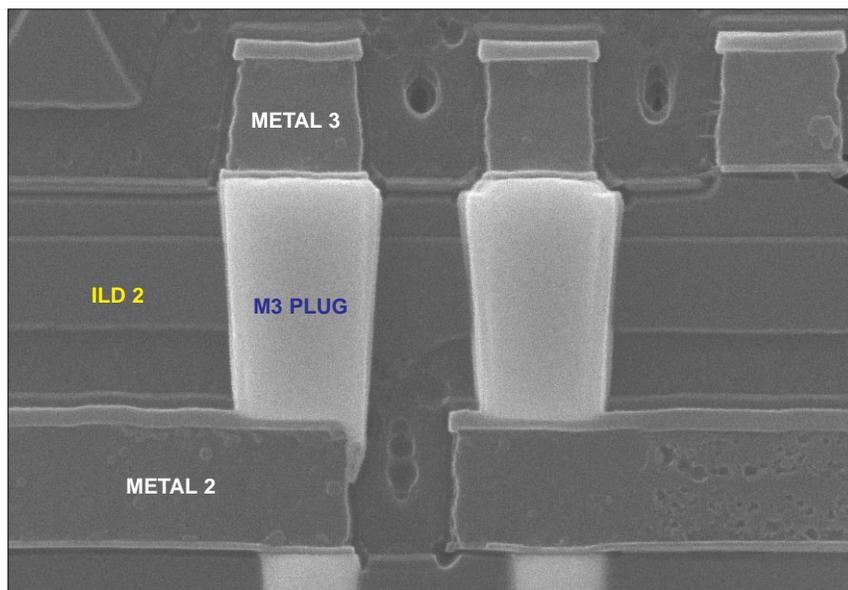
Figure 26. SEM views of metal 3 tungsten plugs. 55°.



Mag. 9000x

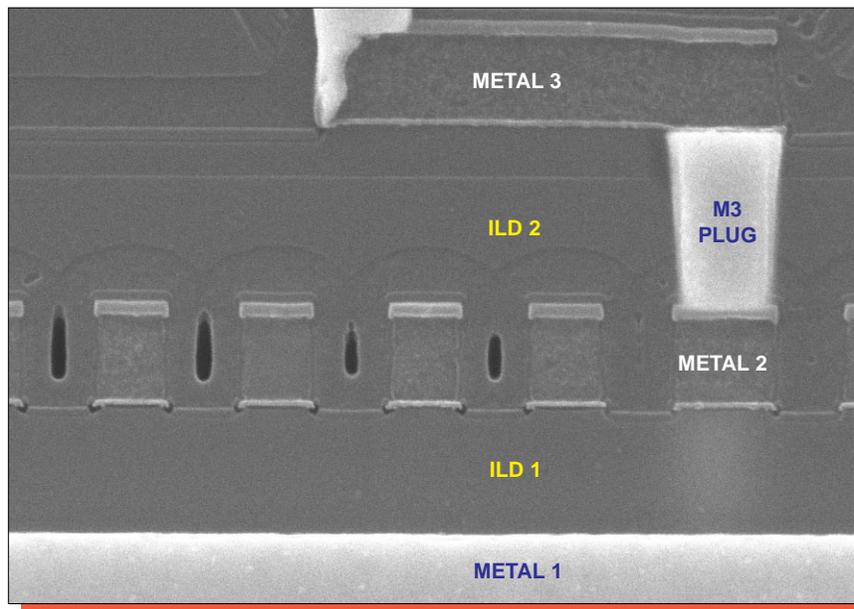


Mag. 26,000x

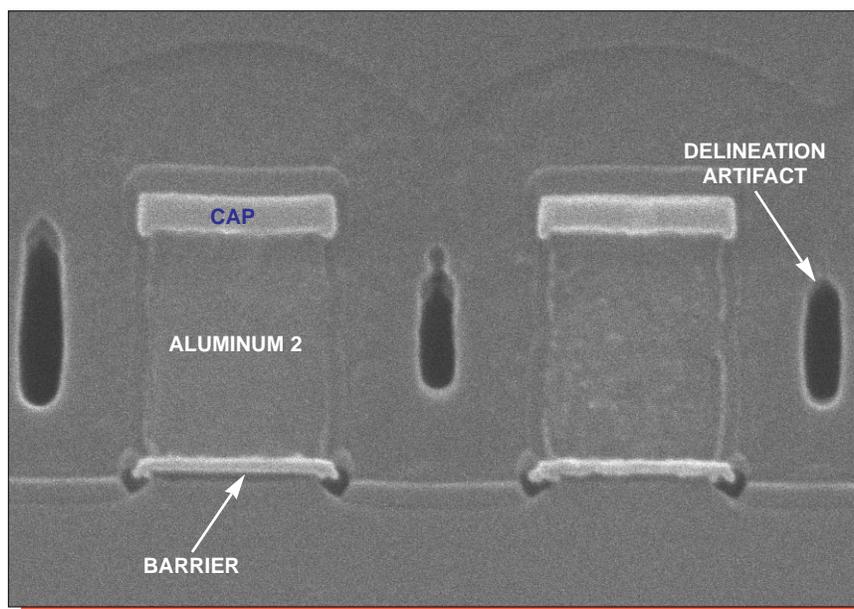


Mag. 26,000x

Figure 27. SEM section views of metal 3-to-metal 2 vias.

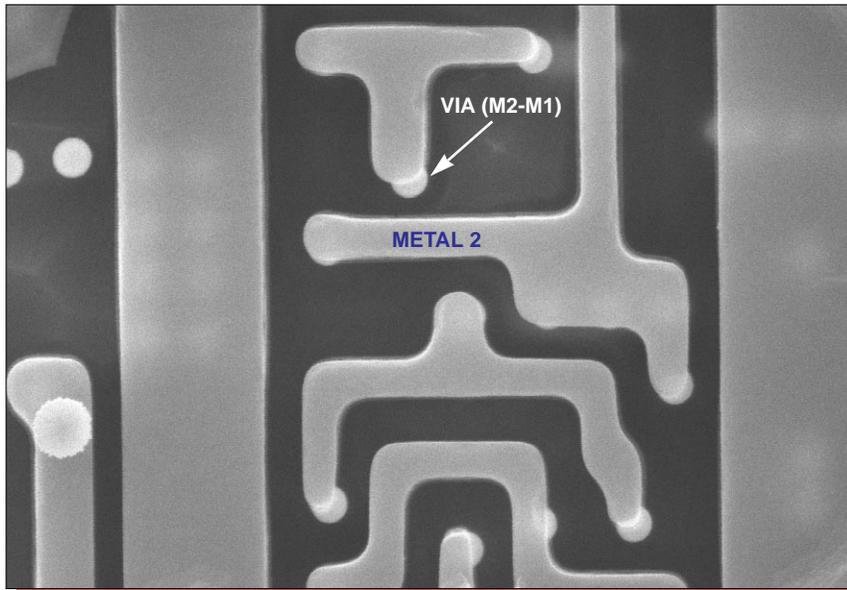


Mag. 20,000x

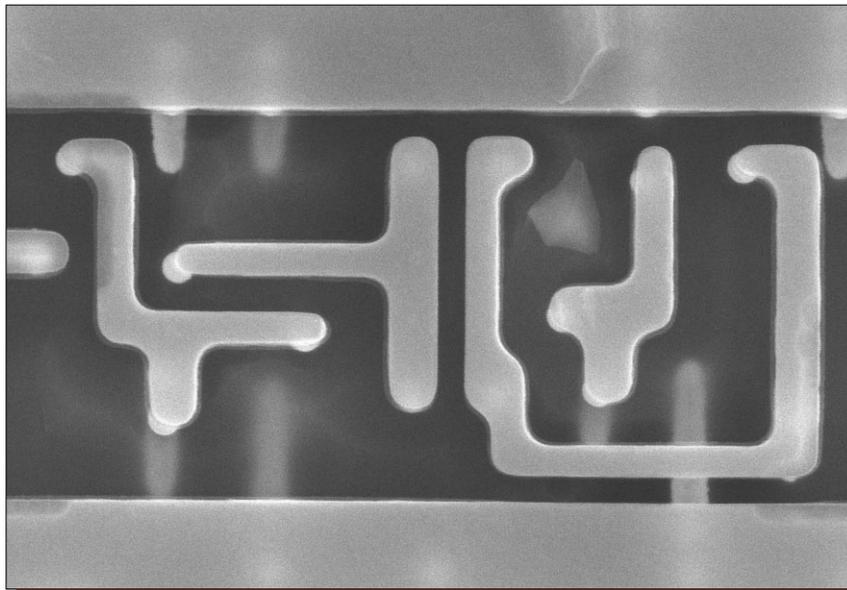


Mag. 52,000x

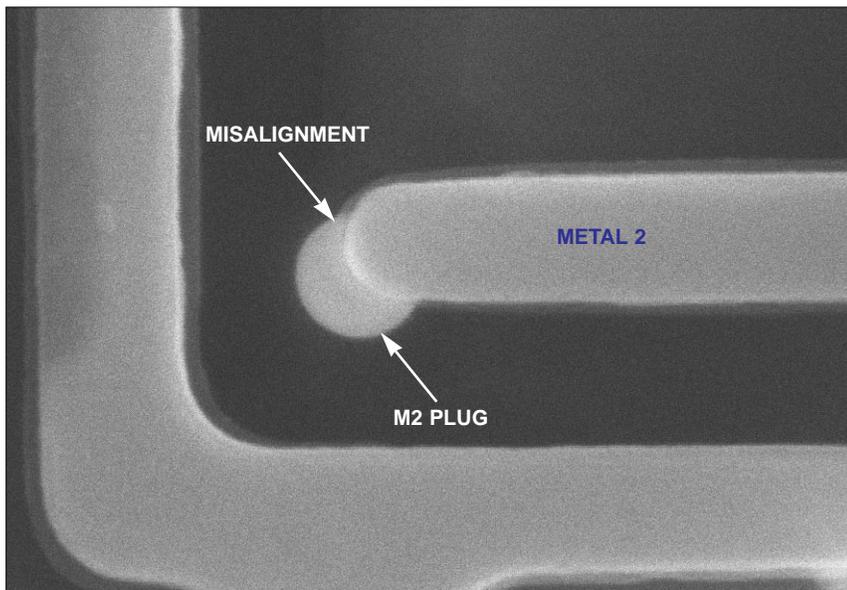
Figure 28. SEM section views of metal 2 line profiles.



Mag. 9000x

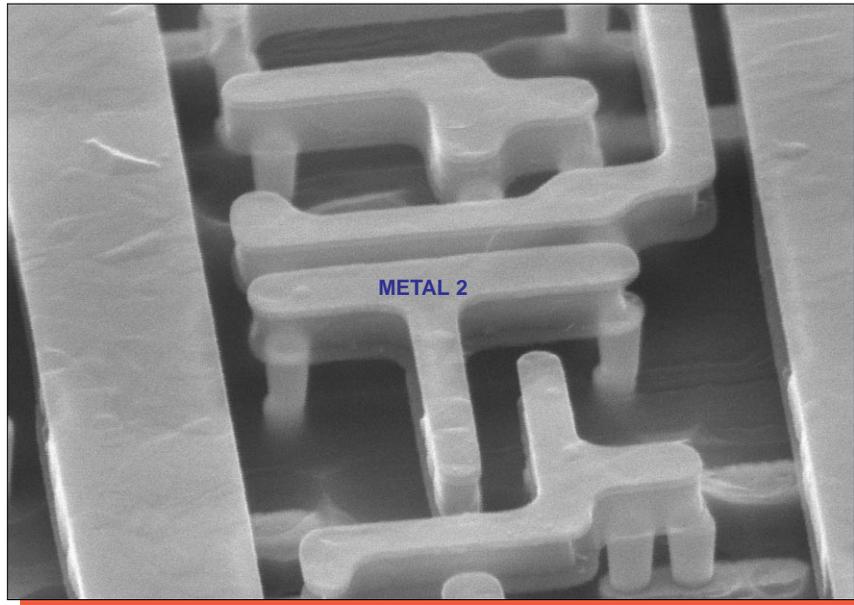


Mag. 8000x

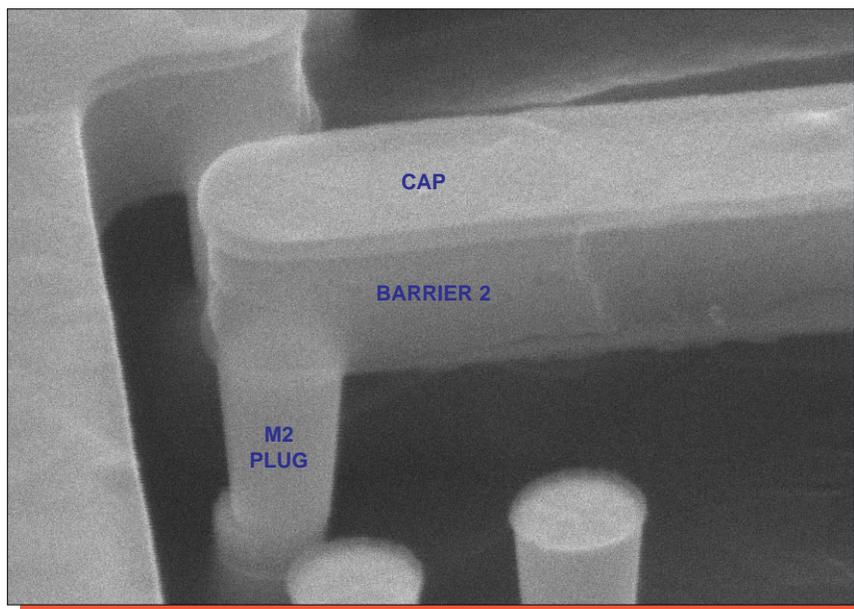


Mag. 32,000x

Figure 29. Topological views of metal 2 patterning. 0°.

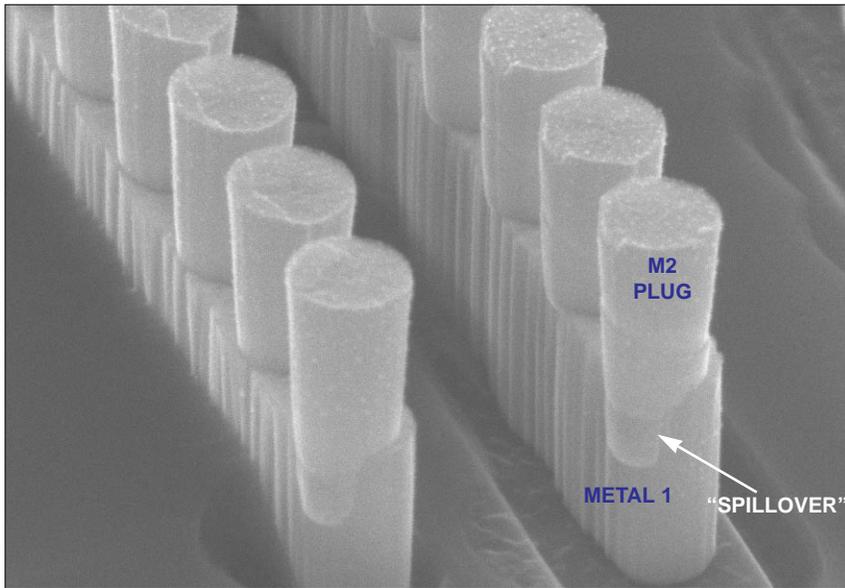


Mag. 11,000x

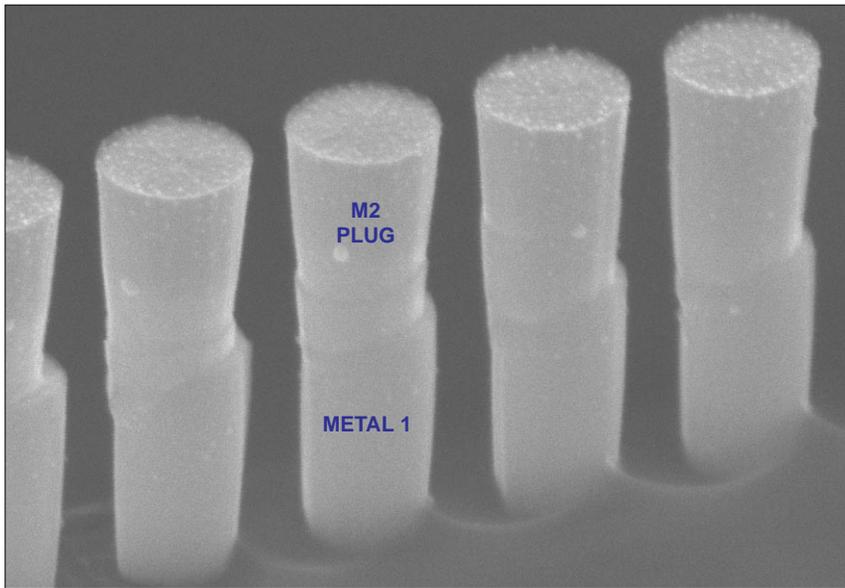


Mag. 31,000x

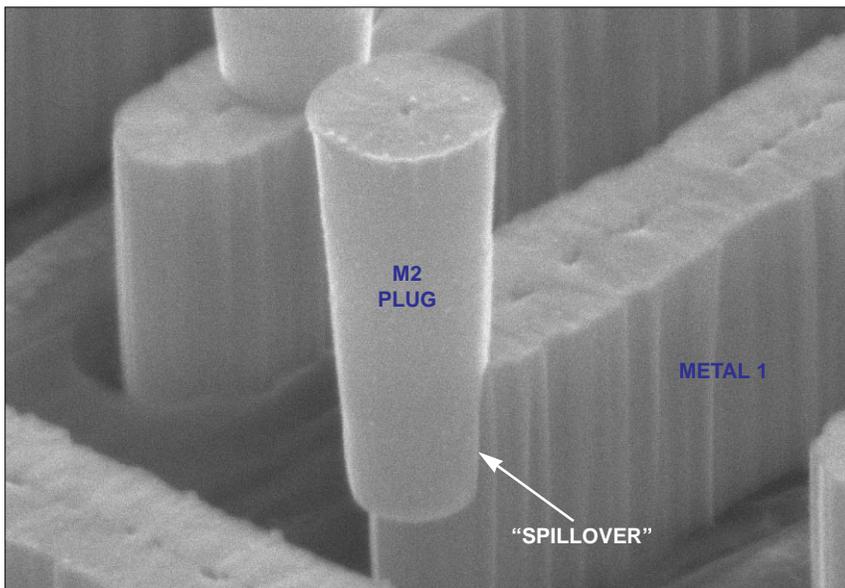
Figure 30. SEM views of general metal 2 integrity. 55°.



Mag. 30,000x

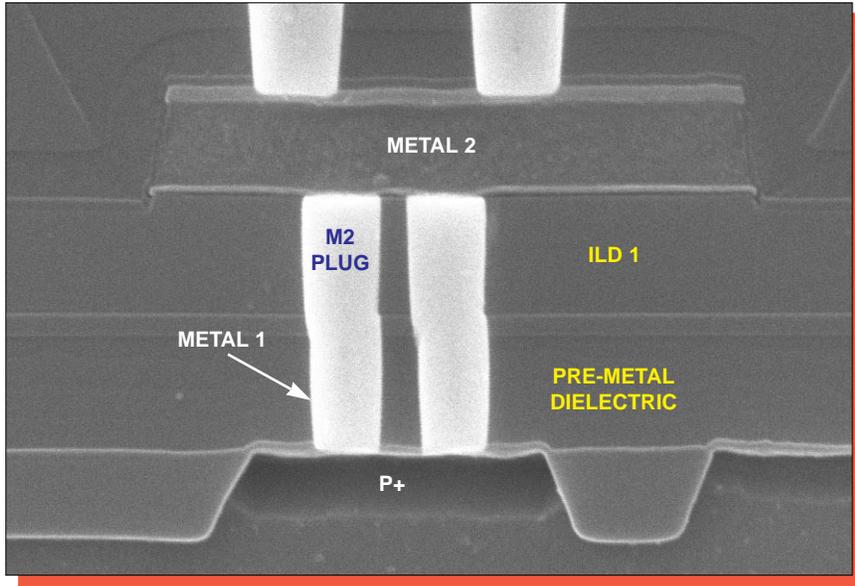


Mag. 35,000x

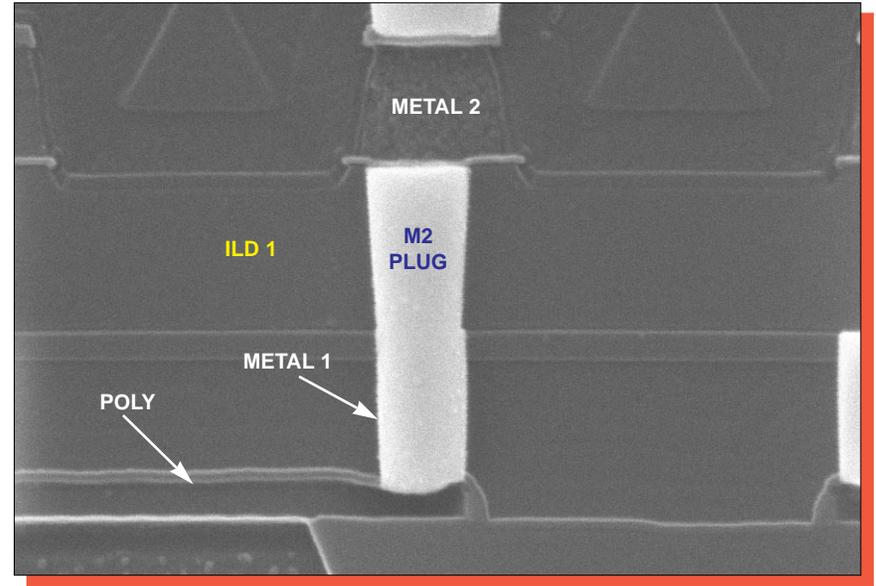


Mag. 45,000x

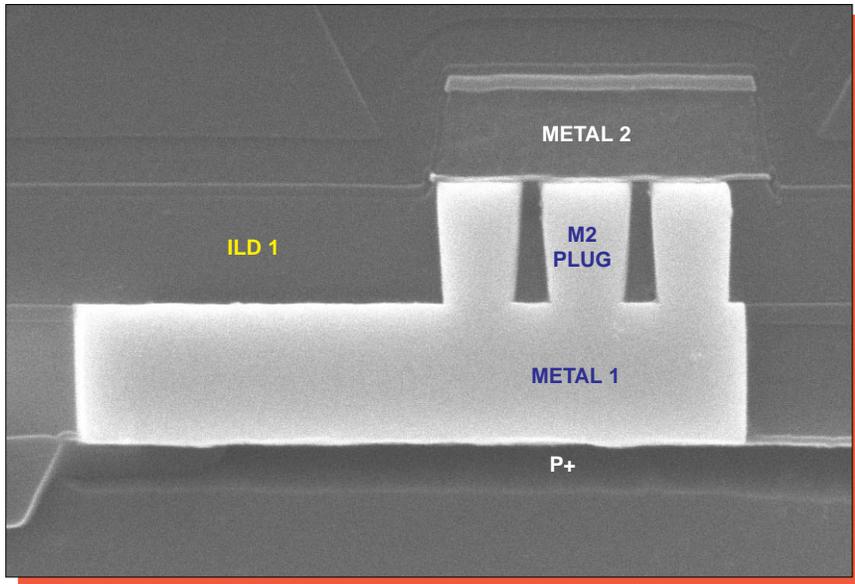
Figure 31. SEM views of metal 2 tungsten plugs. 55°.



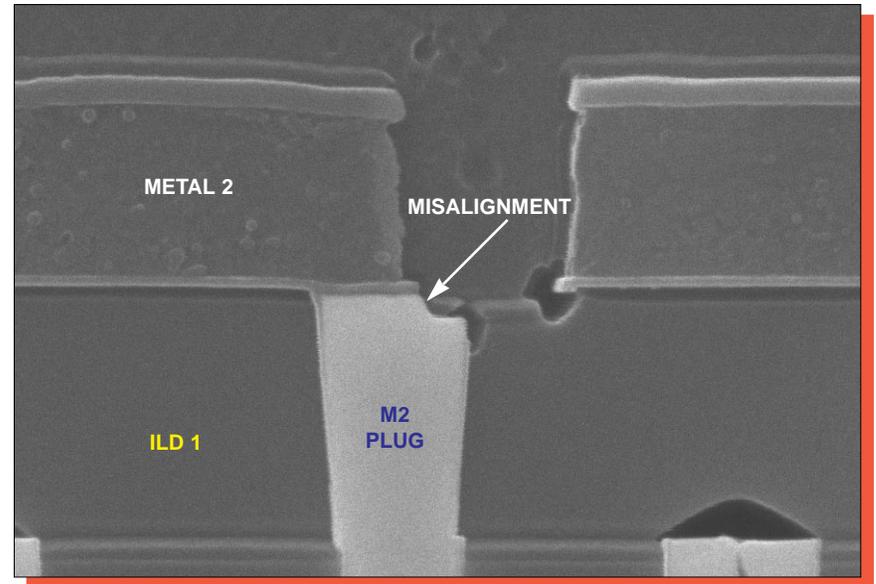
Mag. 20,000x



Mag. 26,000x

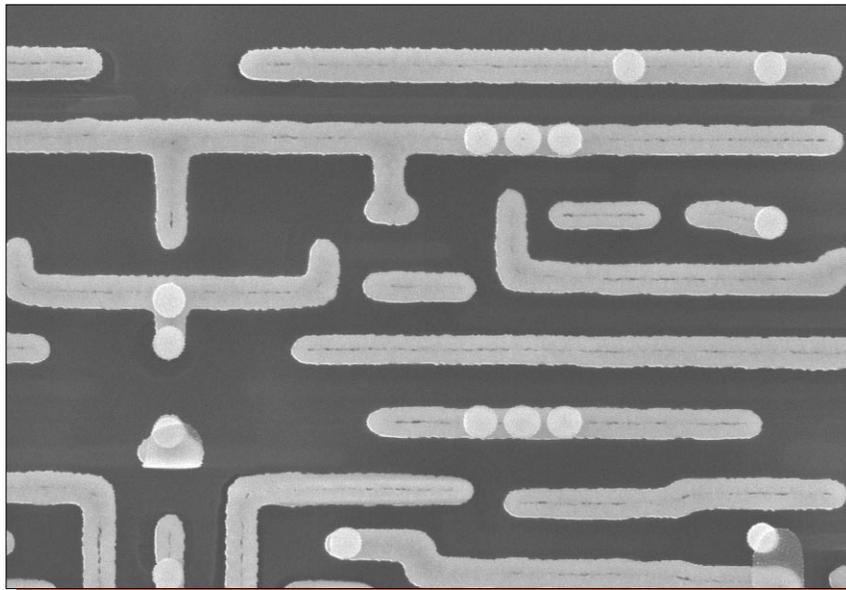


Mag. 20,000x

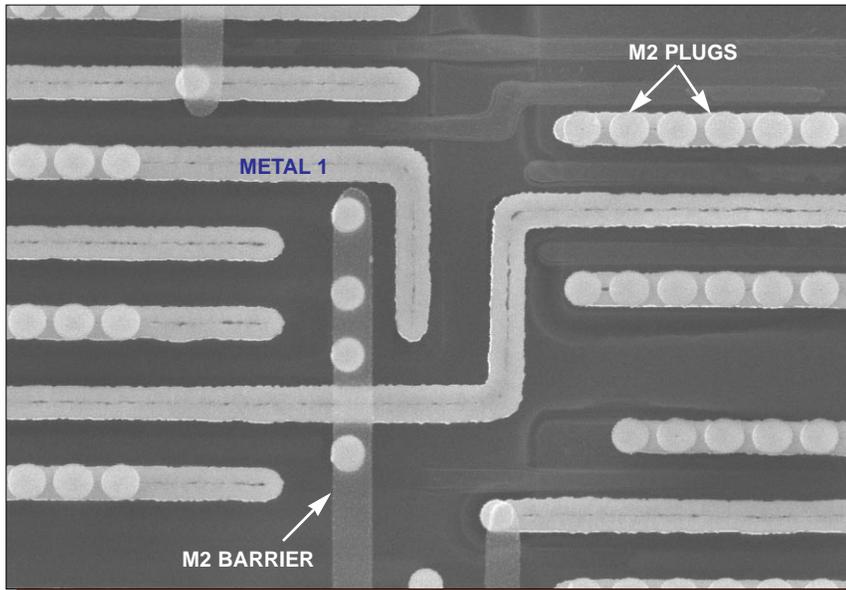


Mag. 40,000x

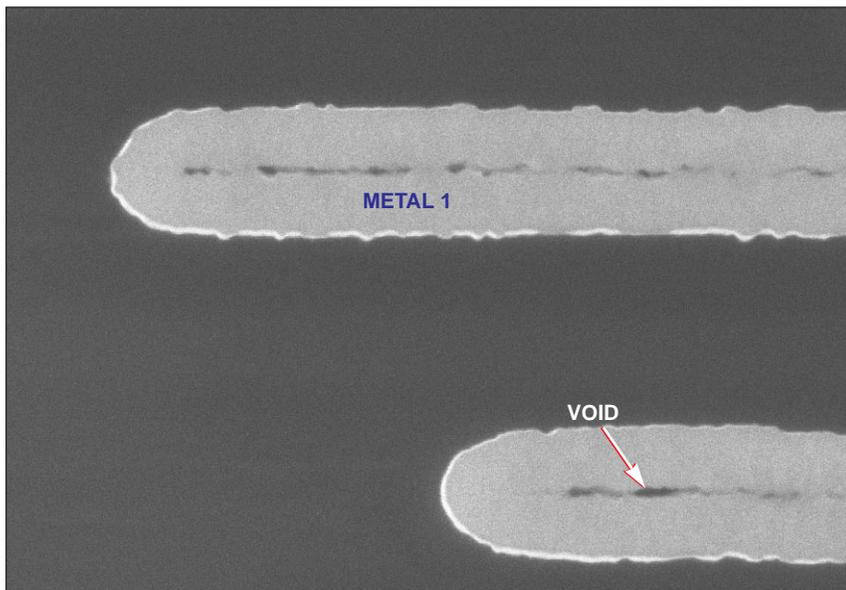
Figure 32. SEM section views of metal 2-to-metal 1 vias.



Mag. 8000x

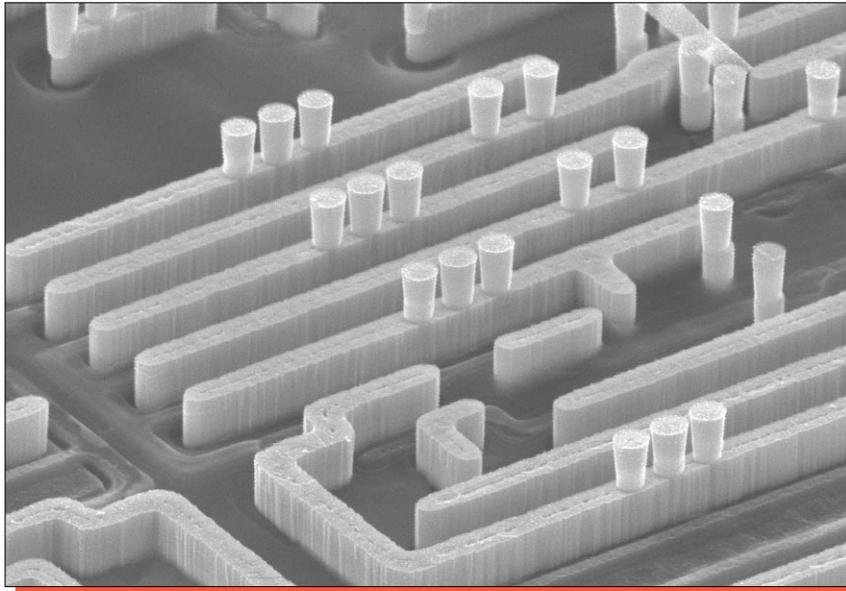


Mag. 9000x

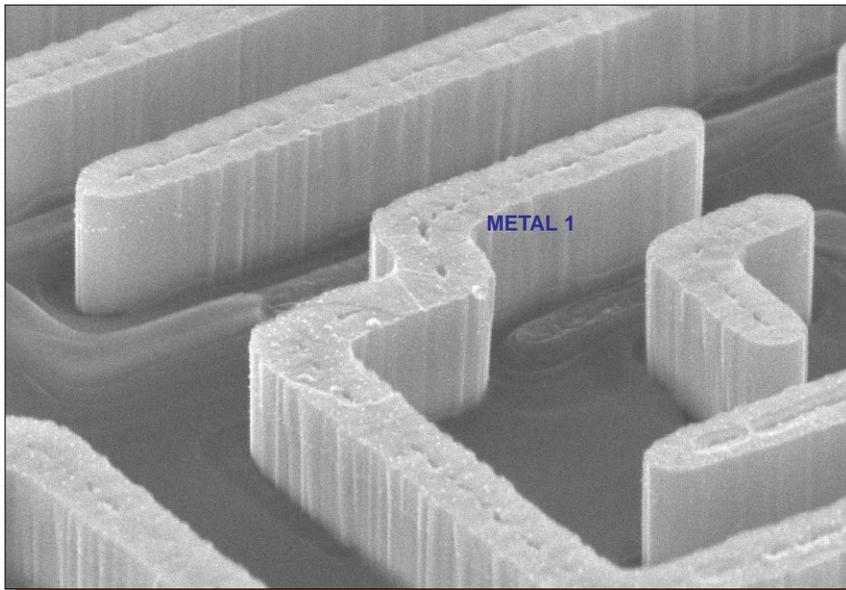


Mag. 35,000x

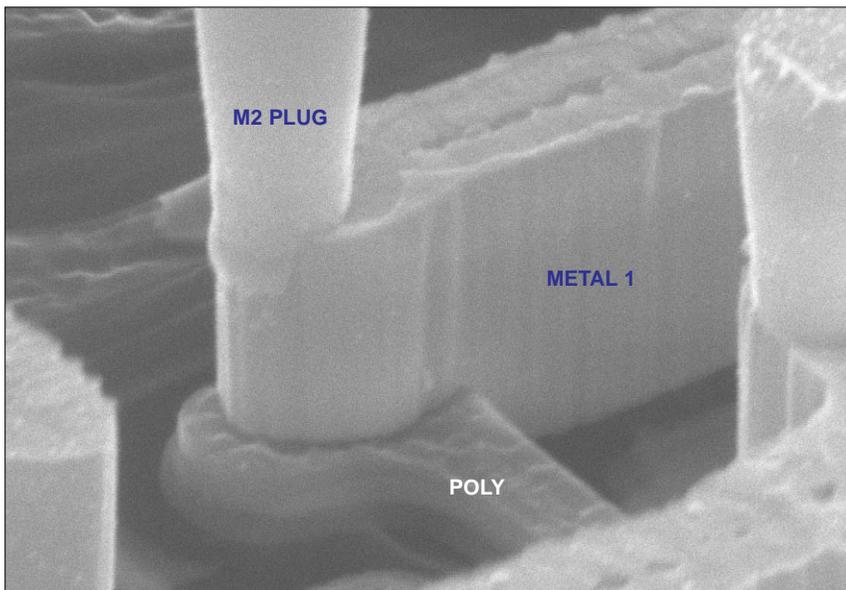
Figure 33. Topological SEM views of metal 1 patterning. 0°.



Mag. 8000x

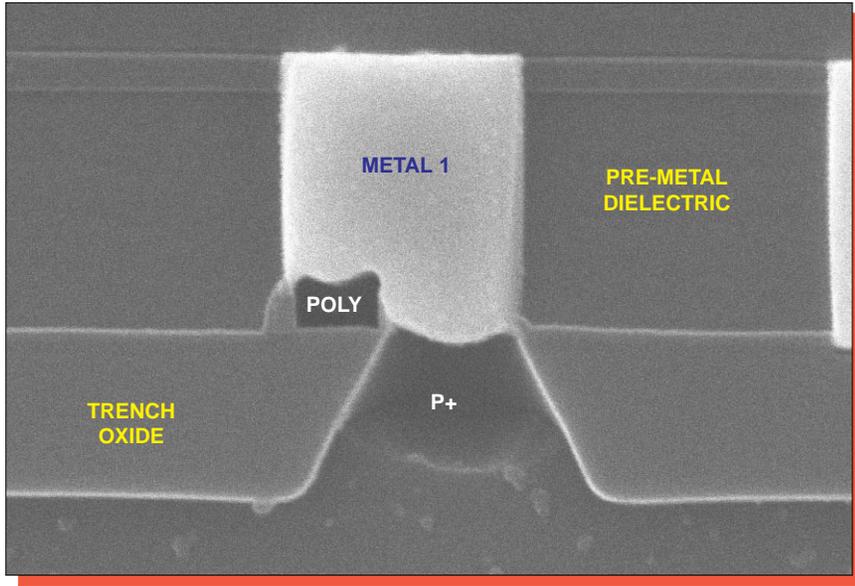


Mag. 20,000x

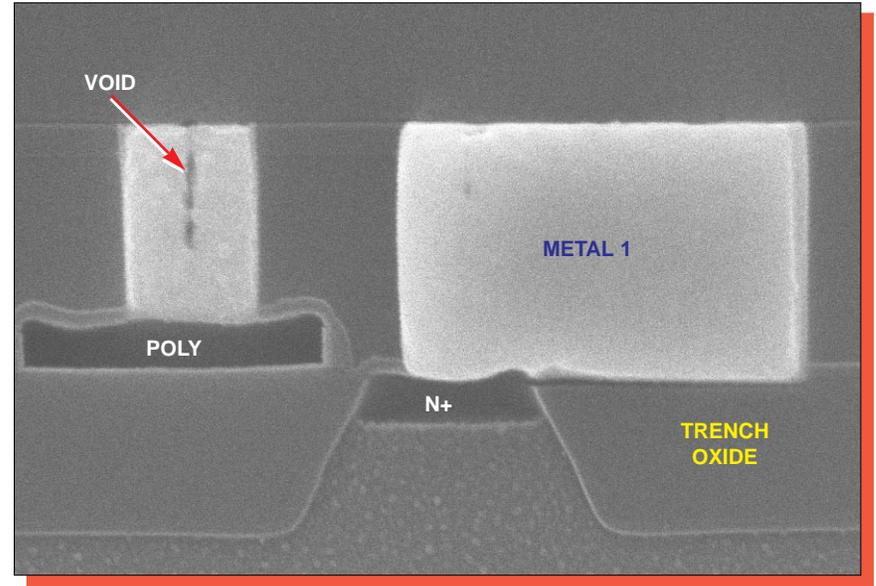


Mag. 48,000x

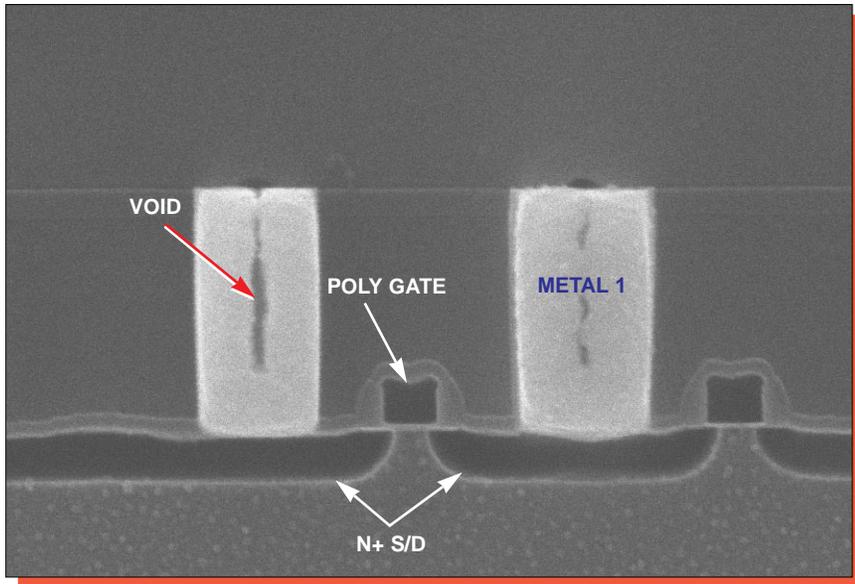
Figure 34. SEM views of general metal 1 integrity. 55°.



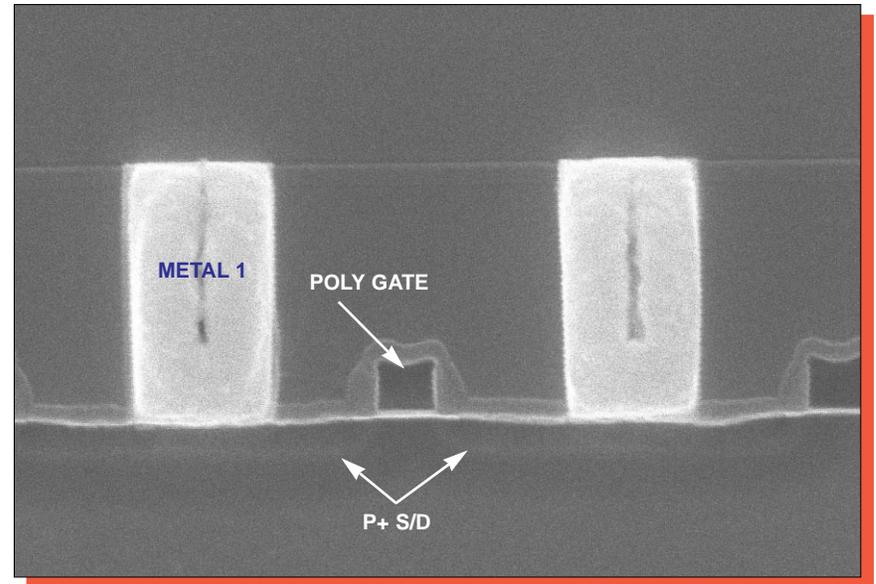
Mag. 40,000x



Mag. 35,000x

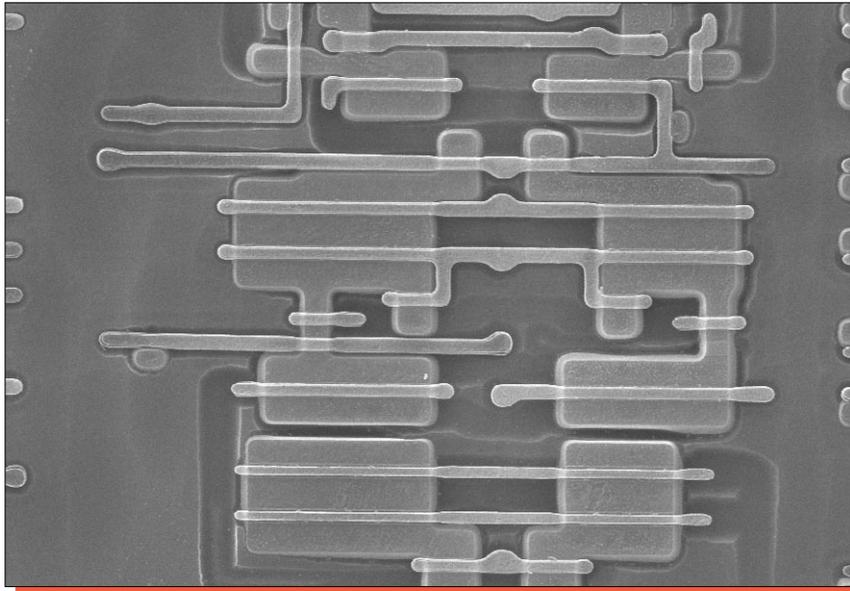


Mag. 35,000x

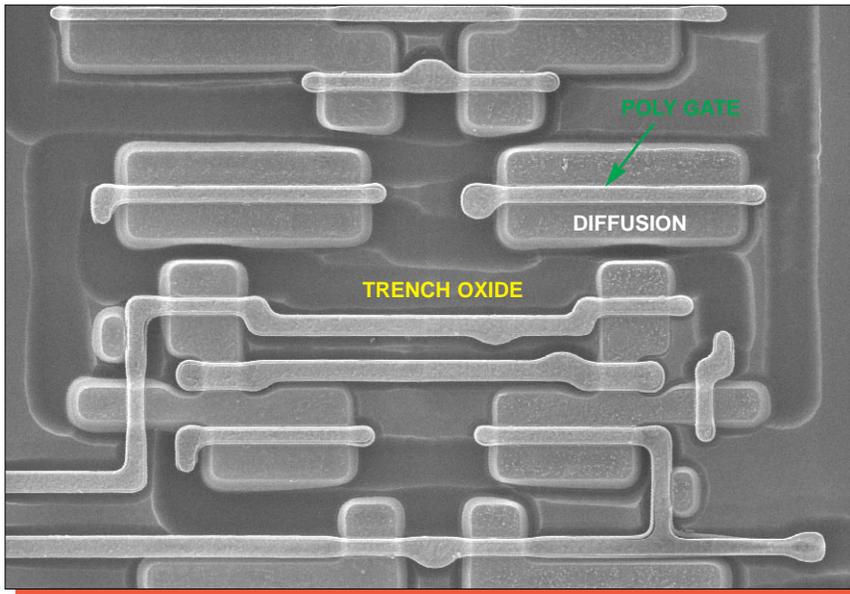


Mag. 40,000x

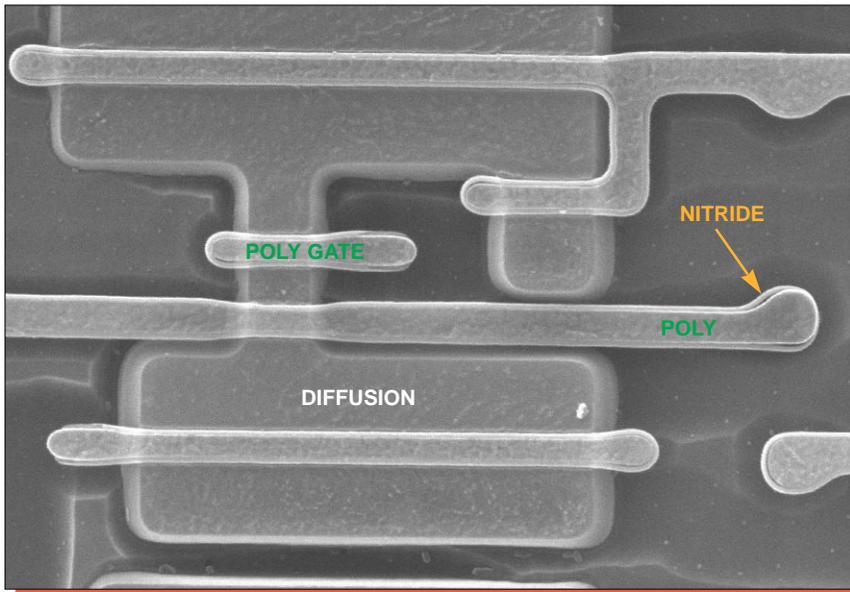
Figure 35. SEM section views of metal 1 contacts.



Mag. 4800x

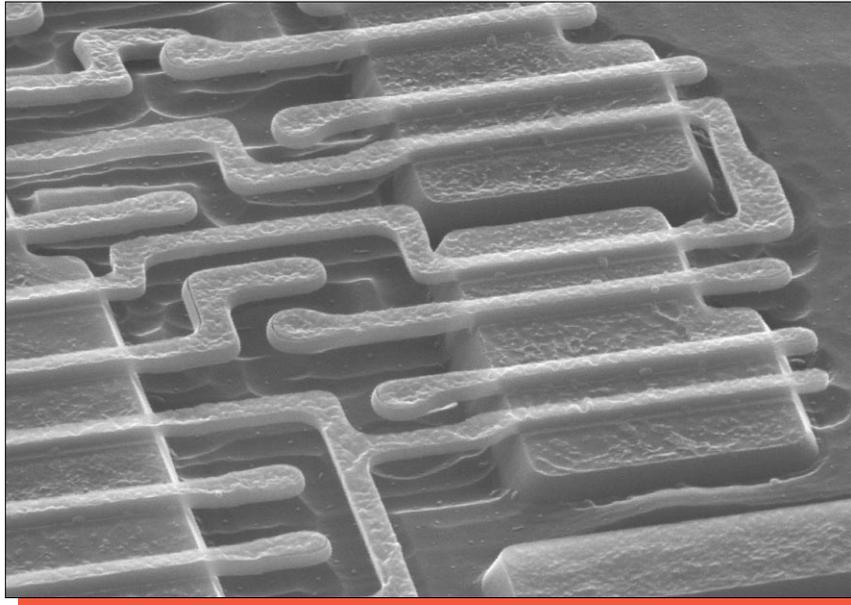


Mag. 6500x

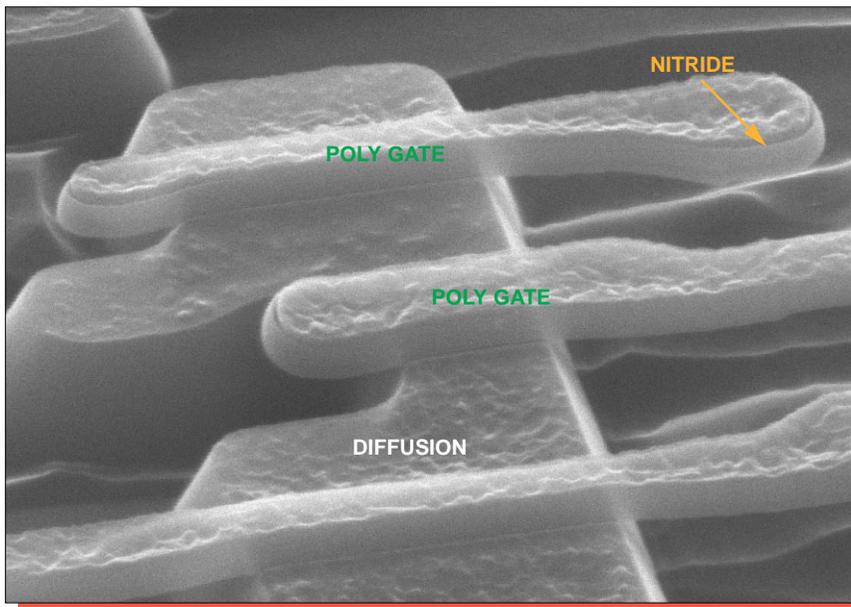


Mag. 13,000x

Figure 36. Topological SEM views of poly patterning. 0°.

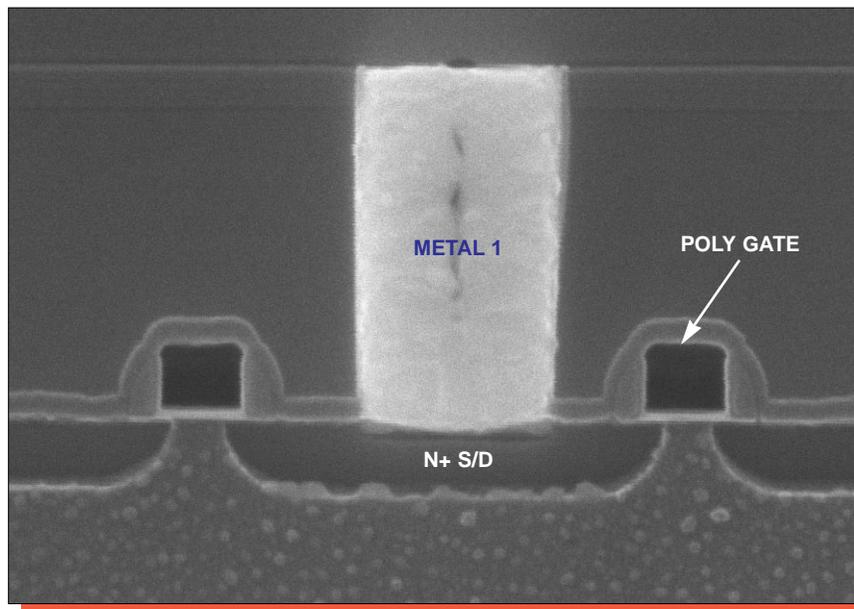


Mag. 13,000x

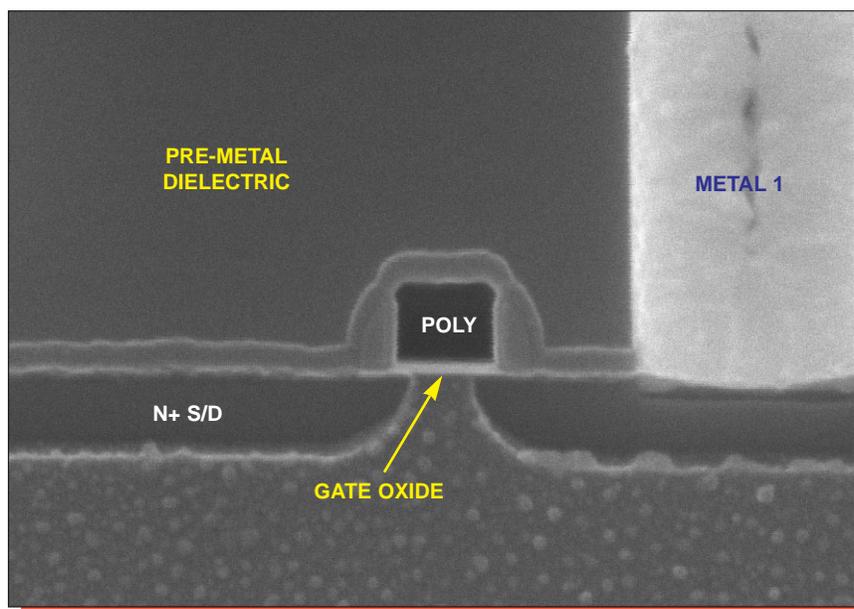


Mag. 31,000x

Figure 37. SEM views of general poly coverage. 55°.

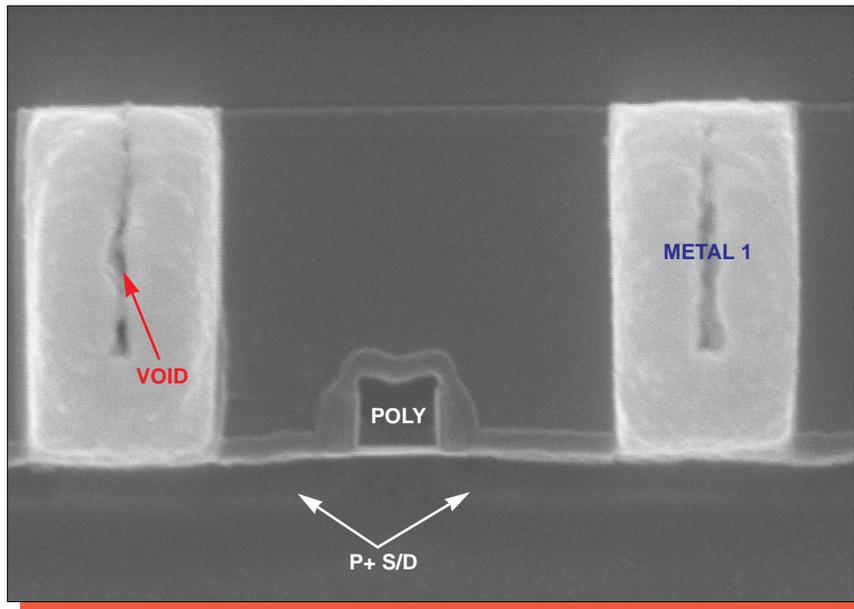


Mag. 52,000x

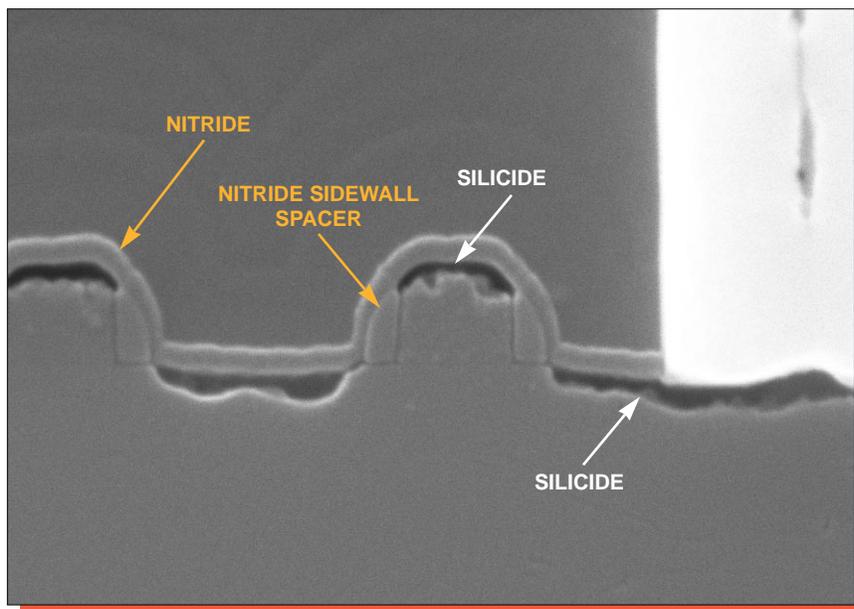


Mag. 65,000x

Figure 38. SEM section views of N-channel transistors.

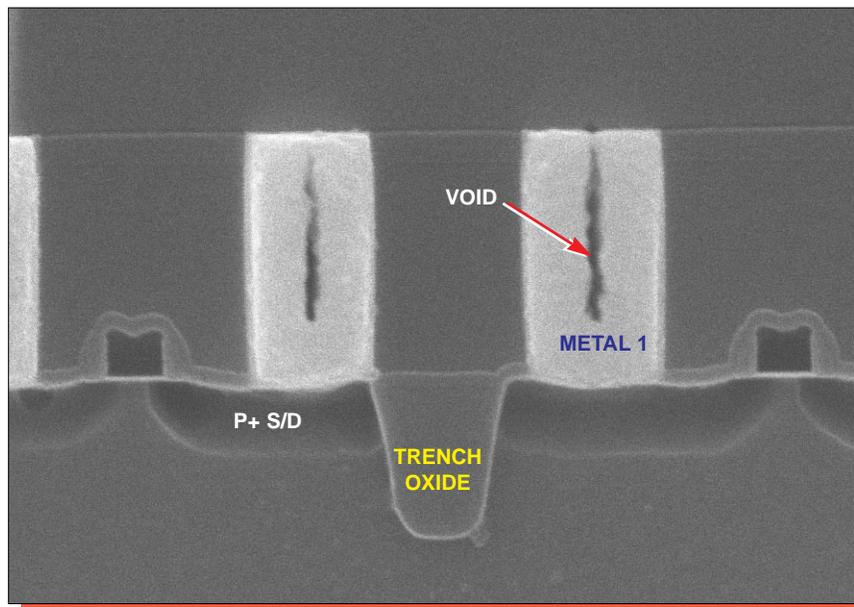


Mag. 52,000x

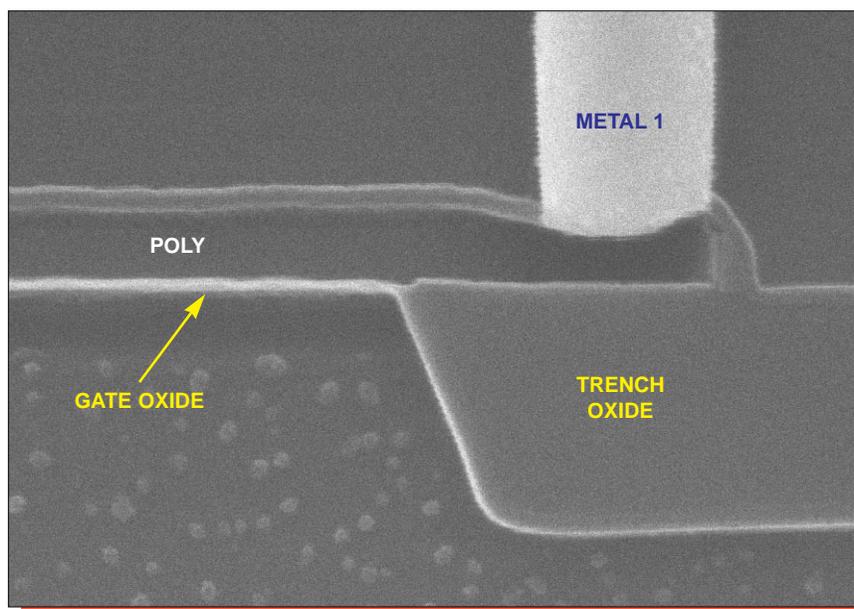


glass etch, Mag. 70,000x

Figure 39. SEM section views of P-channel transistors.

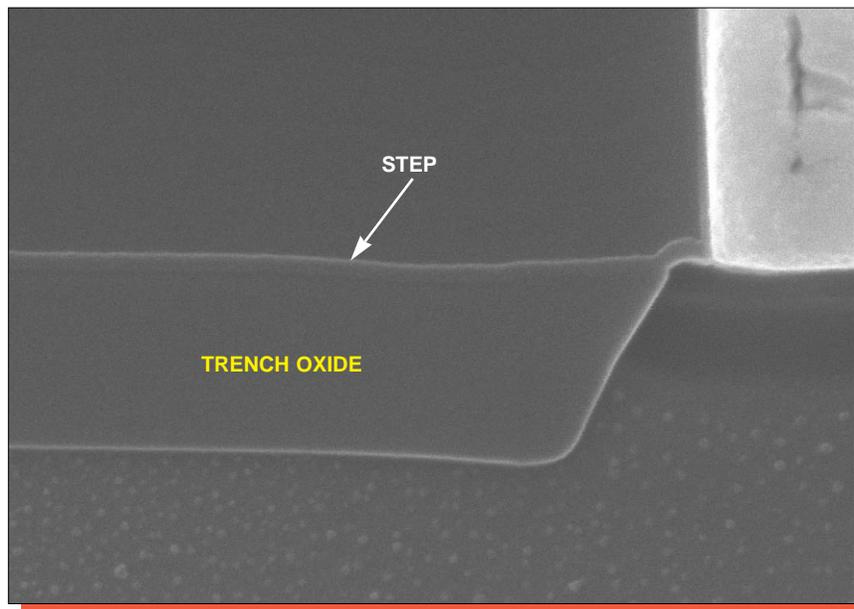


Mag. 40,000x

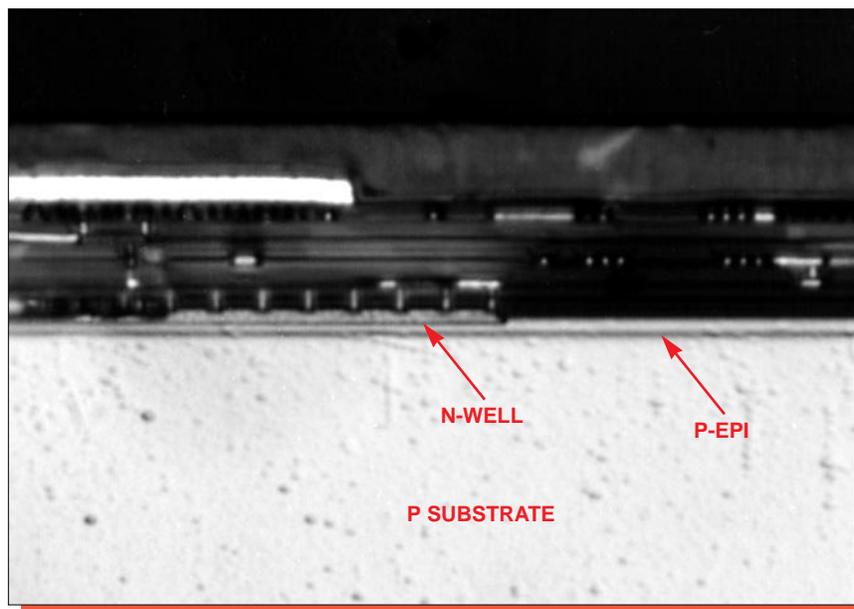


Mag. 52,000x

Figure 40. SEM section views of trench oxide structures.

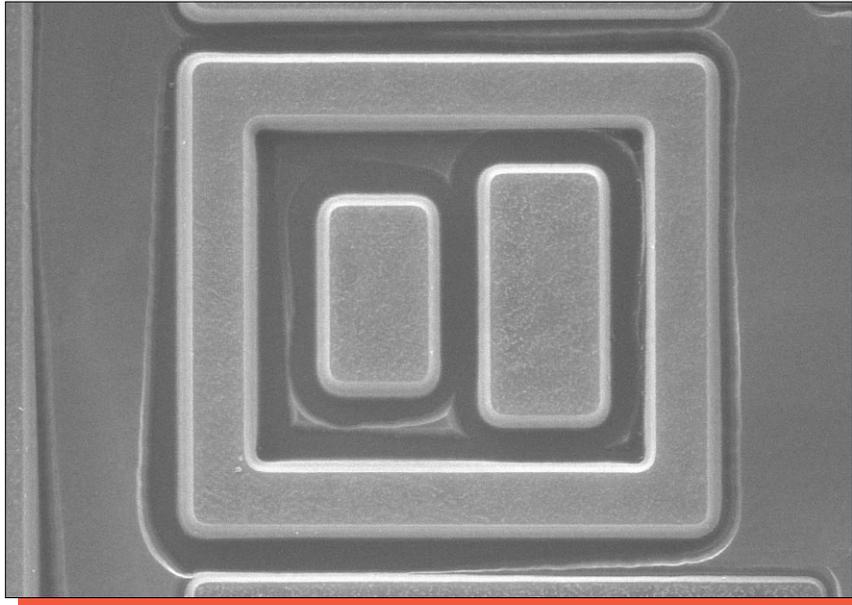


Mag. 45,000x

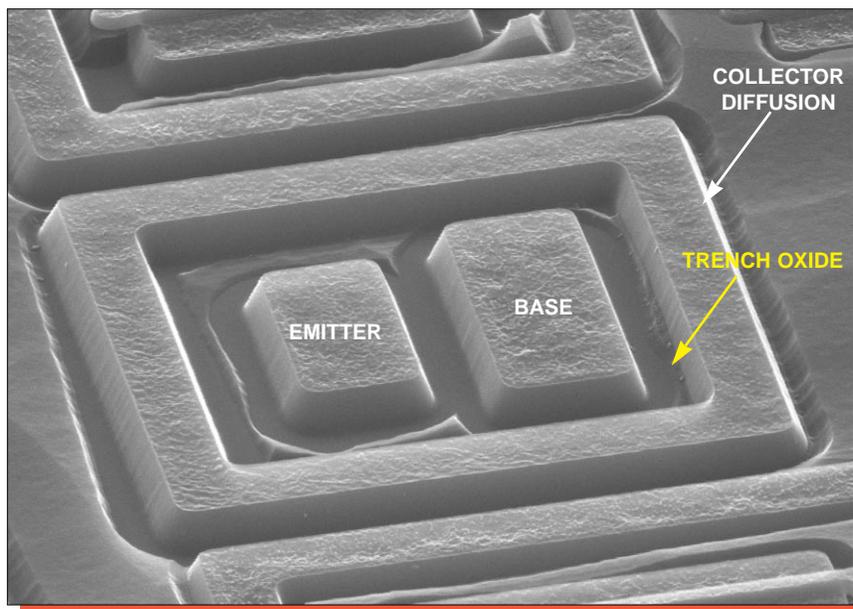


Mag. 1600x

Figure 41. Section views illustrating the well structure.

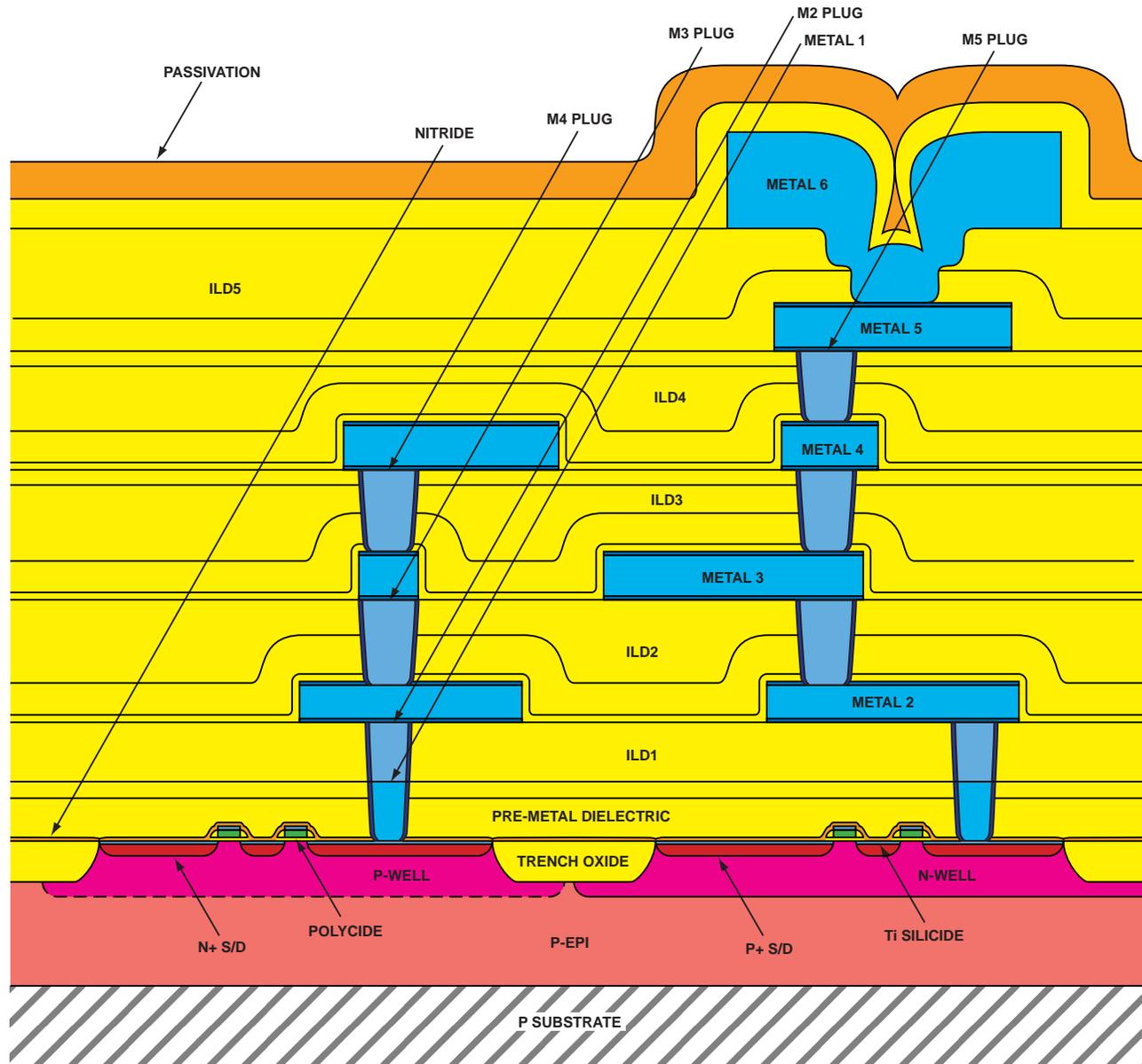


Mag. 9000x, 0°



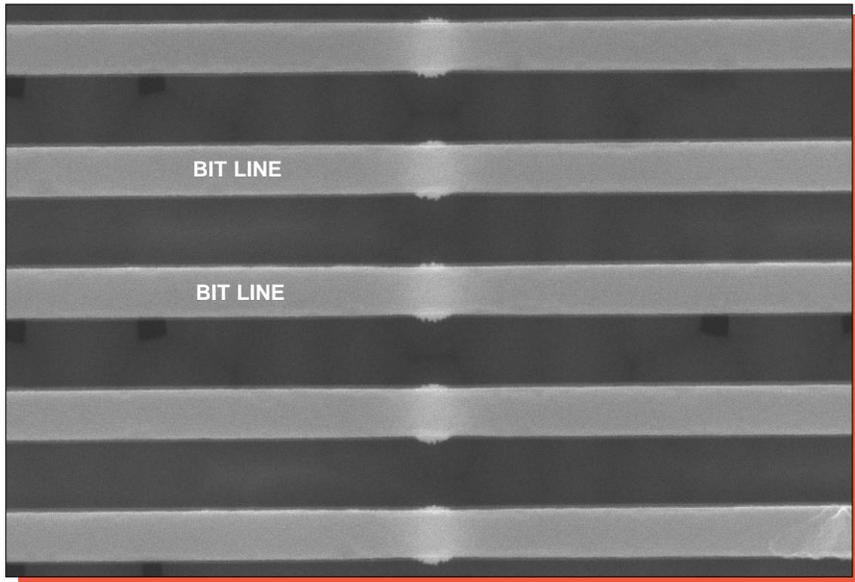
Mag. 10,000x, 55°

Figure 42. SEM views of a bipolar device.

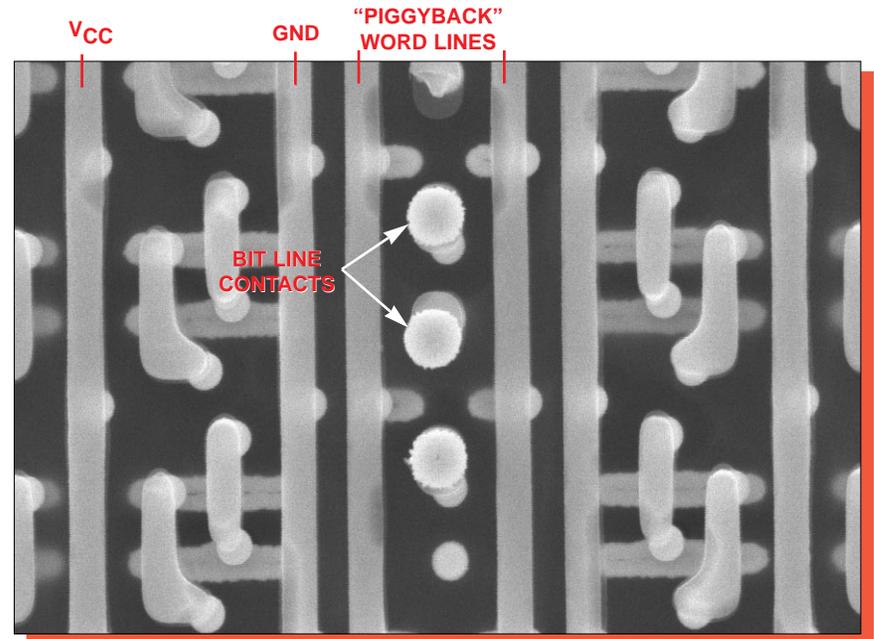


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

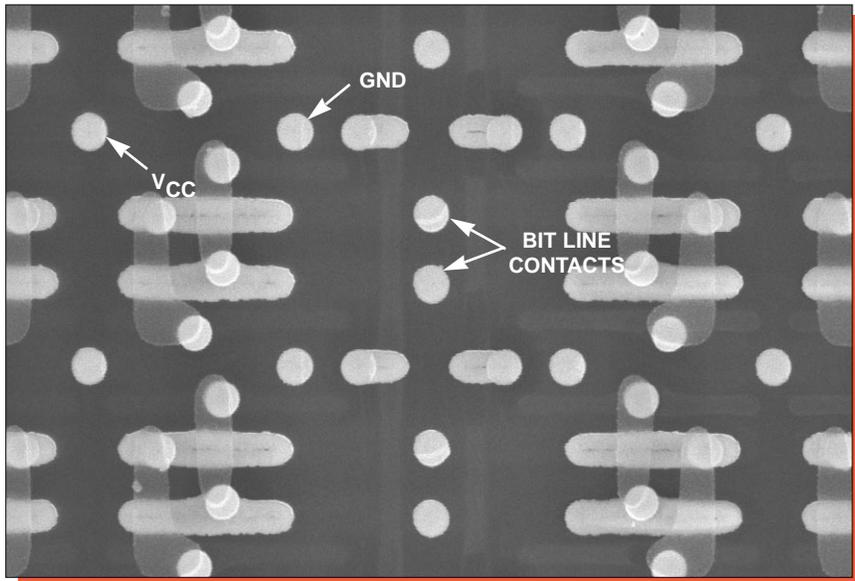
Figure 43. Color cross section drawing illustrating device structure.



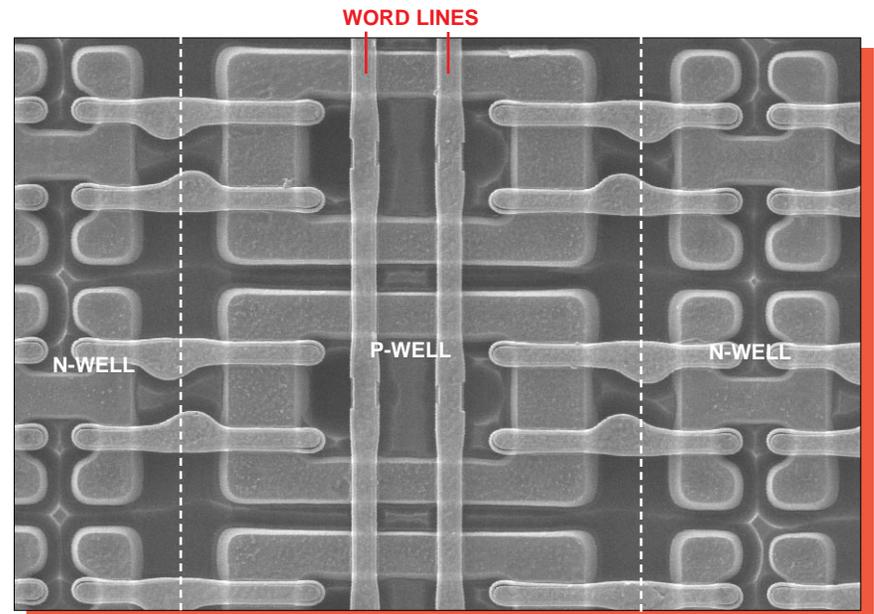
metal 3



metal 2

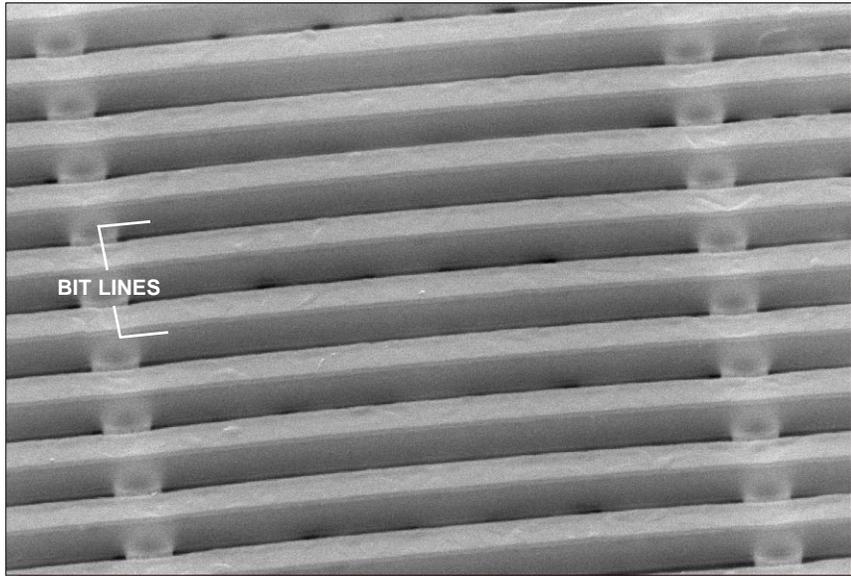


metal 1

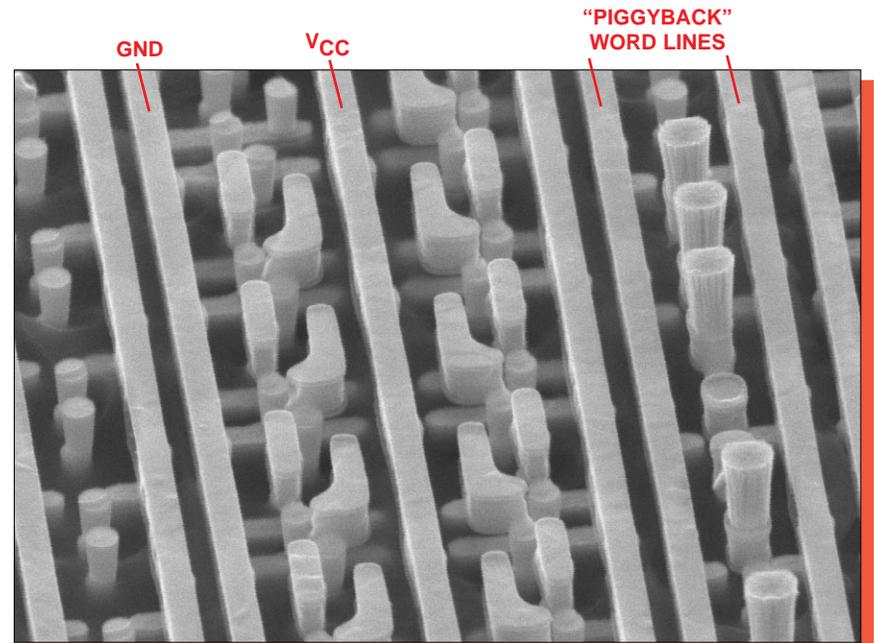


poly

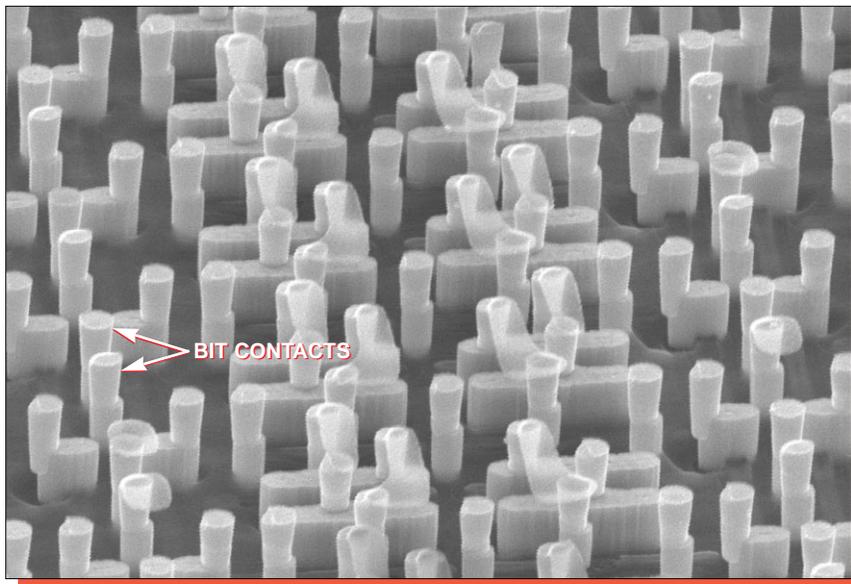
Figure 44. Topological SEM views of the Cache array. Mag. 9000x, 0°.



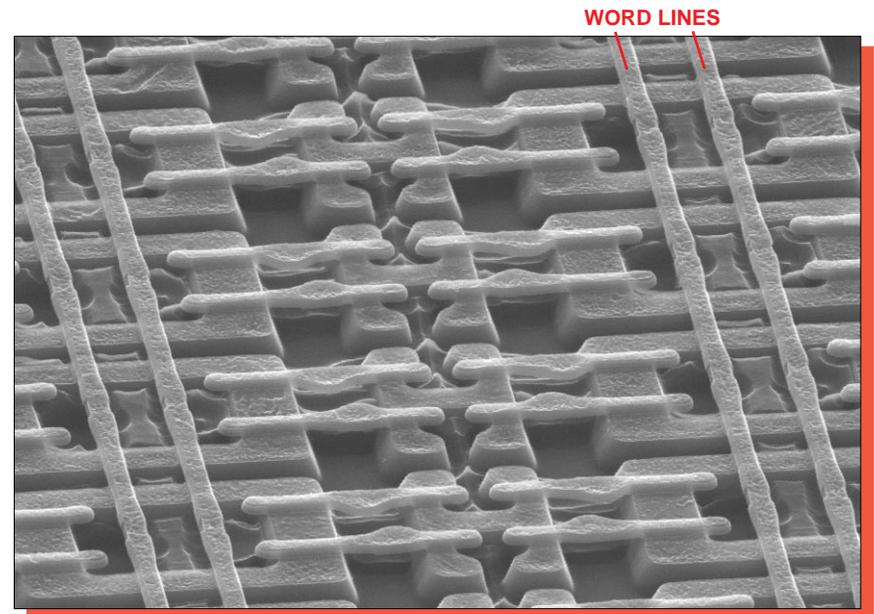
metal 3



metal 2

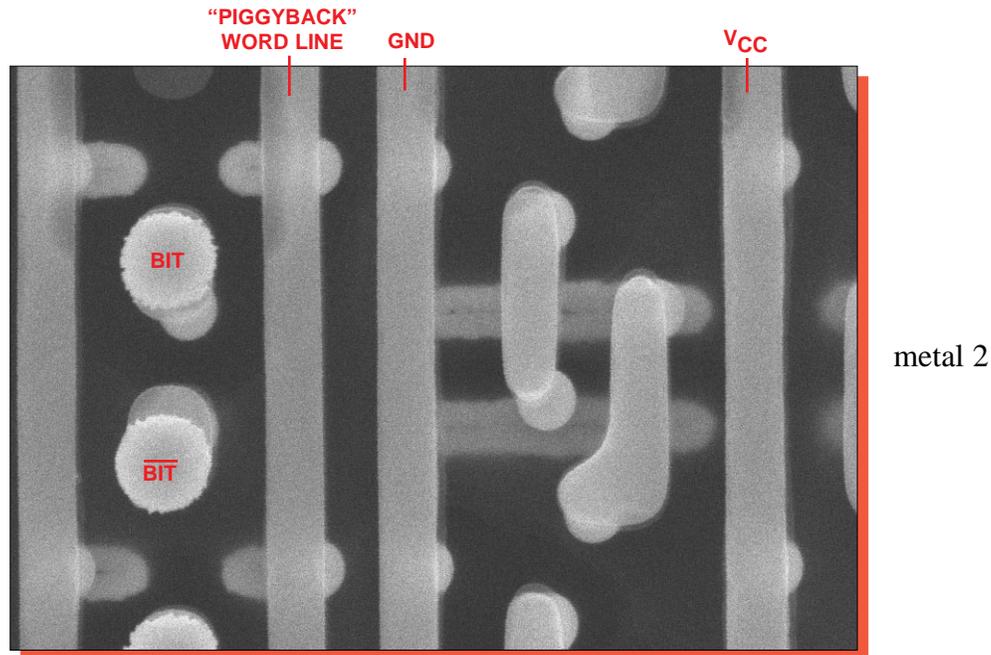


metal 1

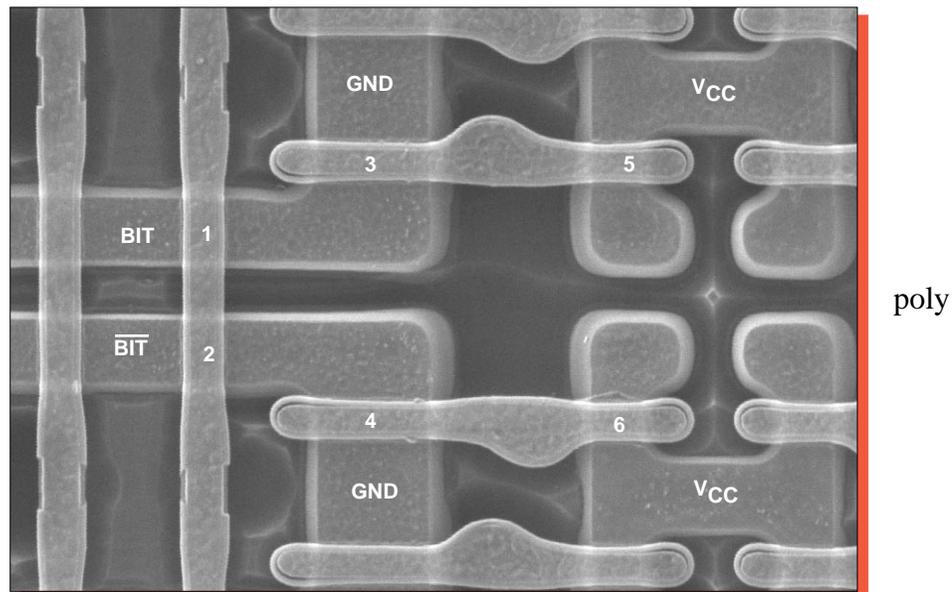


poly

Figure 45. Perspective SEM views of the Cache array. Mag. 8000x, 55°.



metal 2



poly

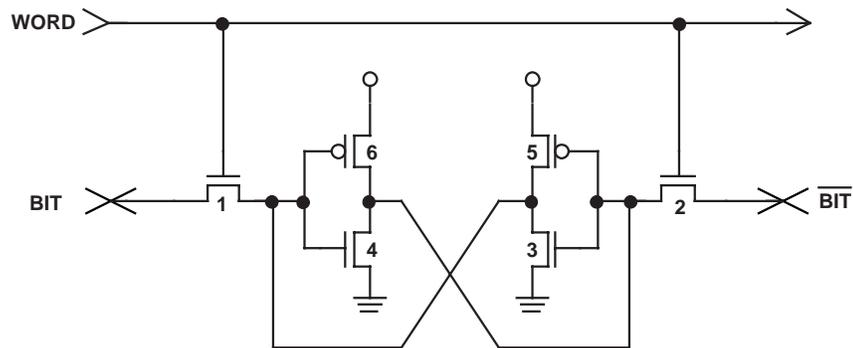


Figure 46. Topological SEM views of a Cache cell with schematic. Mag. 15,000x, 0°.