

Construction Analysis

NKK NR4645LQF-133 64-Bit RISC Microprocessor

Report Number: SCA 9707-547



INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the NKK NR4645LQF-133 64-bit RISC Microprocessor (133MHz). One device packaged in a 128-pin Plastic Quad Flat Package (PQFP) was received for the analysis. The device was date coded 9640.

MAJOR FINDINGS

Questionable Items:¹

- Metal 3 aluminum thinning up to 100 percent² at metal 3-to-metal 2 vias (Figure 12). Barrier maintained continuity.
- Metal 2 aluminum thinning up to 95 percent² at metal 2-to-metal 1 vias (Figure 15).

Special Features:

- Three level metal, twin-well, epi, CMOS process.
- Sub-micron gate lengths (0.35 micron).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended applications

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- The device was packaged in 128-pin Plastic Quad Flat Package (PQFP) for surface mount applications.
- Die separation was by sawing (full depth). Silver-filled epoxy was used to attach the die to the paddle.
- Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire.
- Pins 4, 77 and 80 were not connected. No multiple bonding was noted.

Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an apparent N-epi on a P substrate.
- No die coat was present.
- Final passivation: A layer of nitride over a layer of silicon-dioxide.
- Metallization: Three levels of metal defined by dry-etch techniques. Metal layers 3 and 2 consisted of aluminum with a titanium-nitride (TiN) cap and a titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride (TiN) cap and barrier. Standard vias were used at metal 3 and metal 2. Metal 1 used tungsten (W) plugs for contacts. A thin titanium (Ti) layer was used under metal 1 for adhesion purposes.
- Interlevel dielectrics: Both interlevel dielectrics (between metal 3 and metal 2 and between metal 2 and metal 1) consisted of two layers of silicon-dioxide. No

TECHNOLOGY DESCRIPTION (continued)

spin-on-glass (SOG) was noted. The first layer of glass appeared to have been subjected to an etchback.

- Pre-metal dielectric: This dielectric consisted of a CVD glass (probably BPSG) over various densified oxides. Reflow was performed prior to contact cuts.
- Polysilicon: A single layer of dry-etched poly (no silicide) was used. This layer was used to form all gates on the die and word lines in the SRAM arrays.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing. Diffusions were not silicided.
- Isolation: Local oxide (LOCOS). A step was present in the oxide at the well boundaries indicating a twin well process was employed.
- Wells: Twin wells in what appeared to be an N-epi on a P substrate.
- Memory cells: Two SRAM cell arrays were present. The 6T SRAM cell design used metal 3 to distribute GND and form “piggyback” word lines (via metals 1 and 2), and metal 2 to form the bit lines. Metal 1 distributed GND and Vcc and provided cell interconnect. Poly was used to form the word lines and all gates. The 12T SRAM cell design used metal 3 to distribute input signals, word lines and GND. Metal 2 was used to form the output and bit lines and distribute Vcc and GND. Metal 1 was used to provide cell interconnect. Poly formed the word lines and all gates.

ANALYSIS RESULTS I

Package and Assembly:

Figures 1 - 4

Questionable Items:¹ None.

General Items:

- The device was packaged in a 128-pin Plastic Quad Flat Package (PQFP) for surface mount applications.
- Overall package quality: Good. No defects were noted on the external portion of the package. Pins were well formed (except previously damaged pins).
- Die dicing: Die separation was by sawing (full depth) of normal quality. No large chips or cracks were present.
- Die attach: A silver-filled epoxy was used to attach the die to the paddle. Some voids were apparent on the x-ray; however, overall coverage was approximately 75 percent and no problems are foreseen.
- Wirebonding: Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire. Wirebond formation and placement were normal.
- Pins 4, 77 and 80 were not connected. No multiple bonding was noted.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended applications.

ANALYSIS RESULTS II

Die Process and Design:

Figures 5 - 33

Questionable Items:¹

- Metal 3 aluminum thinning up to 100 percent² at some metal 3-to-metal 2 via locations (Figure 12).
- Metal 2 aluminum thinning up to 95 percent² at some metal 2-to-metal 1 via locations (Figure 15).

Special Features:

- Three level metal, twin-well, epi, CMOS process.
- Sub-micron gate lengths (0.35 micron).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an apparent N-epi on a P substrate.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Die coat: No die coat was present.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended applications.

²Seriousness depends on design margins.

ANALYSIS RESULTS II (continued)

- Final passivation: Passivation consisted of a layer of nitride over a layer of silicon dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was also good.
- Metallization: Three levels of metal defined by dry-etch techniques. Metal layers 3 and 2 consisted of aluminum with a titanium-nitride (TiN) cap and a titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride (TiN) cap and barrier. Standard vias were used under metal 3 and metal 2. Metal 1 used tungsten (W) plugs for contacts. A thin titanium (Ti) layer was used under metal 1 for adhesion purposes. Tungsten (W) plugs used titanium-nitride (TiN) liners.
- Metal patterning: All metal layers were defined by a standard dry etch of normal quality. Metal lines were widened around vias and contacts at all metal levels.
- Metal defects: None. No voiding, notching or cracking of any metal layers was found. No silicon nodules were found following removal of the aluminum.
- Metal step coverage: Metal 3 aluminum thinned up to 100 percent at some via edge locations (barrier maintained continuity). Total metal 3 thinning was reduced to 95 percent with the addition of the cap and barrier metal. Metal 2 aluminum thinned up to 95 percent at some via edge locations. Total metal 2 thinning was reduced to 85 percent with the addition of the cap and barrier. MIL-STD-883D allows up to 70 percent metal thinning for contacts of this size. Virtually no metal 1 thinning was present due to the use of tungsten plugs. All contacts and vias were completely surrounded by metallization.
- Interlevel dielectrics: Both interlevel dielectrics (between metal 3 and metal 2 and between metal 2 and metal 1) consisted of two layers of silicon-dioxide each. No spin-on-glass (SOG) was used to aid planarization. The first layer of glass appeared to have been subjected to an etchback. Voids were noted in the first layer of glass on both levels. They appear to be a result of the first layer of glass cusping between

ANALYSIS RESULTS II (continued)

minimum spaced lines (see Figures 13 and 16). No serious reliability concerns are foreseen due to this since the metals were completely surrounded by glass.

- Pre-metal dielectric: A CVD glass (probably BPSG) over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts. No problems were found.
- Poly: A single level of poly (no silicide). Poly formed all gates on the die and word lines in the SRAM arrays. Definition was by a dry etch of good quality. Oxide sidewall spacers were used throughout and left in place. No problems were found.
- Isolation: Local oxide (LOCOS) isolation was used. No problems were found.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Diffusions were not silicided. An LDD process was used employing oxide sidewall spacers on the gates.
- Wells: Twin-wells were used in an apparent N-epi on a P substrate. A step was noted at the well boundary confirming a twin-well process was employed.
- Memory cells: Two SRAM cell arrays were present. The 6T SRAM cell design used metal 3 to distribute GND and form “piggyback” word lines (via metals 1 and 2), and metal 2 to form the bit lines. Metal 1 was used to distribute GND and Vcc and to provide cell interconnect. Poly was used to form word lines and all gates. Cell pitch was 3.7 x 19.0 microns (70 microns², a very large cell). The 12T SRAM cell design used metal 3 to distribute input signals, word lines and GND. Metal 2 was used to form the output and bit lines and distribute Vcc and GND. Metal 1 was used to provide cell interconnect. Poly was used to form the word lines and all gates. Cell pitch was 10 x 19.5 microns (195 microns²).
- No redundancy elements (fuses) were present.

PROCEDURE

The device was subjected to the following analysis procedures:

External inspection
X-ray
Decapsulation
Internal optical inspection
SEM of assembly and passivation
Passivation integrity test (chemical)
Passivation removal
SEM inspection of metal 3
Aluminum 3 removal
Delayer to metal 2 and inspect
Aluminum 2 removal
Delayer to metal 1 and inspect
Aluminum 1 removal
Delayer to silicon and inspect poly/die surface
Die sectioning (90° for SEM)*
Die material analysis
Measure horizontal dimensions
Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal.

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.0 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP ¹
Metal registration	N
Contact coverage	N
Contact registration	N

¹Metal 3 aluminum thinning up to 100 percent, metal 2 aluminum thinning up to 95 percent.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

(LOGO) NKK JAPAN

NR4645LQF-133

6135840B 9640

BOTTOM

AB 89 (molded)

DIE MATERIAL IDENTIFICATION

Overlay passivation:	Nitride over silicon-dioxide.
Metallization 3:	Aluminum (Al) with a titanium-nitride cap and titanium (Ti) barrier.
Interlevel dielectric 2 (M3-to-M2):	Two layers of silicon-dioxide.
Metallization 2:	Aluminum (Al) with a titanium-nitride cap and a titanium (Ti) barrier.
Interlevel dielectric 1 (M2-to-M1):	Two layers of silicon-dioxide.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier. A thin titanium (Ti) adhesion layer was present under the barrier.
Plugs (metal 1):	Tungsten on a titanium-nitride (TiN) liner.
Pre-metal dielectric:	CVD glass (probably BPSG) over various densified oxides.

VERTICAL DIMENSIONS

Layers

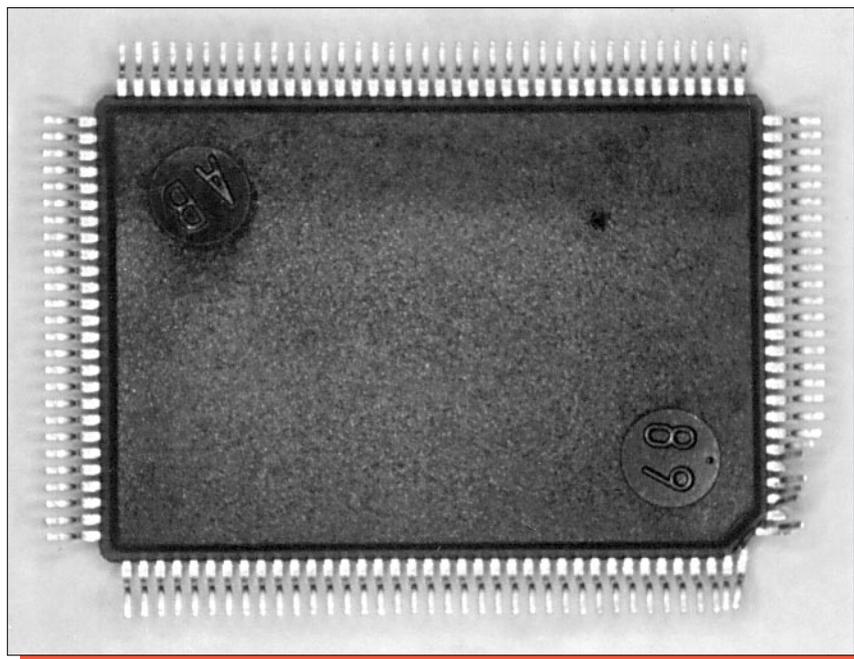
Passivation 2:	0.6 micron
Passivation 1:	0.65 micron
Metal 3 - cap:	0.05 micron (approx.)
- aluminum:	1.0 micron
- barrier:	0.1 micron
Interlevel dielectric 2 - glass 2:	0.35 - 0.4 micron
- glass 1:	0.45 - 1.3 micron
Metal 2 - cap:	0.04 micron (approx.)
- aluminum:	0.6 micron
- barrier:	0.1 micron
Interlevel dielectric 1 - glass 2:	0.4 - 0.5 micron
- glass 1:	0.4 - 0.9 micron
Metal 1- cap:	0.04 micron (approx.)
- aluminum:	0.4 micron
- barrier:	0.06 micron (approx.)
- plugs:	0.6 - 0.9 micron
Pre metal dielectric:	0.5 - 0.8 micron
Oxide on poly:	0.15 micron
Poly:	0.25 micron
Local oxide:	0.35 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.2 micron
P well:	4 microns
N-epi:	10 microns

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12T SRAM CELL STRUCTURE	Figures 29 - 32
I/O AND GENERAL CIRCUITRY	Figure 33



top



bottom

Figure 1. Package photographs of the NKK NR4645 Microprocessor. Mag. 5x.

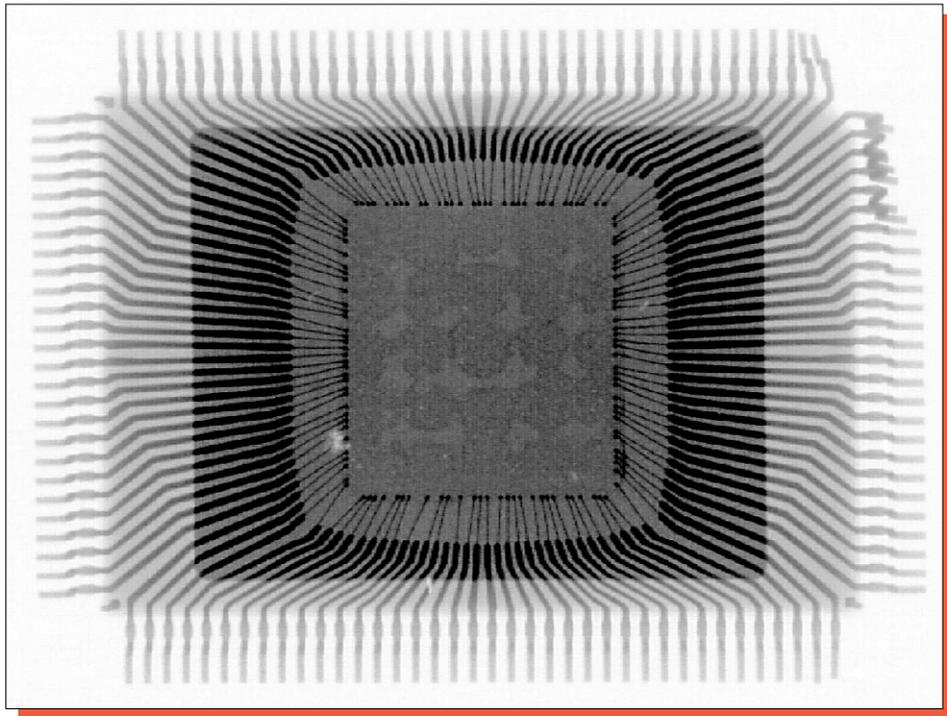
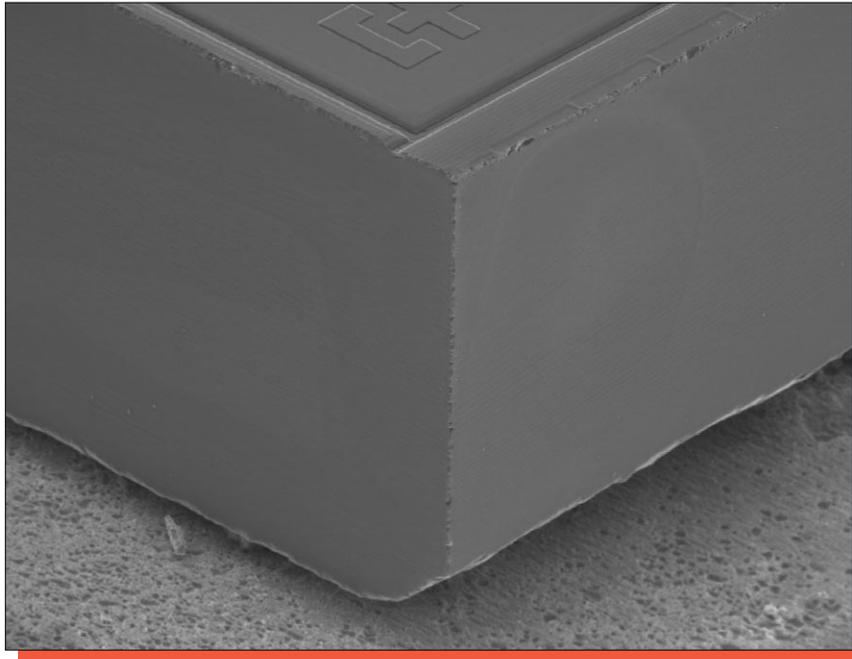
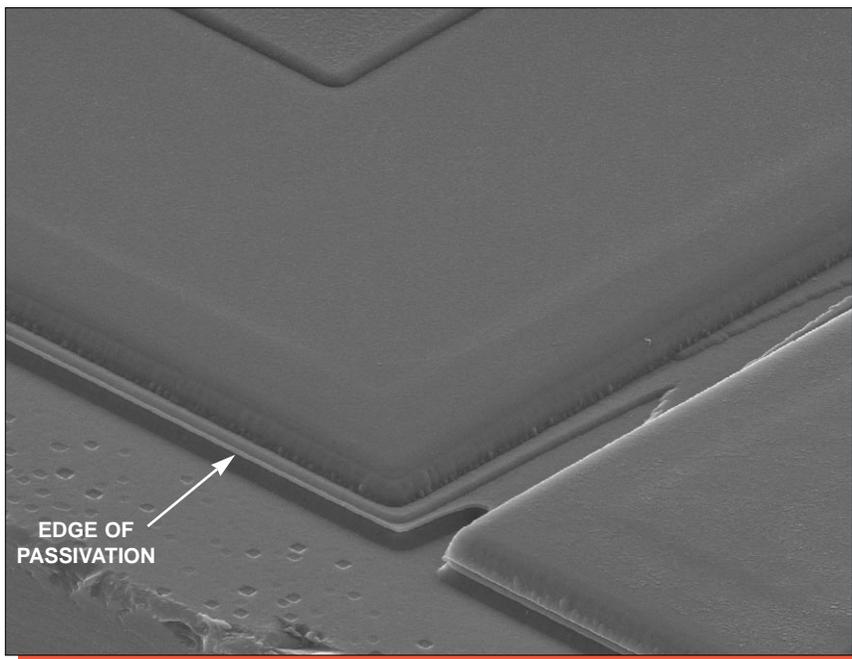


Figure 2. X-ray view of the package. Mag. 5x.

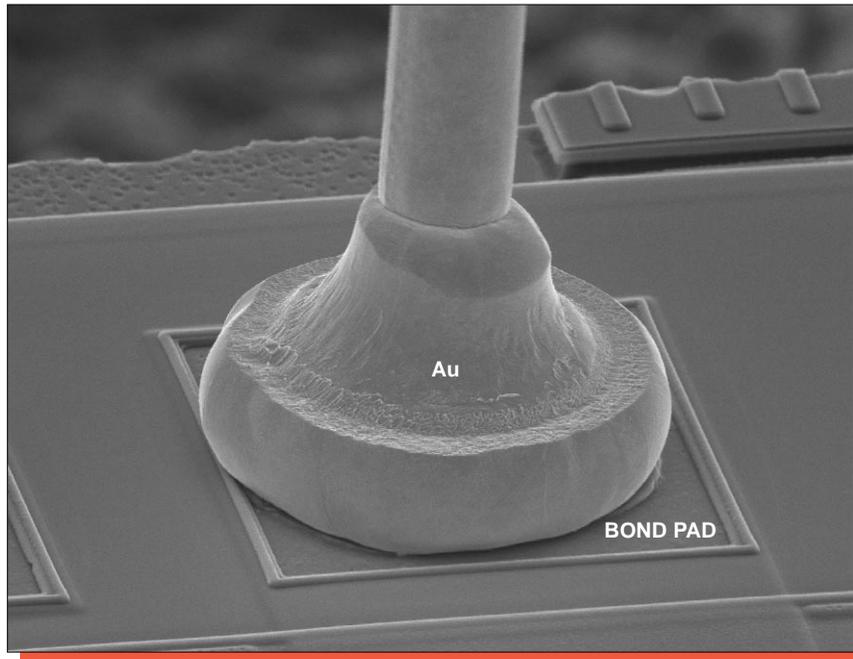


Mag. 190x

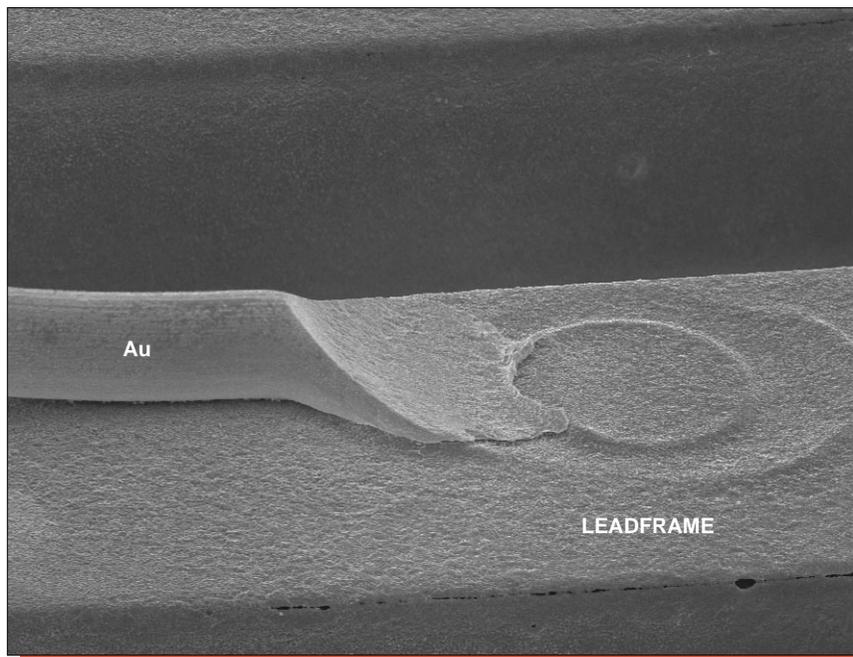


Mag. 1200x

Figure 3. Perspective SEM views of dicing and edge seal. 60°.



Mag. 650x



Mag. 550x

Figure 4. Perspective SEM views of typical bonds. 60°.

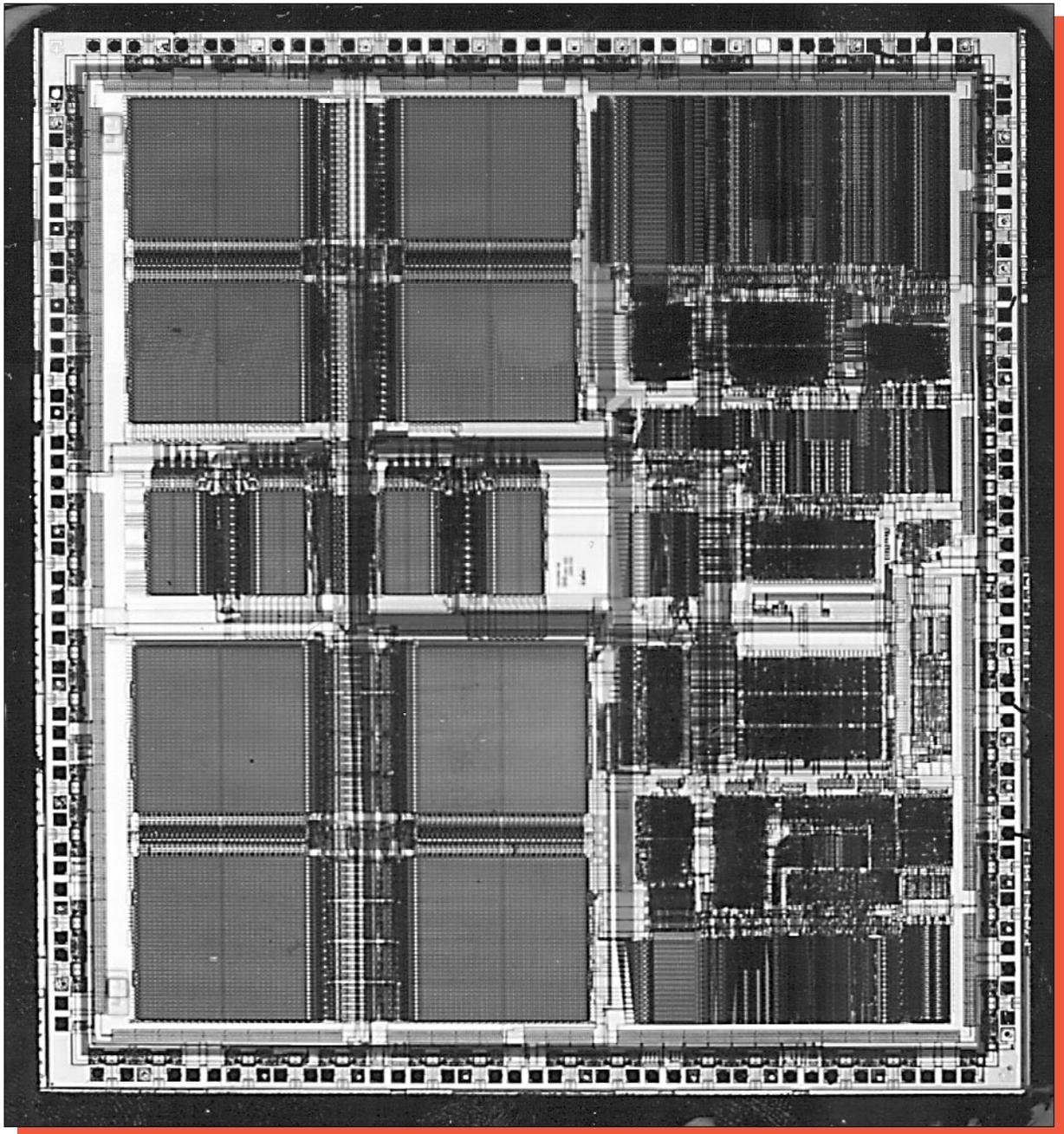
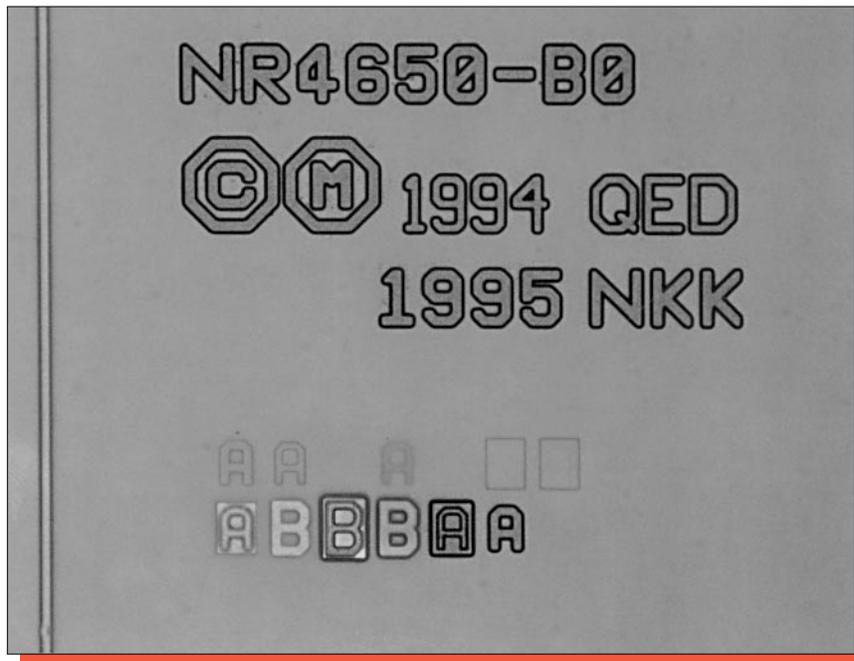
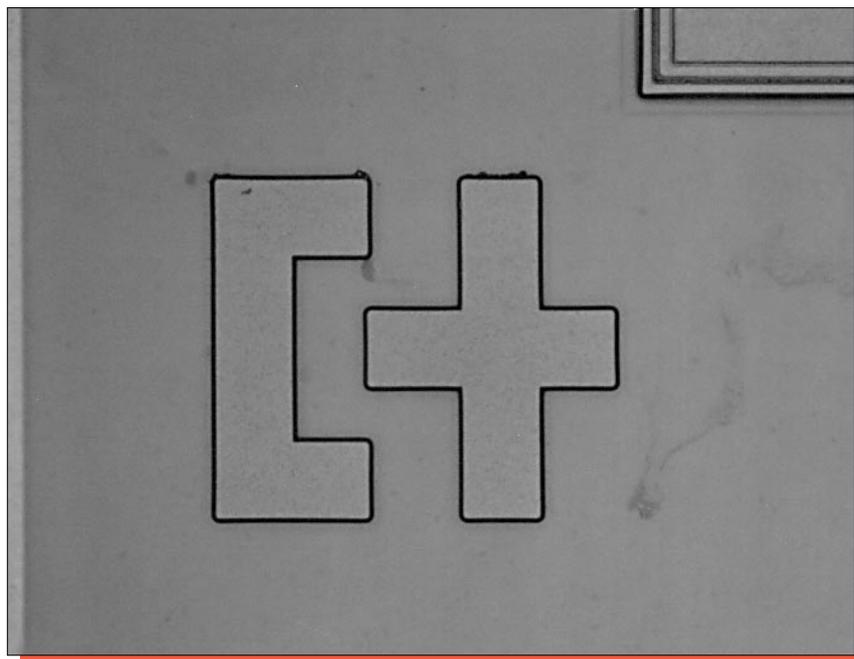


Figure 5. Whole die photograph of the NKK NR4645 Microprocessor. Mag. 21x.



Mag. 320x



Mag. 500x

Figure 6. Optical views of markings on the die surface.

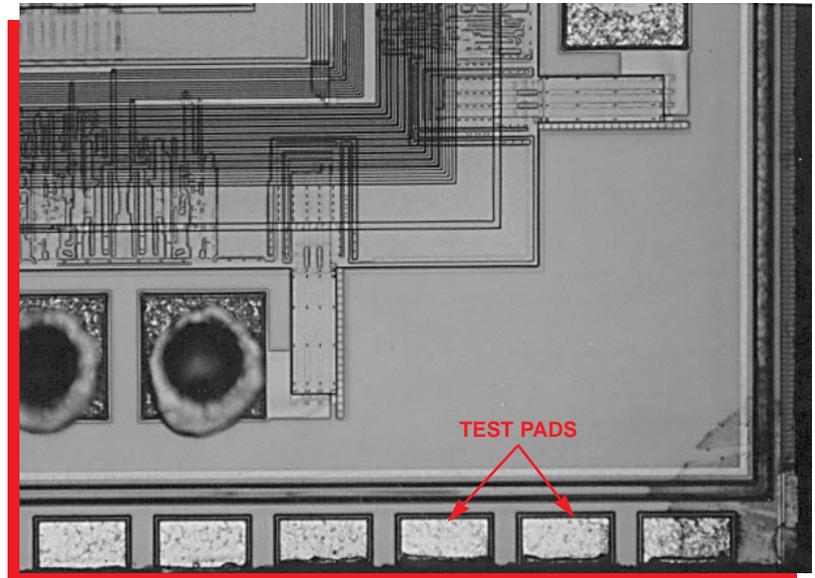
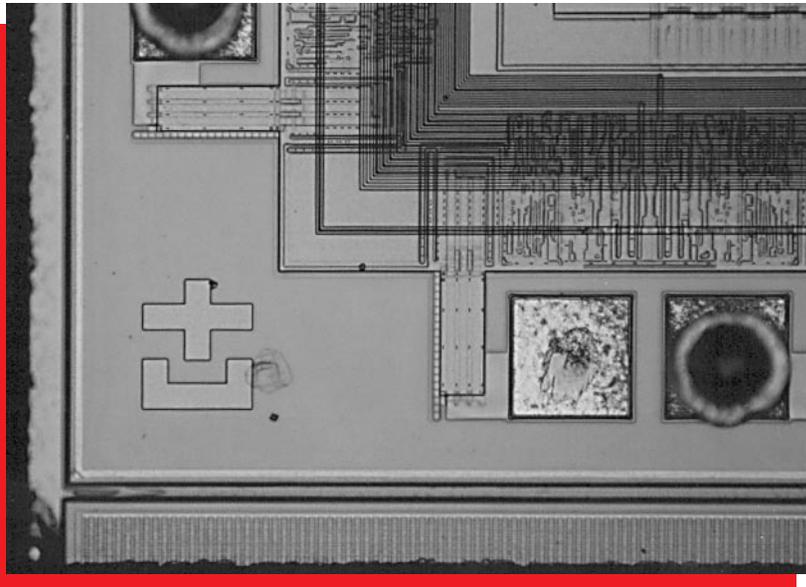
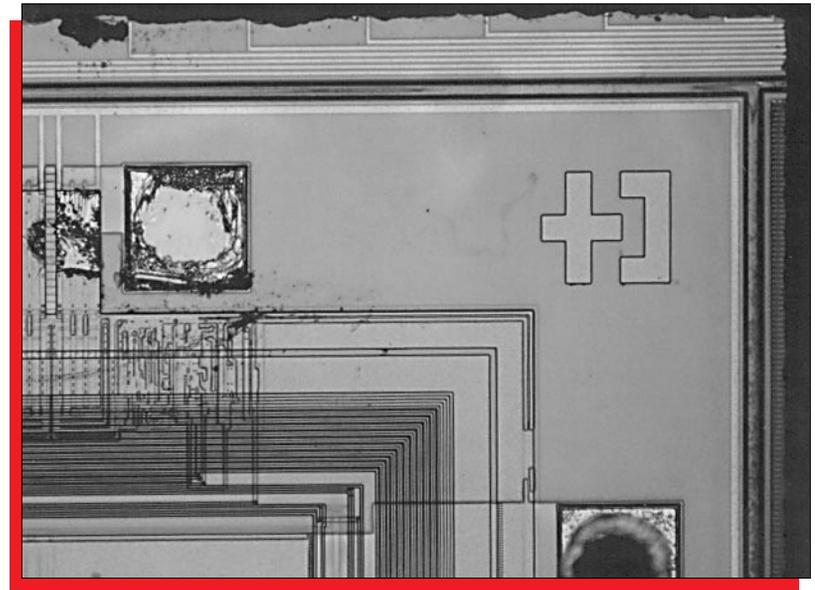
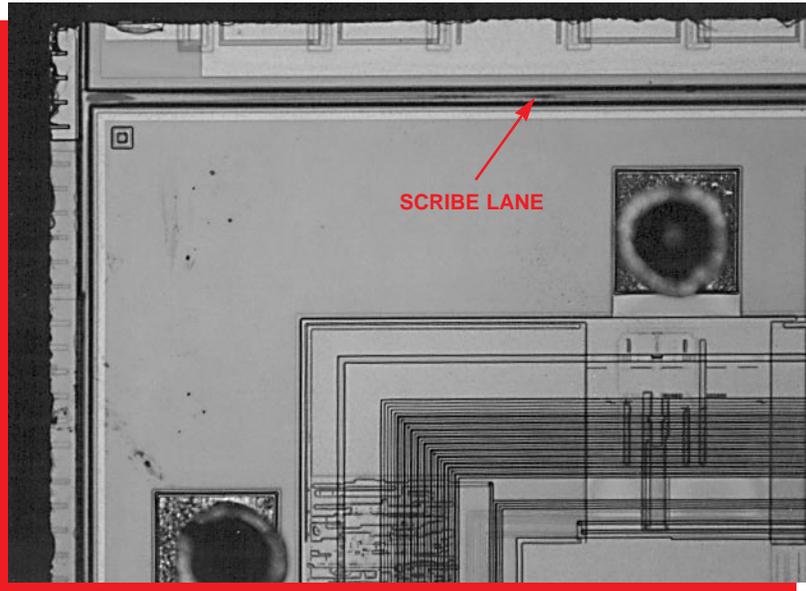
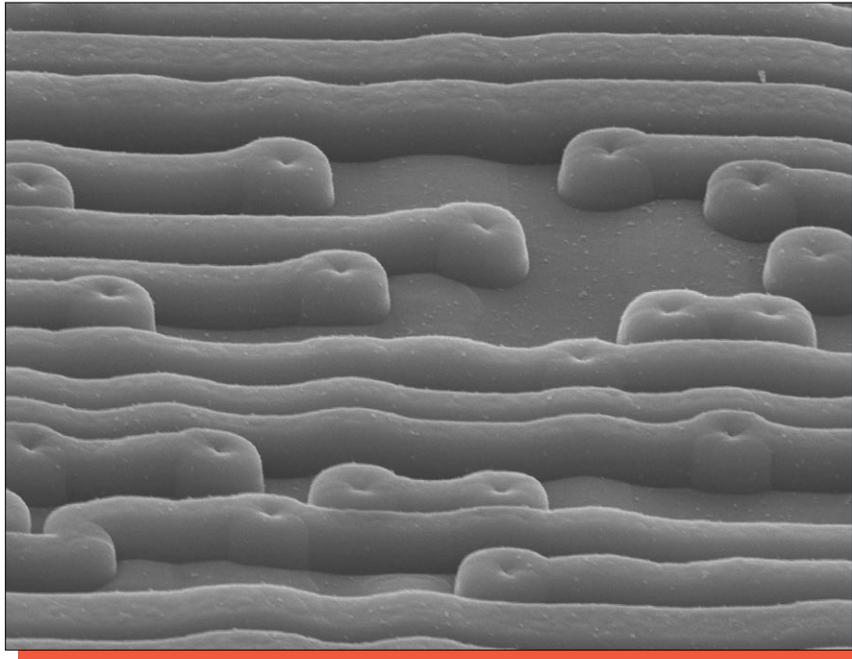
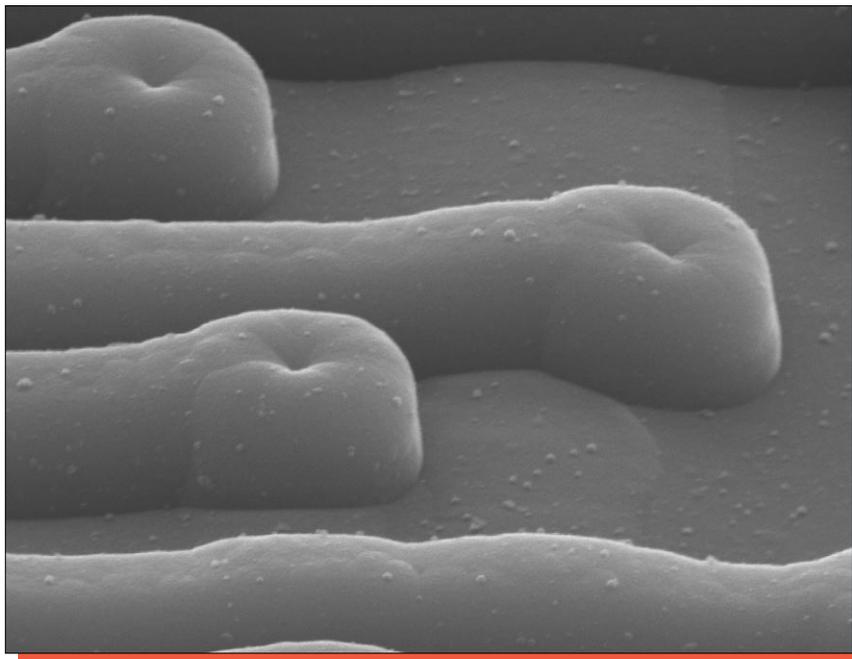


Figure 7. Optical views of the die corners. Mag. 160x.



Mag. 4000x



Mag. 10,000x

Figure 8. Perspective SEM views illustrating overlay passivation coverage. 60°.

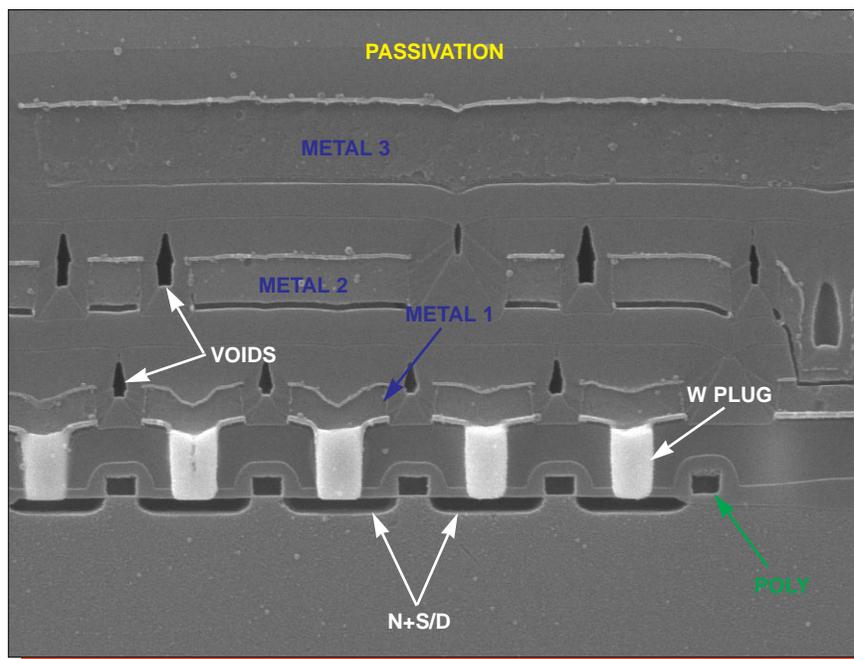
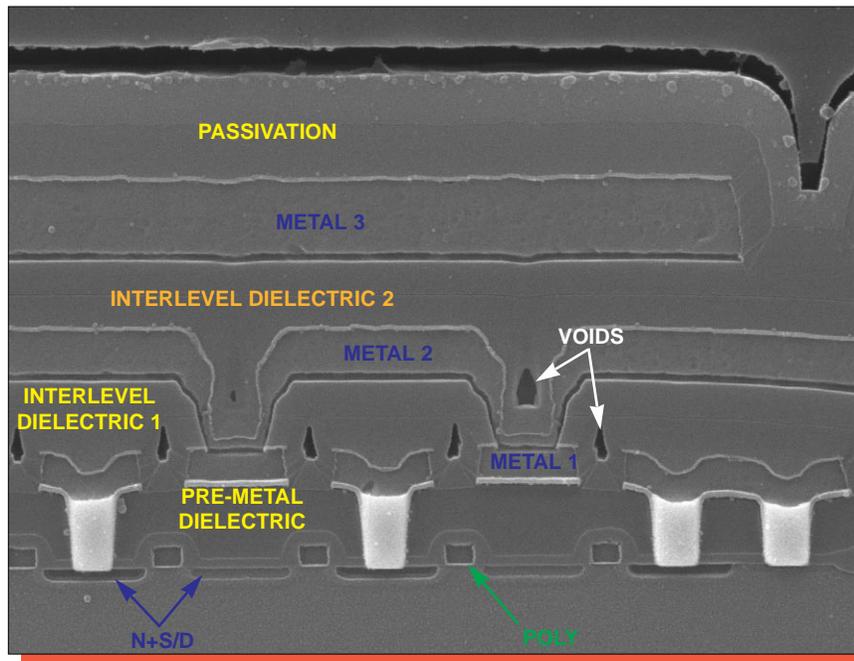
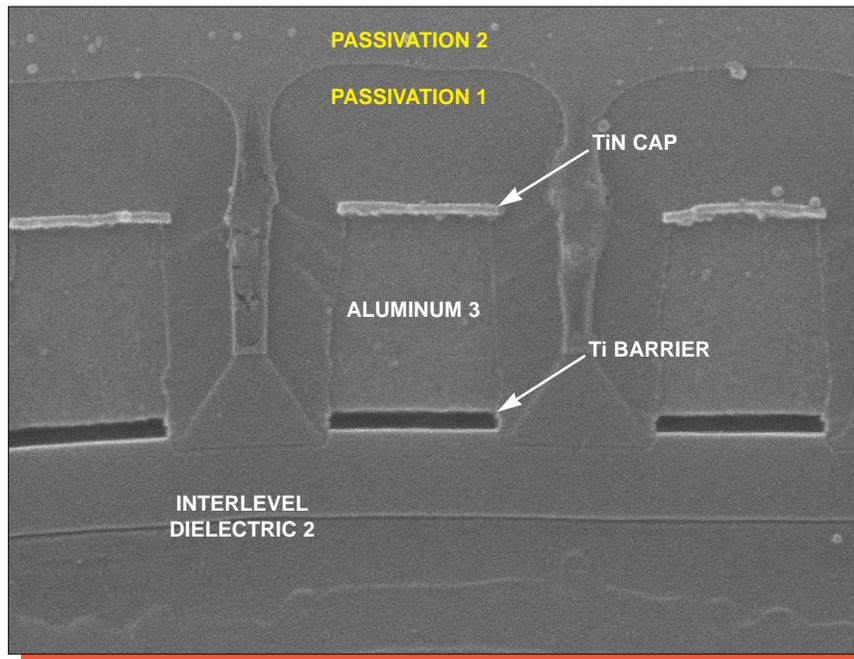
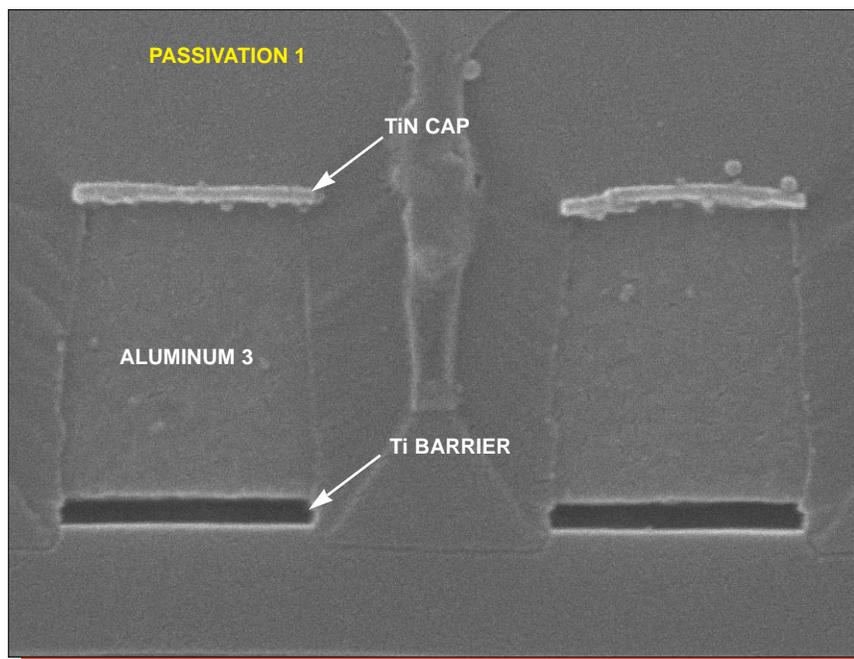


Figure 9. SEM section views illustrating general device structure. Mag. 10,000x.

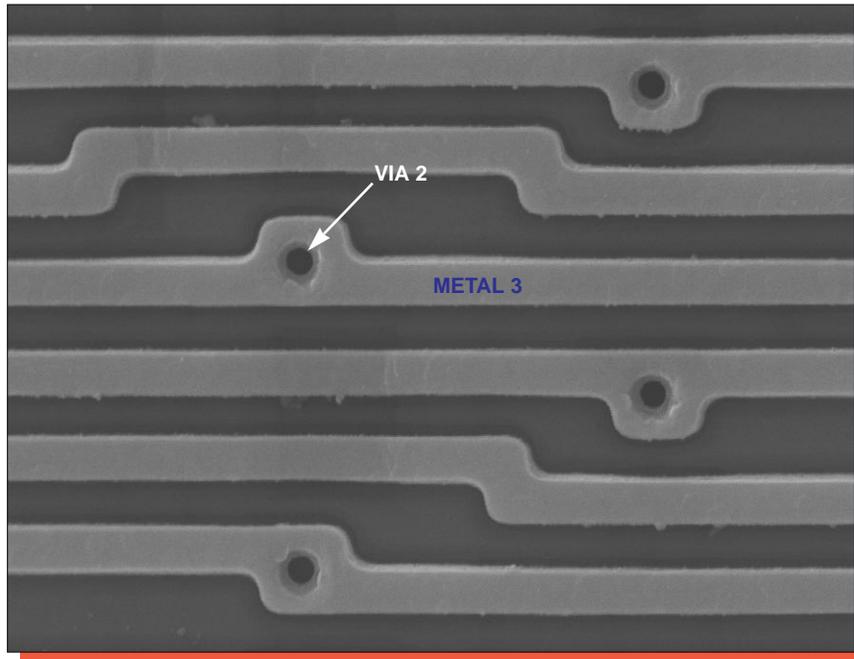


Mag. 26,000x

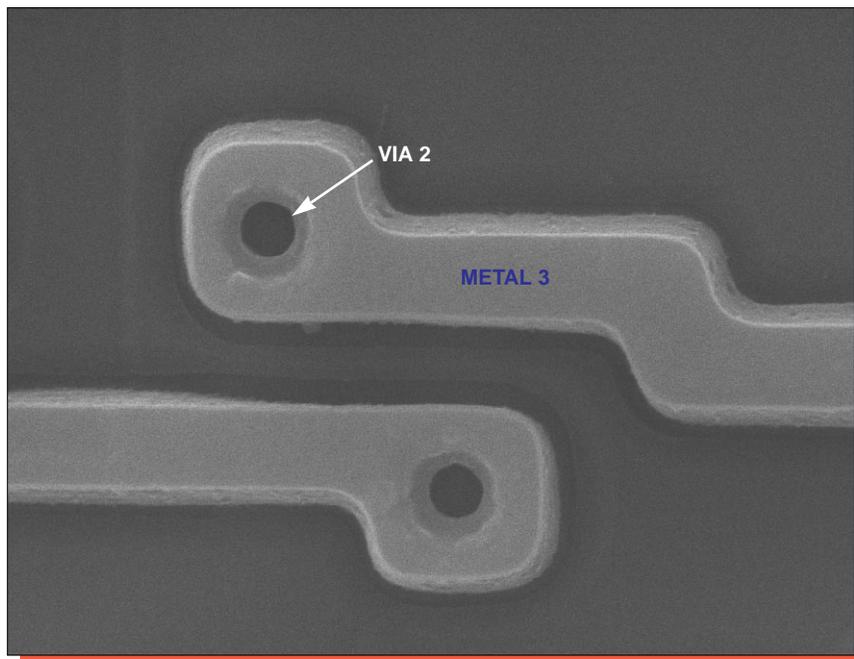


Mag. 40,000x

Figure 10. SEM section views of metal 3 line profiles.

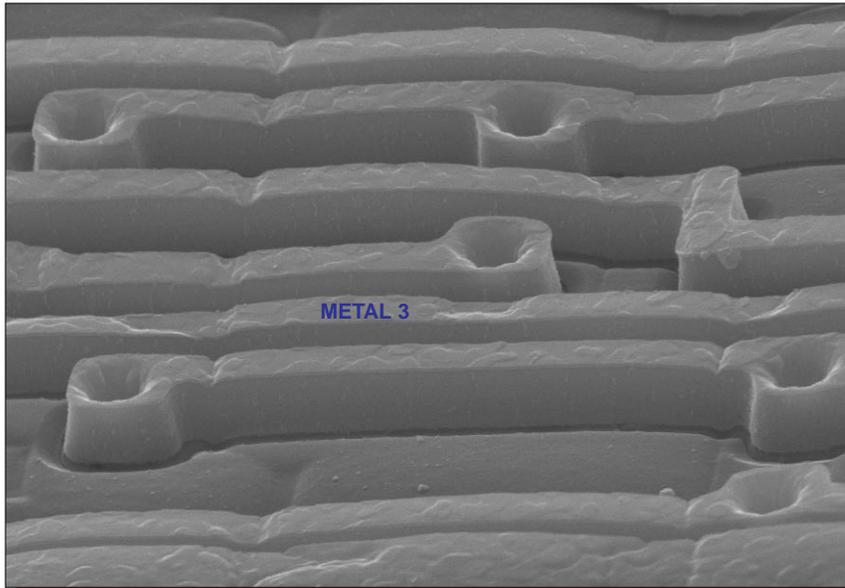


Mag. 6500x

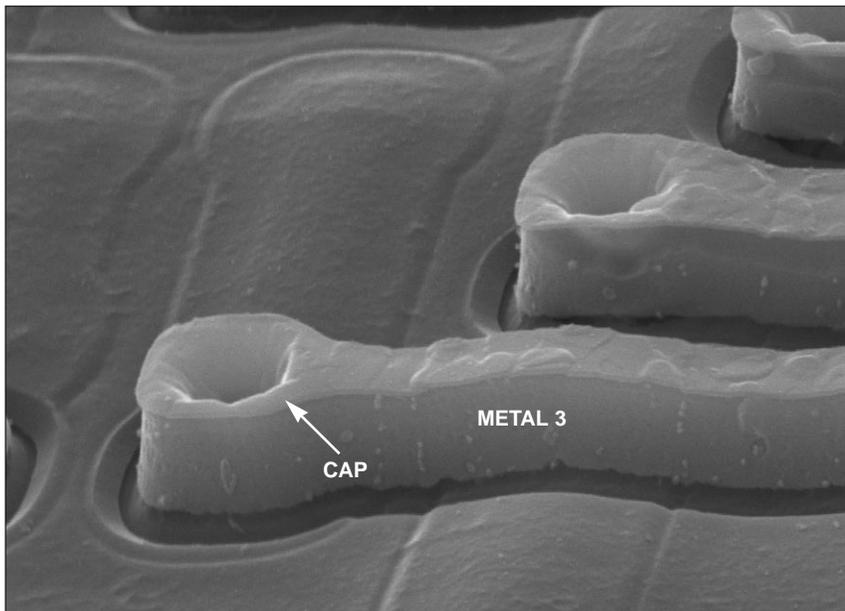


Mag. 13,000x

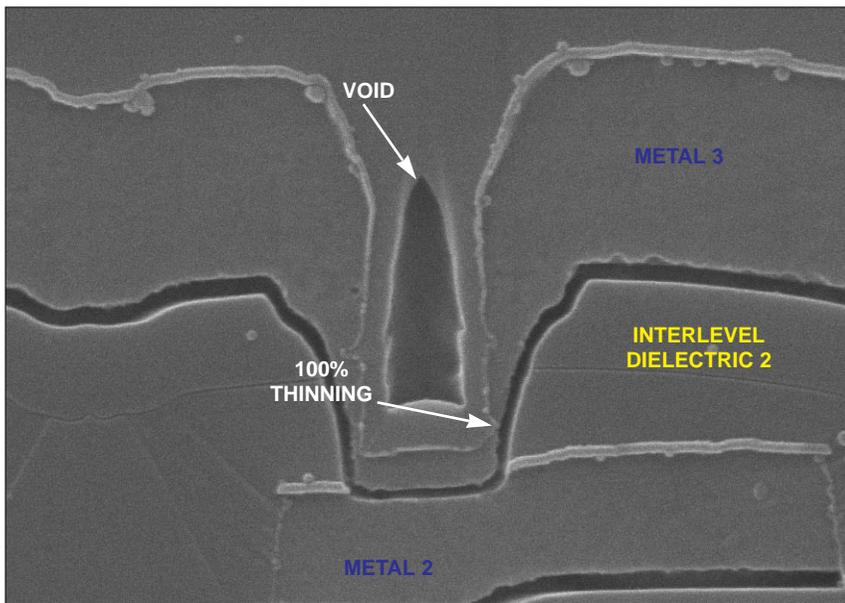
Figure 11. Topological SEM views illustrating metal 3 patterning. 0°.



Mag. 7700x, 60°

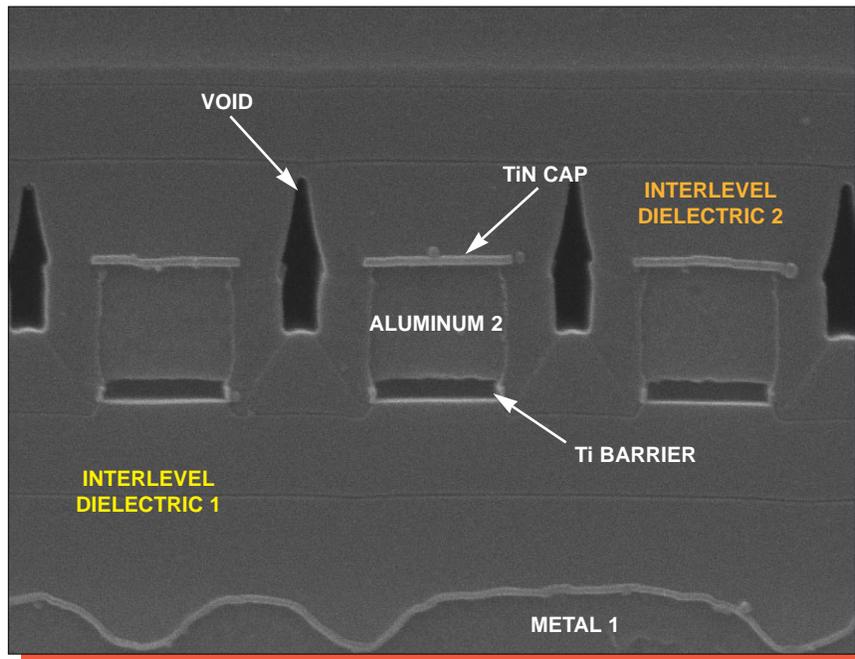


Mag. 13,000x, 60°

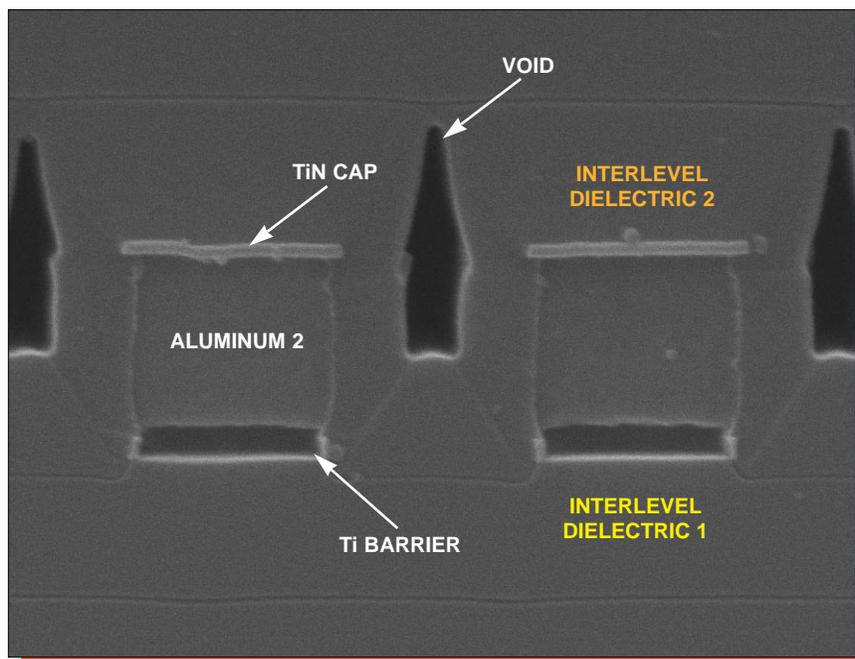


Mag. 26,000x

Figure 12. SEM views illustrating metal 3 step coverage and a metal 3-to-metal 2 via.

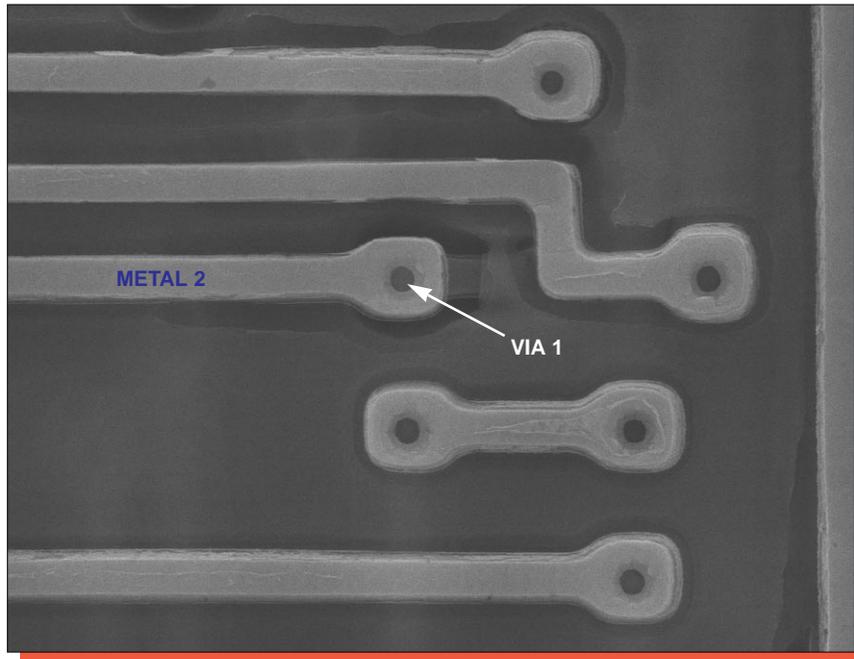


Mag. 26,000x

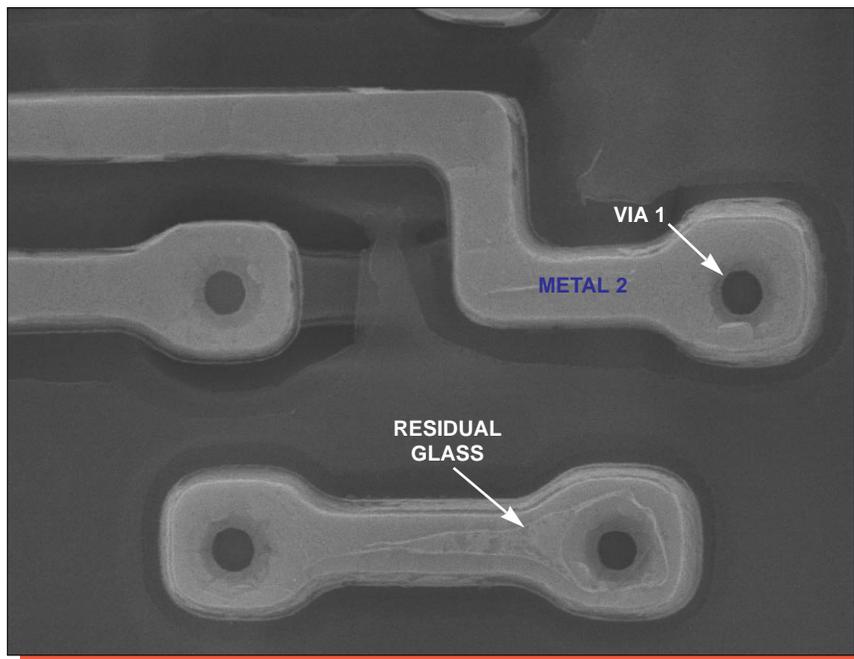


Mag. 40,000x

Figure 13. SEM section views of metal 2 line profiles.

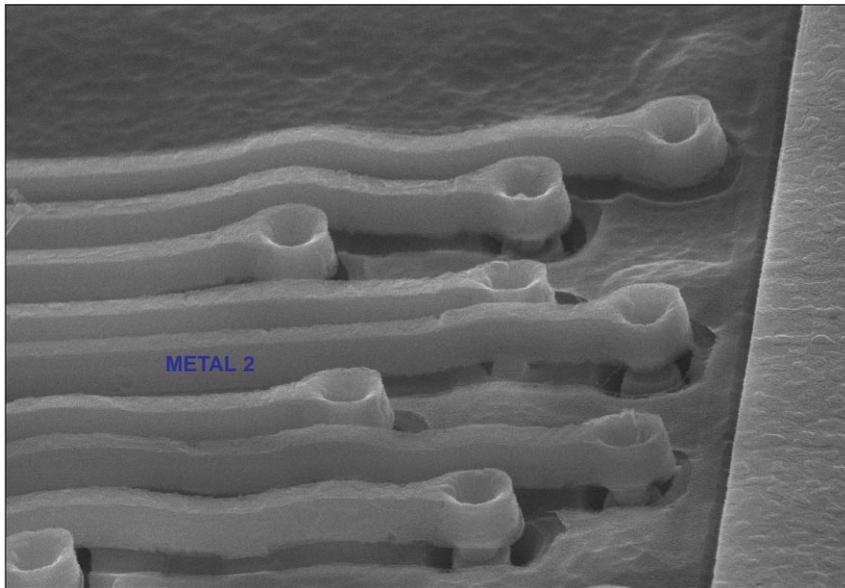


Mag. 6200x

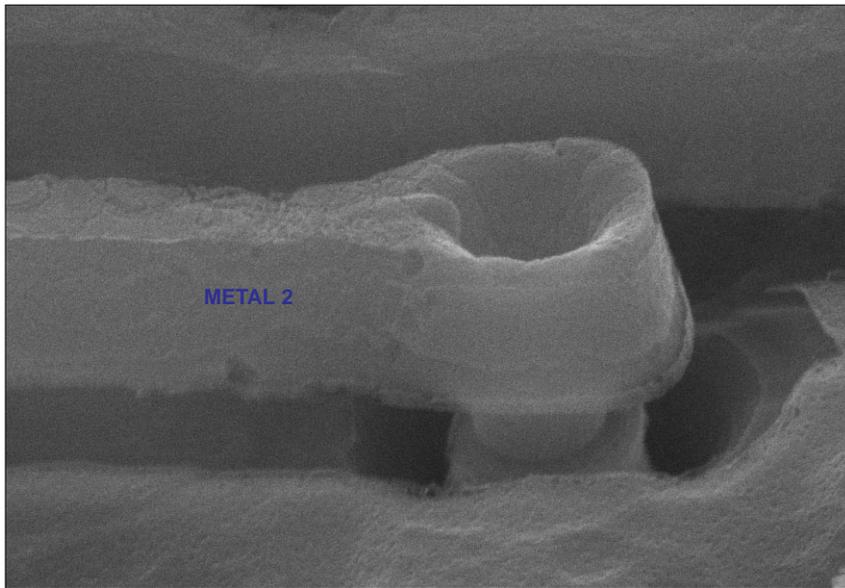


Mag. 10,000x

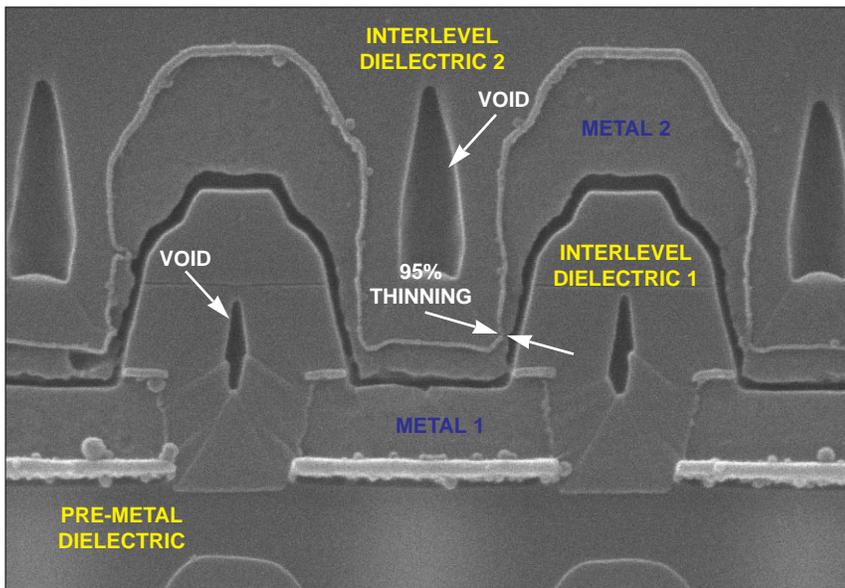
Figure 14. SEM section views of metal 2 patterning. 0°.



Mag. 6000x, 60°

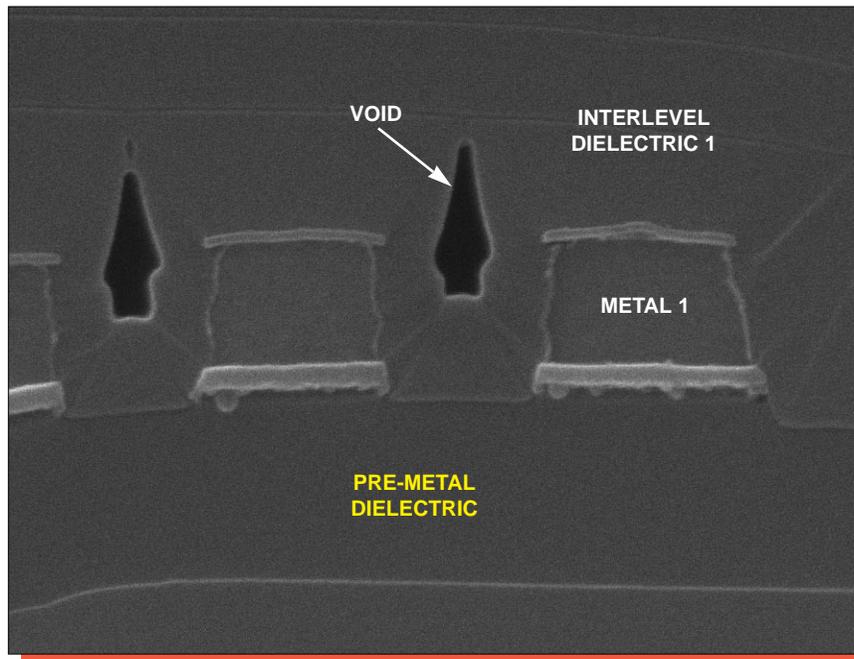


Mag. 20,000x, 60°

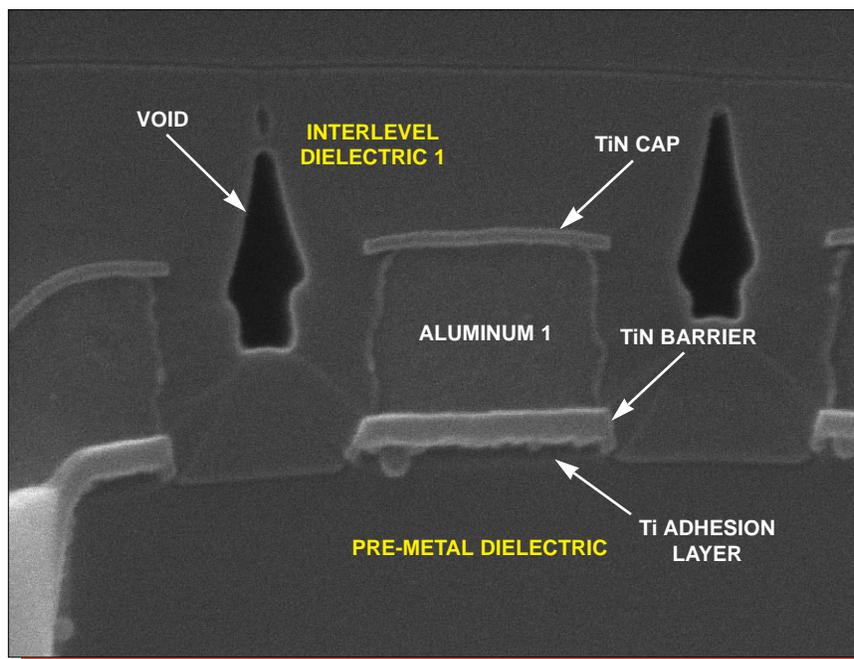


Mag. 26,000x,

Figure 15. SEM views illustrating metal 2 step coverage and metal 2-to-metal 1 via.

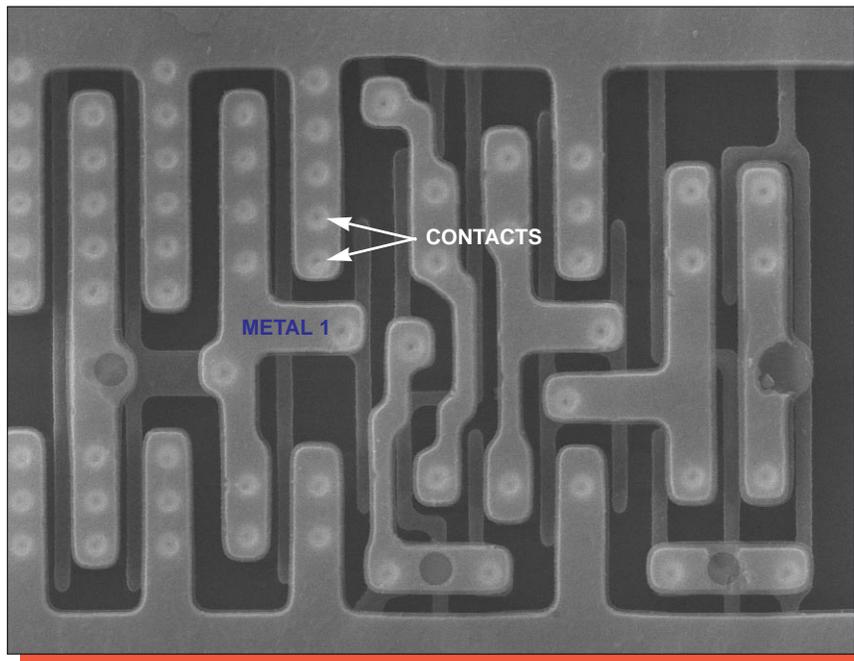


Mag. 40,000x

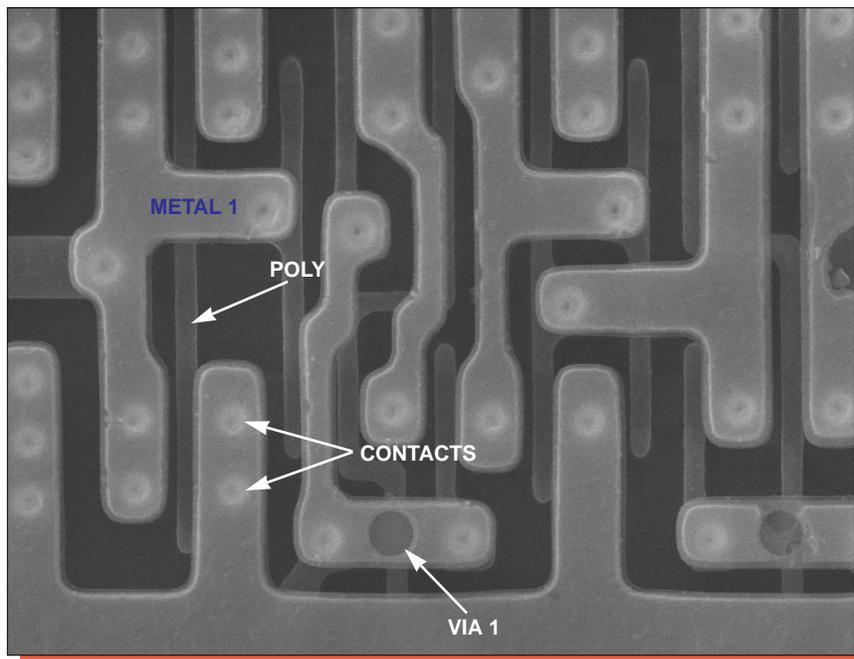


Mag. 52,000x

Figure 16. SEM section views of metal 1 line profiles.

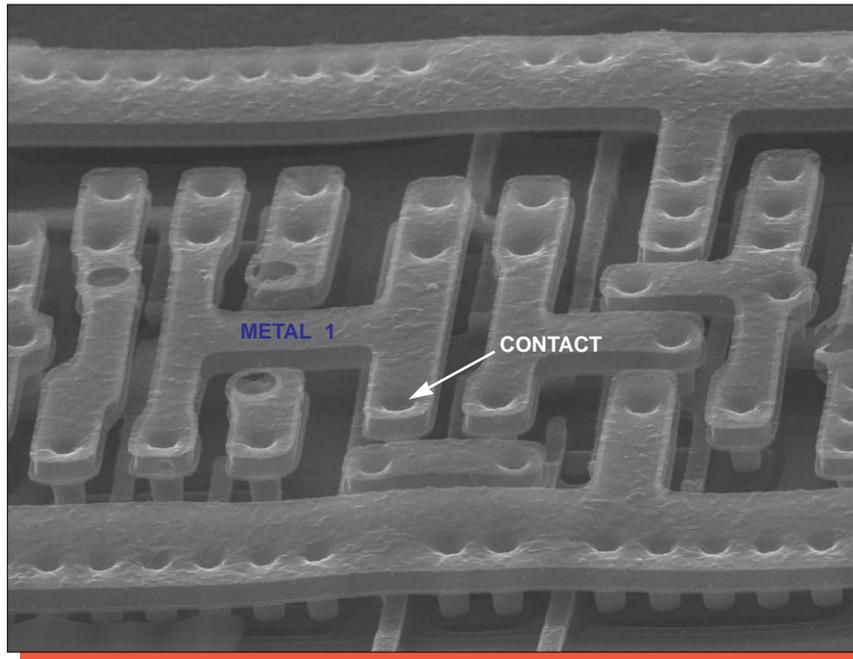


Mag. 5000x

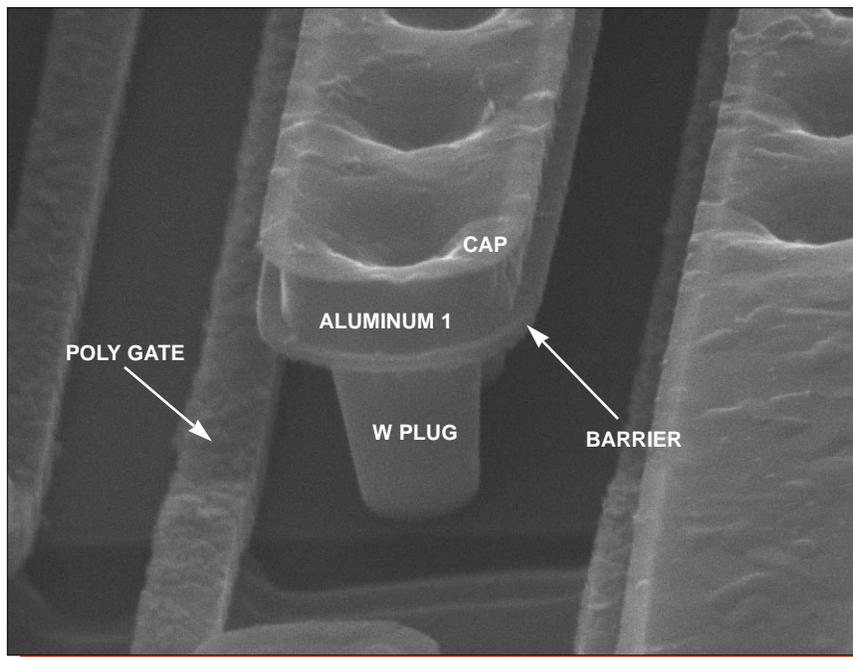


Mag. 6500x

Figure 17. Topological SEM views of metal 1 patterning. 0°.

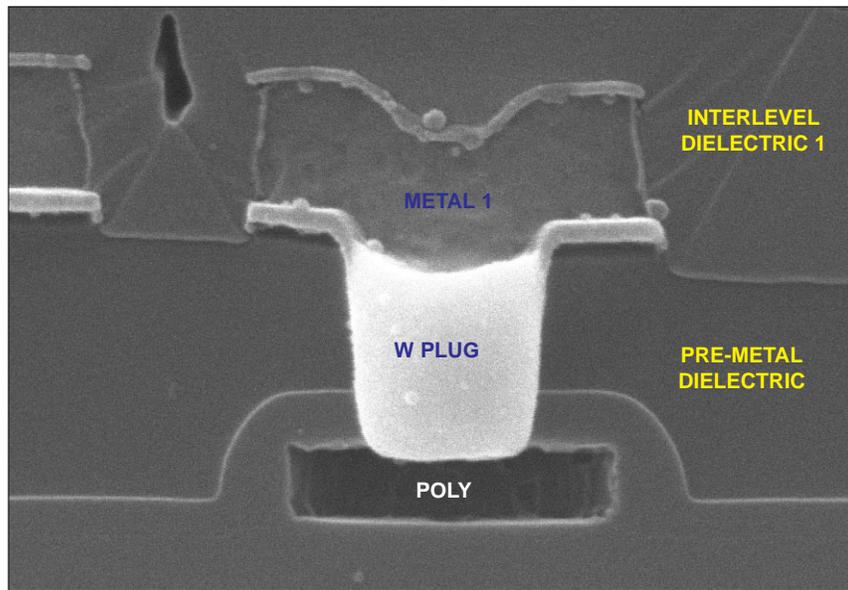


Mag. 6500x

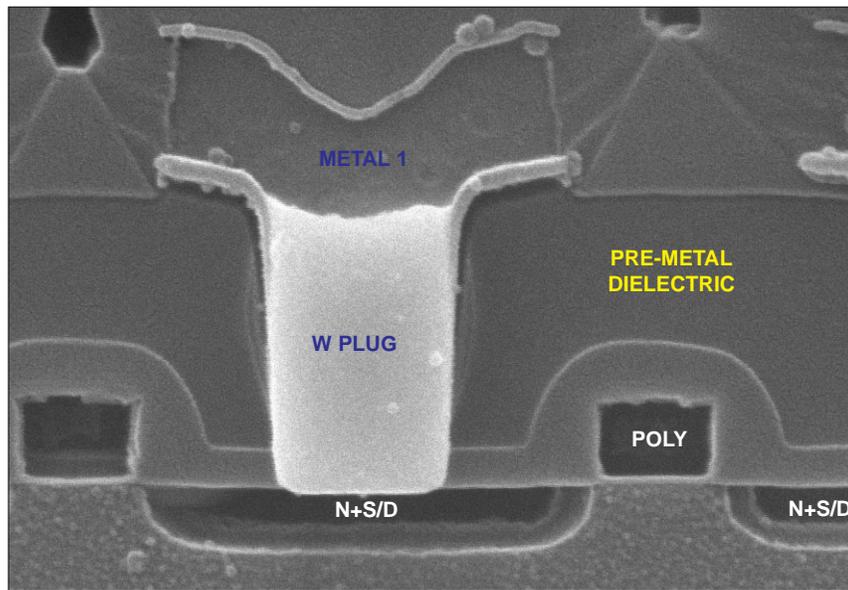


Mag. 26,000x

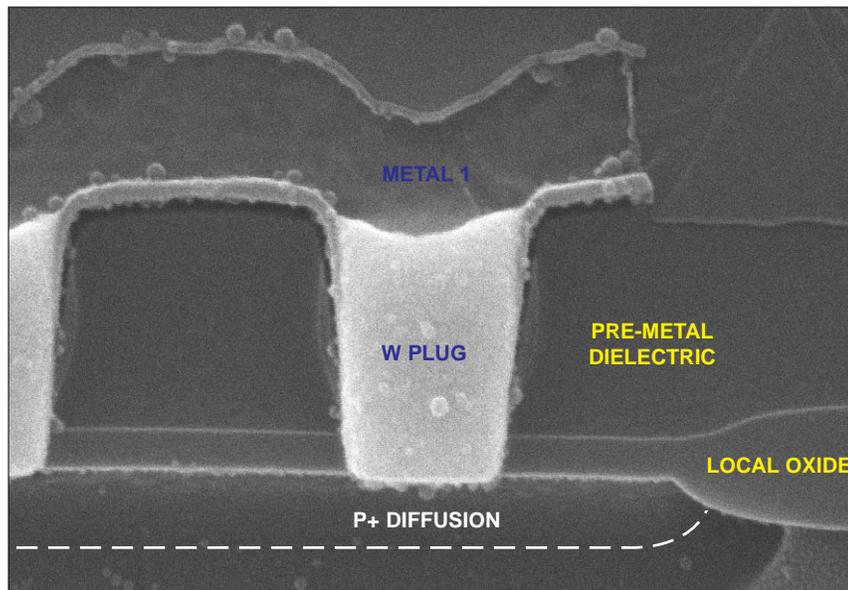
Figure 18. Perspective SEM views illustrating metal 1 step coverage. 60°.



metal 1-to-poly

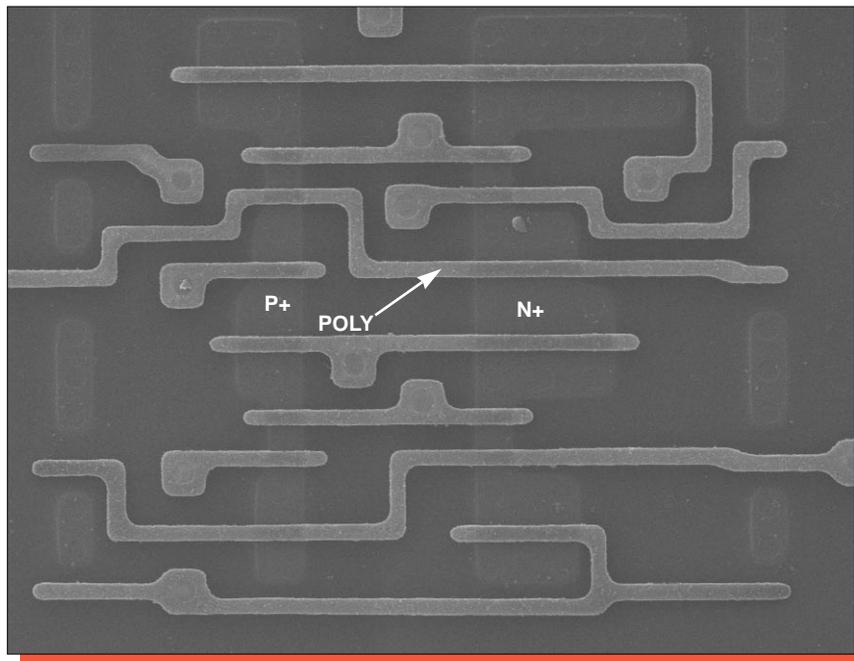


metal 1-to-N+

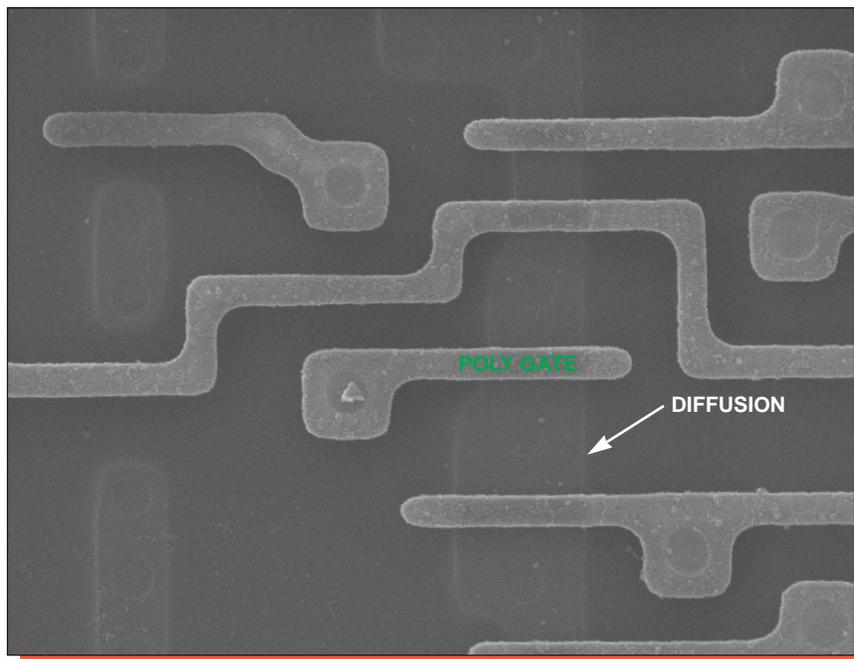


metal 1-to P+

Figure 19. SEM section views of metal 1 contacts (silicon etch). Mag. 40,000x.

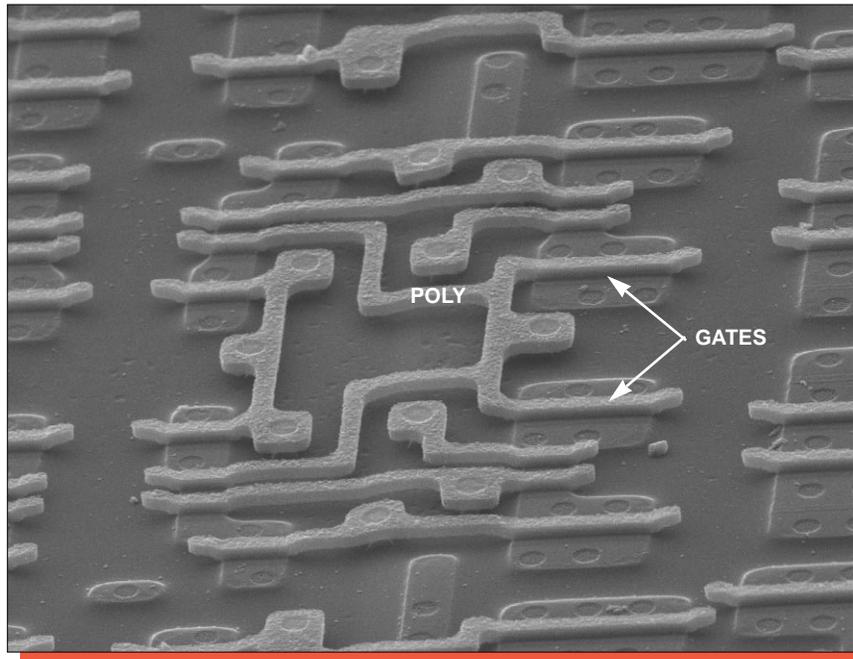


Mag. 5000x

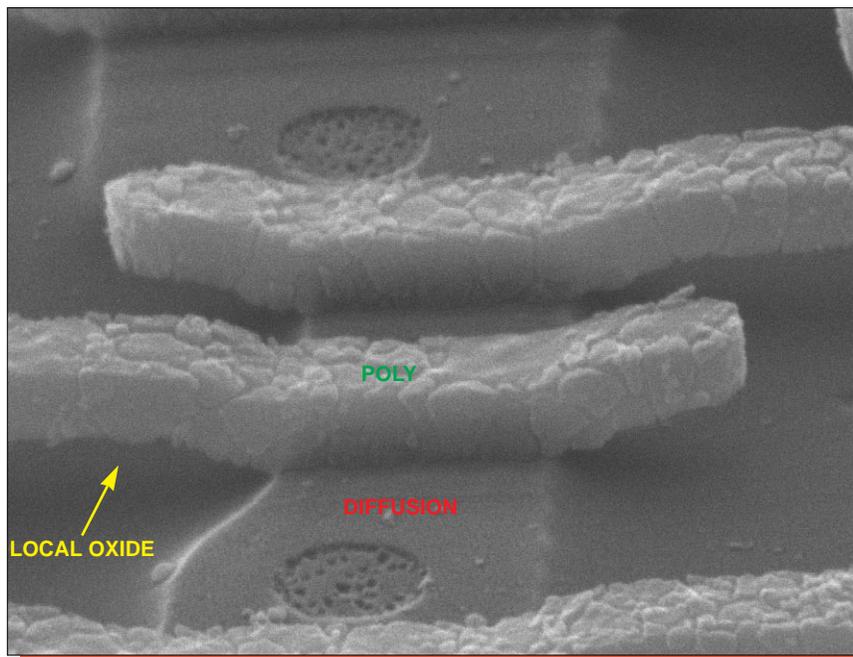


Mag. 10,000x

Figure 20. Topological SEM views of poly patterning. 0°.



Mag. 6500x



Mag. 40,000x

Figure 21. Perspective SEM views of poly coverage. 60°.

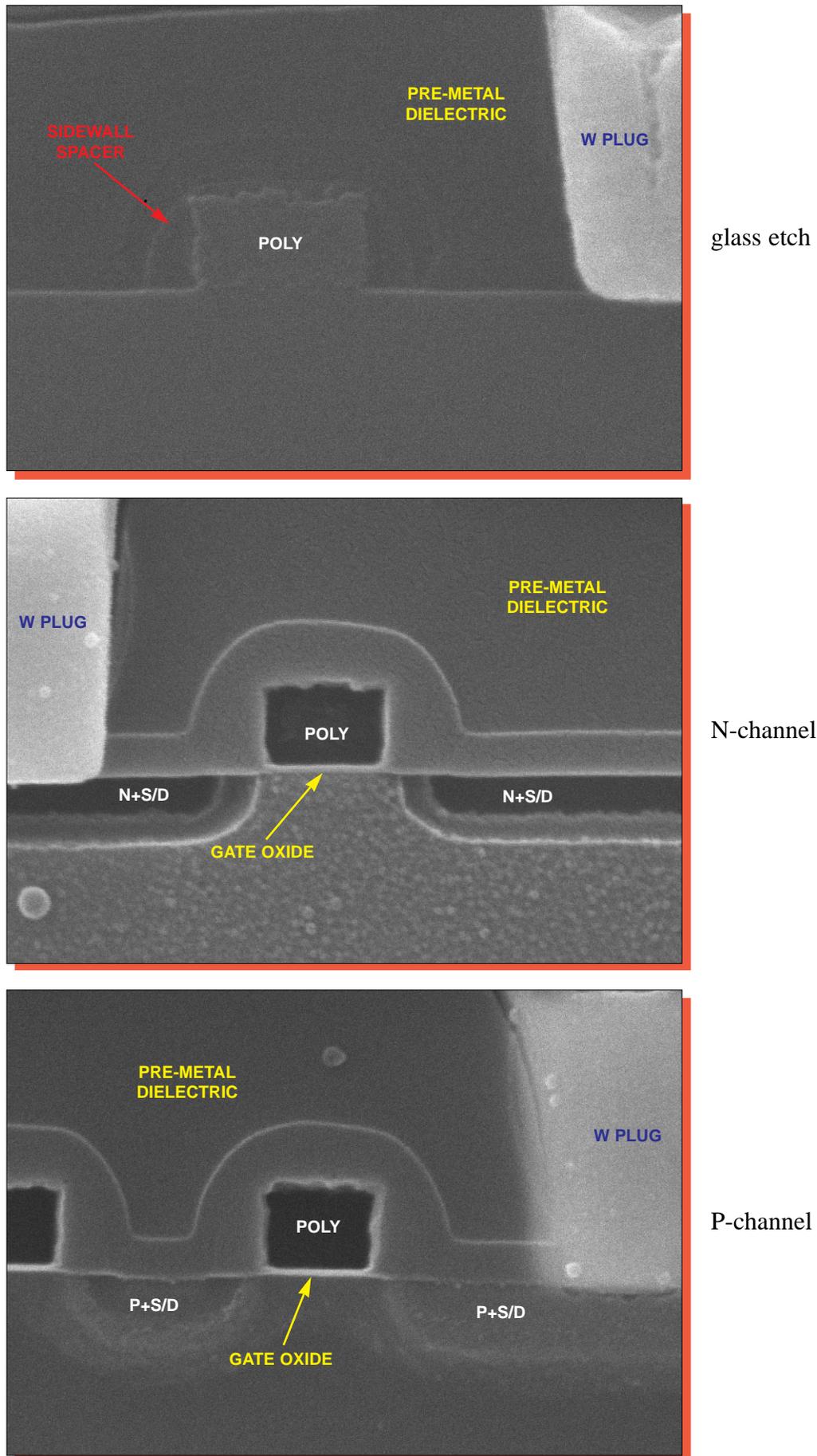


Figure 22. SEM section views of typical transistors. Mag. 52,000x.

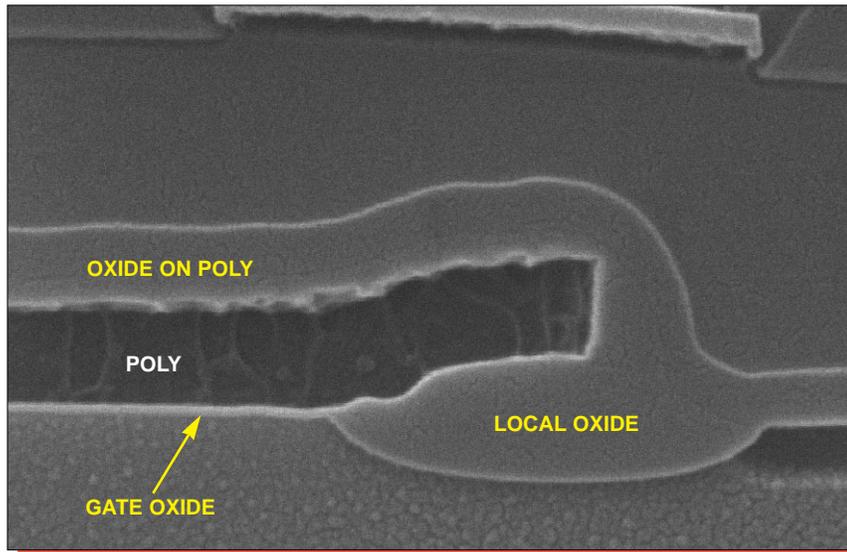
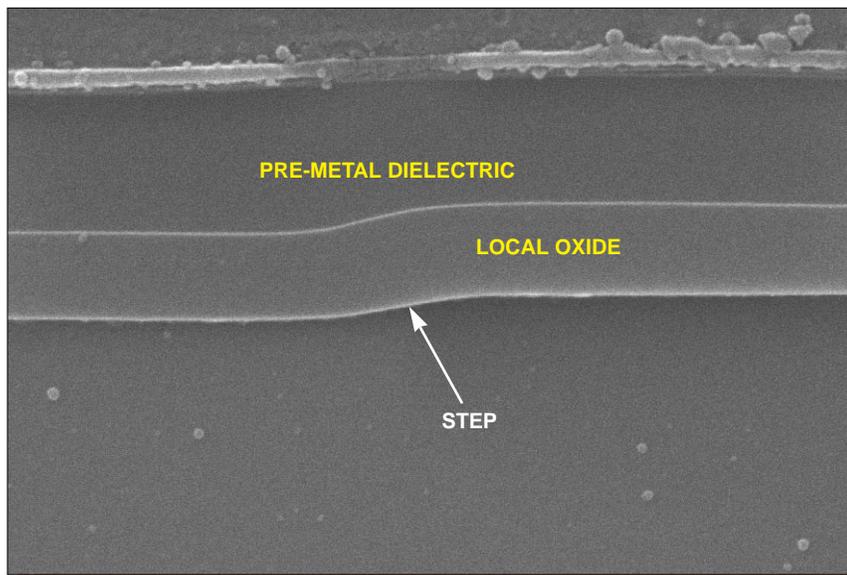
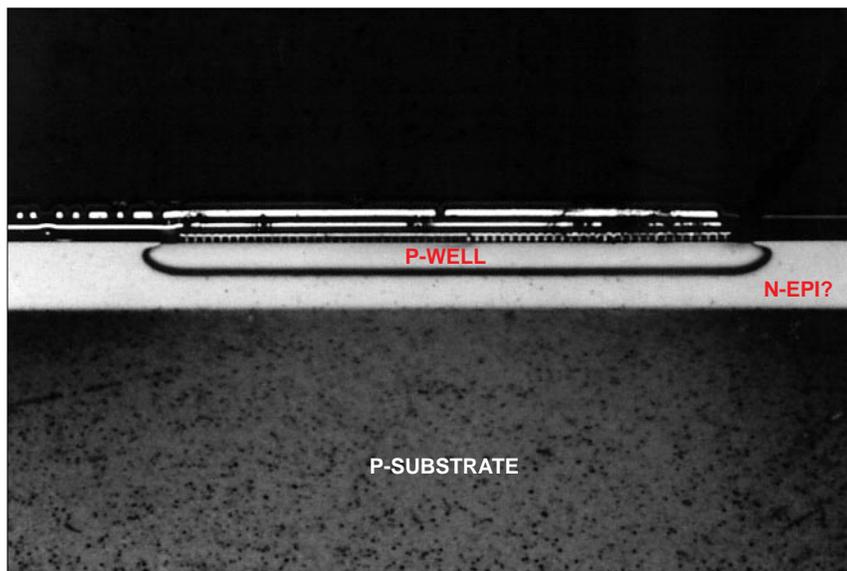


Figure 23. SEM section view of a typical local oxide birdsbeak. Mag. 52,000x.

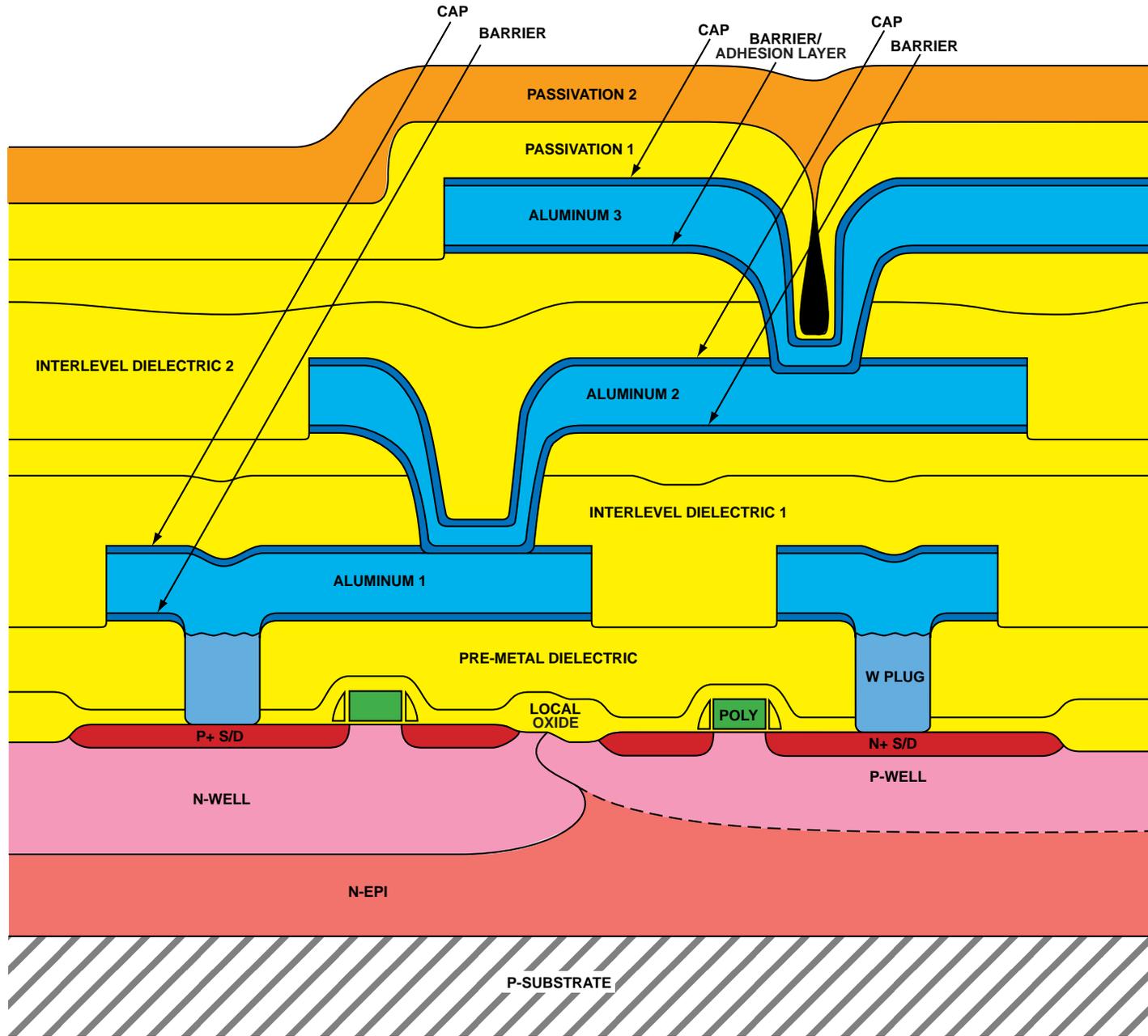


Mag. 26,000x



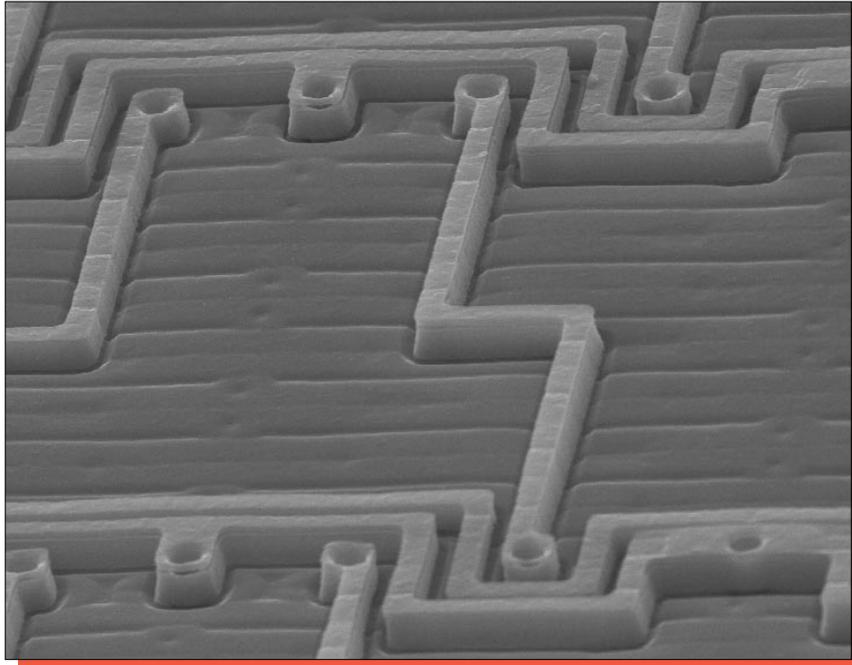
Mag. 800x

Figure 23a. Section views illustrating the well structure. Mag. 800x.

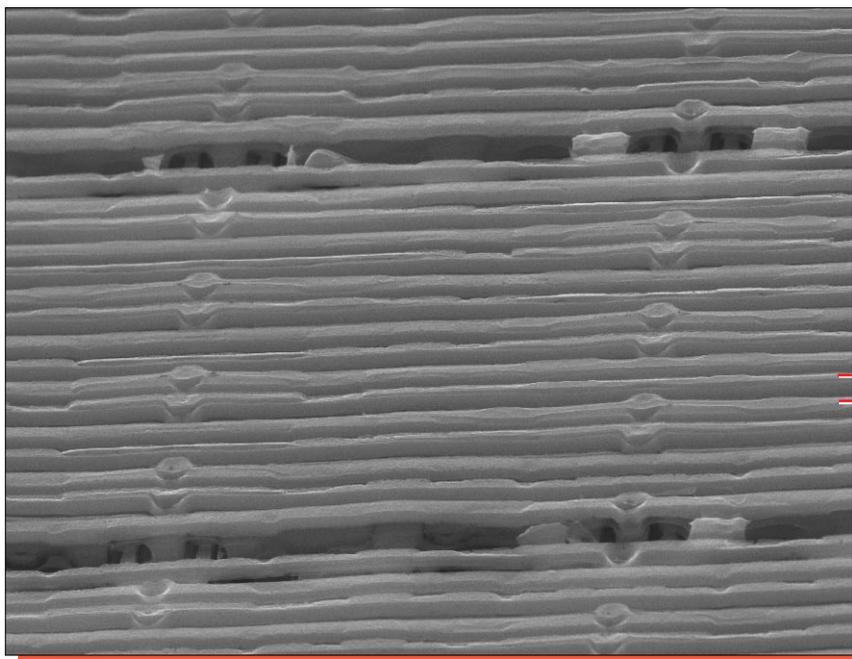


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

Figure 24. Color cross section drawing illustrating device structure.

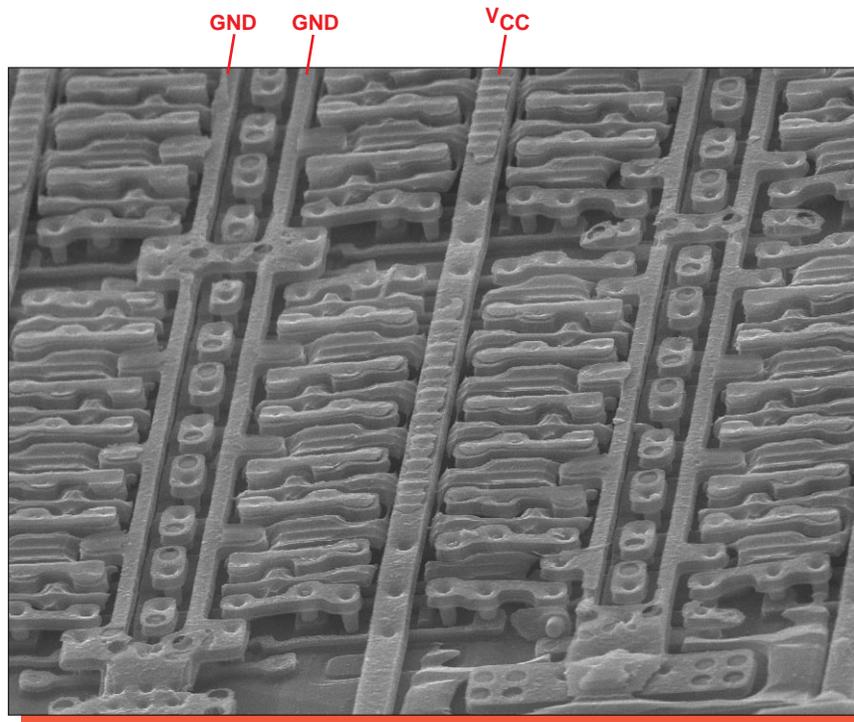


metal 3

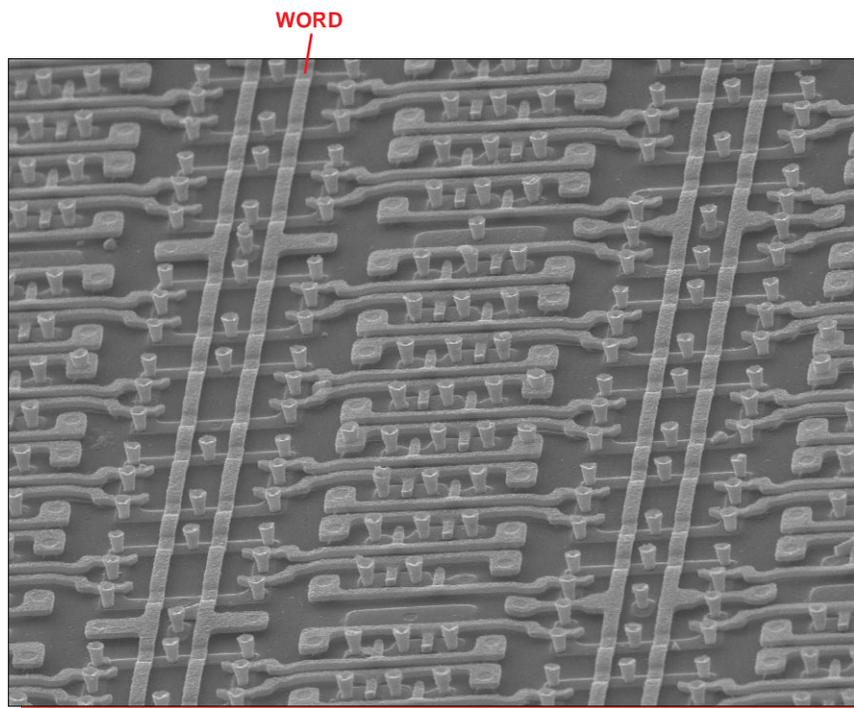


metal 2

Figure 25. Perspective SEM views of the 6T SRAM cell array. Mag. 3200x, 60°.

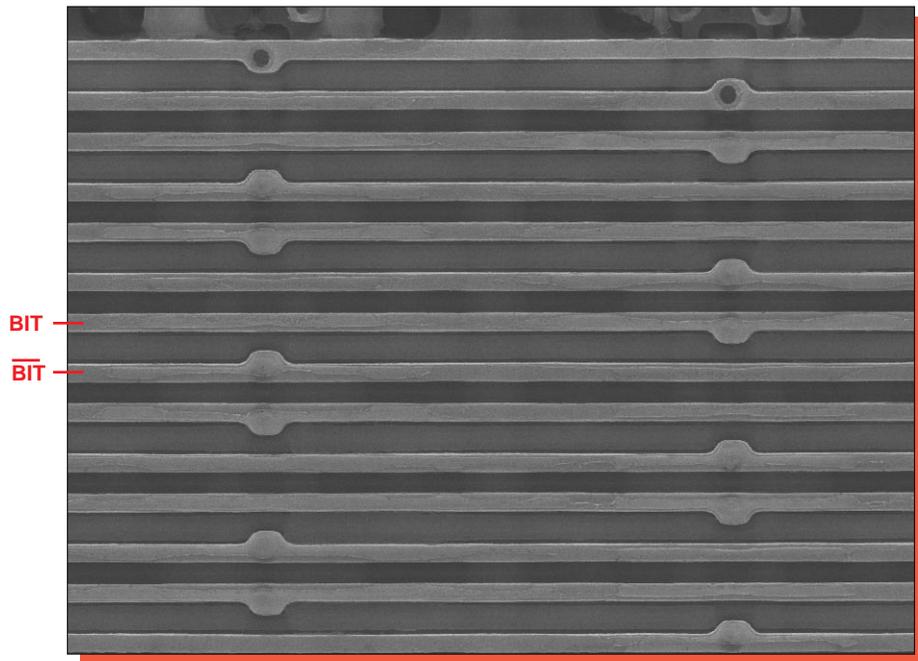


metal 1

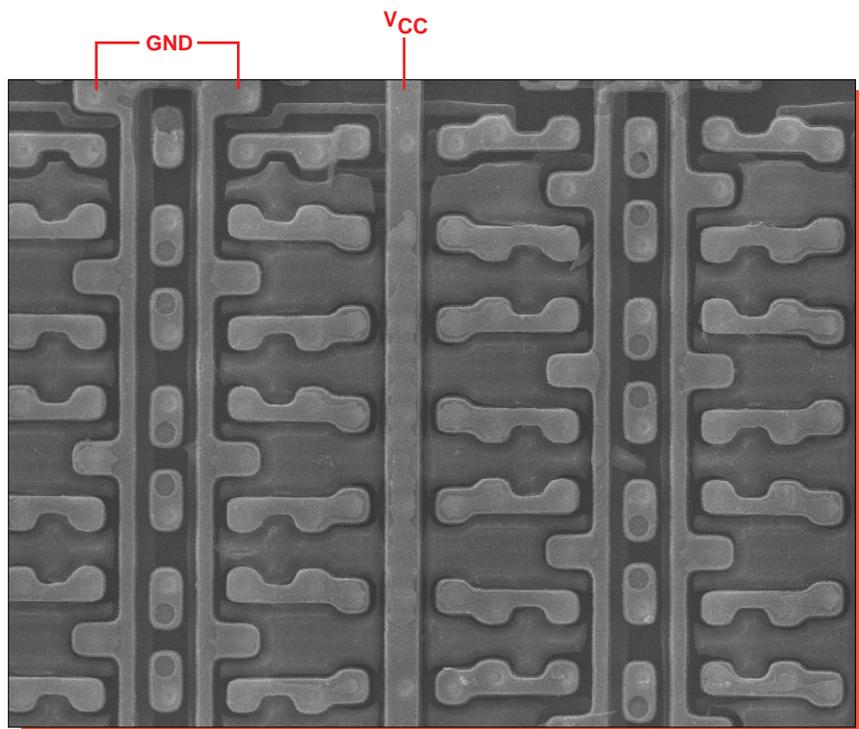


poly

Figure 26. Perspective SEM views of the 6T SRAM cell array. Mag. 3200x, 60°.

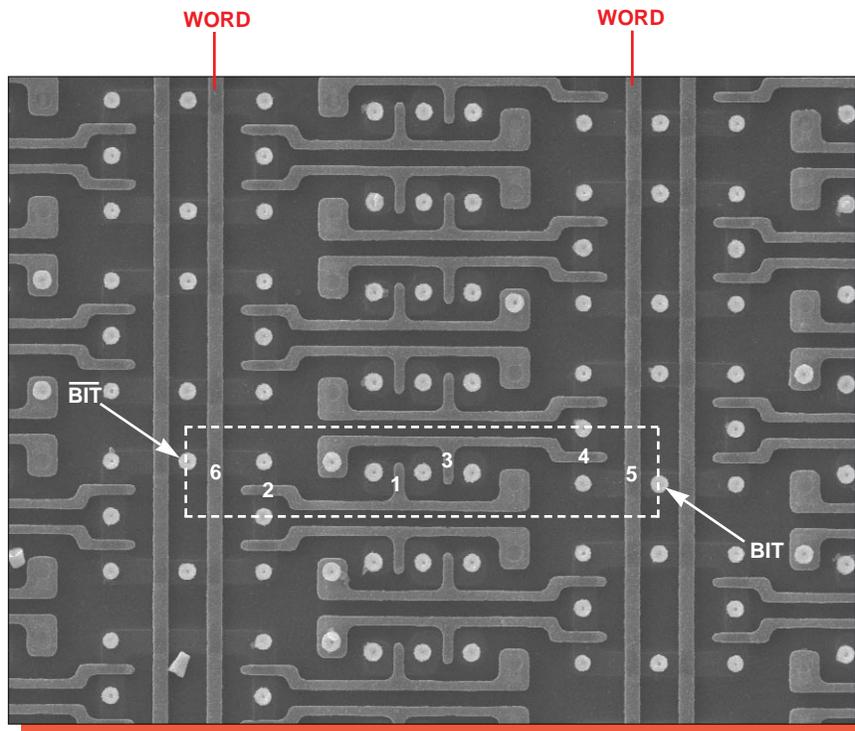


metal 2



metal 1

Figure 27. Topological SEM views of the 6T SRAM cell array. Mag. 3200x, 0°.



poly

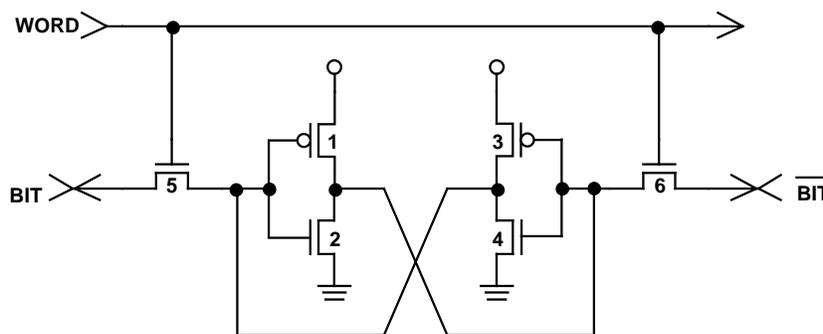
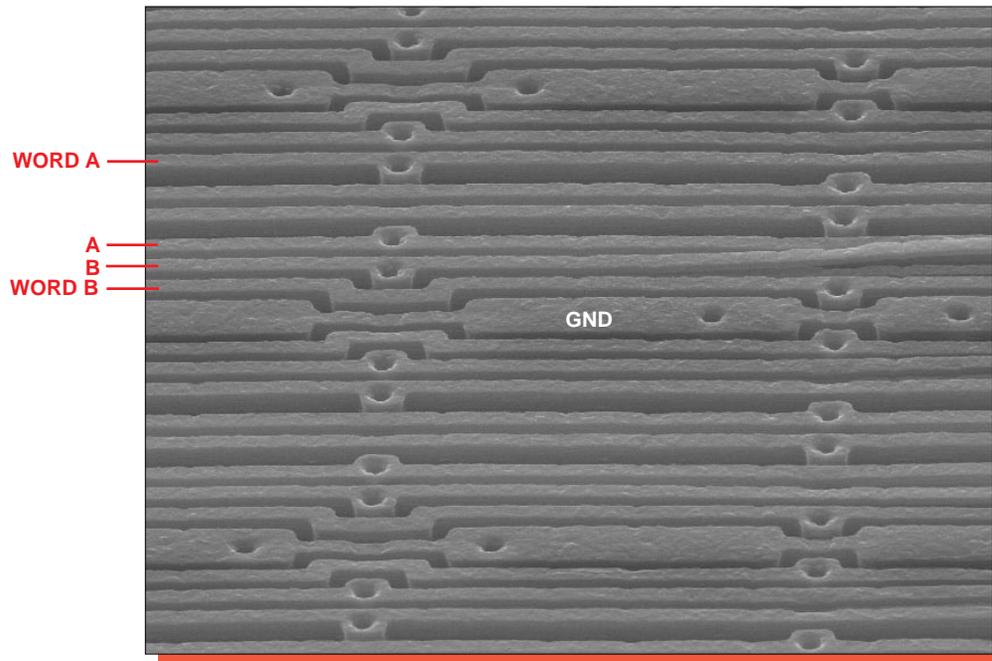
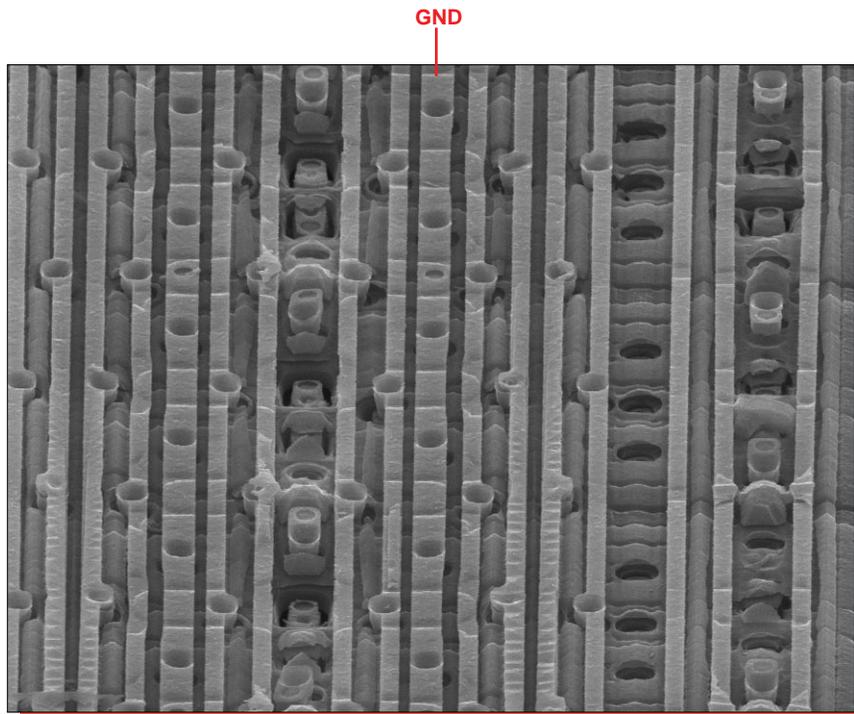


Figure 28. Topological view and schematic of the 6T SRAM cell array. Mag. 3200x, 0°.

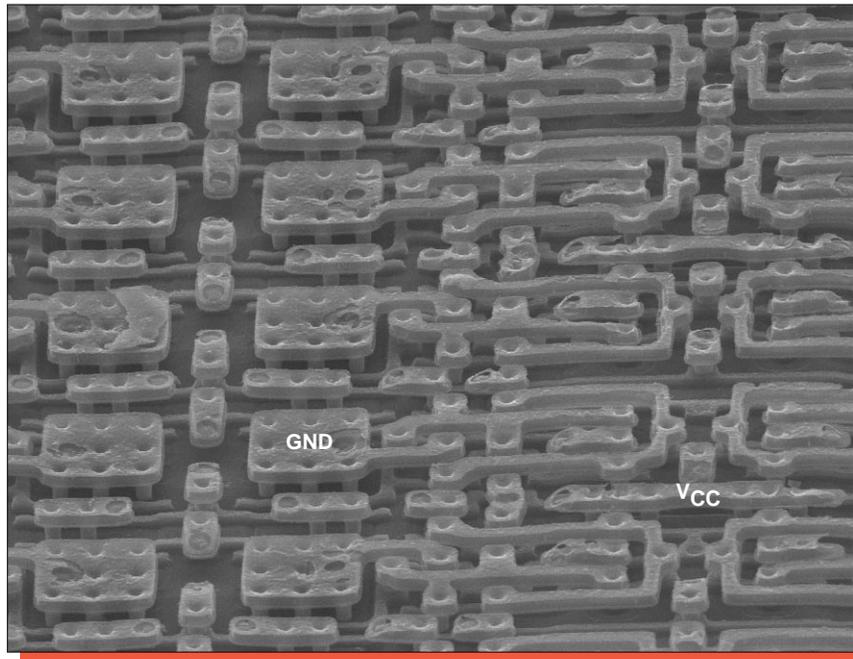


metal 3

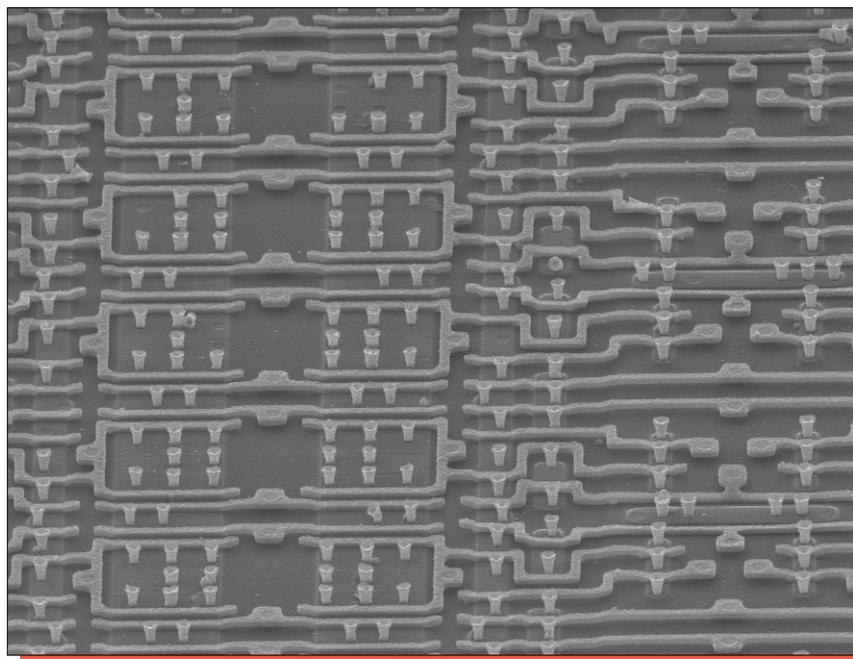


metal 2

Figure 29. Perspective SEM views of the 12T SRAM cell array. Mag. 3200x, 60°.

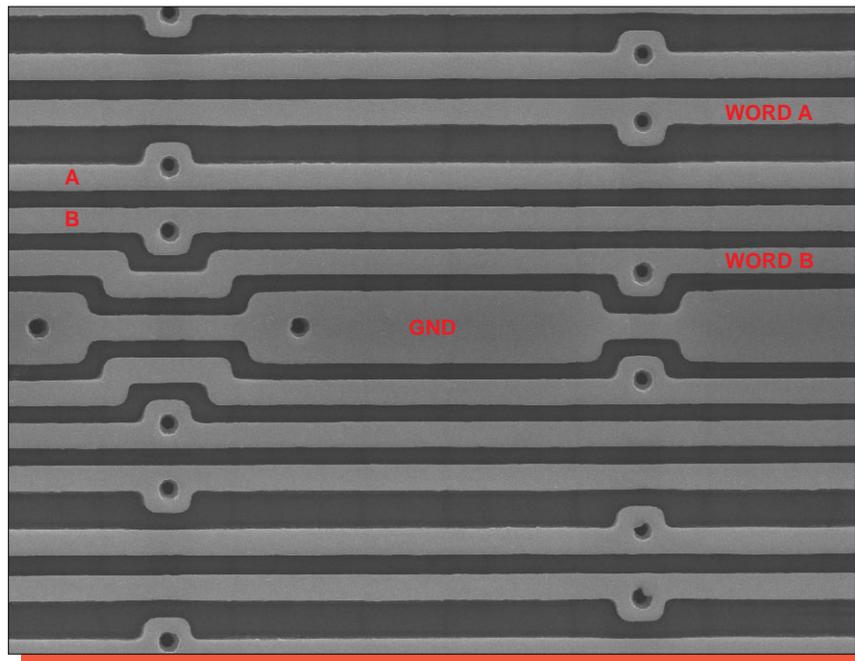


metal 1

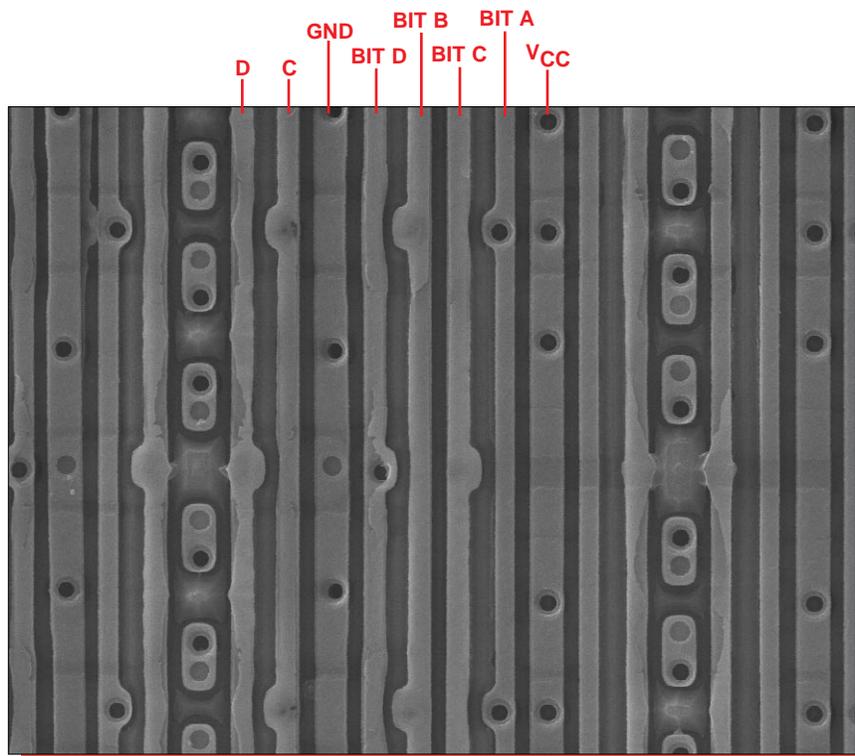


poly

Figure 30. Perspective SEM views of the 12T SRAM cell array. Mag. 3200x, 60°.

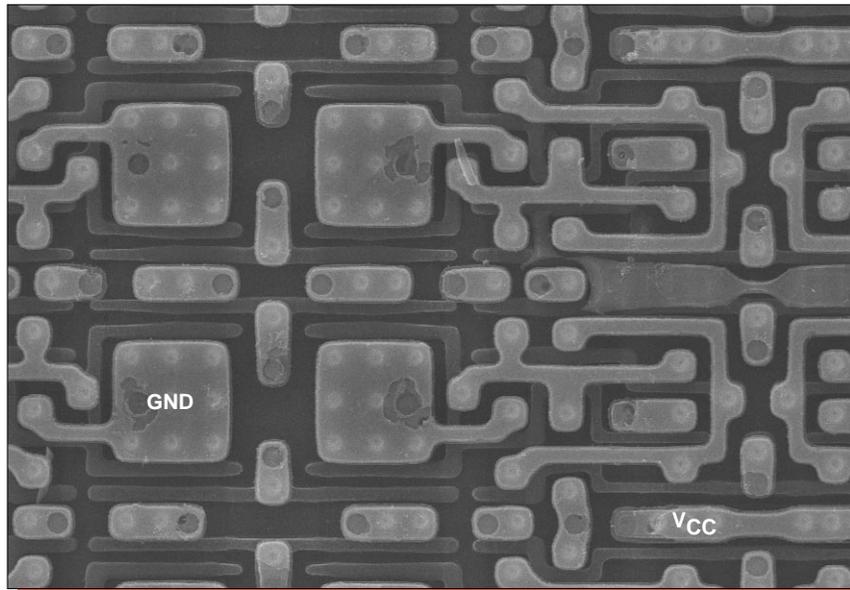


metal 3

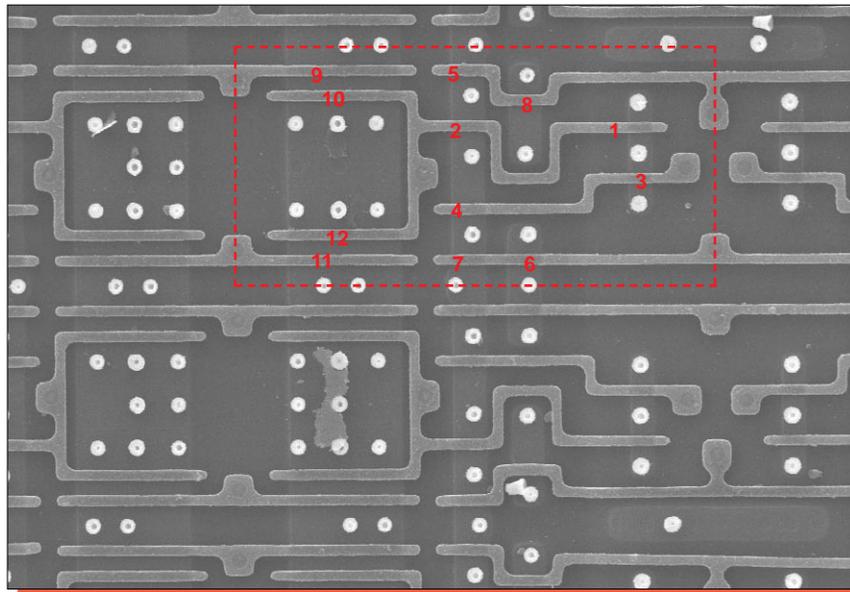


metal 2

Figure 31. Topological SEM views of the 12T SRAM cell array. Mag. 3200x, 0°.



metal 1



poly

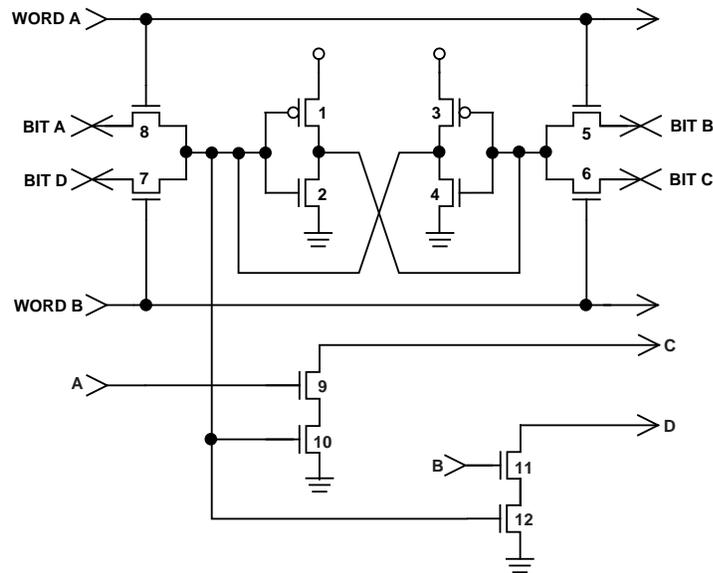
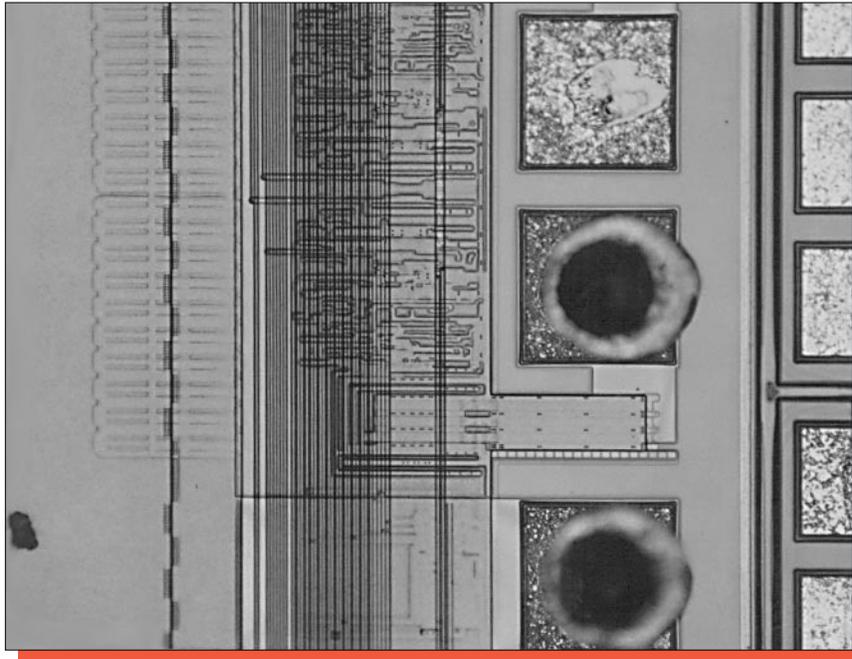
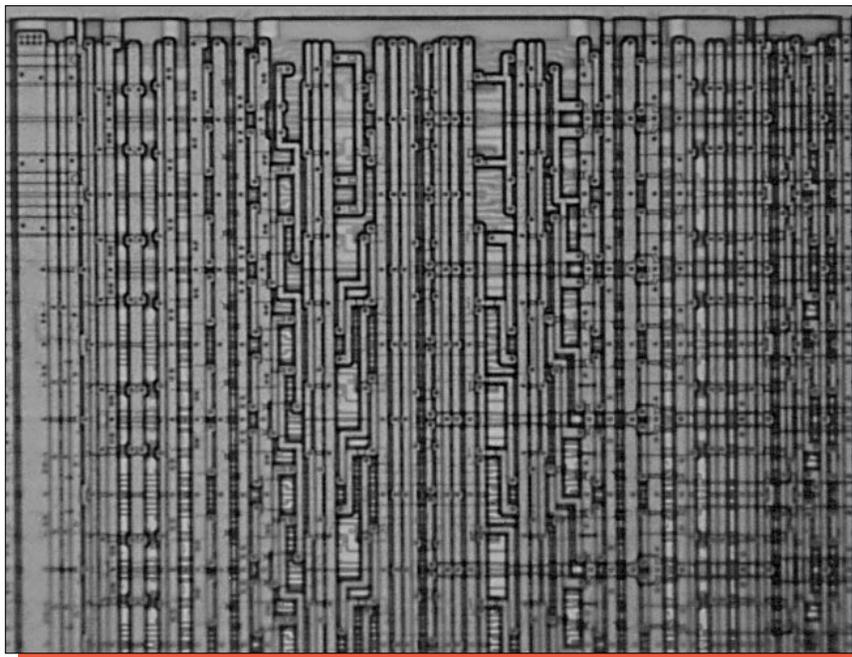


Figure 32. Topological views and schematic of the 12T SRAM cell. Mag. 3200x, 0°.



Mag. 200x



Mag. 500x

Figure 33. Optical views of the I/O structure and general circuitry.