

Construction Analysis

Ok! M5117805A-60J 16Mbit DRAM (EDO)

Report Number: SCA 9707-545



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INTRODUCTION

This report describes a construction analysis of the OKI M5117805A-60J 16Mbit DRAM. Two devices which were encapsulated in 28-pin small-outline packages with J-leads (SOJs) were received for the analysis. No date code was decipherable (1996?).

MAJOR FINDINGS

Questionable Items:¹

- Metal 2 aluminum thinned up to 95 percent² at most vias. The barrier metal remained intact to provide continuity.

Special Features:

- Bit line over capacitor stacked cell design.
- Textured poly capacitor plates.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- 28-pin small-outline plastic packages with J-leads (SOJs).
- LOCEB (lead-on-chip, edge bonded) leadframe design.
- A double backed adhesive tape connected the leadframe to the die surface. A polyimide die coat was present over the die surface.
- Lead-locking provisions (anchors) were present at all pins.
- Multiple bonding wires were used at pins 1, 14, 15 and 28 to provide additional current-carrying capacity to the power buses. All pins were connected.
- Dicing was by sawing (full depth).
- Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire.

Die Process and Design:

- The 16Mbit DRAM was organized as 2,097,152 words x 8 bits. The device features “fast page” mode of operation with EDO.
- Devices were fabricated using a selective oxidation CMOS process with N-wells in a P-substrate. It is believed a twin-well process was employed; however, the P-well could not be delineated. No epi was present.
- A patterned polyimide die coat was present to protect against packaging stresses.
- Final passivation consisted of a single layer of nitride.

TECHNOLOGY DESCRIPTION (continued)

- Two levels of metal were used. Both employed aluminum with titanium-nitride (TiN) caps and barriers. Metal 1 also employed a titanium adhesion layer. Both metal levels were defined using a dry-etch technique. Standard vias were used between metal 2 and metal 1. Tungsten plugs were used as the vertical interconnect under metal 1.
- Intermetal dielectric consisted of two layers of silicon-dioxide. The second layer of glass had been subjected to an etchback. No spin-on-glass (SOG) was employed.
- Pre-metal dielectric consisted of three layers of reflow glass and densified oxide. The glass was reflowed prior to contact cuts. One additional layer was present in the array.
- Four levels of dry-etched polysilicon were used. Poly 1 (poly and tungsten silicide) formed all gates on the die. Poly 2 and 3 were used exclusively in the cell array. Poly 2 was used to form the individual plates of all capacitors. This poly layer was textured to increase the capacitor surface area. Poly 3 formed the common plate of the capacitors. Poly 4 (poly and tungsten silicide) formed the bit lines in the array and was used throughout the die as an interconnect layer.
- N+ and P+ implanted source/drain diffusions formed N- and P-channel transistors. All gates used oxide sidewall spacers that were left in place.
- The memory cells used an NMOS DRAM cell design consisting of a select gate and a stacked capacitor. Poly 1 formed the word lines/select gates and was “piggybacked” by metal 1. Stacked capacitors were formed by poly 2 plates covered by a poly 3 sheet separated by a thin dielectric. The poly 2 plate was textured providing increased area (capacitance). Poly 4 formed the bit lines.
- Redundancy was implemented using poly 4 fuses. Laser blown fuses were noted on both samples inspected. Cutouts were present above fuse locations.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 4

Questionable Items:¹ None.

Special Features:

- LOCEB leadframe design.

General Items:

- 28-pin small-outline plastic packages with J-leads (SOJs). All pins were connected.
- Overall package quality: Normal. No defects were noted on the external portions of the package. No voids or cracks were noted in the plastic material.
- Leadframe: LOCEB leadframe design. No header/paddle was used. Pin condition was good, intact solder coating externally and silver spot plating internally.
- Lead-locking design: Good. Anchors were present at all pins.
- Wirebonding: Thermosonic ball bonds using 1.0 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were normal (see page 10). Bonding wire spacing was good, no excessive wire sweep. Multiple bonding wires were present at pins 1 and 14 (Vcc) and 15 and 28 (Vss) to provide additional current-carrying capacity to the power buses.
- Die dicing: Die separation was by sawing with normal quality workmanship. No large chips or cracks were noted.
- A patterned polyimide die coat was present over the surface of the die.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process:

Figures 4 - 45

Questionable Items:¹

- Metal 2 aluminum thinned up to 95 percent² at most vias. Barrier metal maintained continuity.

General Items:

- Fabrication process: Selective oxidation CMOS employing twin-wells in a P substrate (no epi).
- Process Implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage, process defects, or contamination was found.
- A patterned polyimide die coat was employed.
- Final Passivation: Single layer of nitride. Integrity tests indicated defect-free passivation. Edge seal was good.
- Metallization: Two levels of metallization were used. Metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and a titanium-nitride on titanium (Ti) barrier/adhesion layer. Standard vias were used as the interconnect between metal 1 and metal 2. Tungsten (W) plugs were used under metal 1.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

ANALYSIS RESULTS II (continued)

- Metal patterning: Both metal levels were defined by a dry etch of good quality. Metal 2 was widened around vias. All vias were completely surrounded by metal. Metal one design rules were fairly aggressive providing a 1.3 micron pitch with 0.45 micron wide metal lines in the array.
- Metal defects: No notches or voids were noted in either metal layer. Fairly large silicon nodules were found during cross sectioning. They occupied in excess of 90 percent of the metal line thickness (Figure 20).
- Metal step coverage: Metal 2 aluminum thinned up to 95 percent at most vias. The barrier aided in retaining the connections. Metal 1 thinned up to 50 percent at some contacts. The tungsten plugs were fairly level with the oxide surface, so no large steps were present for the metal to cover.
- Via and contact defects: Some minor over-etching of was noted under tungsten plugs, however; no problems are foreseen.
- Intermetal dielectric: This dielectric consisted of two layers of silicon-dioxide. The second layer had been subjected to an etchback for planarization. No spin-on-glass was employed between these layers.
- Pre-metal dielectric: The dielectric between metal 1 and poly 4 consisted of a BPSG reflow glass and was reflowed prior to contact cuts. An additional layer of this material was present between poly 4 and poly 3, and yet another between poly 2 and poly 1. No problems were found.
- Polysilicon: Four levels of dry-etched polysilicon were used. Poly 1 (poly and tungsten silicide) formed all gates on the die. Poly 2 and 3 were used exclusively in the cell array. Poly 2 was used to form the individual plates of all capacitors. This poly layer was textured to increase the capacitor surface area. Poly 3 formed the common plate of the capacitors. Poly 4 (poly and tungsten silicide) formed the bit lines in the array and was used throughout the die as an interconnect layer.

ANALYSIS RESULTS II (continued)

- Isolation: Local oxide (LOCOS). No problems were present, and no step was found at the well boundaries.
- Diffusions: Implanted N+ and P+ diffusions formed the sources and drains. The process employed oxide sidewall spacers that were left intact. No problems were found.
- Wells: N-wells were employed in a P substrate. It is believed that the P-well could not be delineated in the P substrate.
- Epi: No epi layer was employed.
- Redundancy: Redundancy was implemented by laser blowing poly 4 fuses. Passivation and intermetal dielectric cutouts were present above fuse locations.
- Buried contacts: Direct poly 4-to-N+ diffusion (buried) contacts were present throughout the die. In addition, poly 2 made direct contact to N+ in the cell array.
- Memory cells: Bit line over capacitor DRAM cell design consisting of a select transistor with a stacked capacitor as the storage element. Poly 1 was “piggybacked” by metal 1 to form the word lines/select gates. Poly 2 (textured) and the poly 3 sheet formed the plates of the storage capacitor. Poly 3 also distributed memory enable throughout the cell array. Poly 4 formed the bit lines. Cell size was 1.25 x 2.6 microns (3.25 microns²). This is considered quite large for a 1996 era design.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Delayer to metal 1

SEM inspection of metal 1

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal/Poor

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.0 mil gold wire.
Die attach method	Double backed adhesive tape.
Dicing method	Sawn
Die surface integrity:	
Toolmarks (absence)	N
Particles (absence)	N
Contamination (absence)	N
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity ²	NP
Metal registration	N
Contact coverage	N
Contact registration	N

²95 percent metal 2 aluminum thinning, and fairly large silicon nodules in both metals.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

OKI JAPAN
M5117805A-60J
63022029A9Z

WIREBOND STRENGTH

<u>Sample</u>	1
Wire material:	1.0 mil diameter gold (Au)
Material at package lands:	silver (Ag)
# of wires tested:	14
Bond lifts:	0
Force to break - high:	10g
- low:	7.5g
- avg.:	8.4g
- std. dev.:	1.5

DIE MATERIAL ANALYSIS

Final passivation:	Nitride.
Metallization 2:	Aluminum with a titanium-nitride cap and barrier.
Intermetal dielectric:	Two layers of silicon-dioxide.
Metallization 1:	Aluminum with a titanium-nitride cap and titanium-nitride/titanium barrier/adhesion layer.
Plugs:	Tungsten.
Pre-metal glass:	BPSG.
Silicide on poly 4:	Tungsten.
Silicide on poly 1:	Tungsten.

VERTICAL DIMENSIONS

Die thickness: 0.35 mm (13.8 mils)

Layers

Passivation:	0.7 micron
Metal 2 - cap:	0.12 micron
- aluminum:	0.65 micron
- barrier:	0.12 micron
Interlevel dielectric - glass 2:	0.5 micron (average)
- glass 1:	0.4 micron
Metal 1 - cap:	0.12 micron
- aluminum:	0.5 micron
- barrier/adhesion layer:	0.1 micron
Contact plugs:	0.5 - 1.3 micron
Pre-metal dielectric:	0.4 micron (average)
Poly 4 - silicide:	0.1 micron
- poly:	0.1 micron
Poly 3:	0.1 micron
Poly 2:	0.05 micron (approx.)
Poly 1 - silicide:	0.1 micron
- poly:	0.1 micron
Interpoly dielectric -	
- poly 4 - poly 3:	0.5 micron (average)
- poly 2 - poly 1:	0.3 micron
LOCOS:	0.4 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.3 micron
N-well:	3.3 microns (approx.)

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COLOR DRAWING OF DIE STRUCTURE	Figure 32
DRAM MEMORY CELL STRUCTURES	Figures 33 - 43
CIRCUIT LAYOUT AND I/O	Figures 44 - 45

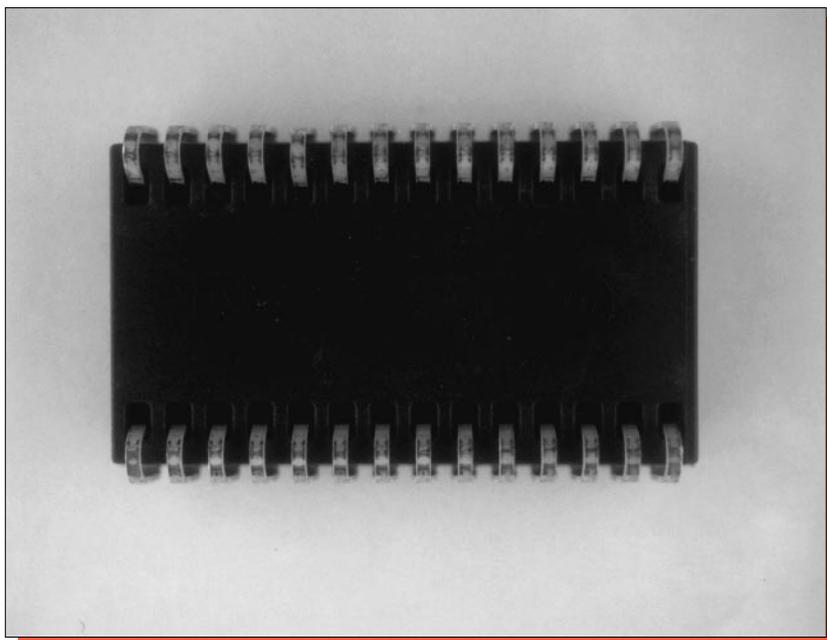
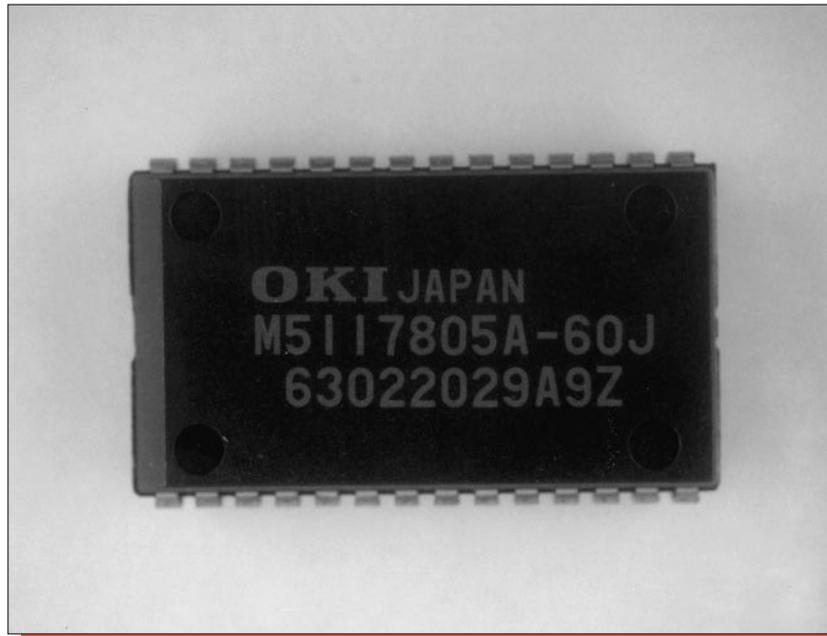


Figure 1. Package photographs of the OKI M5117805A-60J. Mag. 4.2x.

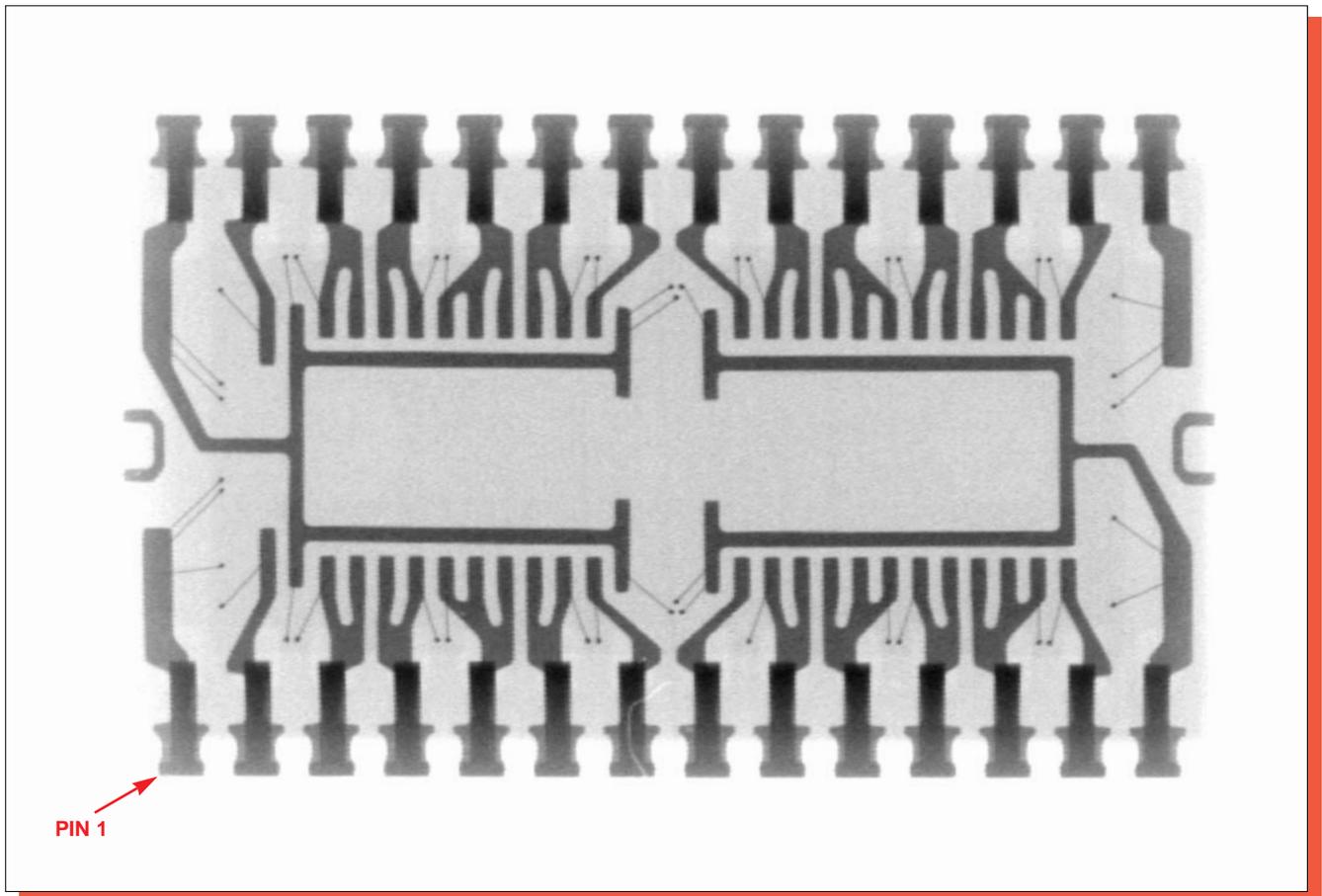
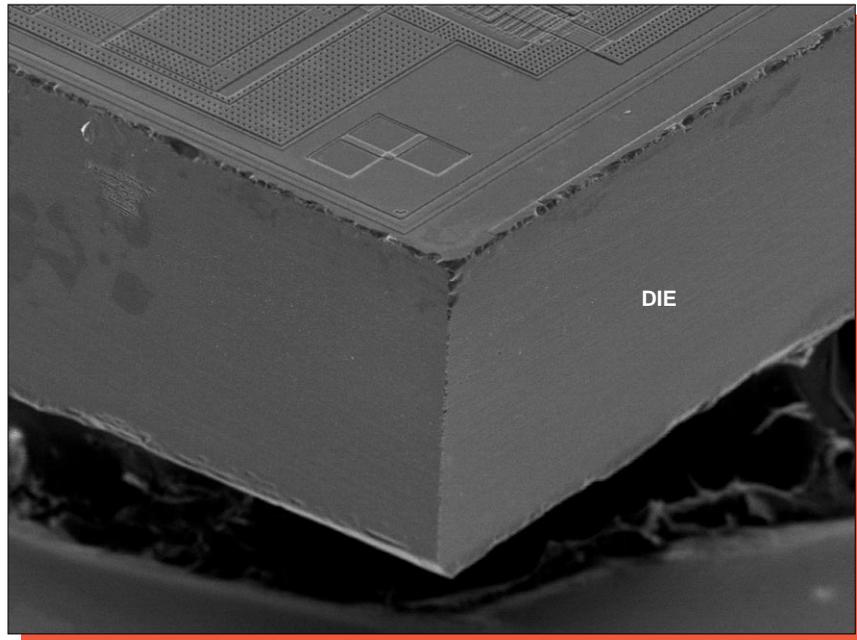
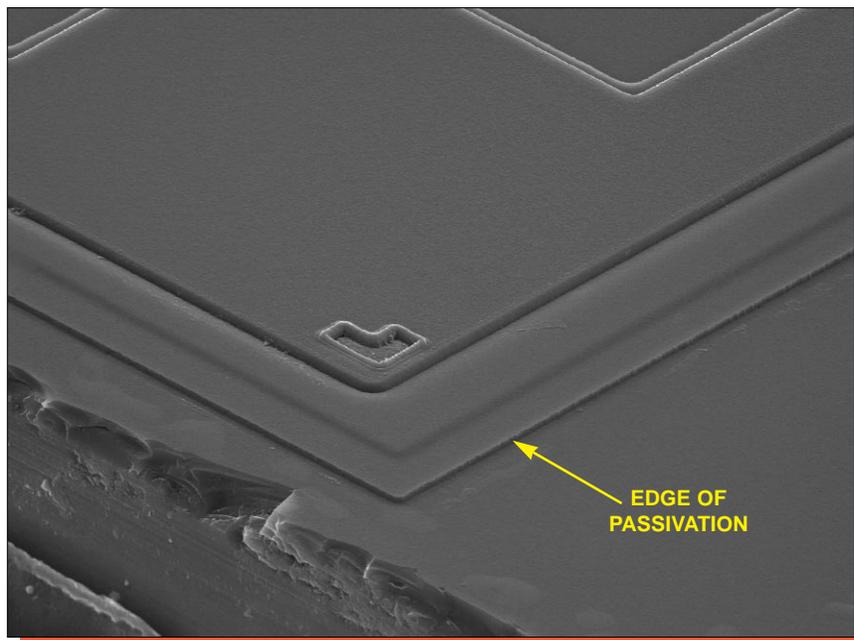


Figure 2. X-ray view of the package. Mag. 8x.

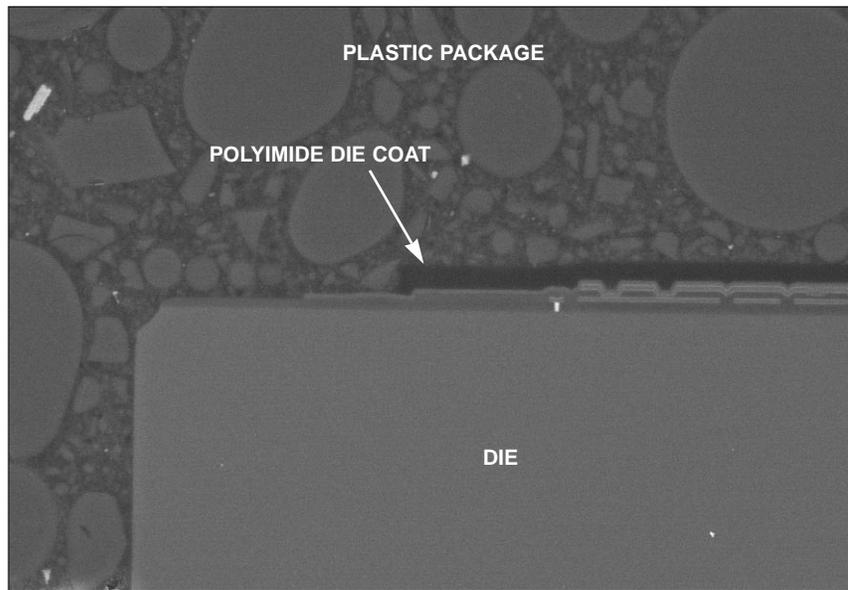


Mag. 140x

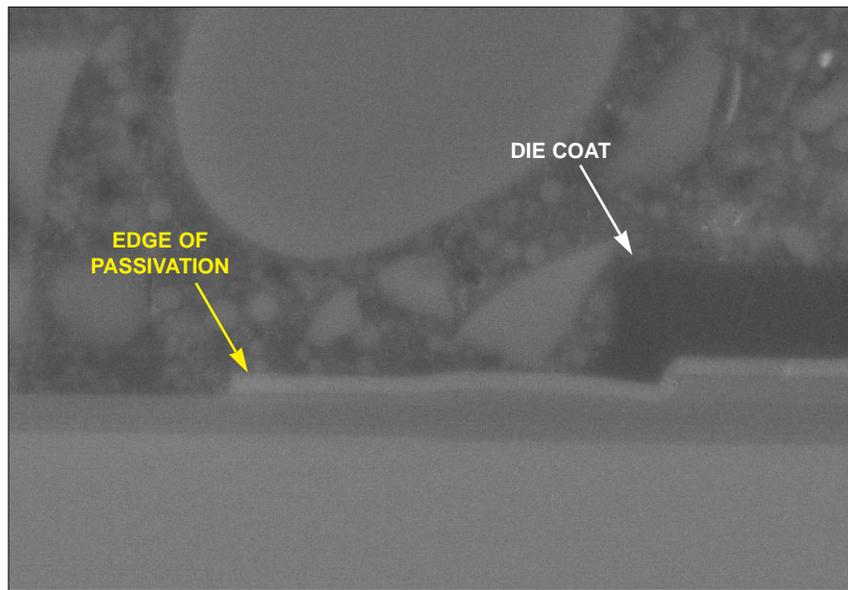


Mag. 960x

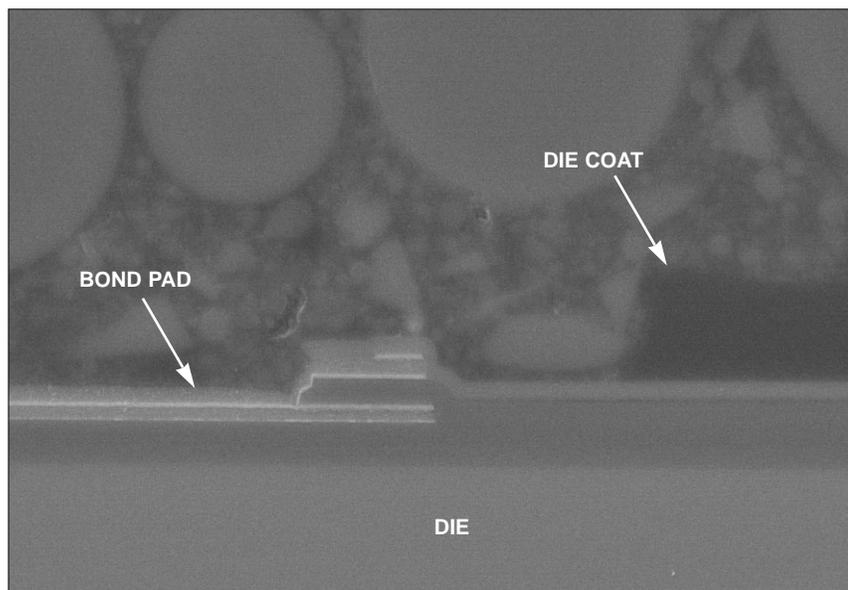
Figure 3. SEM views illustrating dicing and edge seal. 60°.



Mag. 800x



Mag. 3200x



Mag. 3200x

Figure 4. SEM section views illustrating the edge seal and polyimide die coat.

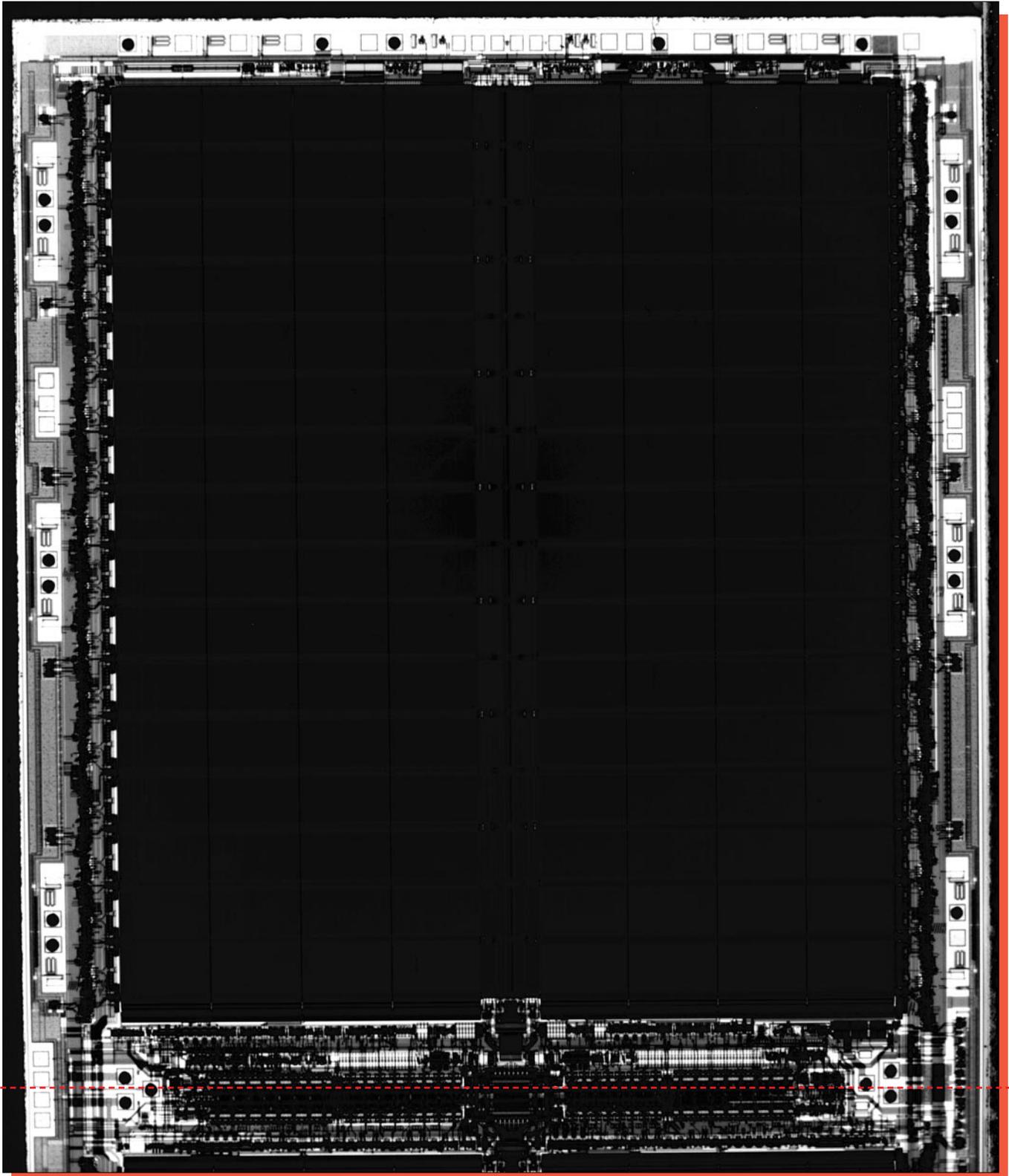


Figure 5. Portion of the OKI M5117805A-60J whole die photograph.
Mag. 26x.

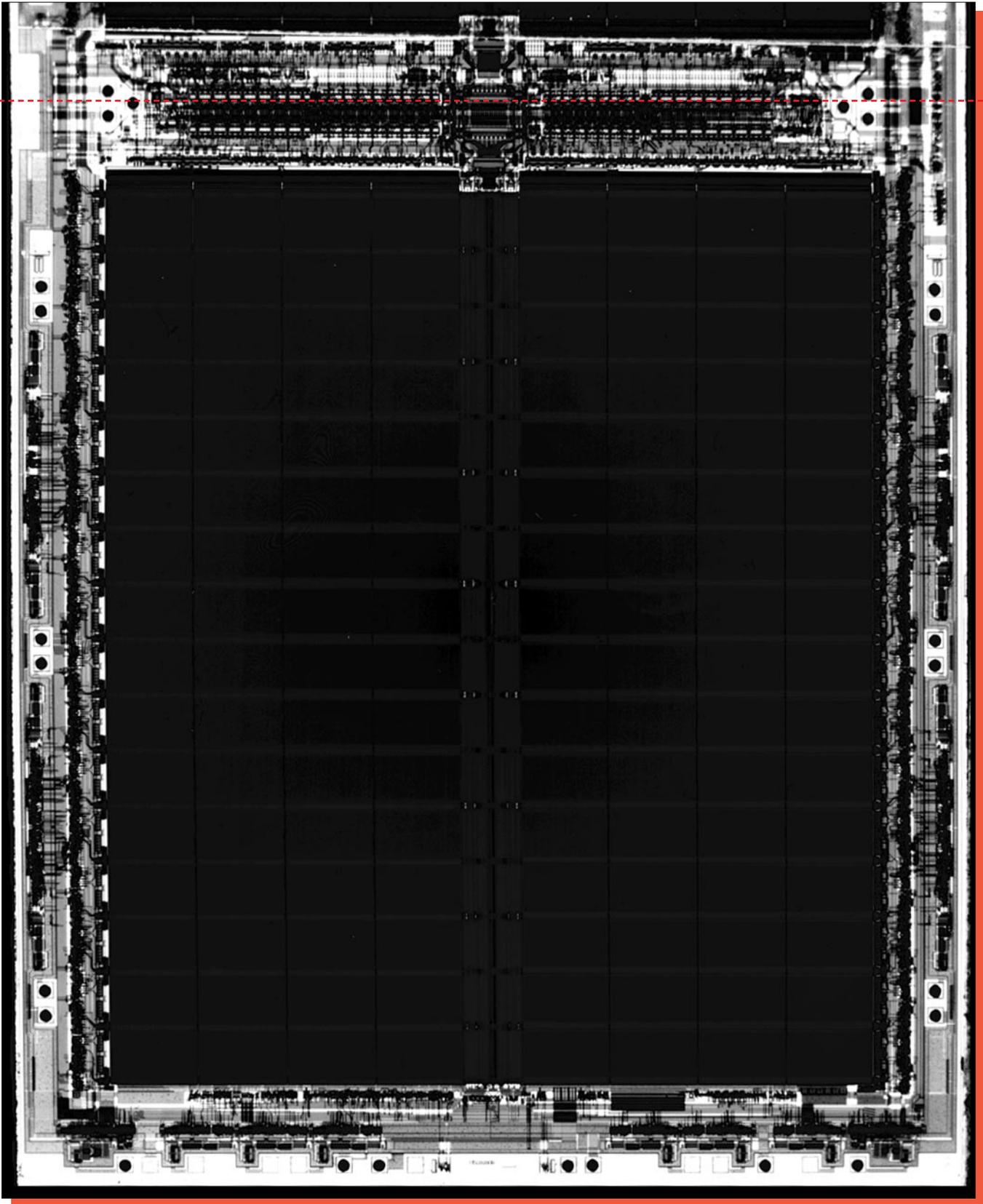


Figure 6. Remaining portion of the OKI M5117805A-60J whole die photograph.
Mag. 26x.

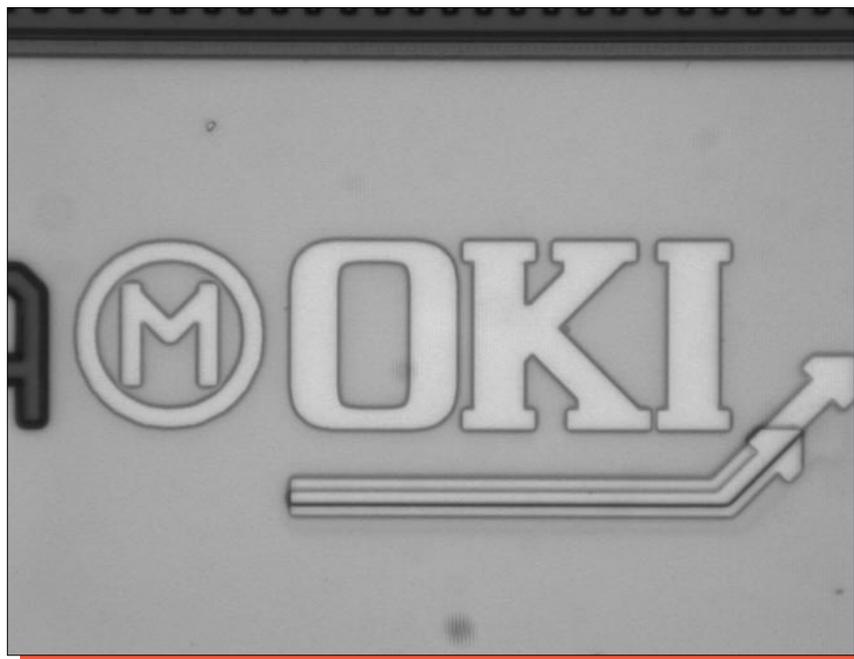
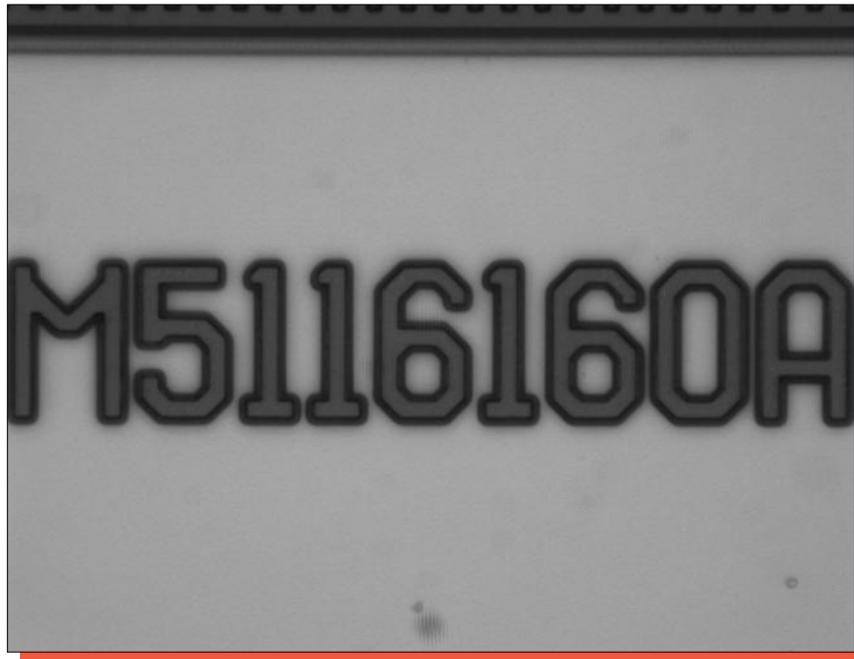


Figure 7. Optical views of die markings. Mag. 600x.

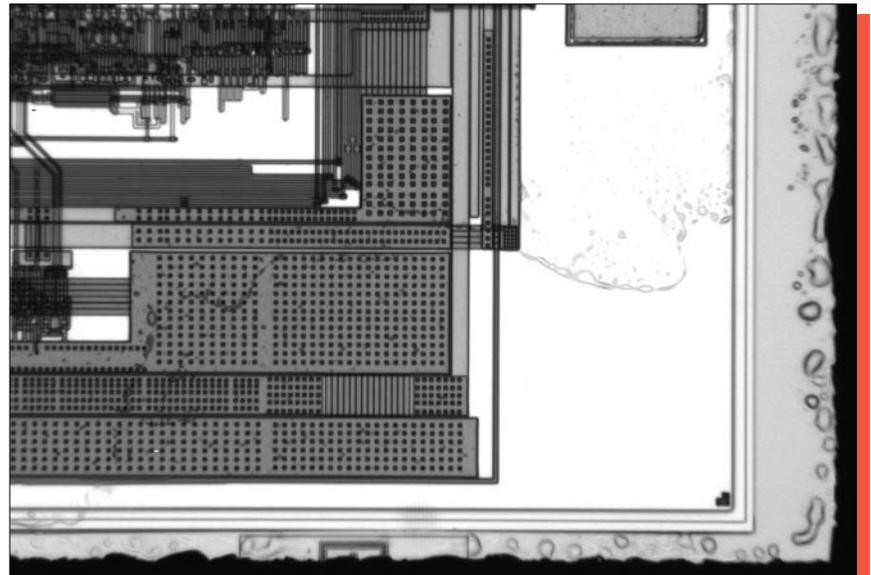
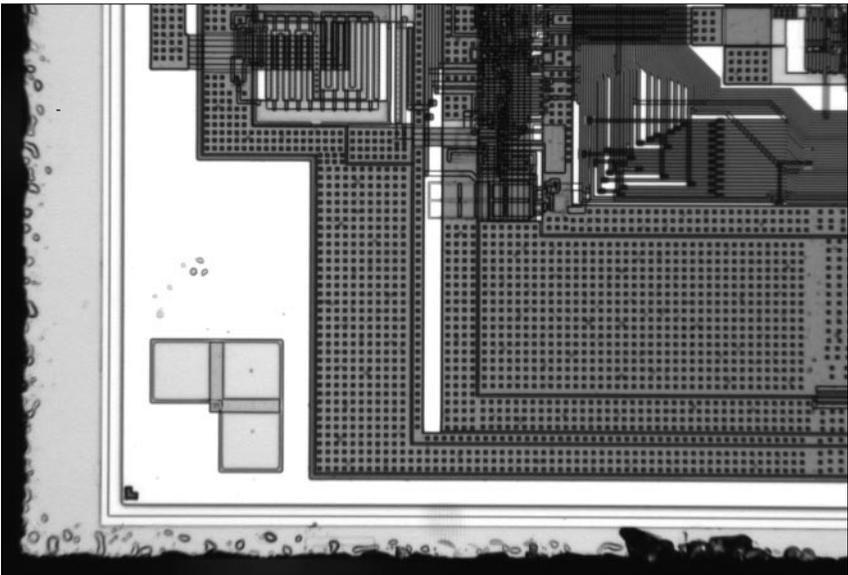
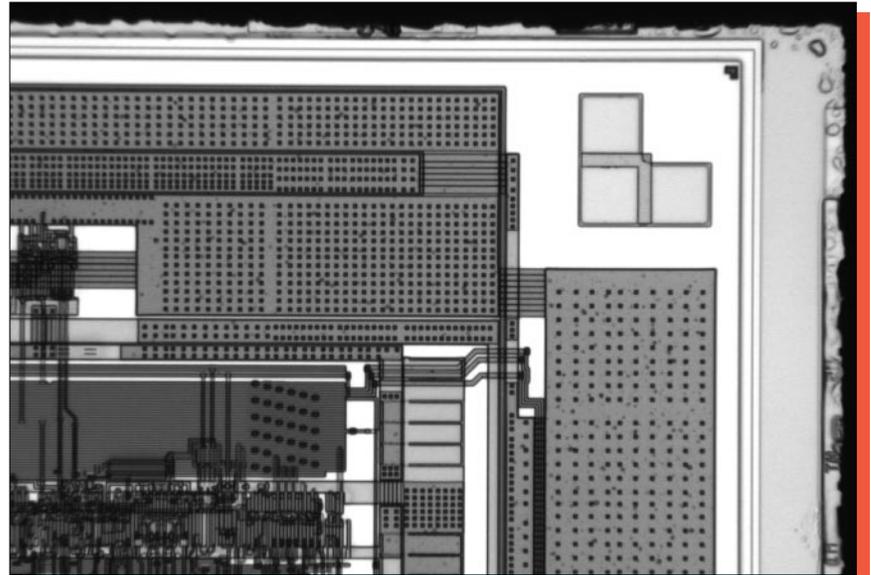
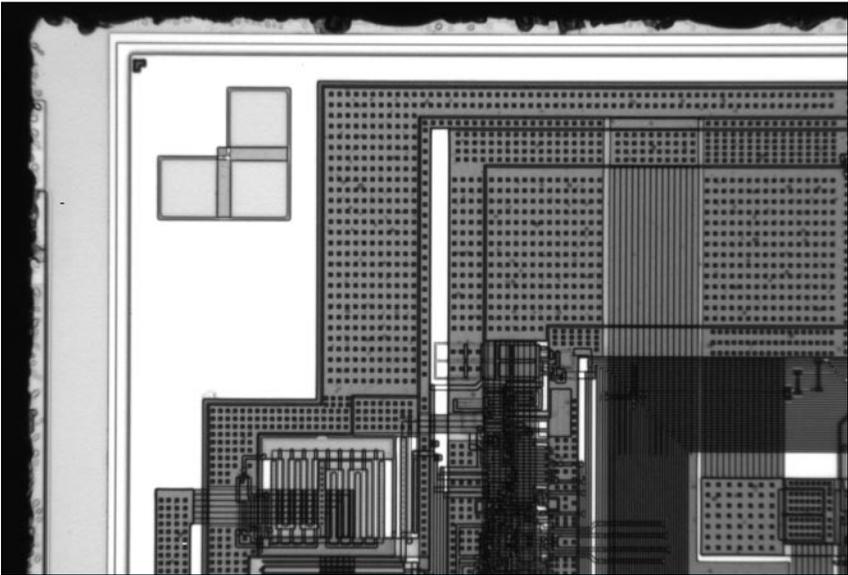
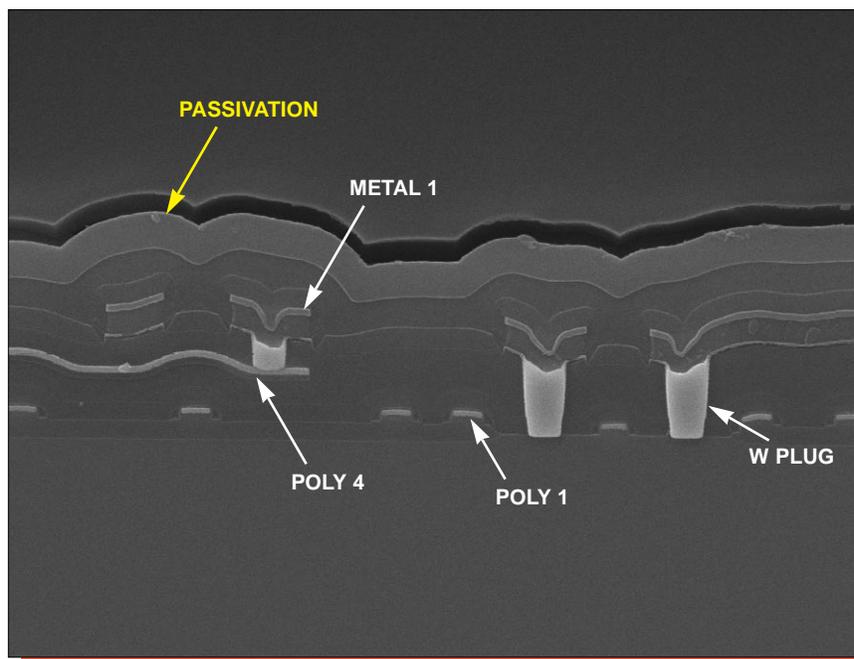
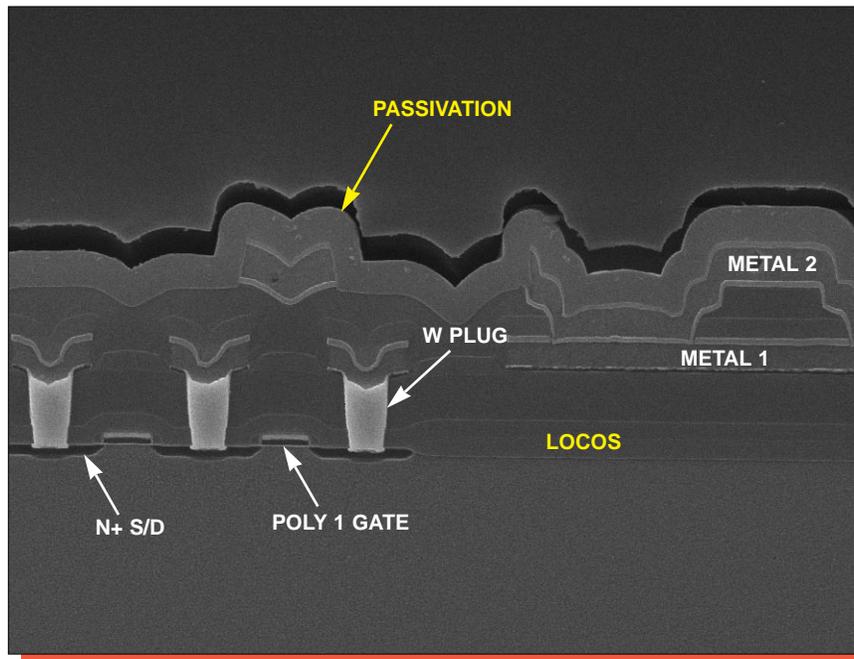
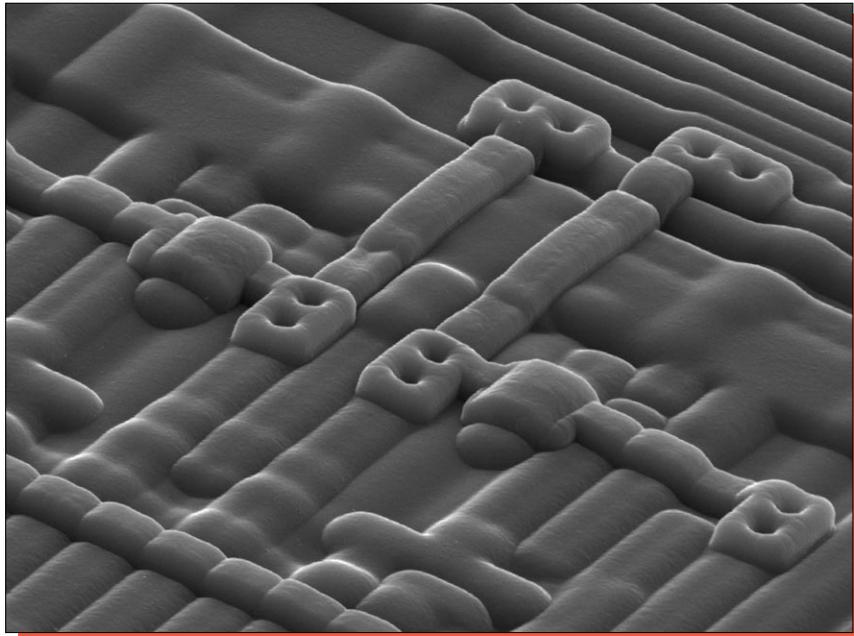


Figure 8. Optical views of die corners. Mag. 150x.

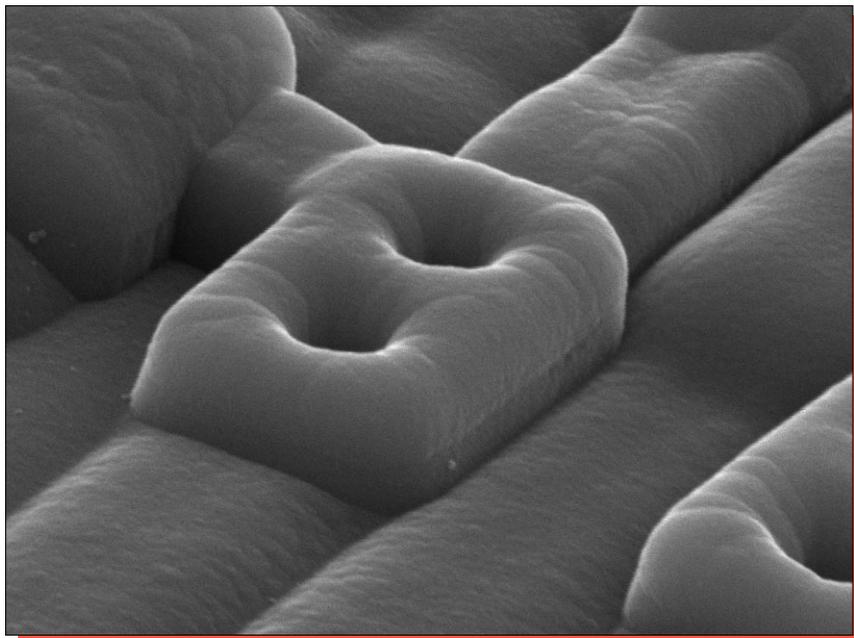


glass etch

Figure 9. SEM section views illustrating general structure. Mag. 6500x.

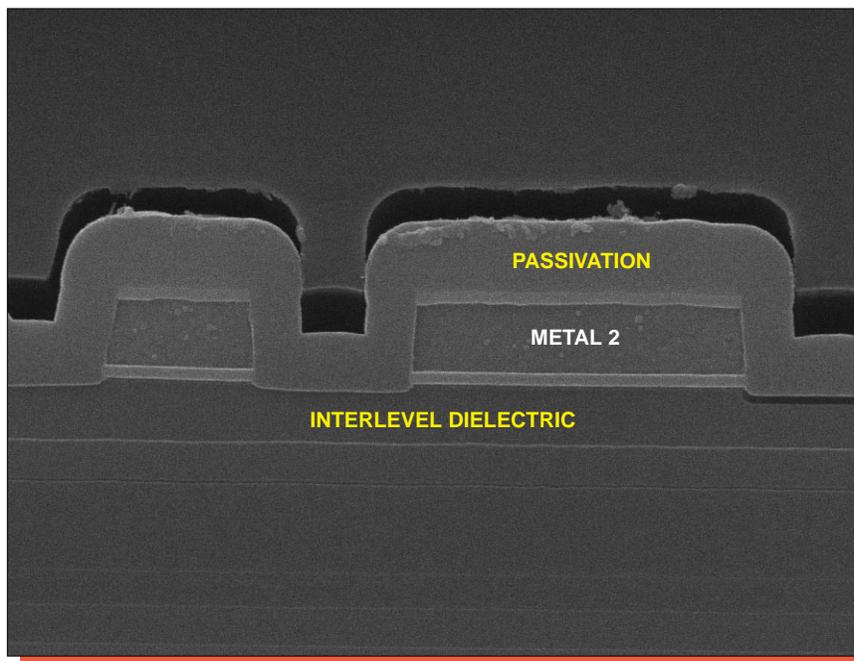


Mag. 3000x

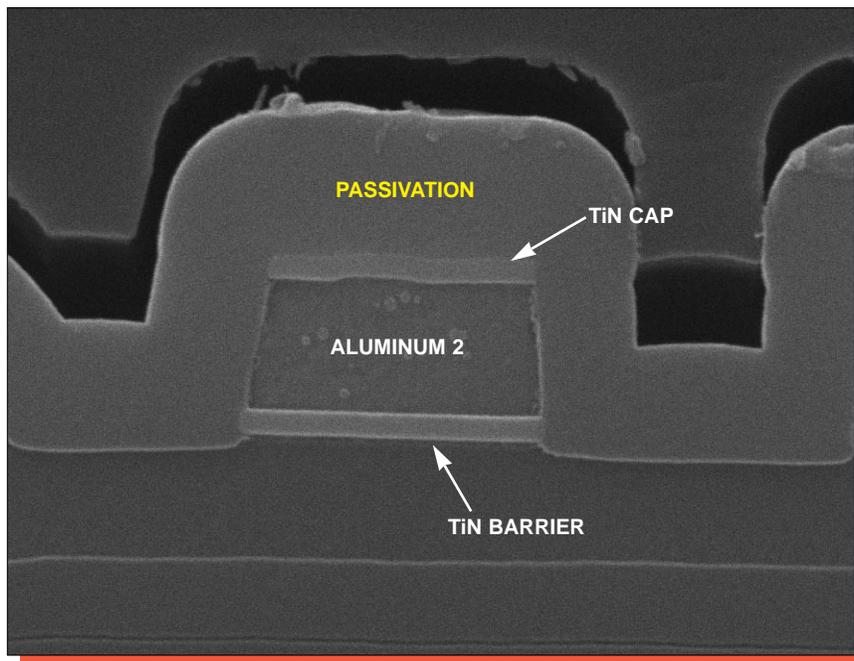


Mag. 12,000x

Figure 10. SEM views illustrating final passivation. 60°.



Mag. 13,000x



Mag. 26,000x

Figure 11. SEM section views of metal 2 line profiles.

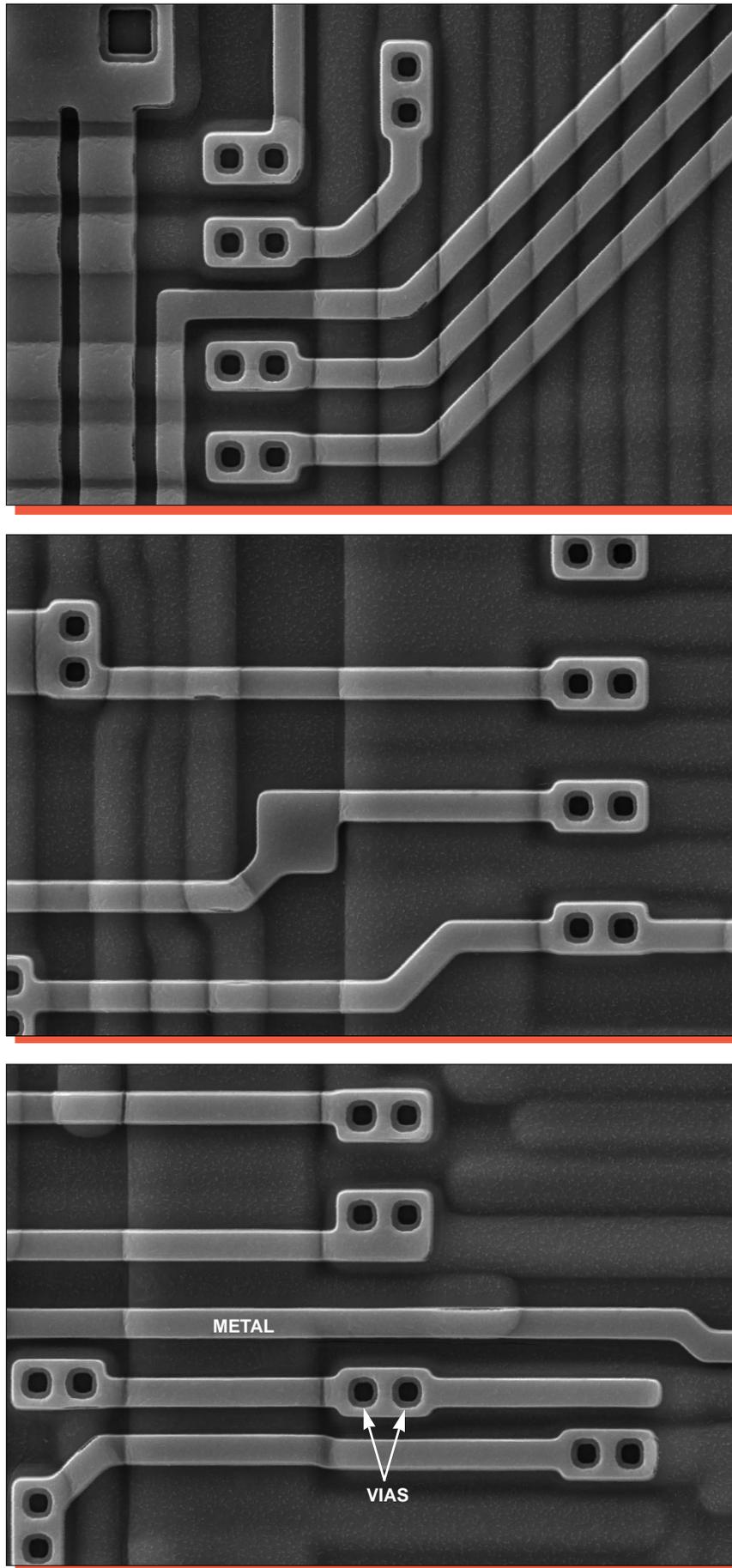
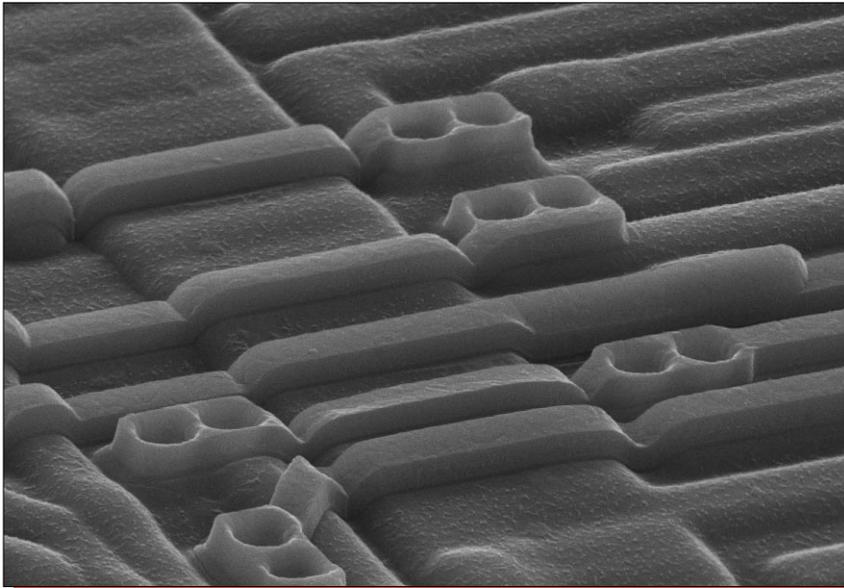
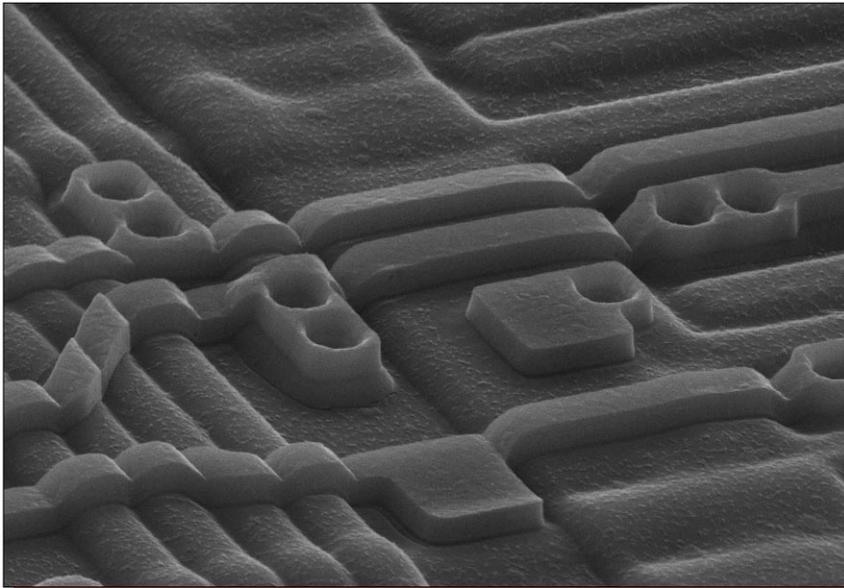


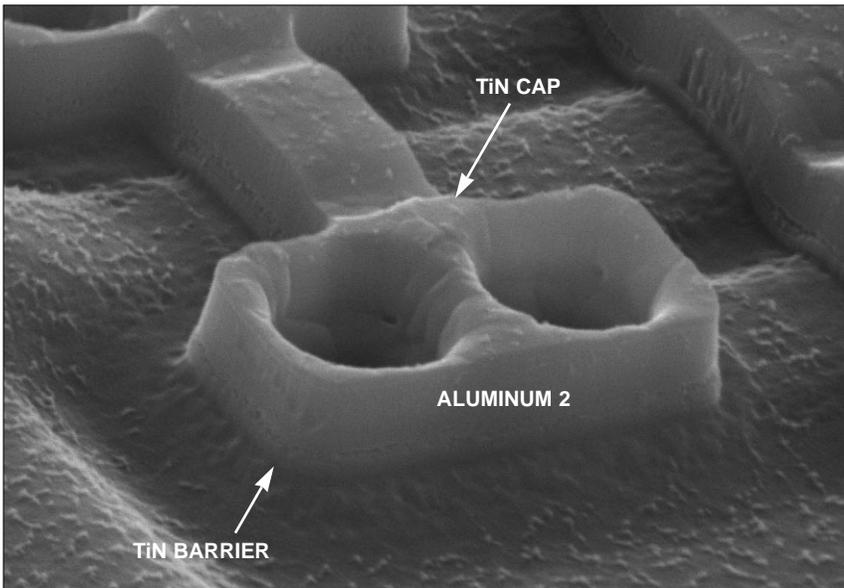
Figure 12. Topological SEM views of metal 2 patterning. Mag. 3000x, 0°.



Mag. 4000x

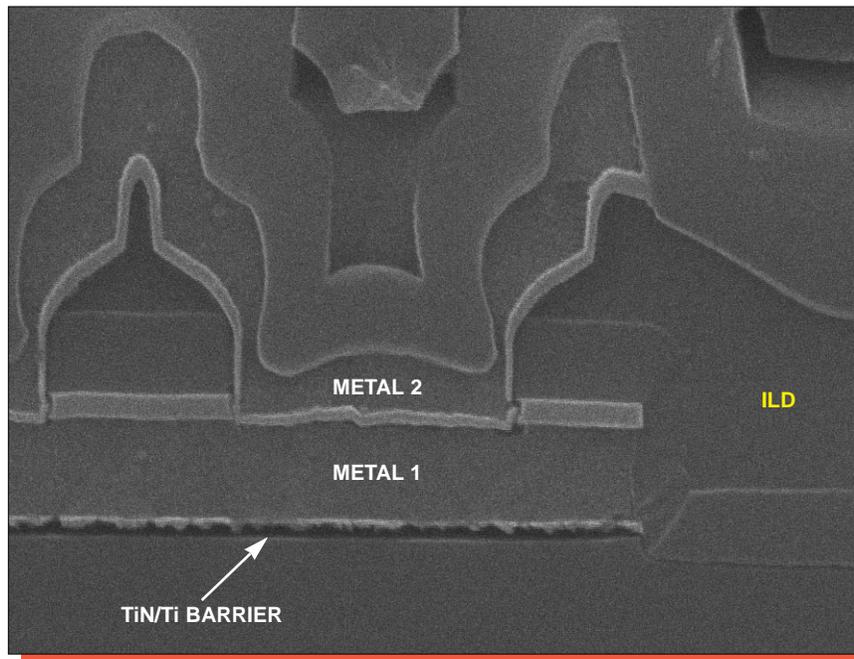


Mag. 4000x

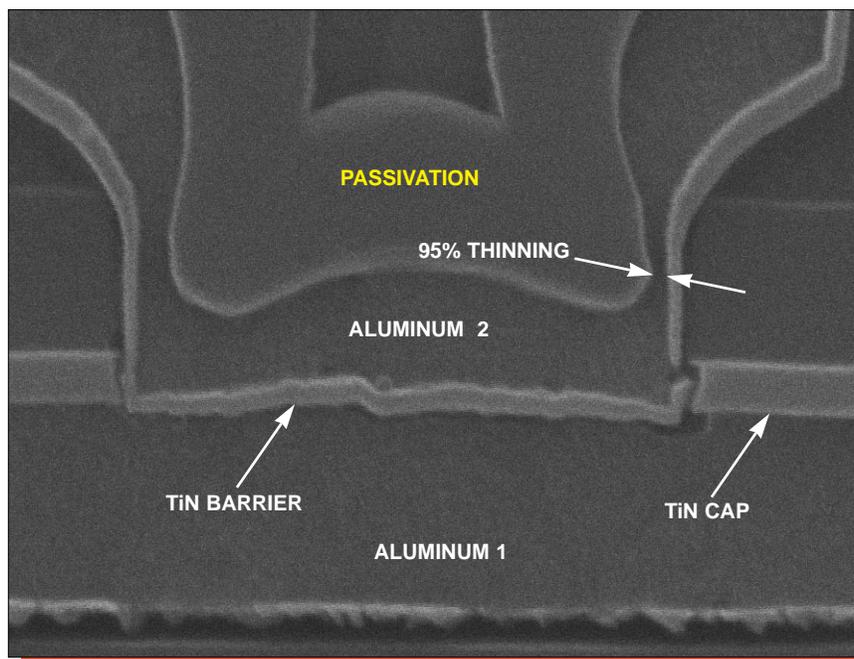


Mag. 13,500x

Figure 13. Perspective SEM views of metal 2 step coverage. 60°.

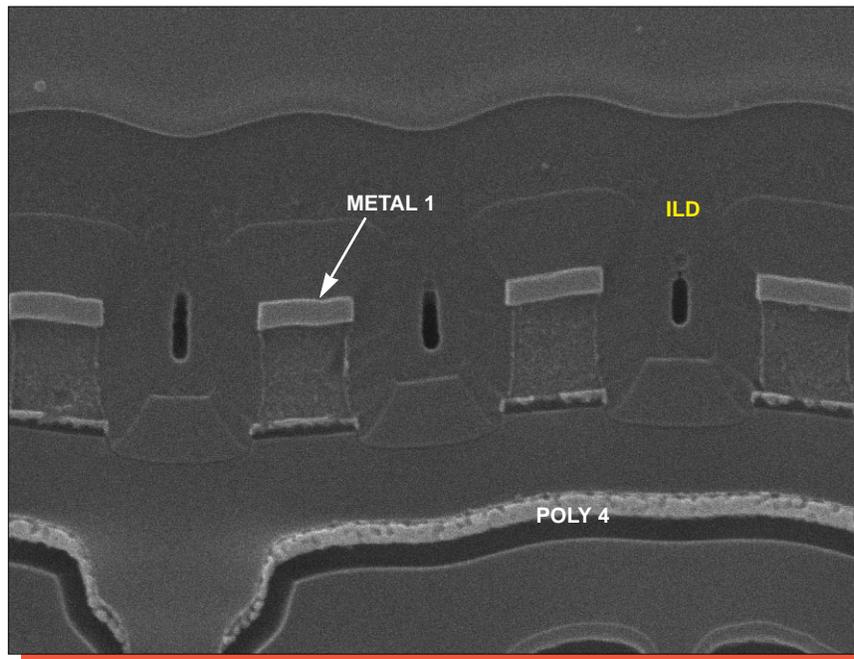


Mag. 26,000x

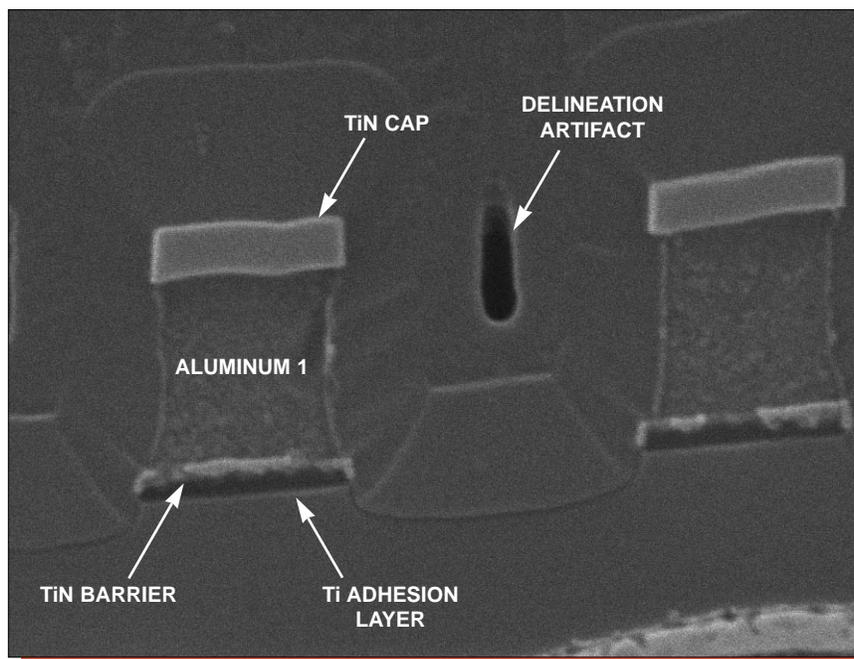


Mag. 52,000x

Figure 14 . SEM section views illustrating a via and interlevel dielectric composition.

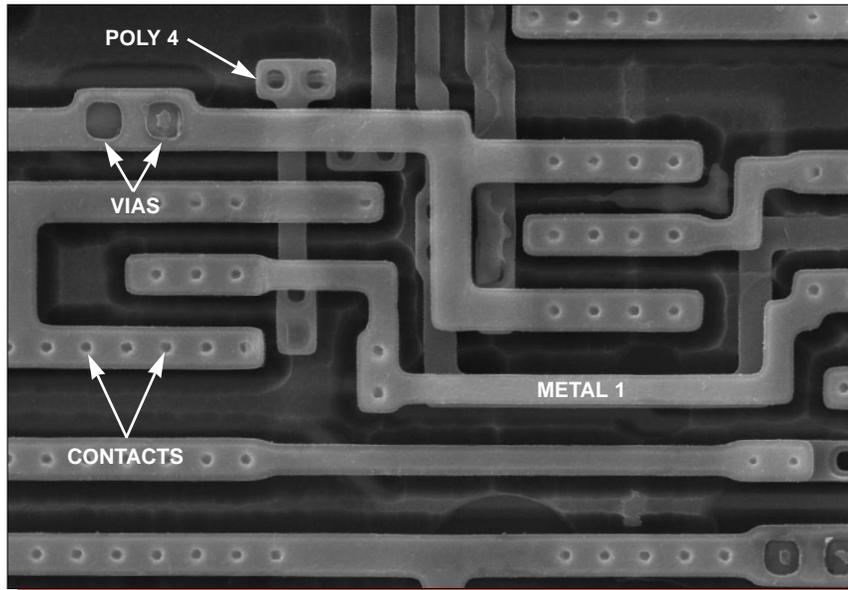


Mag. 26,000x

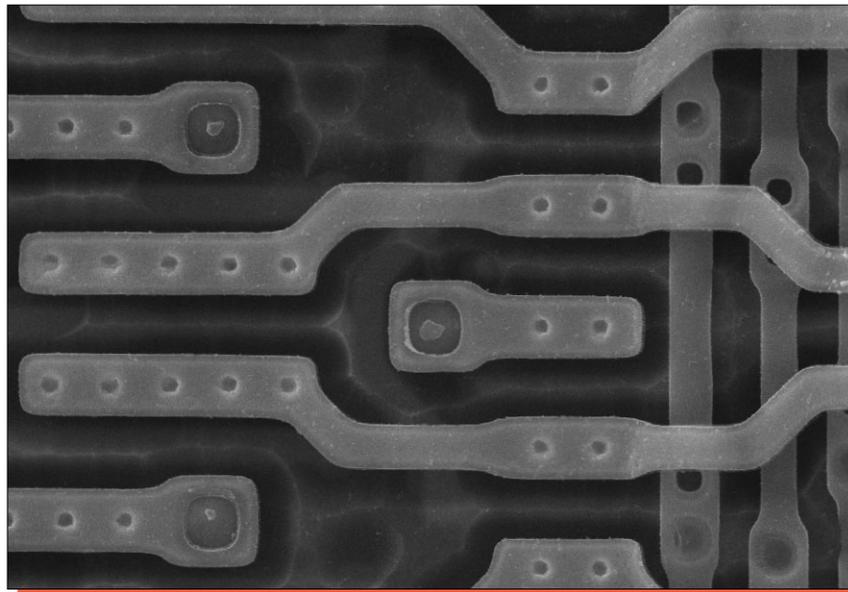


Mag. 52,000x

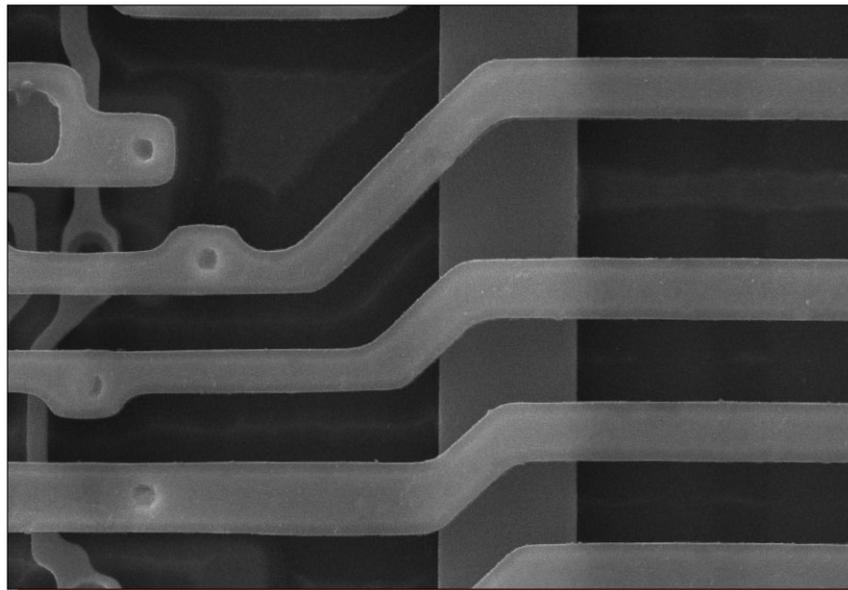
Figure 15. SEM section views of metal 1 line profiles.



Mag. 3200x

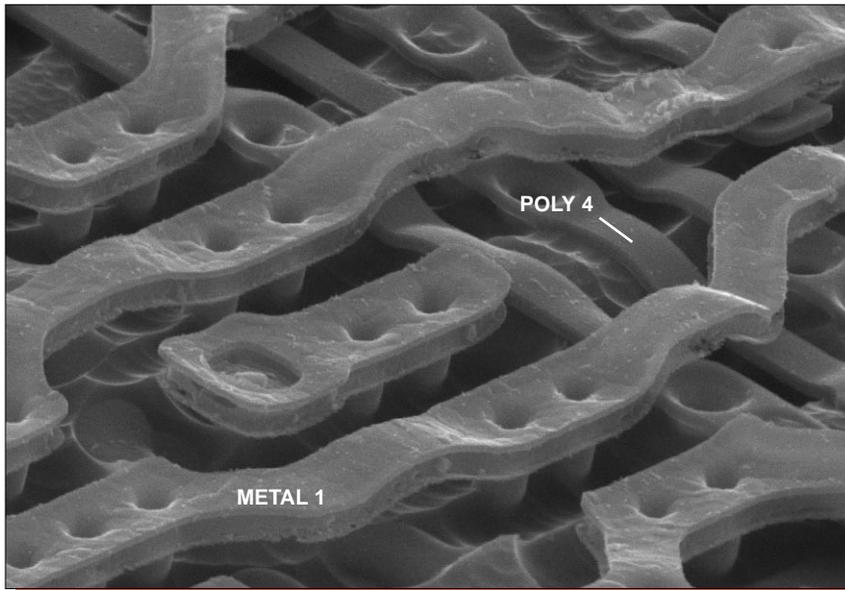


Mag. 5000x

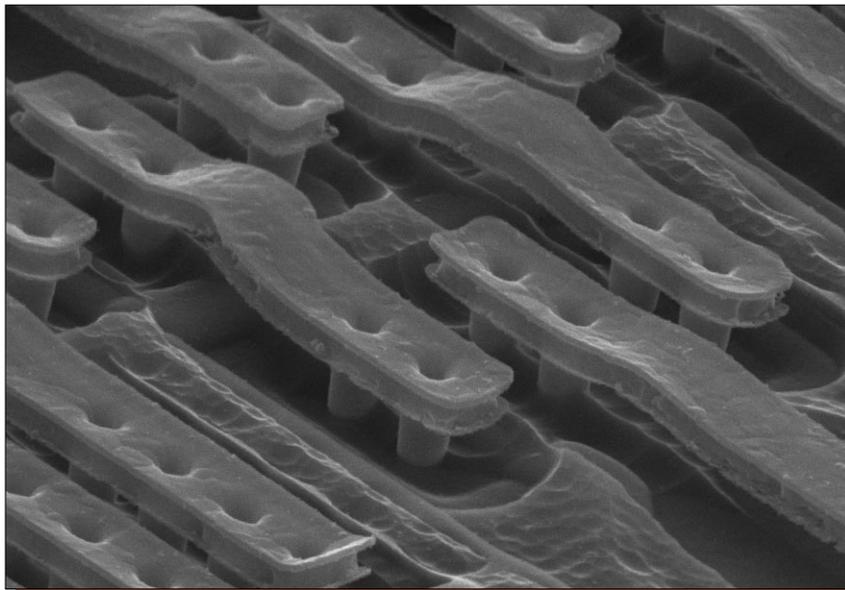


Mag. 6500x

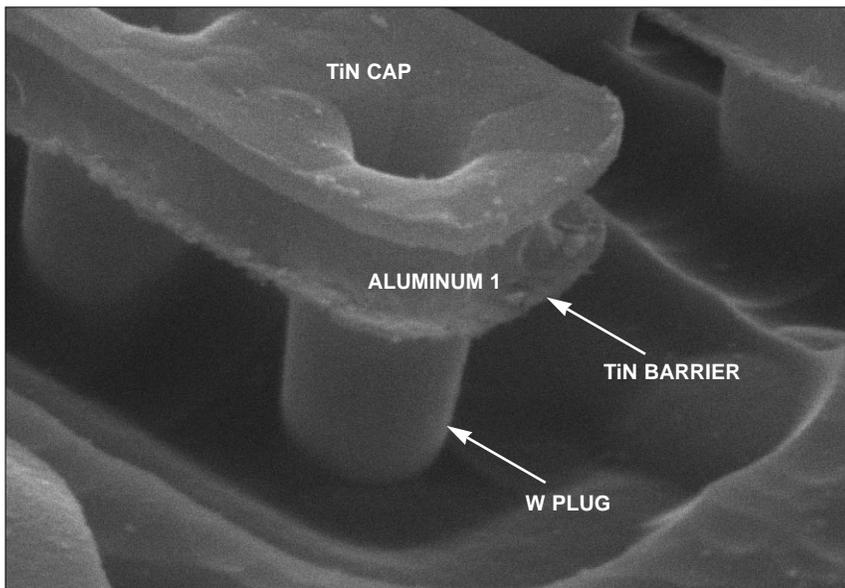
Figure 16. Topological SEM views of metal 1 patterning. 0°.



Mag. 8000x



Mag. 8000x



Mag. 30,000x

Figure 17. Perspective SEM views of metal 1 step coverage. 60°.

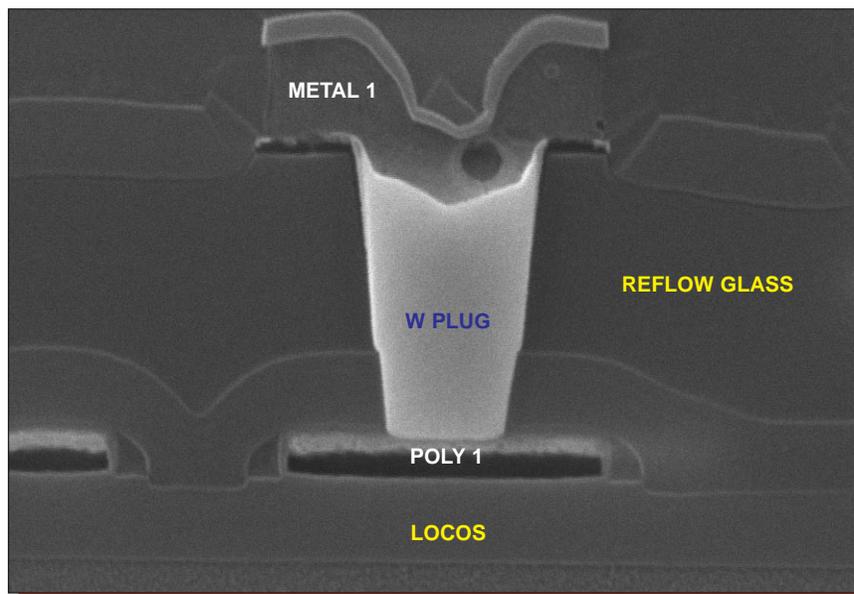
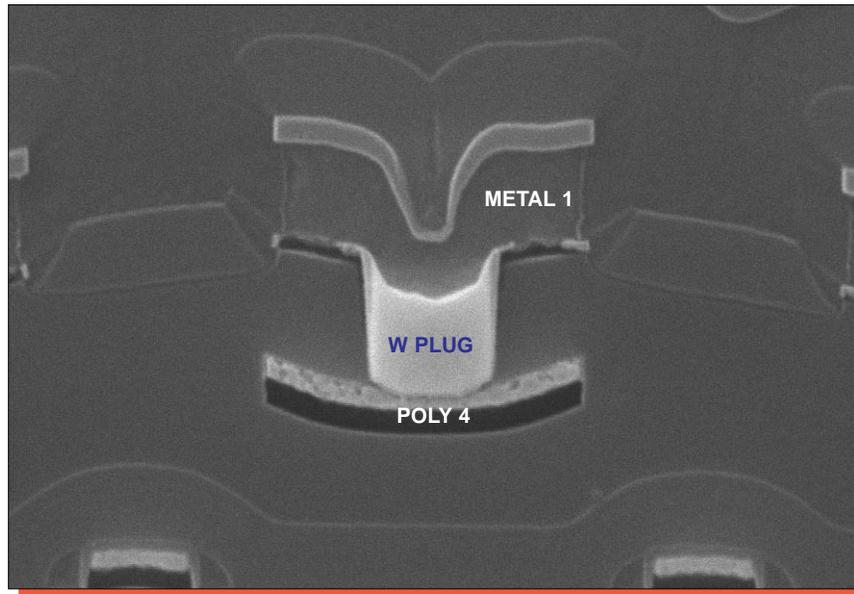
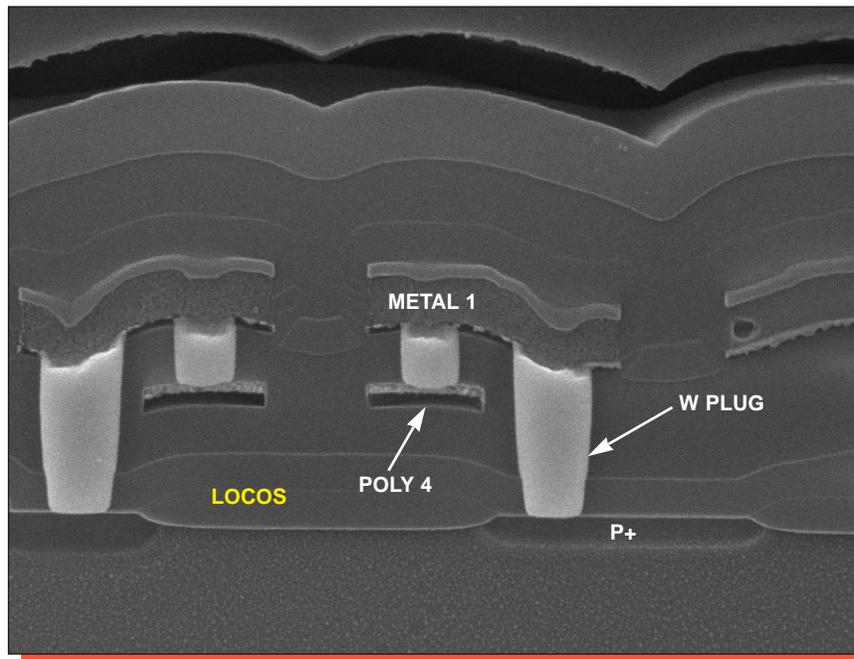
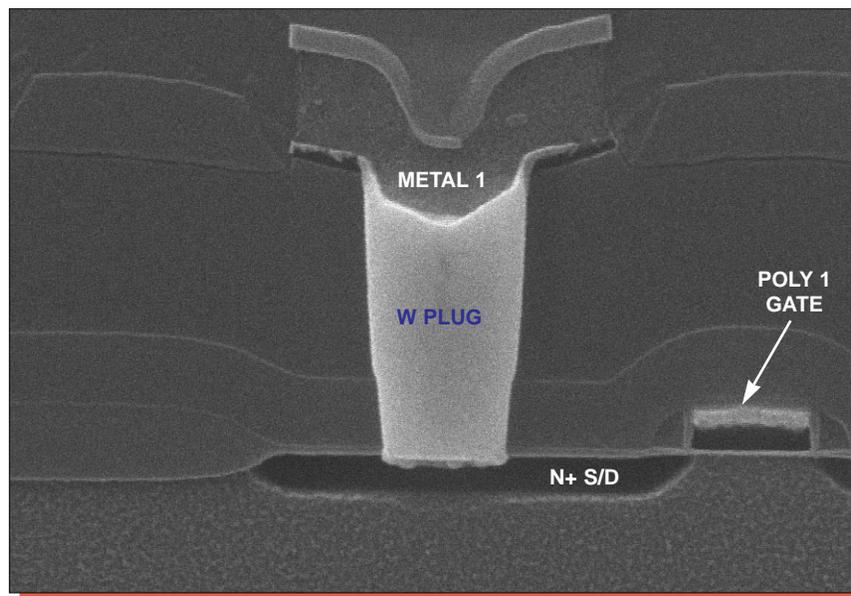


Figure 18. SEM section views illustrating typical metal 1 contacts. Mag. 26,000x.



Mag. 13,000x



Mag. 26,000x

Figure 19. Additional SEM section views of typical metal 1 contacts.

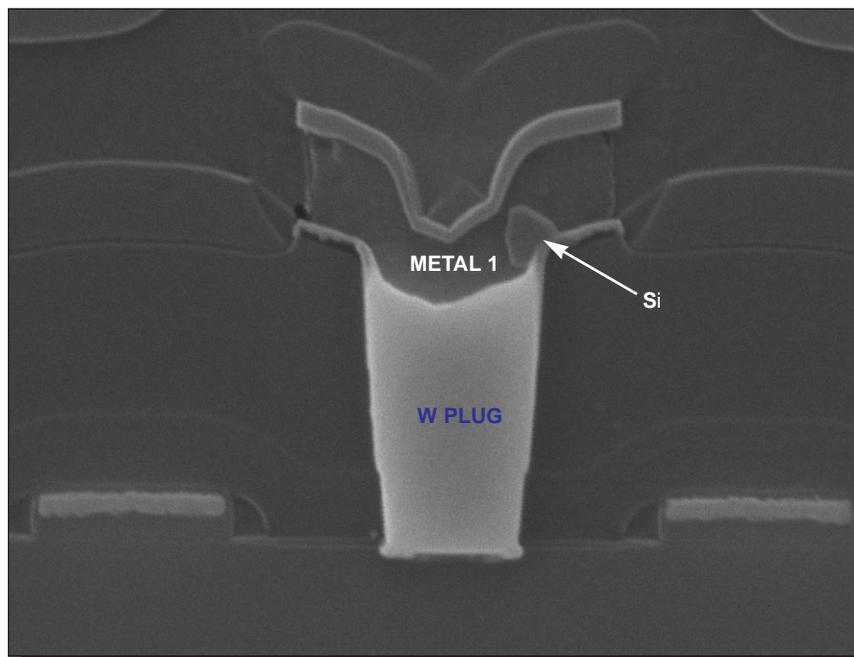
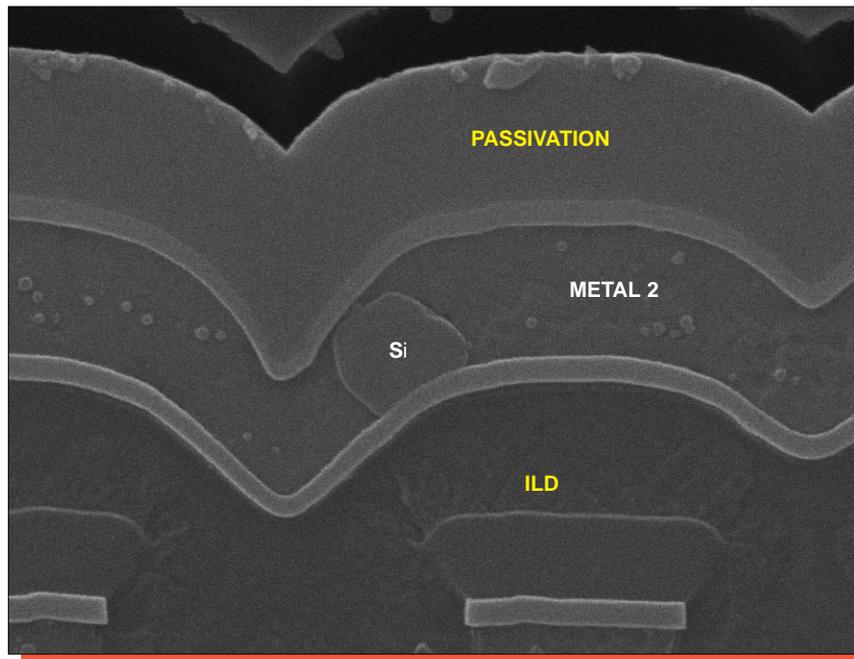


Figure 20. SEM section views illustrating silicon nodules in the aluminum. Glass etch, Mag. 26,000x.

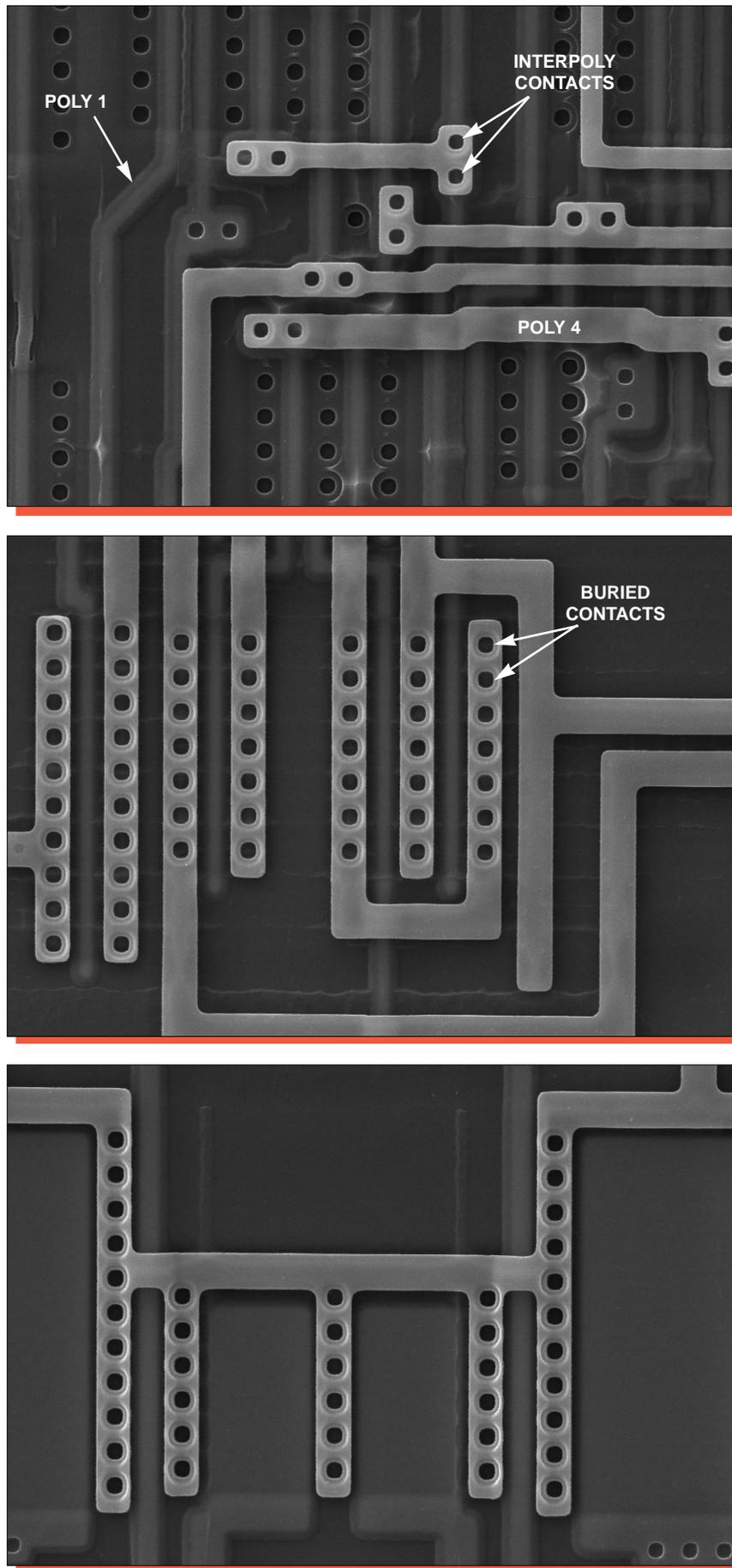
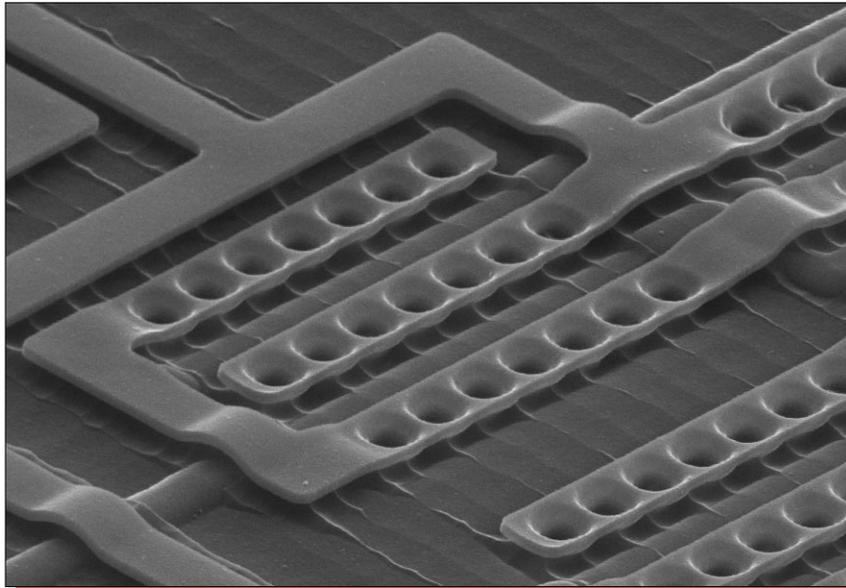
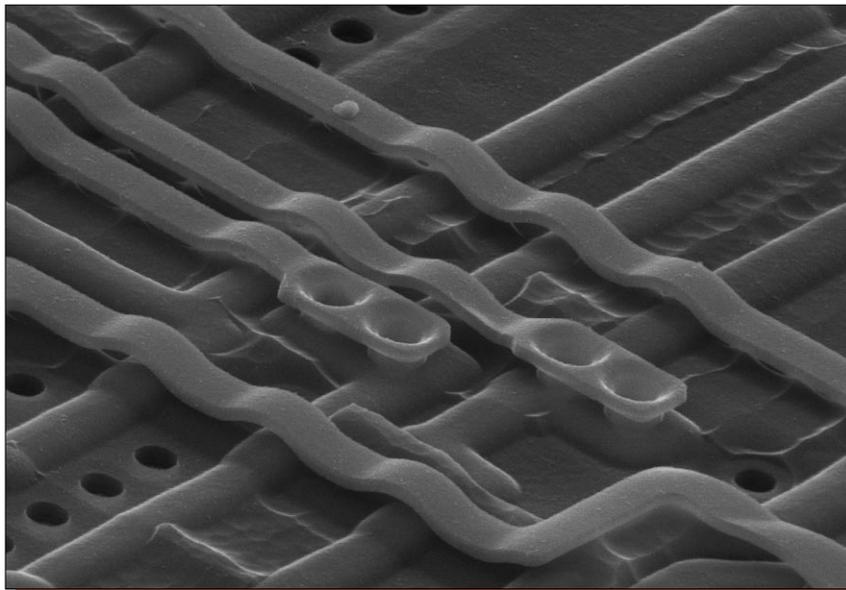


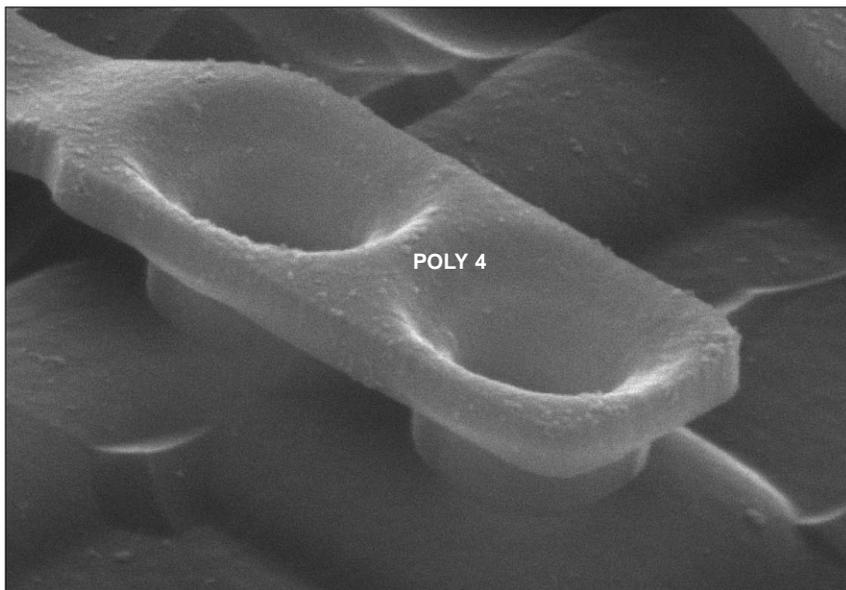
Figure 21. Topological SEM views of poly 4 patterning. Mag. 3200x, 0°.



Mag. 6000x



Mag. 7000x



Mag. 28,000x

Figure 22. Perspective SEM views of poly 4 coverage. 60°.

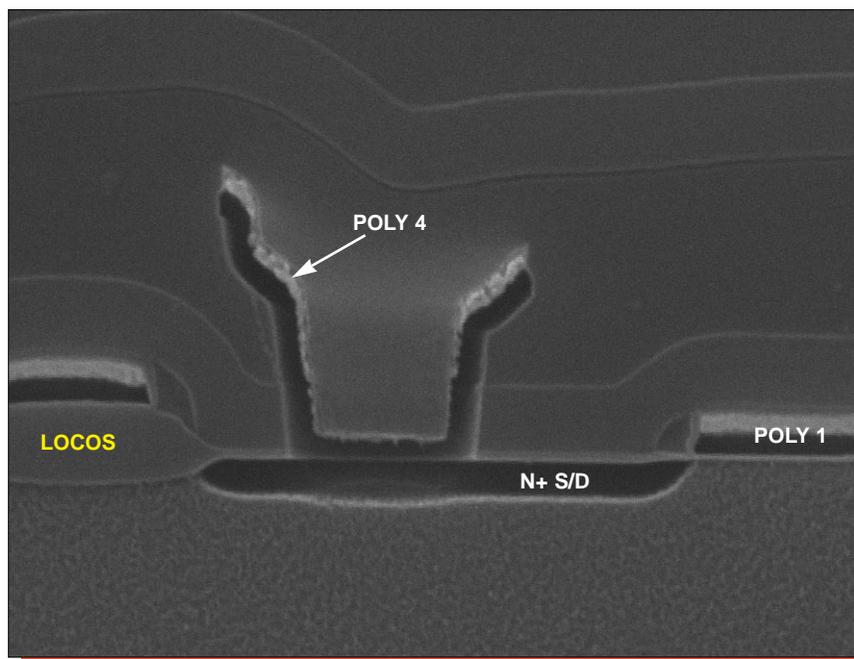
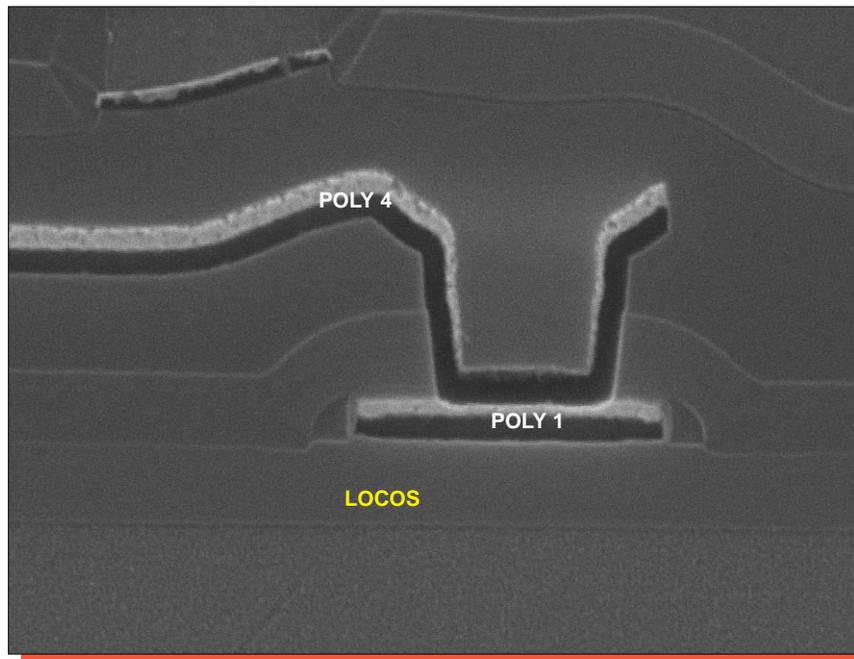


Figure 23. SEM section views illustrating typical poly 4 contacts. Mag. 26,000x.

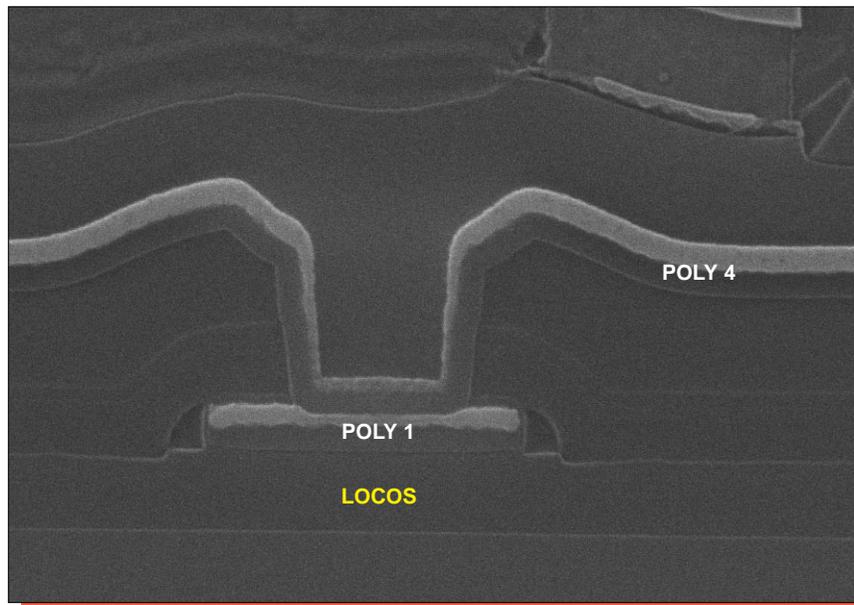
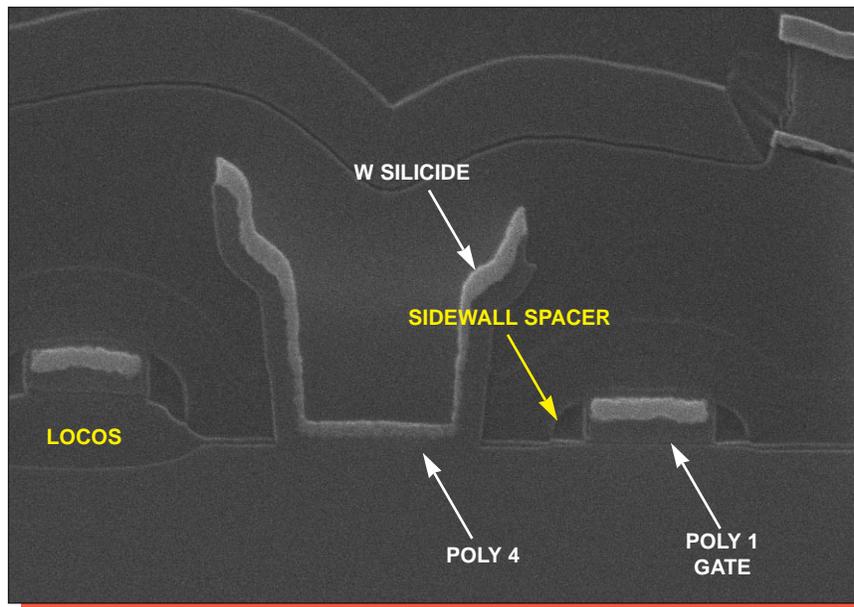
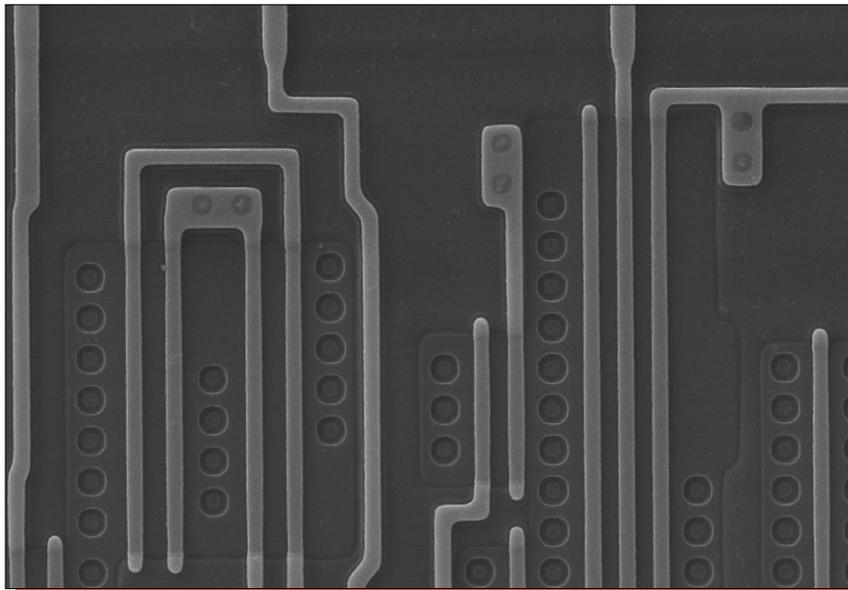
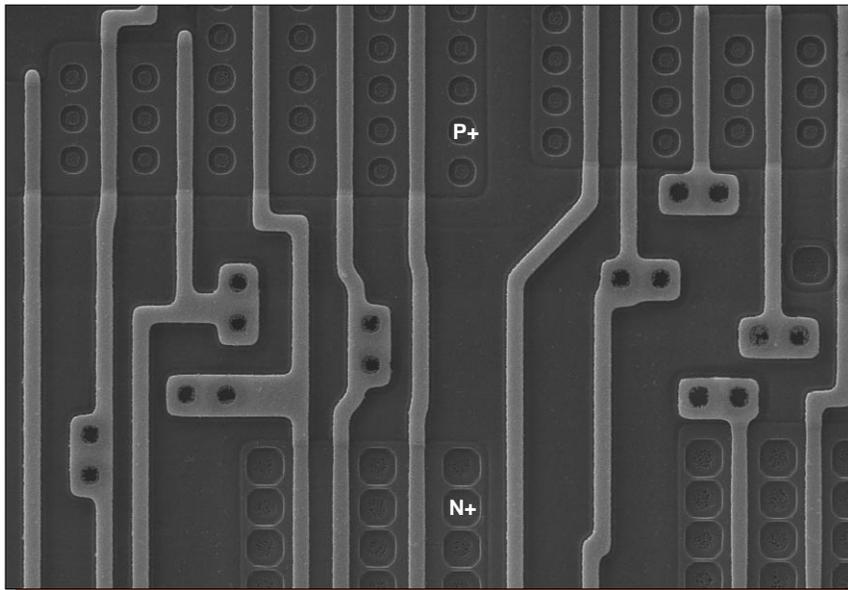


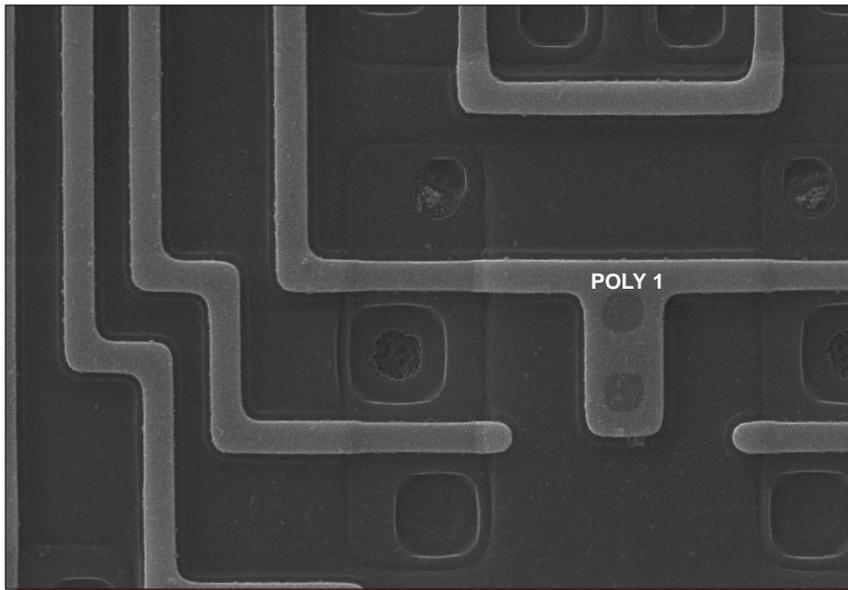
Figure 24. SEM section views illustrating typical poly 4 contacts. Glass etch, Mag. 26,000x.



Mag. 3200x

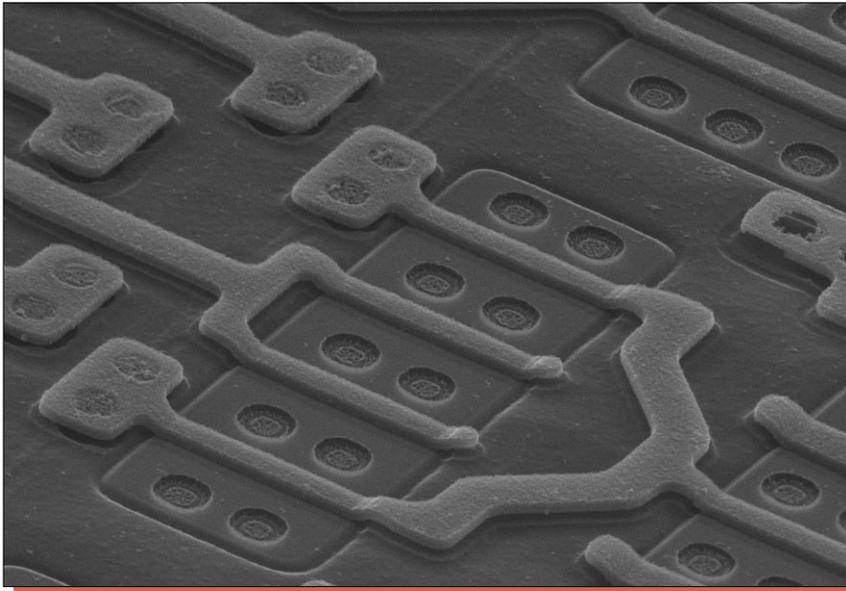


Mag. 3200x

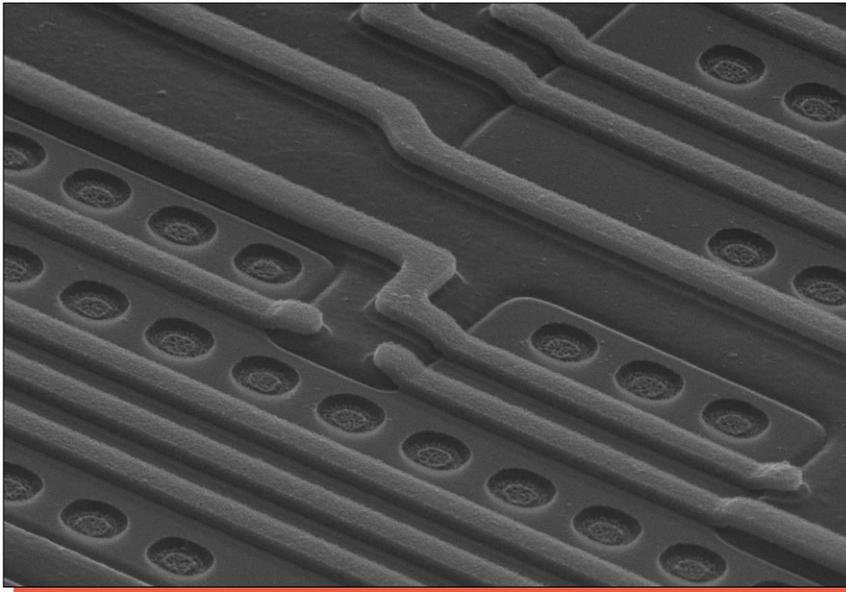


Mag. 6500x

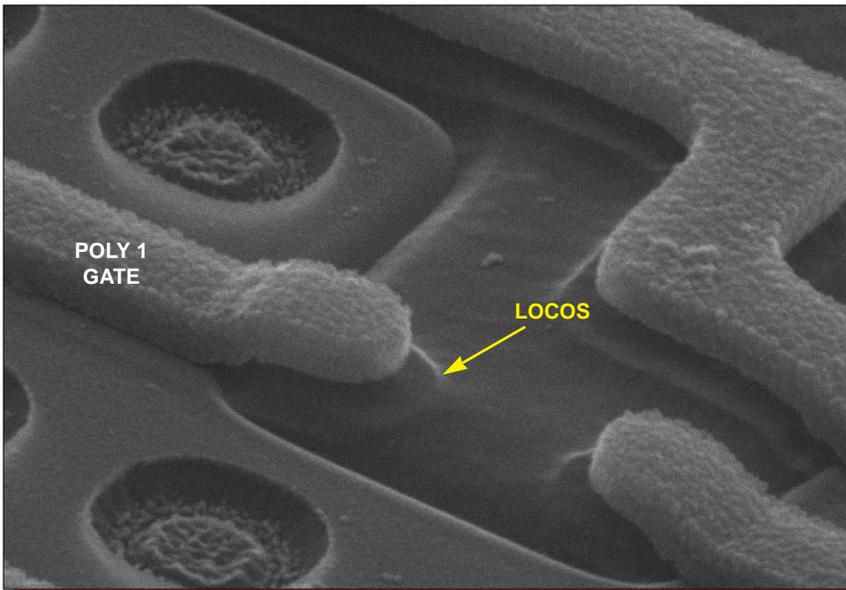
Figure 25. Topological SEM views of poly 1 patterning. 0°.



Mag. 7000x



Mag. 8000x



Mag. 28,000x

Figure 26. Perspective SEM views of poly 1 coverage. 60°.

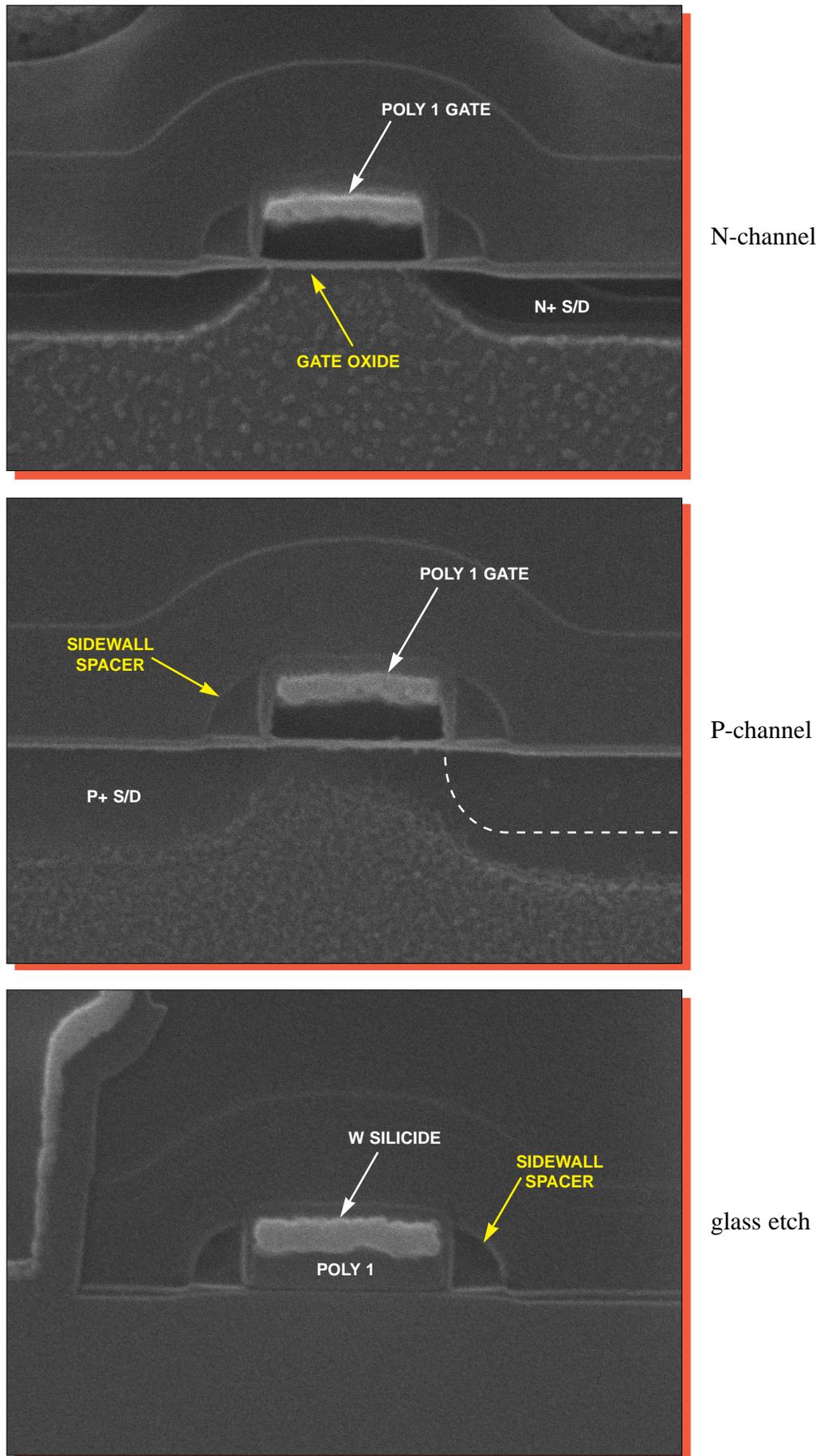


Figure 27. SEM section views of typical transistors. Mag. 52,000x.

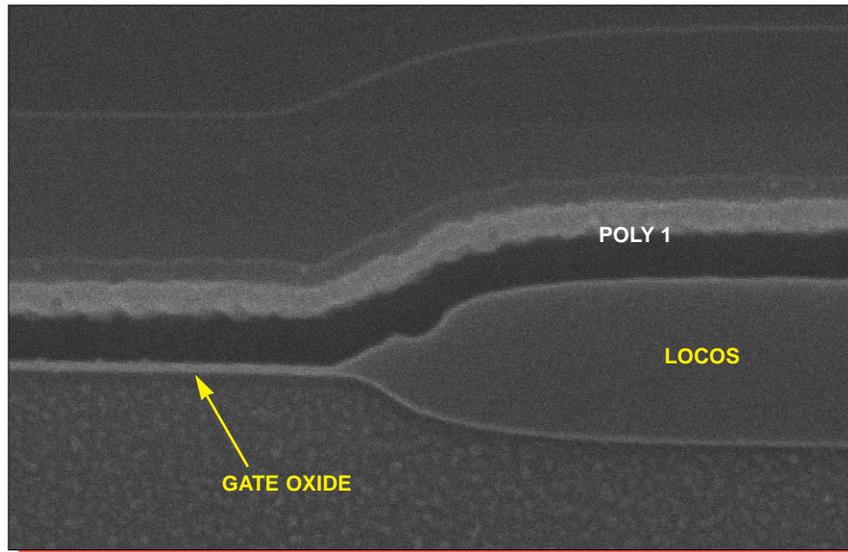
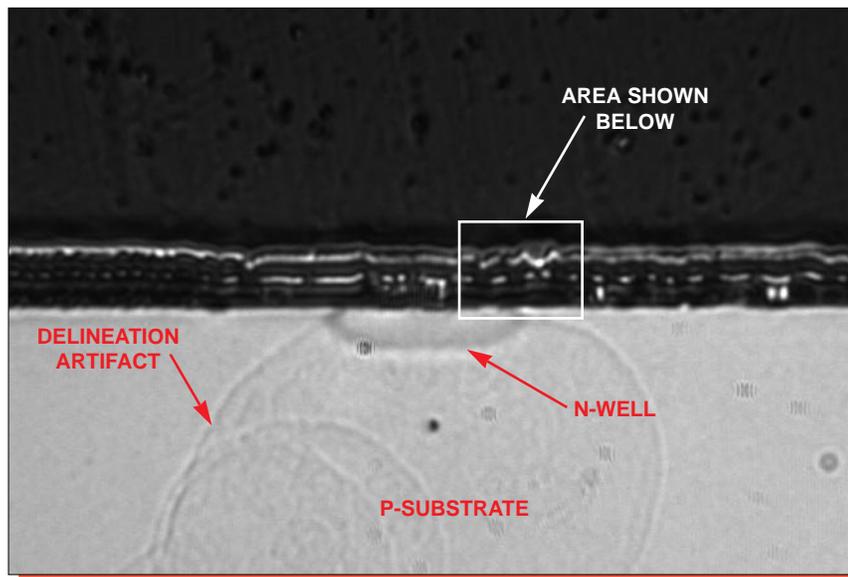
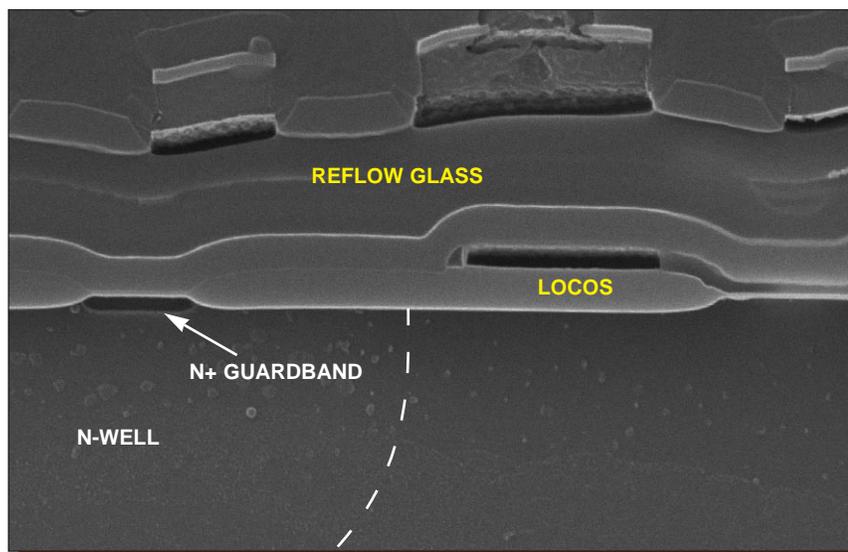


Figure 28. SEM section view of a typical birdsbeak. Mag. 52,000x.

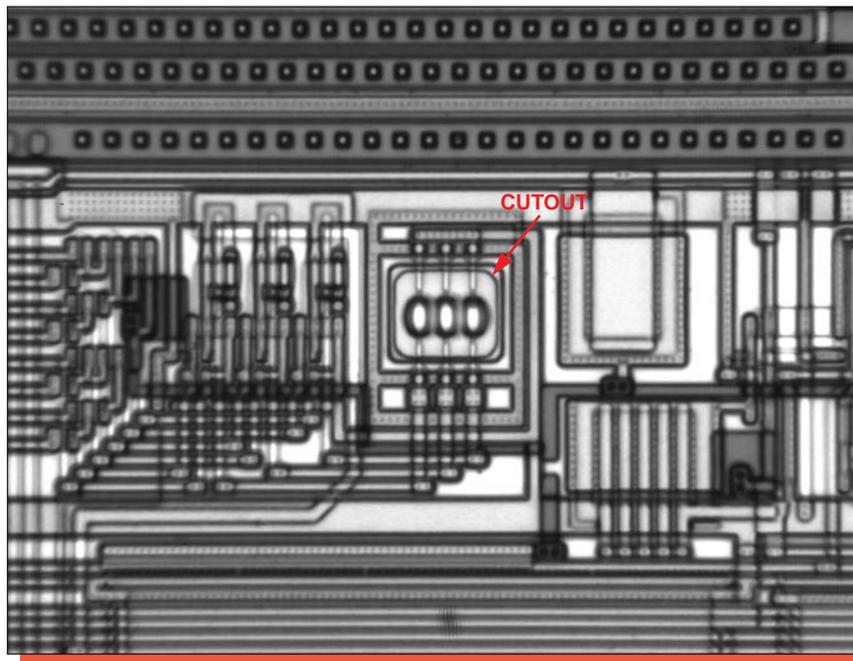


optical,
Mag. 1500x

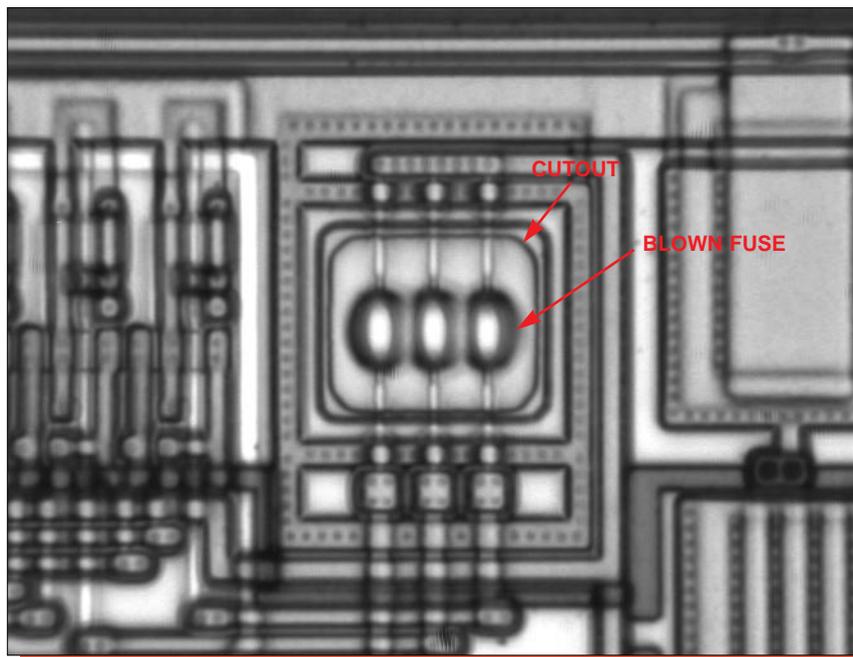


SEM,
Mag. 13,000x

Figure 29. Section views illustrating well structure.

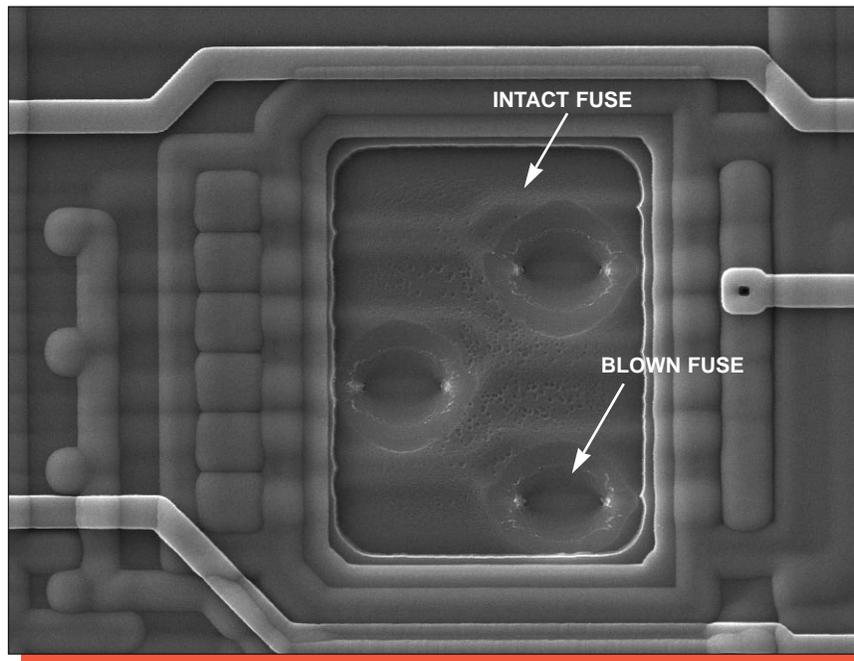


Mag. 620x

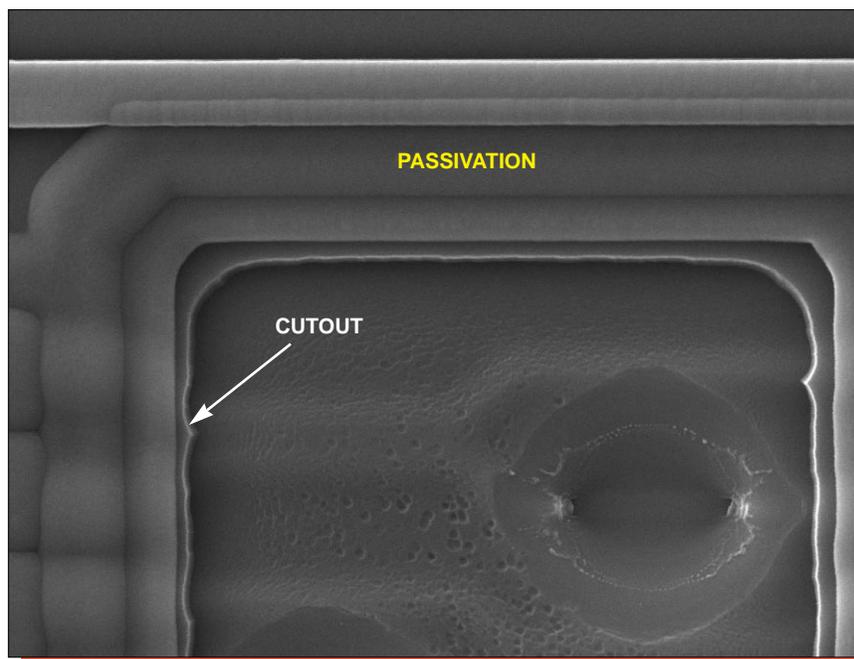


Mag. 1200x

Figure 30. Optical views of typical fuses.

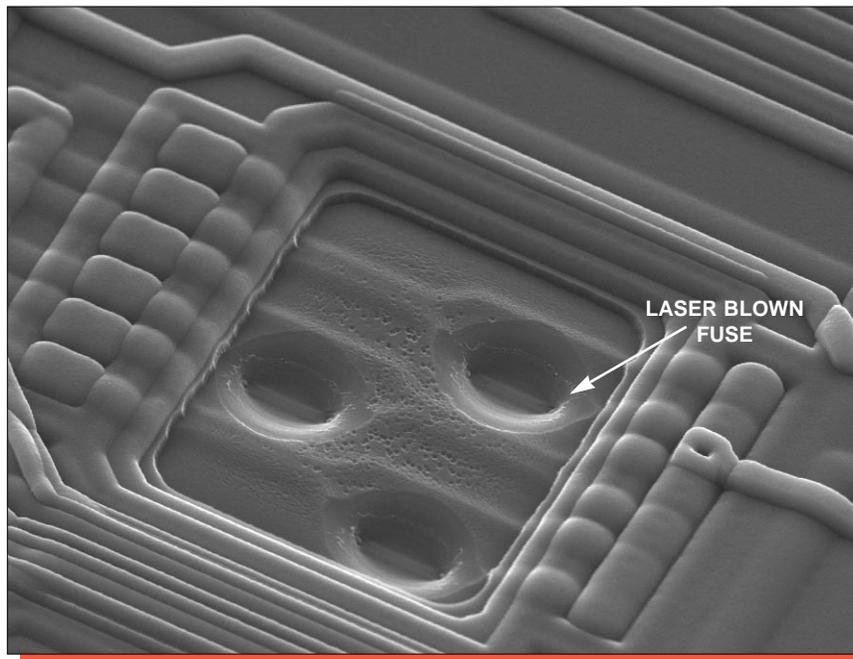


Mag. 1600x

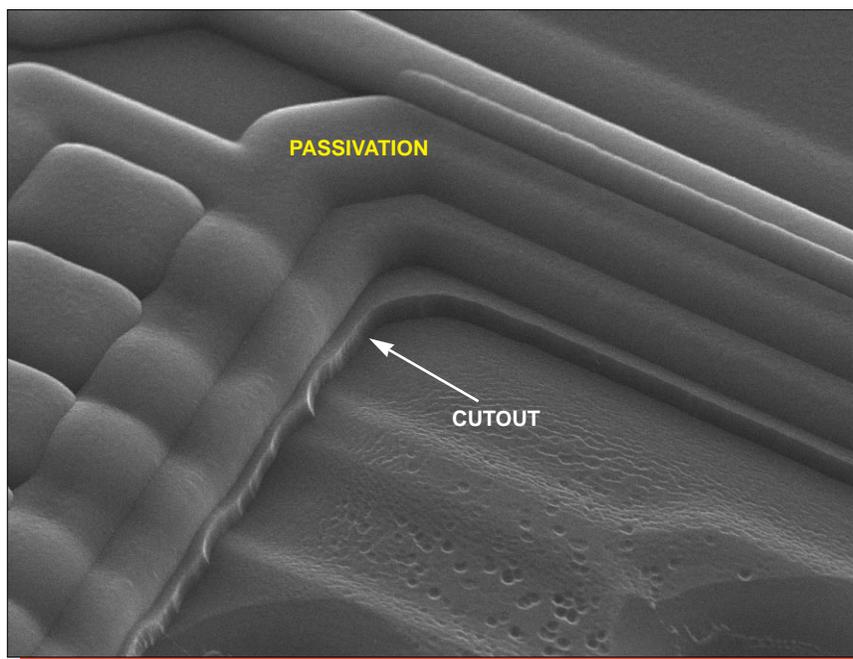


Mag. 3200x

Figure 30a. Topological SEM views of typical fuses. 0°.

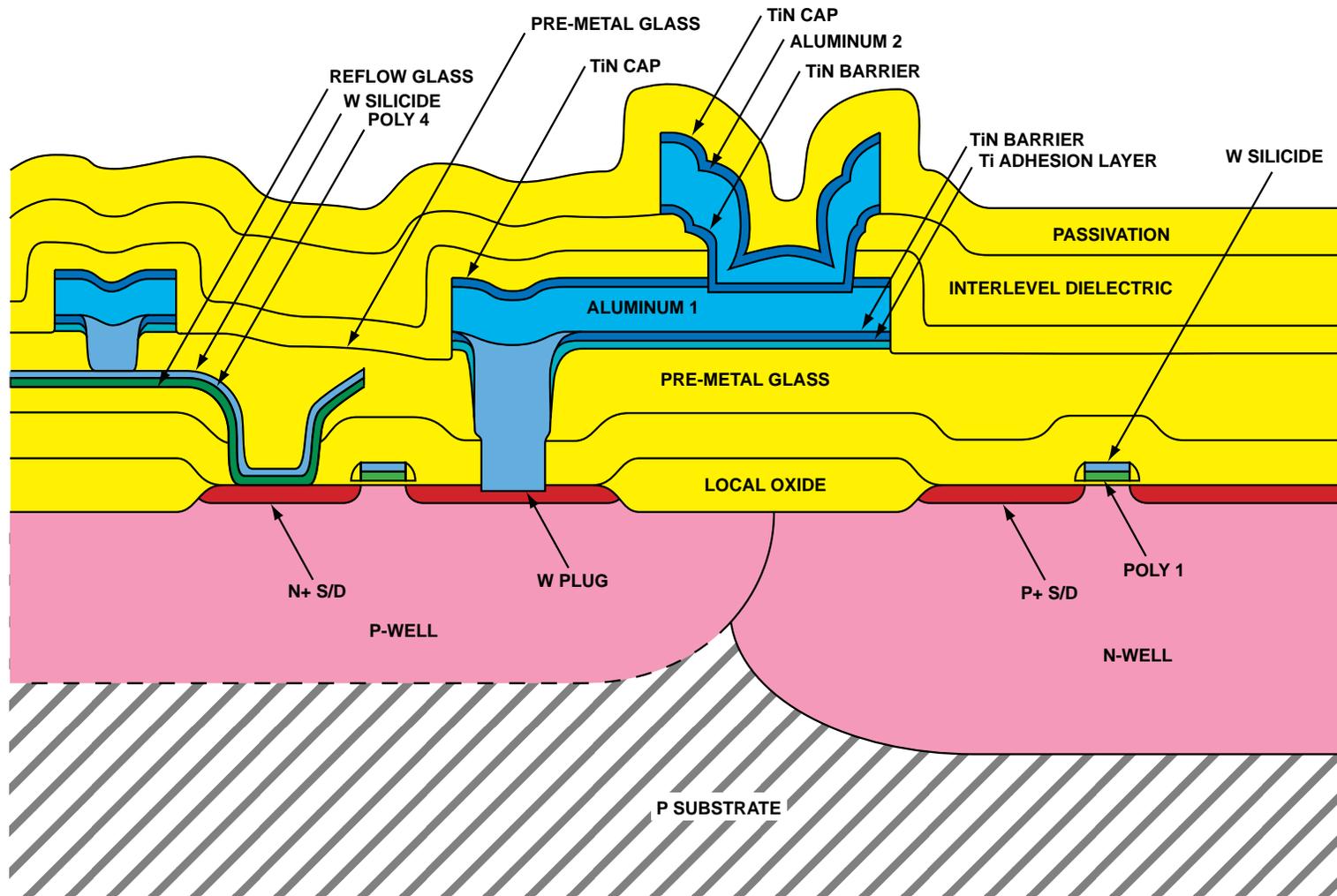


Mag. 2000x



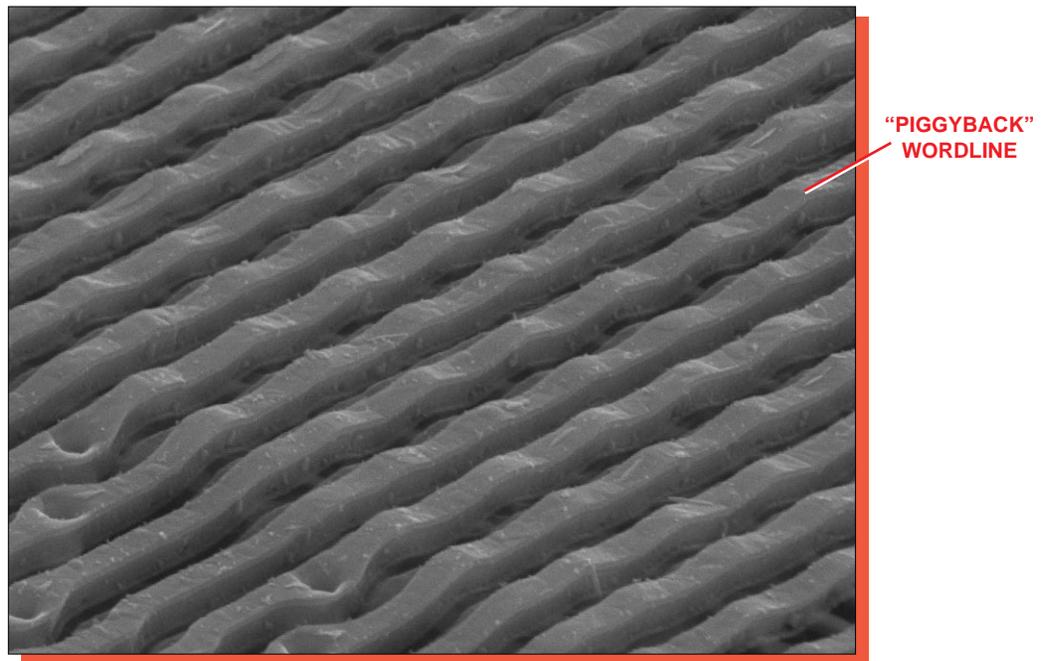
Mag. 4000x

Figure 31. Perspective SEM views of typical fuses. 60°.

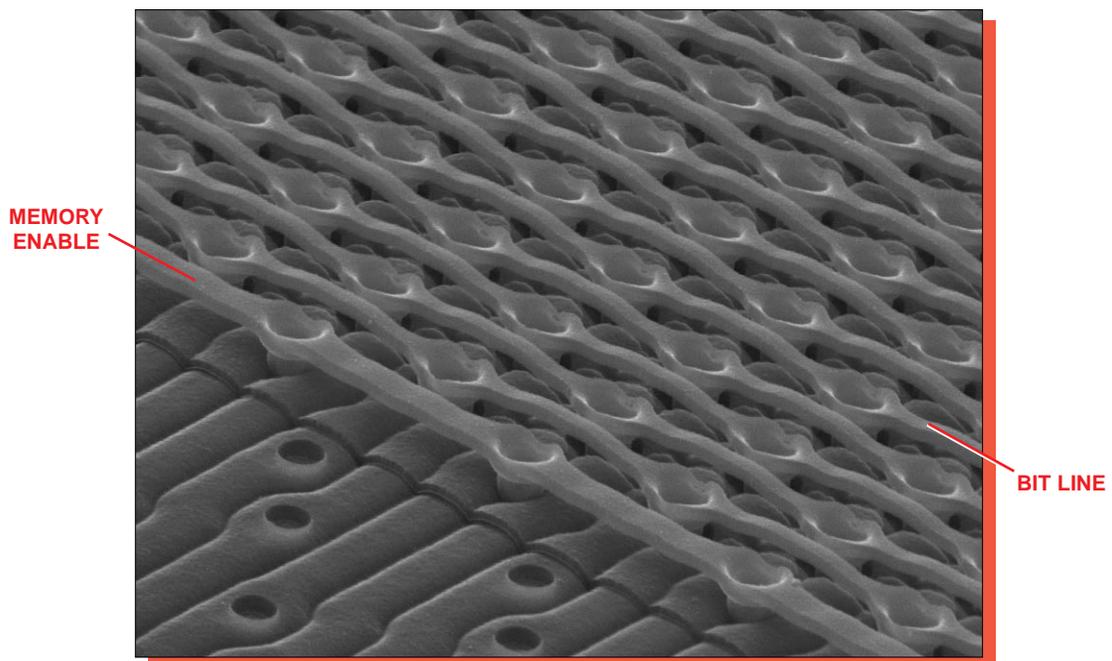


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

Figure 32. Color cross section drawing illustrating device structure.

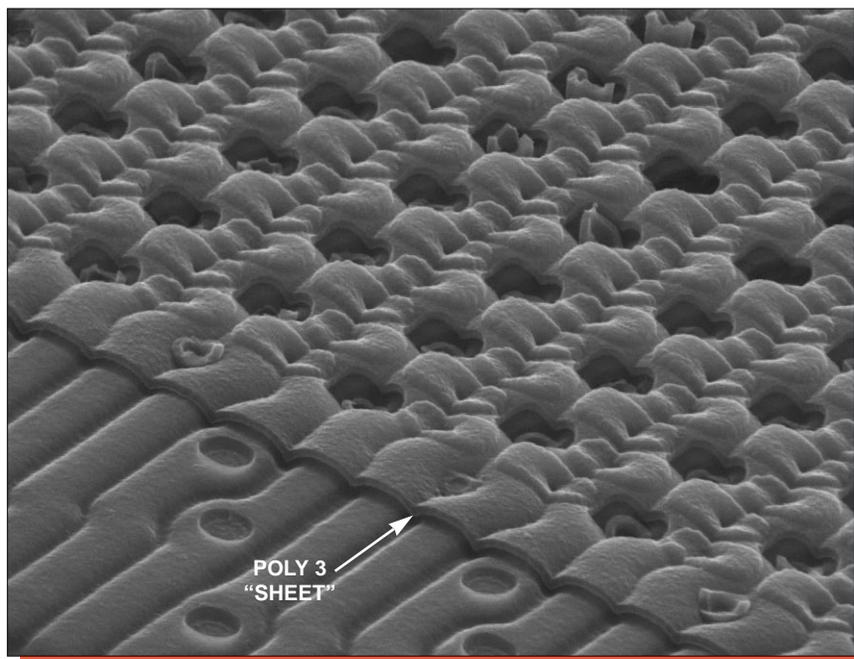


metal 1

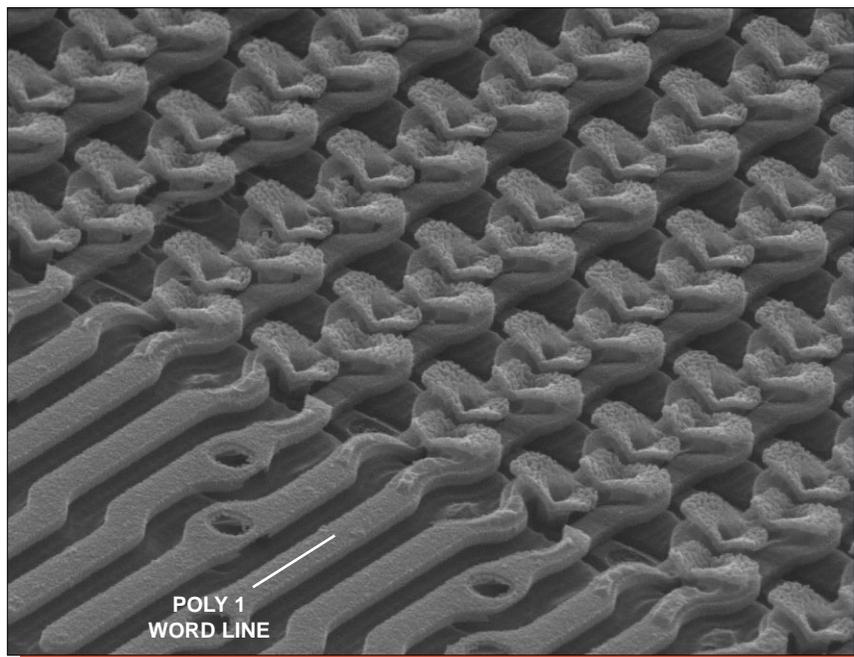


poly 4

Figure 33. Perspective SEM views of the DRAM cell array. Mag. 8000x, 60°.

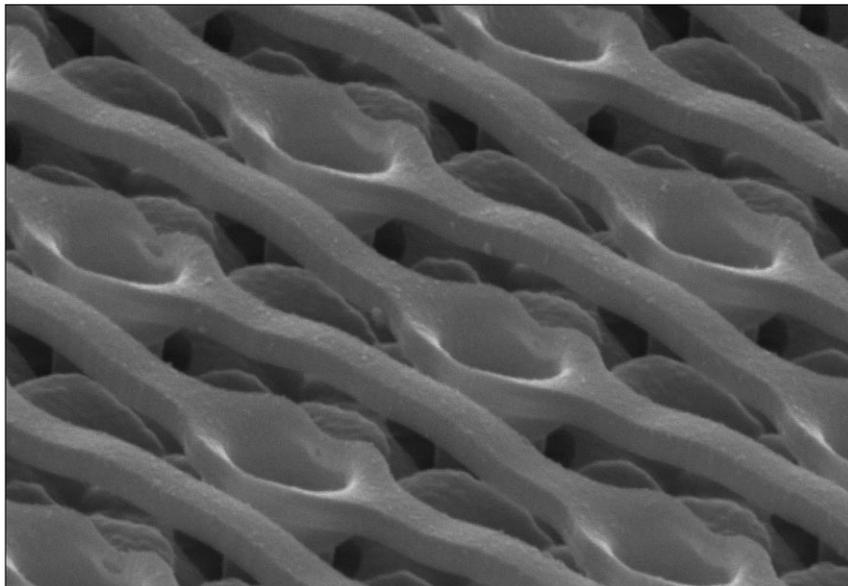


poly 3

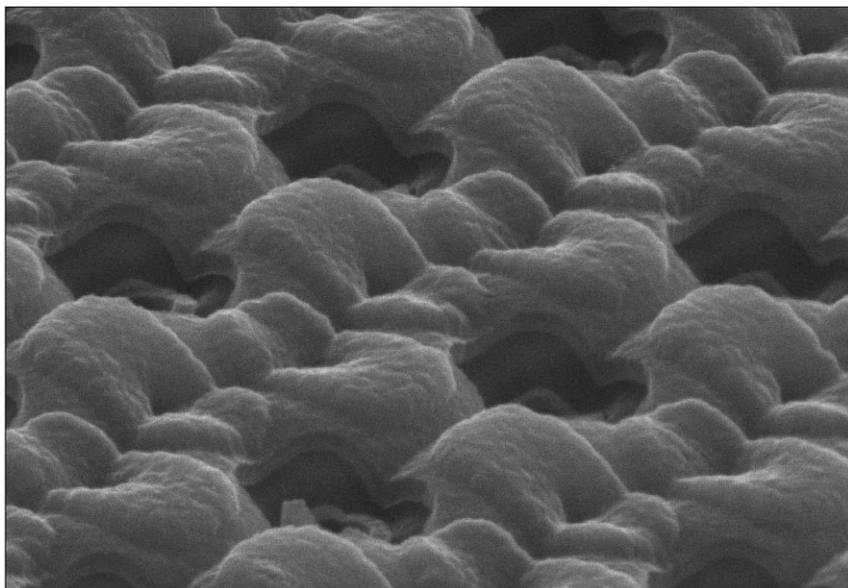


poly 2 and poly 1

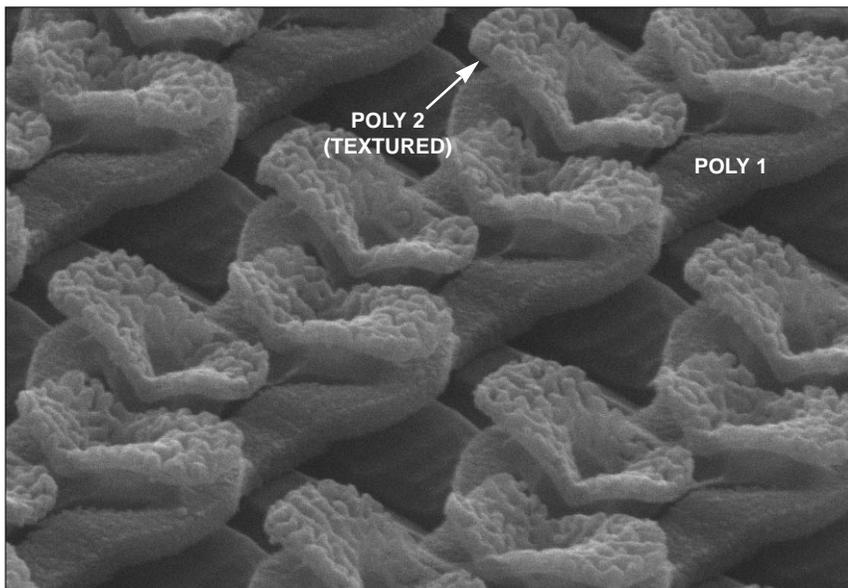
Figure 34. Perspective SEM views of the DRAM cell array. Mag. 8000x, 60°.



poly 4

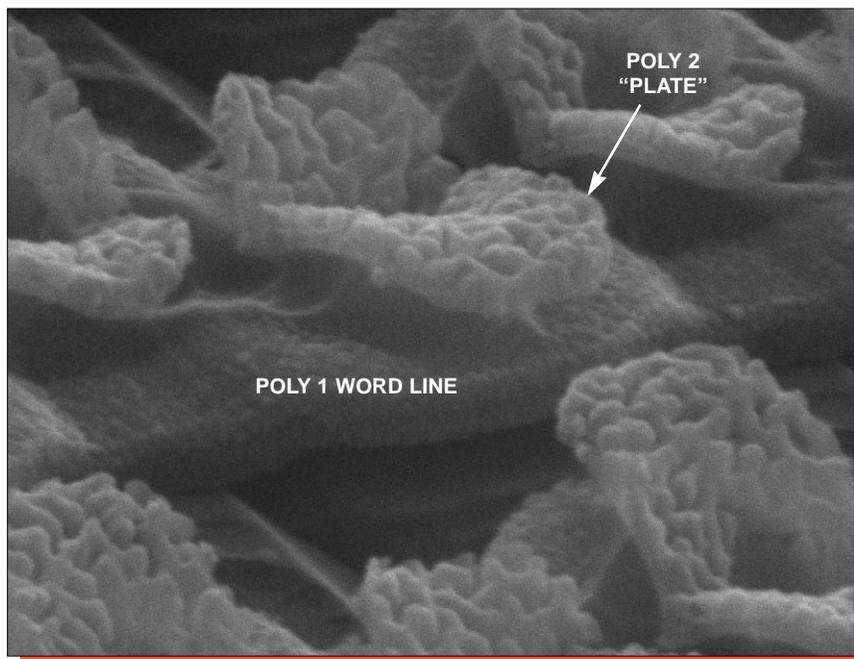


poly 3

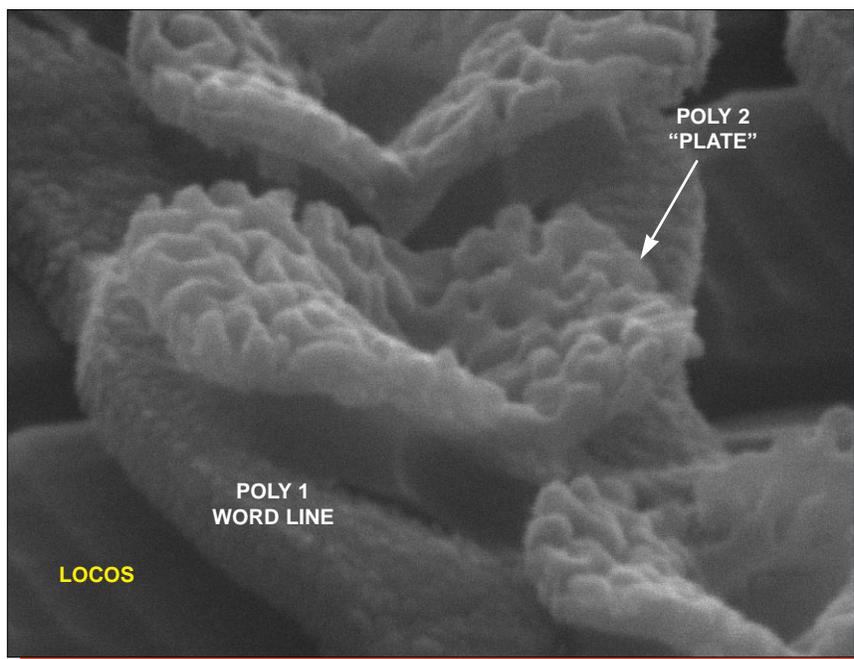


poly 2 and poly 1

Figure 35. Detailed perspective SEM views of the DRAM cell array. Mag. 20,000x, 60°.

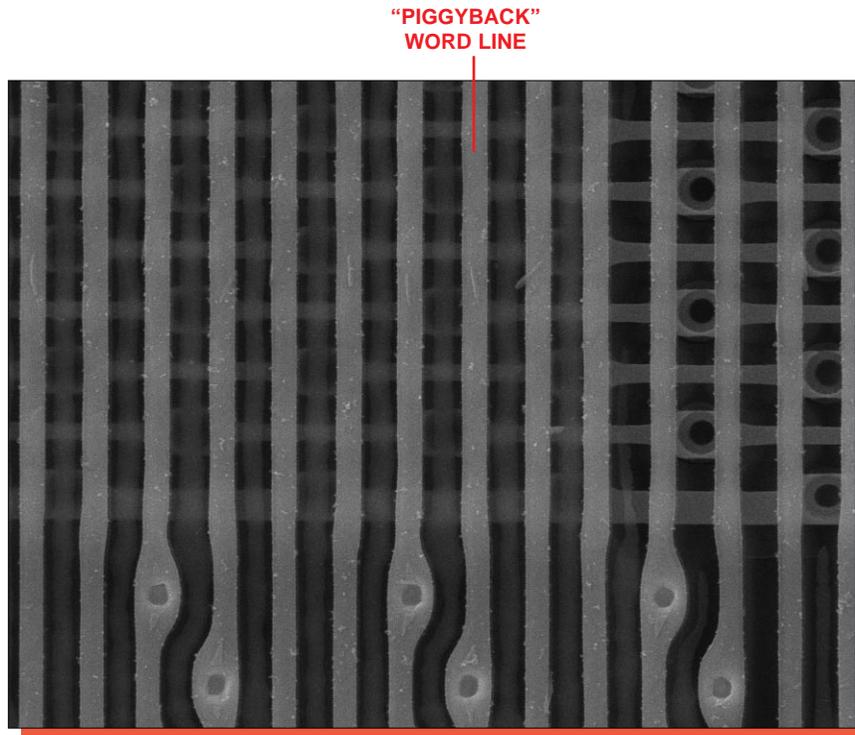


Mag. 40,000x

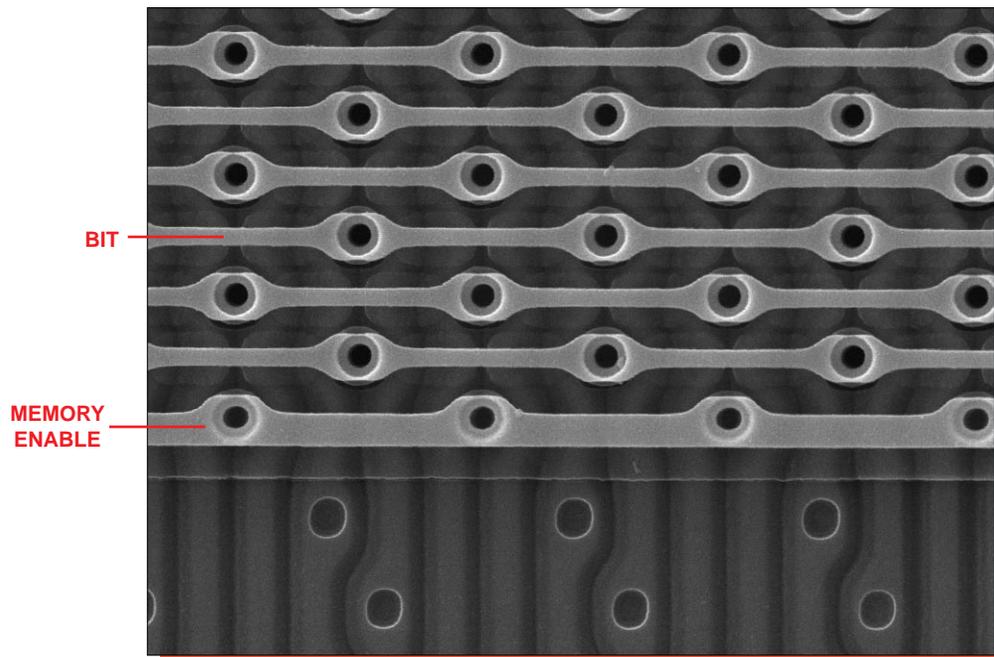


Mag. 52,000x

Figure 36. Detailed SEM views of the textured poly 2 plates. 60°.

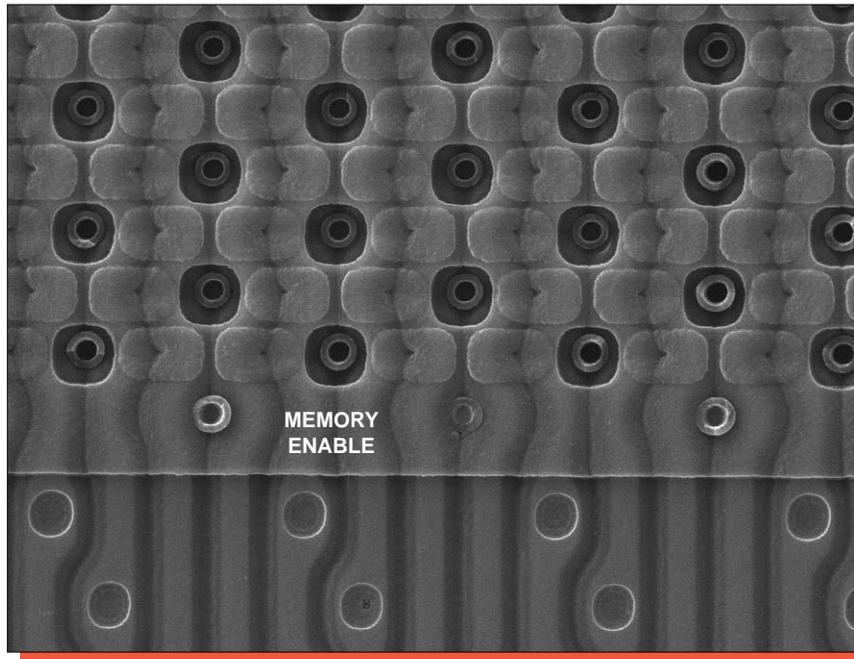


metal 1

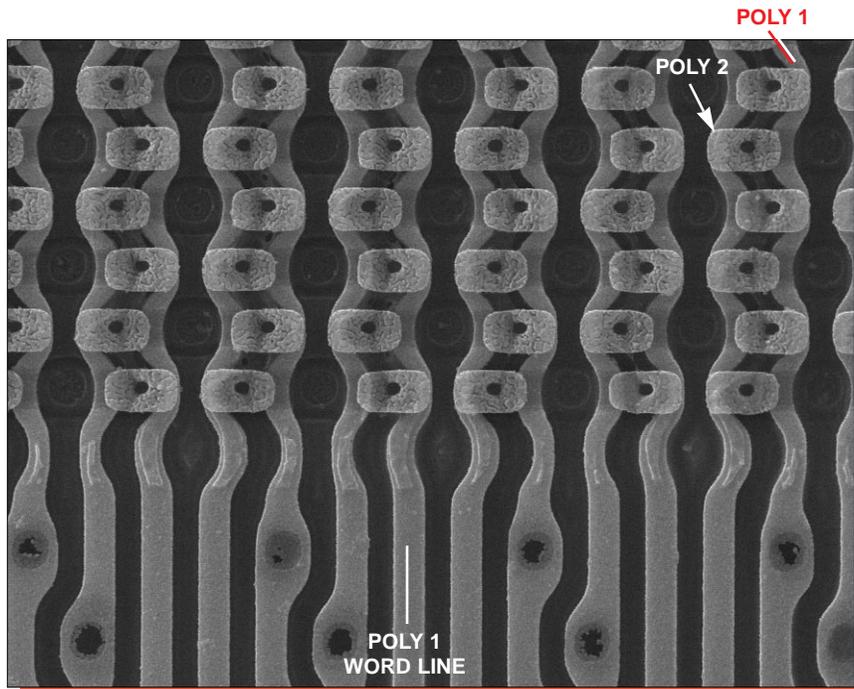


poly 4

Figure 37. Topological SEM views of the DRAM cell array. Mag. 6500x, 0°.

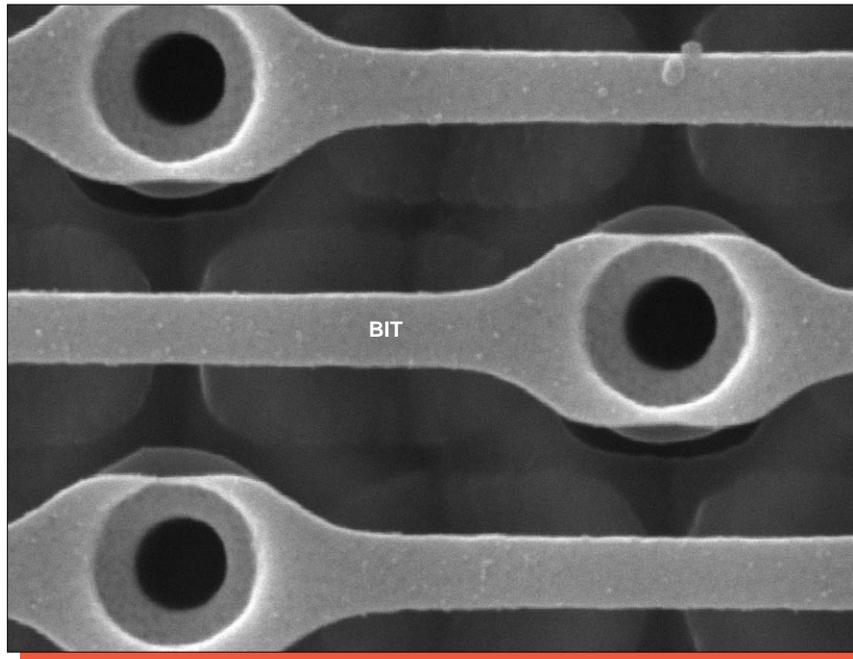


poly 3

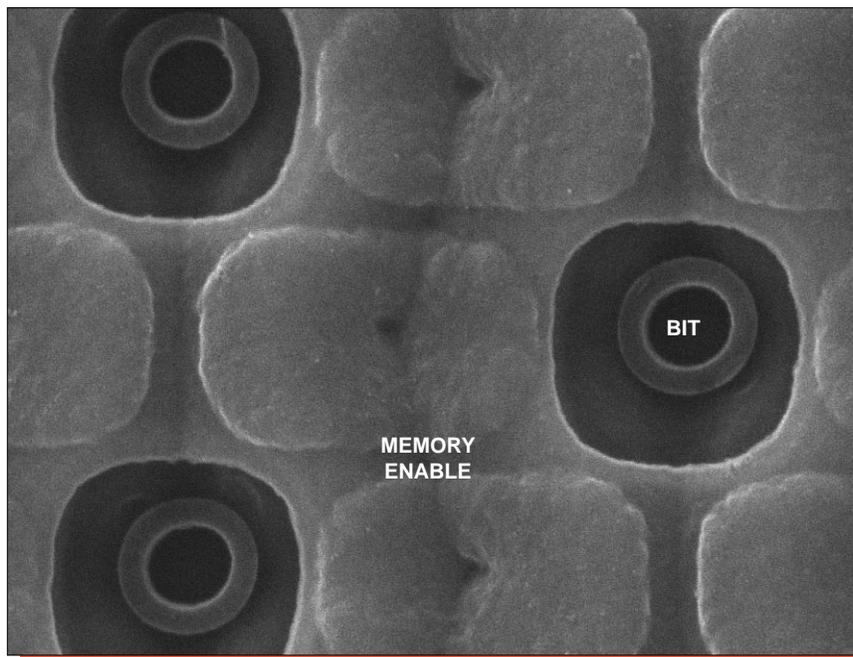


poly 2 and poly 1

Figure 38. Topological SEM views of the DRAM cell array. Mag. 6500x, 0°.



poly 4



poly 3

Figure 39. Topological SEM views of a DRAM cell. Mag. 26,000x, 0°.

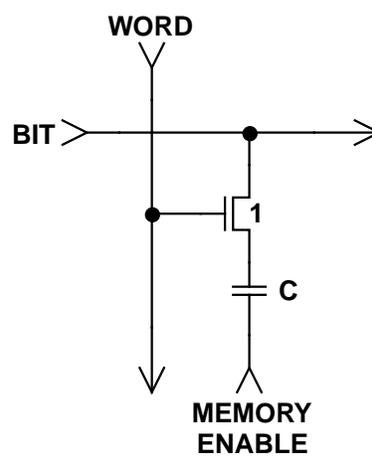
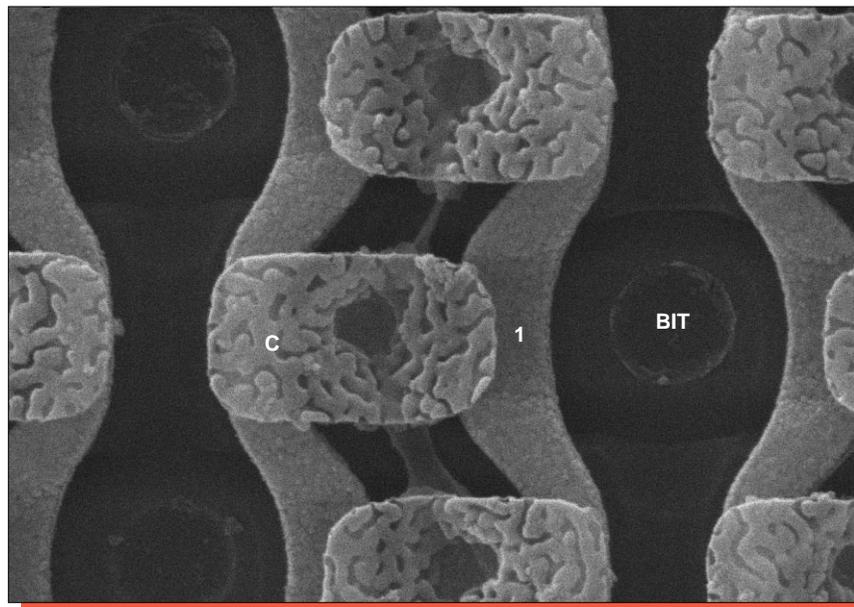
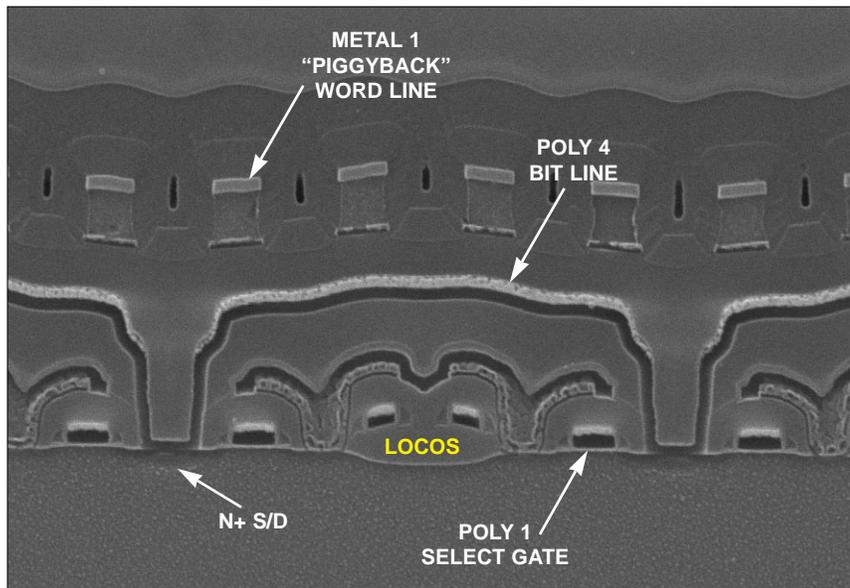
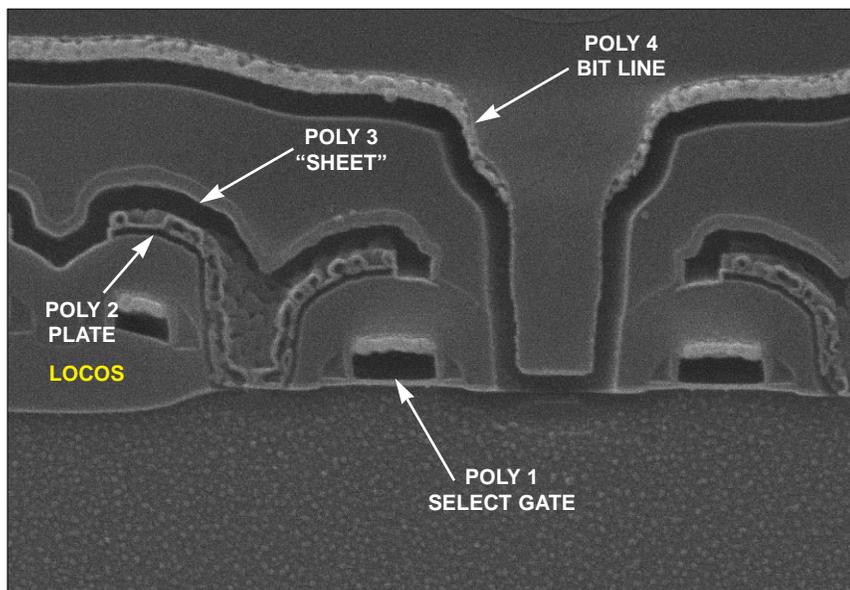


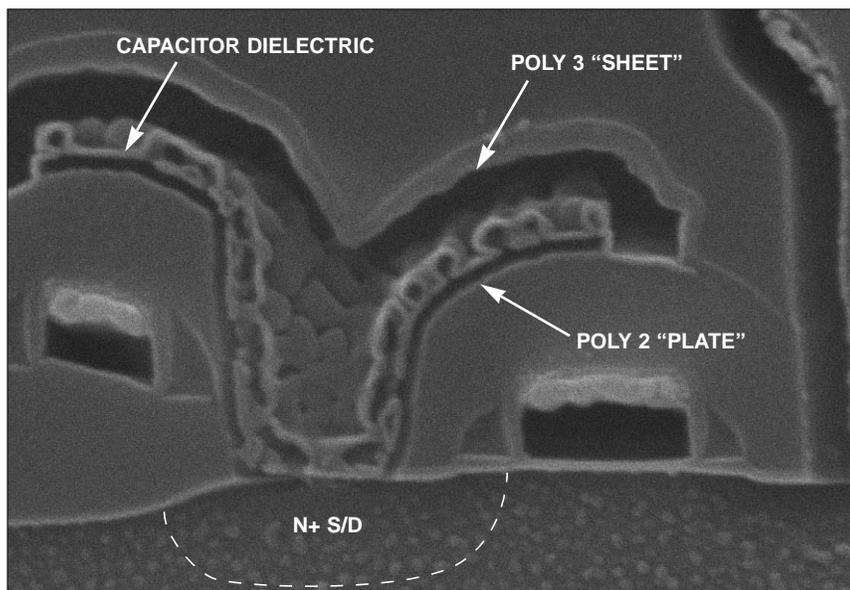
Figure 40. Topological SEM view and schematic of a DRAM cell. Mag. 26,000x, 0°.



Mag. 13,000x

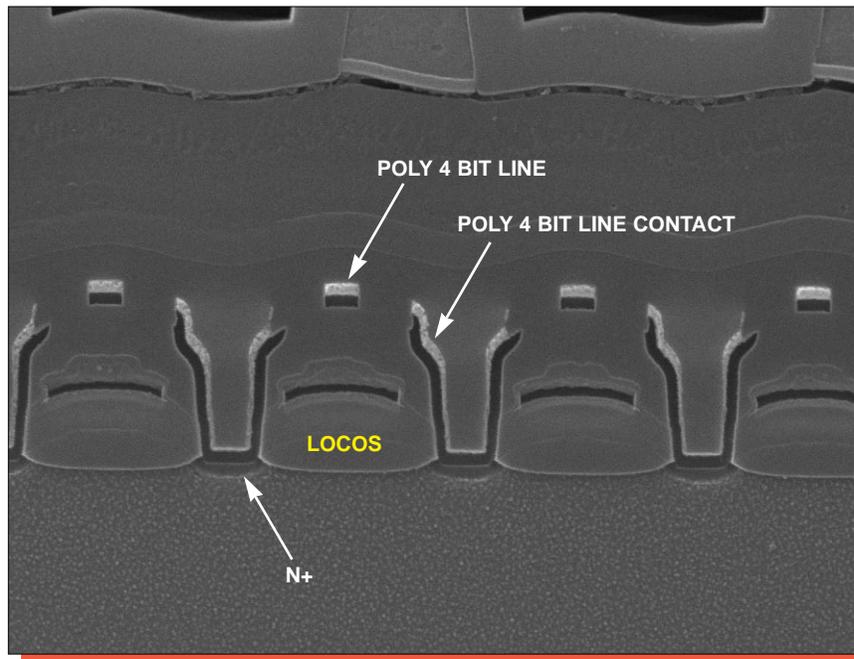


Mag. 26,000x

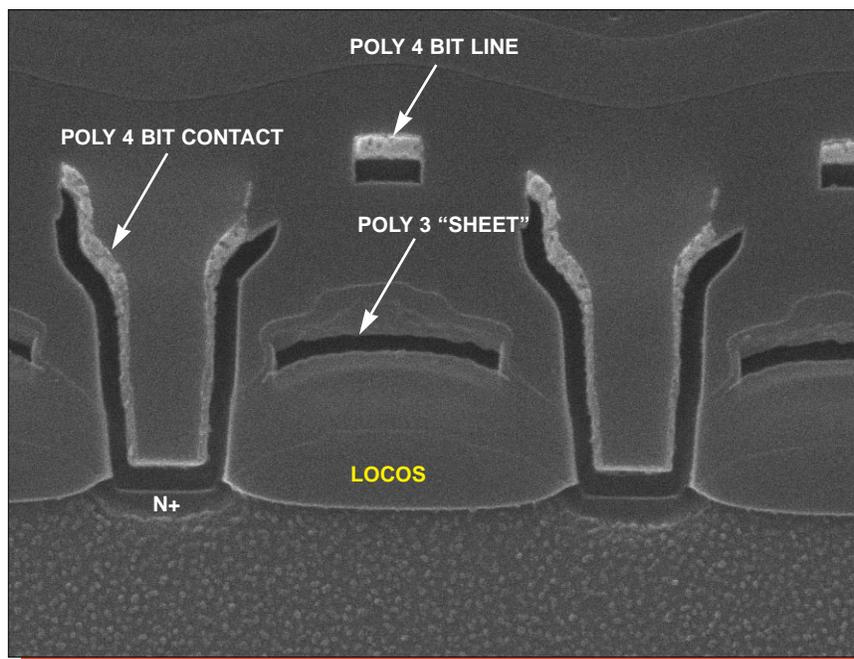


Mag. 52,000x

Figure 41. SEM section views of the DRAM cell array (parallel to bit line).

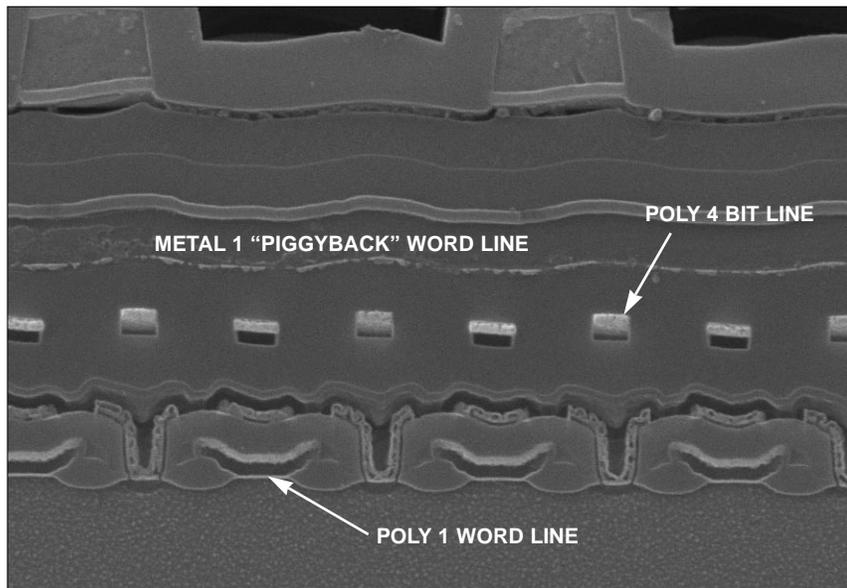


Mag. 13,000x

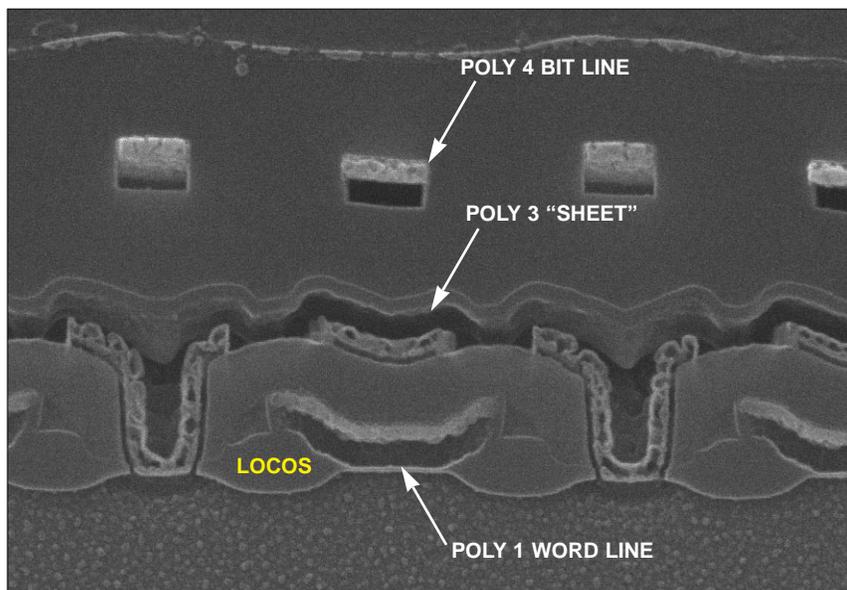


Mag. 26,000x

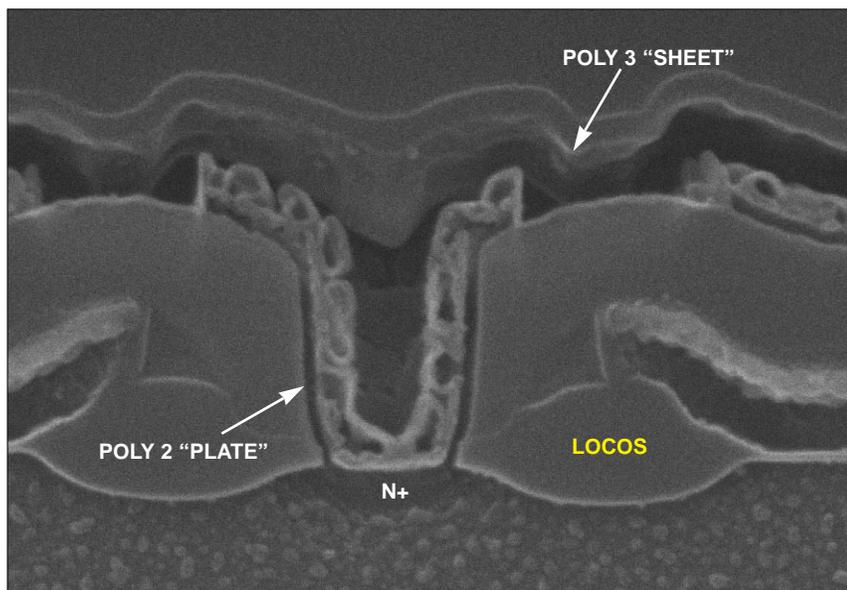
Figure 42. SEM section views of the DRAM cell array (perpendicular to bit lines).



Mag. 13,000x

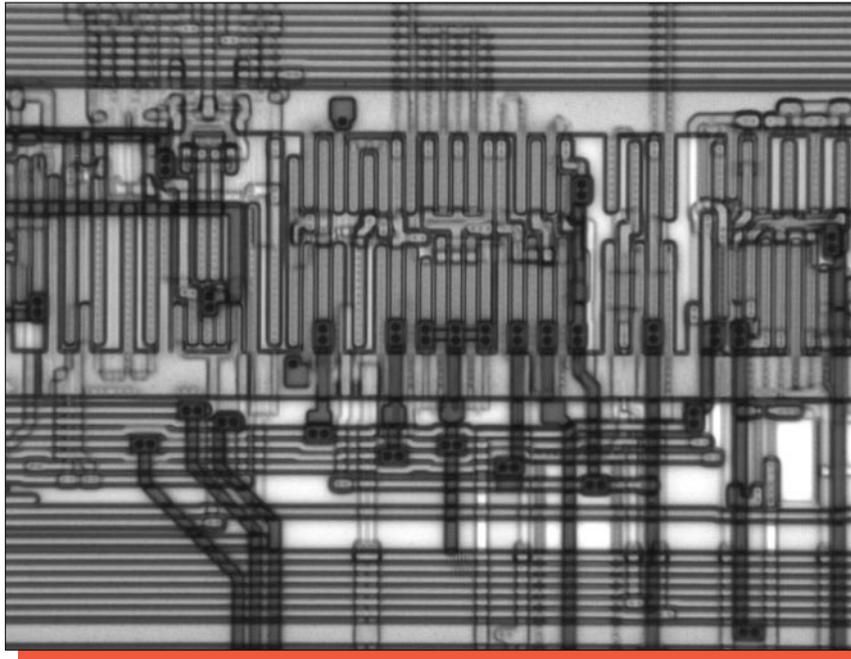


Mag. 26,000x

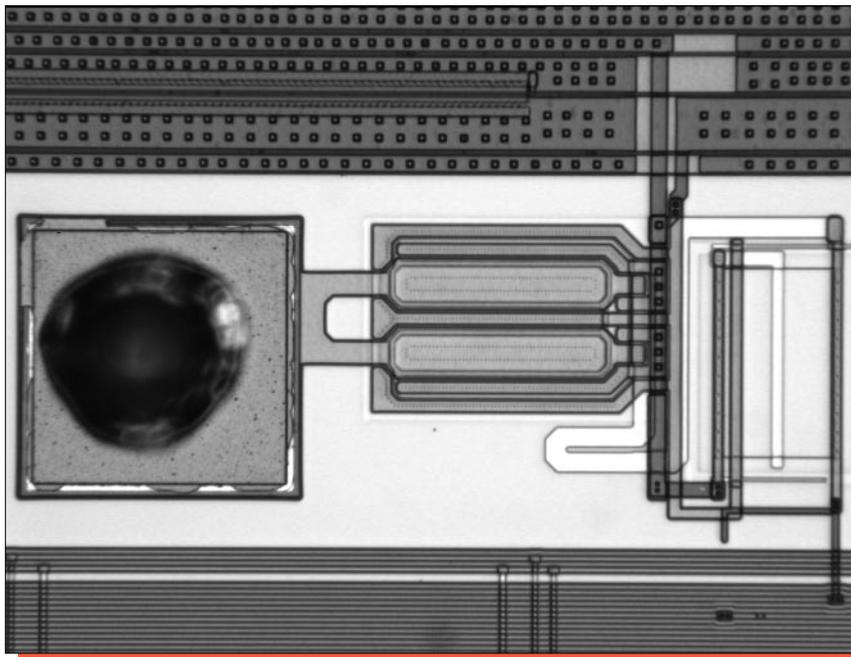


Mag. 52,000x

Figure 43. SEM section views of the DRAM cell array (perpendicular to bit lines).



Mag. 300x



Mag. 600x

Figure 44. Optical views of typical circuitry and input protection.

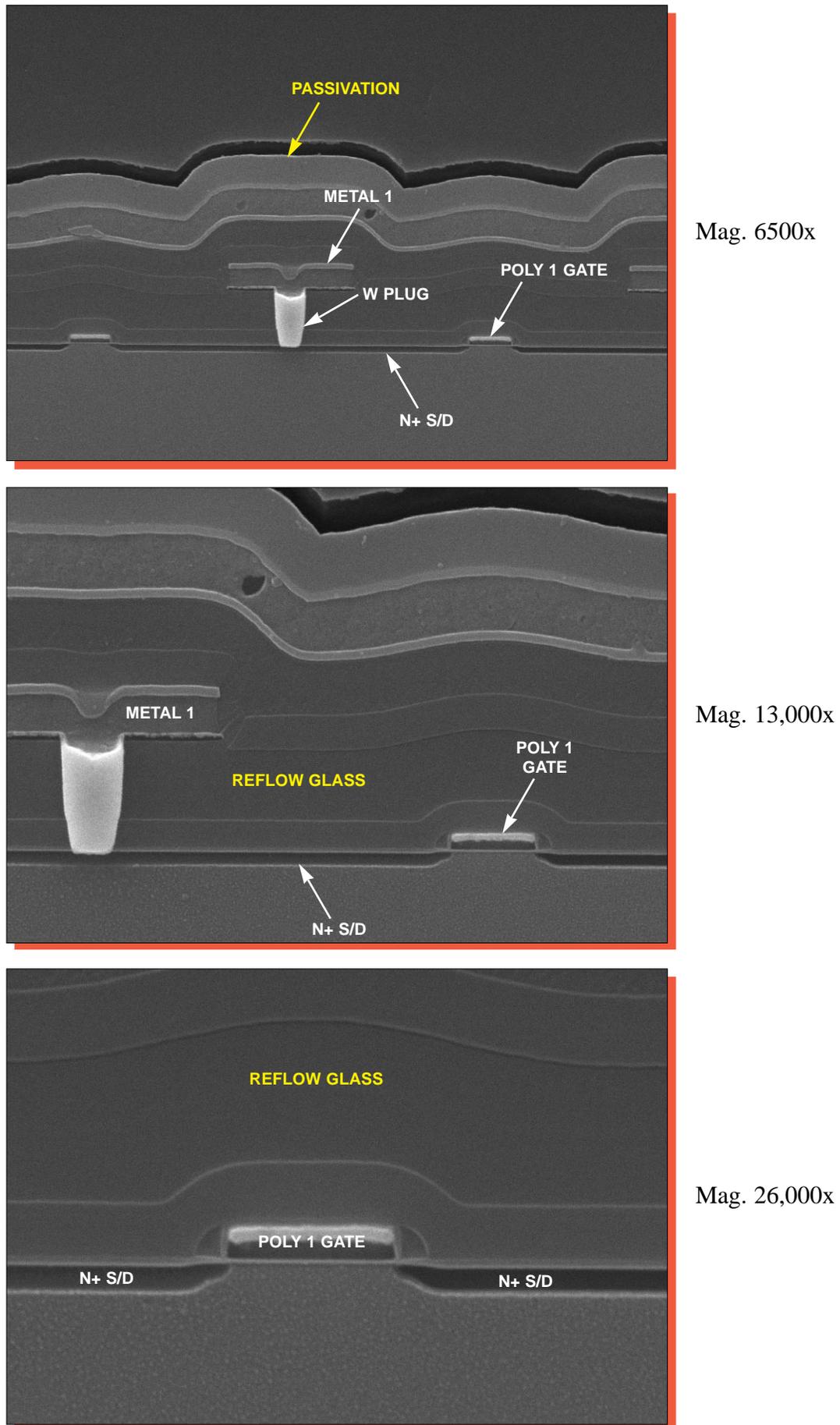


Figure 45. SEM section views of typical I/O structure.