

Construction Analysis

Xilinx XC4036EX FPGA

Report Number: SCA 9706-544



ICE
INTEGRATED CIRCUIT ENGINEERING

15022 N. 75th Street
Scottsdale, AZ 85260-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: <http://www.ice-corp.com/ice>

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INTRODUCTION

This report describes a construction analysis of the Xilinx XC4036EX Field Programmable Gate Array (FPGA). One decapped device was received for the analysis. The device was date coded 9705.

MAJOR FINDINGS

Questionable Items:¹ None. We found no areas of reliability concern.

Special Features:

- Sub-micron gate lengths (0.45 micron N-channel and 0.5 micron P-channel).
- 5T SRAM (select-RAM) cells for programming.
- Reflowed (?) aluminum filled vias.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Die Process and Design:

- The device was fabricated using a selective oxidation, N-well CMOS process in a P-substrate. No epi was used.
- Passivation consisted of a layer of nitride over a layer of silicon-dioxide.
- Three levels of metal interconnect were used. Metal 3 and metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride (TiN) cap and barrier. A thin titanium (Ti) adhesion layer was used under metal 1. Aluminum filled vias were used under both metal 3 and metal 2 and tungsten (W) plugs were used for contacts under metal 1. A titanium nitride (TiN) layer was present under the plugs.
- Interlevel dielectrics consisted of three layers of glass. The first layer was quite thin. The second layer was an SOG subjected to an etchback for planarization. A thick third layer covered these.
- Pre-metal glass consisted of a layer of reflow glass over various densified oxides. Glass was reflowed prior to contact cuts only.
- A single layer of polycide (poly with tungsten silicide) was used to form all the gates on the die. Definition was by a dry etch of normal quality.
- Implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. The process used oxide sidewall spacers that were left in place.
- Local oxide (LOCOS) isolation. No step was present in the oxide at the edge of the well, and no other signs of the use of P-wells was found.

TECHNOLOGY DESCRIPTION (continued)

- The memory cell array utilized a 5T SRAM cell design. Metal 3 was used to form the word lines. Metal 2 was used to form the bit lines and distribute GND and Vcc (via metal 1). Metal 1 provided cell interconnect. Poly was used to form all gates. Variations in the metal interconnect layout were observed.

ANALYSIS RESULTS I

Die Process:

Figures 1 - 32

Questionable Items:¹ None. As mentioned, we found no quality concerns whatsoever.

Special Features:

- Sub-micron gate lengths (0.45 micron N-channel and 0.5 micron P-channel).
- 5T SRAM (select-RAM) cells for programming.
- Reflowed (?) aluminum filled vias.

General items:

- Fabrication process: Devices were fabricated using a selective oxidation, N-well CMOS process in a P-substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good.
- Metal interconnect employed three levels of metal. Metal 3 and metal 2 consisted of aluminum with a titanium-nitride (TiN) cap and titanium (Ti) barrier. Metal 1 consisted of aluminum with a titanium-nitride (TiN) cap and barrier on a thin

¹*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS I (continued)

titanium (Ti) adhesion layer. Aluminum filled vias were used under both metal 3 and metal 2, and tungsten (W) plugs were used for contacts under metal 1.

- Metal patterning: All three metal levels were patterned by a dry etch of normal quality.
- Metal defects: No voiding, notching, or neckdown was noted in the metal 3 or metal 2. No silicon nodules were noted following removal of either metal layer. No problems were noted in any of the layers.
- Metal step coverage: Vias under metal 3 and metal 2 were completely surrounded by metal. Metal 1 used plugs at contacts. Metal 3 and metal 2 had virtually no thinning due to the use of the aluminum filled vias. No thinning was present in metal 1 because of the use of tungsten (W) plugs at contacts.
- Interlevel dielectrics consisted of three layers of glass. The first layer was a thin even thickness, not planarized in any way. The second layer was an SOG subjected to an etchback for planarization. The third covering layer was of even and substantial thickness, and in fact may have been a triple layer rather than a single homogeneous layer. No problems were noted.
- Pre-metal glass: A layer of reflow glass (BPSG) over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.
- Vias and contacts: Via cuts were defined by a two-step process. Vias appeared to have been patterned using a controlled overetch to just penetrate the titanium nitride cap to the aluminum underneath. Contacts used an apparent single etch step, lined with the titanium-nitride barrier and then filled with tungsten. No problems were found.

ANALYSIS RESULTS I (continued)

- A single layer of polycide (poly and tungsten silicide) was used to form all gates on the die. Definition was by a dry-etch of normal quality.
- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. The process used oxide sidewall spacers that were left in place. No problems were found.
- Local oxide (LOCOS) isolation was used. No step was present in the oxide at the well boundaries, nor did we find any other evidence of the use of P-wells.
- The memory cell array utilized a 5T SRAM cell design. Metal 3 was used to form the word lines. Metal 2 was used to form the bit lines and distribute GND and Vcc (via metal 1). Metal 1 provided cell interconnect. Poly was used to form all gates. Cell pitch was 8.7 x 9.5 microns. Process in the array appeared identical to the rest of the die.
- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection

SEM of passivation

Passivation integrity test

Passivation removal

SEM inspection of metal 3

Metal 3 removal and inspect barrier

Delayer to metal 2 and inspect

SEM inspection of metal 2

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly and die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	G
Metal registration	N
Contact coverage	G
Contact registration	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIAL ANALYSIS

Final passivation:	A layer of silicon-nitride over a layer of glass.
Metallization 3:*	Aluminum (Al) with a titanium-nitride (TiN) cap and titanium (Ti) barrier.
Metallization 2:*	Aluminum (Al) with a titanium-nitride (TiN) cap and titanium (Ti) barrier.
Metallization 1:*	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier on a thin titanium (Ti) adhesion layer.
Silicide (poly):	Tungsten (W).

**No evidence of silicon or copper doping was found but amounts less than 0.5 wt. percent may have been present.*

VERTICAL DIMENSIONS

Die thickness:	0.4 mm (15 mils)
<u>Layers:</u>	
Passivation 2:	0.6 micron
Passivation 1:	0.4 micron
Metal 3 - cap:	0.06 micron (approximate)
- aluminum:	1.0 micron
- barrier:	0.08 micron (approximate)
Interlevel dielectric 2 - glass 3:	0.45 micron
- glass 2:	0.6 micron
- glass 1:	0.08 micron (approximate)
Metal 2 - cap:	0.06 micron (approximate)
- aluminum:	0.45 micron
- barrier:	0.08 micron (approximate)
Interlevel dielectric 1- glass 3:	0.5 micron
- glass 2:	0.65 micron
- glass 1:	0.09 micron (approximate)
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.1 micron
Pre-metal dielectric:	0.3 micron (average)
Oxide on poly:	0.11 micron
Poly - silicide:	0.1 micron
- poly:	0.15 micron
Local oxide:	0.4 micron
N+ S/D:	0.22 micron
P+ S/D:	0.15 micron
N-well:	3.75 microns

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GENERAL CIRCUIT LAYOUT	Figure 28

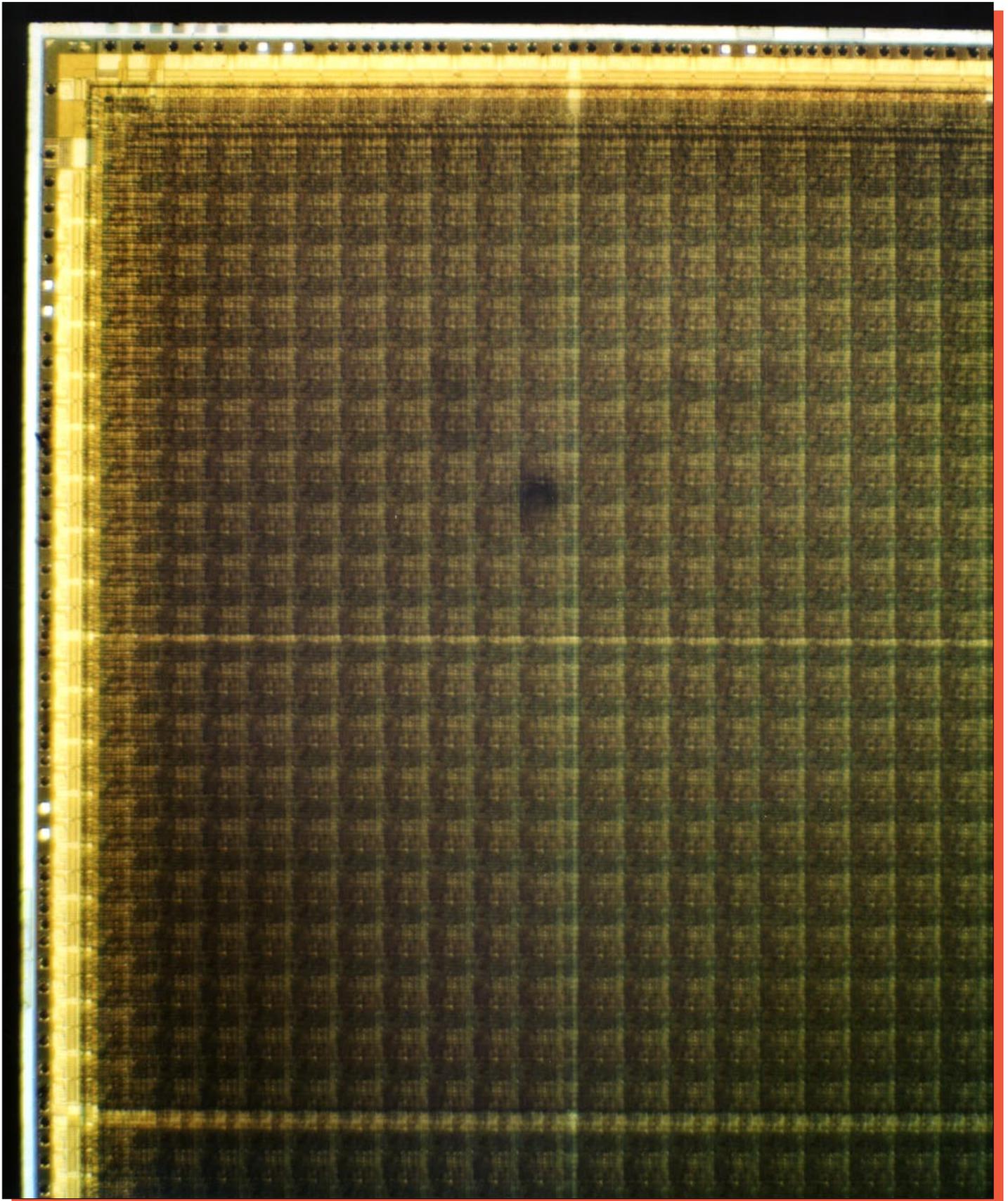


Figure 1. Portion of the whole die photograph of the Xilinx XC4036EX. Mag. 10x.

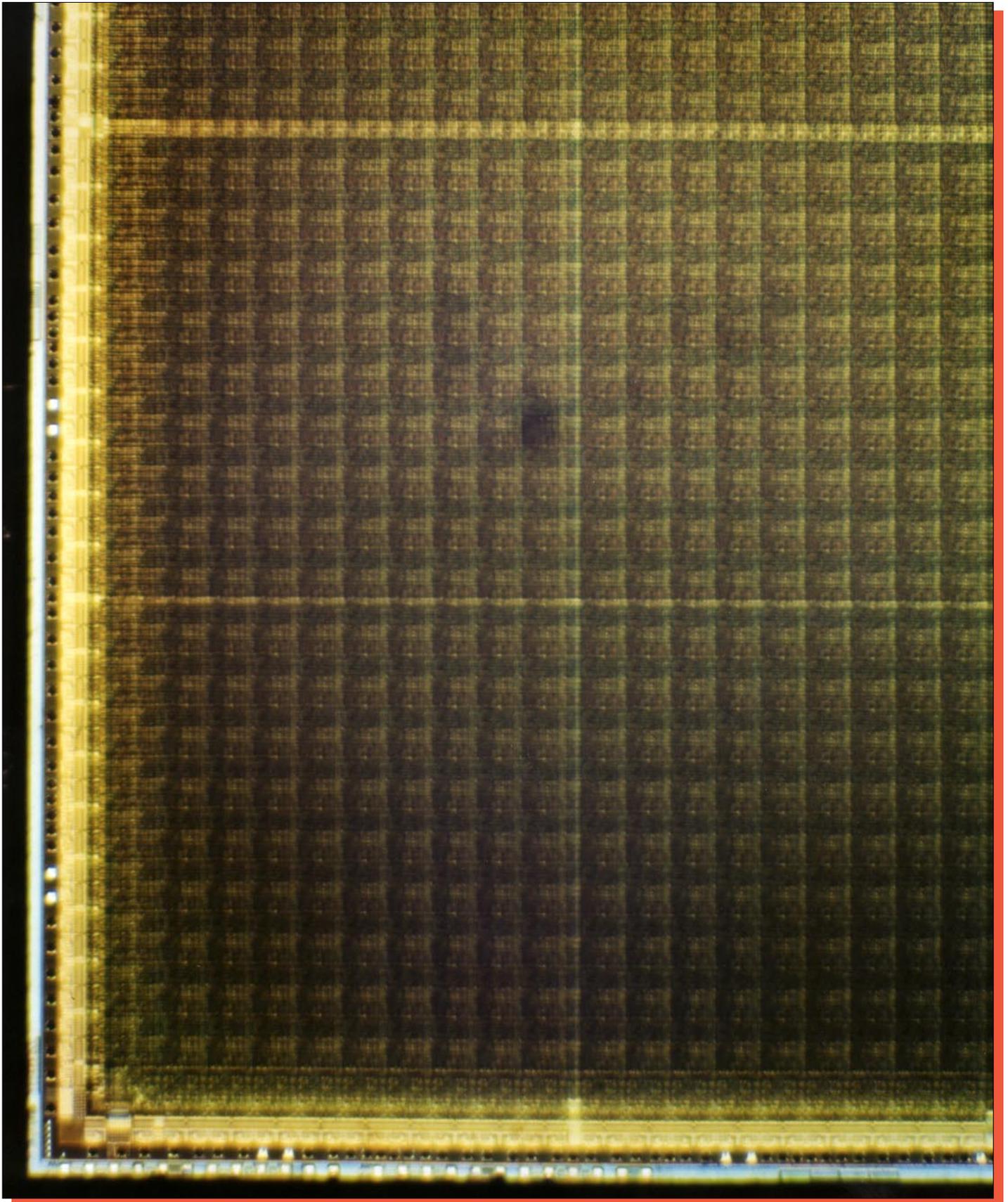


Figure 1a. Portion of the whole die photograph of the Xilinx XC4036EX. Mag. 10x.

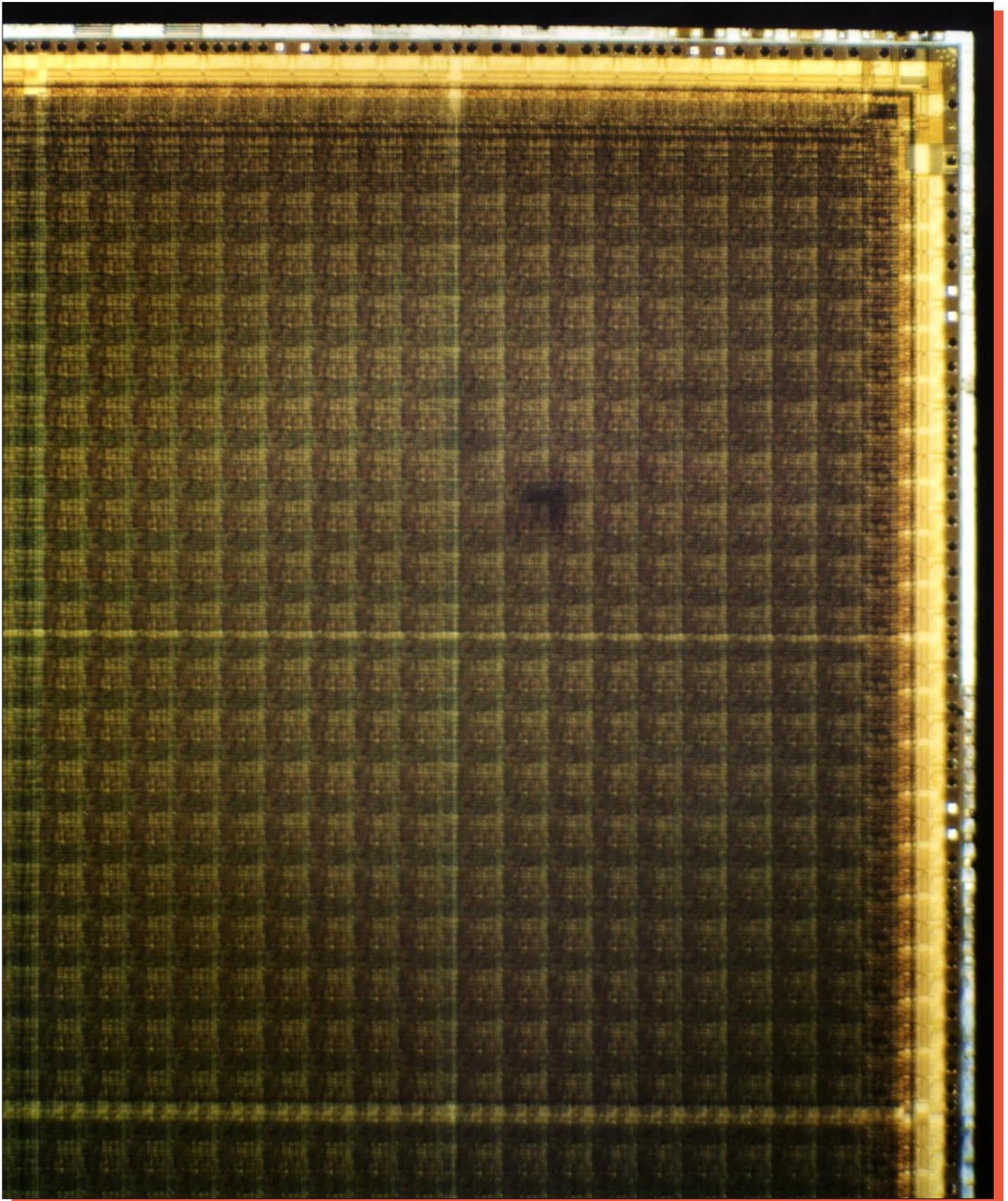


Figure 1b. Portion of the whole die photograph of the Xilinx XC4036EX. Mag. 10x.

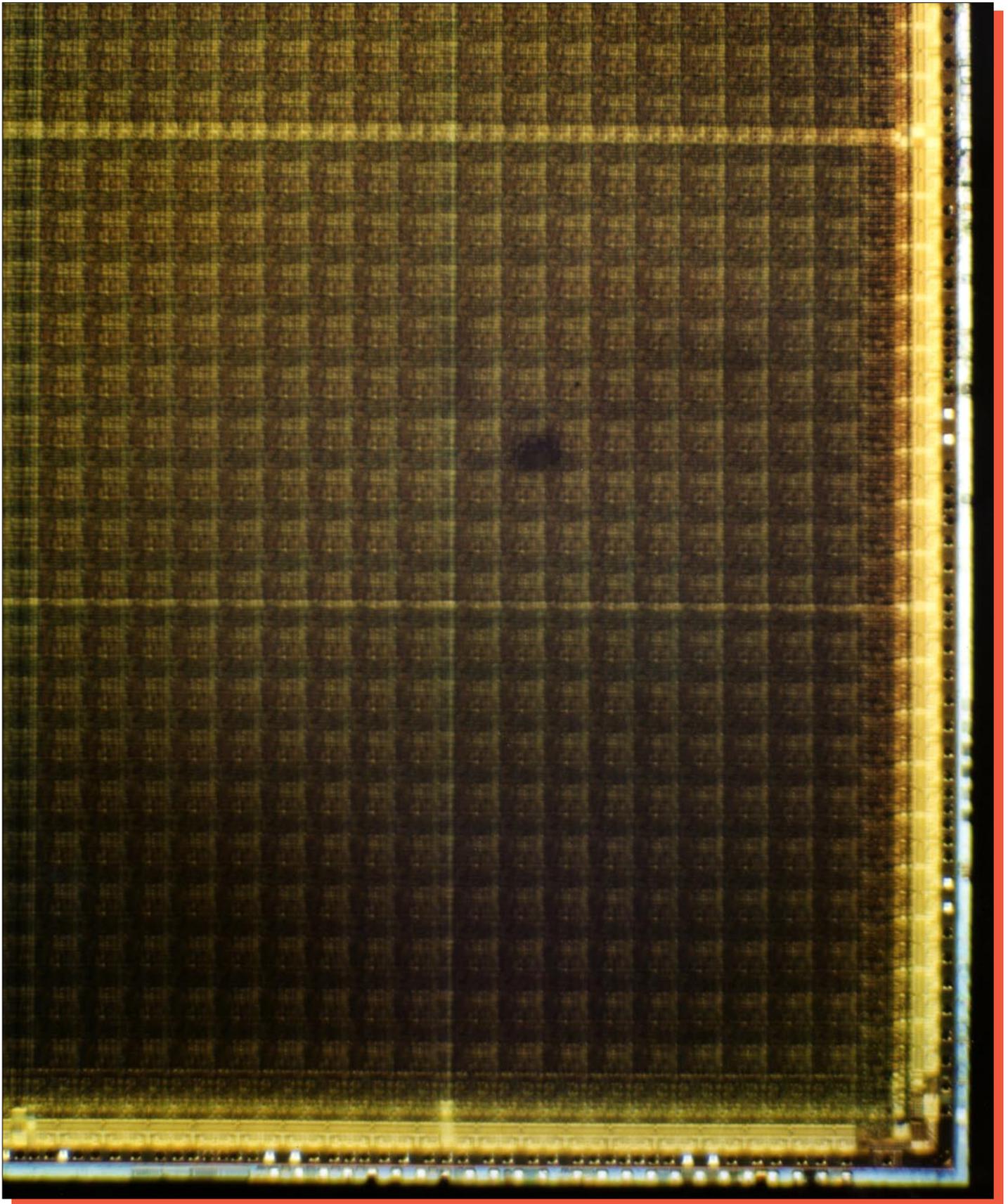
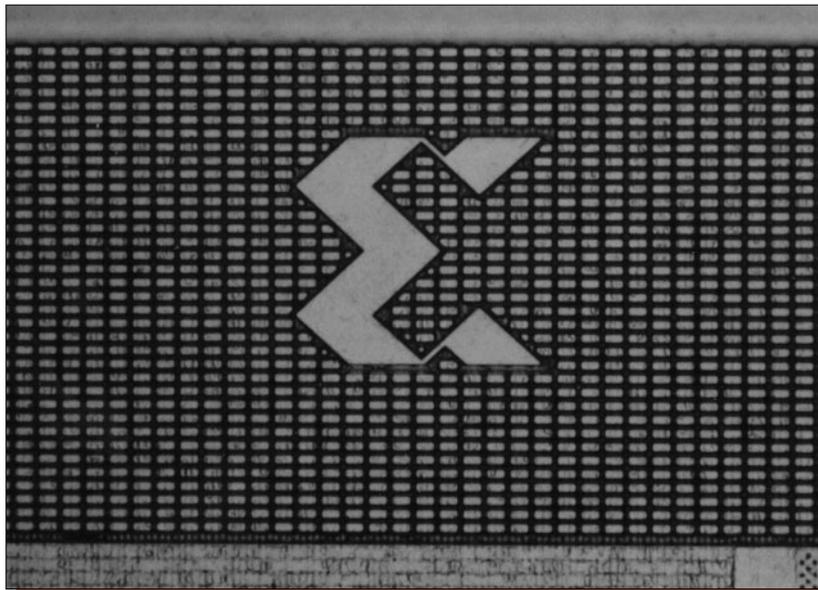


Figure 1c. Remaining portion of the whole die photograph of the Xilinx XC4036EX.
Mag. 10x.



Mag. 200x



Mag. 500x



Mag. 500x

Figure 2. Markings from the die surface.

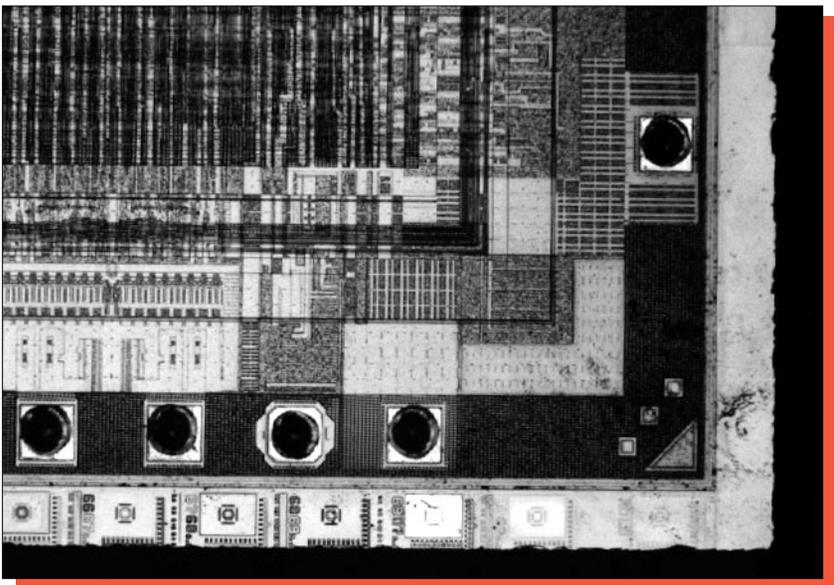
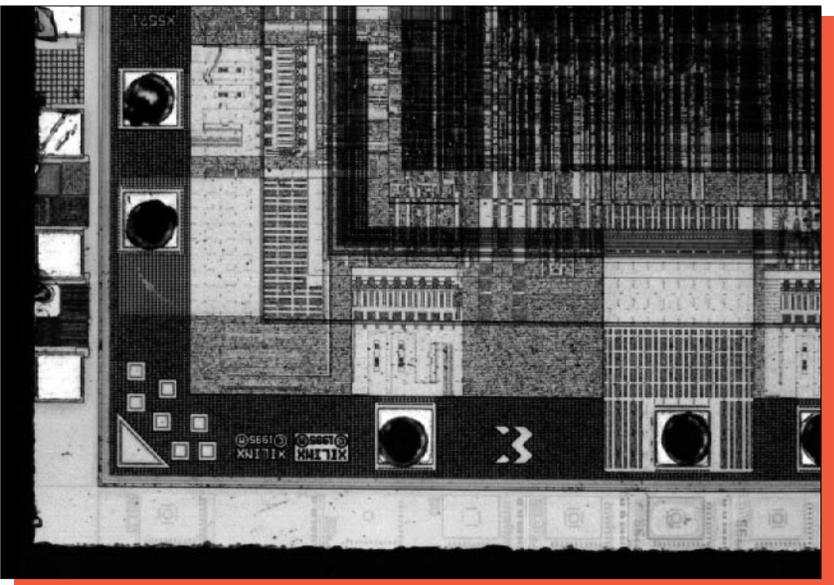
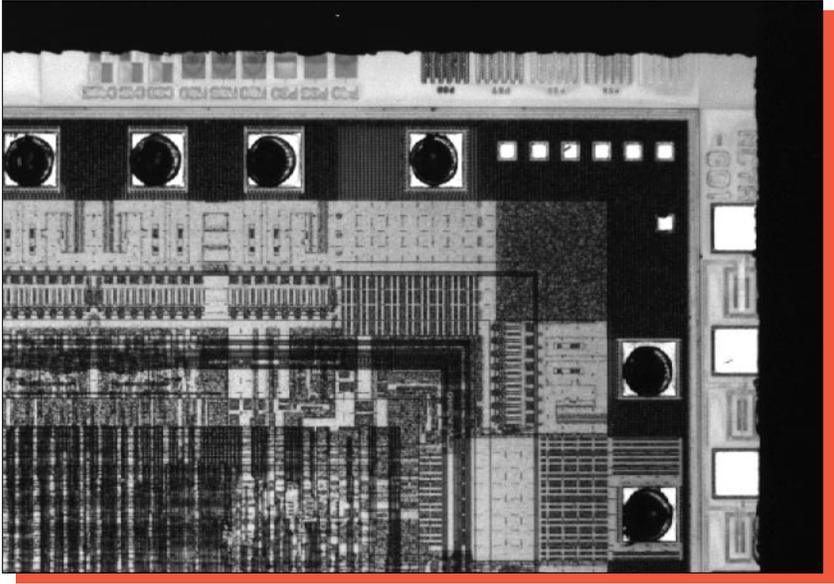
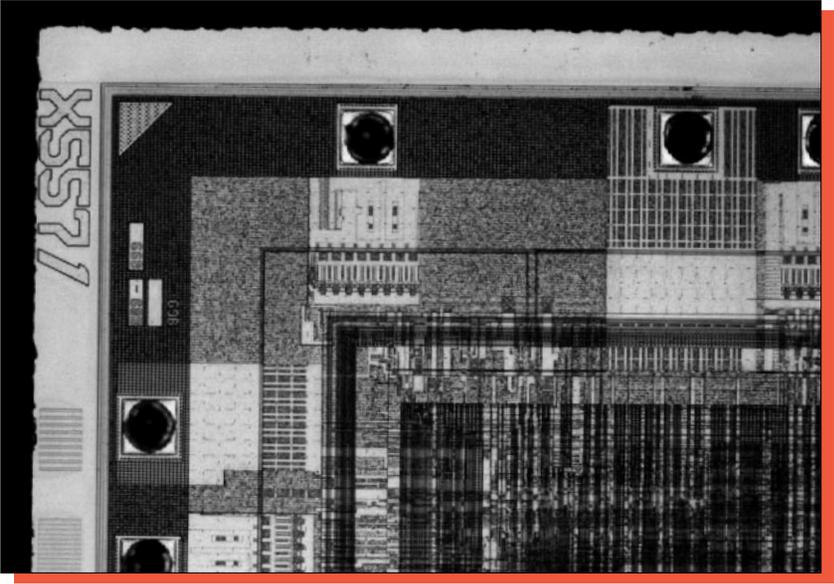
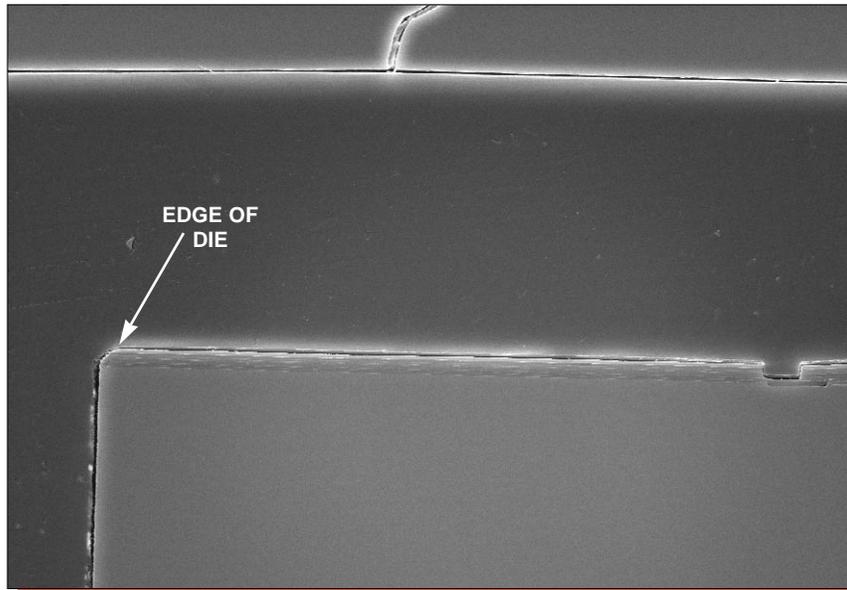
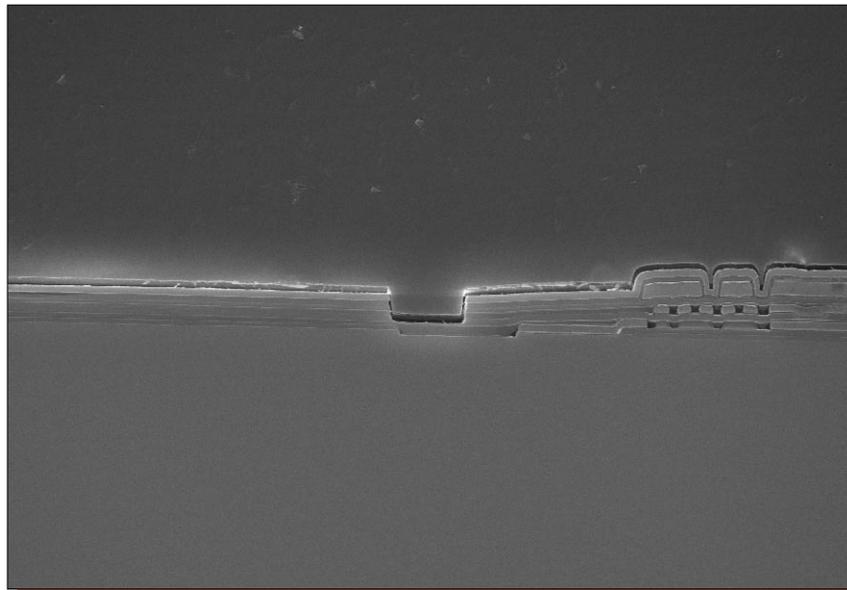


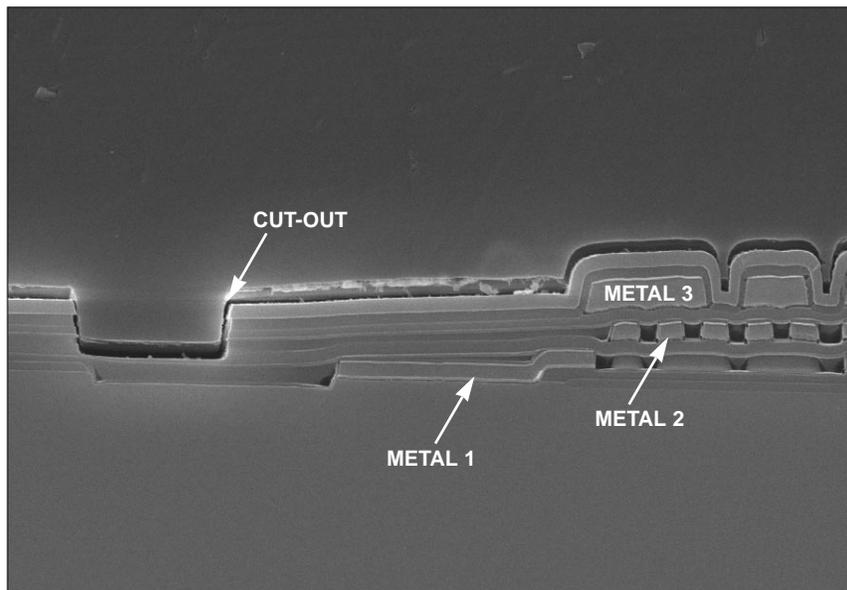
Figure 3. Optical views of the die corners. Mag. 80x.



Mag. 810x

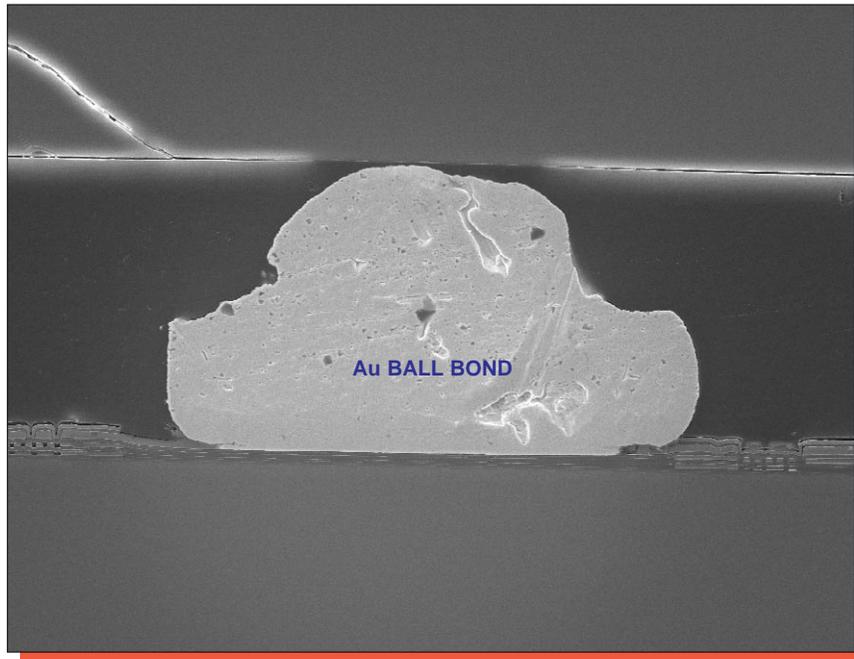


Mag. 1600x

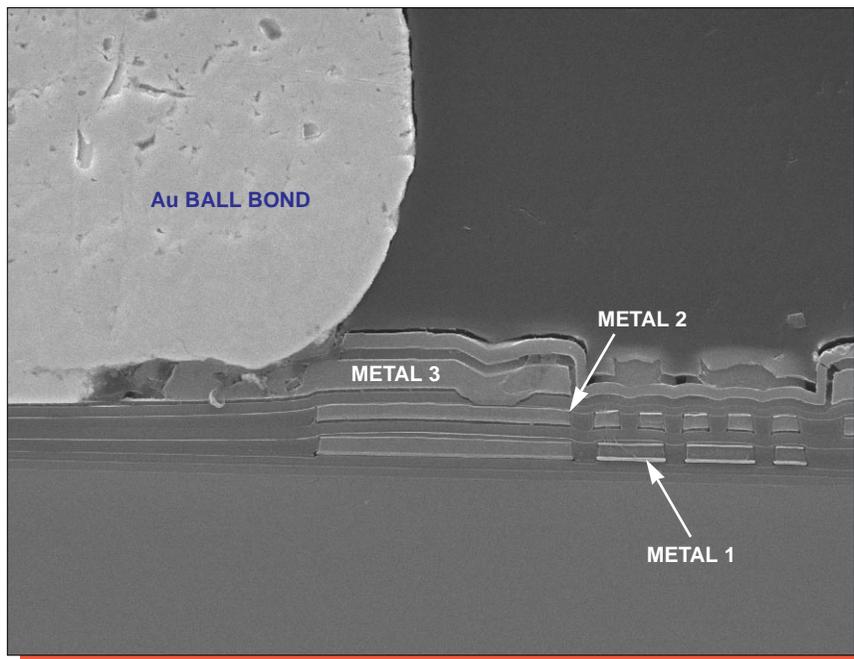


Mag. 3200x

Figure 4. SEM section views of the edge seal.



Mag. 810x



Mag. 3200x

Figure 5. SEM section views of the bond pad structure.

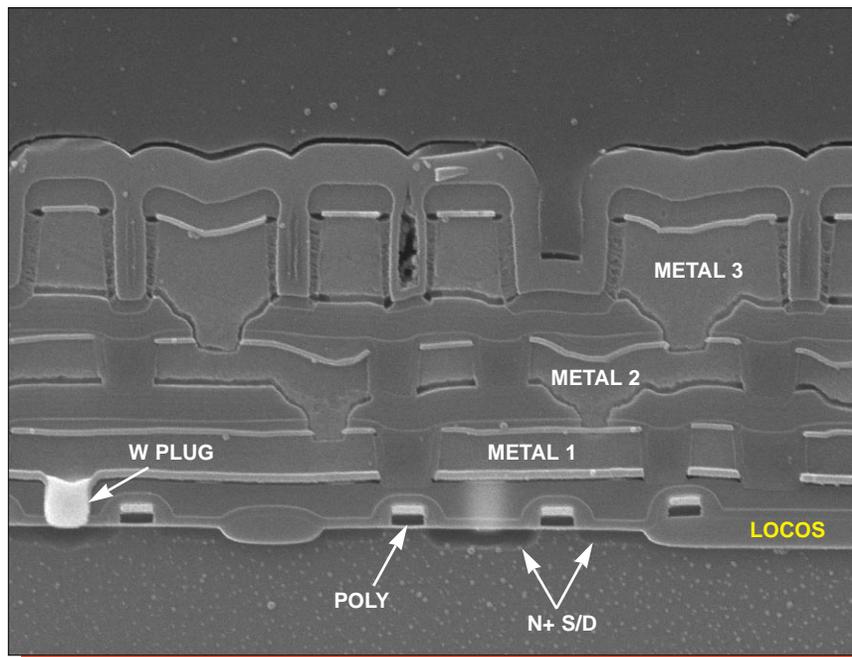
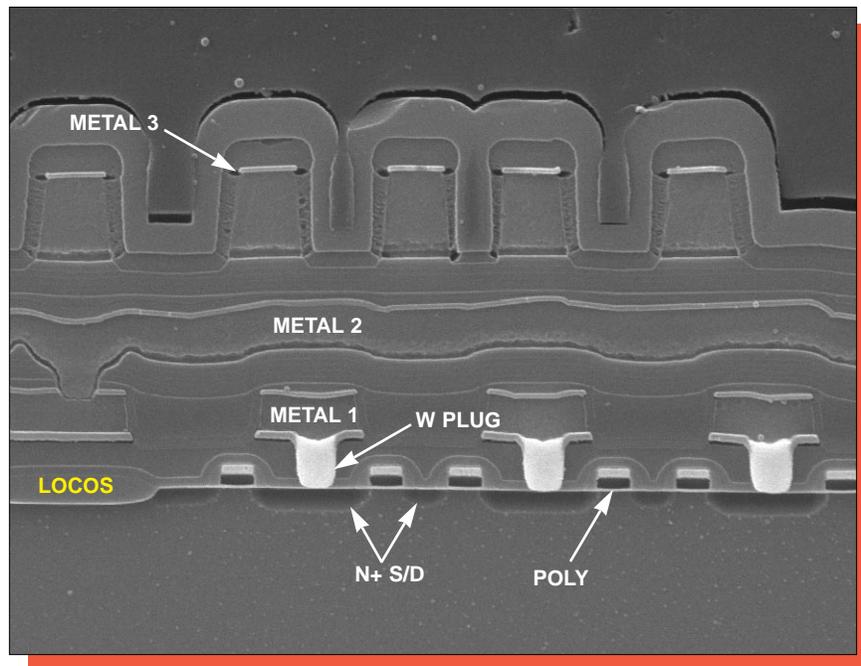
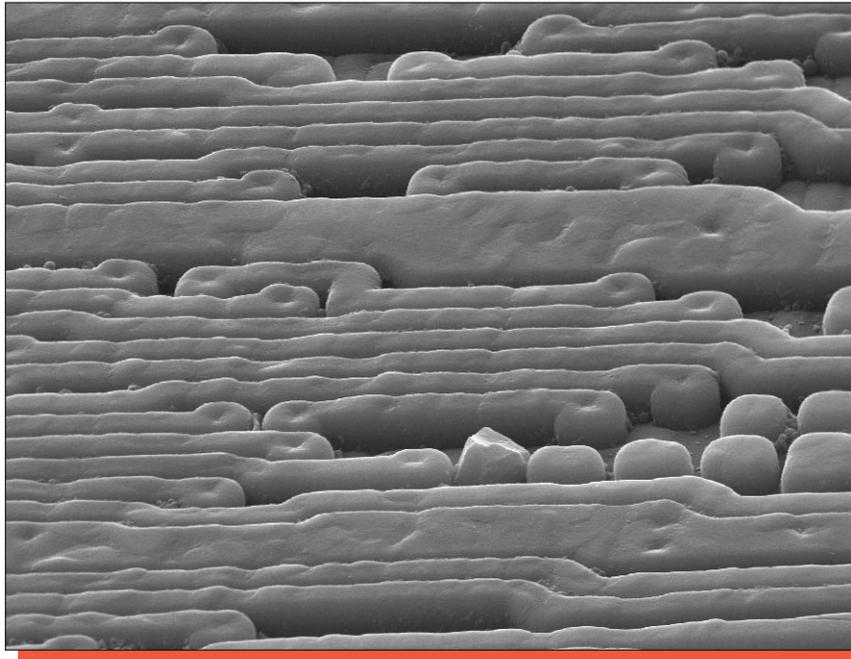
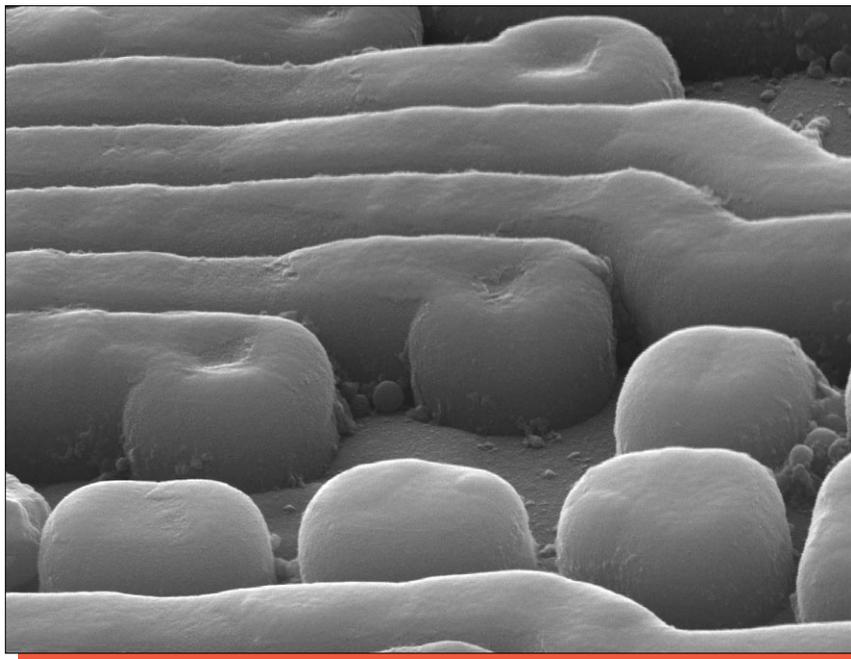


Figure 6. SEM section views of general structure (silicon etch). Mag. 10,000x.

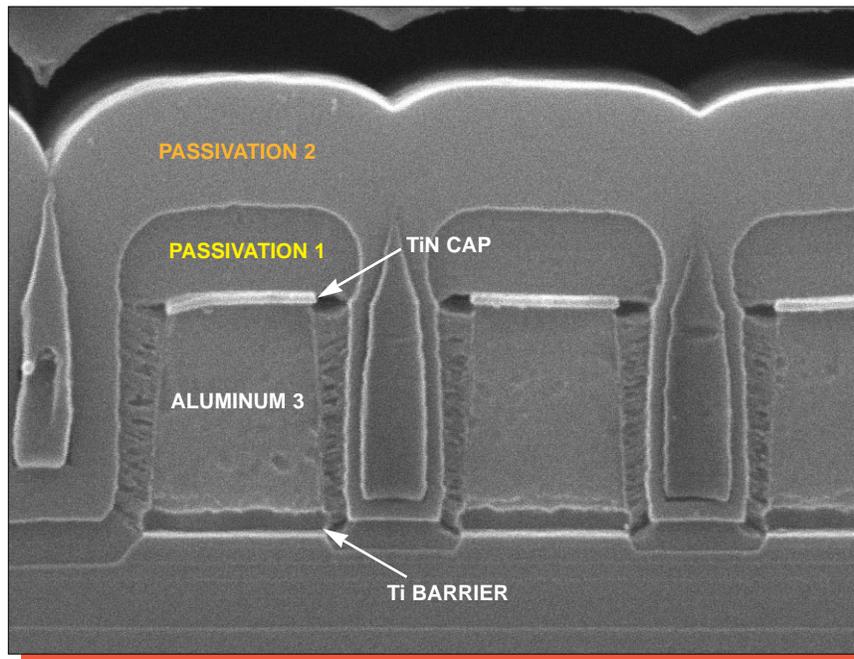


Mag. 3200x

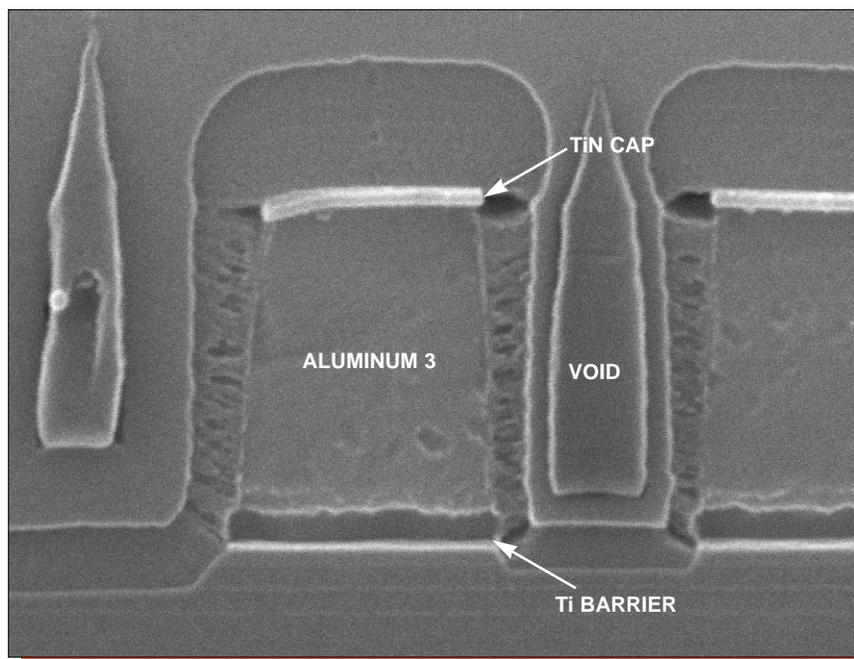


Mag. 10,000x

Figure 7. Perspective SEM views of the overlay passivation coverage. 60°.

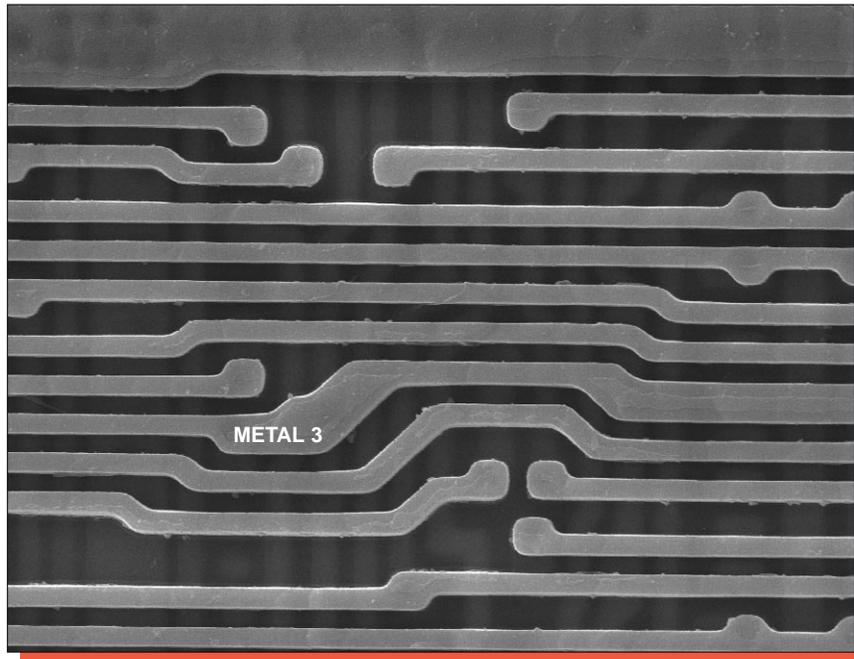


Mag. 26,000x

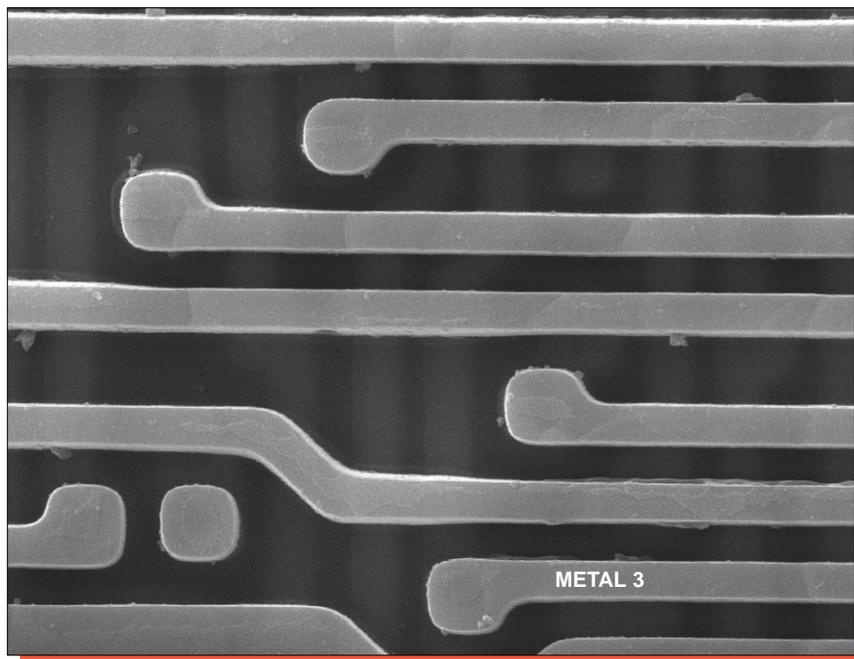


Mag. 40,000x

Figure 8. SEM section views of metal 3 line profiles.

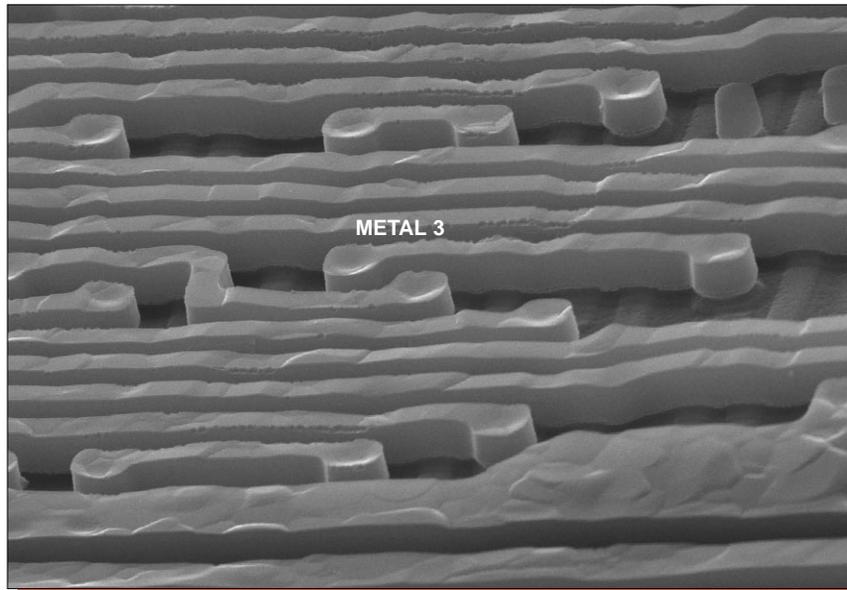


Mag. 3200x

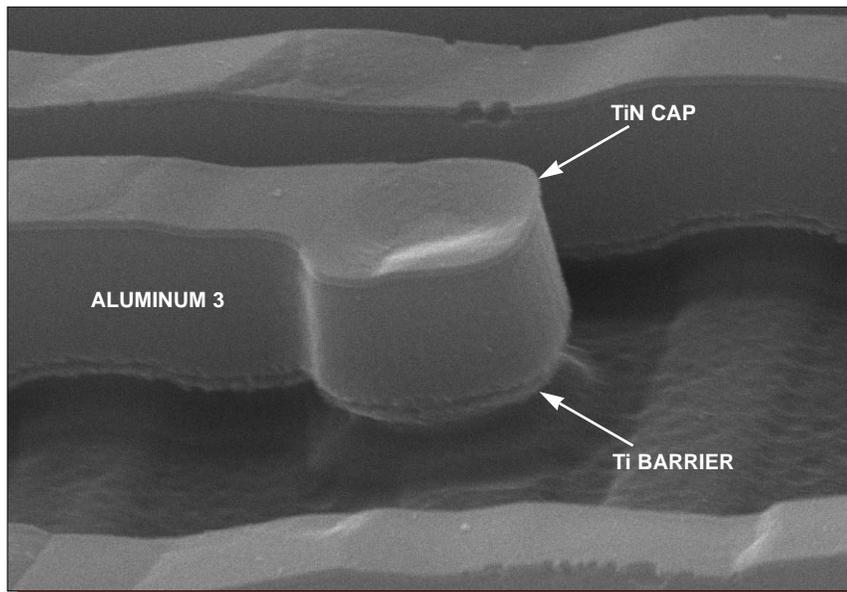


Mag. 6500x

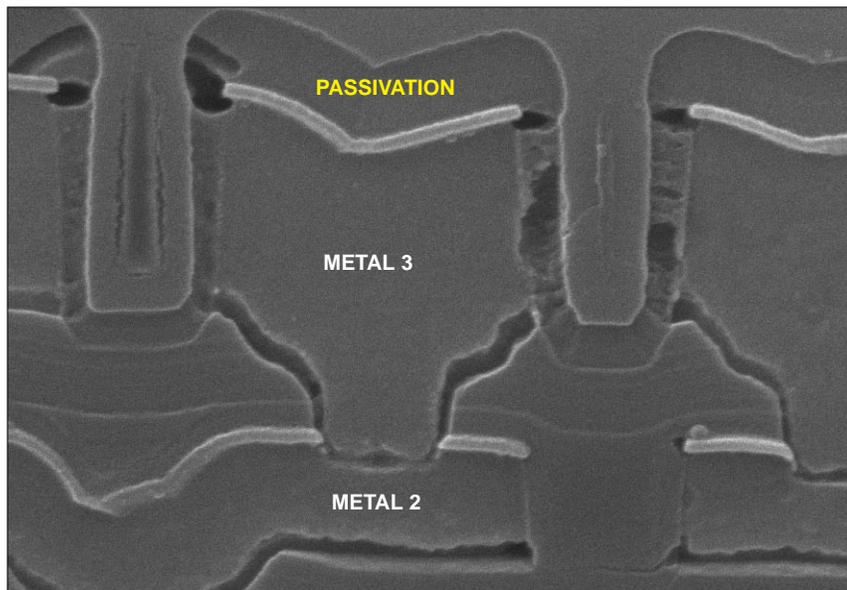
Figure 9. Topological SEM views of metal 3 patterning. 0°.



Mag. 5000x

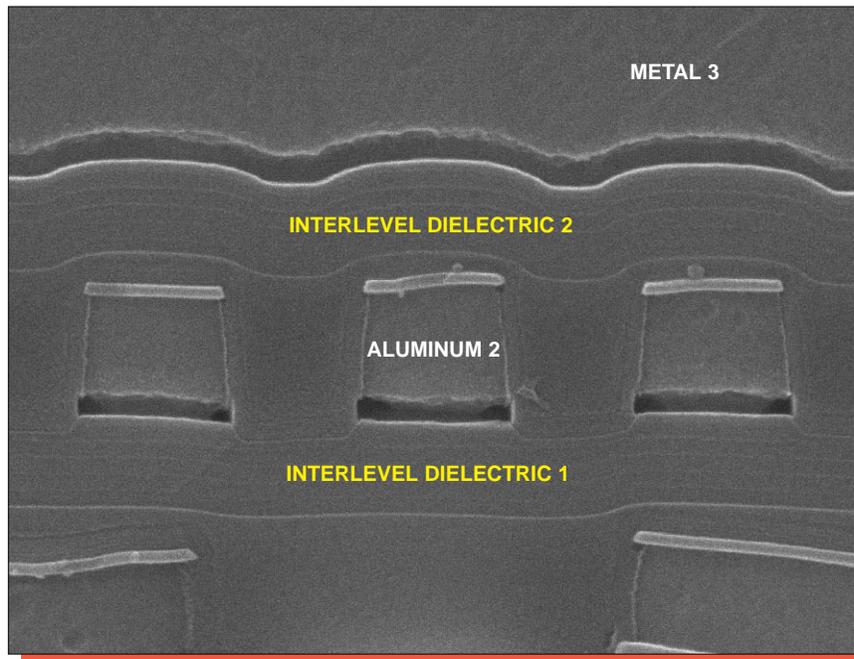


Mag. 20,000x

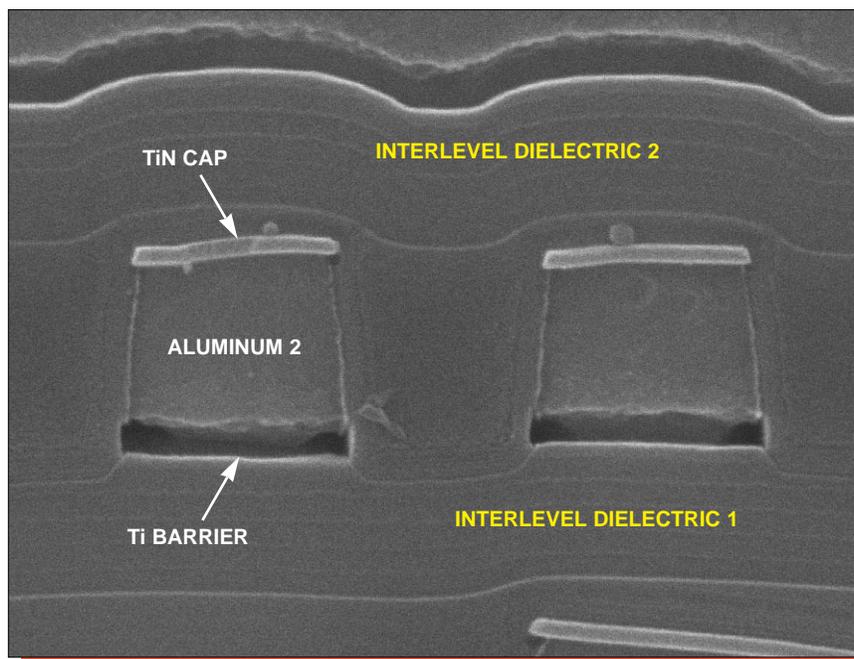


Mag. 26,000x

Figure 10. SEM views of metal 3 coverage and via.

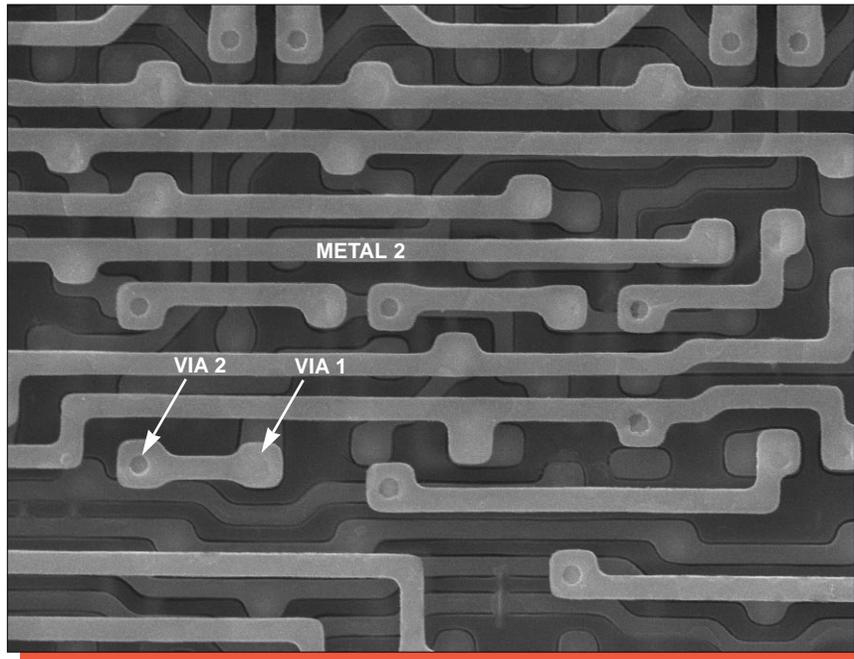


Mag. 26,000x

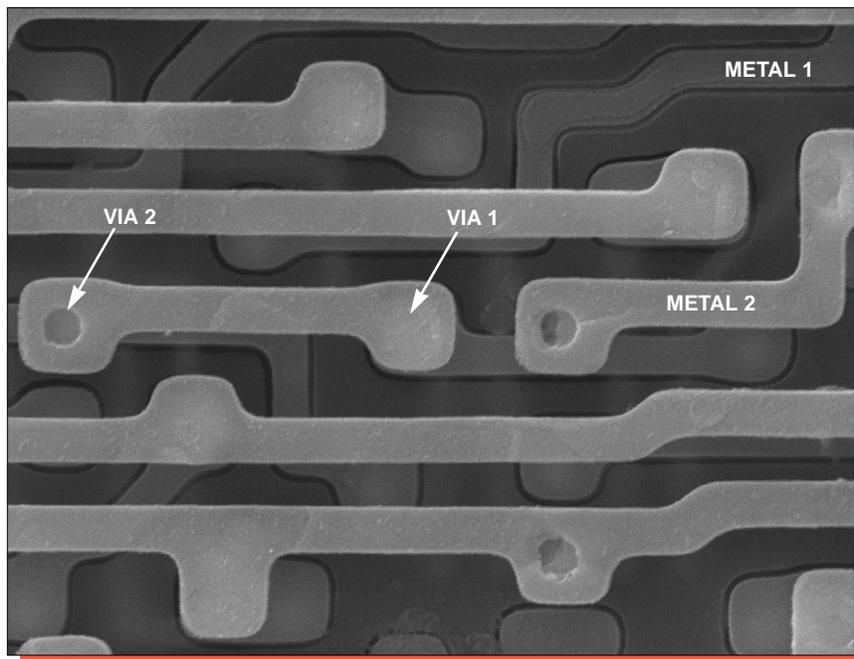


Mag. 40,000x

Figure 11. SEM section views of metal 2 line profiles.

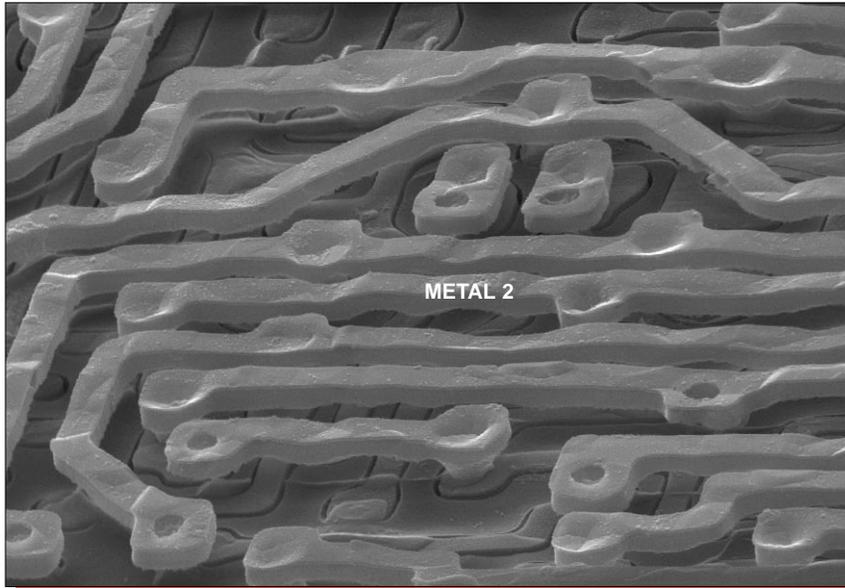


Mag. 4000x

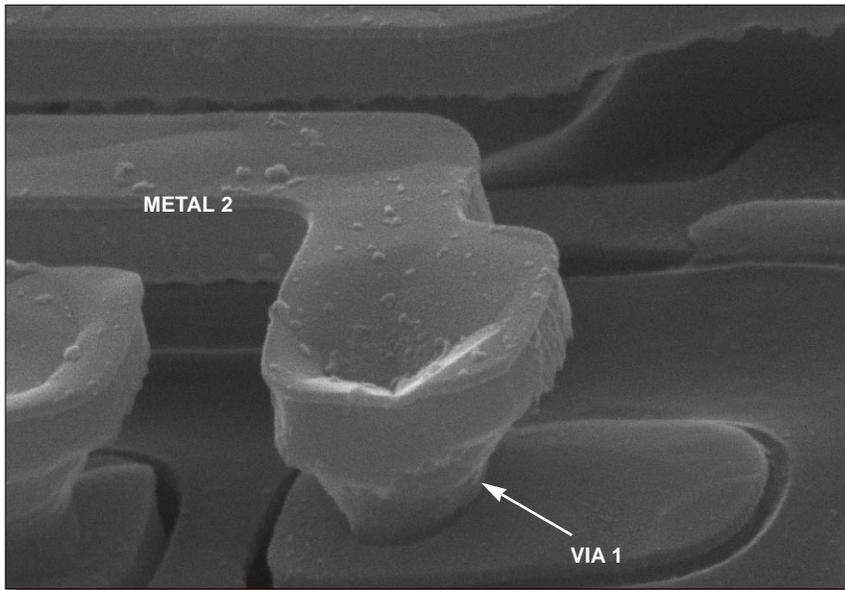


Mag. 8100x

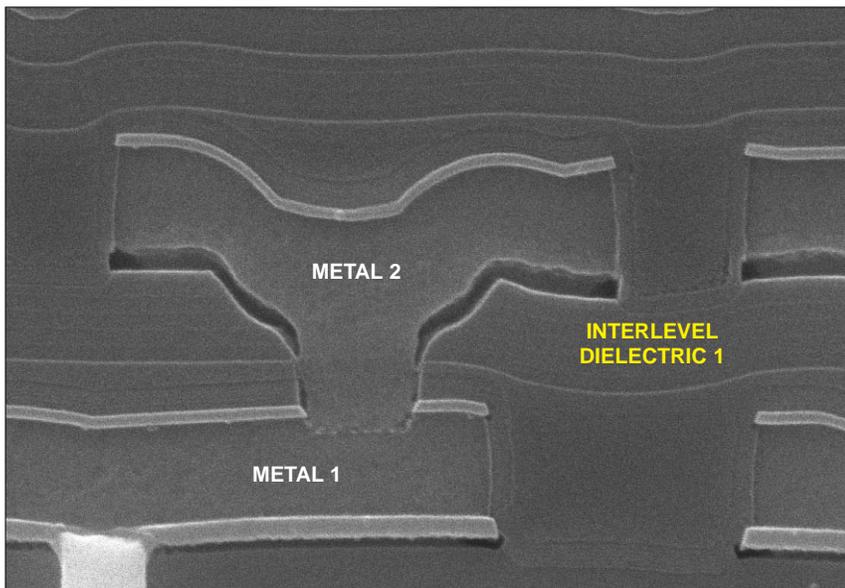
Figure 12. Topological SEM views of metal 2 patterning. 0°.



Mag. 6500x, 60°

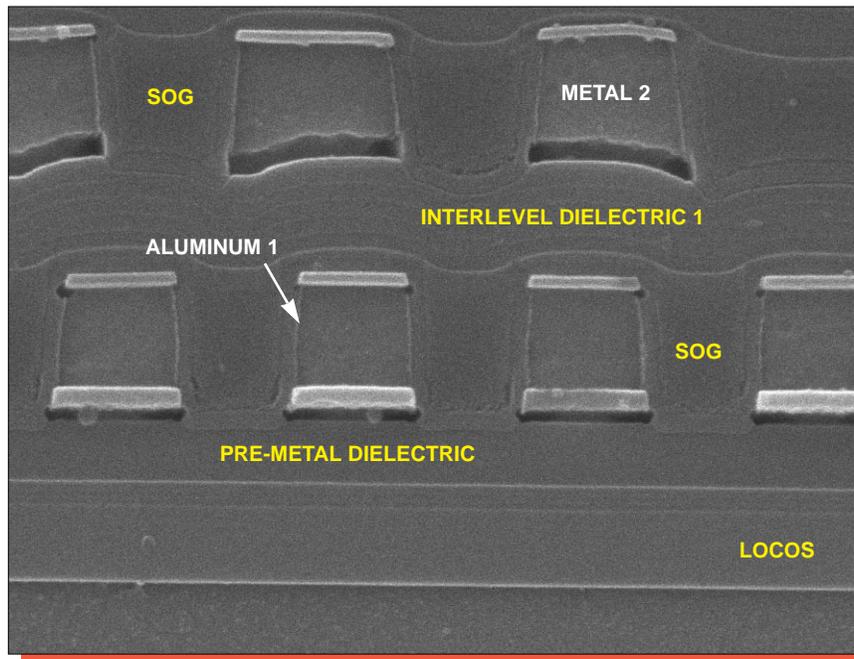


Mag. 26,000x, 60°

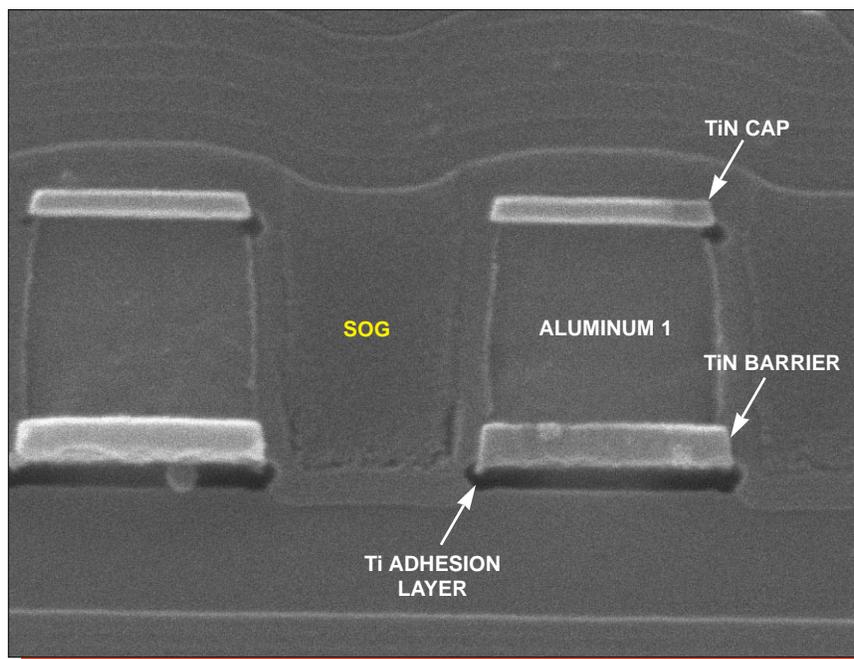


Mag. 26,000x

Figure 13. SEM views of metal 2 coverage and via.

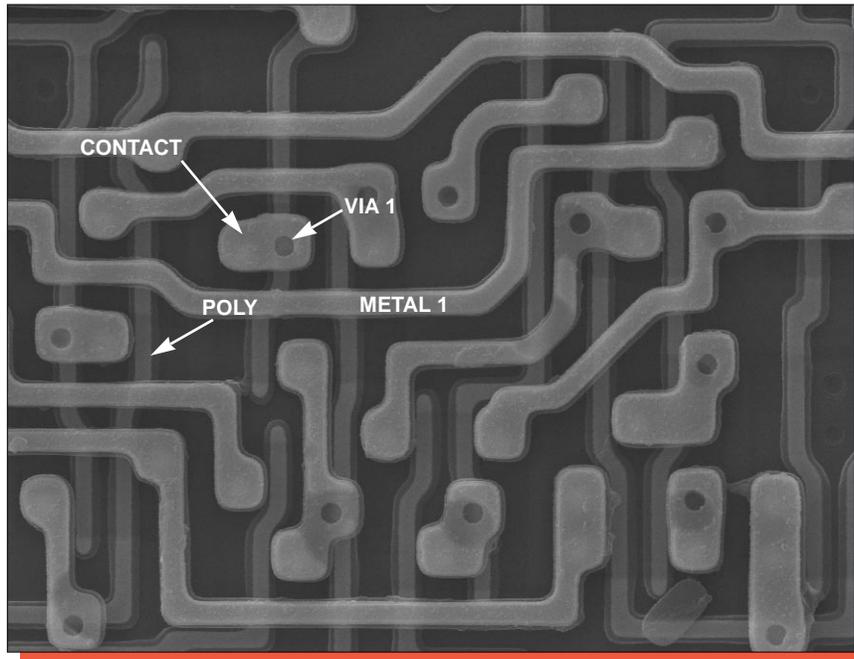


Mag. 26,000x

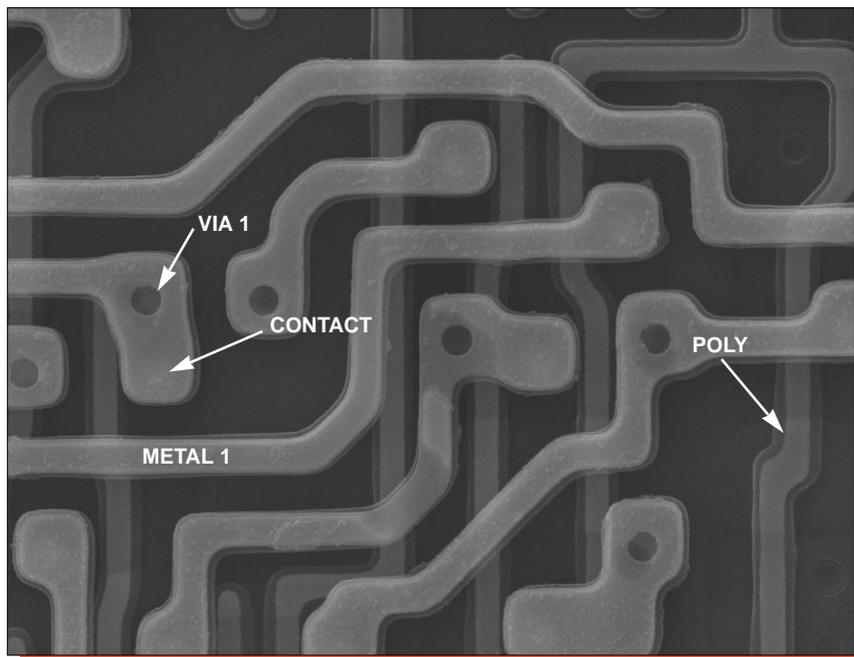


Mag. 52,000x

Figure 14. SEM section views of metal 1 line profiles.

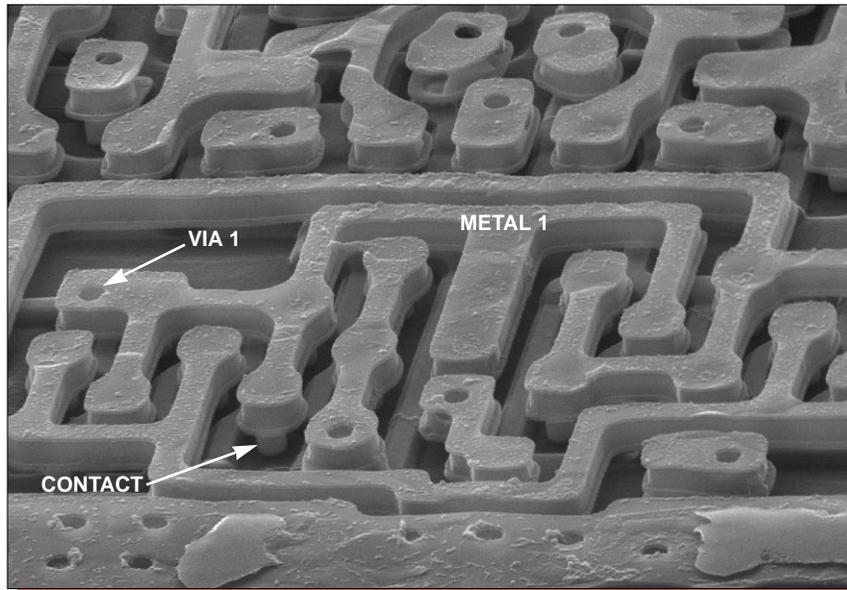


Mag. 5000x

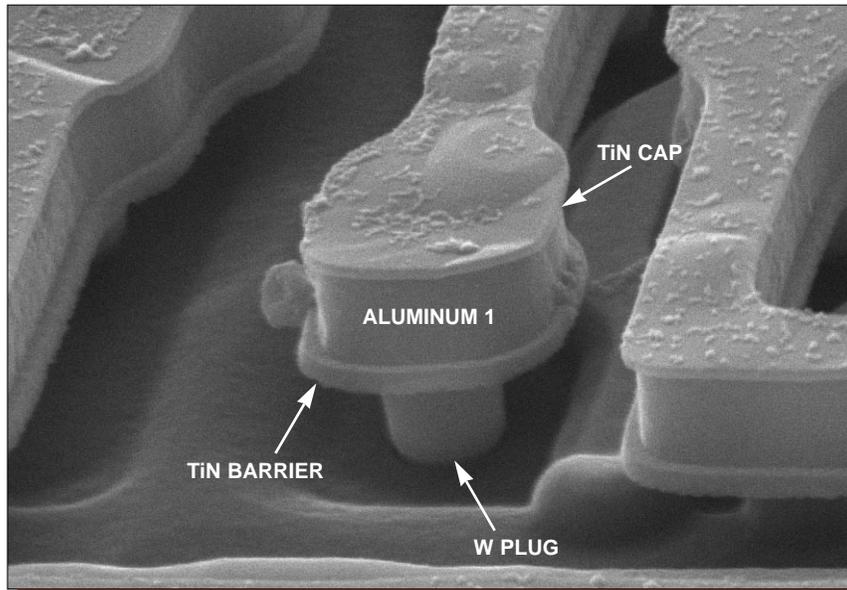


Mag. 7400x

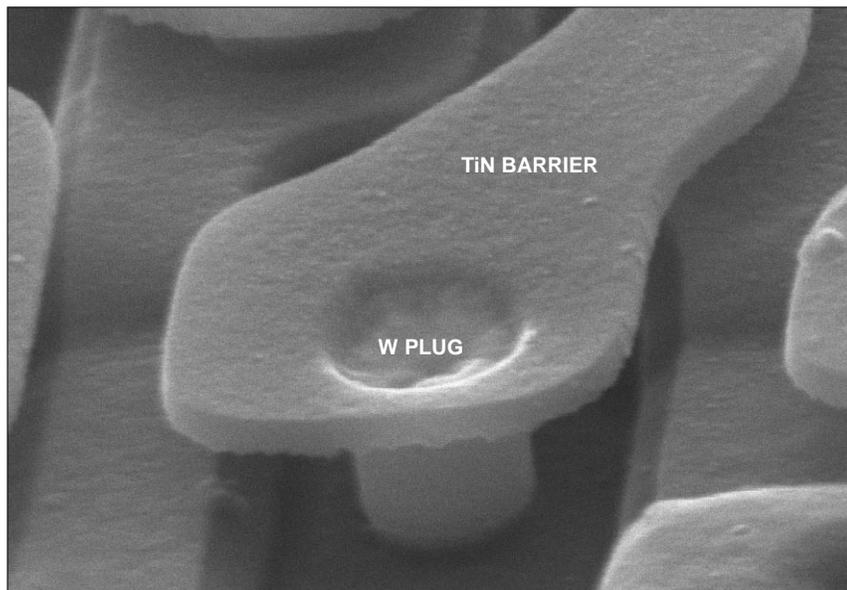
Figure 15. Topological SEM views of metal 1 patterning. 0°.



Mag. 6500x

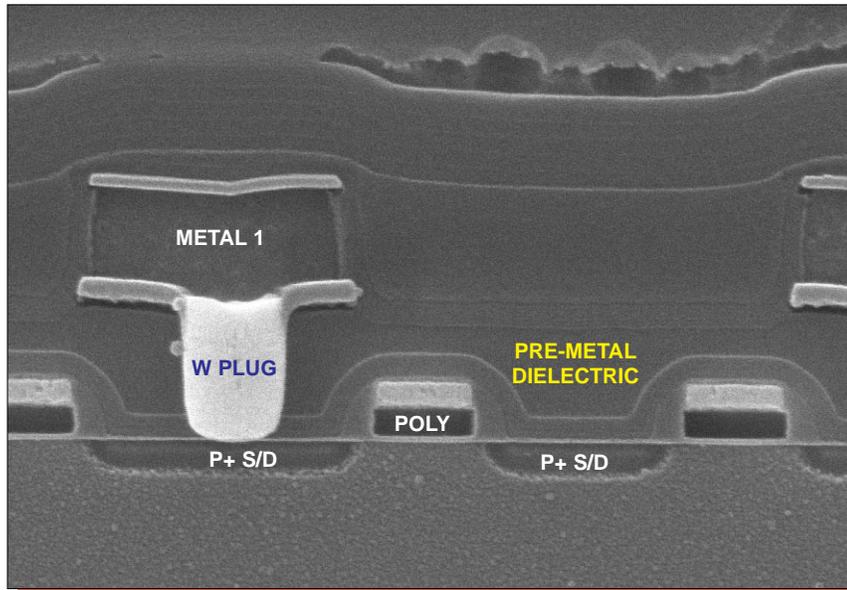


Mag. 26,000x

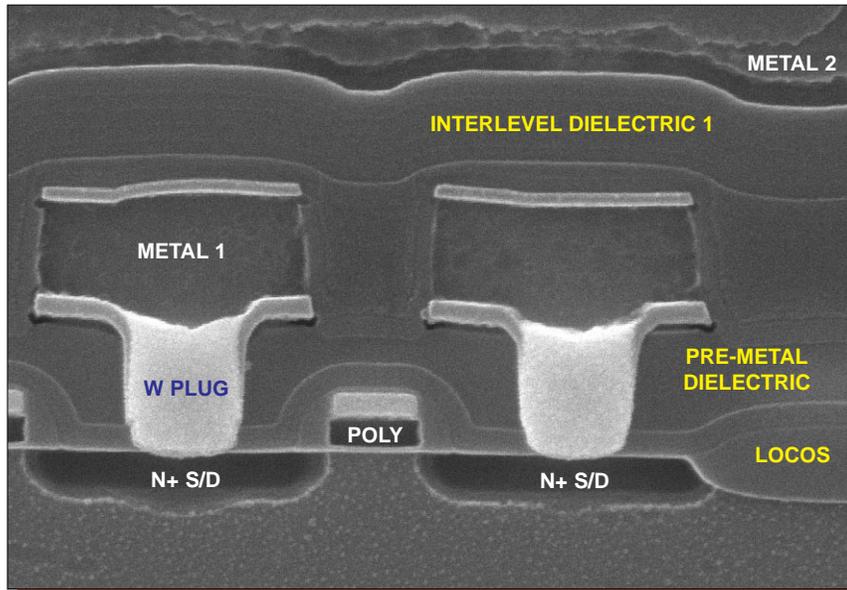


Mag. 40,000x

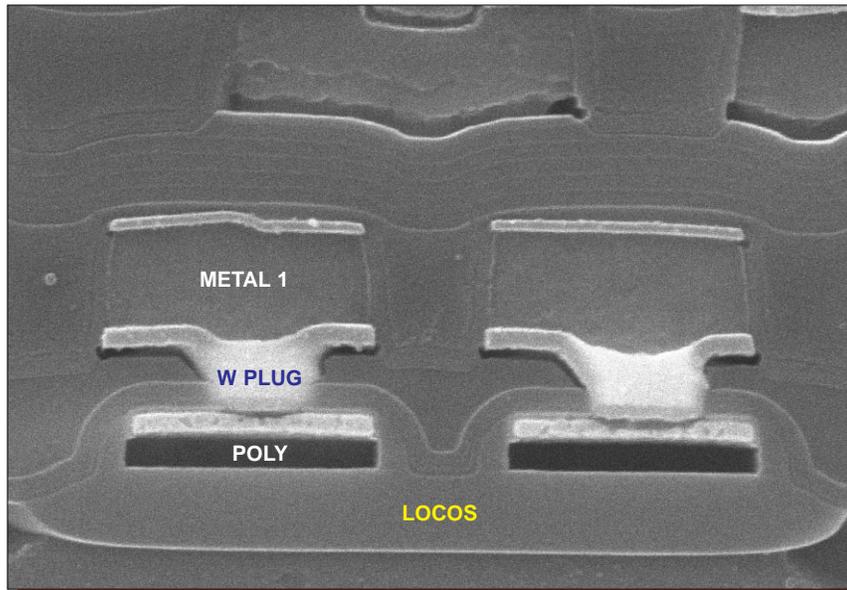
Figure 16. Perspective SEM views of metal 1 coverage and barrier. 60°.



metal 1-to-P+

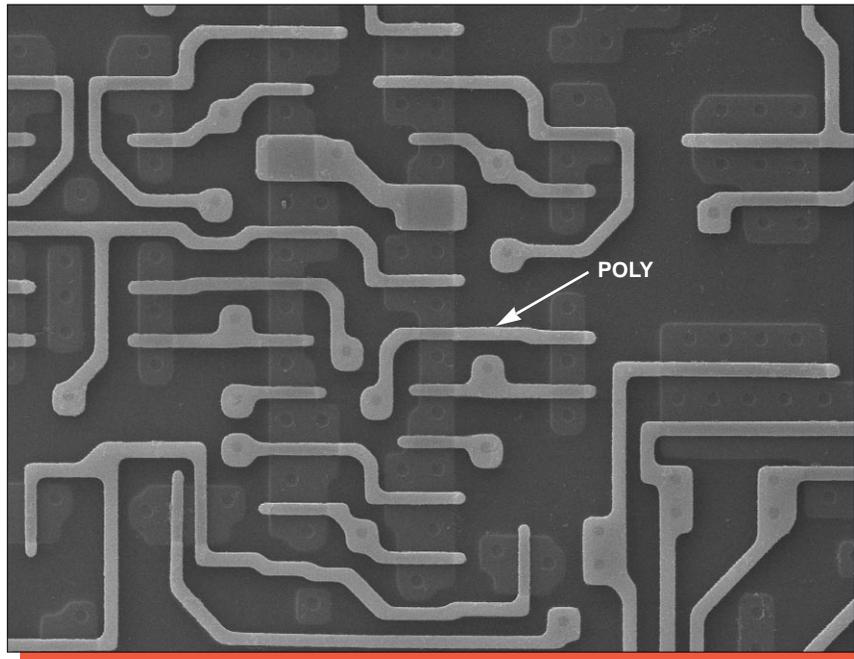


metal 1-to-N+

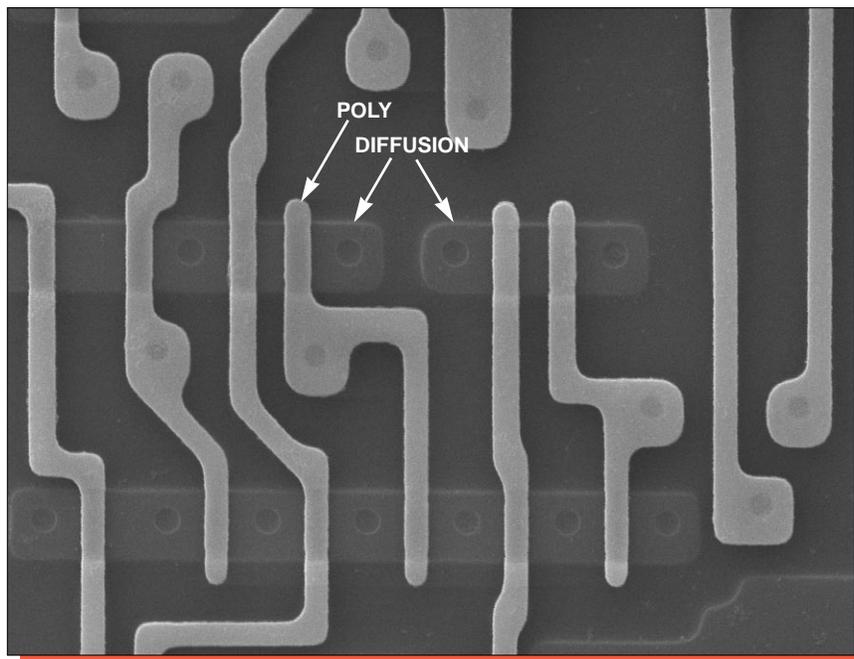


metal 1-to-poly

Figure 17. SEM section views of typical metal 1 contacts. Mag. 26,000x.

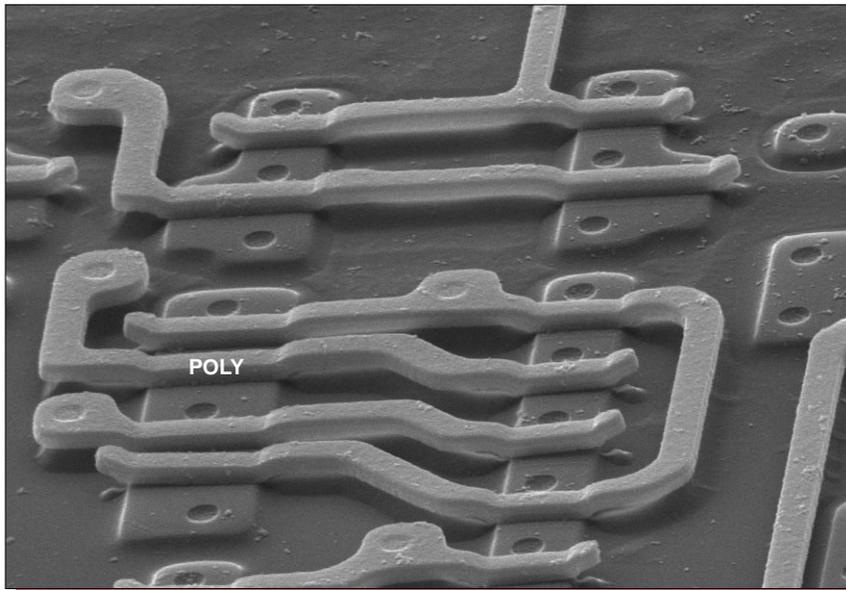


Mag. 3200x

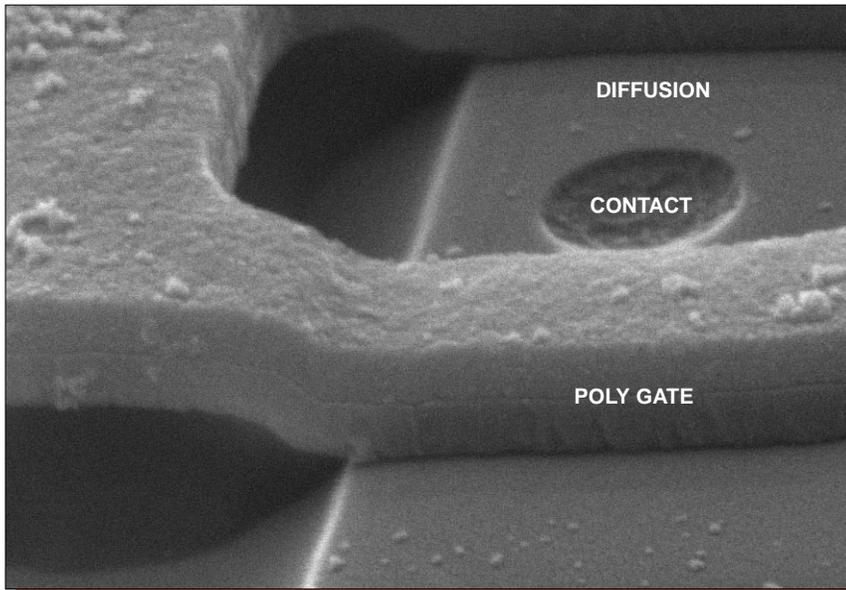


Mag. 6500x

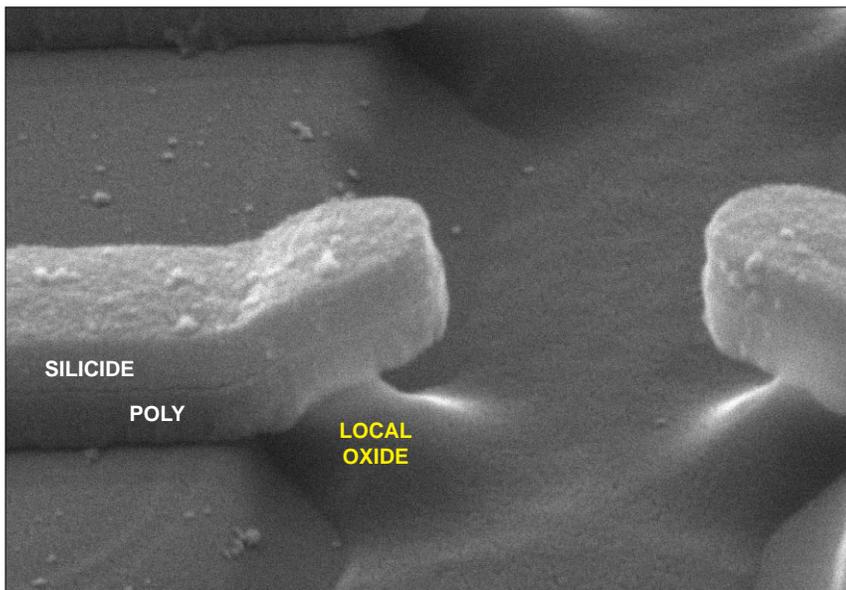
Figure 18. Topological SEM views of poly patterning. 0°.



Mag. 8800x

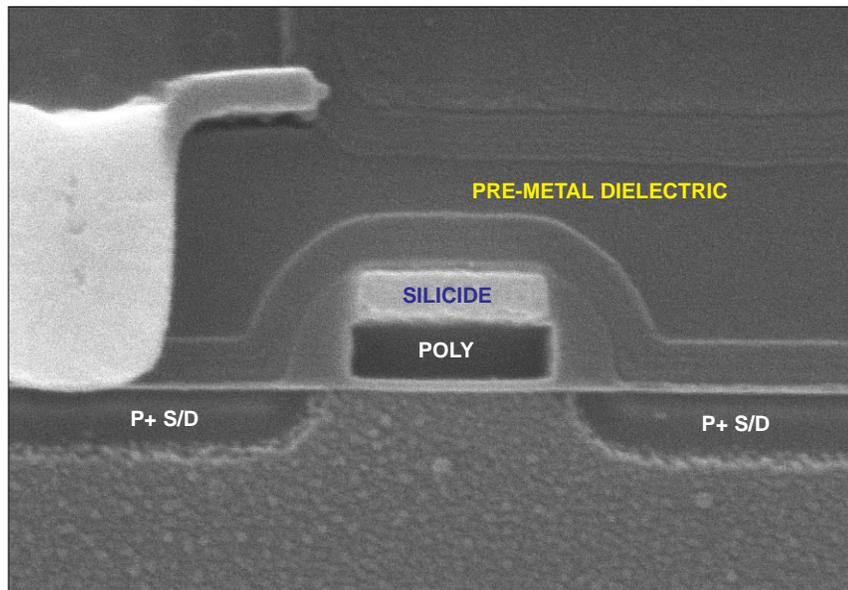


Mag. 52,000x

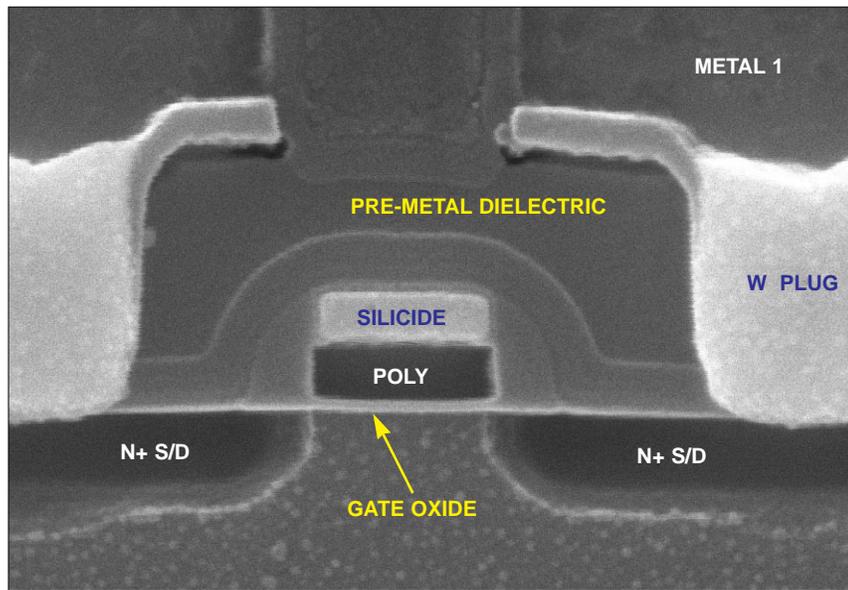


Mag. 52,000x

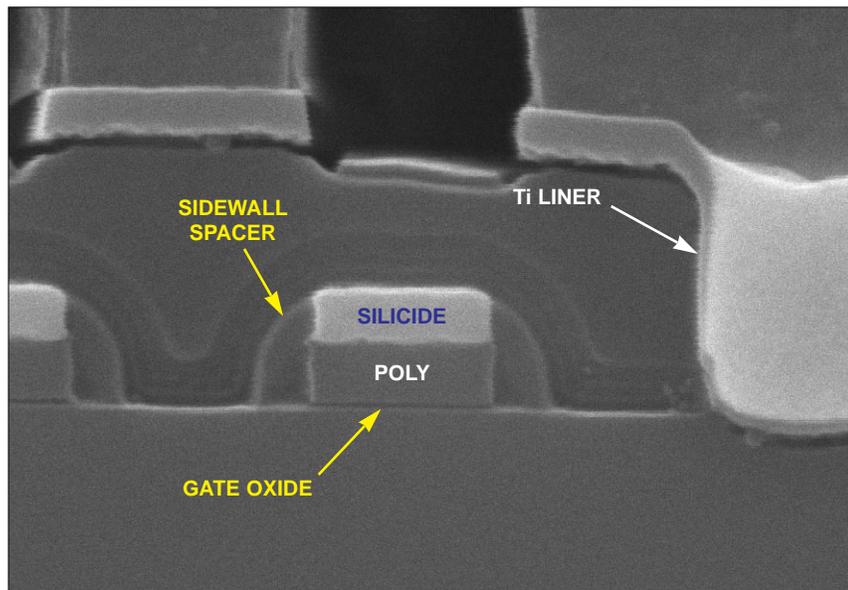
Figure 19. Perspective SEM views of poly coverage. 60°.



P-channel,
silicon etch



N-channel,
silicon etch



glass etch

Figure 20. SEM section views of typical transistors. Mag. 52,000x.

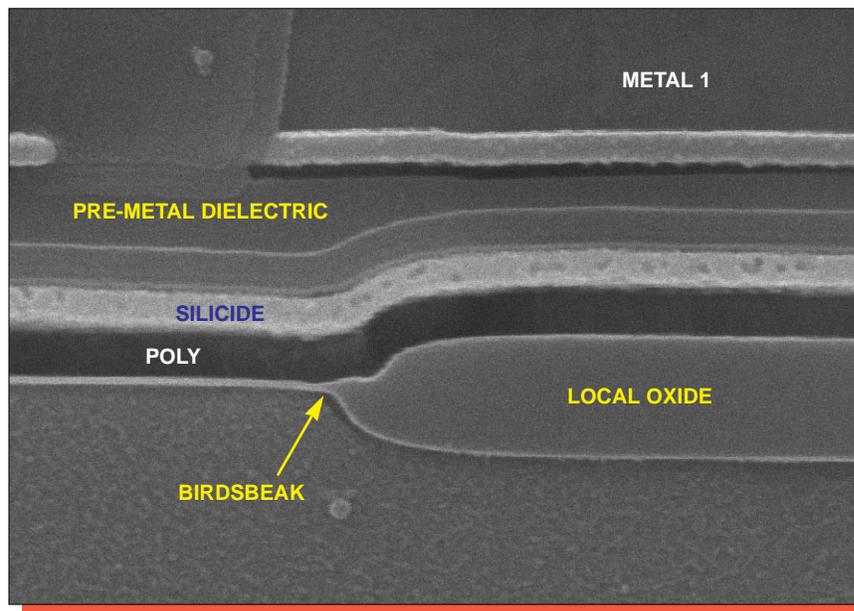


Figure 21. SEM section view of a local oxide birdsbeak. Mag. 40,000x.

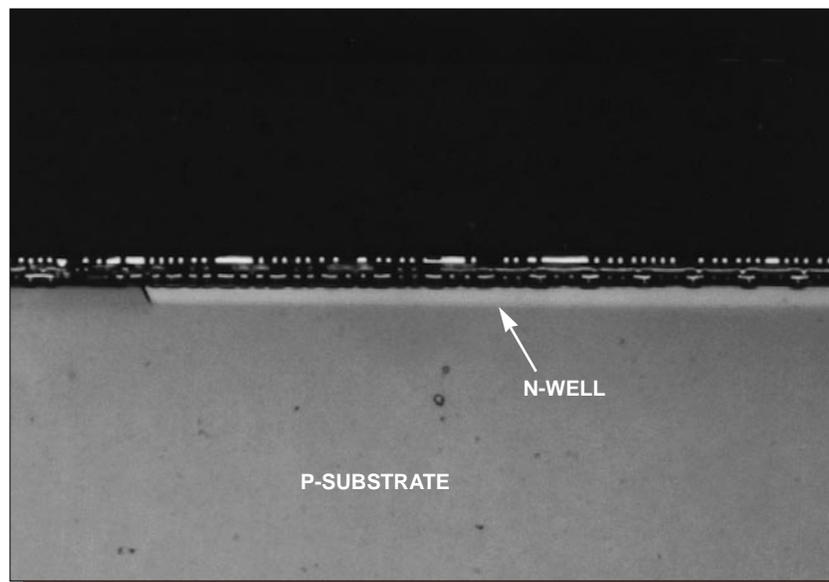
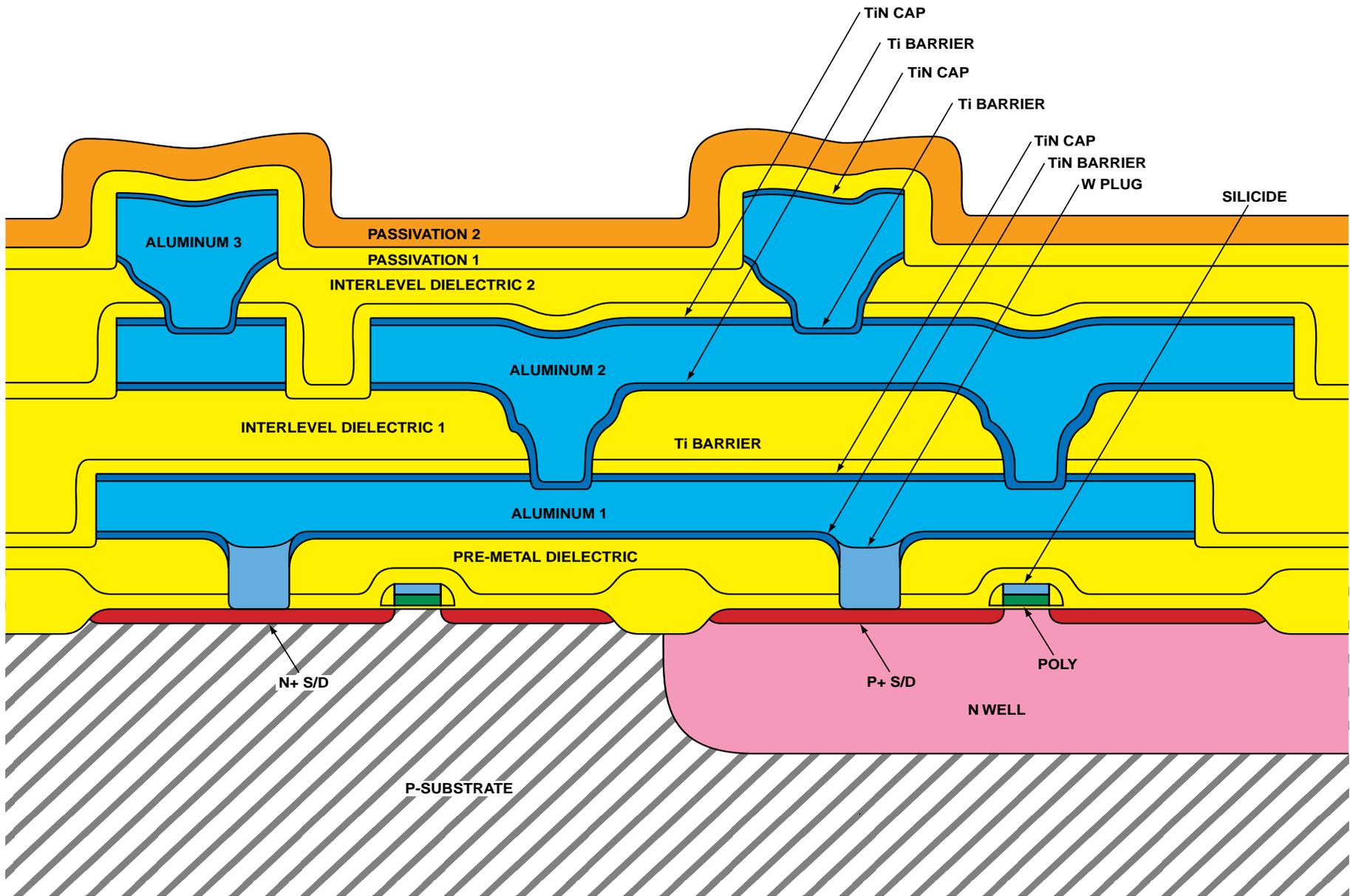
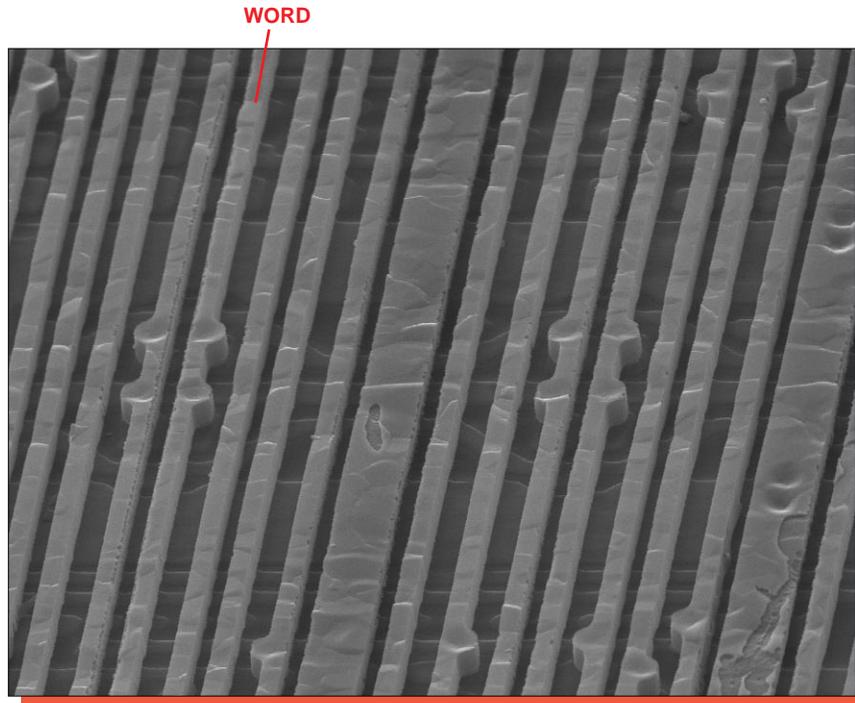


Figure 21a. Optical view of the well structure. Mag. 800x.

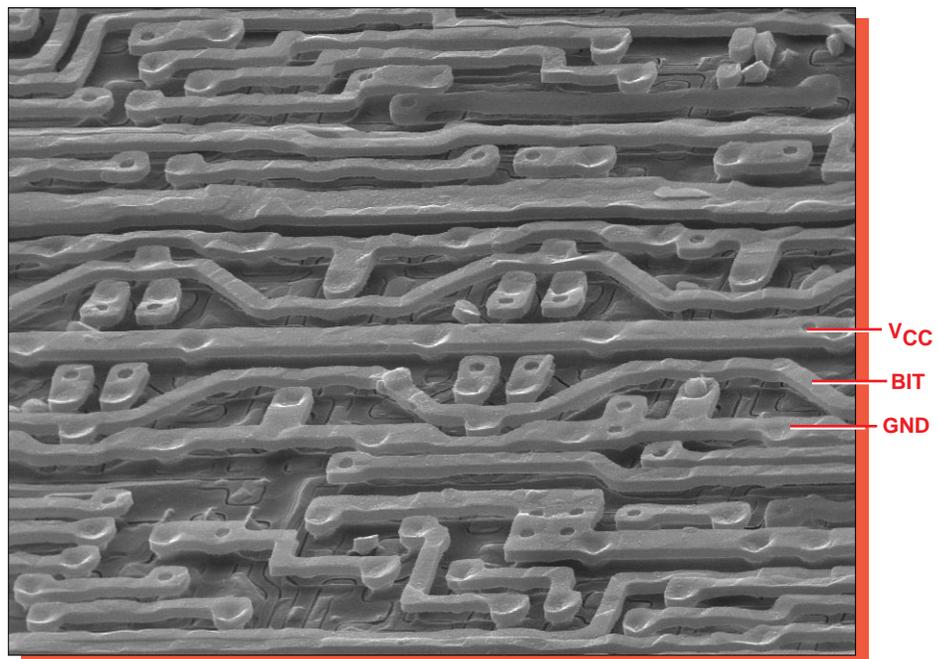


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

Figure 22. Color cross section drawing illustrating device structure.

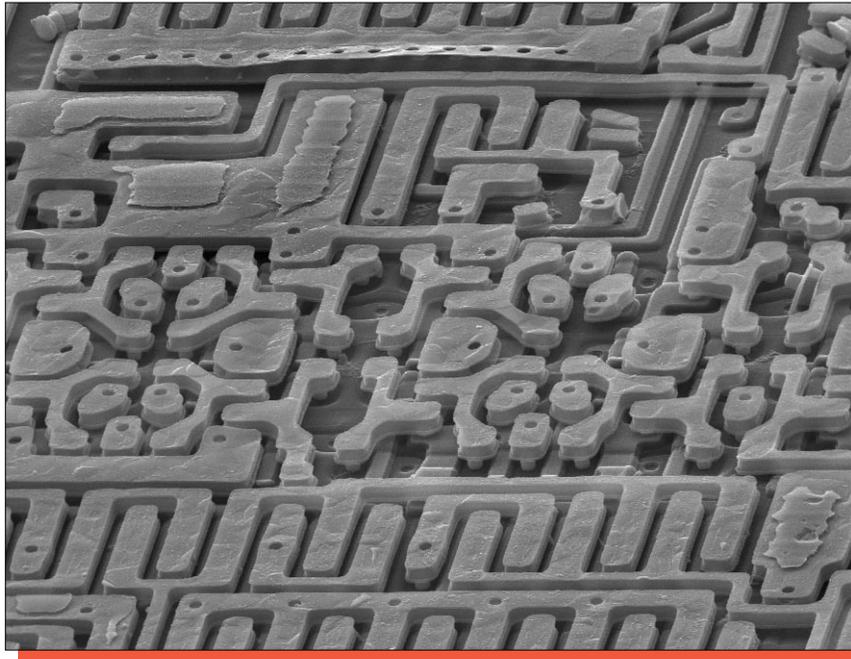


metal 3

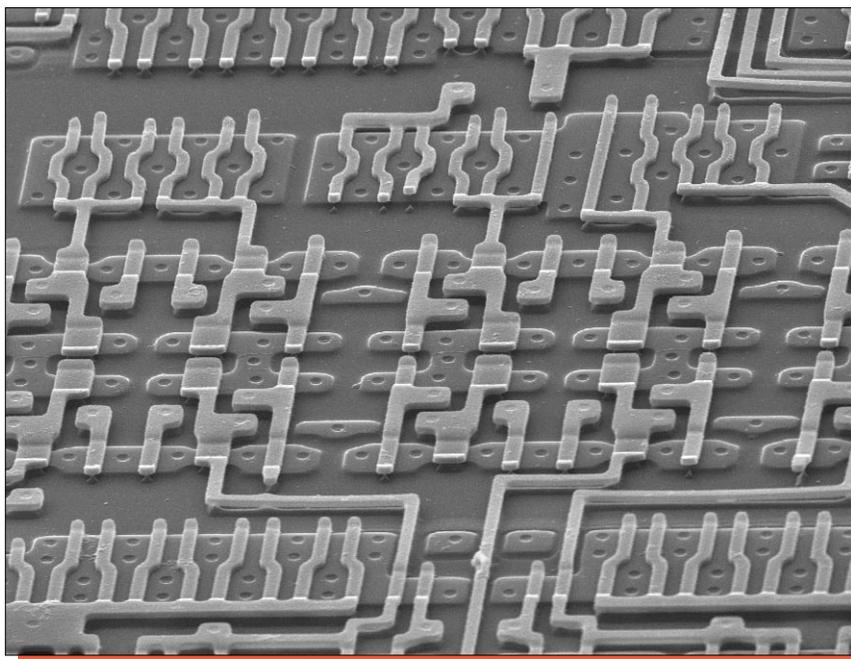


metal 2

Figure 23. SEM views of the SRAM cell. Mag. 3200x, 60°.

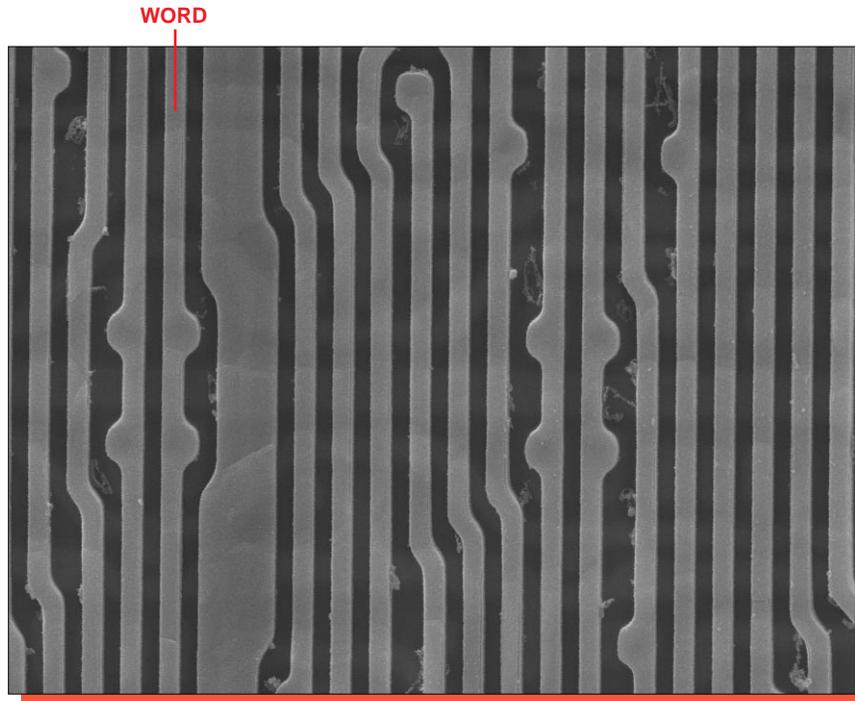


metal 1

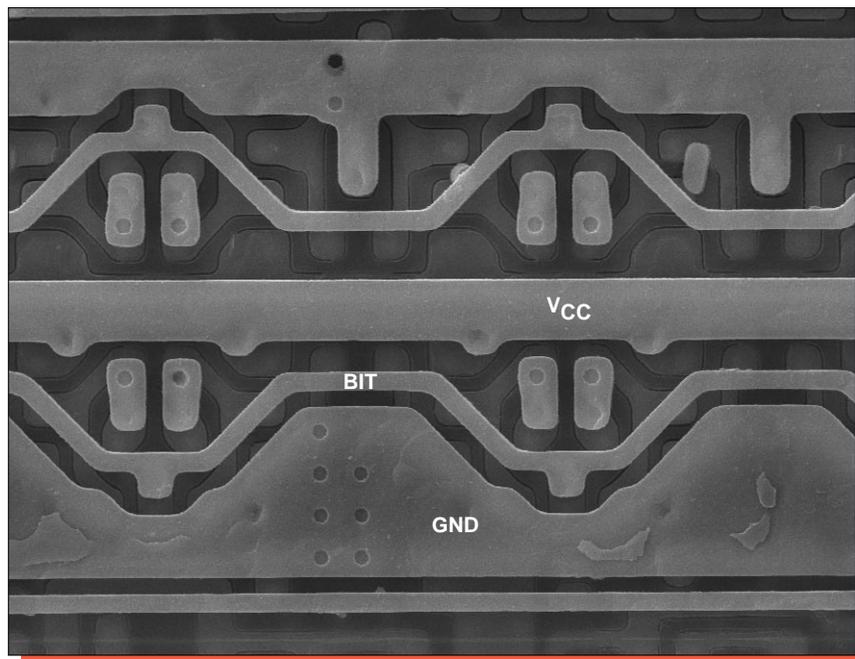


poly

Figure 24. SEM views of the SRAM cell. Mag. 3200x, 60°.



metal 3



metal 2

Figure 25. Topological SEM views of the SRAM cell. Mag. 3200x, 0°.

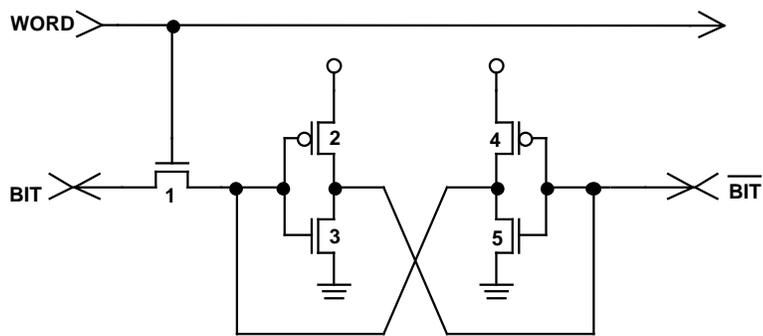
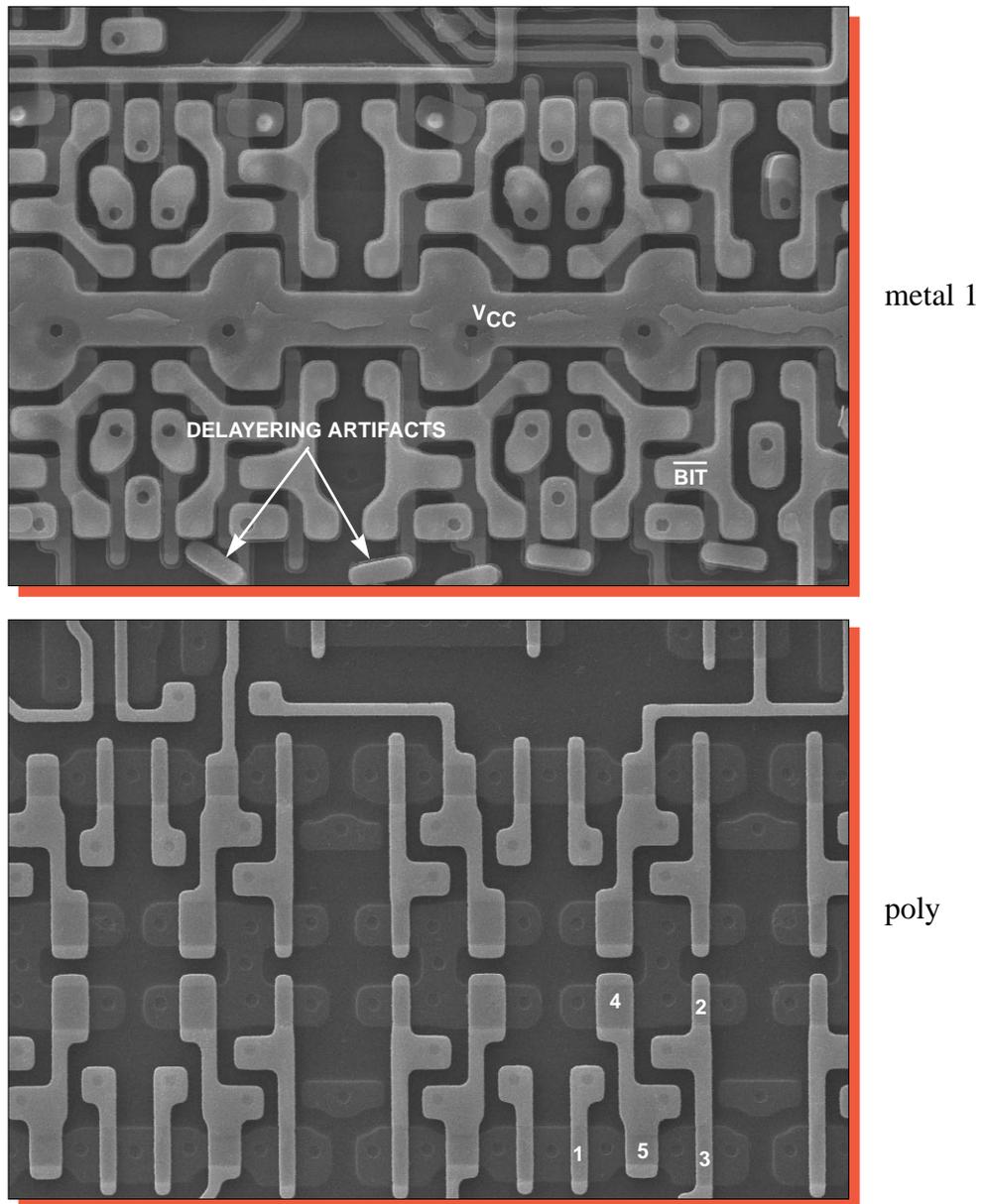
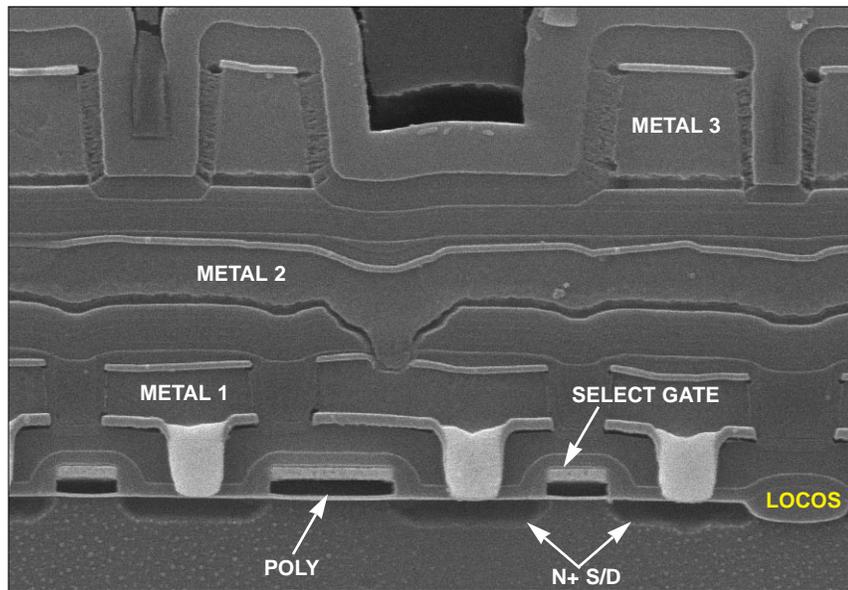
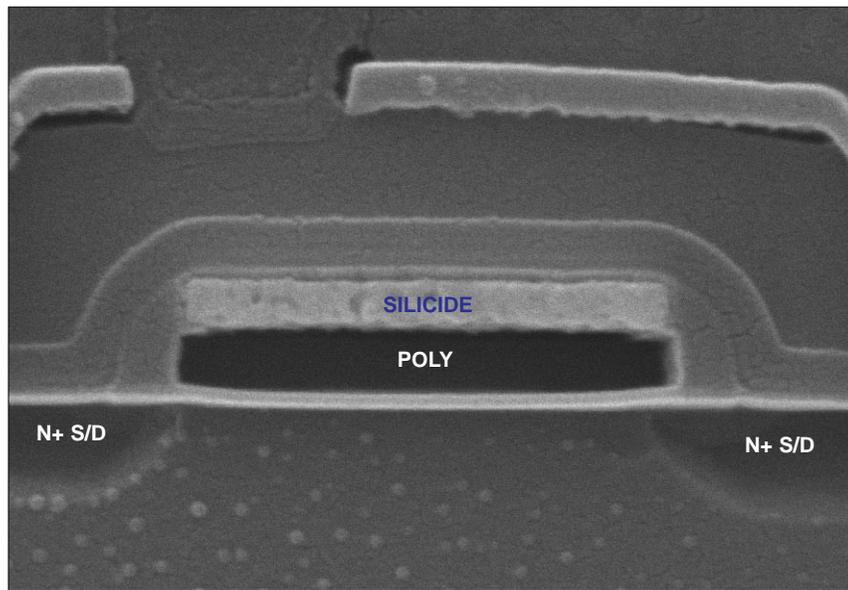


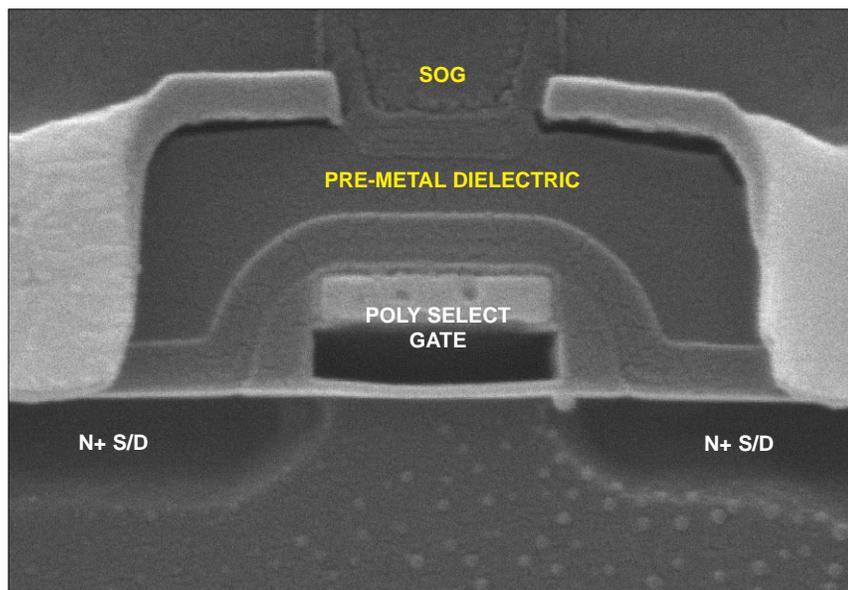
Figure 26. Topological views and schematic of the SRAM cell. Mag. 3200x, 0°.



Mag. 13,000x

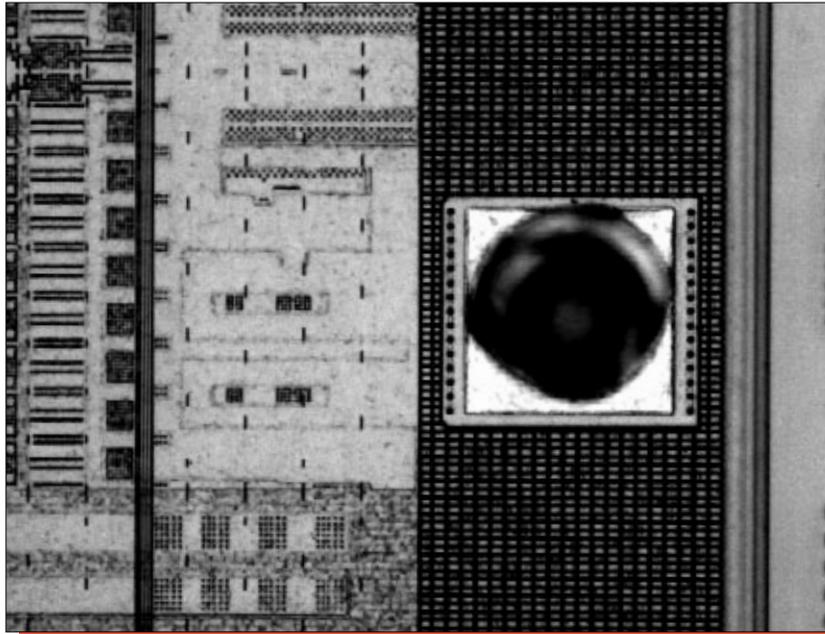


Mag. 32,000x



Mag. 52,000x

Figure 27. SEM section views of the SRAM cell.



Mag. 300x



Mag. 800x

Figure 28. Optical views of the I/O structure and general circuitry.