

Construction Analysis

Atmel AT89C2051 & AT89S8252 Microcontrollers

Report Number: SCA 9706-543



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INTRODUCTION

This report describes a construction analysis of the Atmel AT89C2051 and the AT89S8252 8-Bit Microcontrollers. Ten AT89C2051 devices encapsulated in 20-pin Dual-In-line Packages (DIPs) and two AT89S8252 devices in 40-pin Dual-In-line Packages were used for the analysis. The AT89C2051 devices were date coded 9642 and the AT89S8252 had a date code of 9709.

MAJOR FINDINGS

Questionable Items:¹

- Metal 1 aluminum thinning up to 90 percent² at some contact edges on the AT89C2051 (Figure 13).

Special Features: None.

Noteworthy Items:

- Both devices are of similar structure; however, there are distinct differences. The Flash cell design is the same on both devices; however, the cell of the AT89S8252 is smaller. The AT89S8252 also has an EEPROM memory. Cell design is identical and the only distinction between the Flash and the EEPROM memory appears to be the method in which the cells are erased. The other significant difference is that the AT89S8252 employs a second metal layer which is used sparsely, mainly to connect circuit blocks.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly (AT89C2051 device only unless indicated):

- 20-pin plastic Dual-In-line Package (DIP).
- 40-pin plastic Dual-In-line Package (DIP) AT89S8252.
- External leads plated with tin-lead (SnPb) and internally spot-plated with silver (Ag).
- A silver-epoxy die attach was employed on both die.
- Die coat was not employed on either die.
- Lead-locking provisions (holes) were present at all pins.
- Multiple wirebonds were used at Vcc and GND pins to provide extra current-carrying capacity. A bonding wire was connected from ground to the paddle for biasing purposes.
- Thermosonic wirebonding using 1.2 mil O.D. gold wire.
- Dicing was by sawing (full depth) on both die.

Die Process and Design

- Note: Process description is same on both devices except where noted.
- Fabrication process: CMOS process employing twin-wells, on a P-substrate.
- Final passivation: Two thick layers of silicon-dioxide.

TECHNOLOGY DESCRIPTION (continued)

- Metallization: Single level metallization was used on the AT89C2051 device. No cap was used; however a titanium-nitride barrier was employed. The metal was defined by a standard dry etch. Two levels of metallization were used on the AT89S8252 device. Metal 2 employed a titanium-nitride barrier and metal 1 employed a titanium-nitride cap and barrier. Metal 2 was sparsely used and appeared to mainly connect circuit blocks together.
- Interlevel dielectric (AT89S8252 device only): The dielectric consisted of two layers of glass. The first layer appeared to have been subjected to an etchback.
- Pre-metal: A single layer of reflow glass over grown oxides. The glass appeared to have been reflowed following the contact cuts.
- Polysilicon: Two layers of standard poly silicon were employed. Poly 2 was used to form all gates on the die and word lines and program lines in the EEPROM arrays. Poly 1 was used exclusively in the EEPROM arrays where it formed the floating gates.
- Diffusions: Standard implanted N⁺ and P⁺ diffusions formed the sources/drains of transistors. No sidewall spacers were present on the gates and no evidence of LDD structures was found.
- Isolation: LOCOS, a step was noted in the local oxide at the well boundary indicating a twin-well process was employed.
- Wells: Twin-wells in an P substrate.
- Fuses: No fuses were employed on this device.
- Buried contacts: No buried contacts were used.

TECHNOLOGY DESCRIPTION (continued)

- **SRAM:** The memory cell consisted of a 6T SRAM design. Metal 1 formed the bit lines and distributed Vcc and GND. Poly 2 formed the word lines, storage gates and pull-up devices.
- **EEPROM:** The memory cell design consisted of a poly 2 word line and program line and a poly 1 floating gate. Metal one formed the bit lines. Programming is achieved through ultra-thin tunnel oxide windows. Interpoly dielectric consisted of an ONO dielectric. Both of the devices AT89S8252 and AT89C2051 have the same layout design for both EEPROM (AT89S8252 only) and Flash memory. However, the cell size of the AT89S8252 was about half the size of the cell on the AT89C2051. On the AT89S8252 both EEPROM and Flash had the same design on the AT89S8252 device, but the way the cells are erased distinguishes the two types.
- **MROM:** An MROM cell array was employed on both devices. The cell was programmed by the metal 1 layer. No detailed analysis of this memory was performed since structures are the same as the peripheral circuits.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 4

Questionable Items:¹ None.

Special Features: None.

General Items:

- Overall package quality: Good. No significant defects were found on the external or internal portions of the packages on both die. No voids or cracks were noted in the plastic package on both die.
- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. All bond pull strengths were normal and no bond lifts occurred (see page 11).
- Die attach: Silver-epoxy of normal quality. No problems were found.
- Die dicing: Die separation was by sawing (full depth) and showed normal quality workmanship. No large chips or cracks were present at the die surface.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 5 - 31

Questionable Items:¹

- Metal 1 aluminum thinning up to 90 percent² at some contact edges on the AT89C2051 (Figure 13).

Special Features: None.

Noteworthy Items:

- Both devices are of similar structure; however, there are distinct differences. The Flash cell design is the same on both devices; however, the cell of the AT89S8252 is smaller. The AT89S8252 also has an EEPROM memory. Cell design is identical and the only distinction between the Flash and the EEPROM memory appears to be the method in which the cells are erased. The other significant difference is that the AT89S8252 employs a second metal which is used sparsely, mainly to connect circuit blocks.

General Items:

- Fabrication process: CMOS process employing twin-wells in a P substrate. All P-channel devices were formed in N-wells. All N-channel devices were formed in P-wells. No epi was employed on these devices.
- Design implementation: Die layout was clean. Alignment was good at all levels.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

ANALYSIS RESULTS II (continued)

- Surface defects: No contamination, processing defects or tool marks were found.
- Final passivation: Two thick layers of silicon-dioxide.
- Metallization: A single level metallization was used on the AT89C2051 device. No cap was used; however a titanium-nitride barrier was employed. Two levels of metallization were used on the AT89S8252 device. Metal 2 employed a titanium-nitride barrier and metal 1 employed a titanium-nitride cap and barrier. Metal 2 was used mainly to connect circuit blocks together.
- Metal patterning: The metal layers were defined by standard dry etch. Metal completely surrounded all contacts. Standard contacts were employed (no plugs).
- Metal defects: No notching or voiding was found. No silicon nodules were observed following removal of the aluminum layers.
- Metal step coverage: Metal 1 aluminum thinning was up to 90 percent thinning (Figure 13) at some contacts. The amount of thinning is excessive a manufacturer's design specifications should be verified (AT89C2051 only).
- Contacts: Contacts were overetched slightly into the substrate and polysilicon; however, no problems are foreseen.
- Interlevel dielectric (AT89S8252 device only): The dielectric consisted of two layers of glass. The first layer appeared to have been subjected to an etchback. No problems were noted.
- Pre-metal: A single layer of reflow glass over grown oxides. The glass was reflowed following the contact cuts. No problems were found.

ANALYSIS RESULTS II (continued)

- Polysilicon: Two layers of standard polysilicon were employed. Poly 2 was used to form all gates on the die and word lines and program lines in the EEPROM array. Poly 1 was used exclusively in the EEPROM array where it formed the floating gates.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries.
- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. No sidewall spacers were used and no evidence of LDD structures were found.
- Wells: Twin-wells in an P substrate.
- Fuses: No fuses were employed on this device.
- Buried contacts: No buried contacts were used.
- SRAM: The memory cell consisted of a 6T SRAM design. Metal 1 formed the bit lines and distributed Vcc and GND. Poly 2 formed the word lines, storage gates and pull-up devices.
- EEPROM: The memory cell design consisted of a poly 2 word line and program line and a poly 1 floating gate. Metal one formed the bit lines. Programming is achieved through ultra-thin tunnel oxide windows. Interpoly dielectric consisted of an ONO dielectric. Both of the devices AT89S8252 and AT89C2051 have the same layout design for both EEPROM (AT89S8252 only) and Flash memory. However, the cell size of the AT89S8252 was about half the size of the cell on the AT89C2051. On the AT89S8252 both EEPROM and Flash had the same design. The way the cells are erased distinguishes the two types.
- MROM: An MROM cell array was employed on both devices. The cell was programmed through metal 1 layer. No detailed analysis of this memory was performed since structures are the same as peripheral circuits.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

Decapsulation

Optical inspection

Wirepull test

SEM of passivation and assembly features

Passivation removal and inspect metal

Aluminum removal

Delayer to poly and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	N
Dicing quality	N
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Contact registration	G

*Metal 1 aluminum thinning up to 90 percent.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

AT89C2051

TOP

(Logo)
AT89C2051
9642
12PC

BOTTOM

6C203-1
9056F
1-F 6C9642

AT89S8252

TOP

(Logo)
AT89S8252
24PC
9709

BOTTOM

6D0412-2
19552H
1 KOREA
6D9706

WIREBOND STRENGTH (AT89C2051)

Wire material: 1.2 mil diameter gold

Die pad material: aluminum

<u>Sample #</u>	1
# of wires pulled:	15
Bond lifts:	0
Force to break - high:	19.0g
- low:	14.0g
- avg.:	16.1g
- std. dev.:	1.7

DIE MATERIALS

Passivation:	Two layers of silicon-dioxide.
Metal 2 (AT89S8252 device only):	Aluminum with a titanium-nitride barrier.
Metal 1:	Aluminum with a titanium-nitride barrier. Metal 1 also employed a titanium-nitride cap on the AT89S8252 device.
Interlevel dielectric (AT89S8252 device only):	Two layers of silicon-dioxide.
Pre-metal dielectric:	BPSG glass.

VERTICAL DIMENSIONS

Note: All dimensions taken from the AT89C2051 device, except where noted.

Die thickness: 0.3 mm (11.5 mils)

Layers

Passivation 2:	0.8 micron
Passivation 1:	0.6 micron
Metal 2 (AT89S8252) - aluminum:	1.0 micron
- barrier:	0.06 micron (approx.)
Metal 1 (AT89C2051) - aluminum:	0.7 micron
- barrier:	0.06 micron (approx.)
Interlevel dielectric (AT89S8252):	1.3 micron (average)
Pre-metal dielectric:	0.55 micron (average)
Oxide on poly 2:	0.15 micron
Poly 1:	0.25 micron
Poly 2:	0.4 micron
Local oxide:	0.8 micron
N+ S/D diffusion:	0.4 micron
P+ S/D diffusion:	0.3 micron
N-well:	5 microns (approx.)

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AT89C2051

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AT89S8252

PACKAGE PHOTOS	Figure 32
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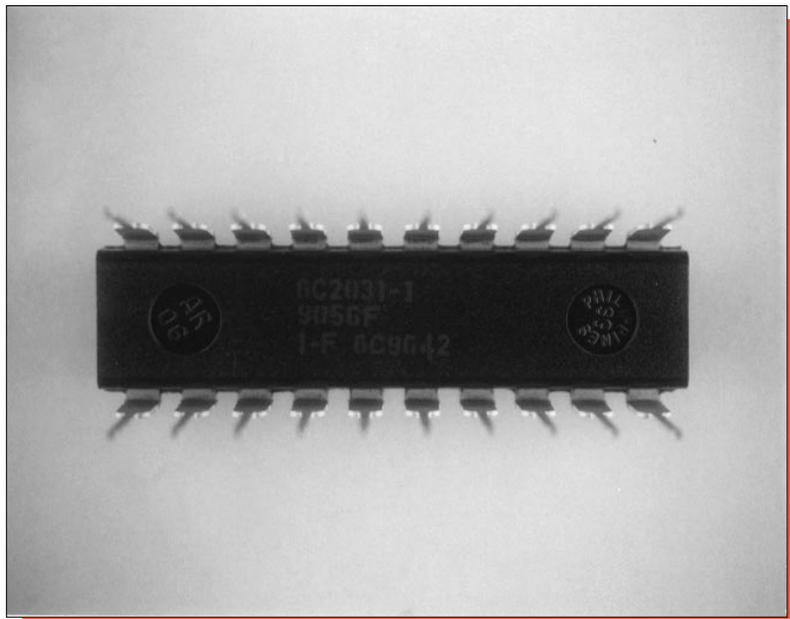
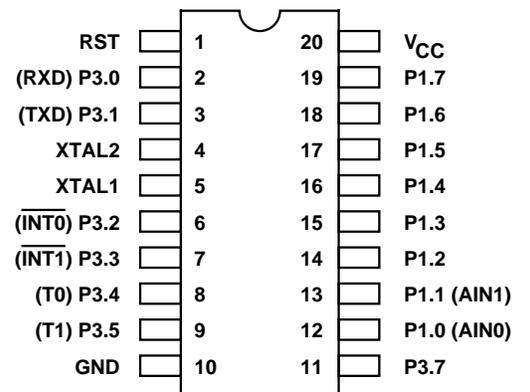
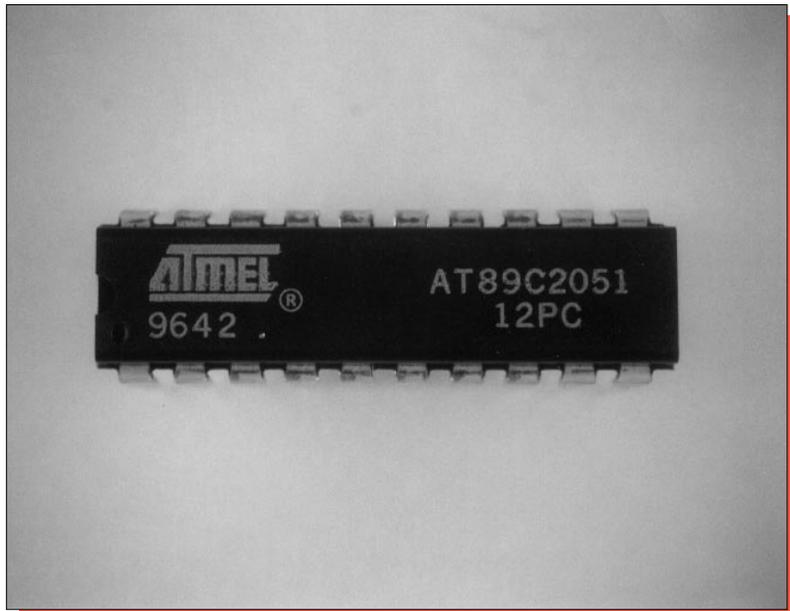


Figure 1. Package photographs and pinout of the Atmel AT89C2051. Mag. 3x.

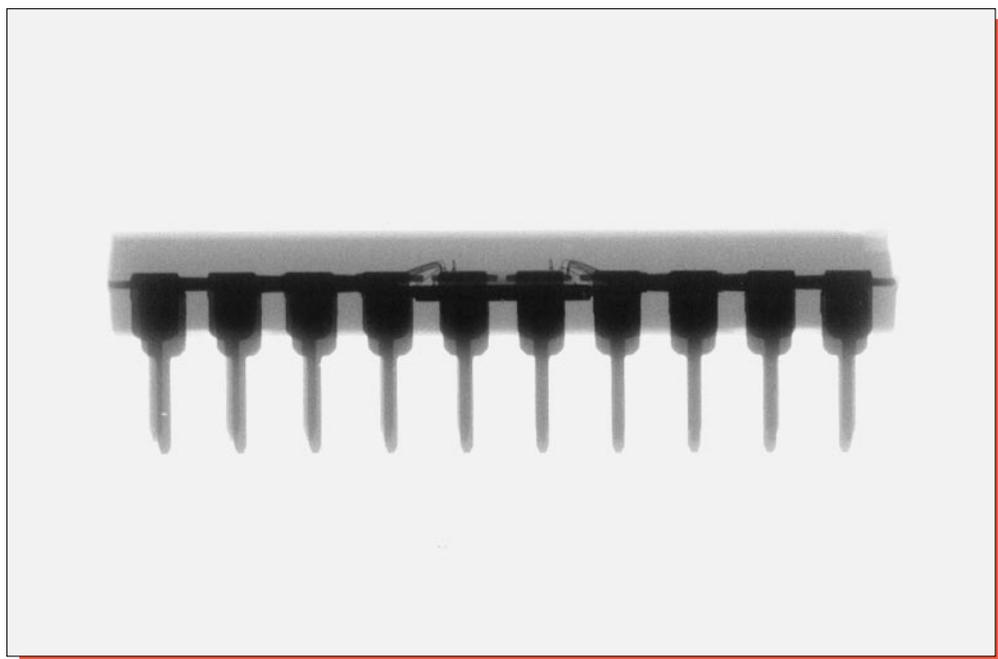
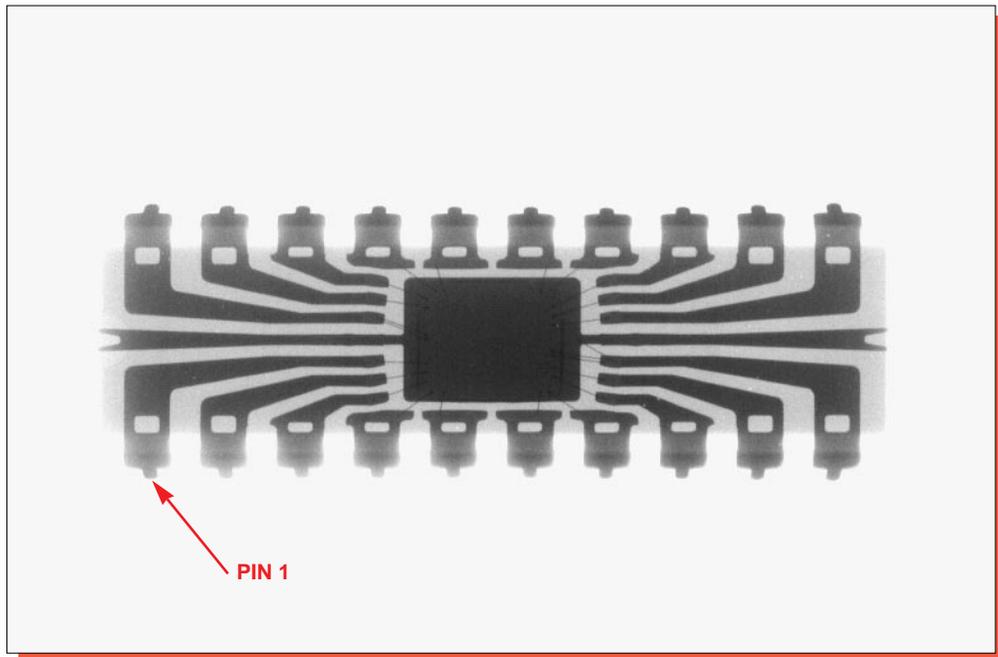
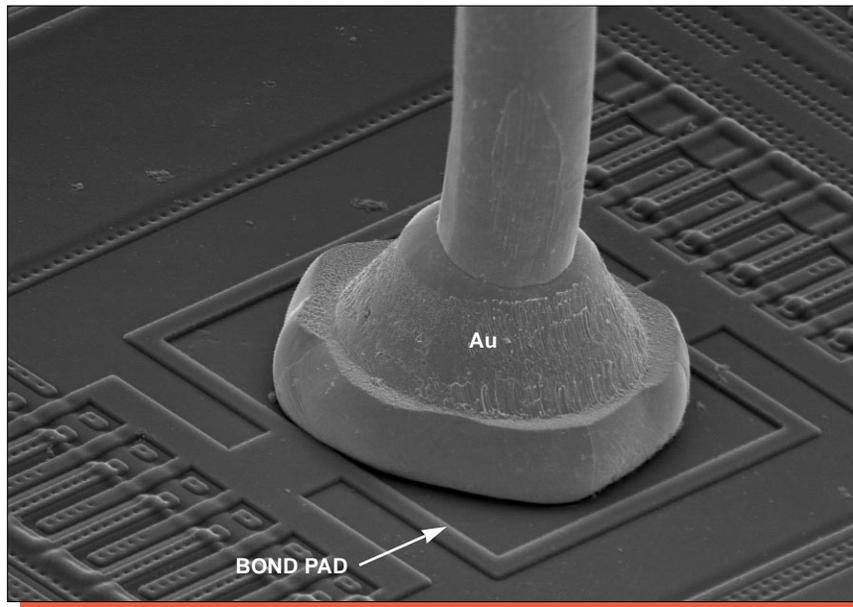
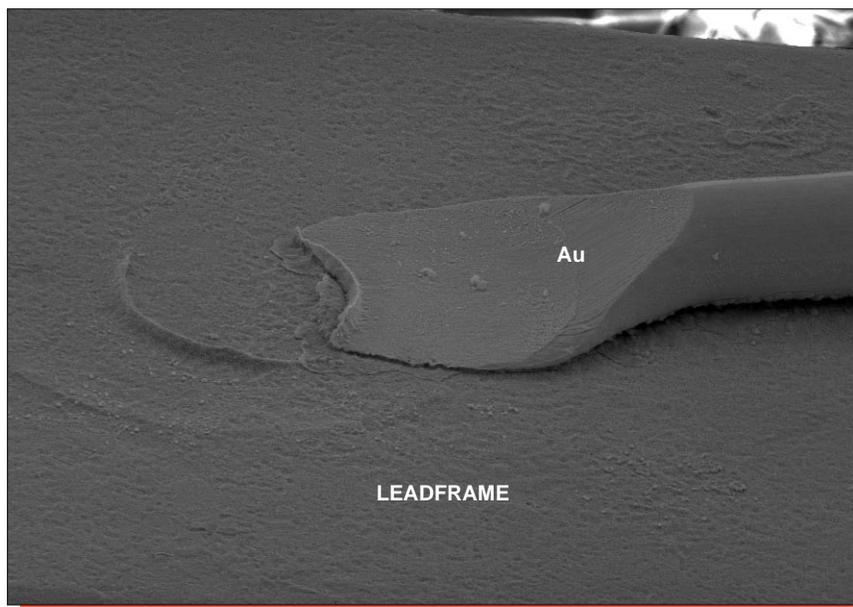


Figure 2. X-ray views of the package. Mag. 4x.

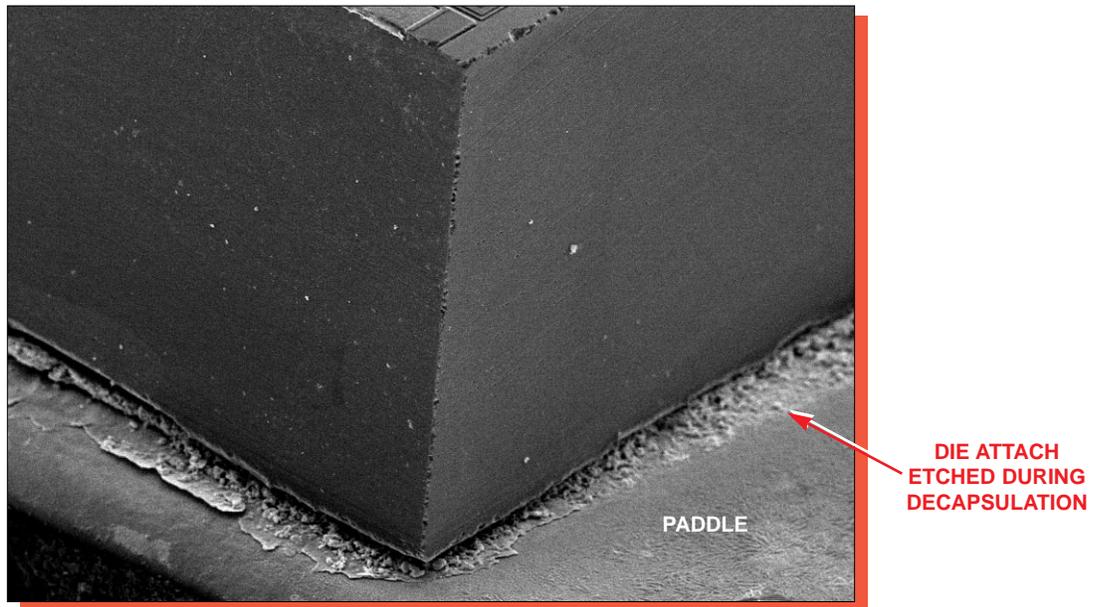


Mag. 570x

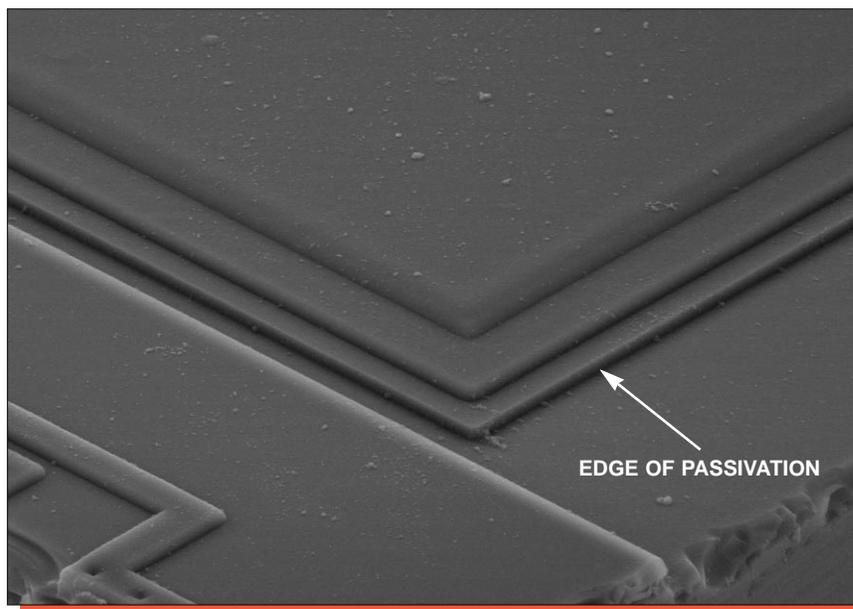


Mag. 500x

Figure 3. SEM views of typical wirebonds. 60°.



Mag. 150x



Mag. 1100x

Figure 4. SEM views illustrating die corner and edge seal. 60°

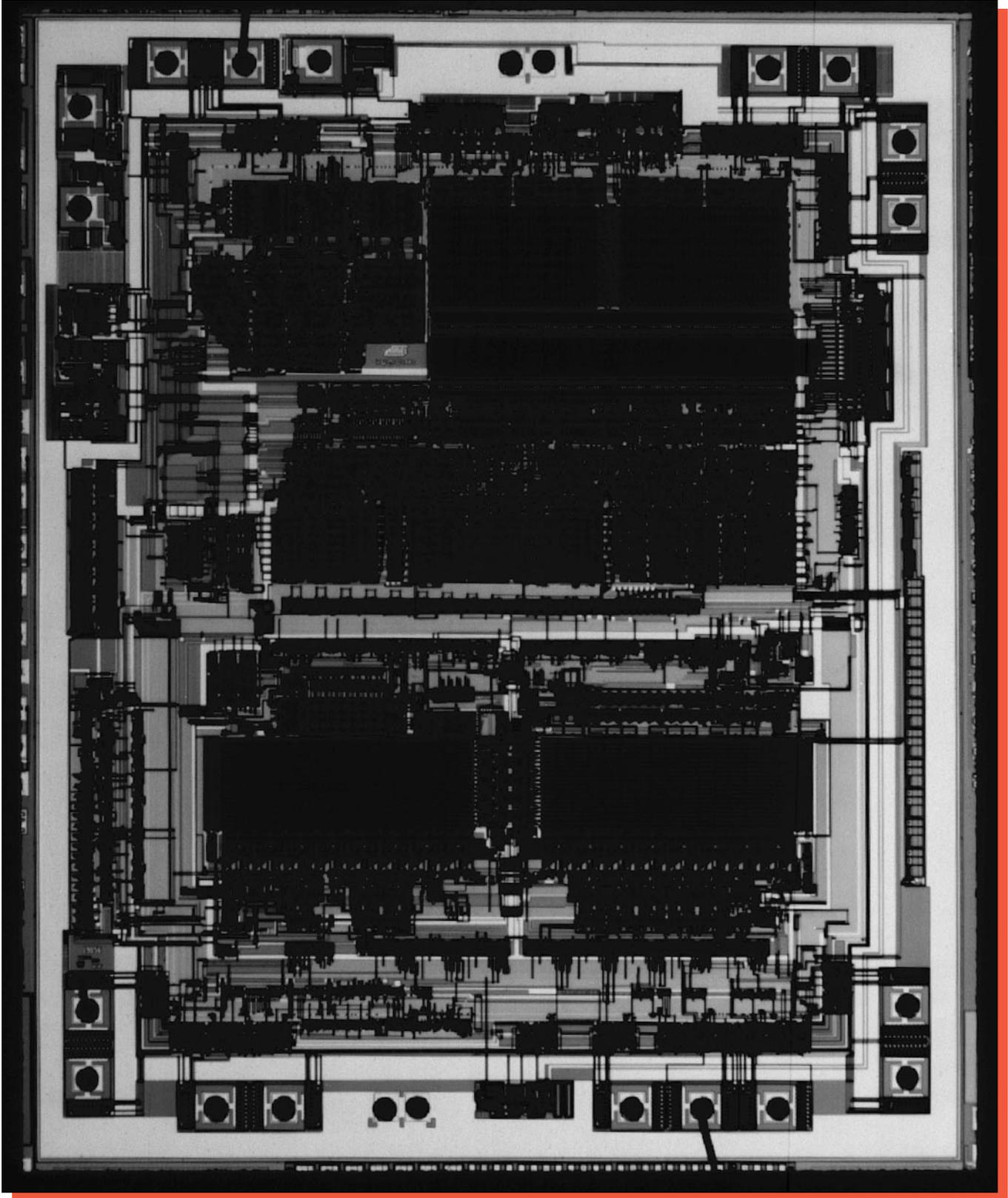


Figure 5. Whole die photograph of the Atmel AT89C2051. Mag. 44x.

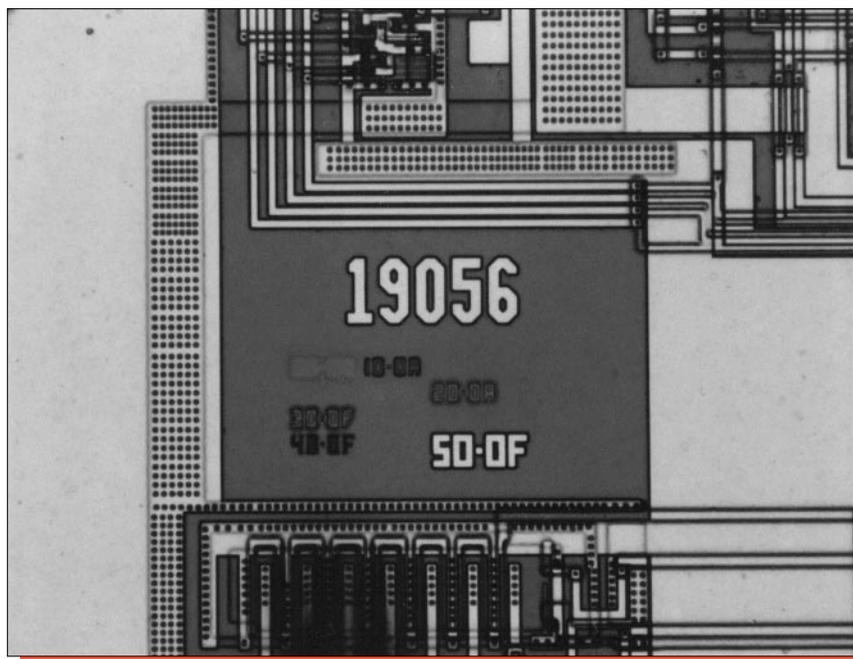
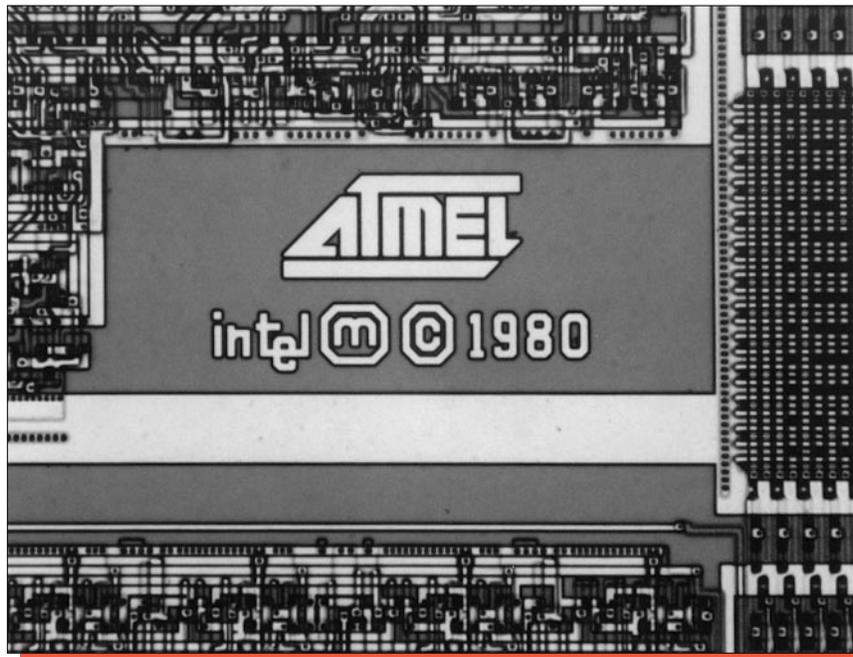


Figure 6. Optical views illustrating markings on the die surface. Mag. 320x.

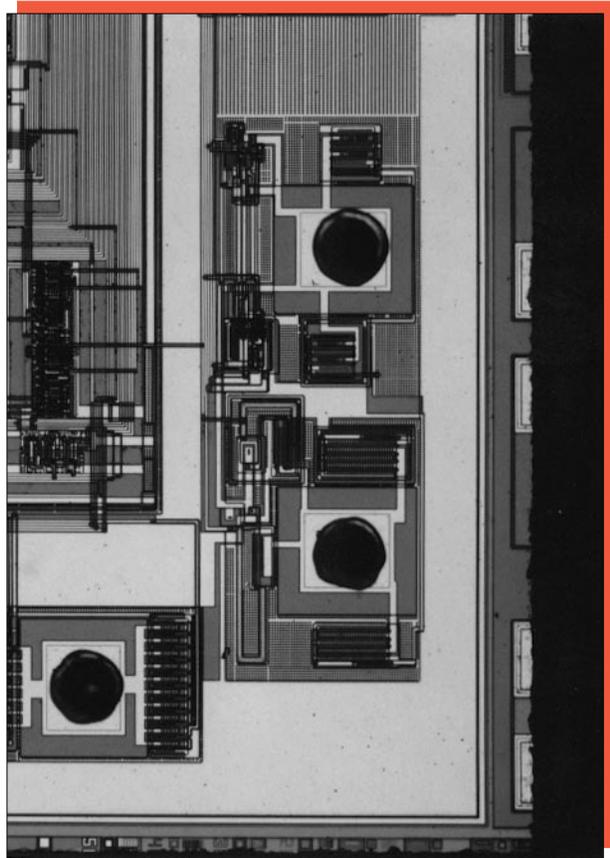
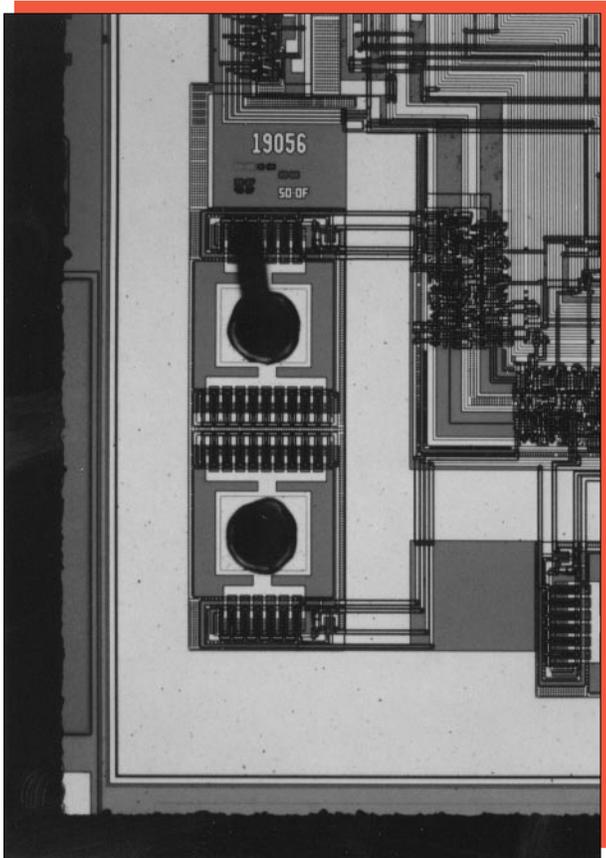
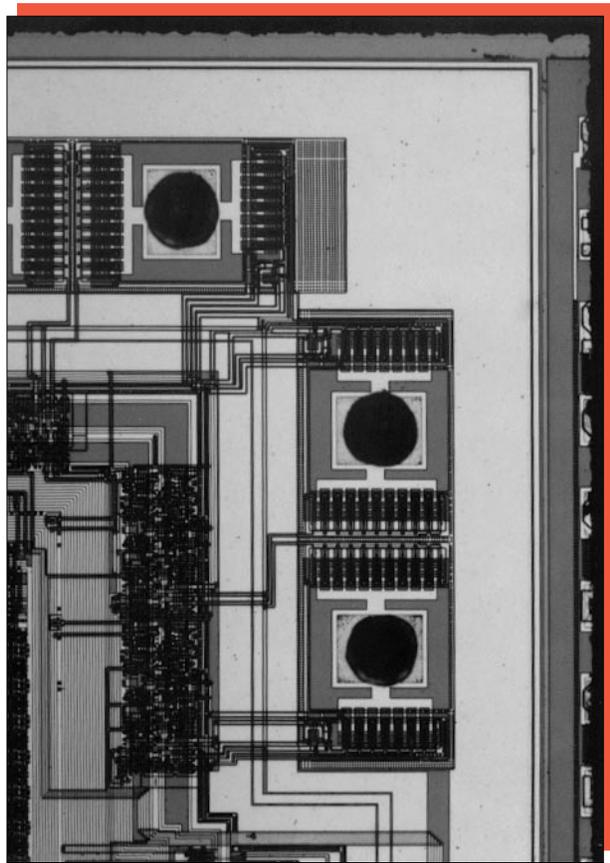
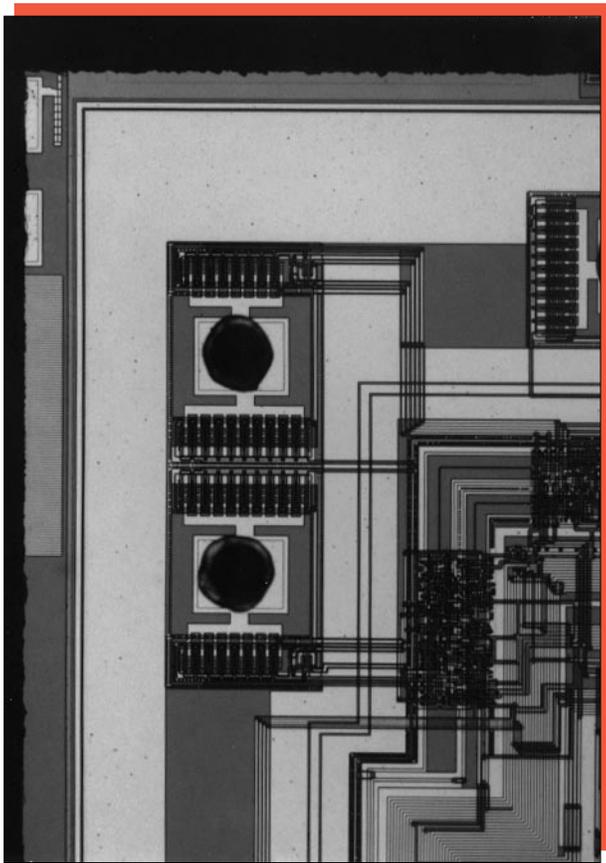
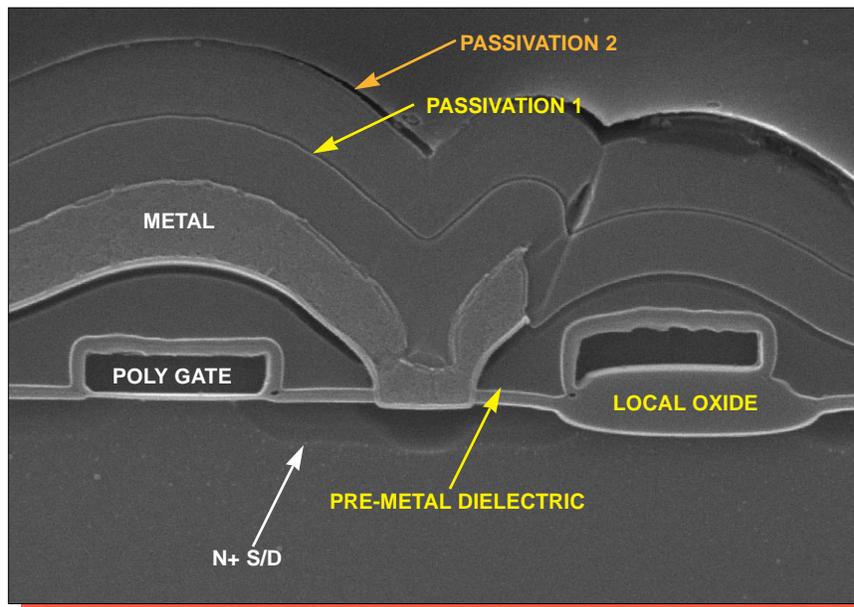
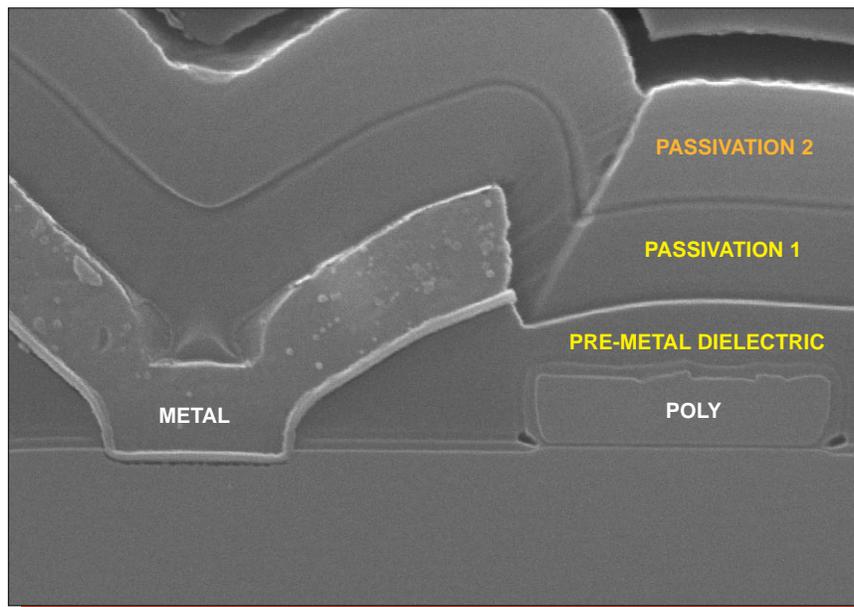


Figure 7. Optical views of die corners. Mag. 100x.

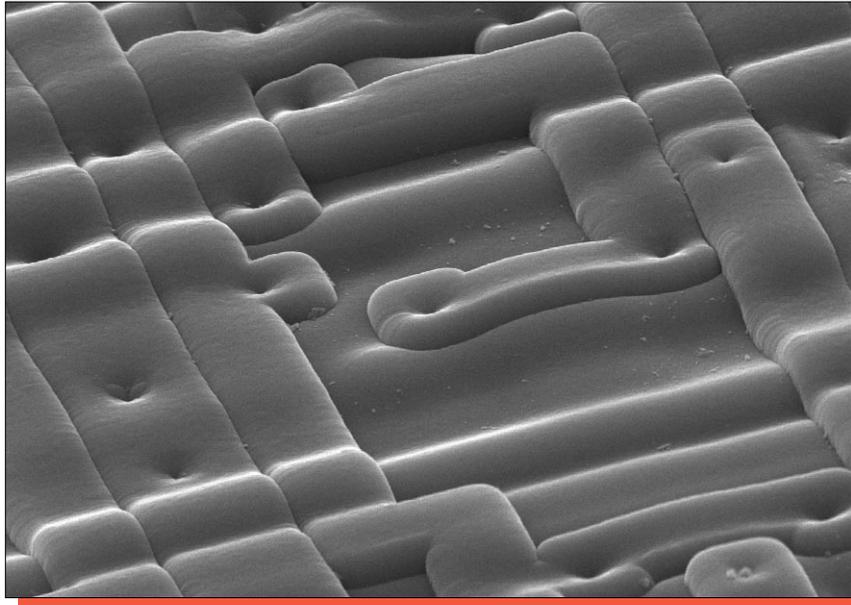


silicon etch, Mag. 13,000x

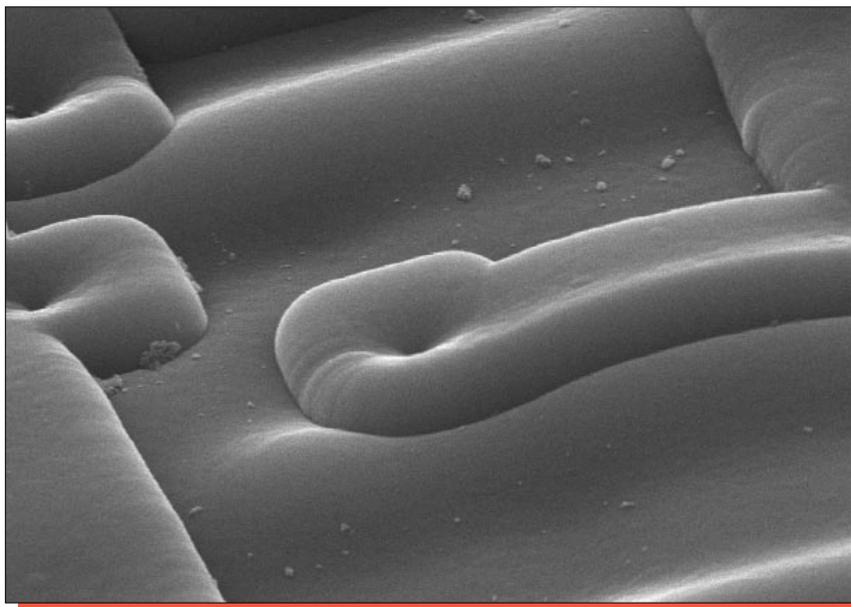


glass etch, Mag. 21,000x

Figure 8. SEM section views of general structure.

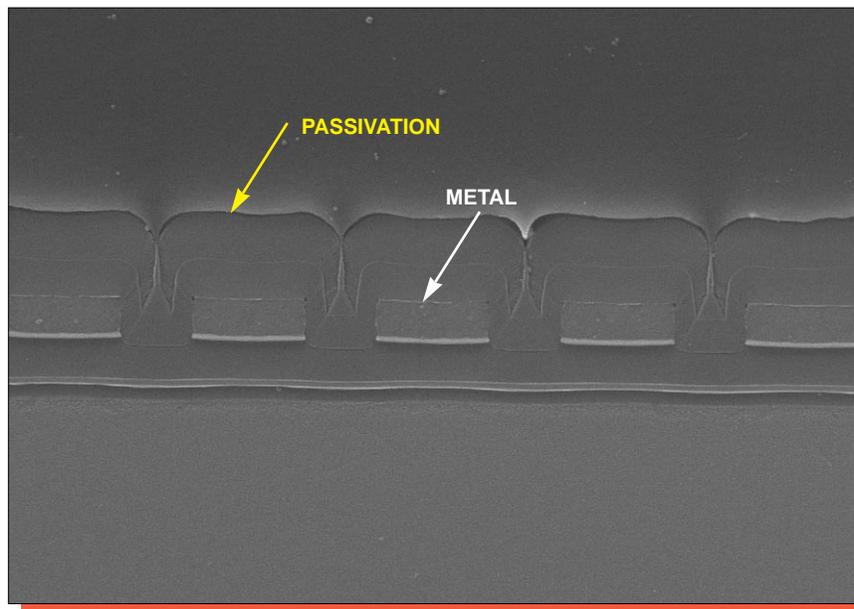


Mag. 3200x

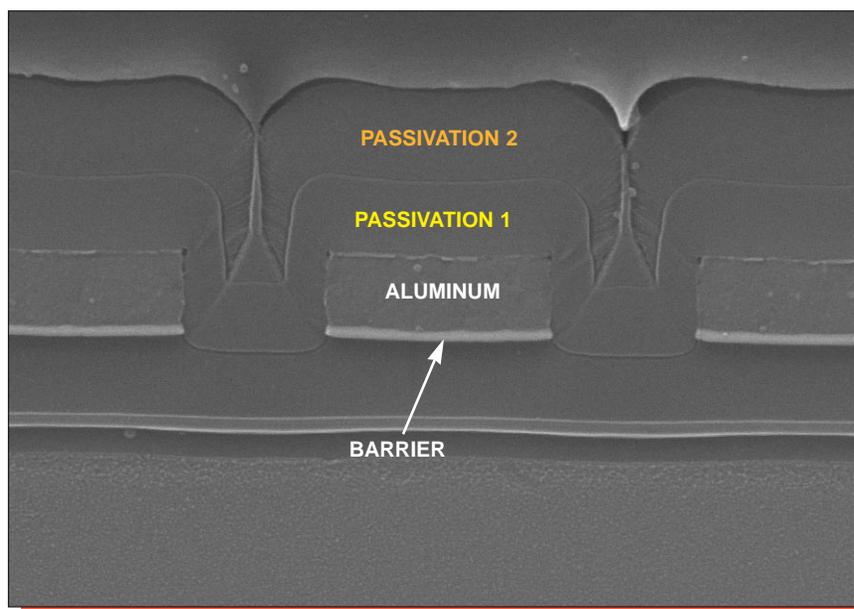


Mag. 7500x

Figure 9. Perspective SEM views illustrating overlay passivation coverage. 60°.

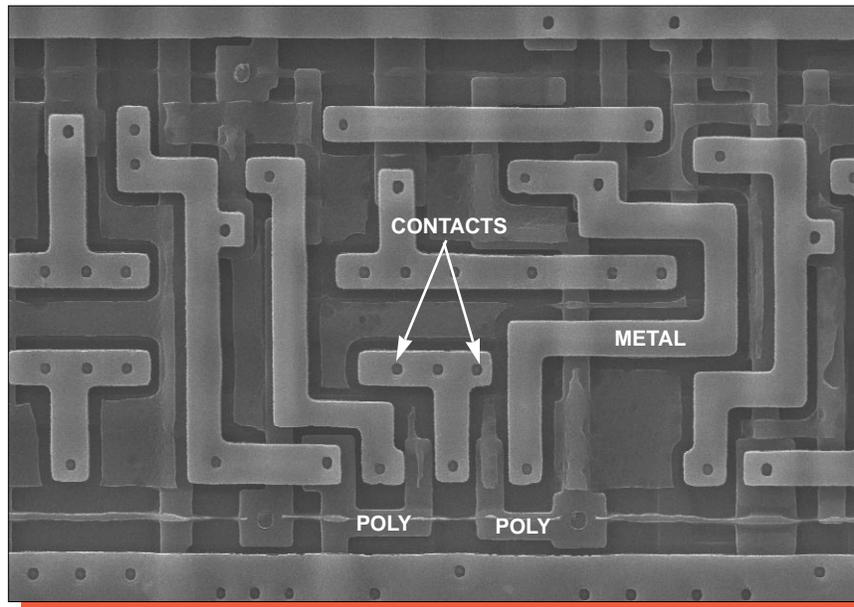


Mag. 6500x

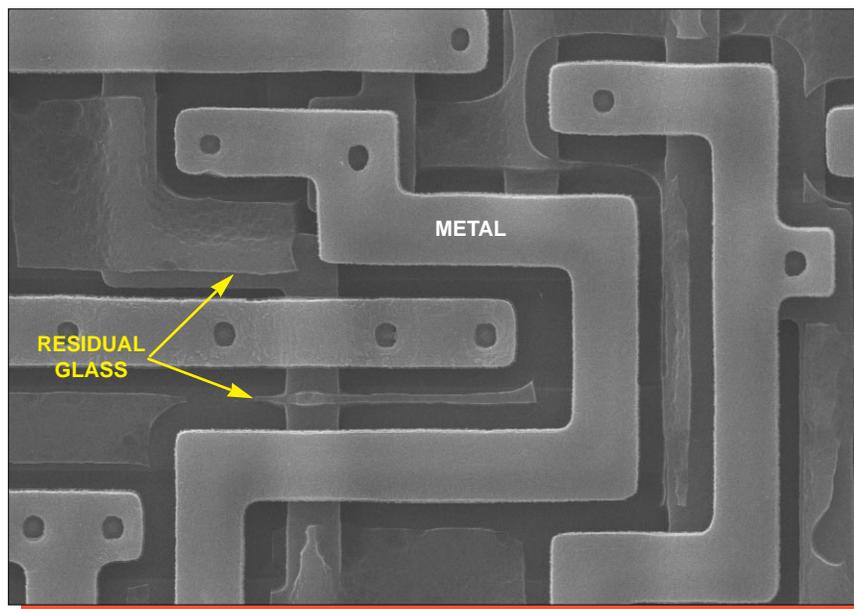


Mag. 13,000x

Figure 10. SEM section views illustrating metal line profiles.

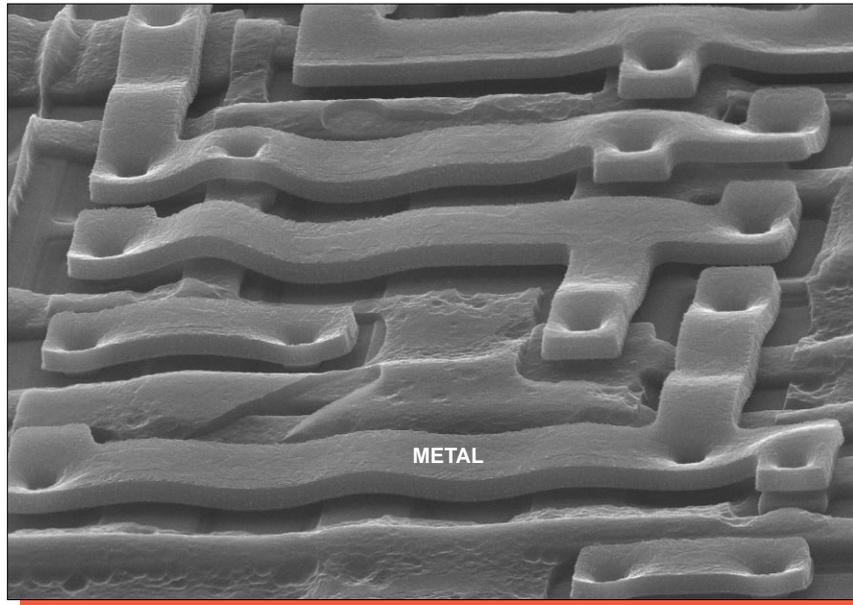


Mag. 1600x

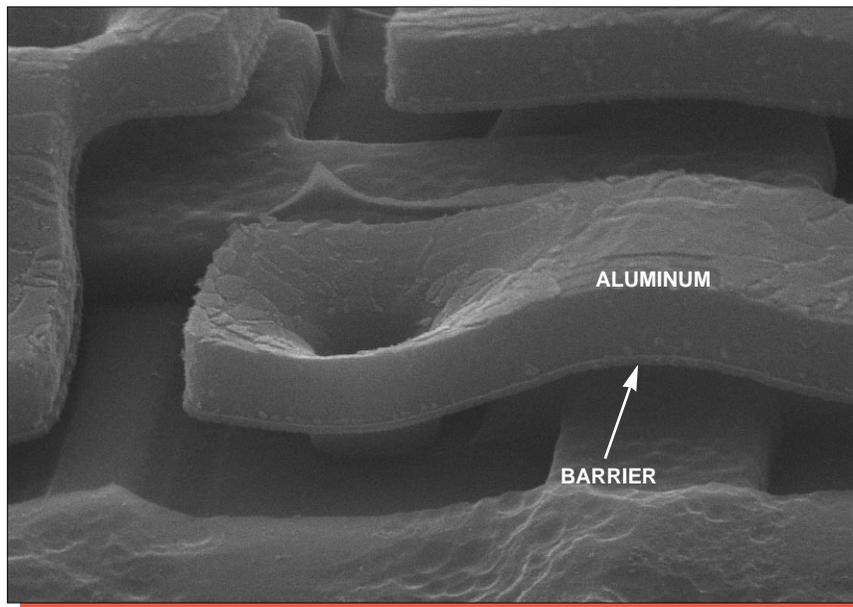


Mag. 3200x

Figure 11. Topological SEM views illustrating metal patterning. 0°.

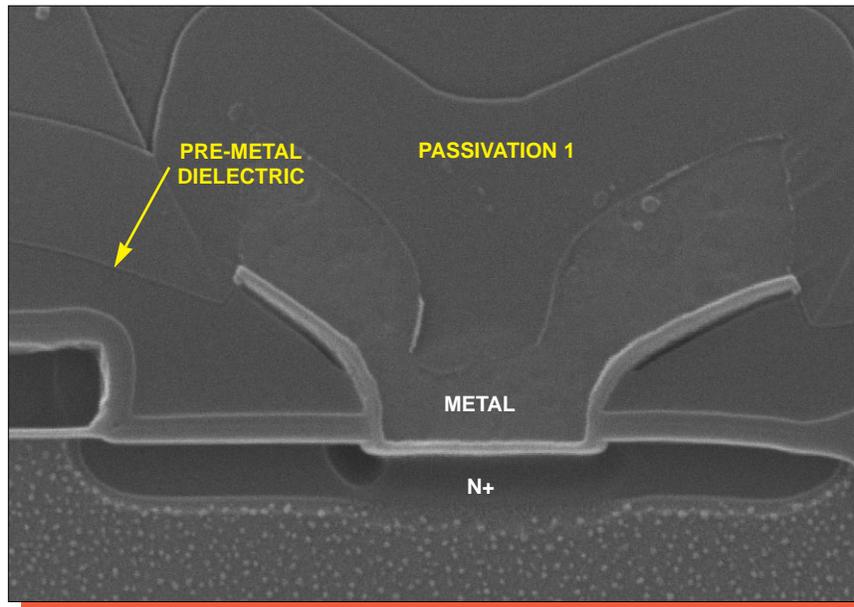


Mag. 3700x

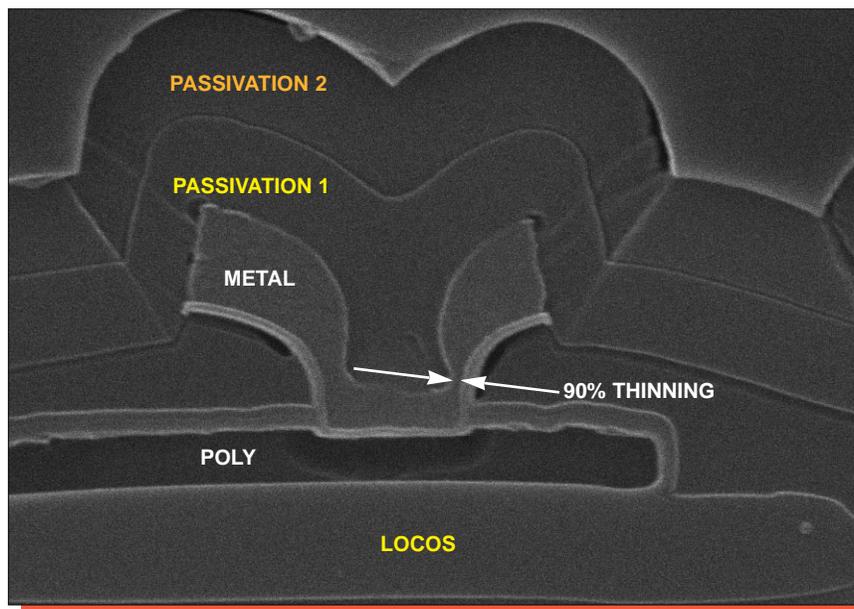


Mag. 13,000x

Figure 12. SEM views illustrating metal coverage. 60°.

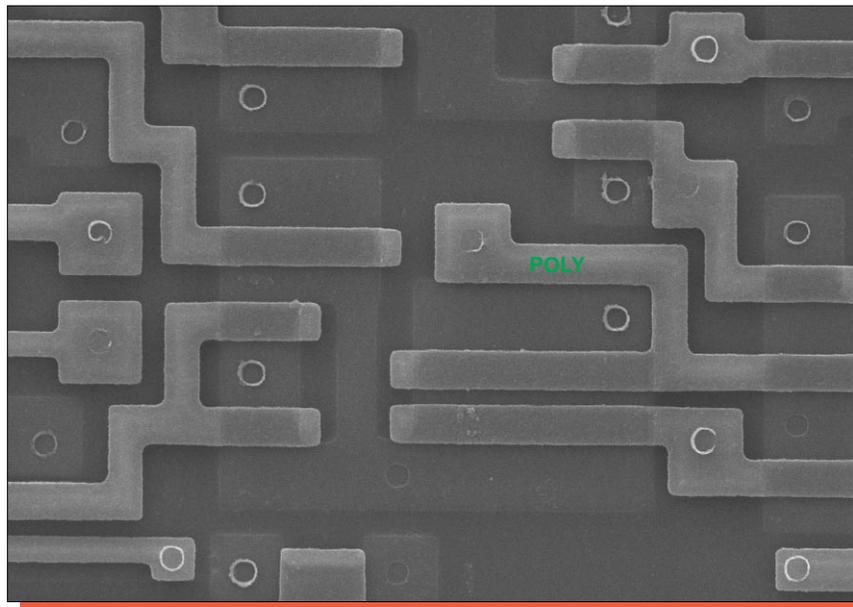


Mag. 26,000x

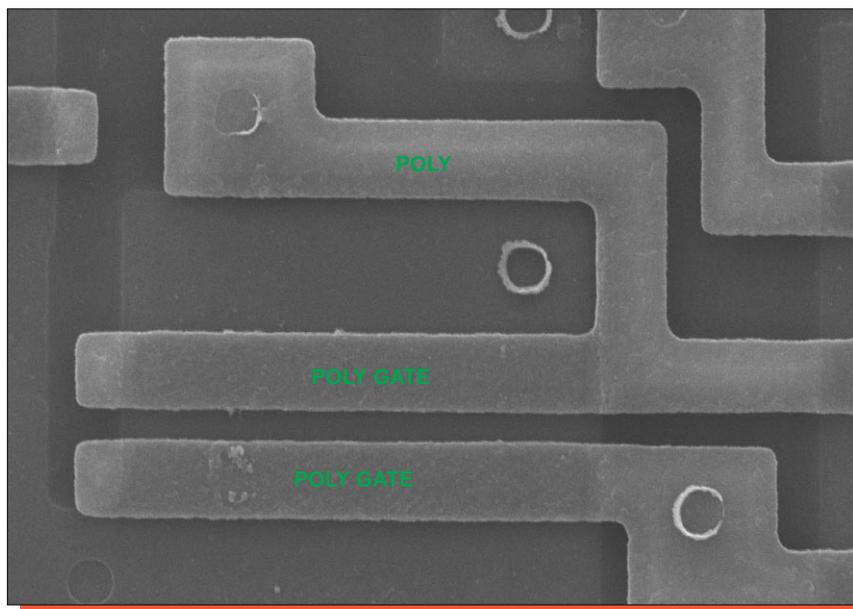


Mag. 17,600x

Figure 13. SEM section views illustrating metal contacts.

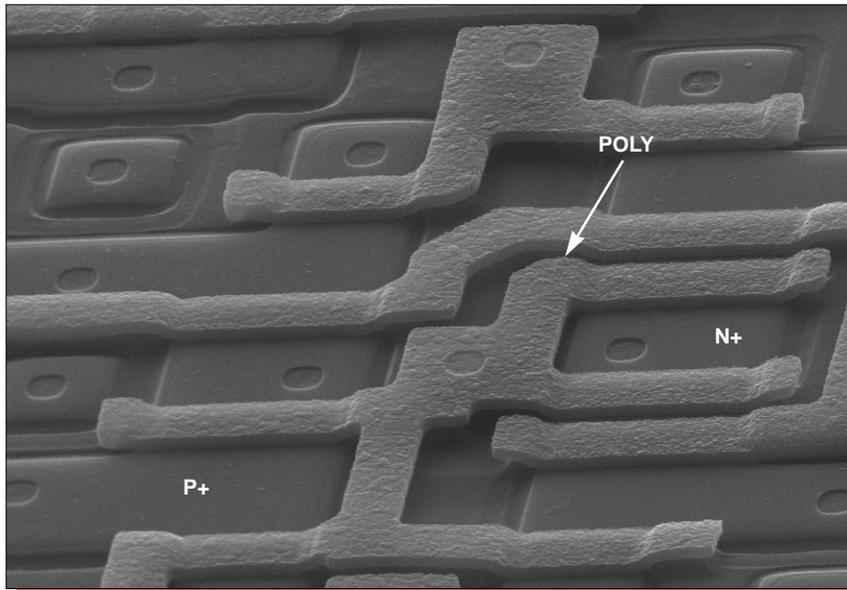


Mag. 2400x

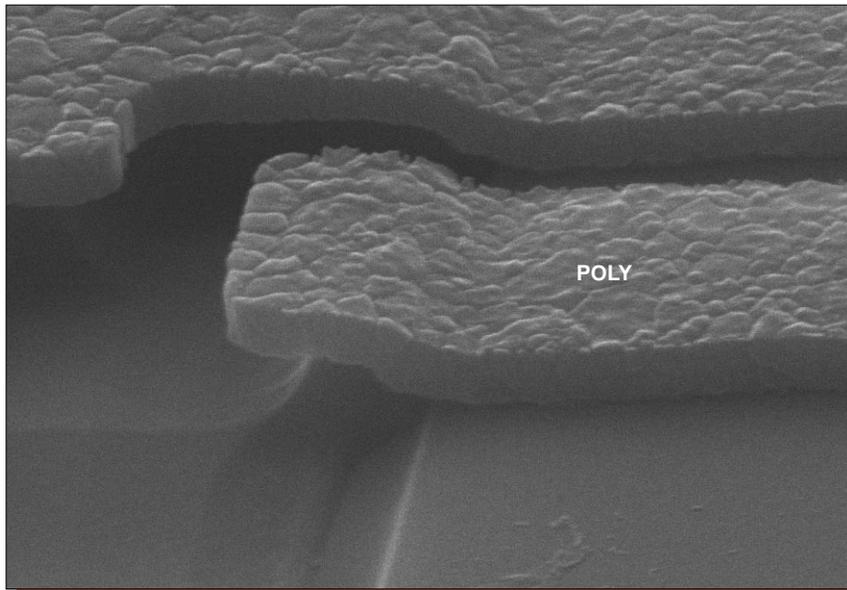


Mag. 4700x

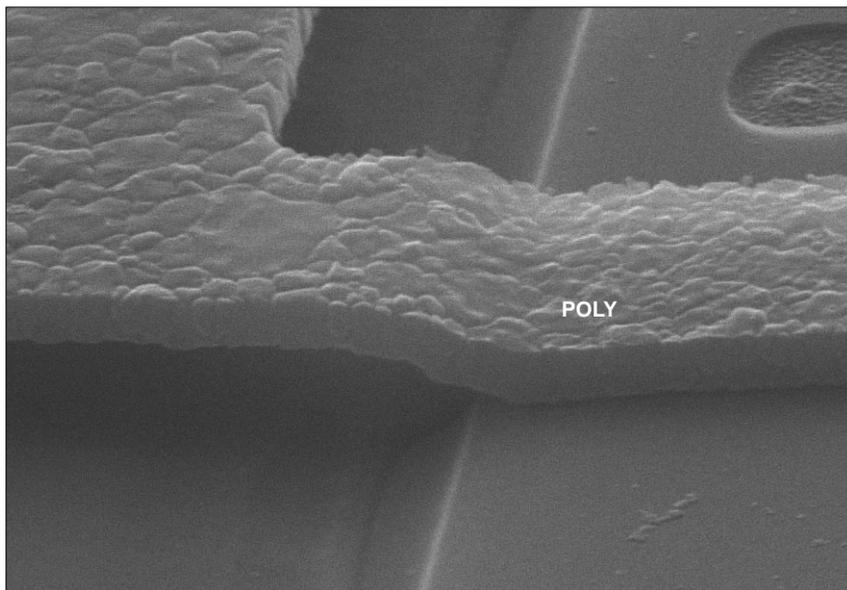
Figure 14. SEM views illustrating poly patterning. 0°.



Mag. 4400x

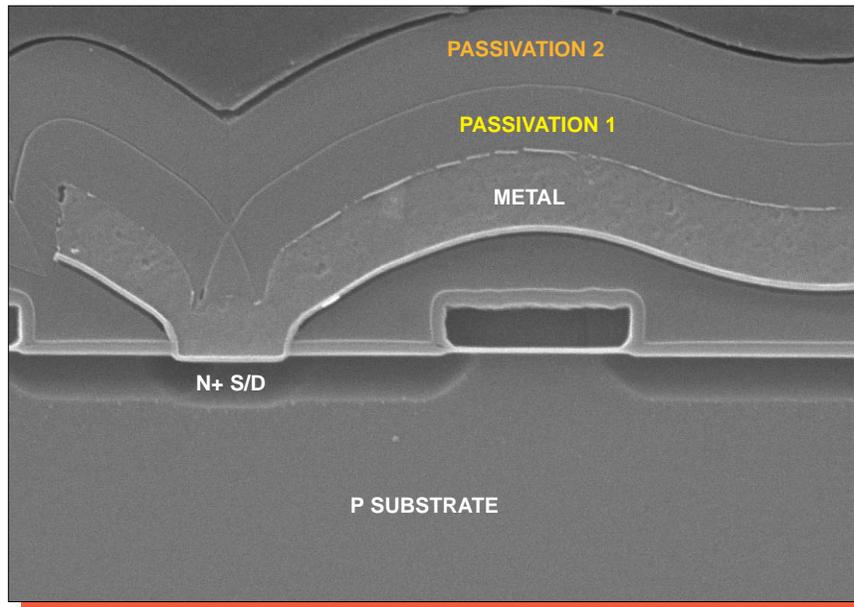


Mag. 20,000x

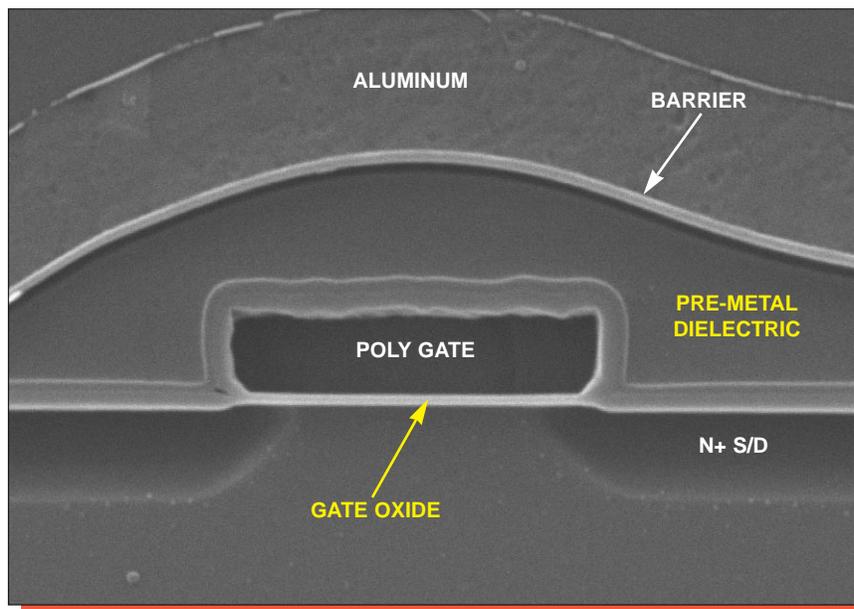


Mag. 20,000x

Figure 15. SEM views illustrating poly coverage. 60°.

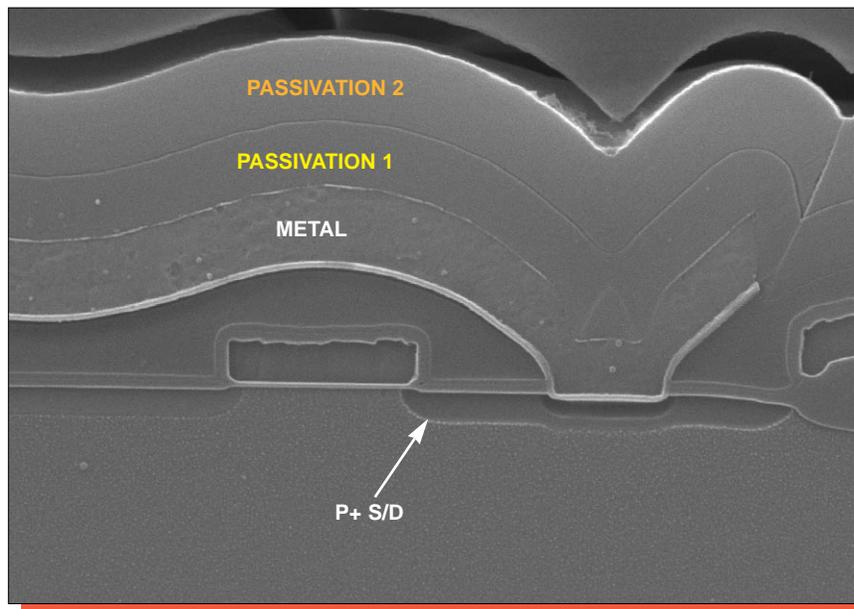


Mag. 13,000x

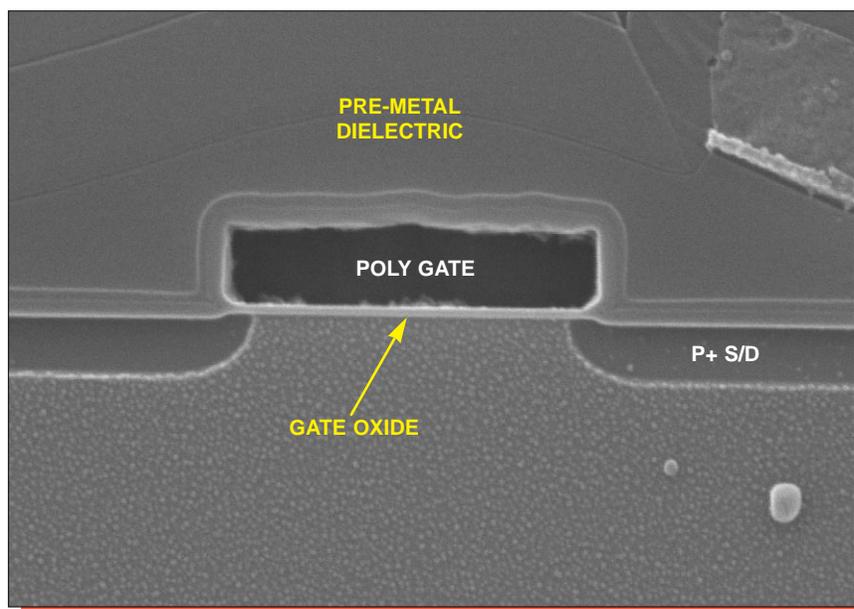


Mag. 26,000x

Figure 16. SEM section views illustrating N-channel transistor.

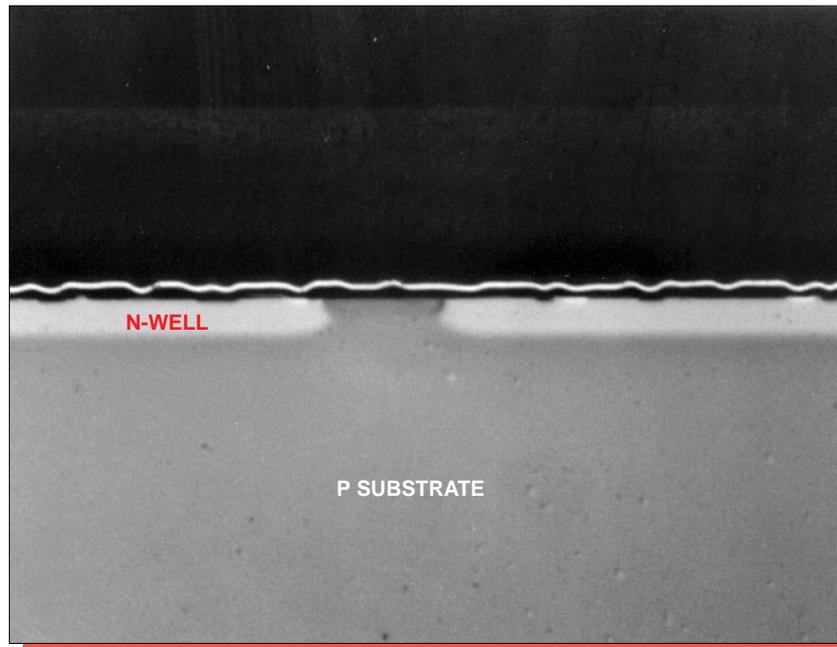


Mag. 13,000x

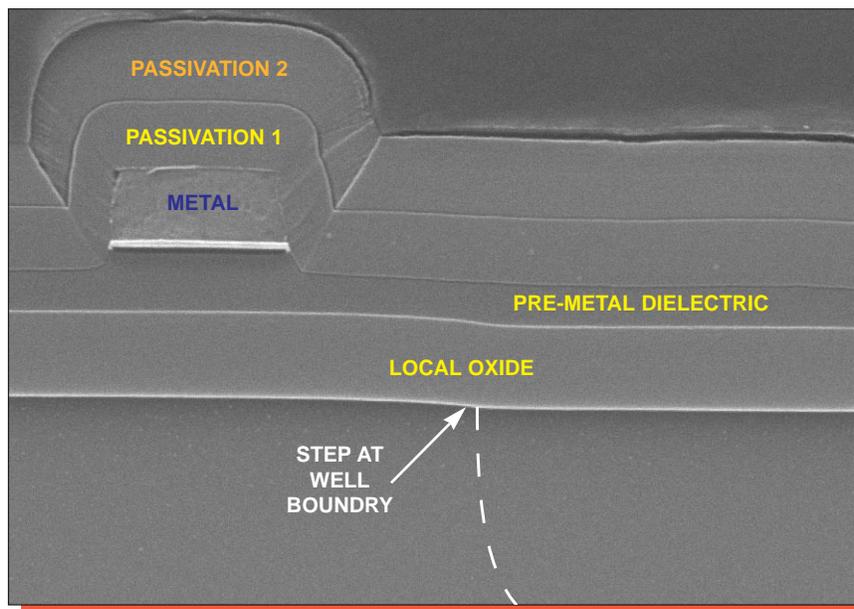


Mag. 26,000x

Figure 17. SEM section views illustrating P-channel transistor.

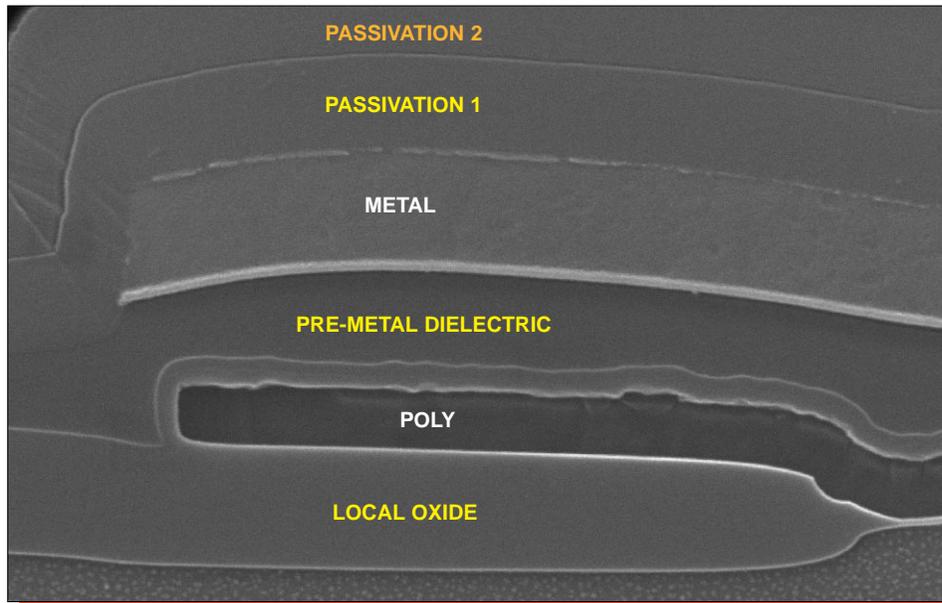


Mag. 800x

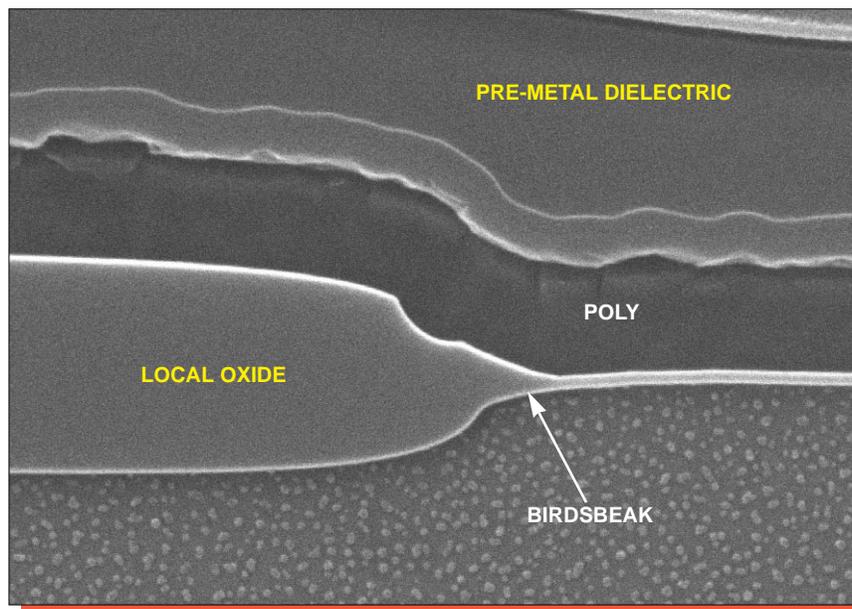


Mag. 13,000x

Figure 18. SEM section views illustrating well structure.

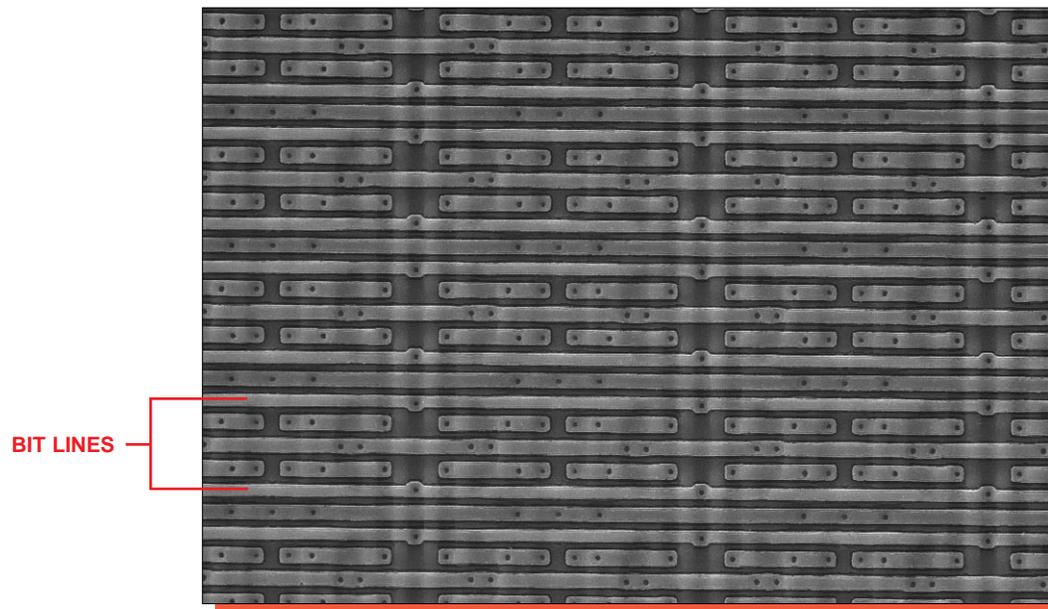


Mag. 20,800x

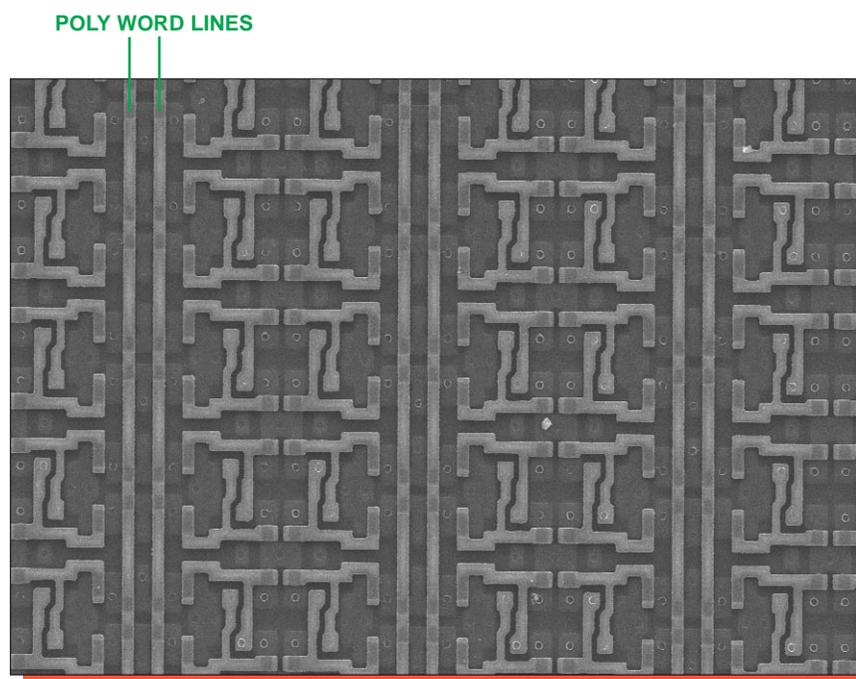


Mag. 36,600x

Figure 19. SEM section view illustrating birdsbeak.

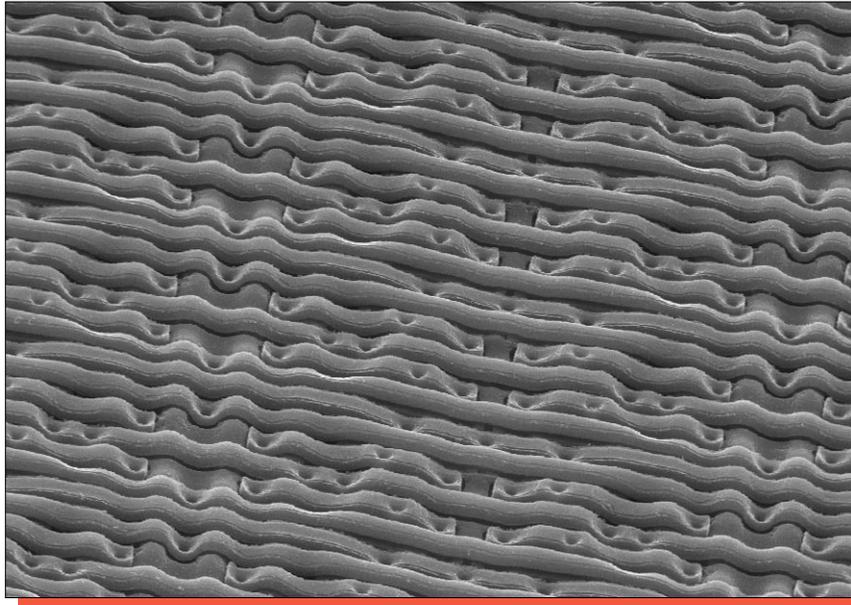


metal

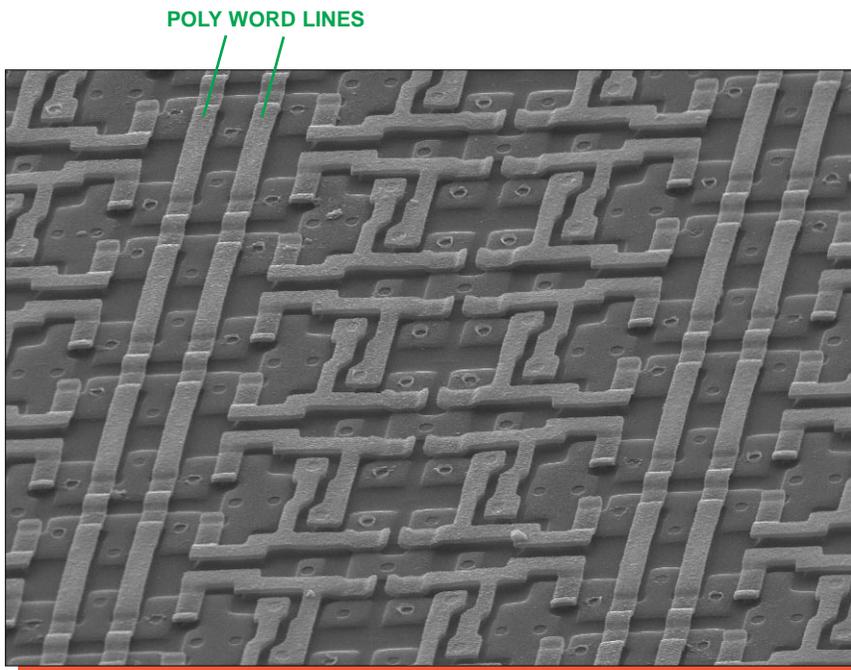


unlayered

Figure 20. Topological SEM views illustrating 6T SRAM array. Mag. 810x, 0°.

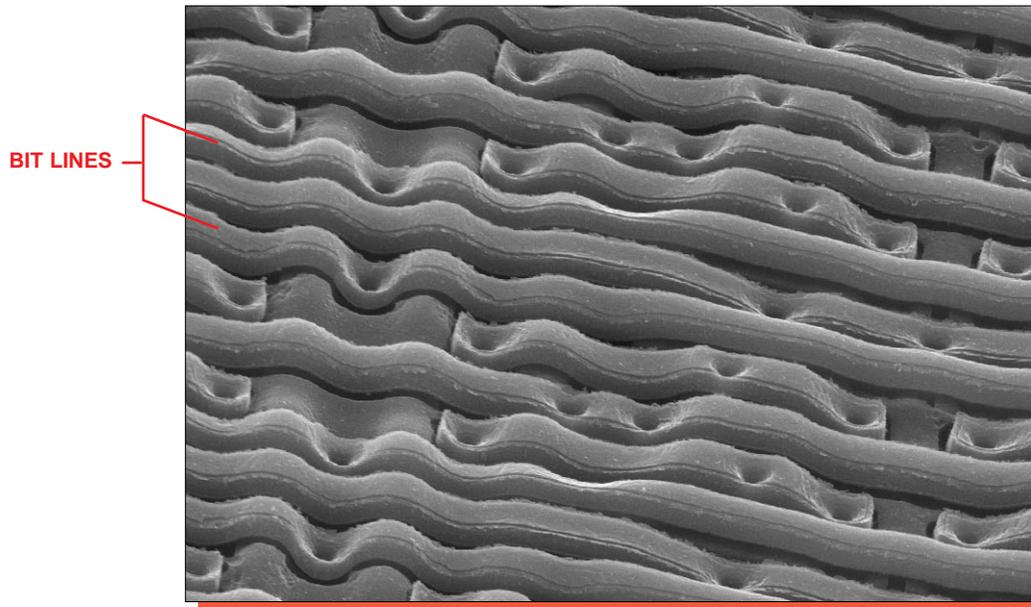


metal

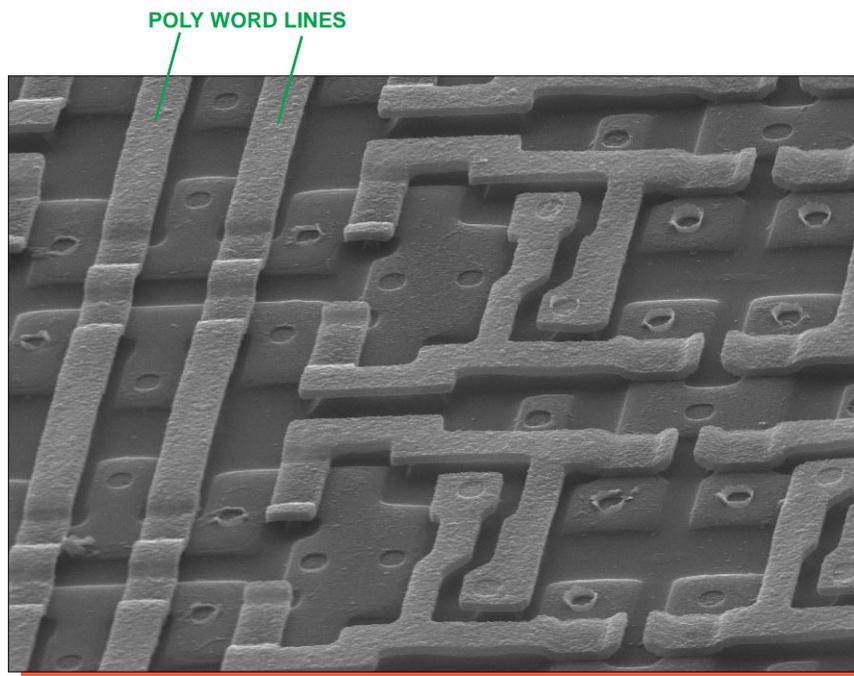


unlayered

Figure 21. Perspective SEM views illustrating 6T SRAM array. Mag. 1600x, 60°.



metal



unlayered

Figure 22. Perspective SEM views illustrating 6T SRAM array. Mag. 3240x, 60°.

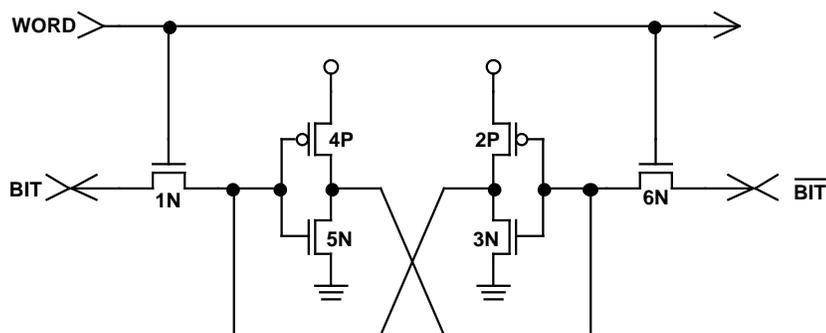
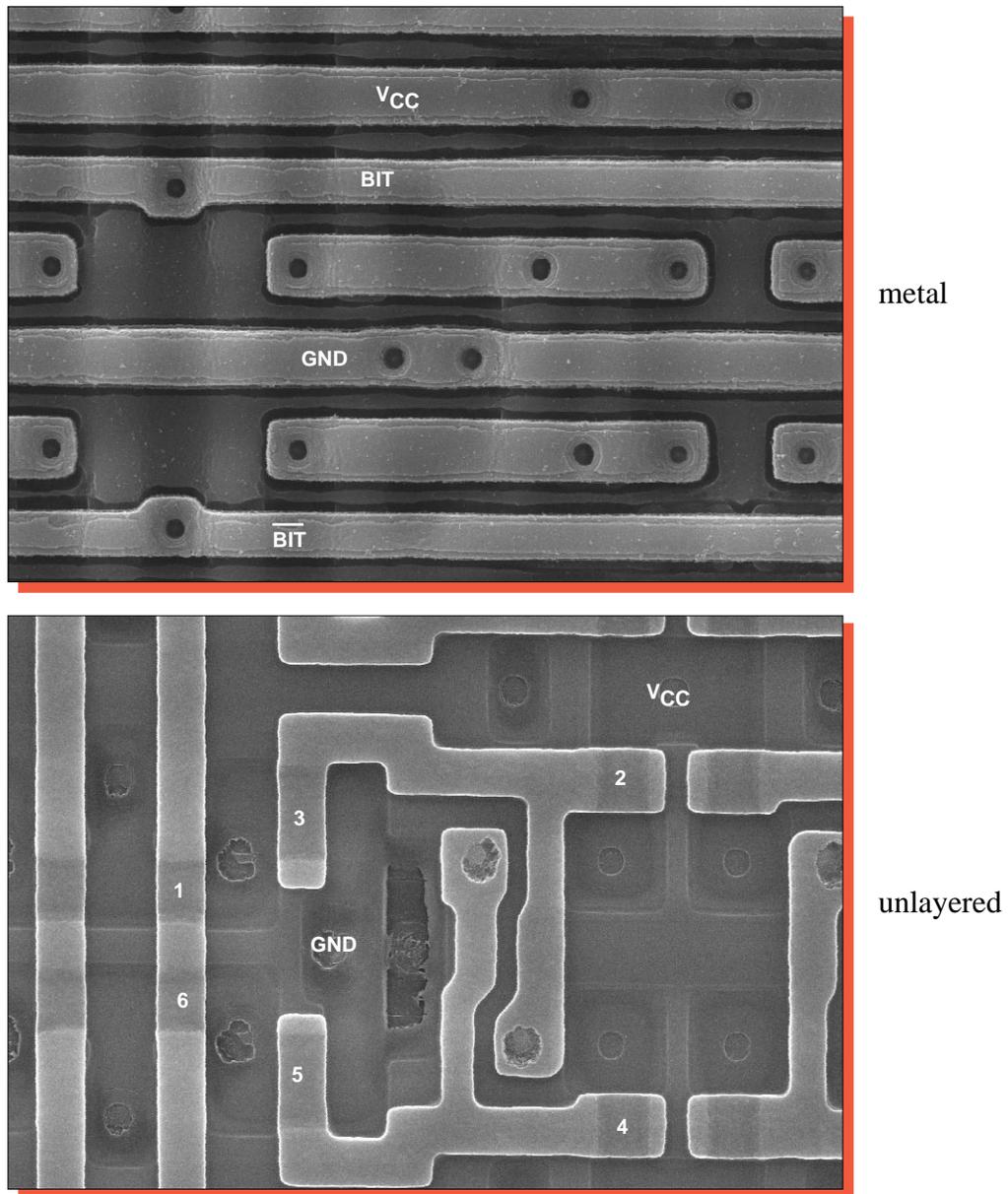
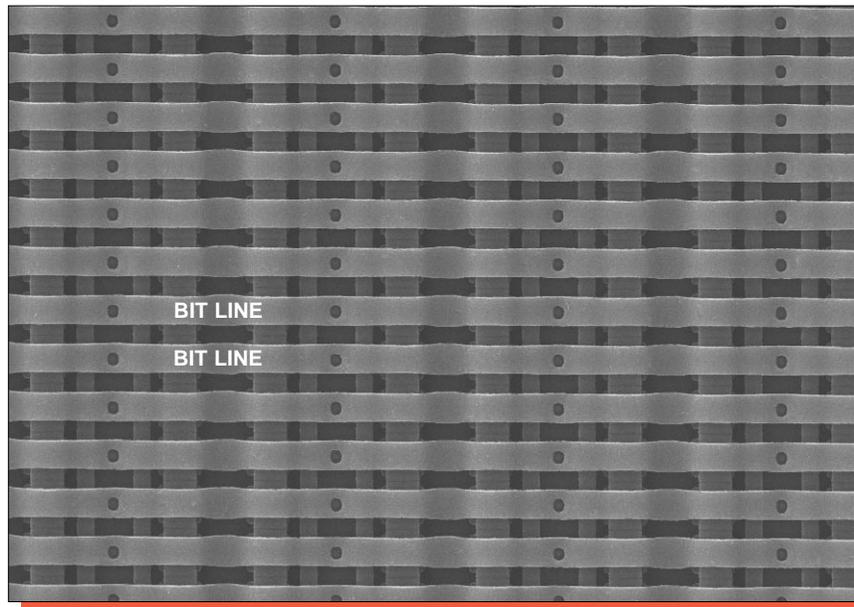
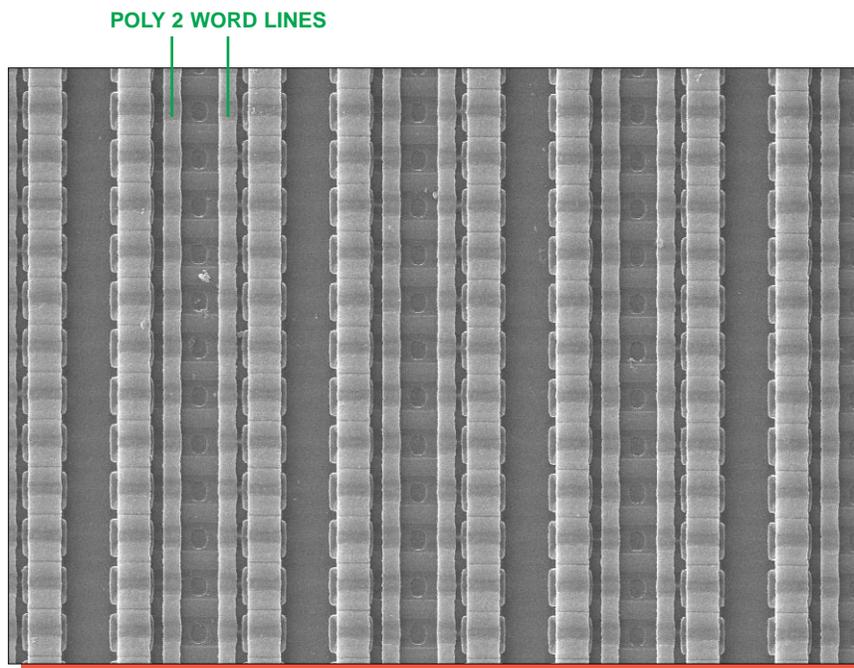


Figure 23. Perspective SEM views illustrating 6T SRAM cell and schematic.
Mag. 3200x, 0°.

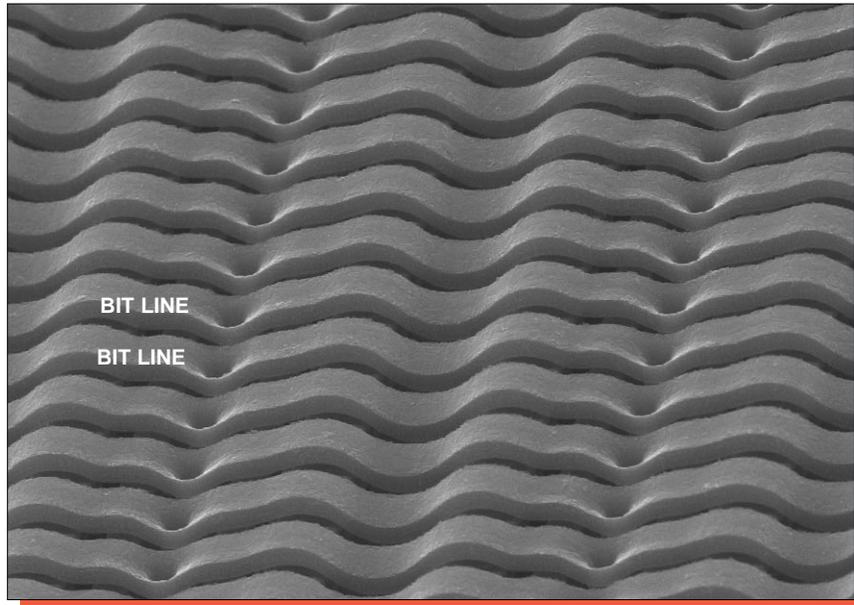


metal

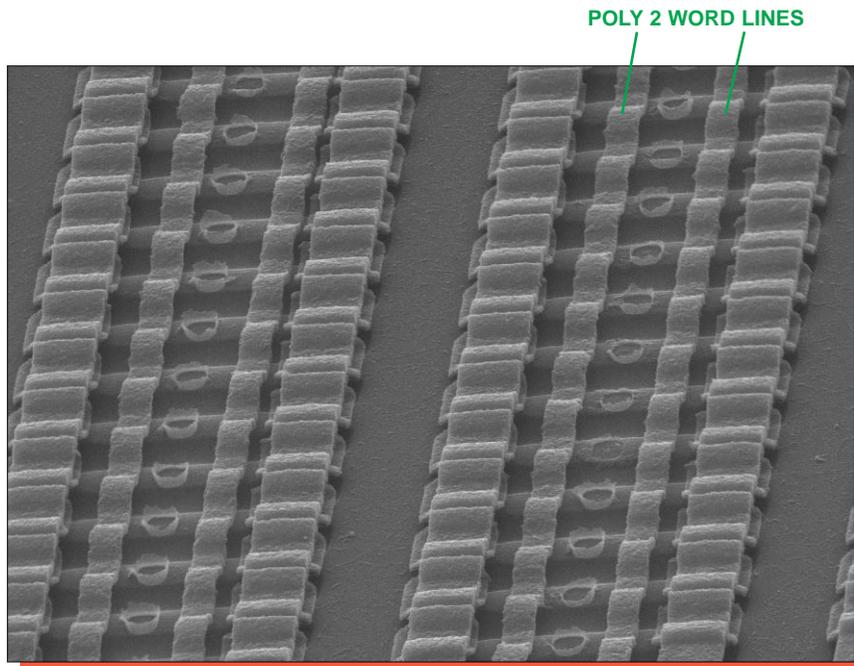


unlayered

Figure 24. Topological SEM views illustrating EEPROM array. Mag. 1620x, 0°.

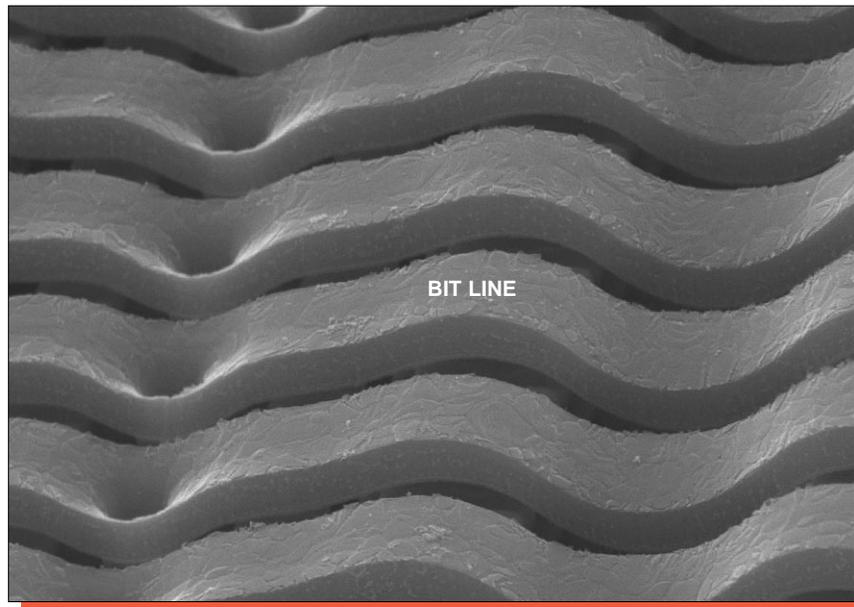


metal



unlayered

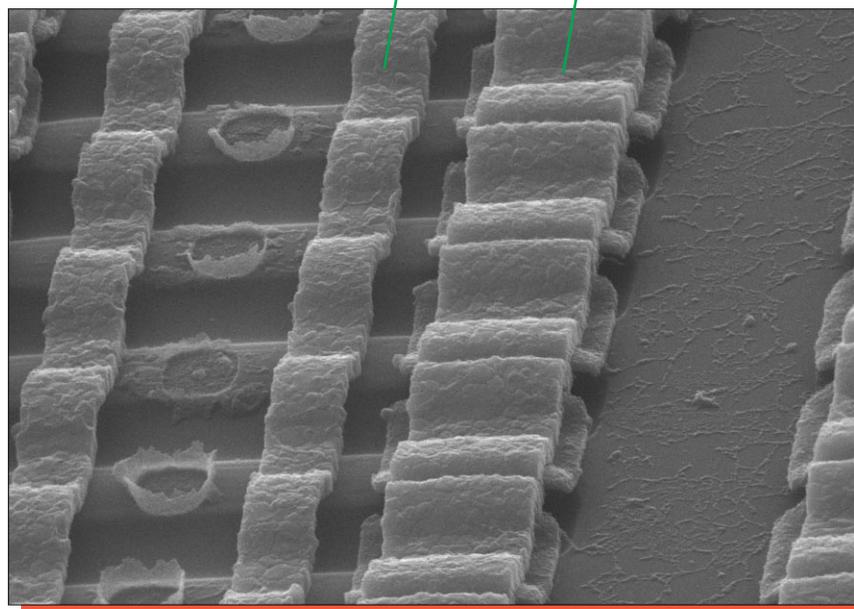
Figure 25. Perspective SEM views illustrating EEPROM array. Mag. 3240x, 60°.



metal

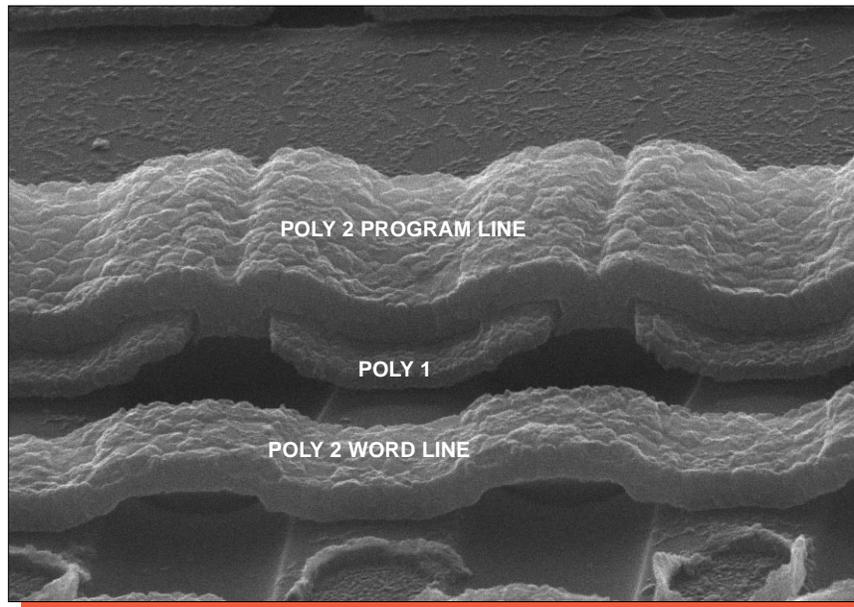
POLY 2
WORD
LINE

POLY 2
PROGRAM
LINE

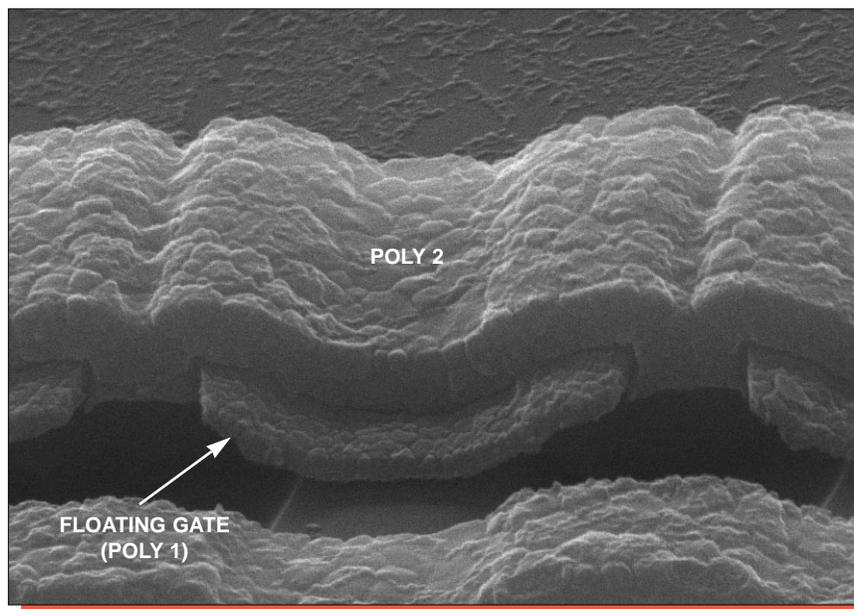


unlayered

Figure 26. Perspective SEM views illustrating EEPROM array. Mag. 8000x, 60°.



Mag. 13,000x



Mag. 20,000x

Figure 27. Perspective SEM views illustrating details of the EEPROM cell. Unlayered, 60°.

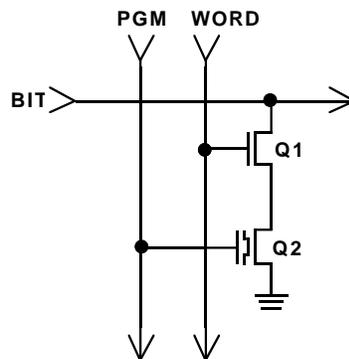
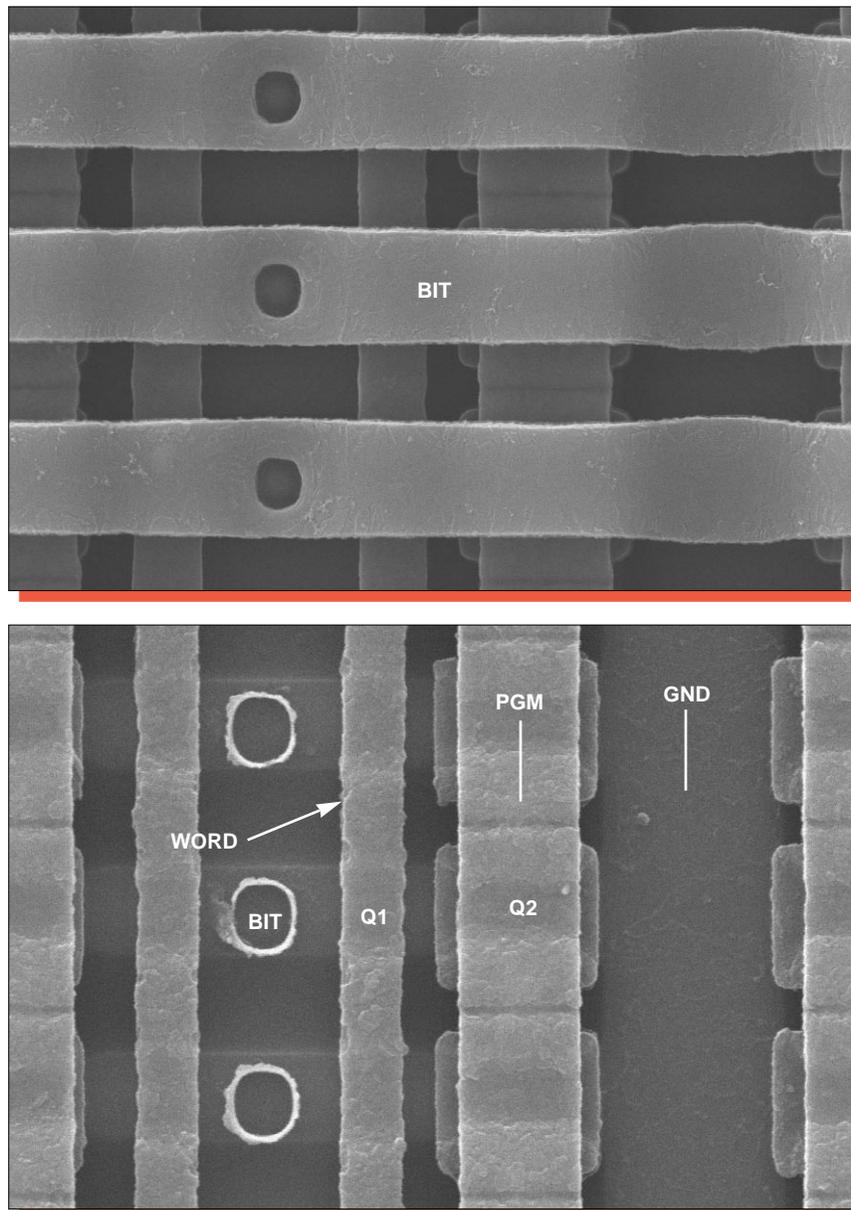


Figure 28. SEM views illustrating EEPROM cell and schematic. Mag. 6500x, 0°.

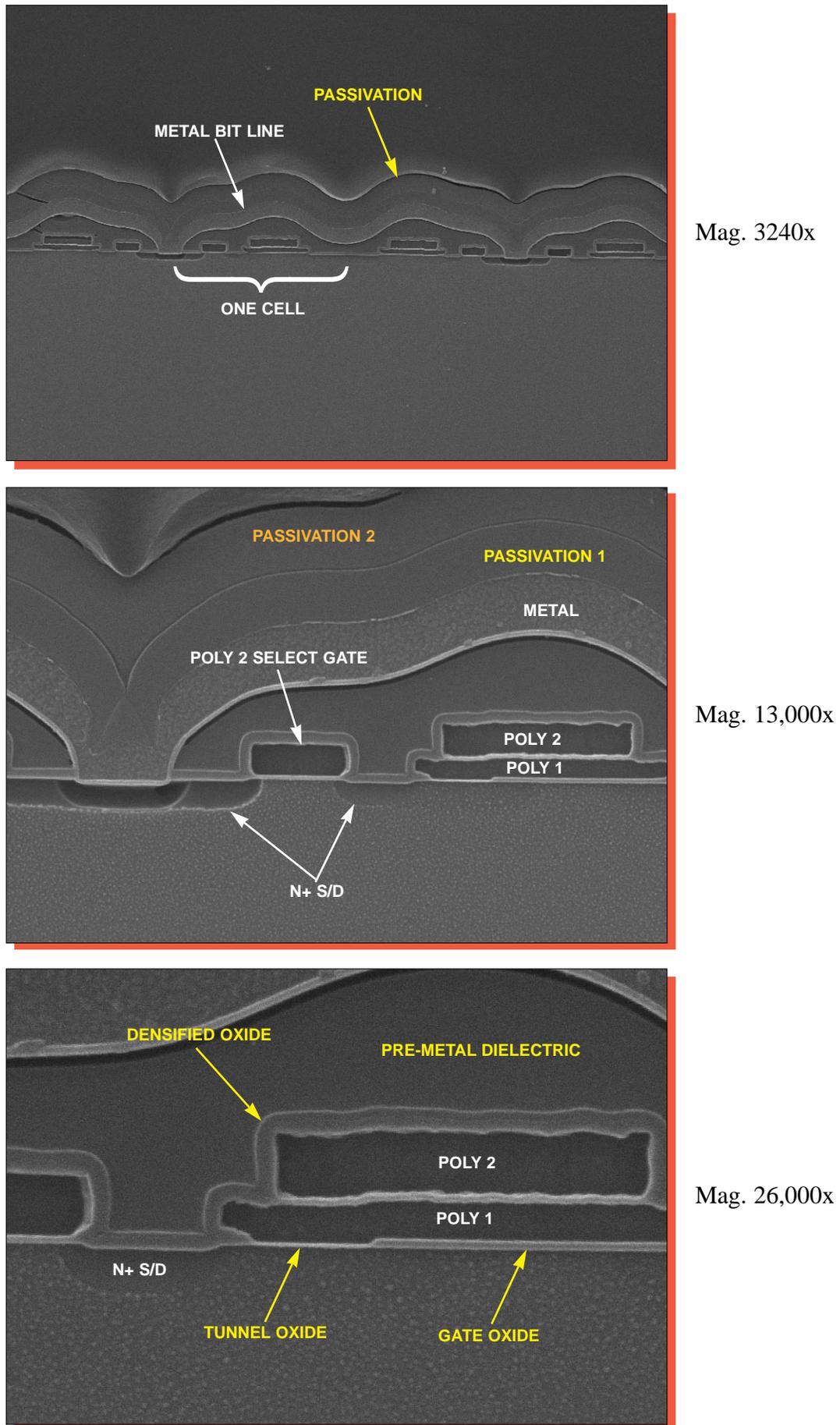
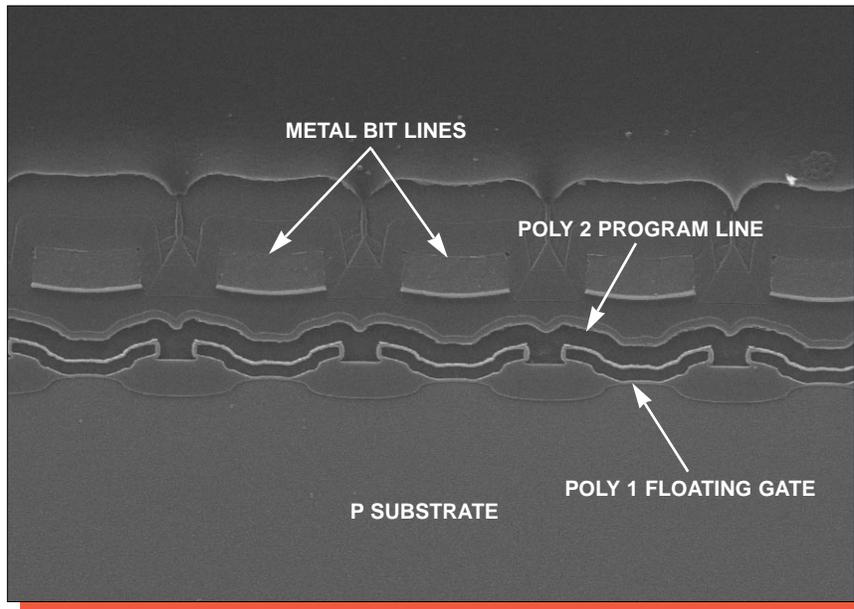
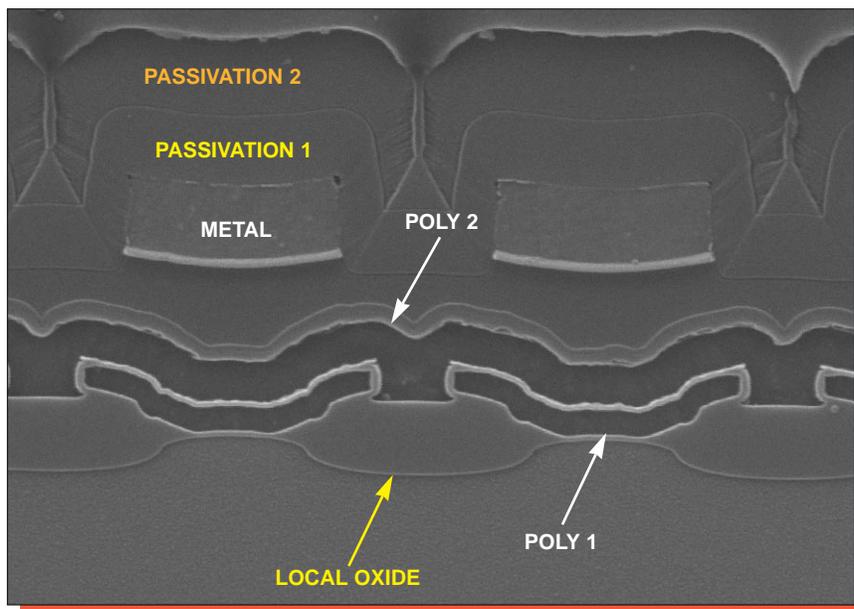


Figure 29. SEM cross section views of EEPROM cell (parallel to bit lines).

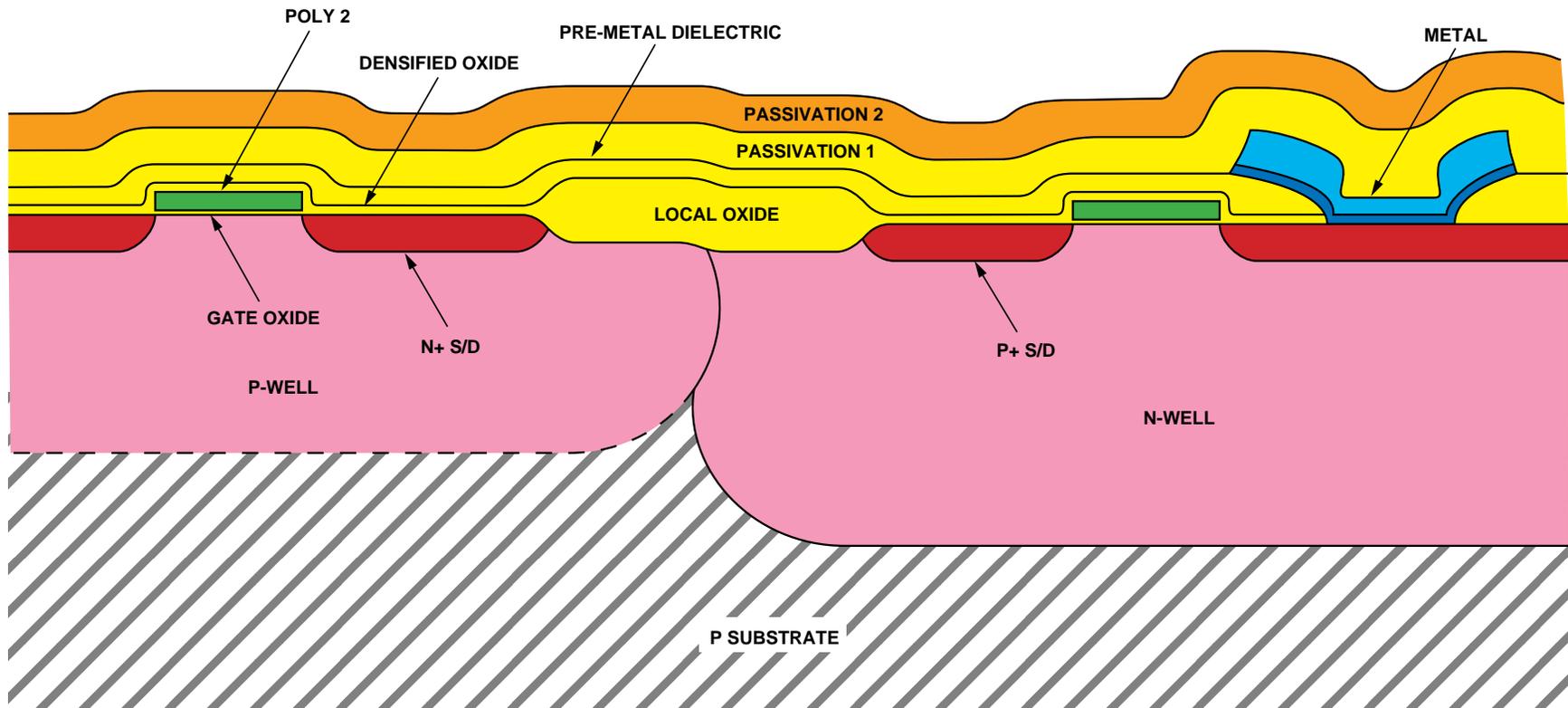


Mag. 6500x



Mag. 13,000x

Figure 30. SEM cross section views of EEPROM cell (perpendicular to bit lines).



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 31. Color cross section drawing illustrating device structure.

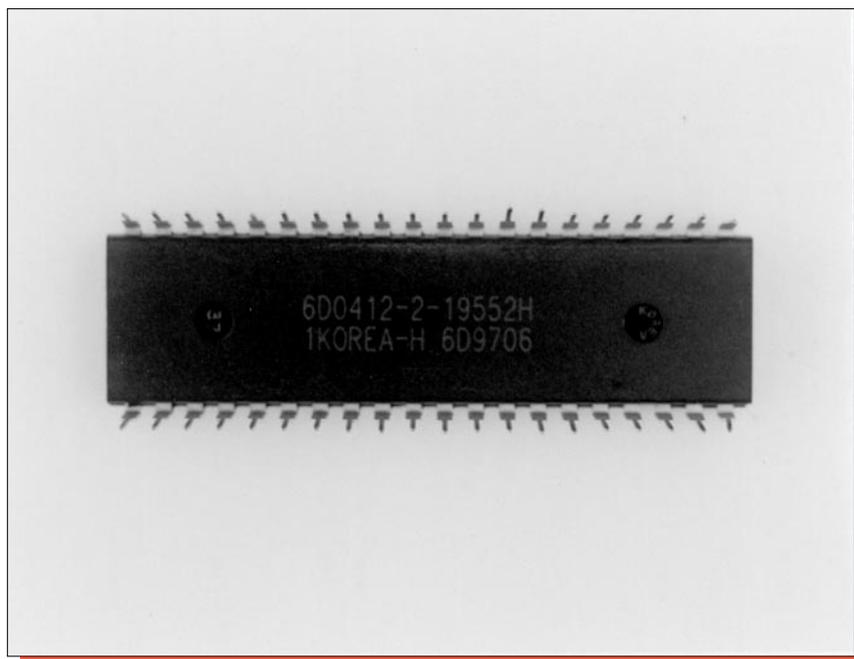
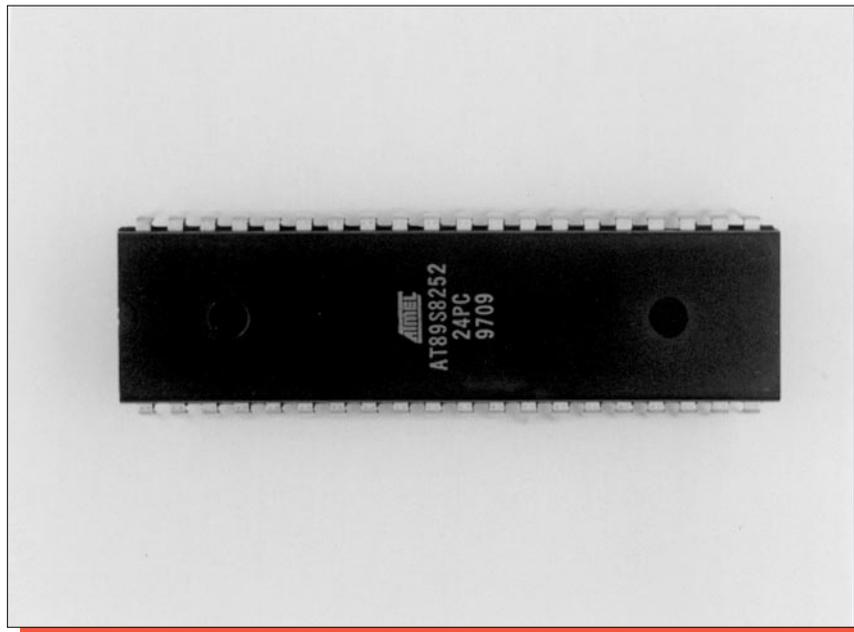


Figure 32. Package photographs of the Atmel AT89S8252. Mag. 1.7x.

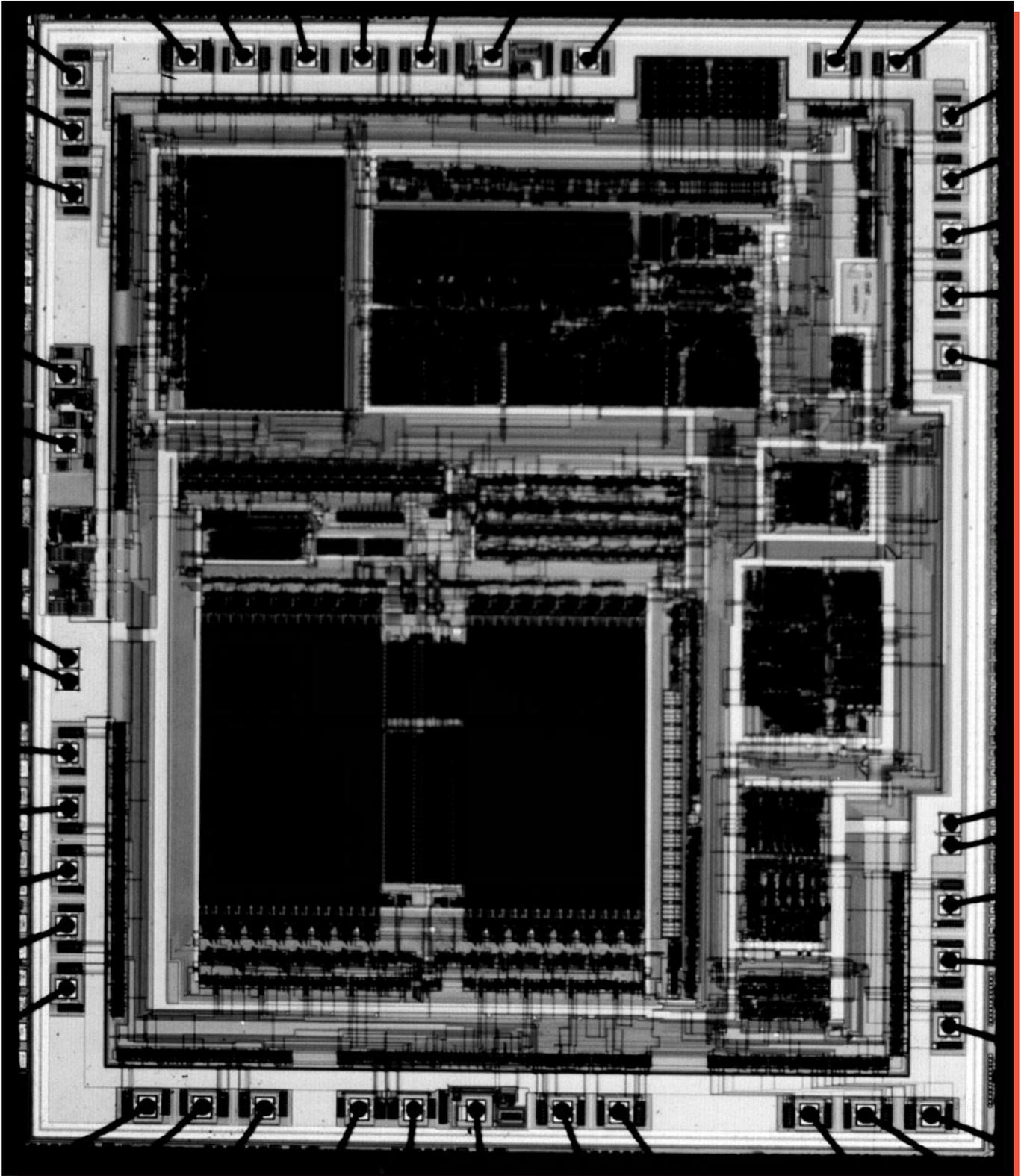
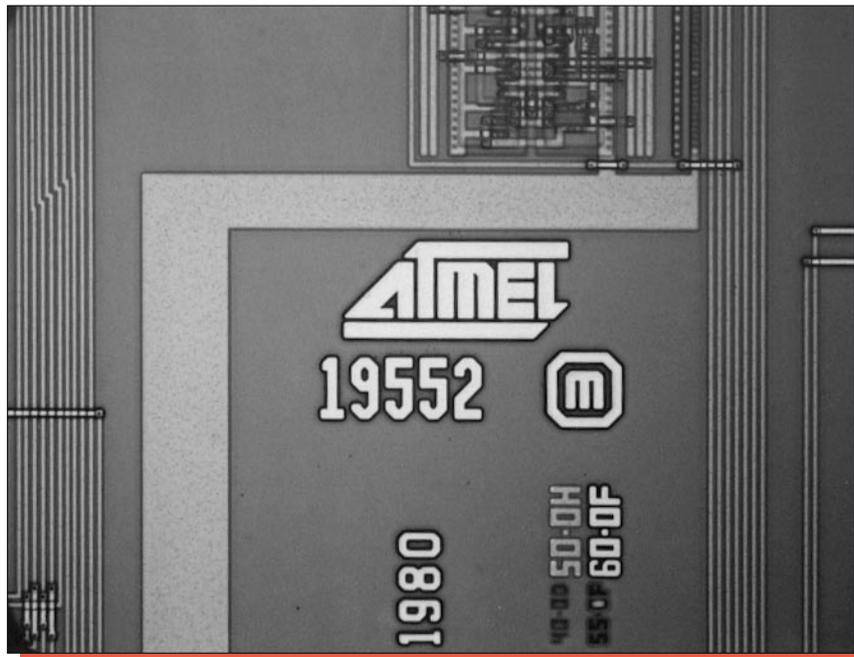
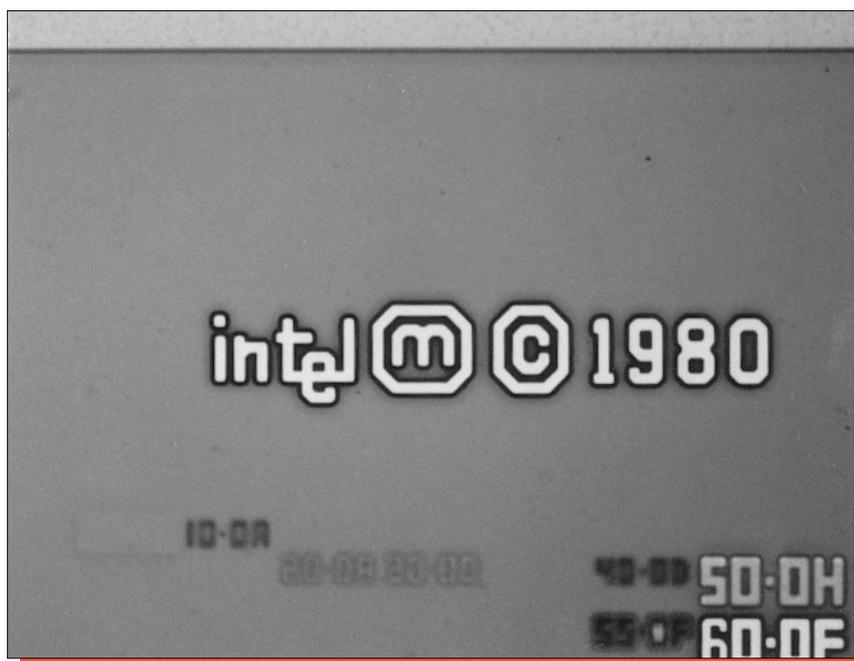


Figure 33. Whole die photograph of the Atmel AT89S8252. Mag. 44x.



Mag. 400x



Mag. 500x

Figure 34. Optical views illustrating markings on the die surface.

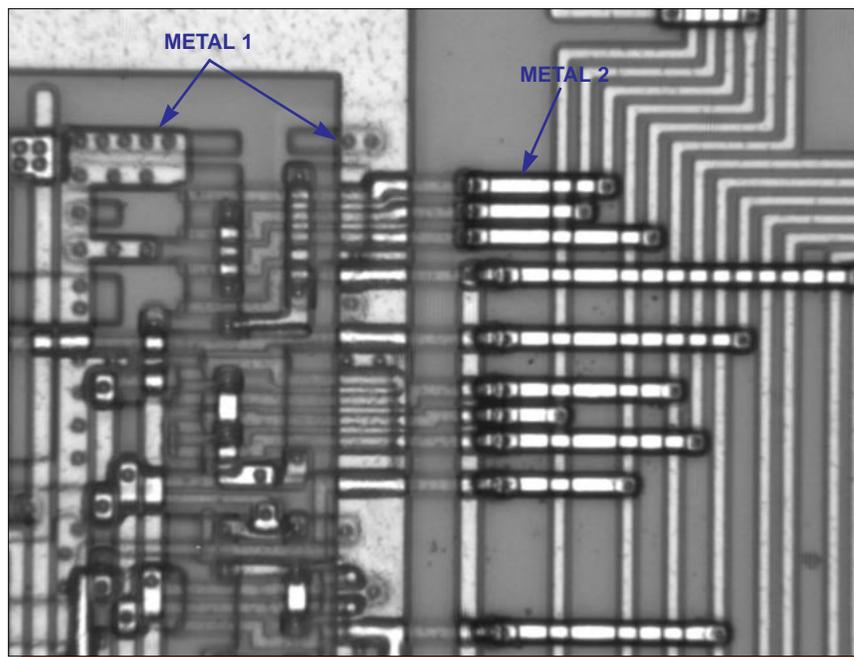
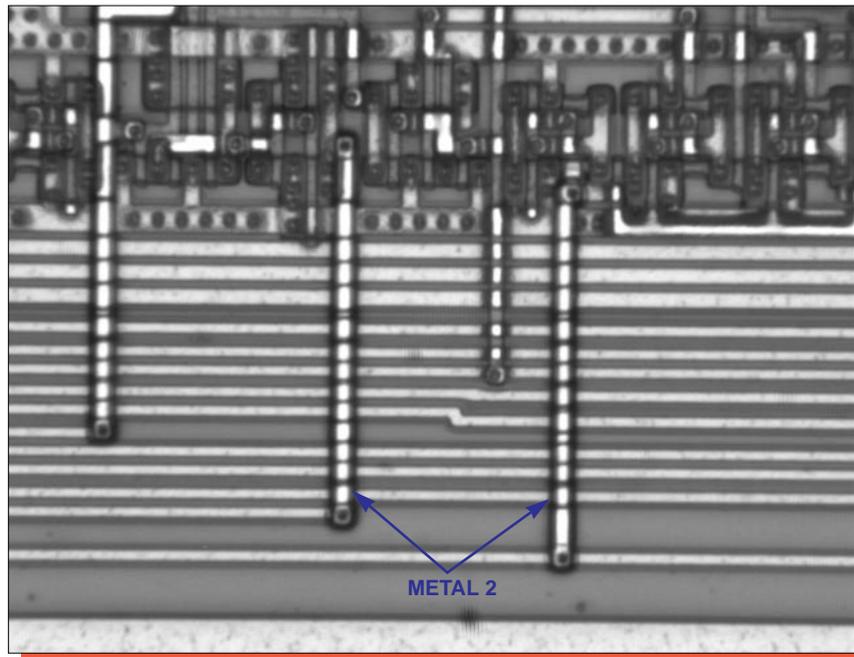
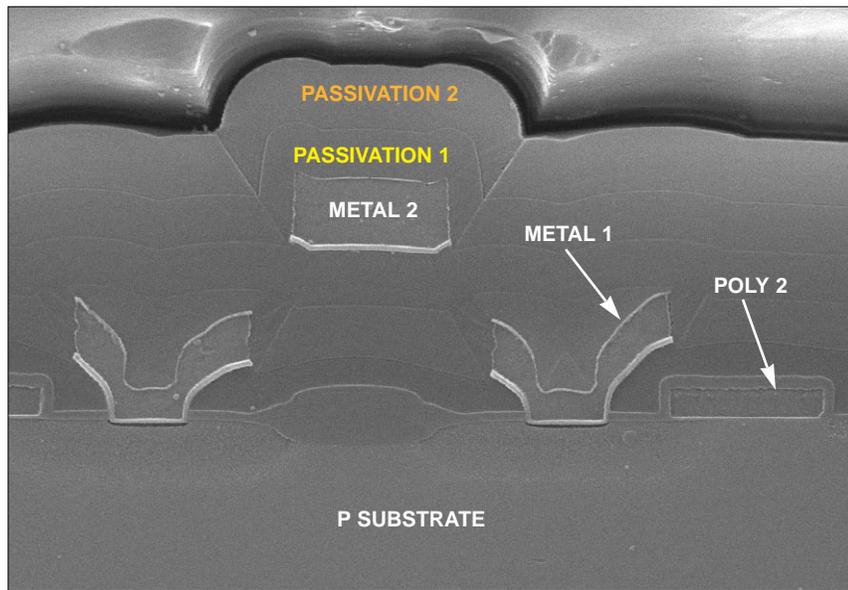
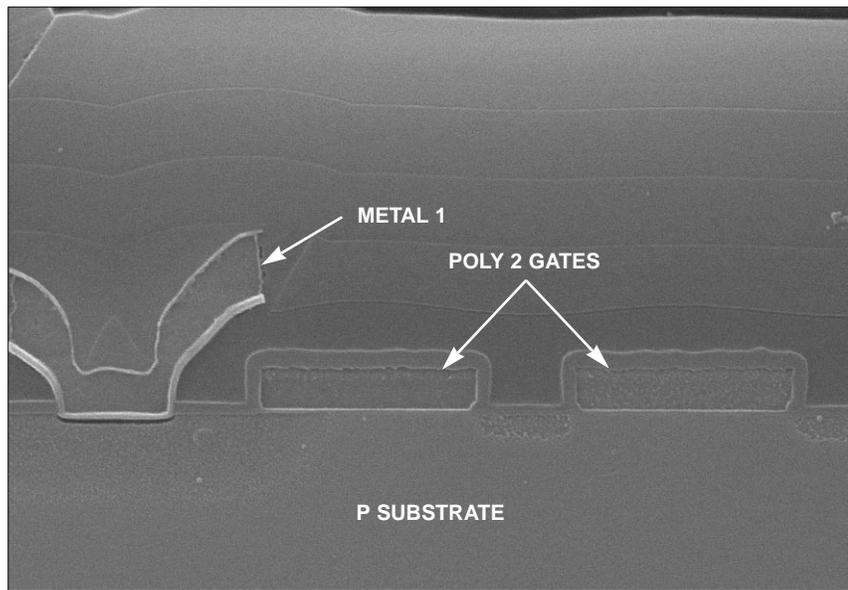


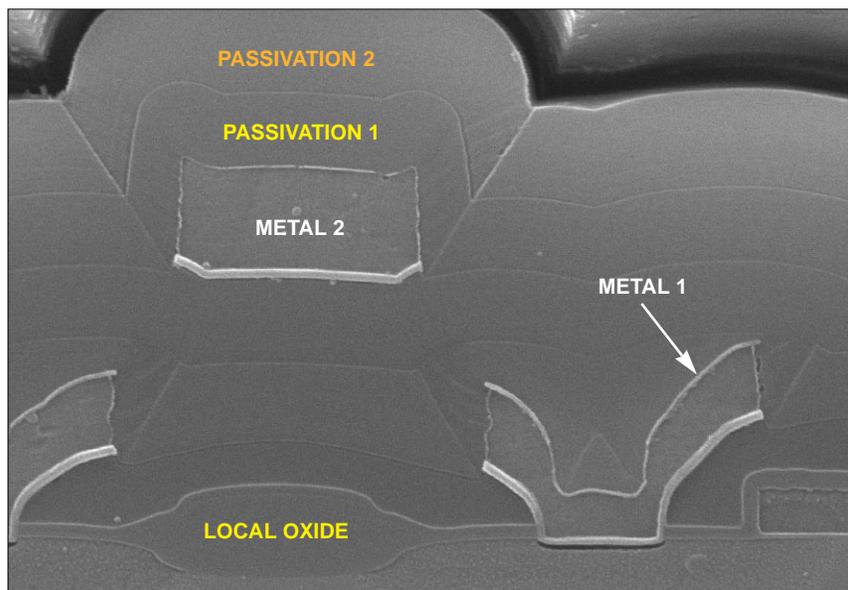
Figure 35. Optical views illustrating metal 2 interconnect. Mag. 825x.



Mag. 10,000x

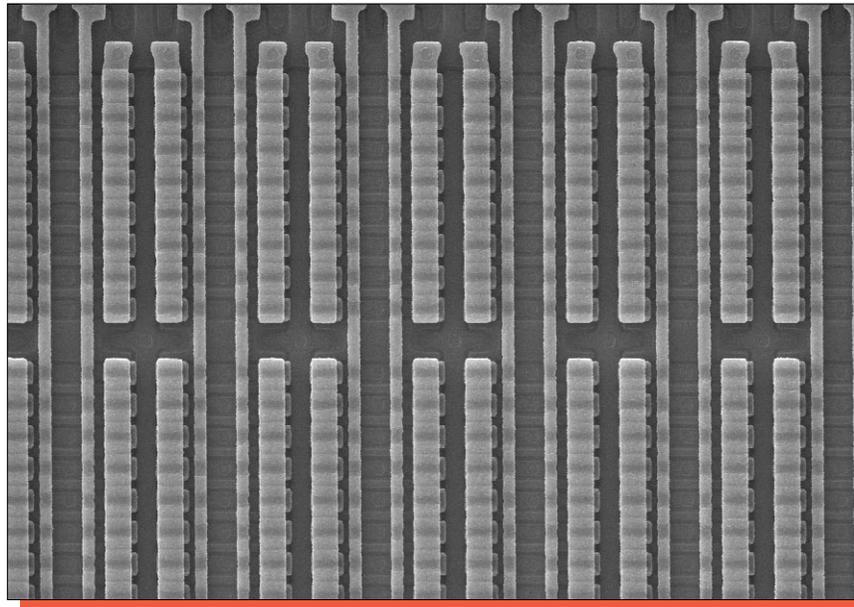


Mag. 13,000x

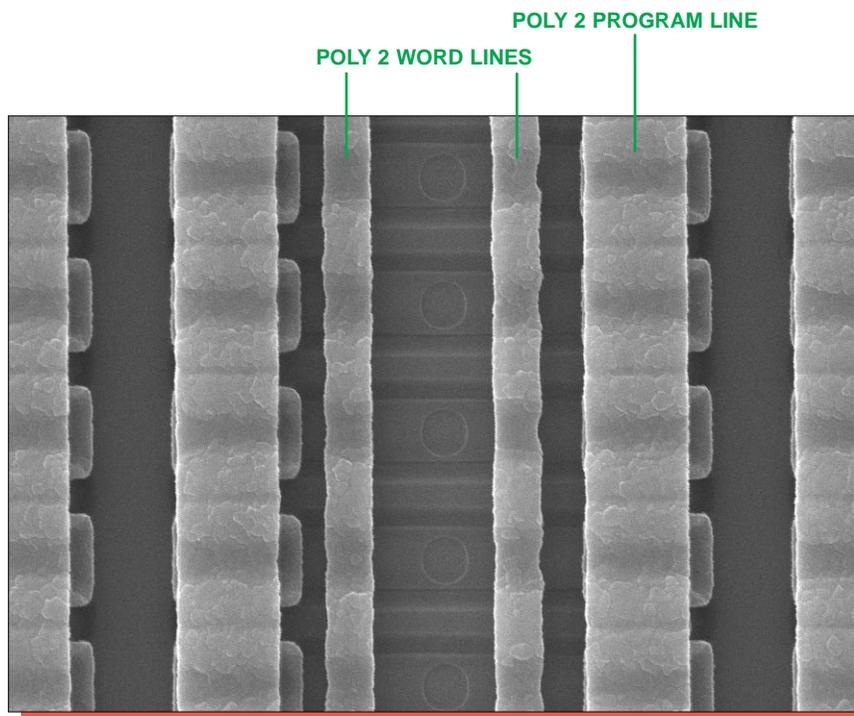


Mag. 15,000x

Figure 36. Glass etch section views illustrating general structure.

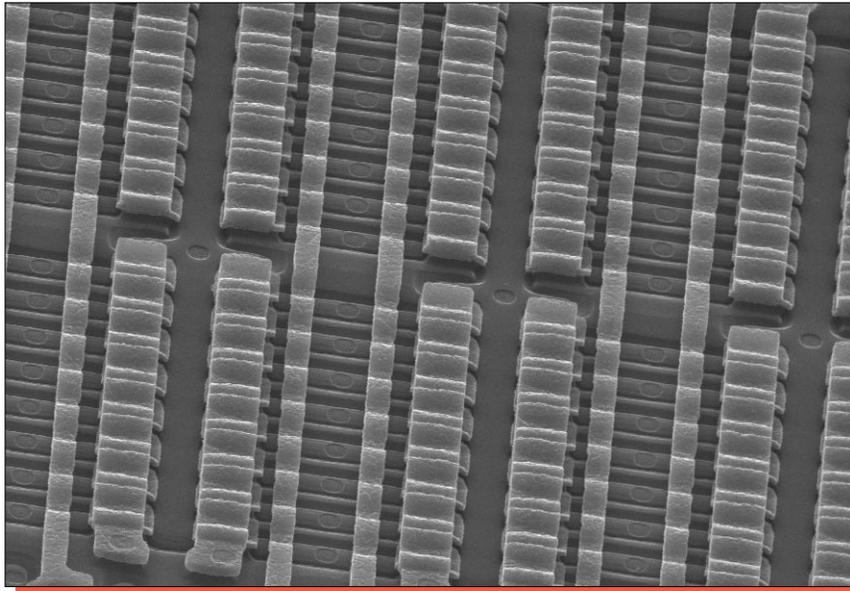


Mag. 1600x

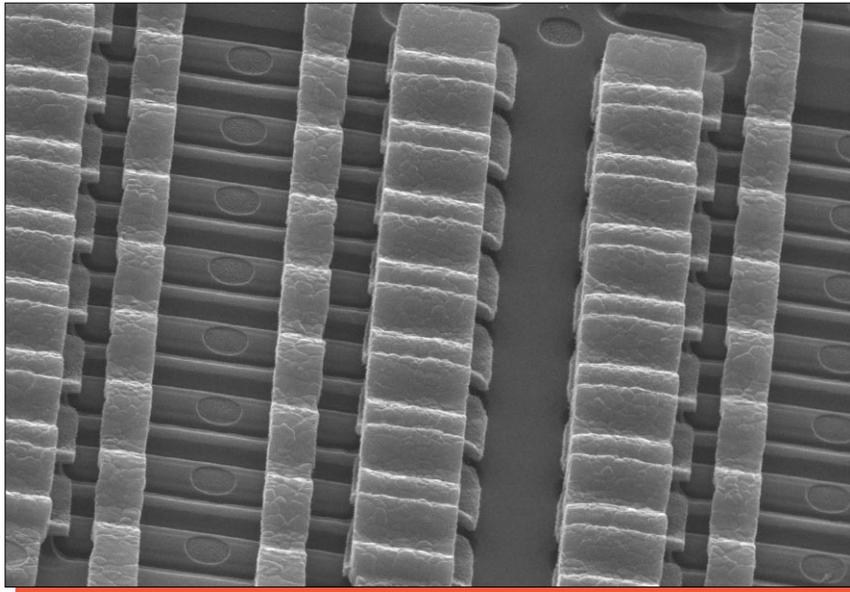


Mag. 6500x

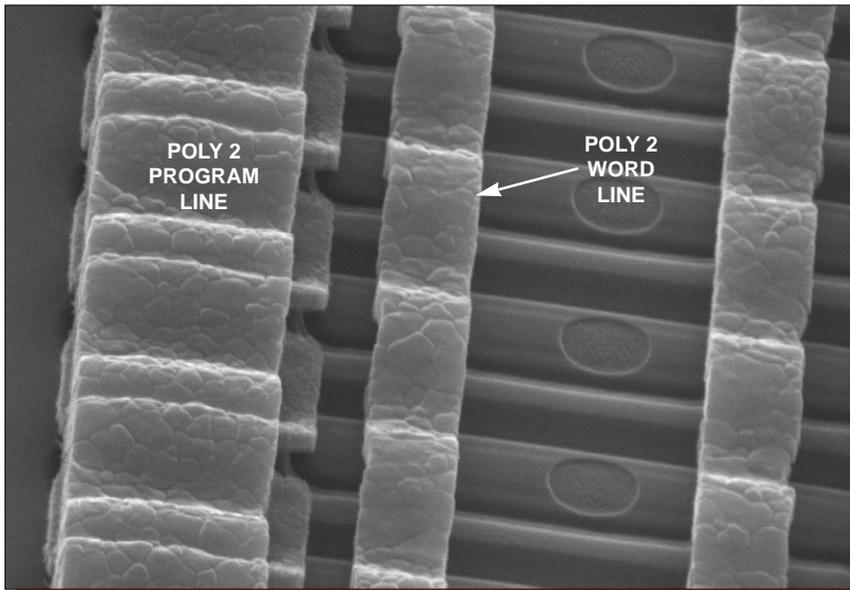
Figure 37. Unlayered topological views illustrating EEPROM array on the AT89S8252 device. 0°.



Mag. 3240x

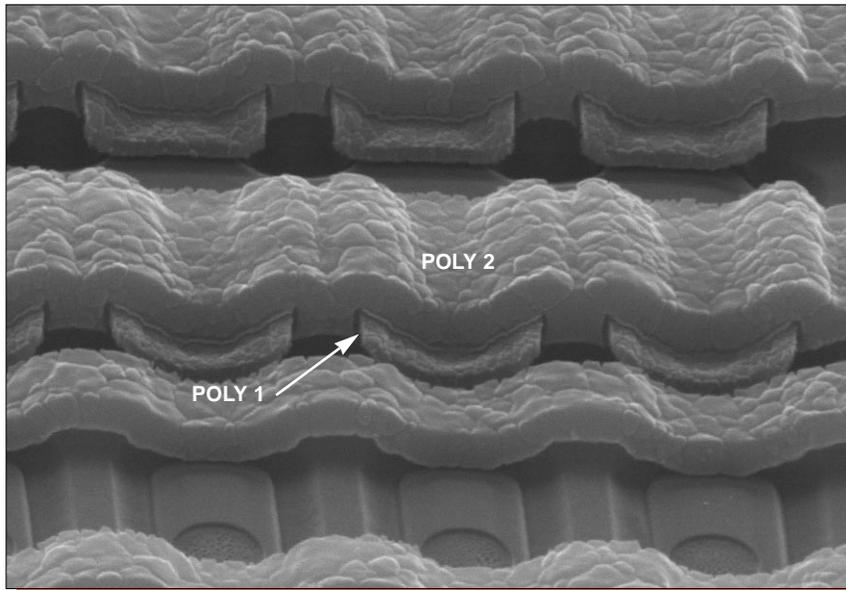


Mag. 6500x

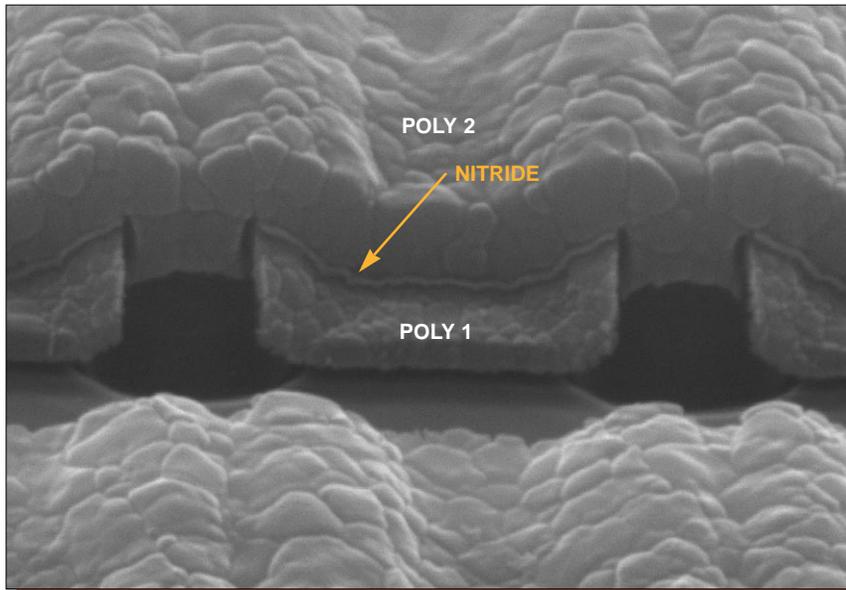


Mag. 13,000x

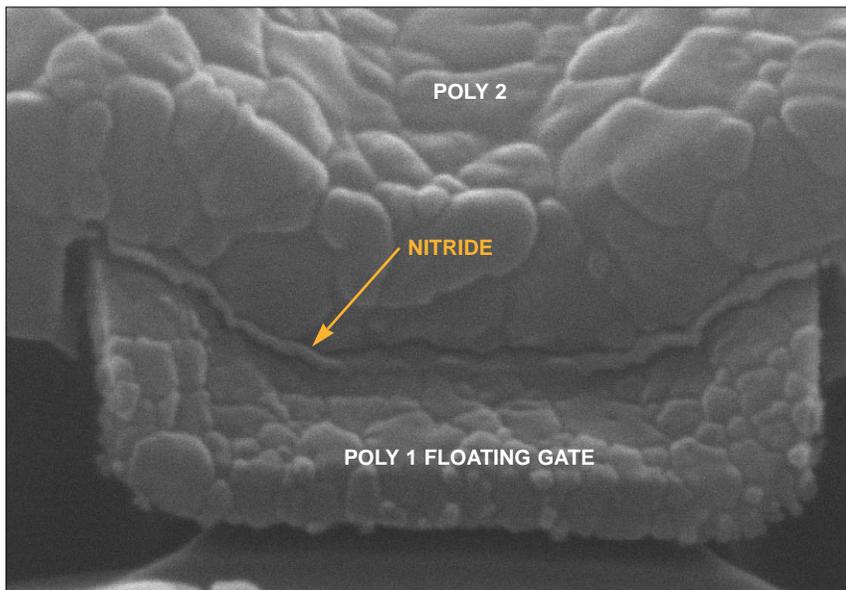
Figure 38. Perspective SEM views illustrating EEPROM array on the AT89S8252 device. 60°.



Mag. 13,000x

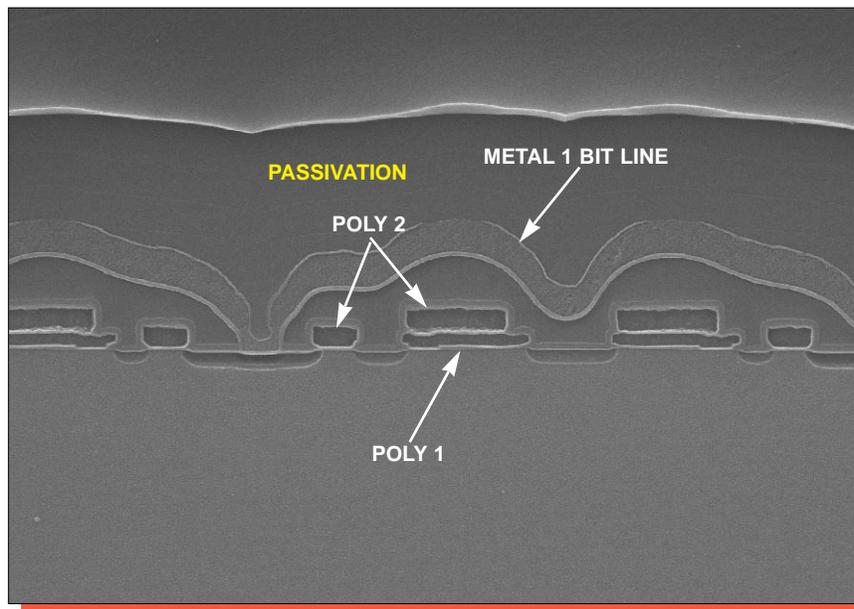


Mag. 26,000x

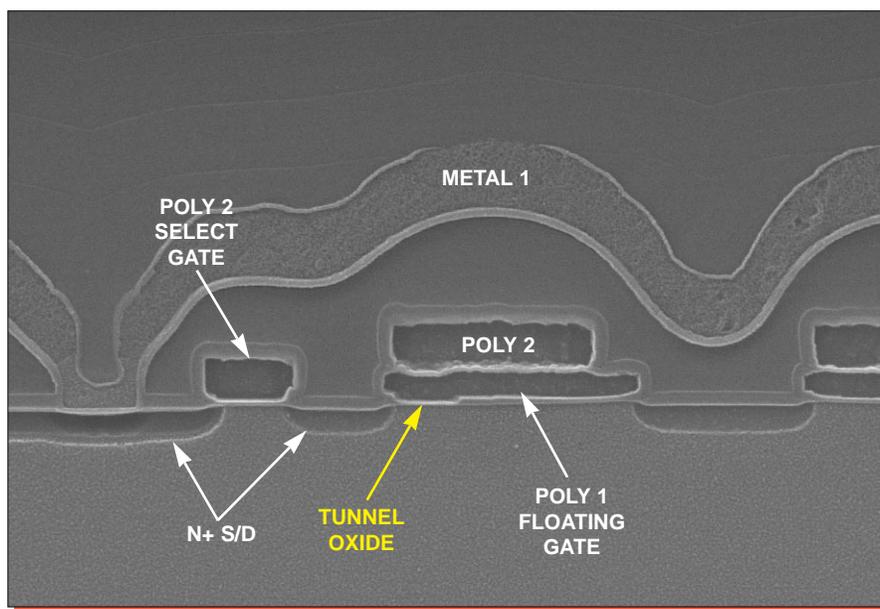


Mag. 52,000x

Figure 39. Detailed views of the EEPRM cell.

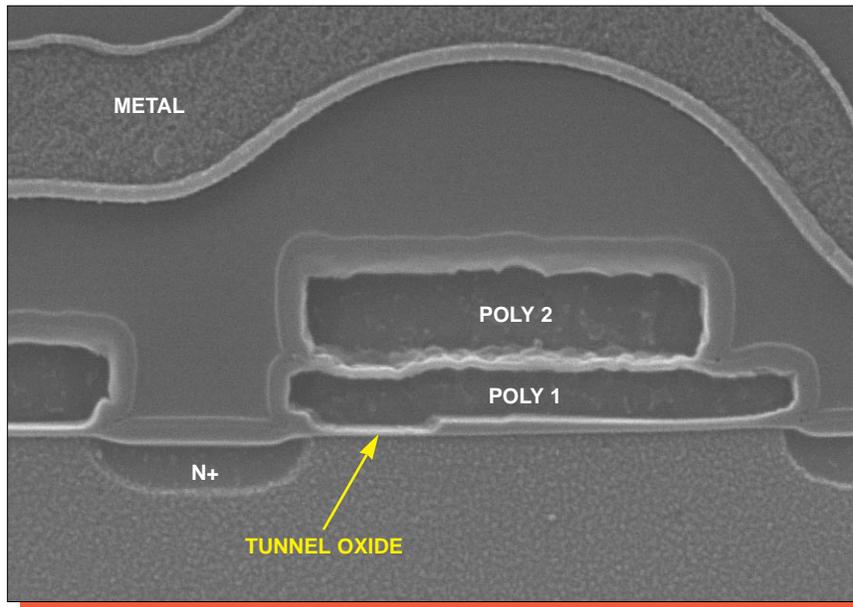


Mag. 6500x

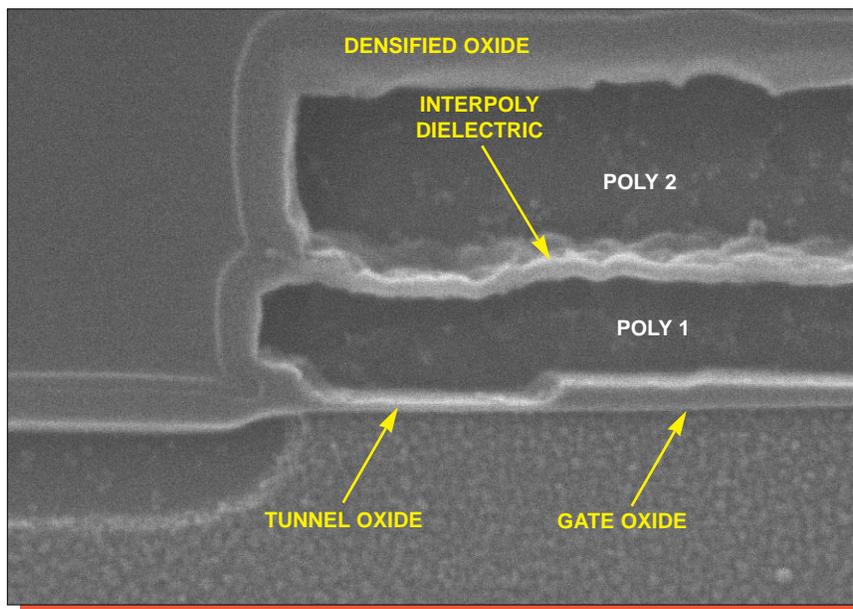


Mag. 13,000x

Figure 40. SEM section views of EEPROM cell on the AT89S8252 device (parallel to bit lines).



Mag. 26,000x



Mag. 52,000x

Figure 41. Detailed SEM section views of EEPROM cell (parallel to bit lines).

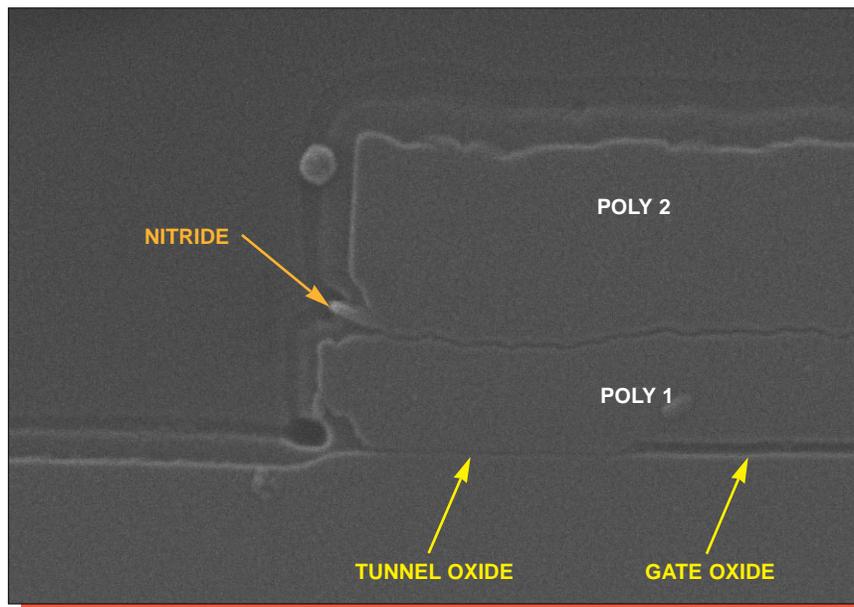
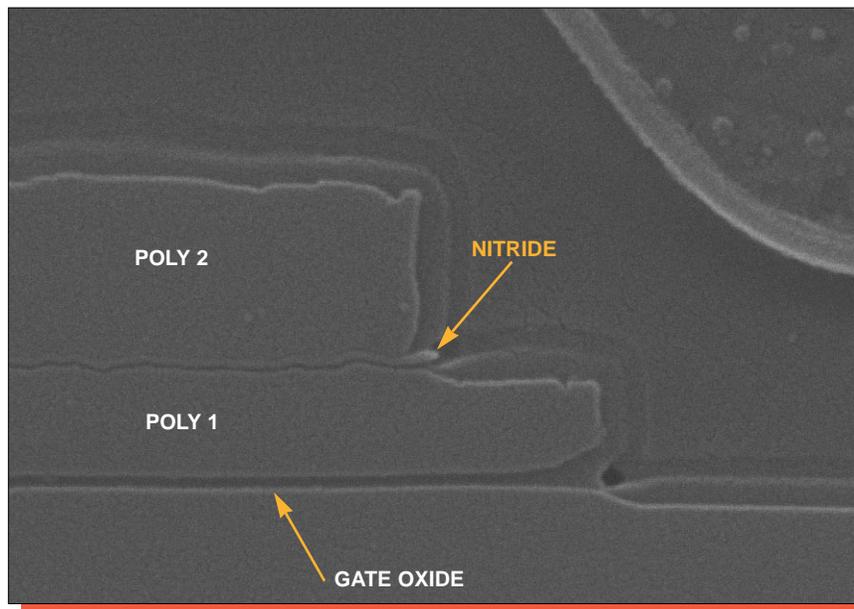


Figure 42. Glass etch section views illustrating the ONO interpoly dielectric.
Mag. 52,000x.