

Construction Analysis

Advanced Micro Devices 200MHz K6 Microprocessor

Report Number: SCA 9706-541



INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the AMD 200MHz K6 Microprocessor with MMX technology. Two samples were used for the analysis. The devices were received in 321-pin CPGA packages date coded 9713.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

- Six metal, N-epi, CMOS process.
- Metal 1 (tungsten) was defined by a damascene process. Stacked vias were employed.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 321-pin ceramic pin grid arrays (CPGA). An aluminum lid was employed on the top of the package. The die was mounted surface down on the ceramic substrate (C4 flip-chip assembly). The package contained nine internal levels of interconnect.
- Nine decoupling capacitors were present on top of the ceramic (inside the package).
- A blue colored underfill was present between the die surface and the ceramic substrate. A gray heat conductive grease was employed between the backside of the die and the metal lid.
- External pins were plated with gold over nickel and were brazed to the package.
- Solder balls were employed for all connections to die metallization (C4 flip-chip process).
- Sawn dicing (full depth).

Die Process:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process employing twin wells in an apparent N-epi on an N substrate.
- Die coat: A thin patterned polyimide die coat was present over the entire die.
- Final passivation: A layer of nitride over two layers of glass.
- Metallization: Six levels of metal defined by dry-etch techniques (except M1). Metal 1 (tungsten) was defined by a damascene process. Metals 2 - 6 consisted of copper-doped aluminum. Metal 6 appeared to employ a very thin aluminum-oxide cap. Metals 2 - 5 employed titanium-nitride caps. There appeared to be evidence of very thin titanium adhesion layers under all metals. Tungsten plugs were employed for vias under metals 2 - 5. Metal 6 used standard vias. All tungsten plugs and

TECHNOLOGY DESCRIPTION (continued)

tungsten metal 1 were lined with titanium-nitride. Stacked vias were employed at all levels.

- Interlevel dielectrics: Interlevel dielectrics 2 - 5 used the same dielectric structure. A very thin glass was deposited first, followed by an SOG (spin-on-glass) followed by a thick layer of glass. The third layer of glass was planarized by CMP which left the surface very planar. No CMP was performed directly under metal 6. Interlevel dielectric 1 (between M1 and M2) consisted of a single thick layer of glass which had also been subjected to CMP.
- Pre-metal glass: A thick layer of glass over a thin nitride. This dielectric was also planarized by CMP.
- Polysilicon: A single layer of dry-etched polycide (poly and titanium-silicide). This layer was used to form all gates on the die. Oxide sidewall spacers were used to provide the LDD spacing.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Titanium was sintered into the diffusions (salicide process).
- Isolation: Field oxide isolation consisted of oxide-filled shallow-trench isolation. It was very planar with the diffused silicon surfaces.
- Wells: Twin-wells in a N-epi on a N substrate.
- SRAM: On-chip Level 1 data and instruction cache memory cell arrays (32KByte each) were employed. The memory cells used a 6T CMOS SRAM cell design. Metal 4 distributed Vcc and GND and formed “piggyback” word lines (via metals 1 - 3). Metal 3 formed the bit lines and metal 2 distributed GND and Vcc throughout the cells and was used as cell interconnect. Metal 1 also provided cell interconnect. Polycide formed the select and storage gates. Cell pitch was 4.5 x 7 microns (31.5 microns²).
- No redundancy fuses were found.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 8

Questionable Items:¹ None.

Special Features:

- CPGA with metal lid.

General items:

- The devices were packaged in 321-pin ceramic PGA packages. An aluminum lid/heat dissipater was employed. It was attached to the ceramic substrate with a silicone-type adhesive. The die was mounted surface down on the ceramic (flip-chip assembly). The PGA contained nine molybdenum internal interconnect levels. Vias between trace levels were also formed with molybdenum. Nine ceramic chip capacitors were present inside the package.
- Overall package quality: Good. No defects were found on the external or internal portions of the packages. External pins (iron-nickel-cobalt) were straight and placement was good. No voids were noted in the silver-copper solder. External plating of the pins was of good quality (gold over nickel).
- Die connections: Lead solder balls were used for connections to the die (C4 process). Ball placement was good. Die pad structure consisted of tin-copper with a lead-chromium barrier. Ball pitch was 14.5 mils (0.34mm). There were a total of 682 solder balls present on the die. A blue colored underfill was present between the die and the ceramic substrate. No voids were noted in this material. A gray heat conductive grease was used between the backside of the die and the lid for a thermal transfer.
- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 9 - 52

Questionable Items:¹ None.

Special Features:

- Six metal, N-epi, CMOS process.
- Metal levels 2 - 5 employed tungsten via plugs. Metal 1 was defined by a damascene process. Stacked vias were employed at all levels.
- Chemical-mechanical-planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium silicided diffusion structures.

General Items:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process employing twin-wells in an apparent N-epi on an N substrate. No problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Die coat: A patterned polyimide die coat was present over the entire die surface.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II (continued)

- Final passivation: A layer of nitride over two layers of glass. Coverage was good. Edge seal was also good as the passivation extended to the scribe lane to seal the metallization.
- Metallization: Six levels of metal interconnect. Metals 2 - 6 consisted of copper-doped aluminum. Metals 2 - 5 employed titanium-nitride caps. Metal 6 apparently employed a thin aluminum-oxide cap. There appeared to be evidence of very thin titanium adhesion layers under all metals. Tungsten plugs were employed with metals 2 - 5. Standard vias were employed under metal 6. All plugs were lined with titanium-nitride underneath and the presumed adhesion layer over top. Metal 1 consisted of tungsten defined by a damascene process. The metal 1 tungsten was also lined with titanium-nitride and an apparent titanium adhesion layer.
- Metal patterning: All aluminum metal levels were defined by a dry etch of good quality. Metal lines were not widened at via connections.
- Metal defects: None. No voiding, notching or cracking of the metal layers was found. No silicon nodules were found following removal of the metal layers.
- Metal step coverage: Metal 6 thinned up to 85 percent at vias. Although the thinning exceeds MIL-STDs (70 percent) it is not considered a serious reliability concern. No metal thinning was present at the connections to the tungsten via plugs or metal 1. The absence of thinning is due to the good control of plug height and the planarization technique employed.
- Vias and contacts: All via and contact cuts were defined by a dry etch of good quality. Again, alignment of the metals and plugs was good. Metal 2 tungsten plugs “spilled over” one edge of the tungsten metal 1. IBM uses this “borderless” contact technique for improved contact resistance. Vias and contacts were placed directly over one another (stacked vias). No problems were noted.
- Interlevel dielectrics: Interlevel dielectrics 2 - 5 consisted of the same type of oxide structure. A very thin glass was deposited first, followed by an SOG and a thick layer of glass. The thick layer of glass was subjected to CMP which left the surface very planar. No CMP was performed on ILD 5 (under metal 6). Interlevel

ANALYSIS RESULTS II (continued)

dielectric 1 consisted of a single thick layer of glass which had also been subjected to CMP. No problems were found with any to these layers.

- Pre-metal glass: A thick layer of silicon-dioxide over a thin nitride. This layer was also planarized by chemical-mechanical-planarization. No problems were found.
- Polysilicon: A single level of polycide (poly and titanium-silicide) was used. It formed all gates and word lines in the array. Definition was by dry etch of good quality. Oxide sidewall spacers were used throughout and left in place. No problems were found.
- Isolation: The device used oxide-filled shallow-trench isolation which was quite planar with the silicon surface. No problems were present.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Titanium was sintered into the diffusions (salicide process) to reduce series resistance. An LDD process was used employing oxide sidewall spacers. No problems were found.
- Wells: Twin-wells were used in what we believe to be an N-epi on an N substrate. Definition was normal.
- Buried contacts: Direct poly to diffusion contacts were not used.
- SRAM: As mentioned, on-chip Level 1 data and instruction cache memory cell arrays (32KByte each) were employed on the device. The SRAM cell array used a 6T CMOS SRAM cell design. Metal 4 distributed Vcc and GND and formed “piggyback” word lines (via metals 1 - 3). Metal 3 formed the bit lines. Metal 2 distributed GND and Vcc throughout the cells and was used as cell interconnect. Metal 1 also provided cell interconnect. Polycide formed the word lines/select and storage gates. Cell pitch was 4.5 x 7 microns (31.5 microns²).
- No redundancy fuses were noted.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Package section and EDX

Die optical inspection

Delayer to metal 6 and inspect

Aluminum removal (metal 6)

Delayer to metal 5 and inspect

Aluminum removal (metal 5) and inspect tungsten plugs

Delayer to metal 4 and inspect

Aluminum removal (metal 4) and inspect tungsten plugs

Delayer to metal 3 and inspect

Aluminum removal (metal 3) and inspect tungsten plugs

Delayer to metal 2 and inspect

Aluminum removal (metal 2) and inspect tungsten plugs

Delayer to metal 1 and inspect

Tungsten removal (metal 1)

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

OVERALL QUALITY EVALUATION: Overall Rating: Normal to Good.

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Solder ball placement	G
Solder ball interconnect quality	G
Dicing quality	N
Die attach quality	G
Die attach method	C4 solder ball interconnect technique
Dicing method	Sawn
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	N
Metal registration	G
Contact coverage	G
Via/contact registration	N
Etch control (depth)	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP (lid)

AMD (logo)
AMD-K6™
AMD-K6/PR2-200ALR
2.9V B9713CJB
© 1997 AMD
Designed for
Microsoft®
Windows® 95
(logo)

PACKAGE MATERIALS

Lid:	Aluminum (Al)
Lid attach:	Silicone-type adhesive
External pins:	Iron-nickel-cobalt (FeNiCo)
Pin plating:	Gold over nickel (Au/Ni)
Pin attach:	Silver-copper (AgCu) solder
Contact pads:	Nickel (Ni)
Internal traces and vias:	Molybdenum (Mo)
Solder balls:	Lead (Pb)
Bond pads:	Tin-copper (SnCu)
Bond pad barrier:	Lead-chromium (PbCr)
Capacitor end terminations:	Silver (Ag)
End termination barrier:	Nickel (Ni)
Capacitor attach	Tin-lead (SnPb) solder

DIE MATERIAL ANALYSIS

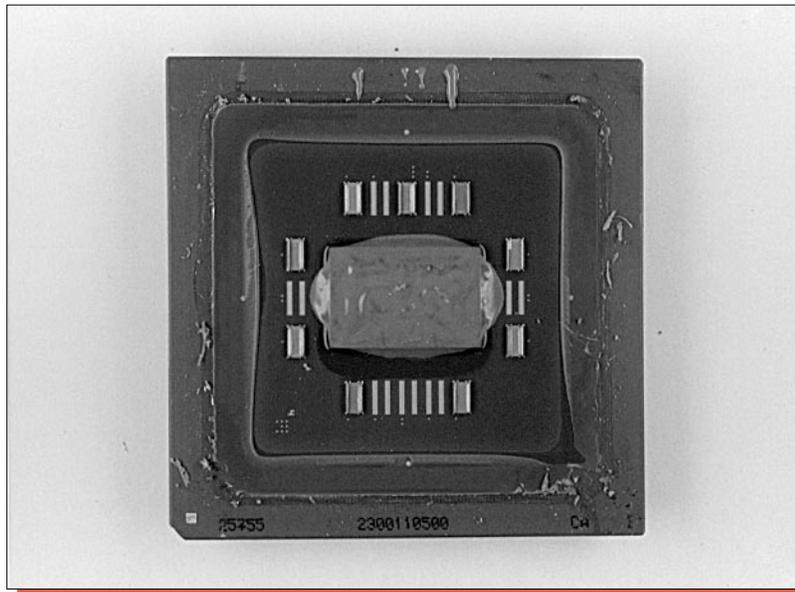
Final passivation:	Single layer of nitride over dual glass layers.
Metallization 6:	Aluminum with an aluminum-oxide cap (and a thin titanium adhesion layer?).
Metallization 2 - 5:	Aluminum with titanium-nitride caps (and thin adhesion layers?).
Interlevel dielectrics 2 - 5:	A thin layer of glass followed by an SOG and a thick layer of glass.
Interlevel dielectric 1:	Thick layer of glass.
Metallization 1:	Tungsten (damascene process) with titanium-nitride liner and an apparent titanium adhesion layer.
Vias (M2 - M5):	Tungsten (lined with titanium-nitride).
Pre-metal glass:	Thick layer of silicon-dioxide over a thin nitride.
Polycide:	Titanium-silicide on polysilicon.
Salicide on diffusions:	Titanium-silicide.

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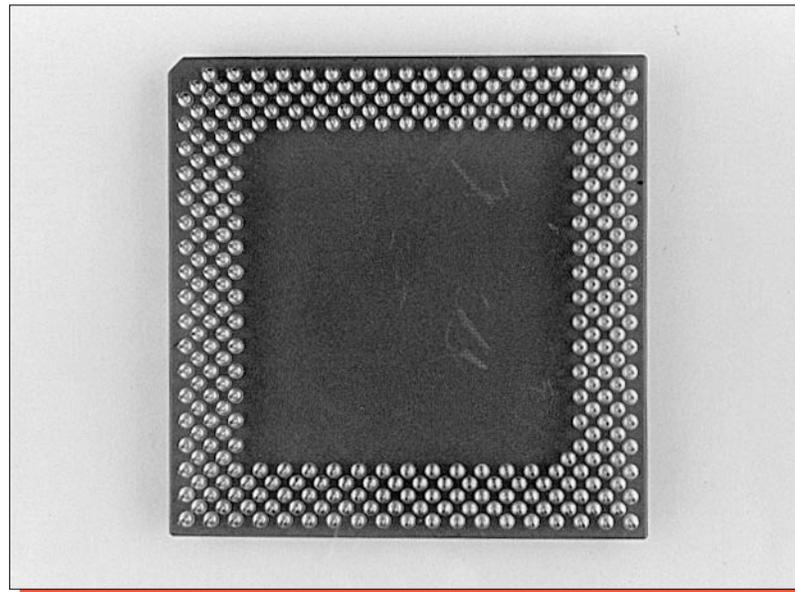
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top, intact



top, lid removed



bottom

Figure 1. Package photographs of the AMD K6 Microprocessor. Mag. 1.3x.

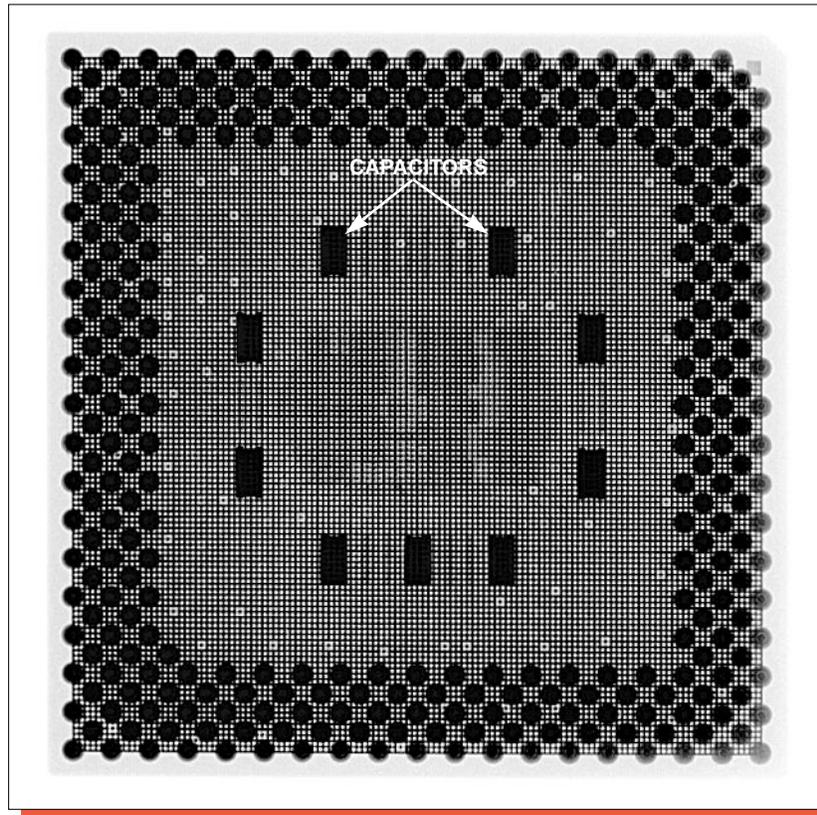


Figure 2. Topological x-ray view of the package. Mag. 2x.

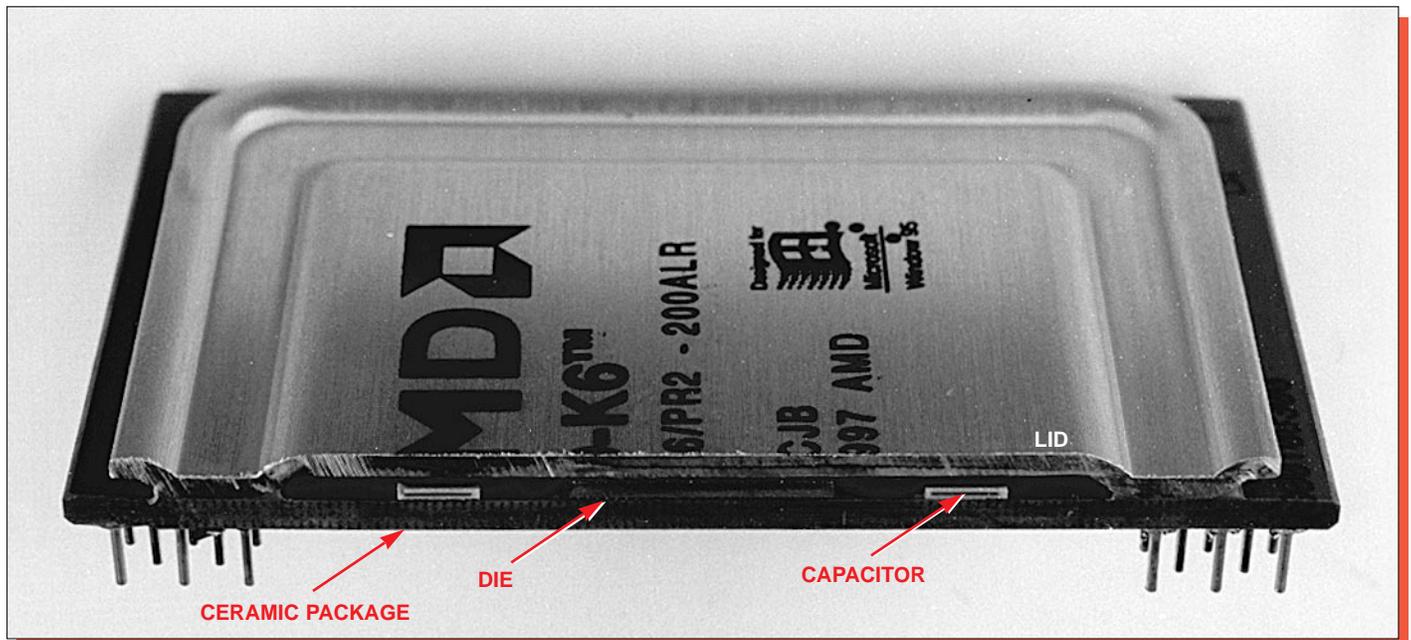
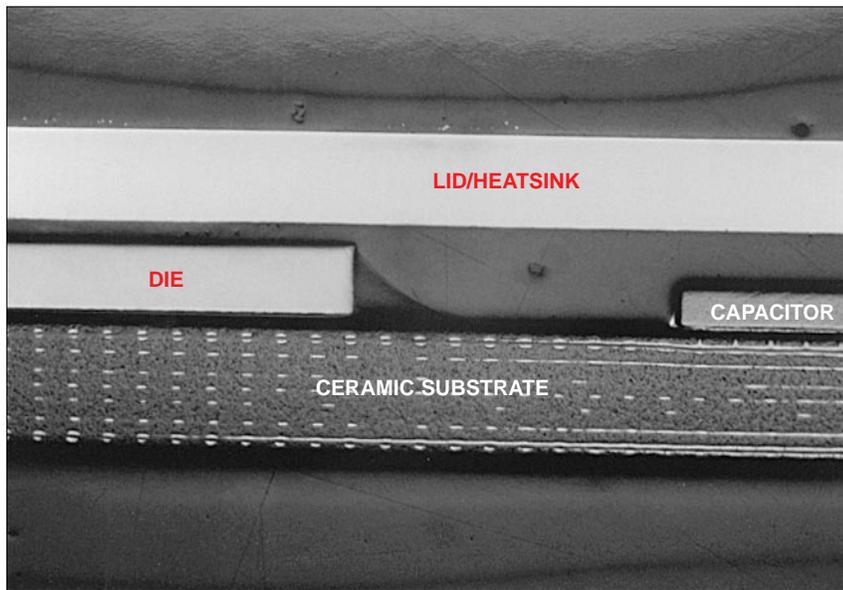
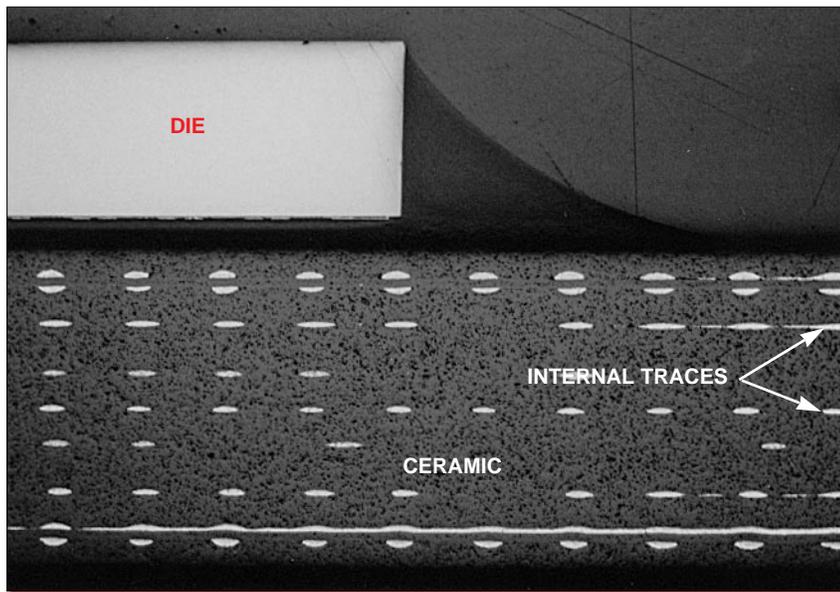


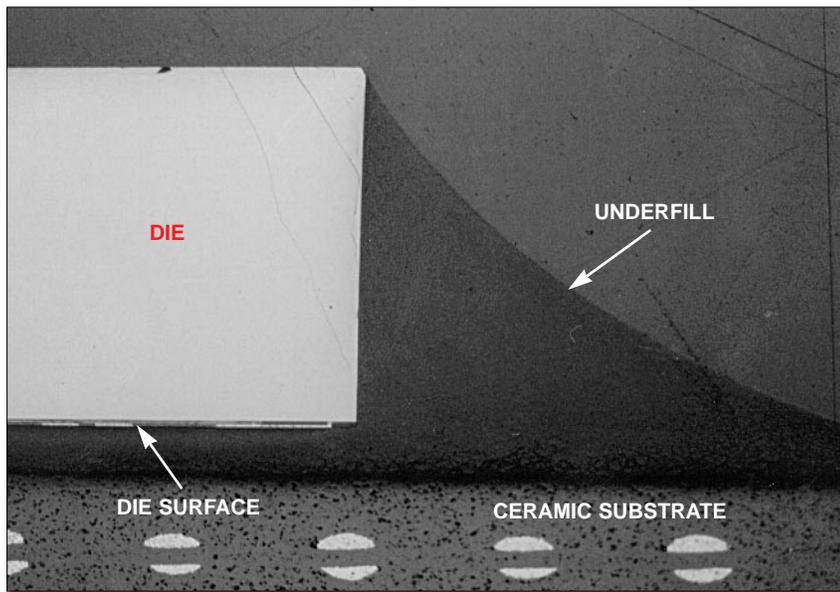
Figure 3. General cross section view of the package. Mag. 3.5x.



Mag. 13x

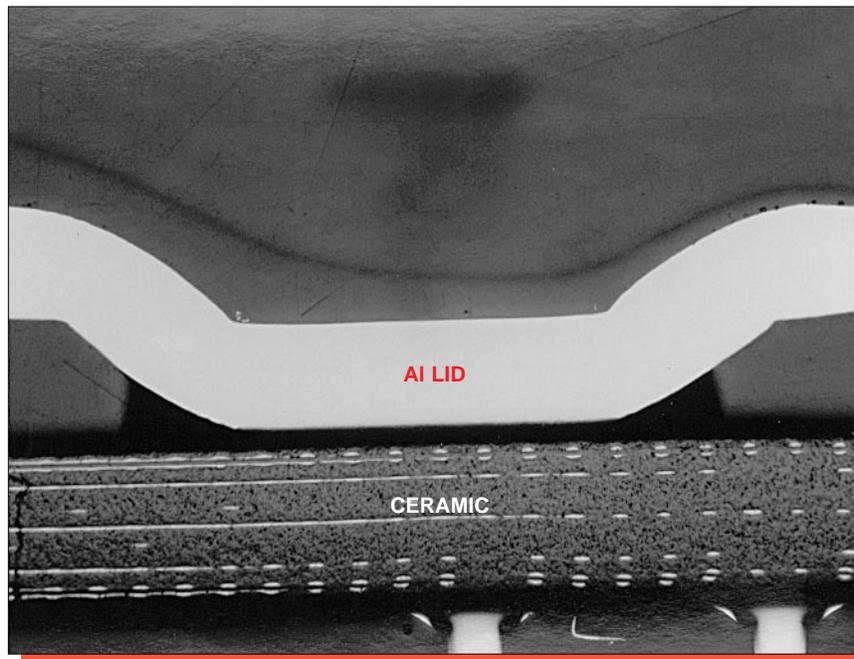


Mag. 30x

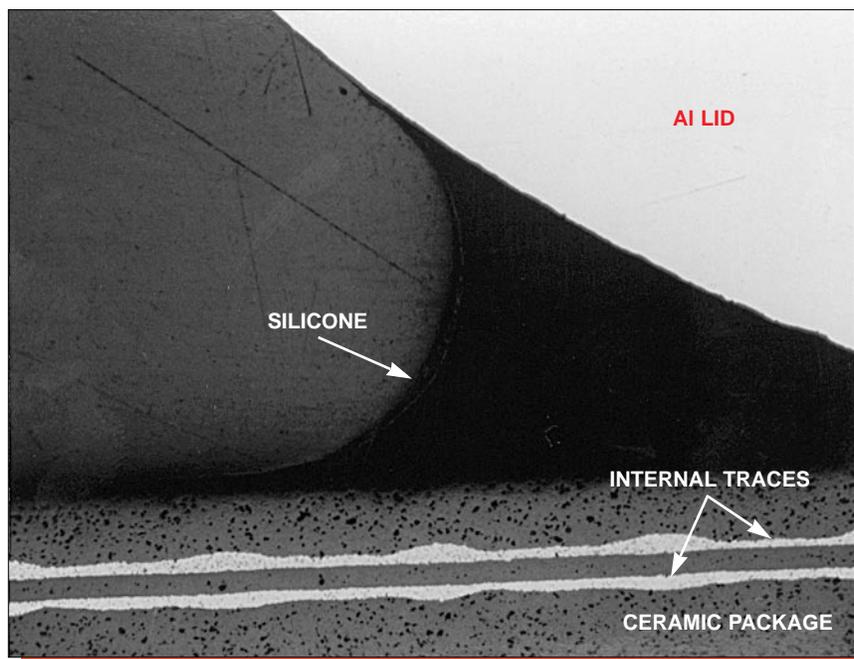


Mag. 65x

Figure 4. Package section views illustrating general construction.



Mag. 16x

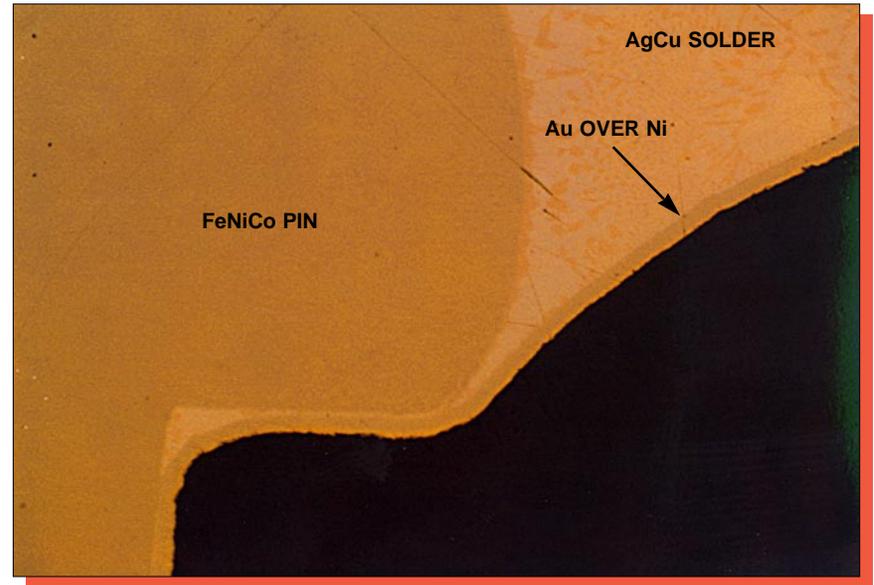


Mag. 80x

Figure 5. Package section views of the lid structure.



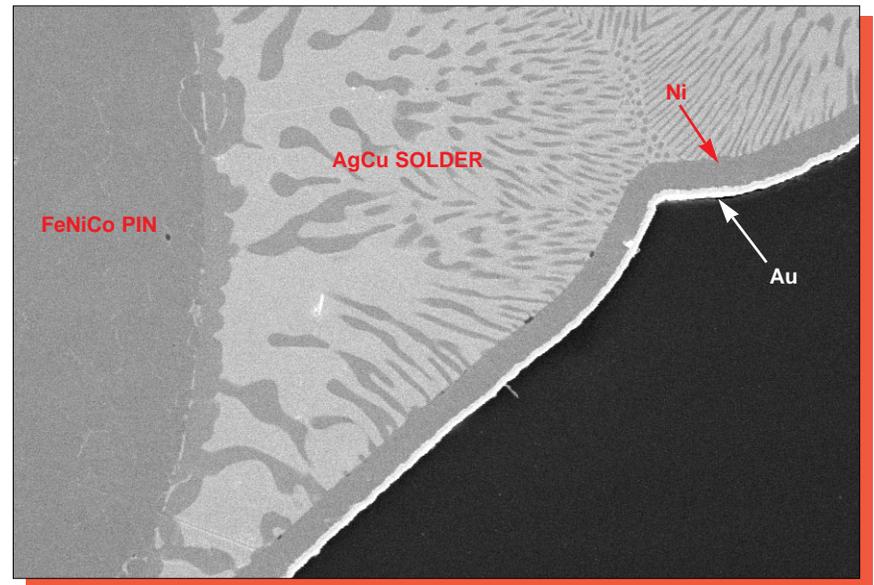
Mag. 65x



Mag. 320x

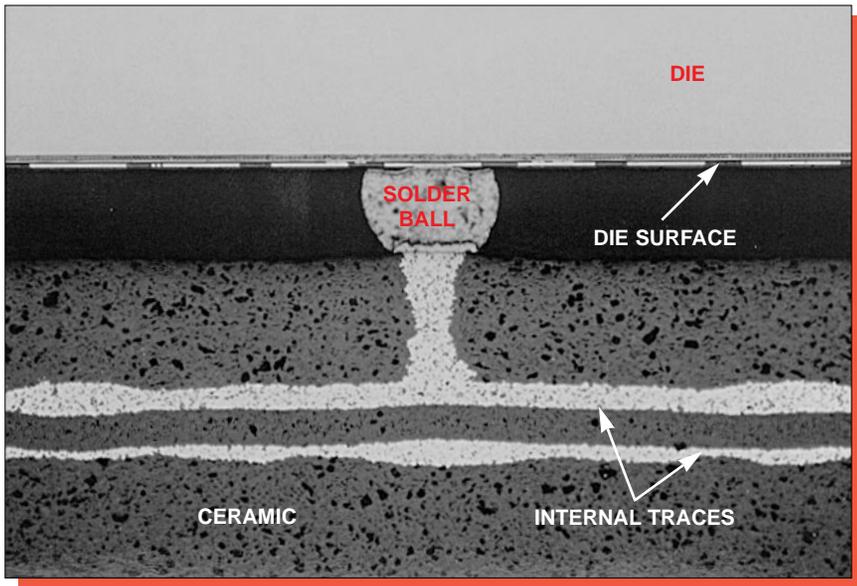


Mag. 130x

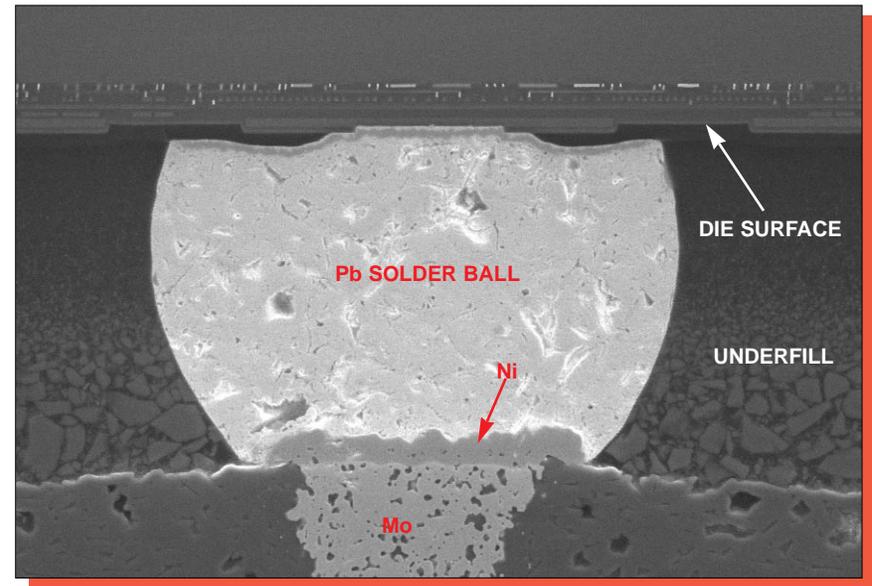


Mag. 750x

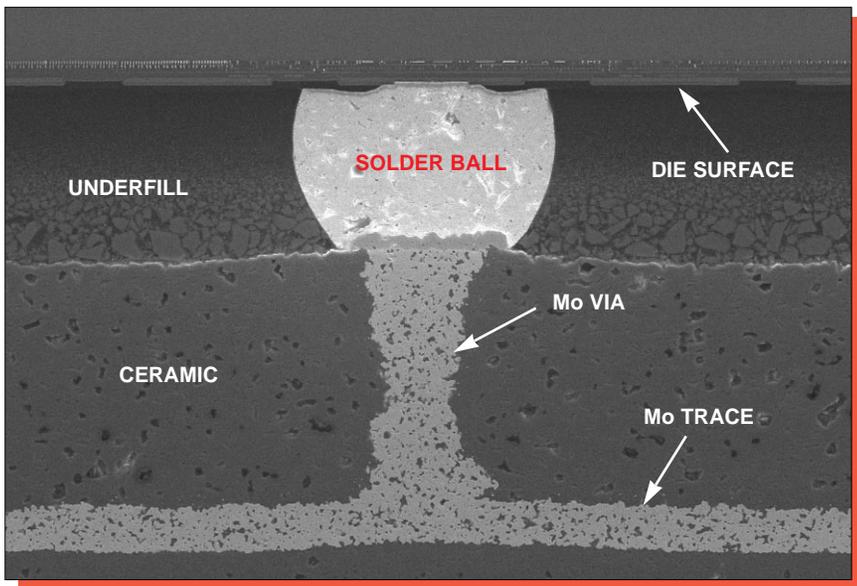
Figure 6. Package section views illustrating external lead connection.



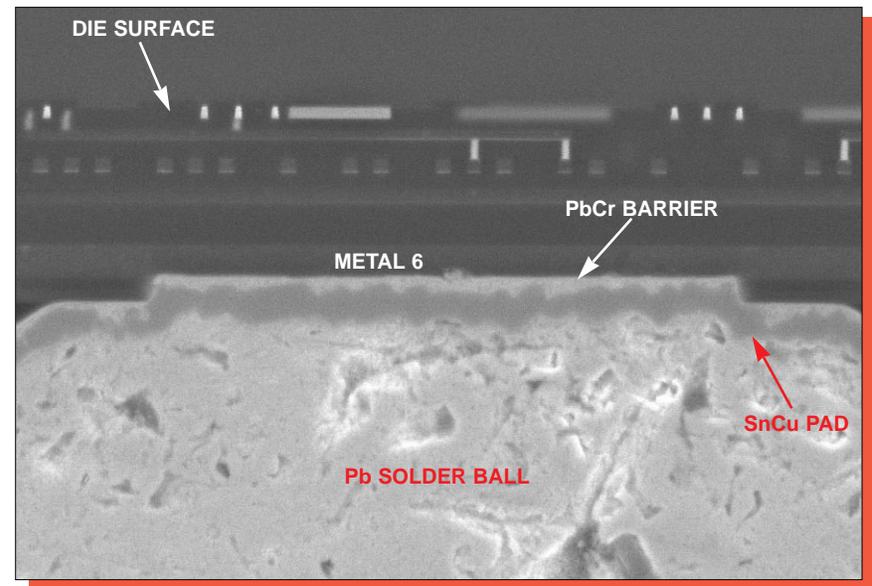
Mag. 130x



Mag. 500x

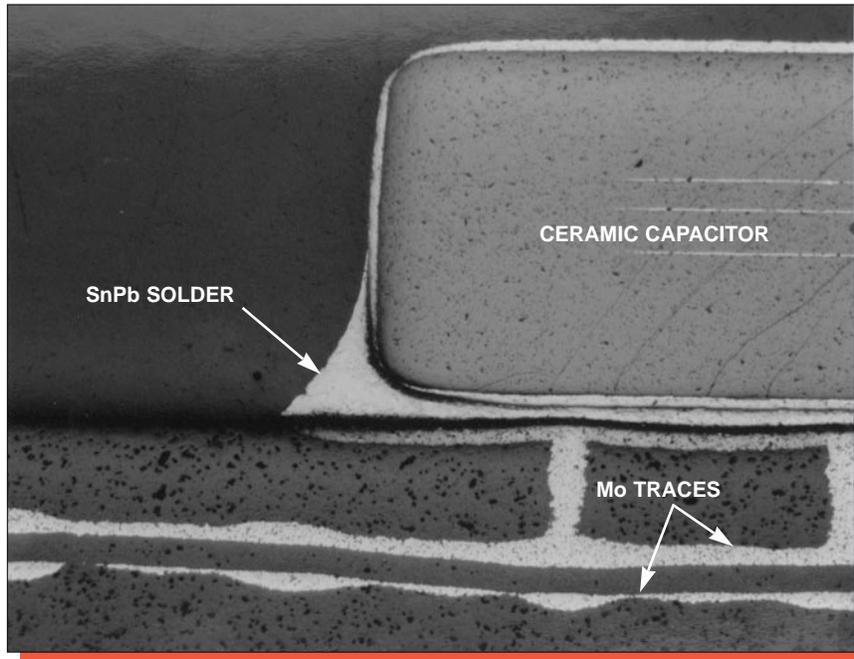


Mag. 250x

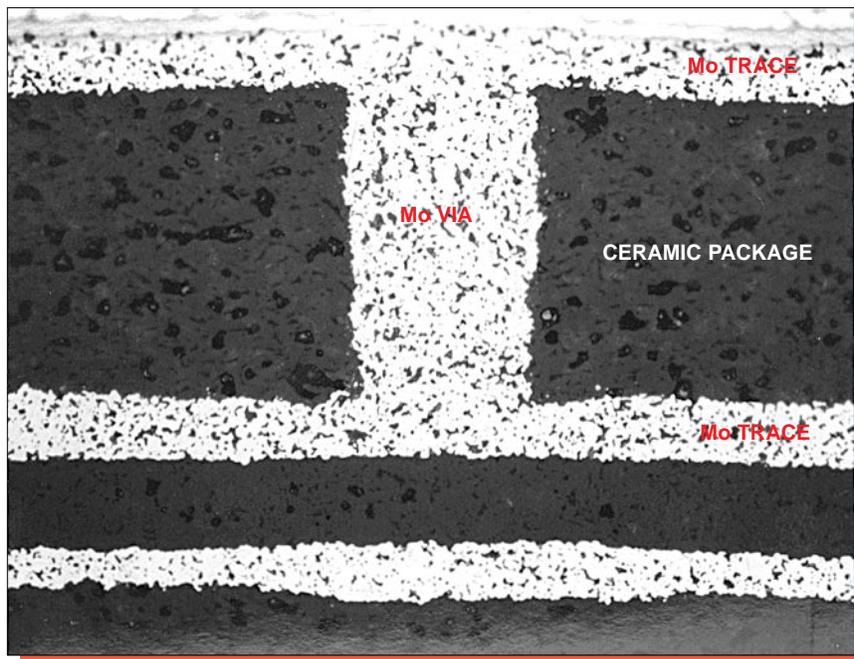


Mag. 2000x

Figure 7. Package section views of a typical solder ball connection.



Mag. 100x



Mag. 320x

Figure 8. Package section views of a capacitor attach and an internal via.

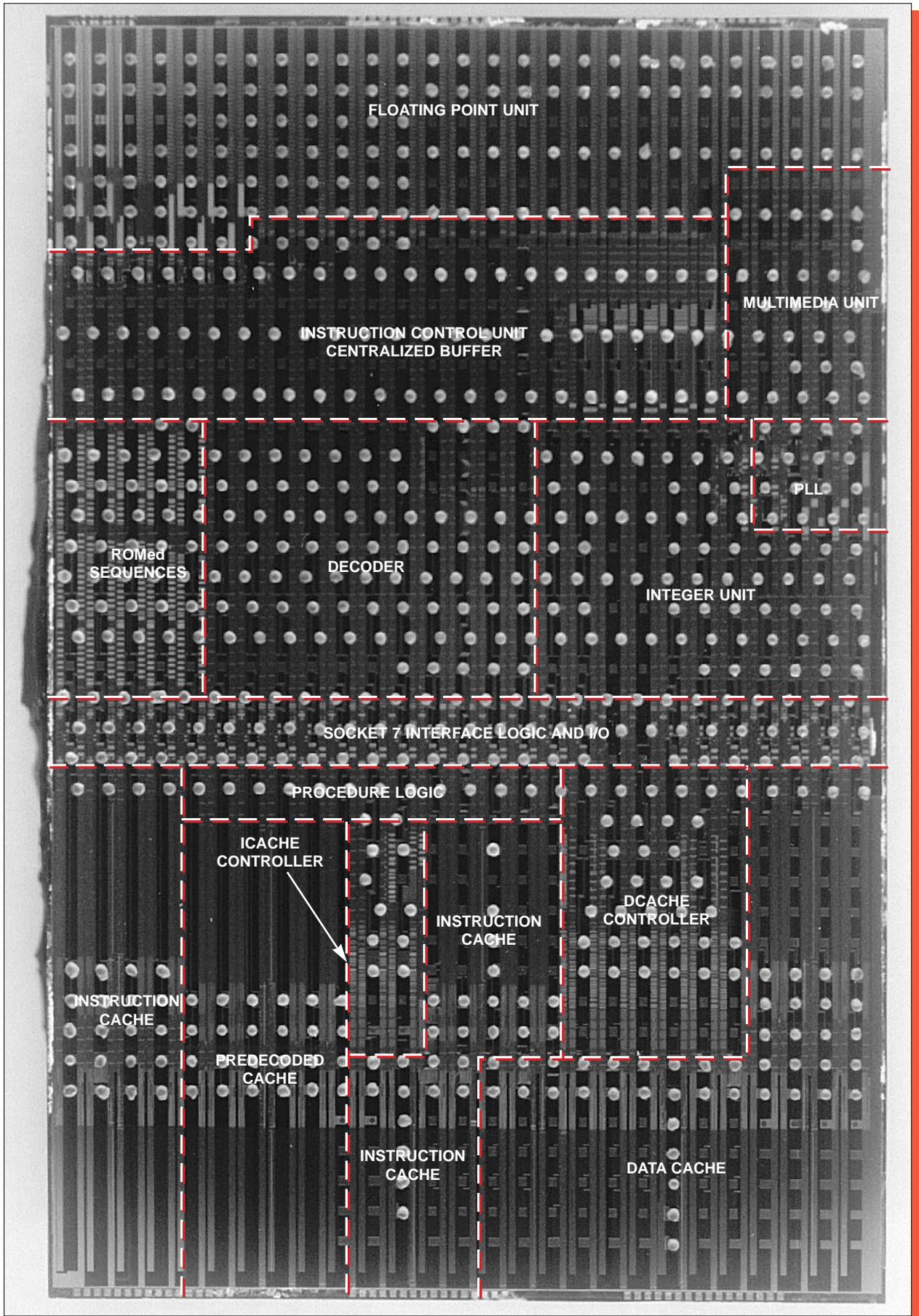


Figure 9. Whole die photograph of the AMD K6 Microprocessor. Mag. 15x.



Figure 10. Optical views of die markings. Mag. 225x.

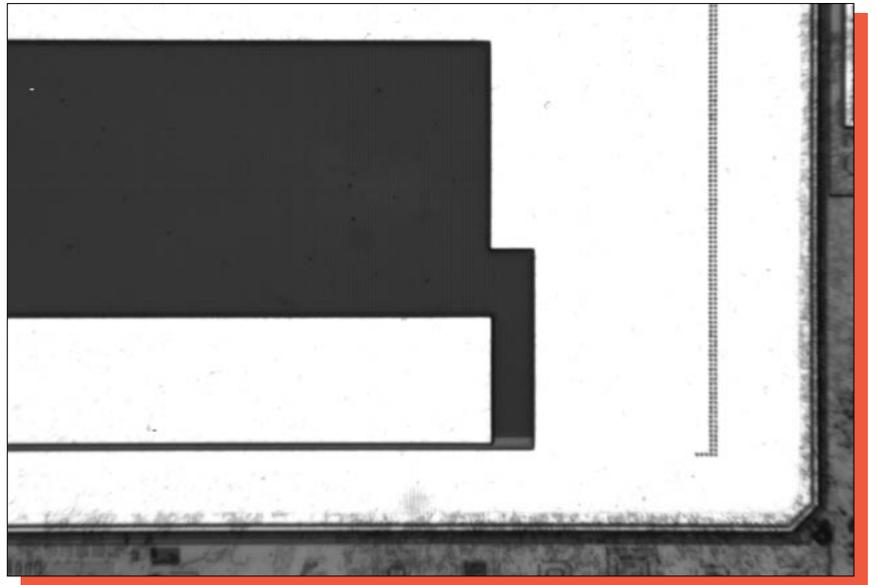
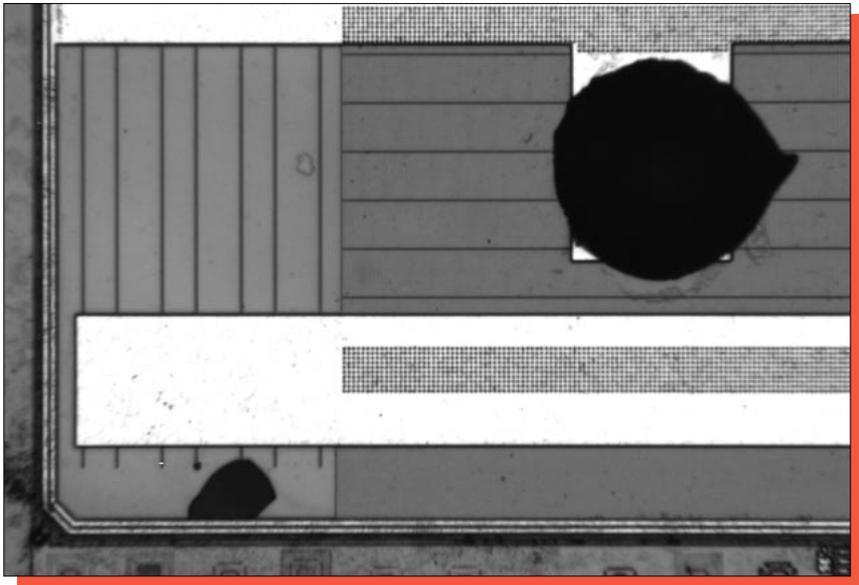
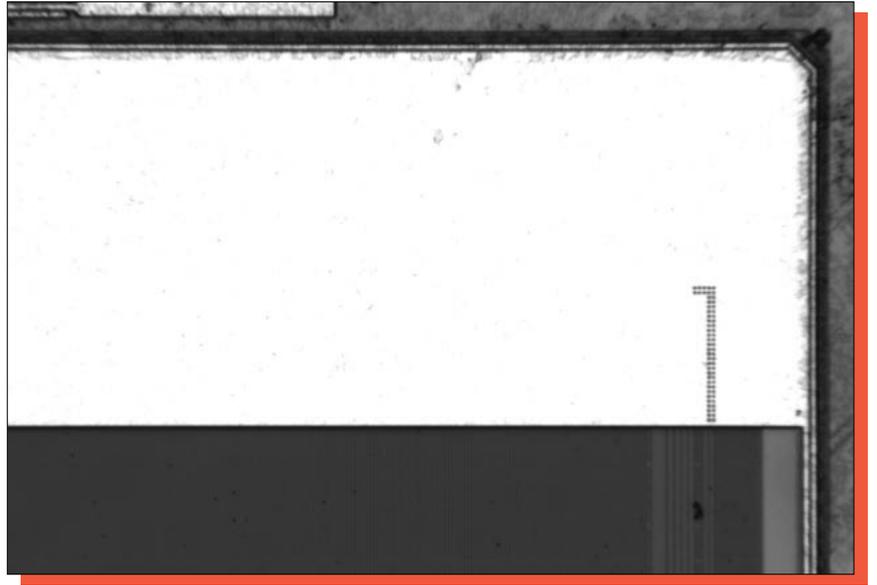


Figure 11. Optical views of die corners. Mag 225x.

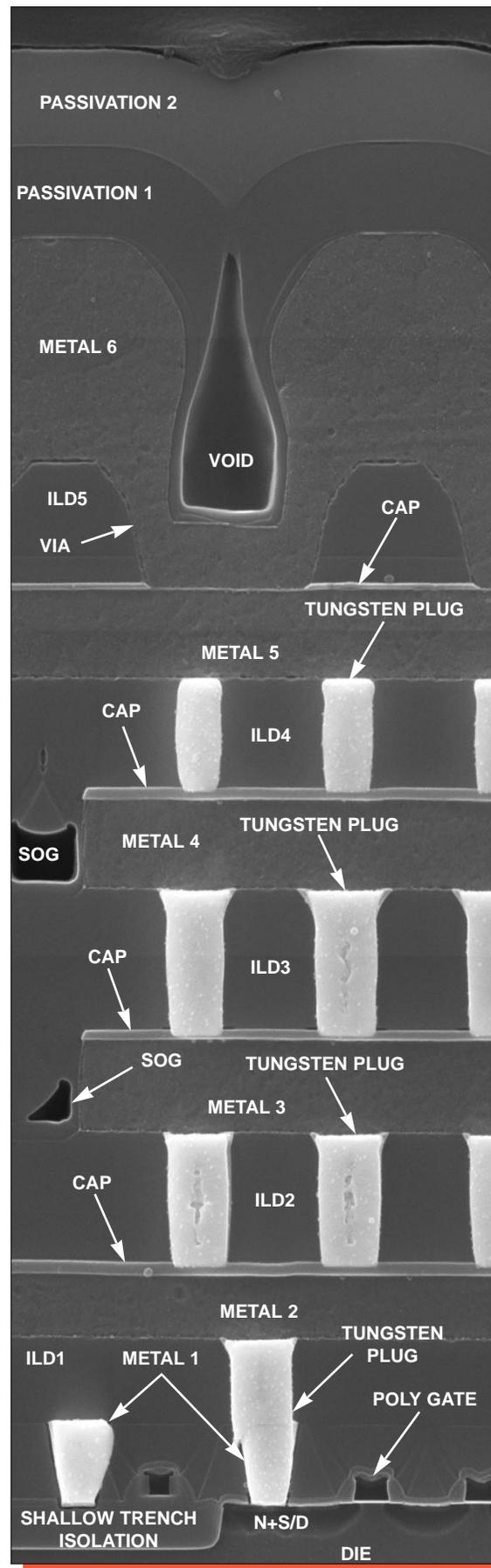
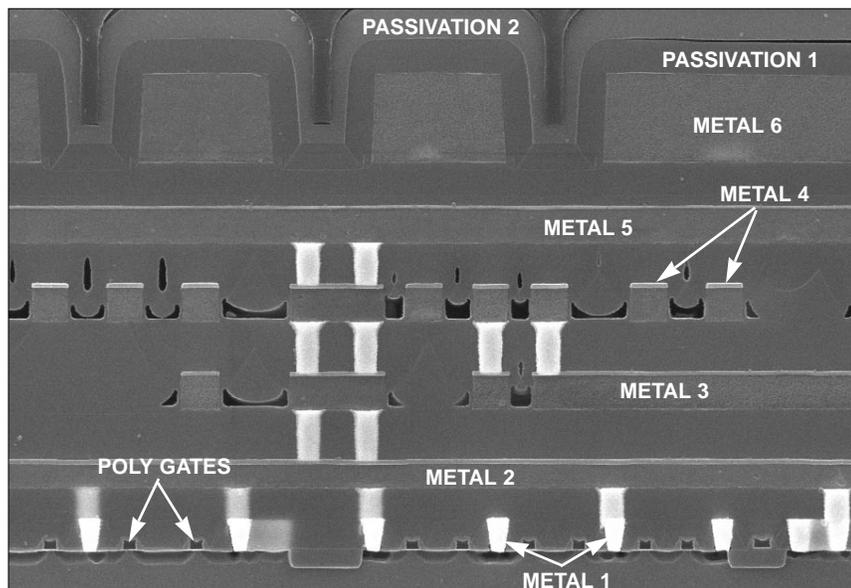
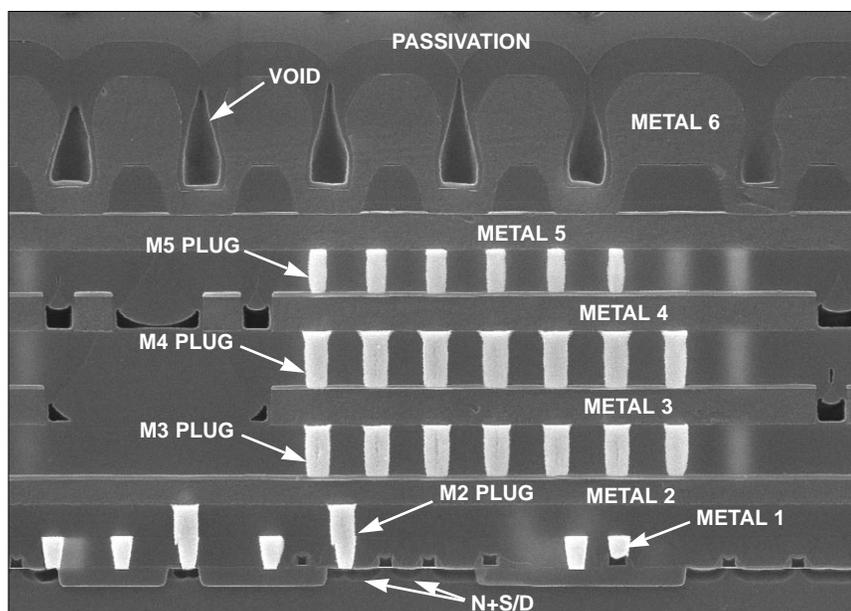


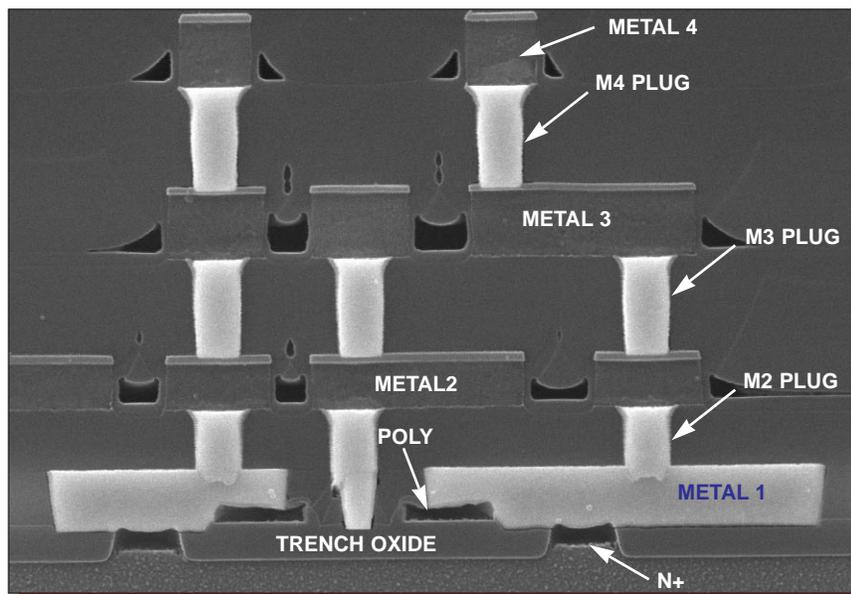
Figure 12. SEM section view illustrating general device structure. Mag. 17,400x.



Mag. 6000x

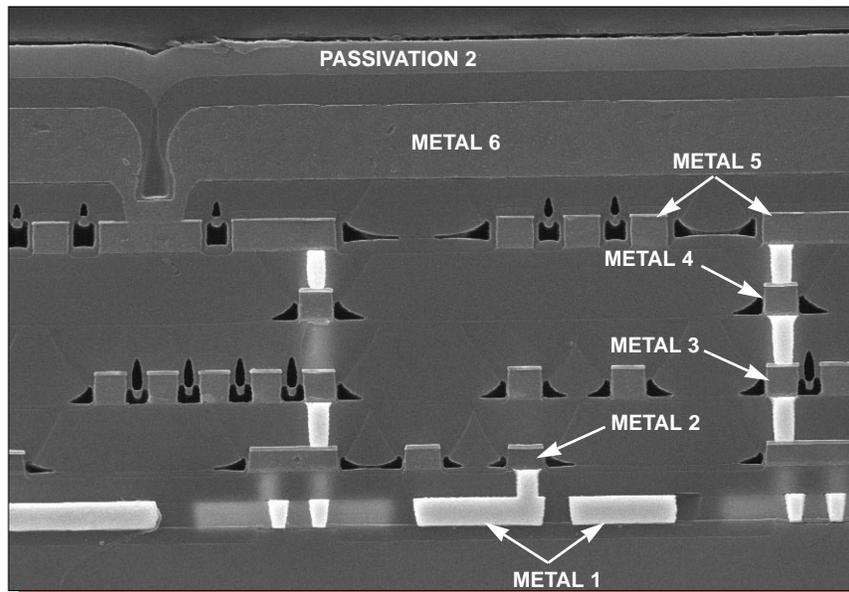


Mag. 6000x

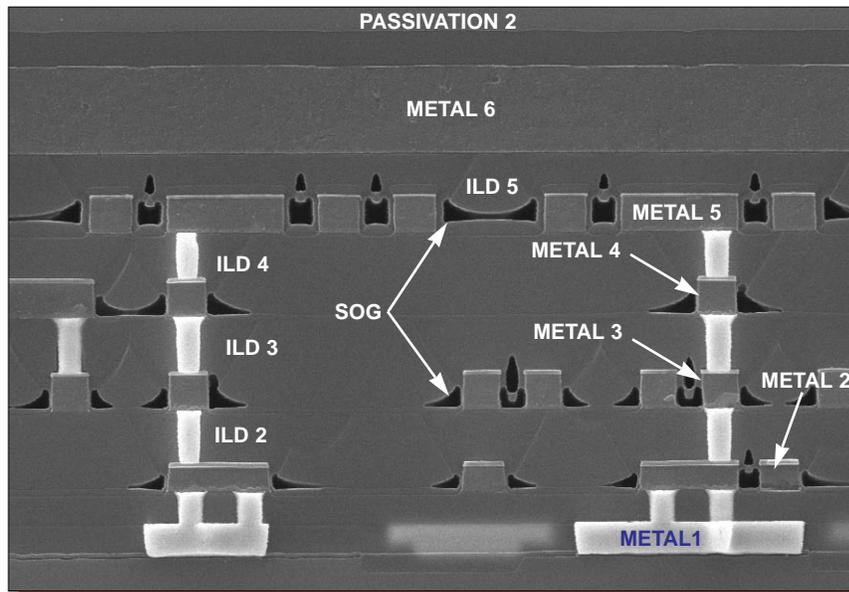


Mag. 11000x

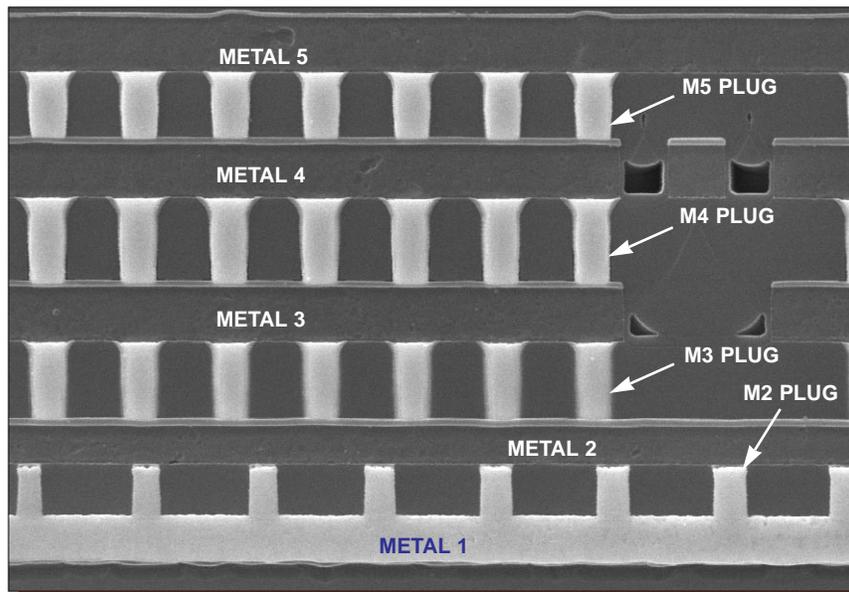
Figure 12a. SEM section views illustrating general device structure.



Mag. 5000x

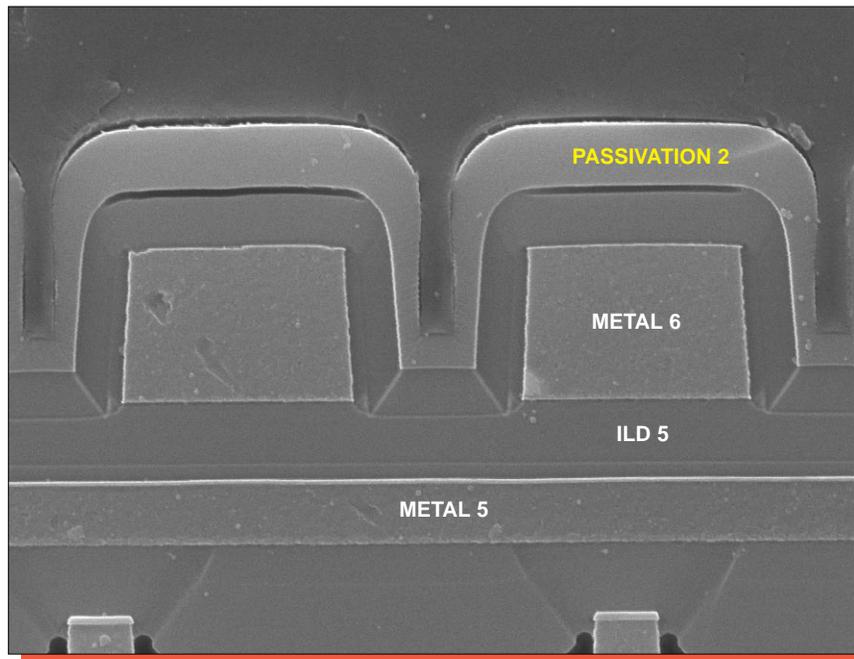


Mag. 6000x

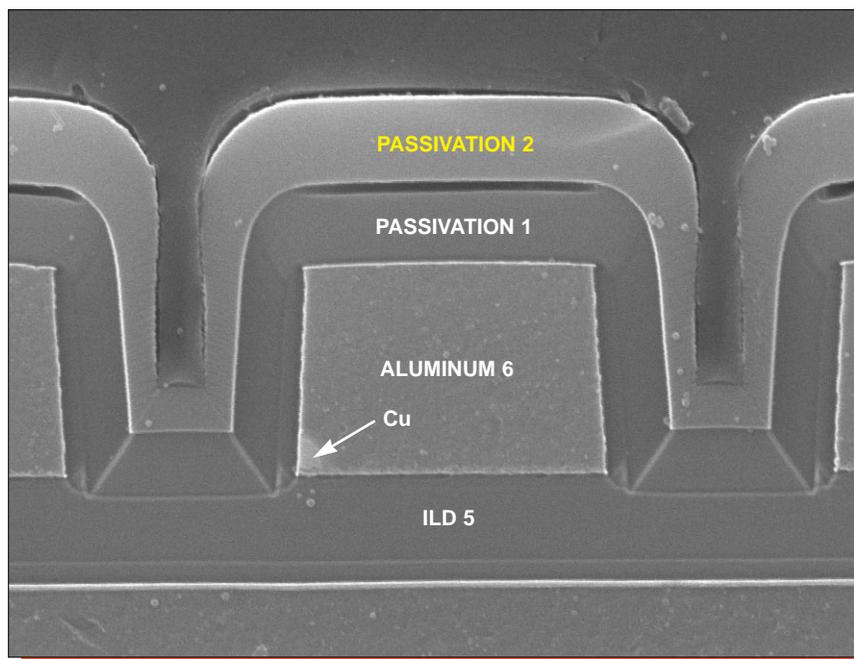


Mag. 11,000x

Figure 13. Glass etch section views illustrating general device structure.

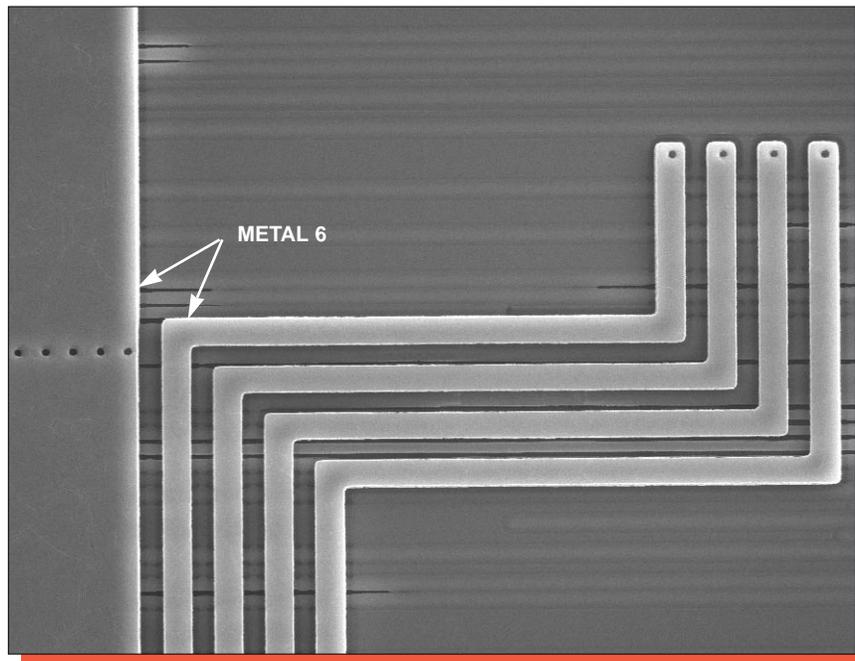


Mag. 10,000x.

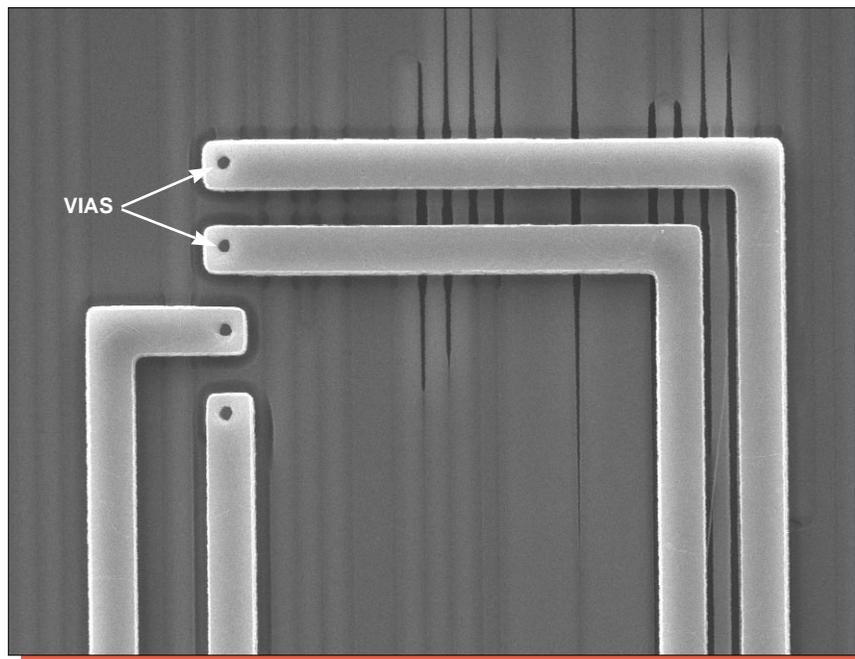


Mag. 13,000x

Figure 14. SEM section views of metal 6 line profiles.

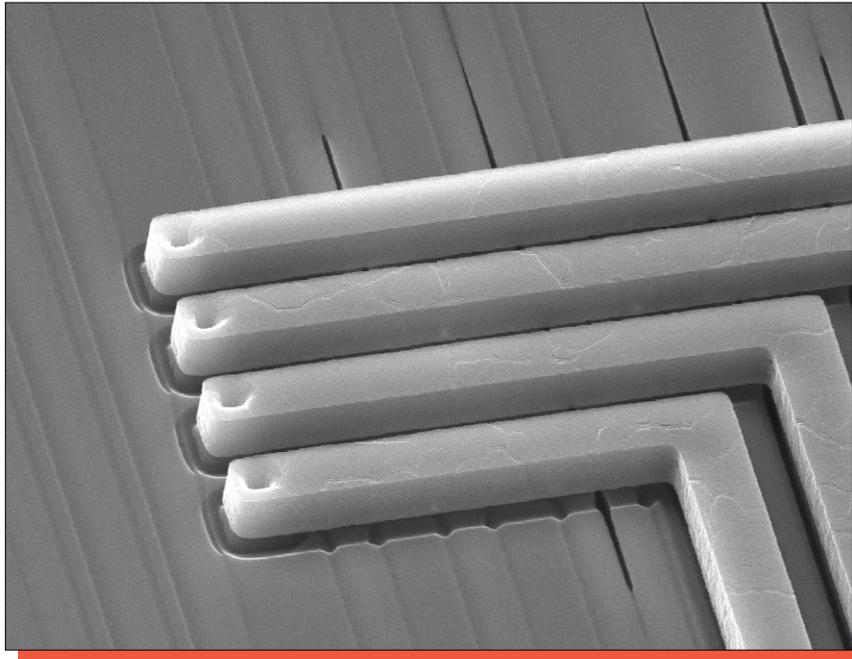


Mag. 1250x

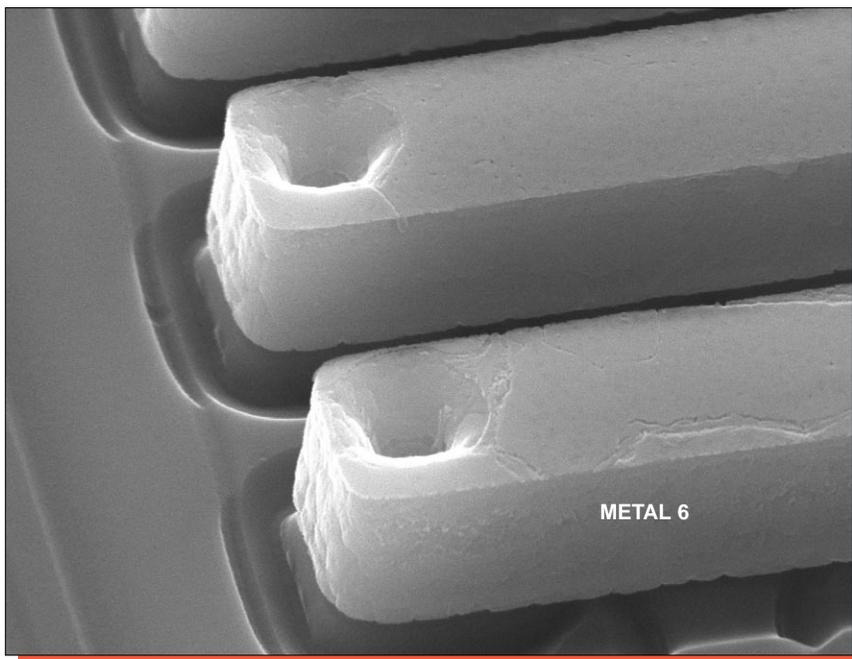


Mag. 2000x

Figure 15. Topological SEM views of metal 6 patterning. 0°.

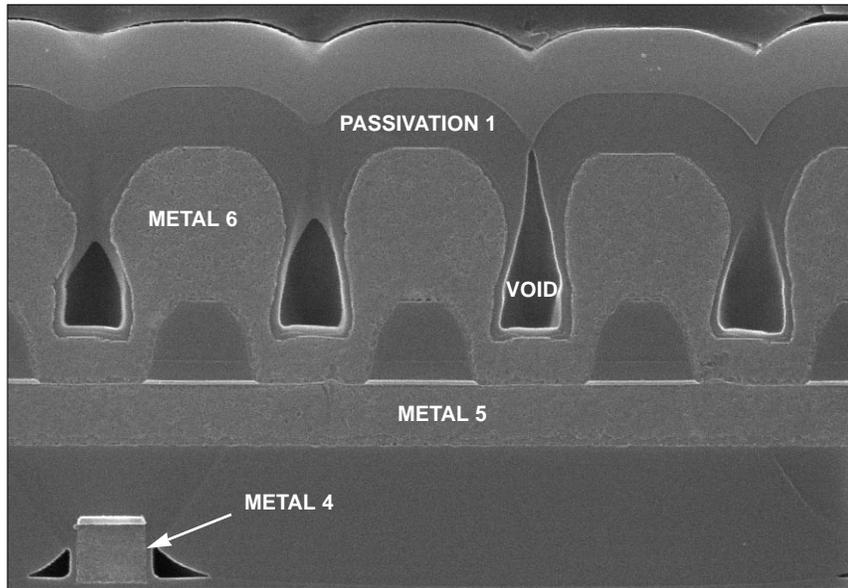


Mag. 2800x

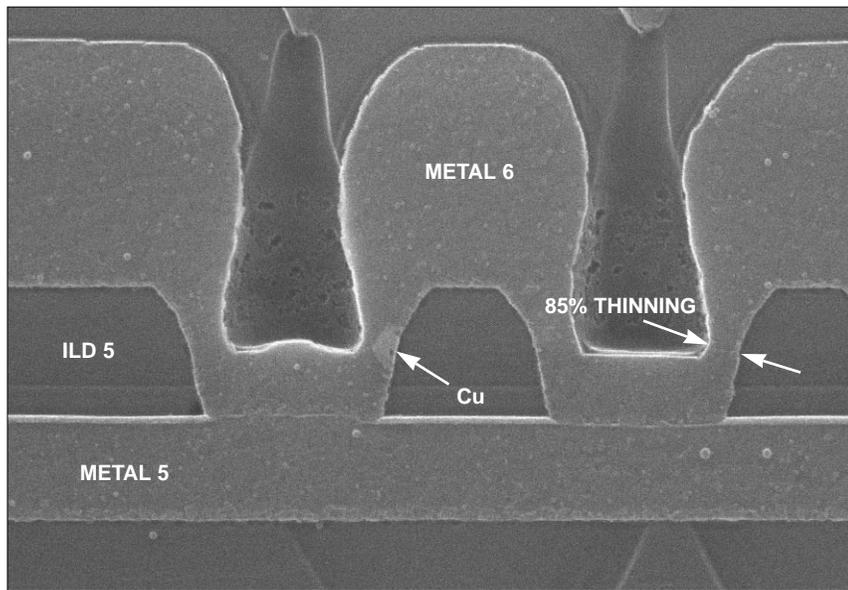


Mag. 10,000x

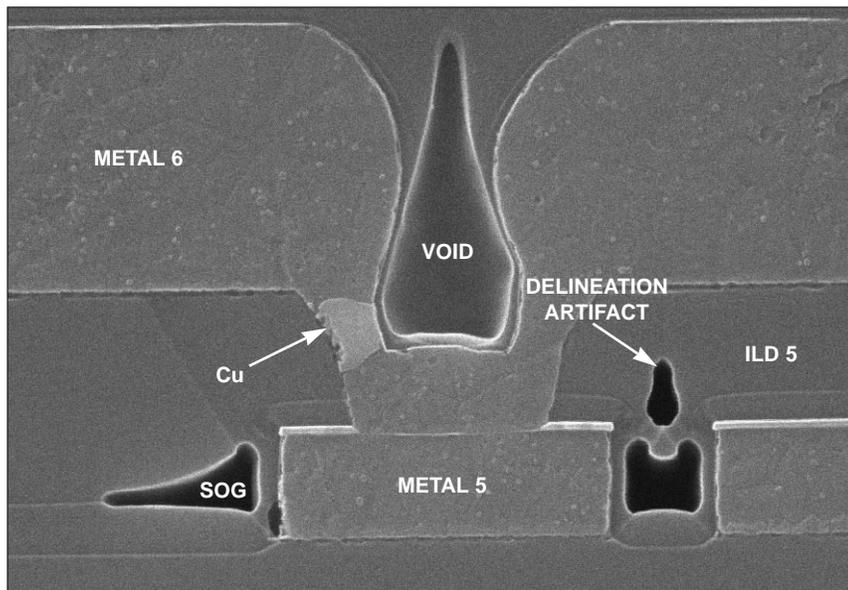
Figure 16. SEM views of metal coverage. 50°.



Mag. 10,000x

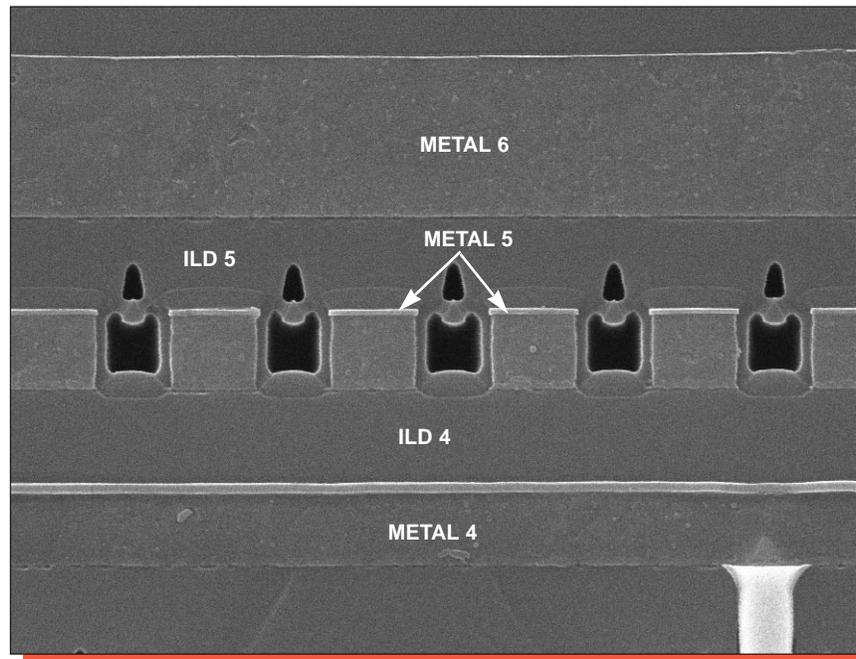


Mag. 15,000x

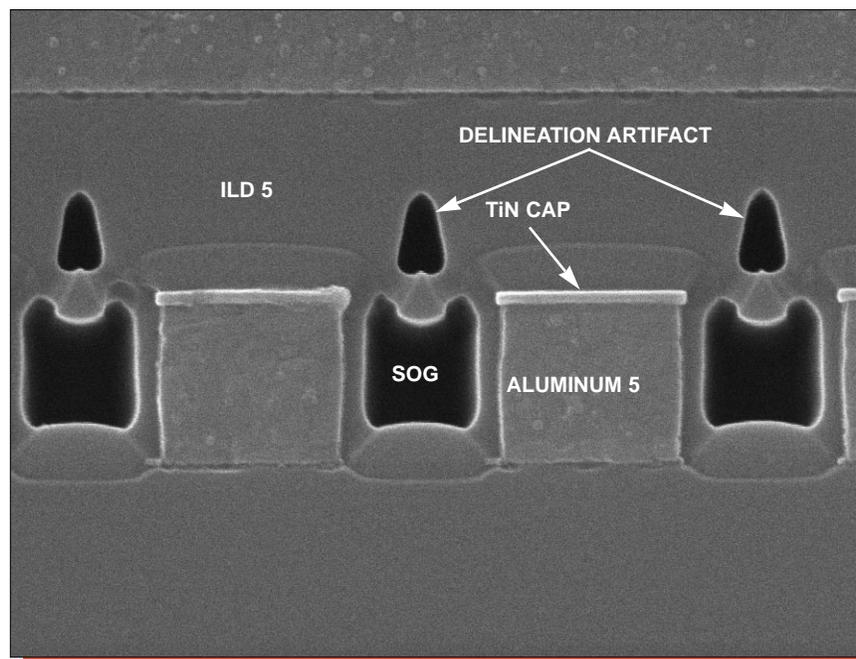


Mag. 17,500x

Figure 17. SEM section views of metal 6-to-metal 5 vias.



Mag. 12,400x



Mag. 26,000x

Figure 18. SEM section views of metal 5 line profiles.

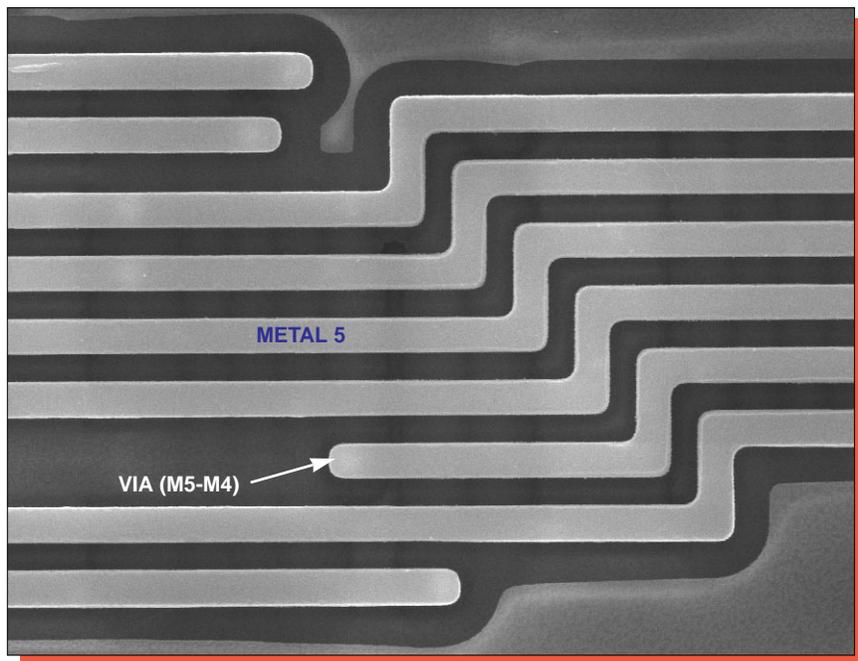
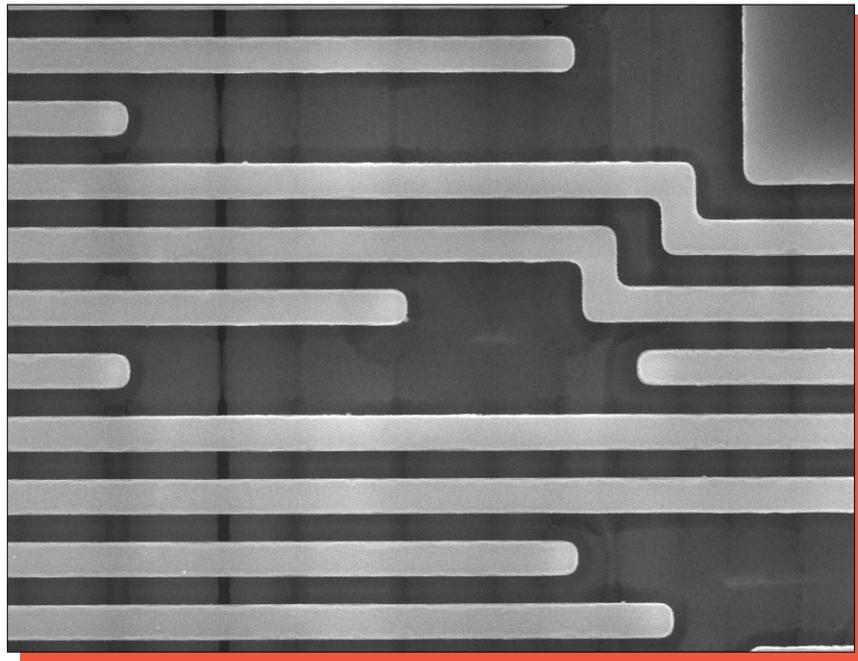
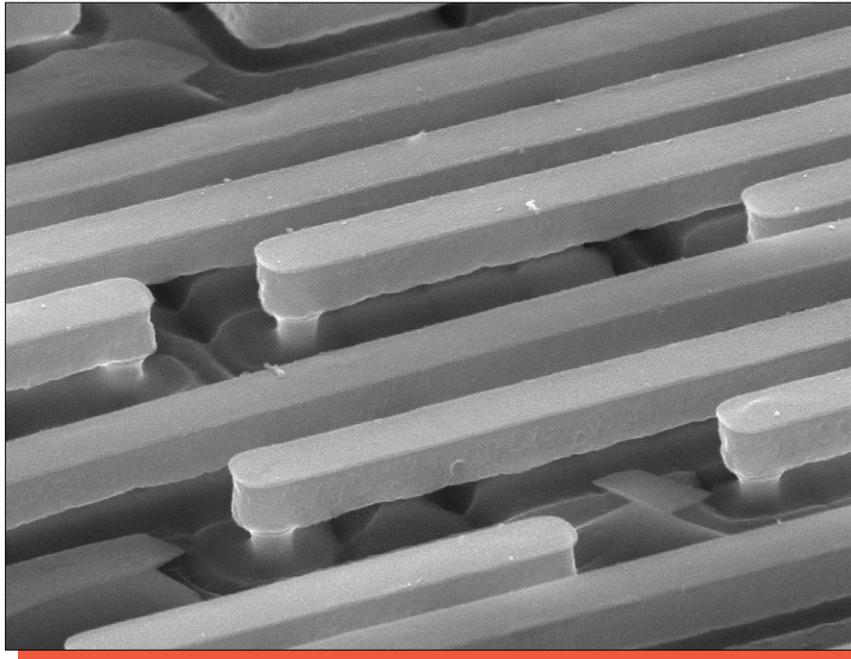
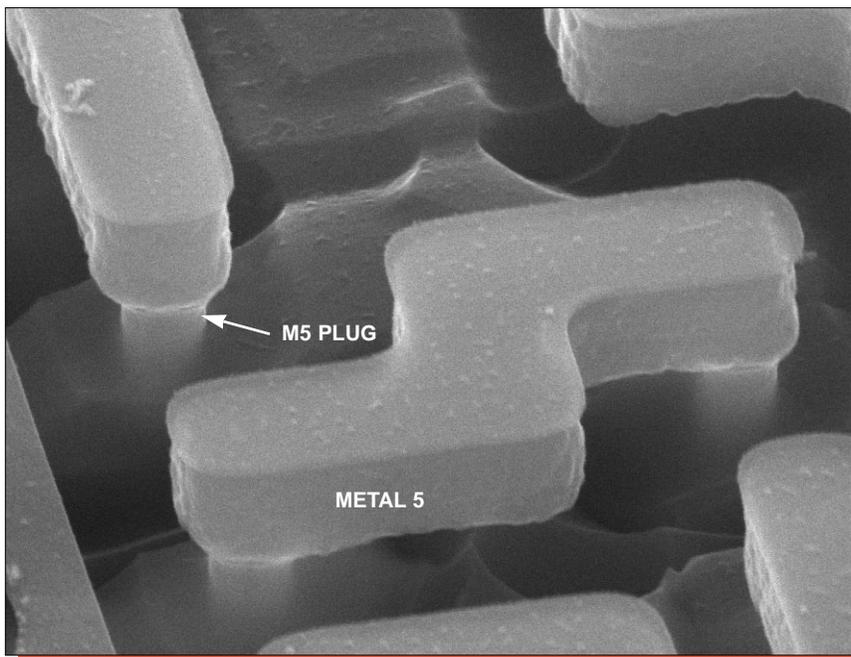


Figure 19. Topological SEM views of metal 5 patterning. Mag. 5000x, 0°.

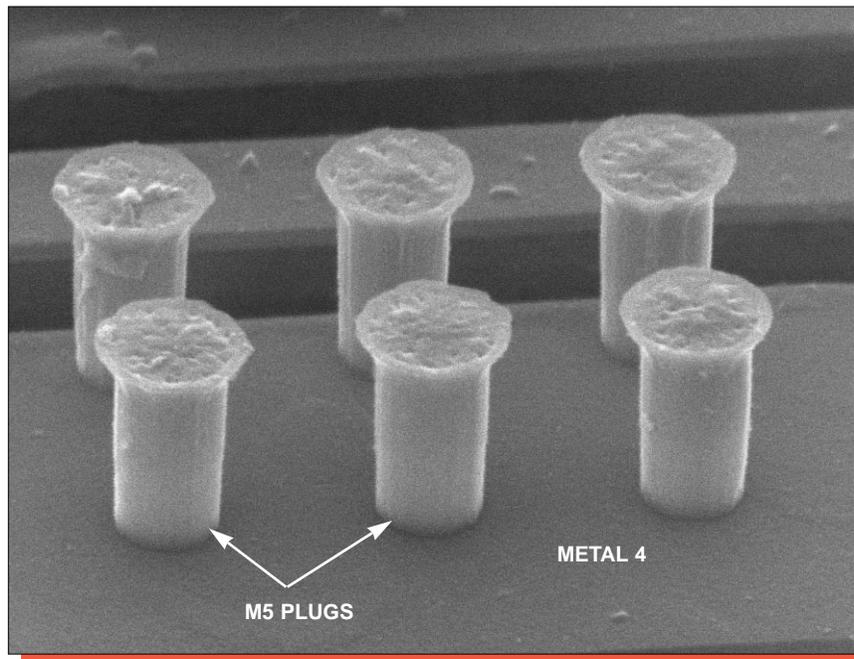


Mag. 9000x

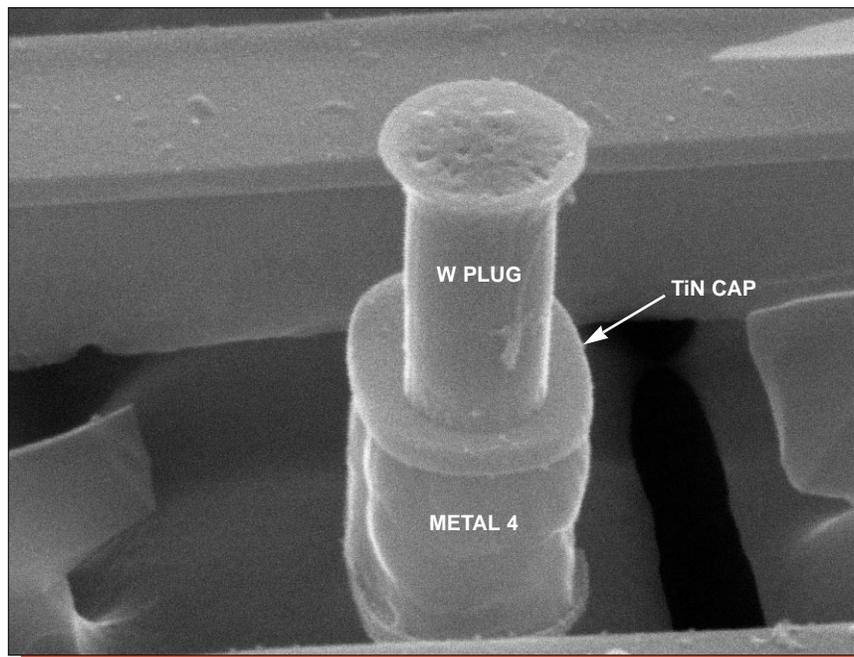


Mag. 20,000x

Figure 20. SEM section views of metal 5 coverage. 60°.

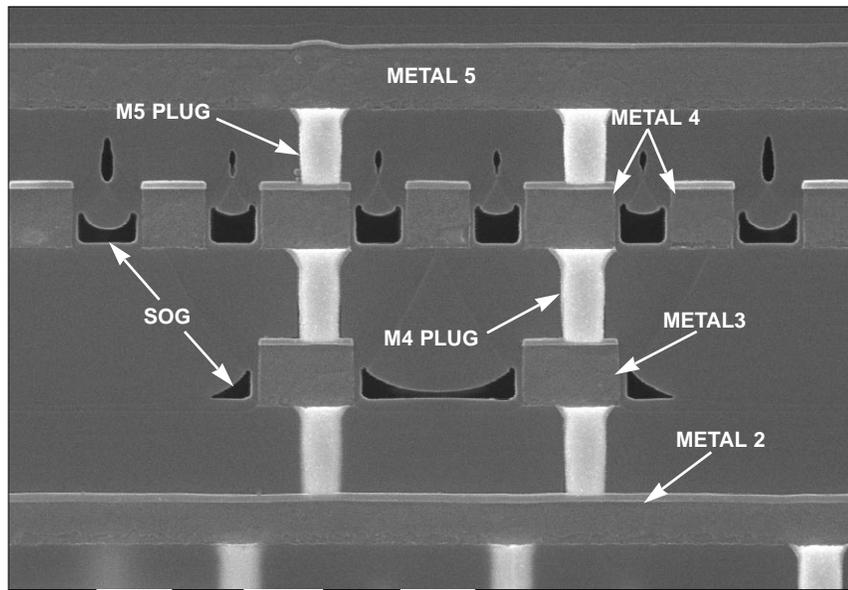


Mag. 28,000x

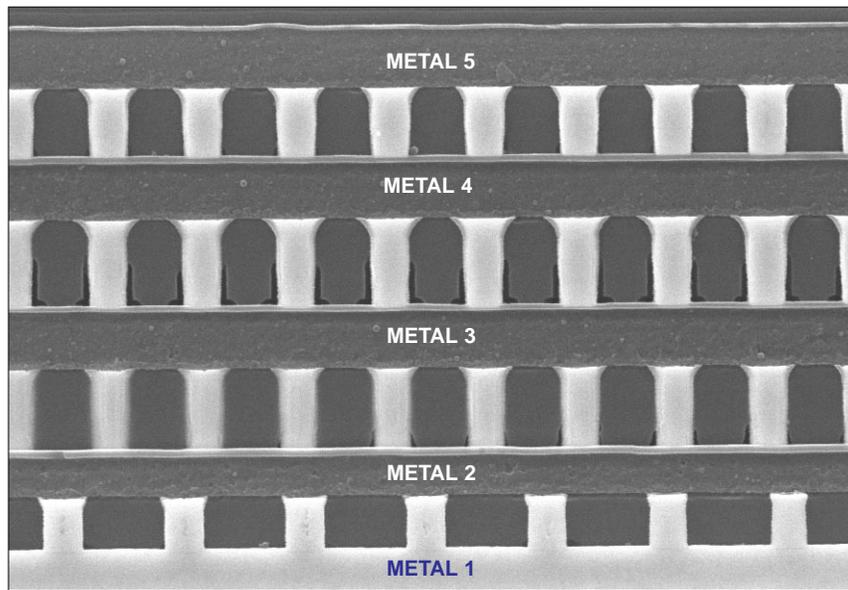


Mag. 40,000x.

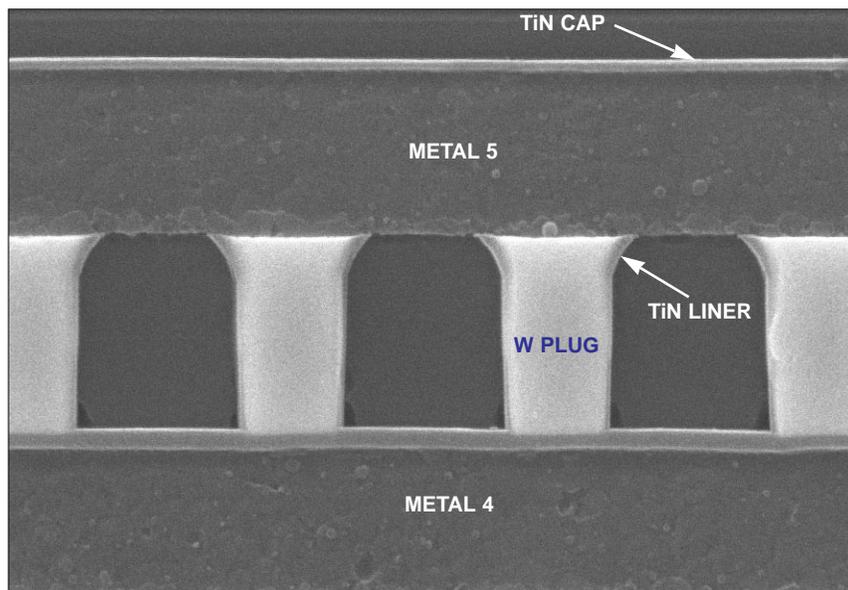
Figure 21. SEM views of metal 5 plugs. 50°.



Mag. 10,000x

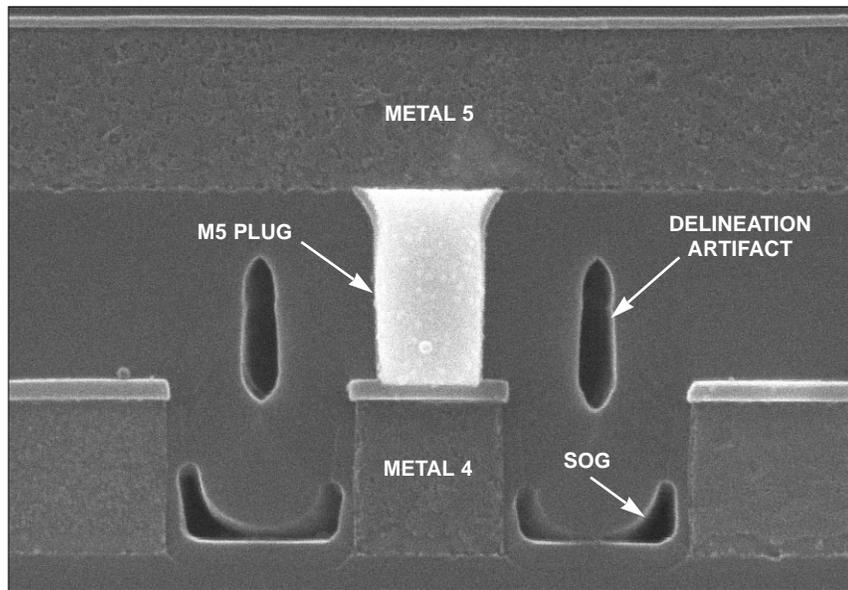


Mag. 9000x

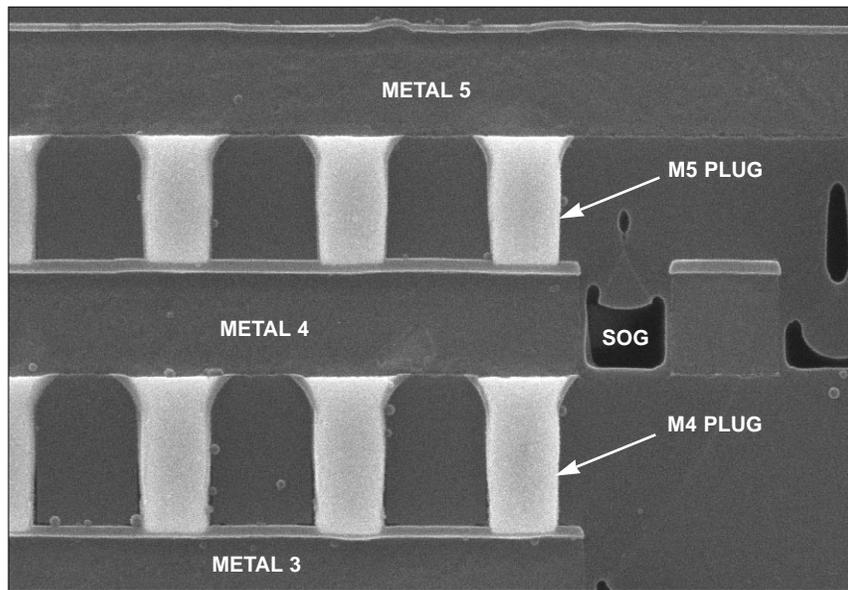


Mag. 26,000x

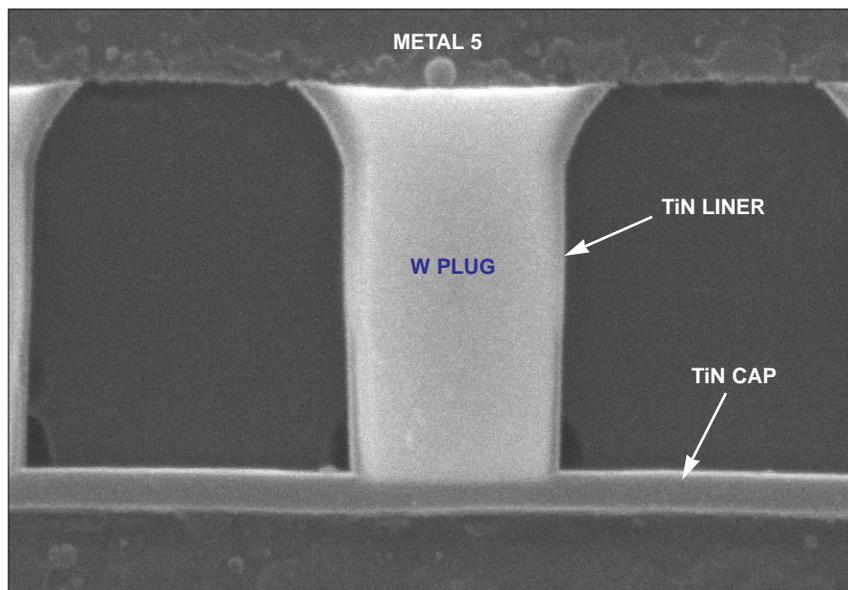
Figure 22. SEM section views of metal 5-to-metal 4 vias.



Mag. 26,000x

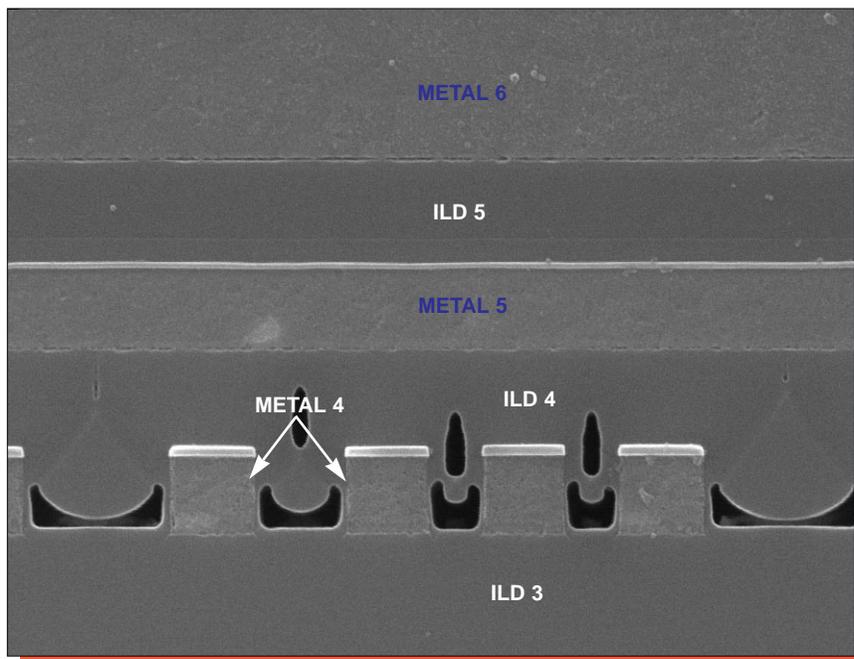


Mag. 17,000x

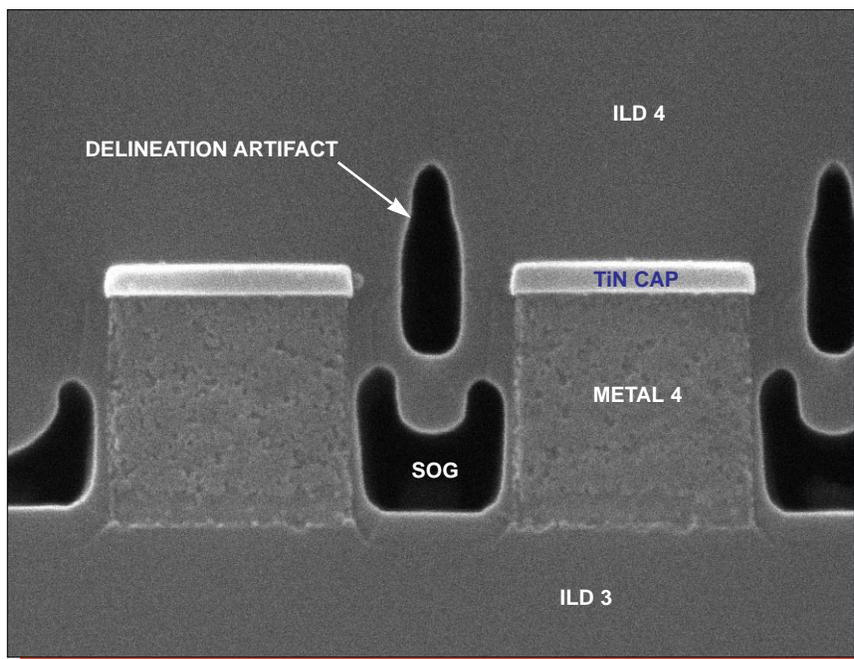


Mag. 52,000x

Figure 22a. Additional SEM section views of metal 5-to-metal 4 vias.



Mag. 13,000x



Mag. 40,000x

Figure 23. SEM section views of metal 4 line profiles.

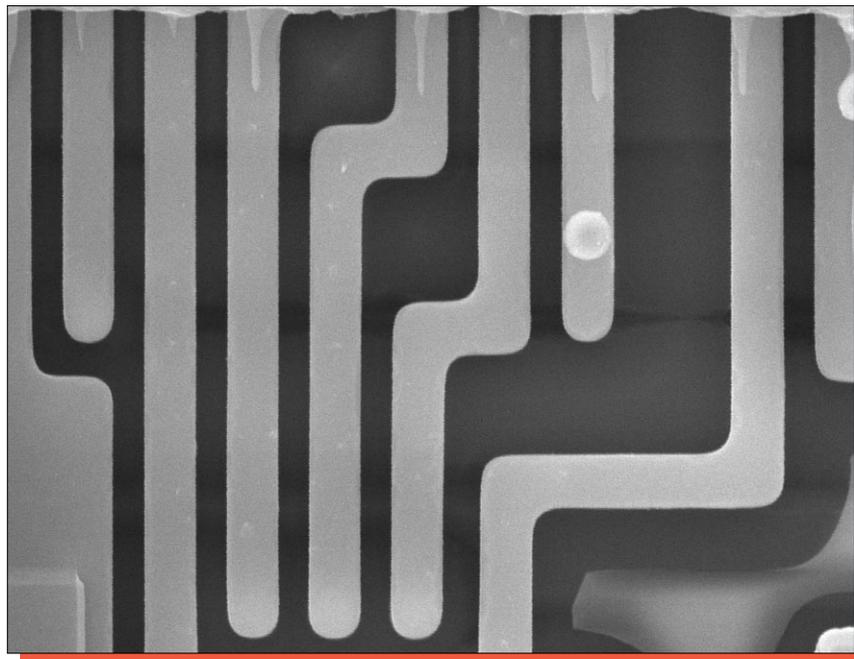
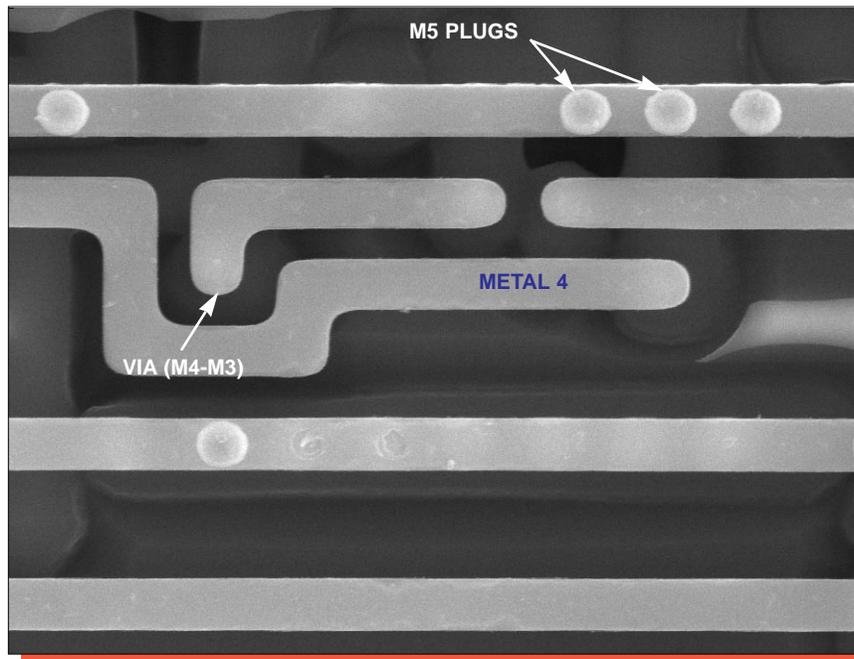
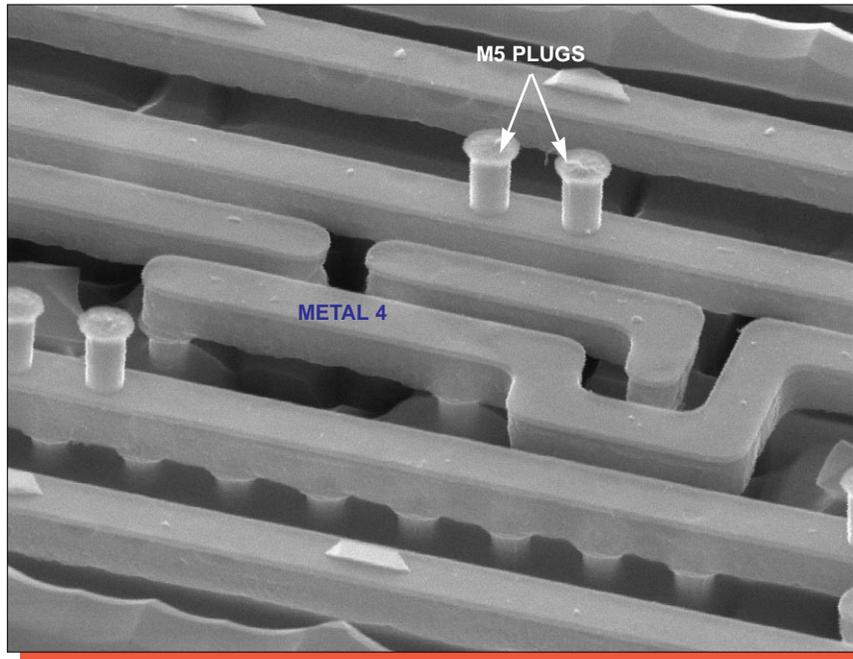
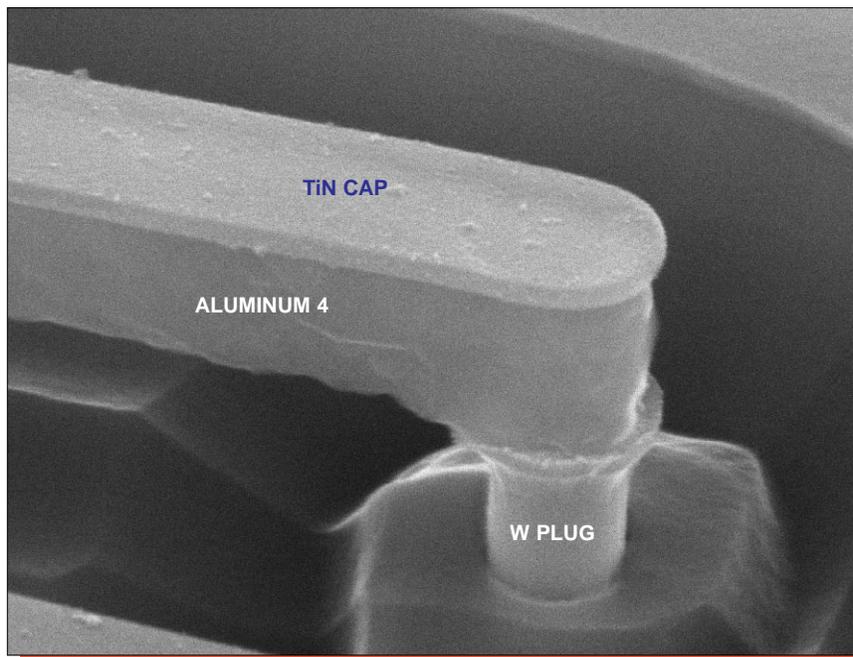


Figure 24. Topological SEM views of metal 4 patterning. Mag. 8400x, 0°.

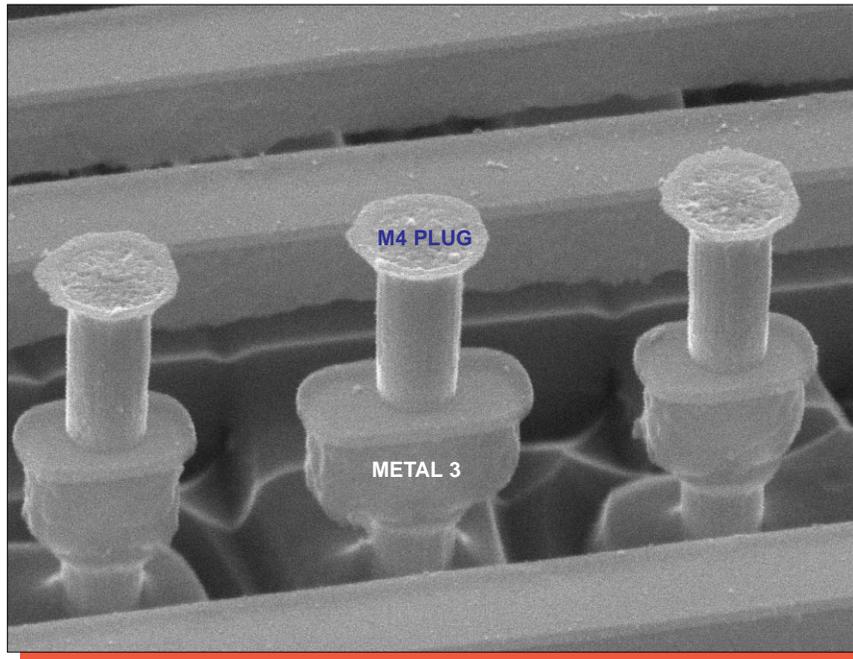


Mag. 10,000x

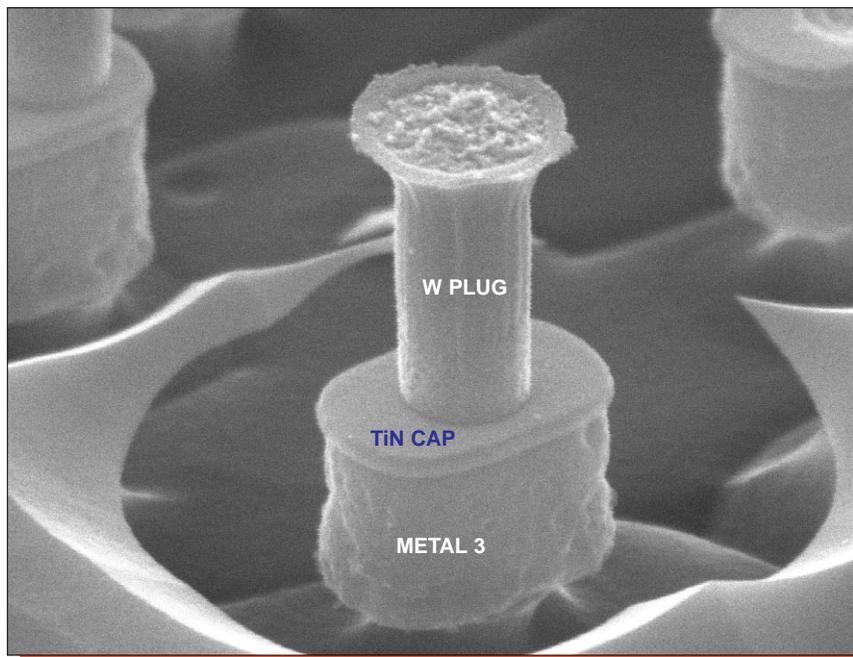


Mag. 35,000x

Figure 25. SEM views of metal 4 coverage. 55°.

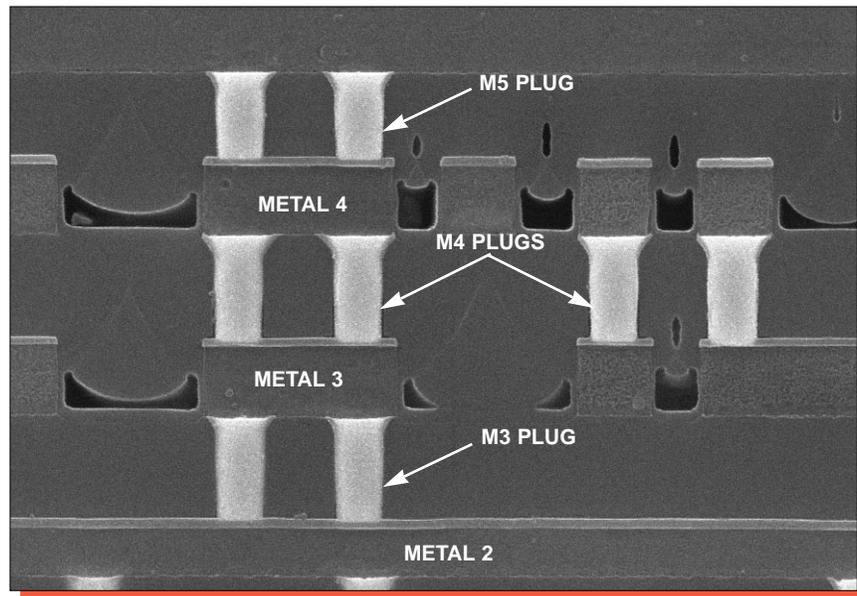


Mag. 20,000x

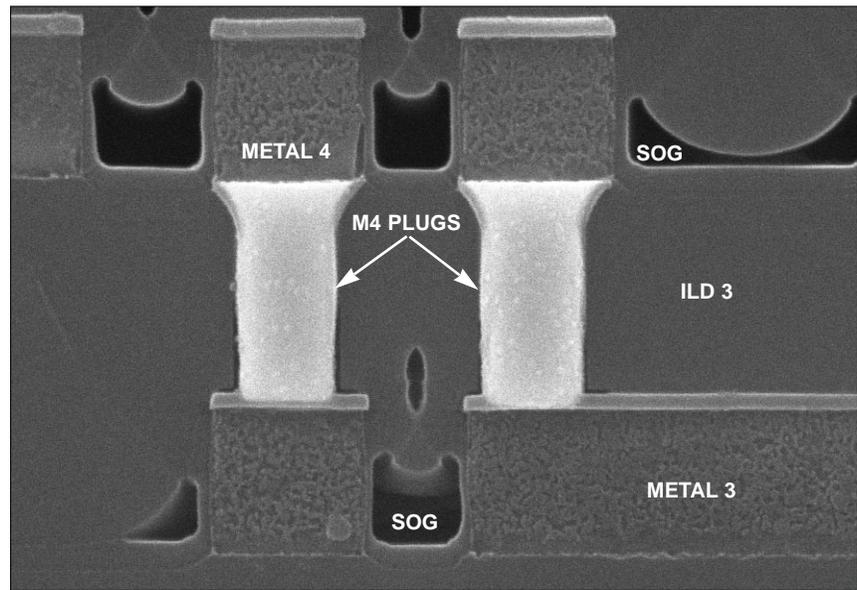


Mag. 35,000x

Figure 26. SEM views of metal 4 plugs. 55°.

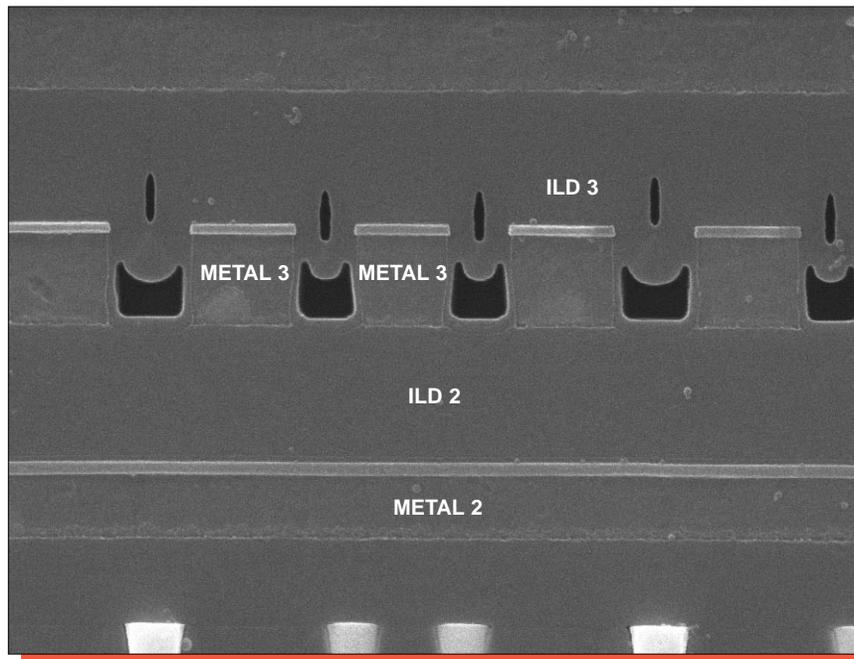


Mag. 12,000x

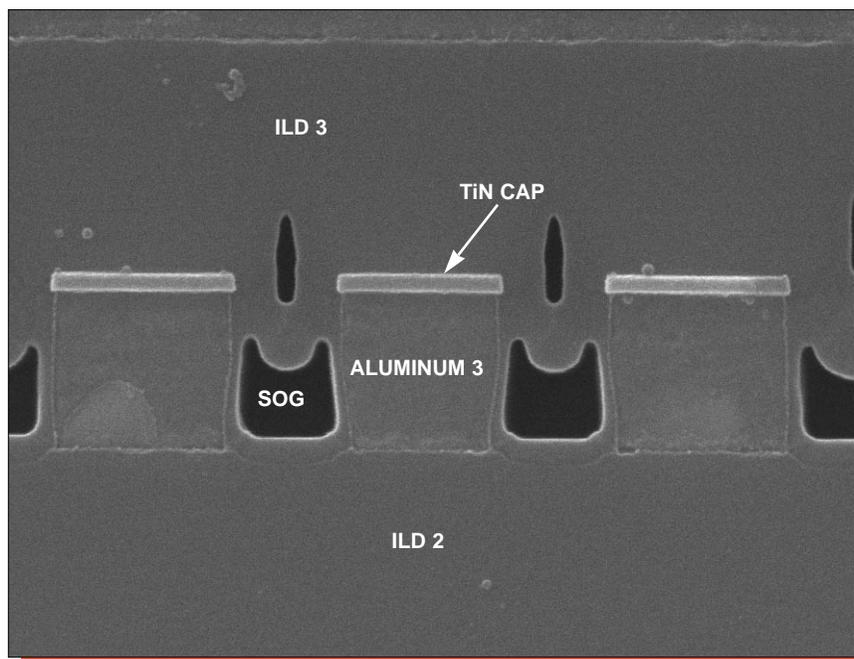


Mag. 25,000x

Figure 27. SEM section views of metal 4-to-metal 3 vias.

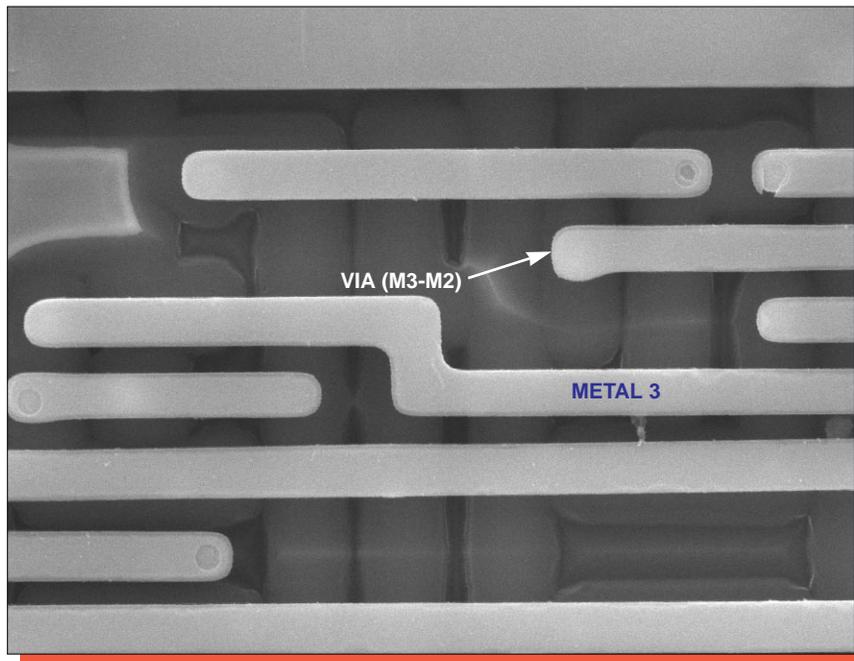


Mag. 15,000x

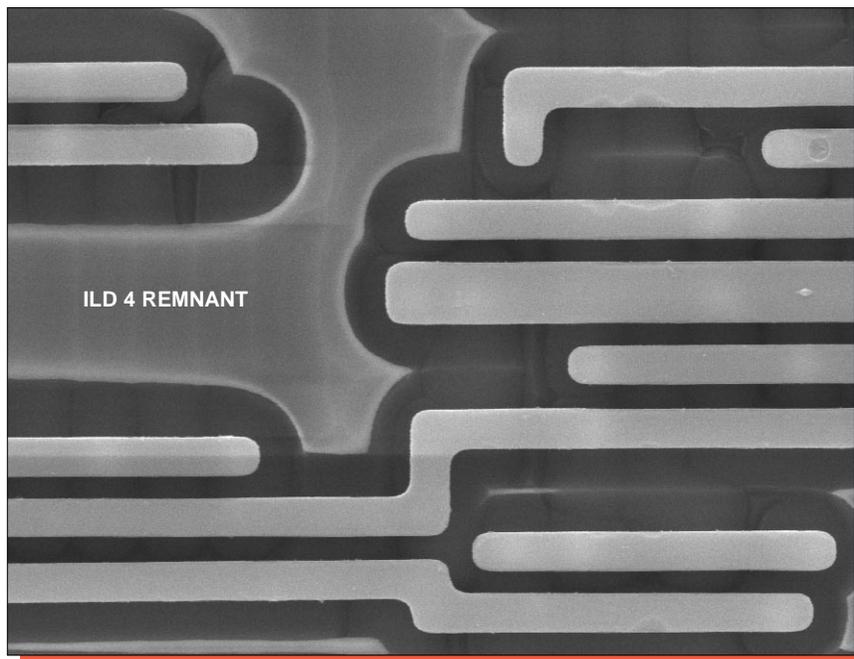


Mag. 26,000x

Figure 28. SEM section views of metal 3 line profiles.

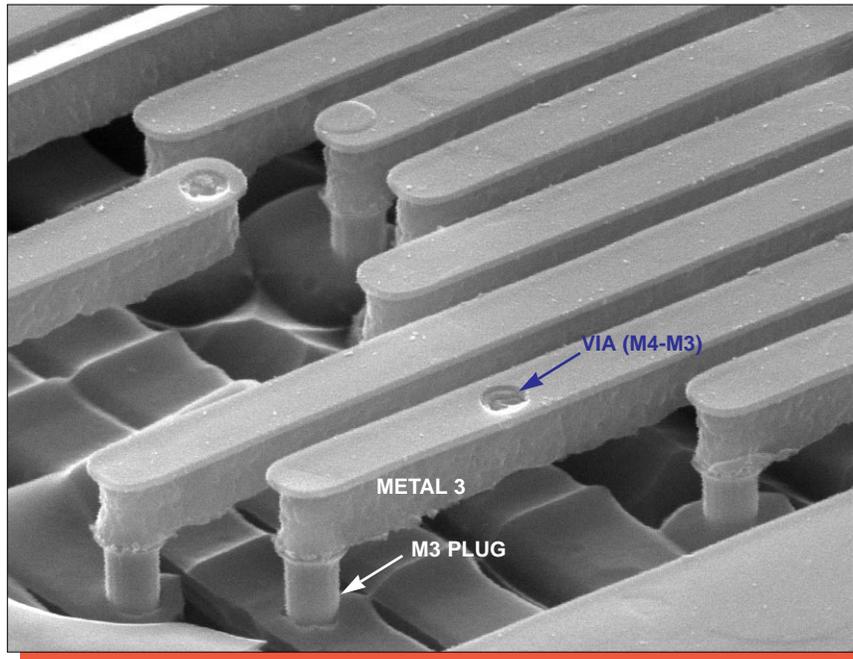


Mag. 7000x

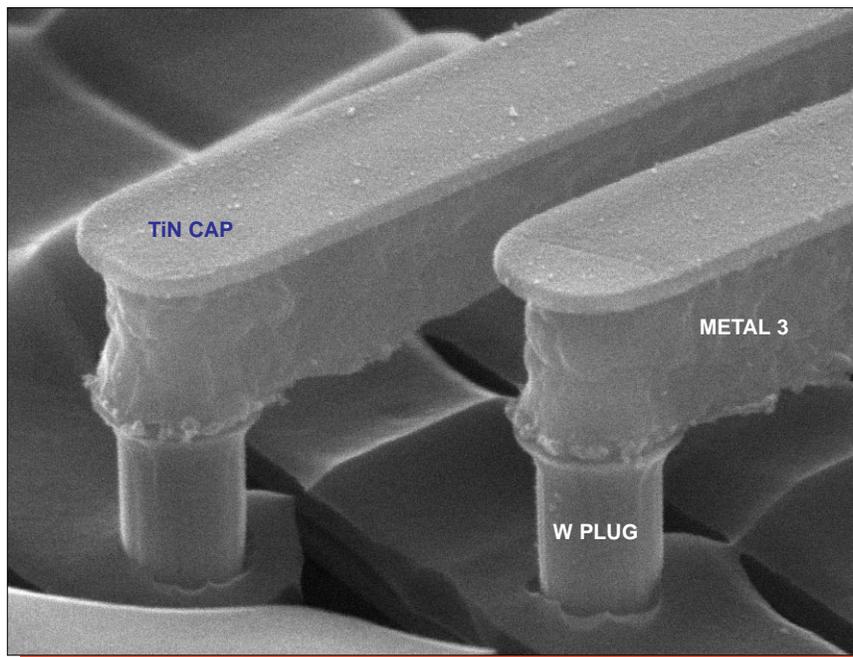


Mag. 6000x

Figure 29. Topological SEM views of metal 3 patterning. 0°.



Mag. 13,500x



Mag. 30,000x

Figure 30. SEM views of metal 3 coverage. 60°.

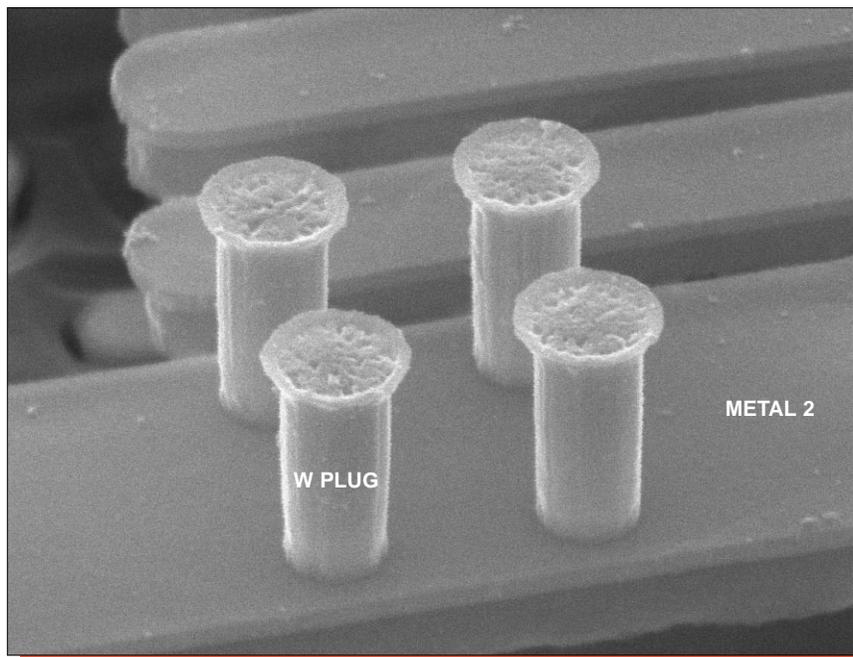
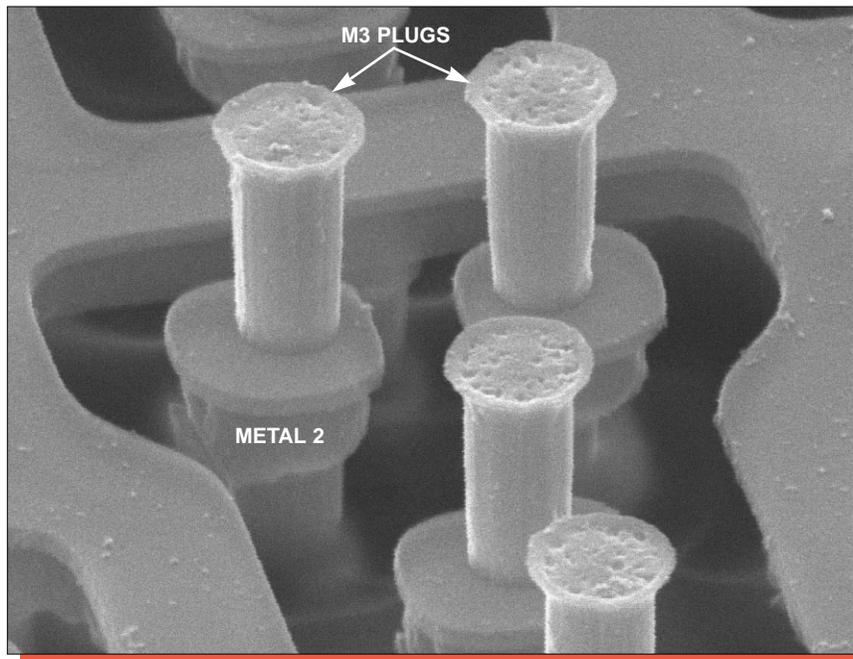
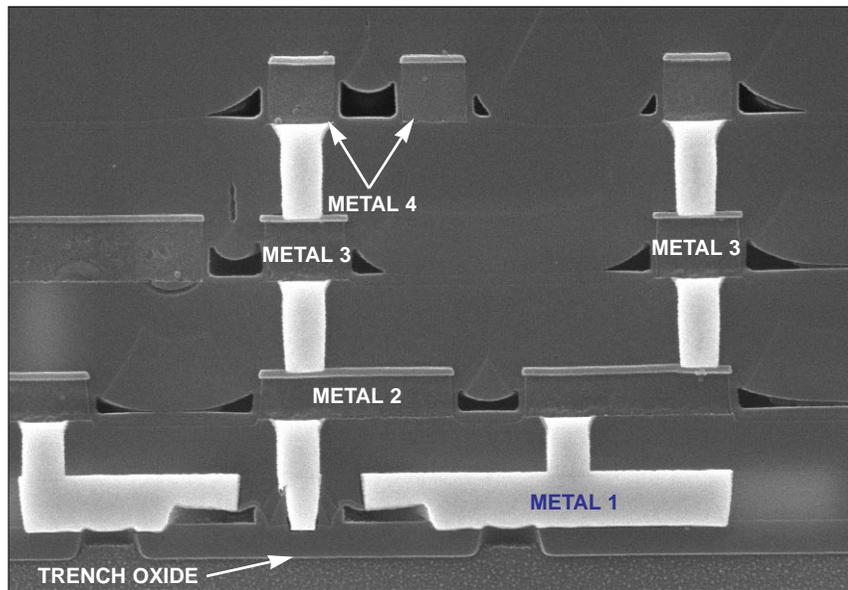
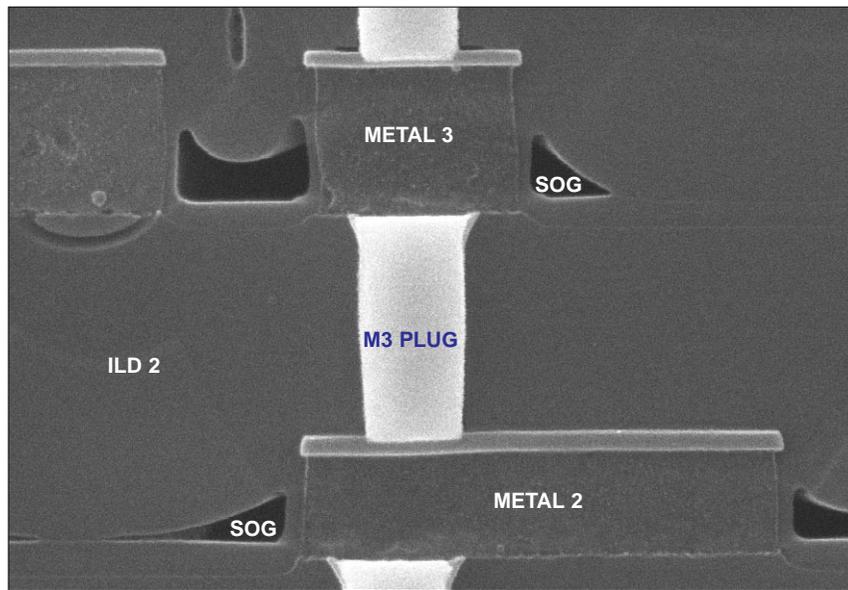


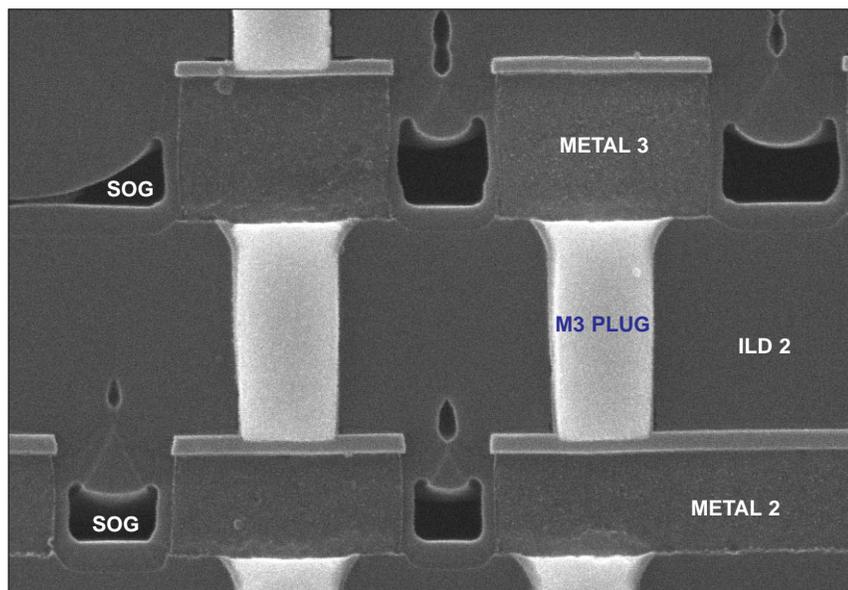
Figure 31. SEM views of metal 3 plugs. Mag. 27,000x, 55°.



Mag. 10,000x

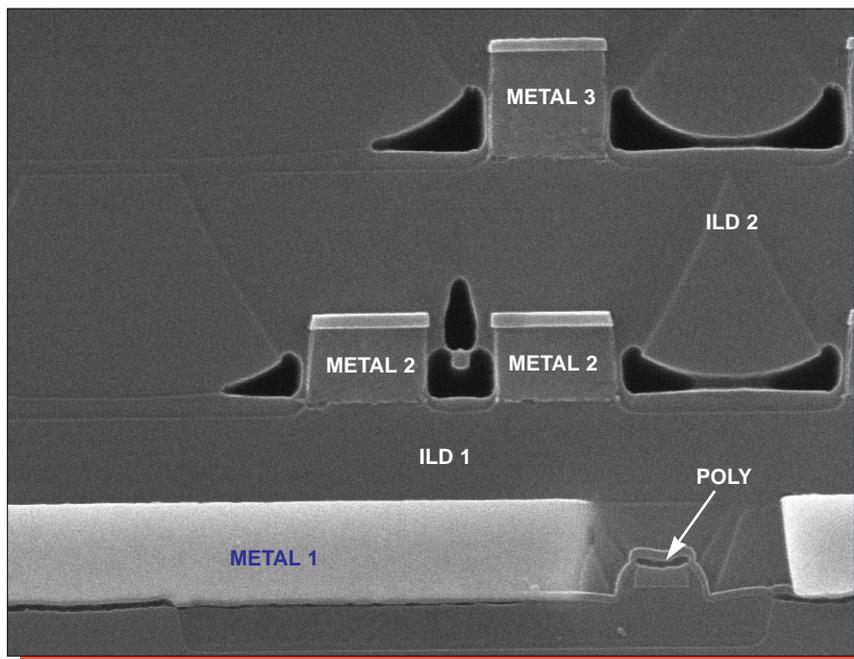


Mag. 25,000x

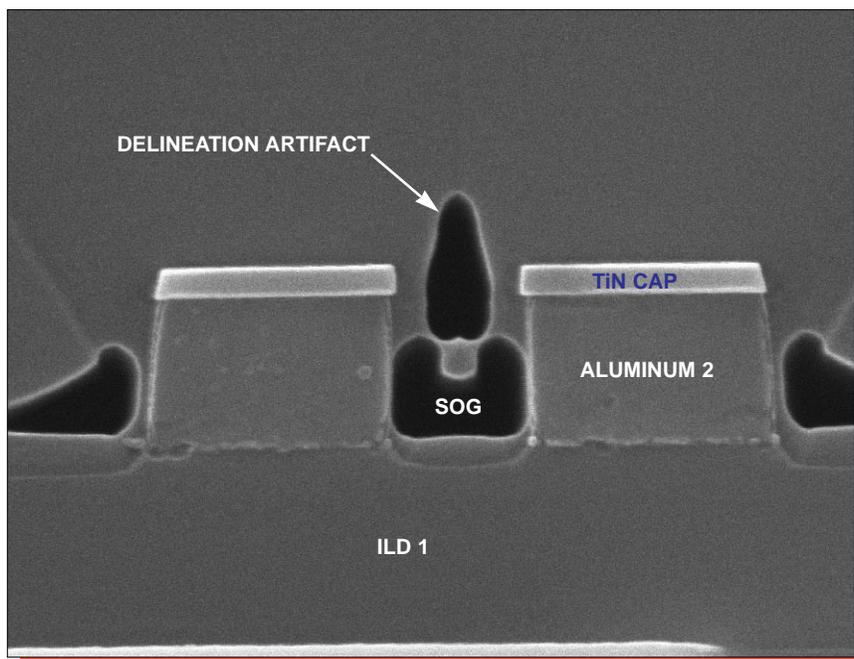


Mag. 25,000x

Figure 32. SEM section views of metal 3-to-metal 2 vias.

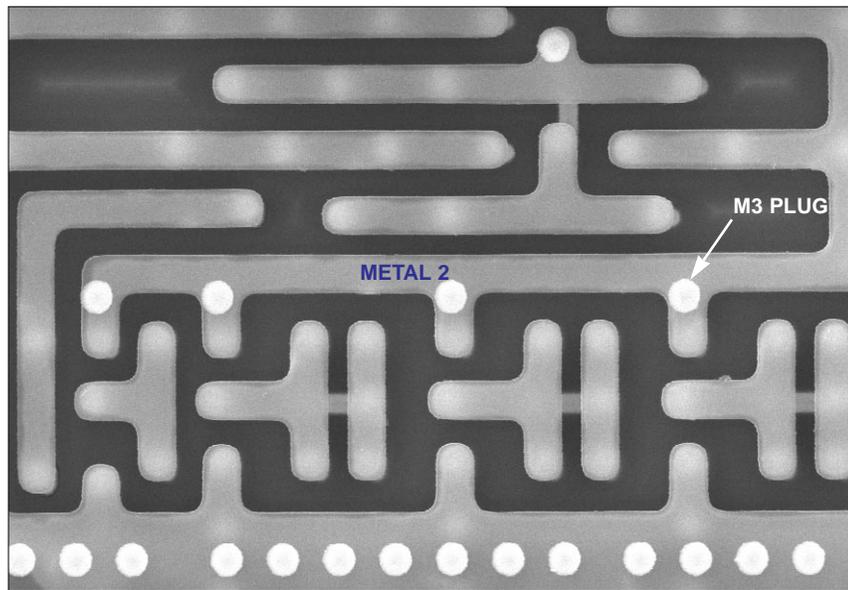


Mag. 17,600x

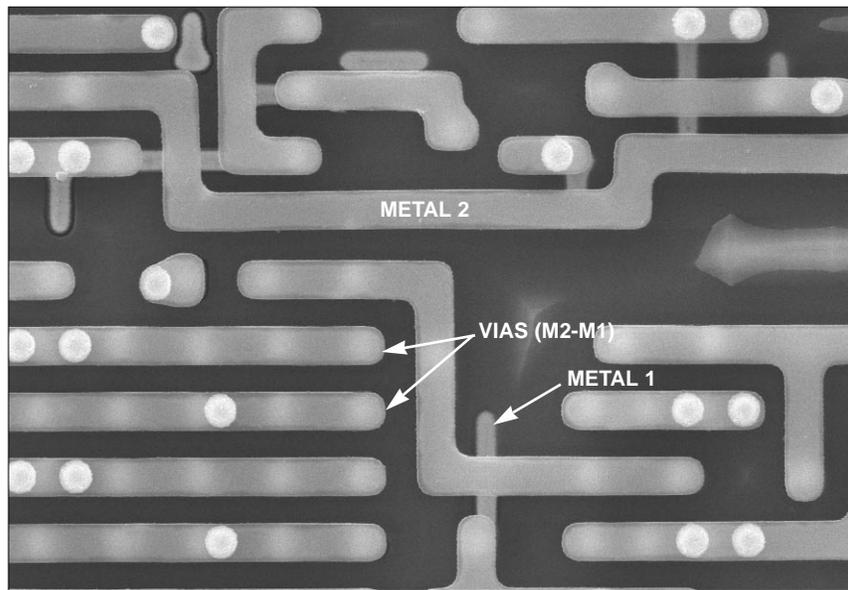


Mag. 35,000x

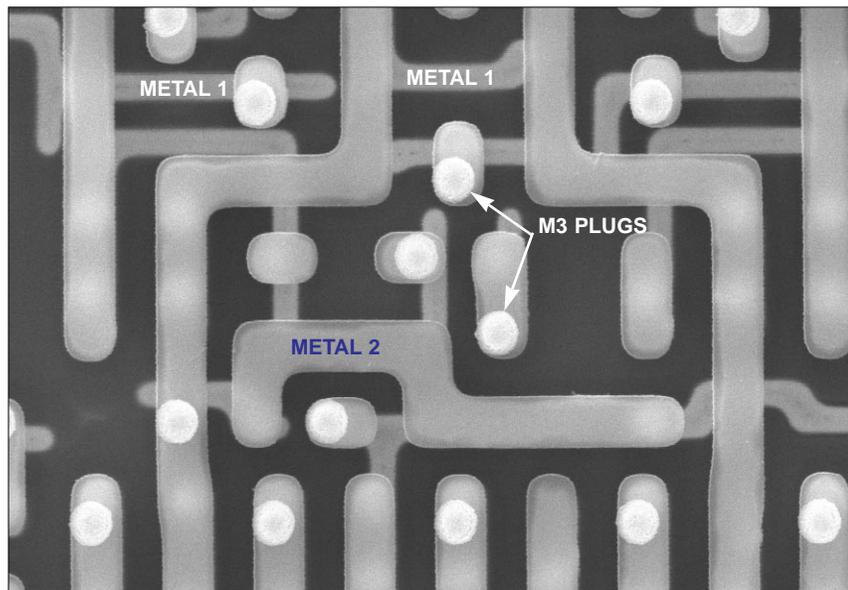
Figure 33. SEM section views of metal 2 line profiles.



Mag. 5500x

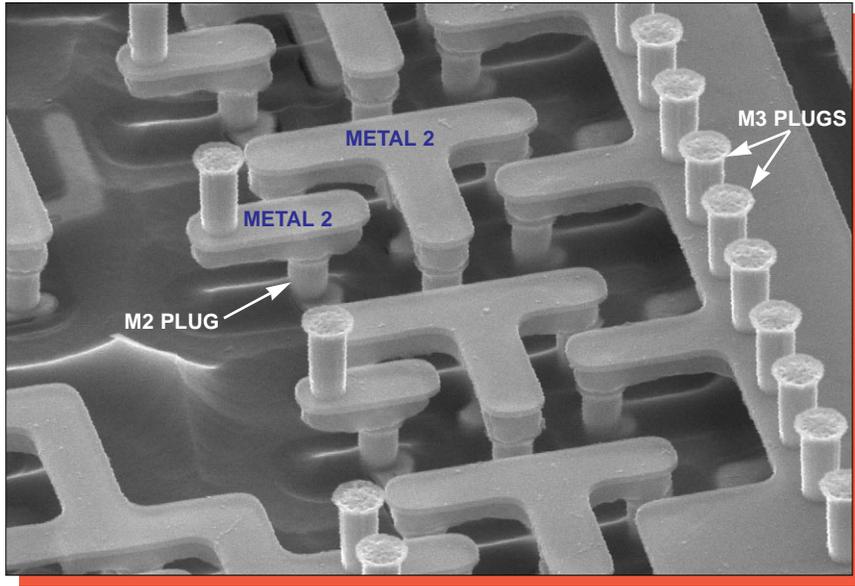


Mag. 5700x

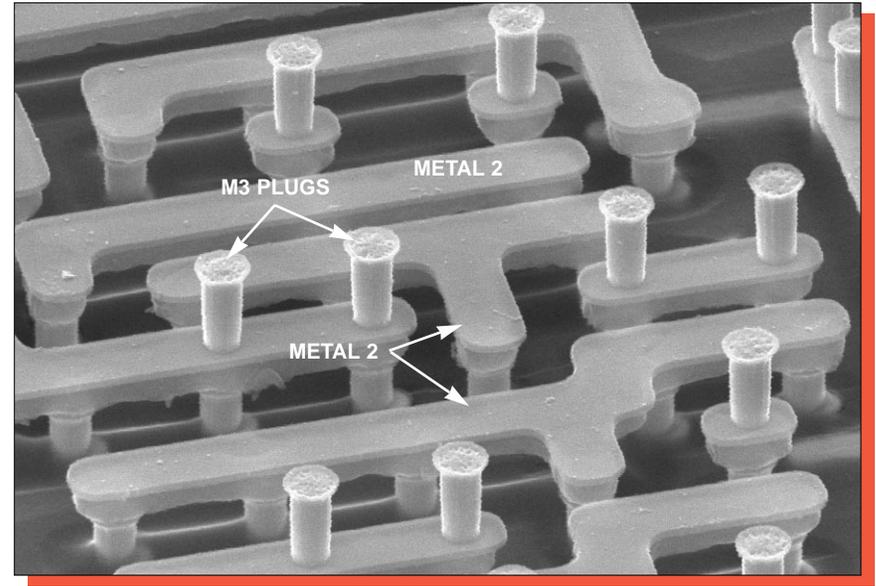


Mag. 7400x

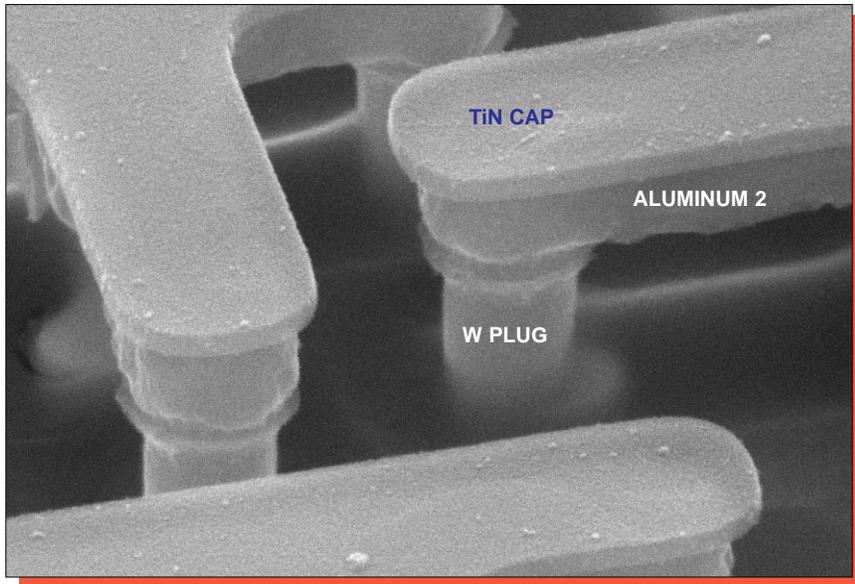
Figure 34. Topological SEM views of metal 2 patterning. 0°.



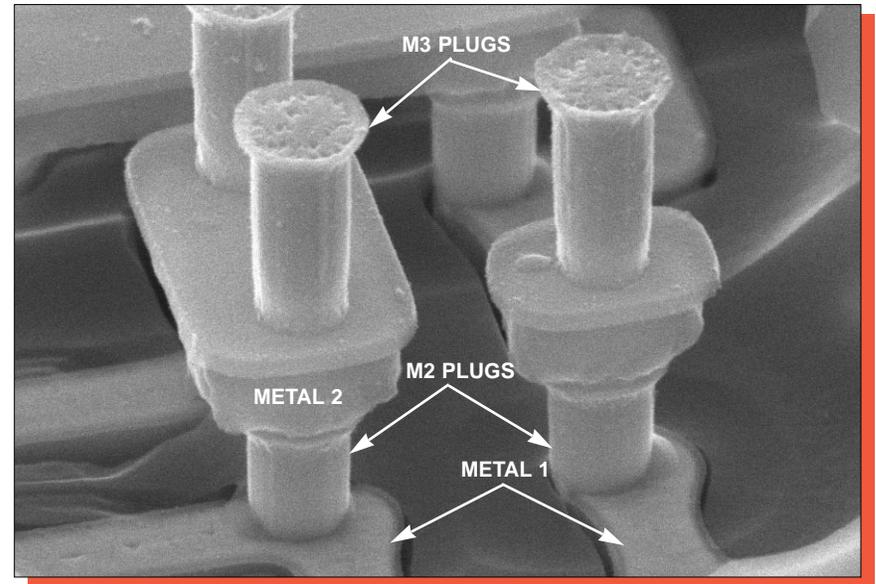
Mag. 9000x



Mag. 10,000x

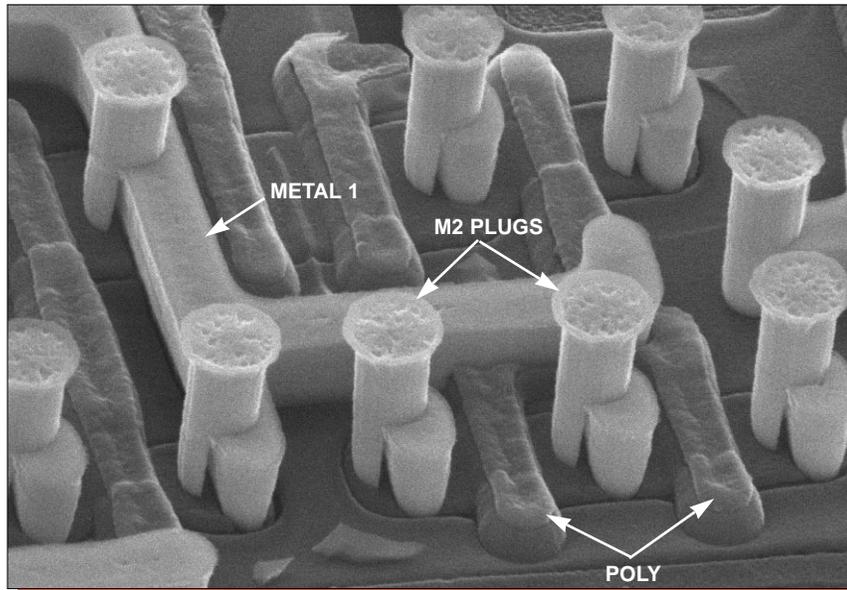


Mag. 30,000x

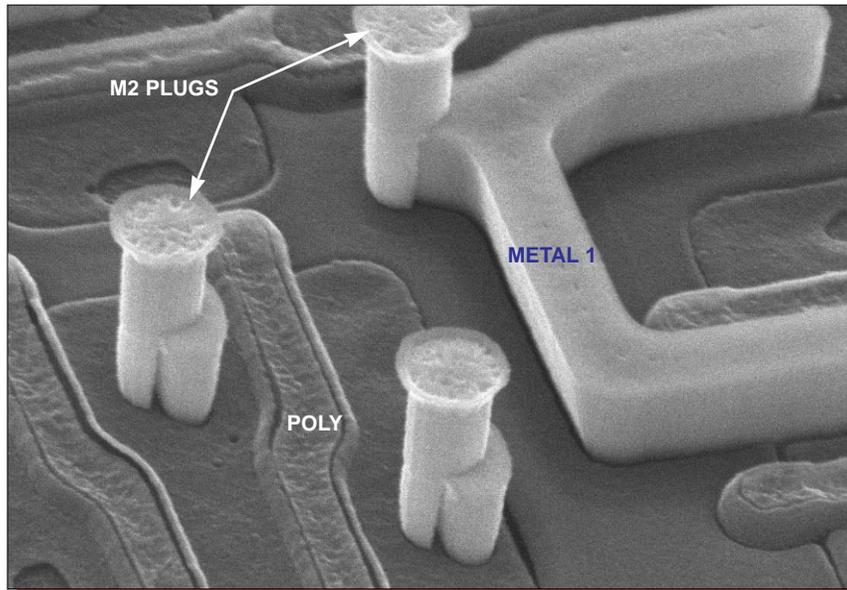


Mag. 23,000x

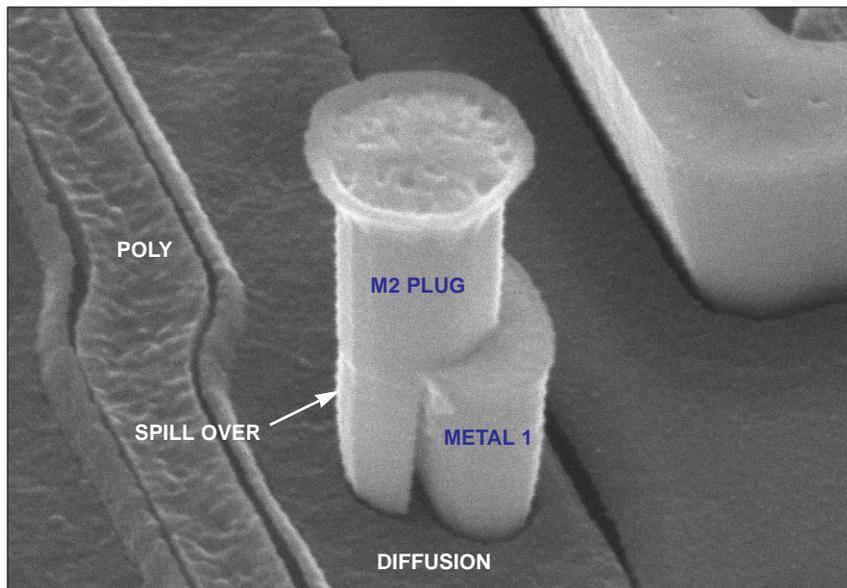
Figure 35. SEM views of metal 2 coverage. 55°.



Mag. 18,000x

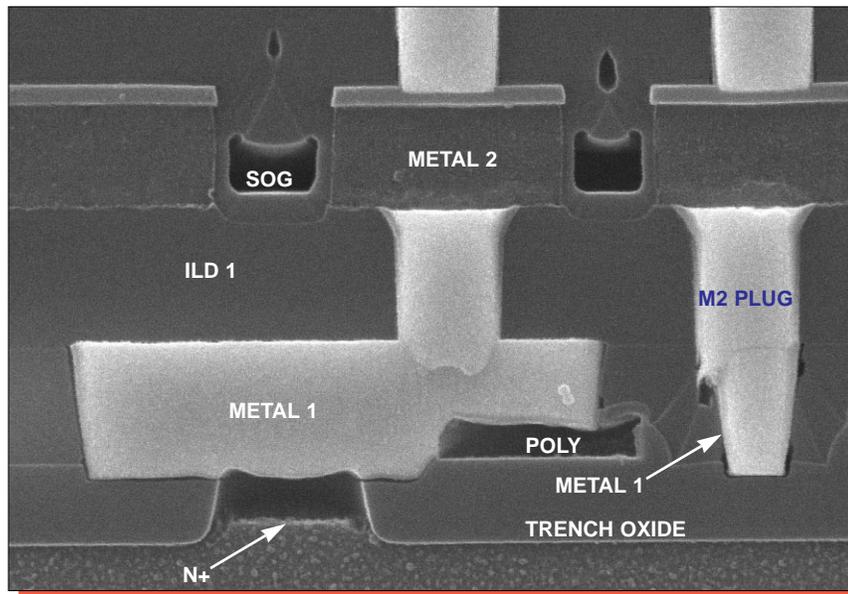


Mag. 20,000x

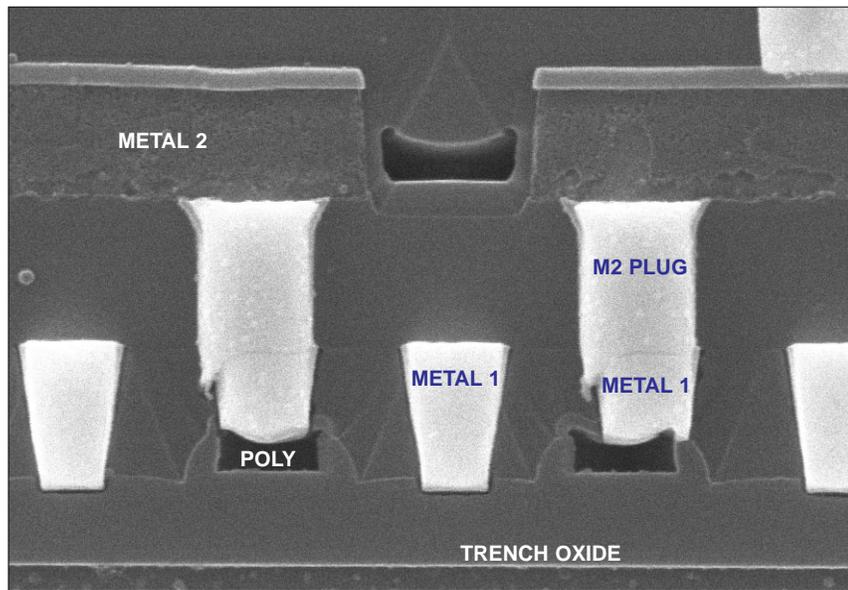


Mag. 40,000x

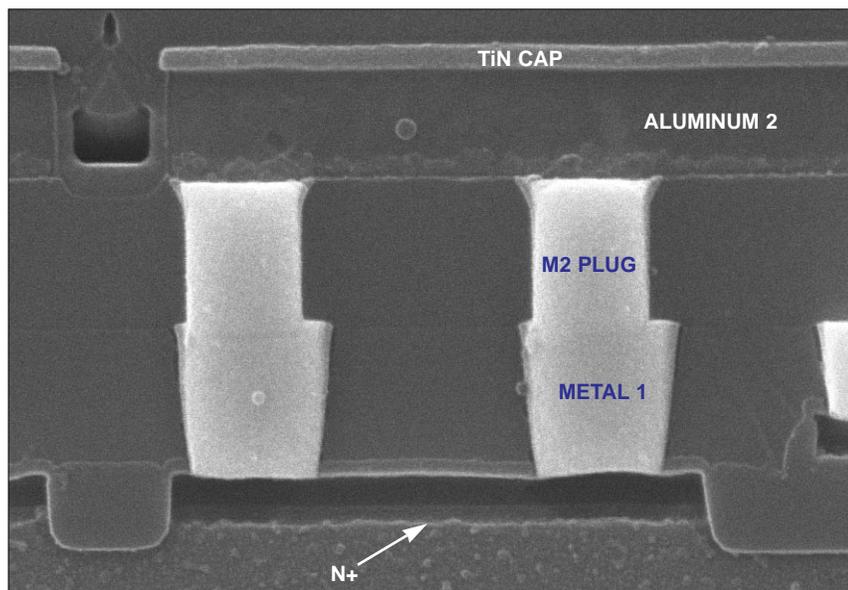
Figure 36. SEM views of metal 2 plugs. 50°.



Mag. 25,000x



Mag. 26,000x



Mag. 26,000x

Figure 37. SEM section views of metal 2-to-metal 1 vias.

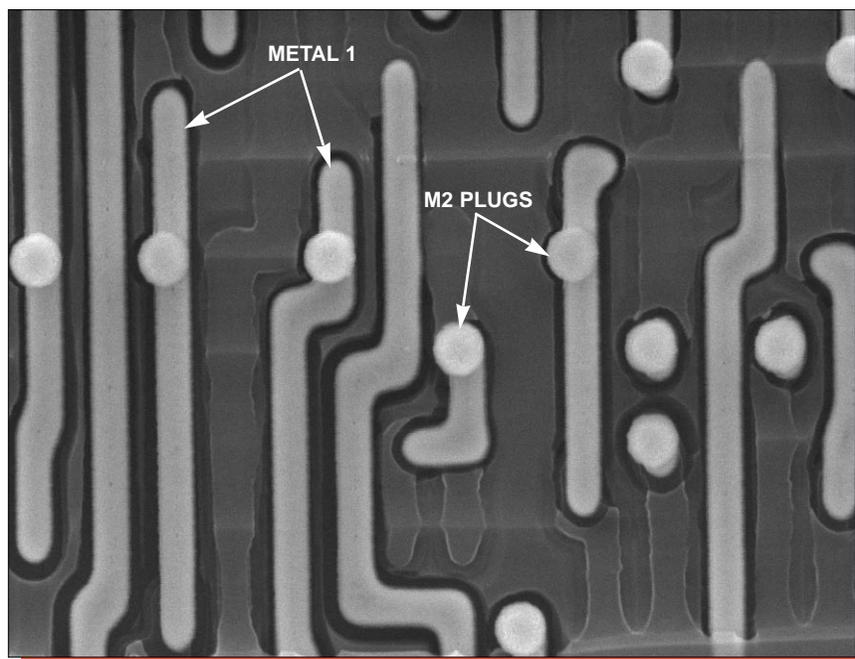
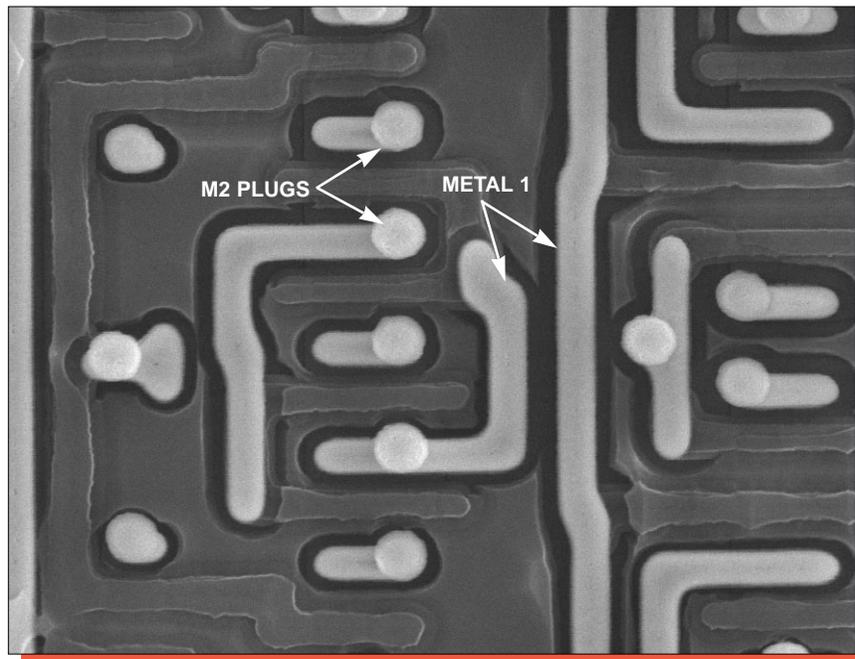
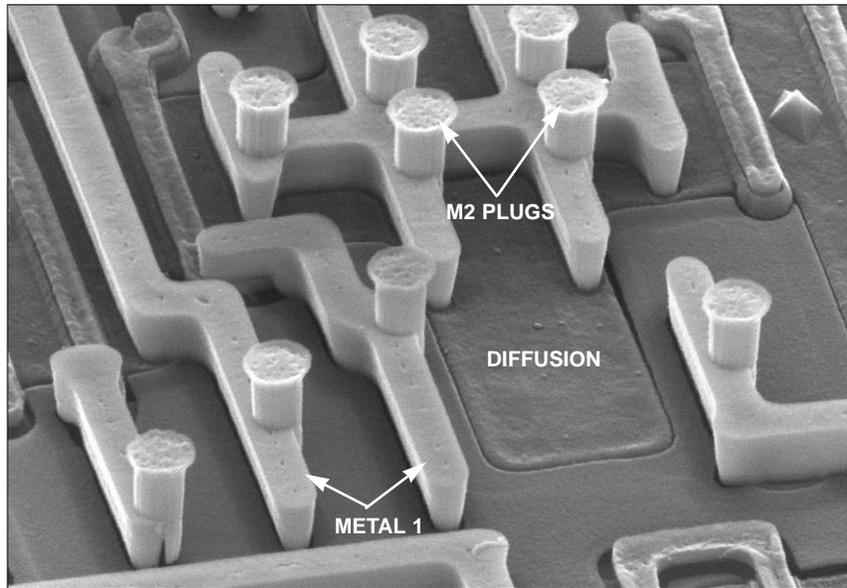
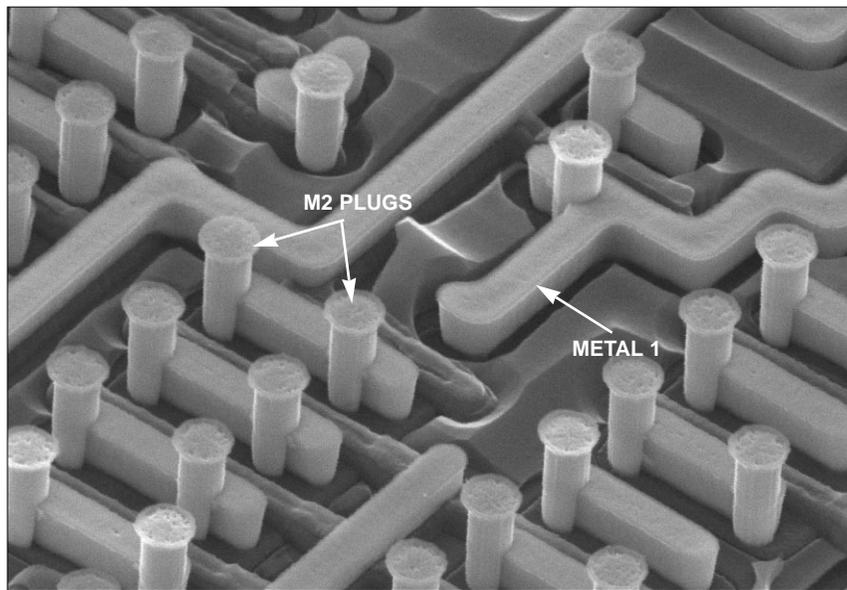


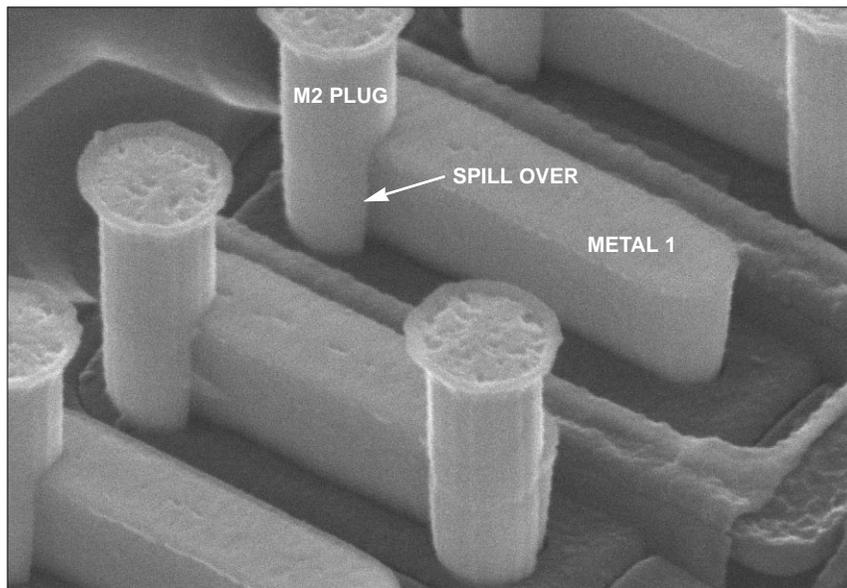
Figure 38. Topological SEM views of metal 1 patterning. Mag. 9000x, 0°.



Mag. 12,400x

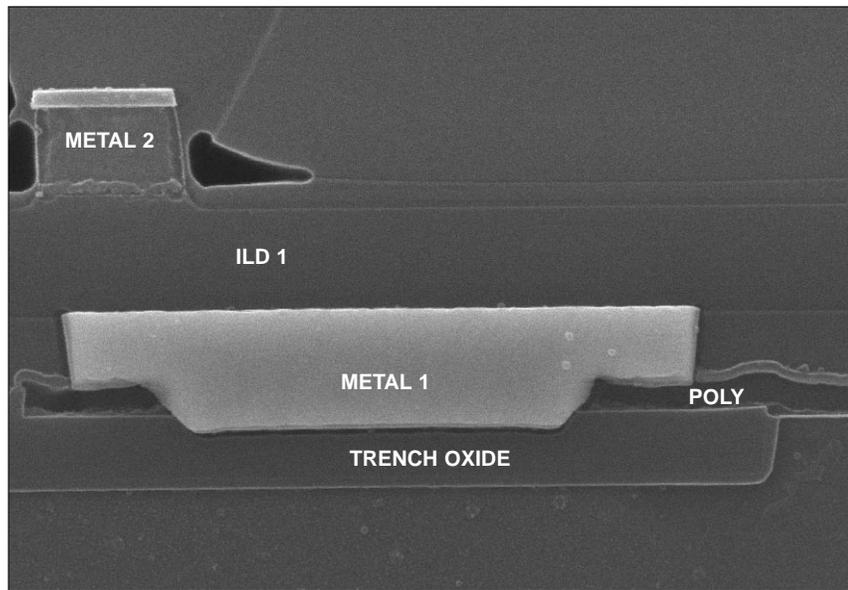


Mag. 11,400x

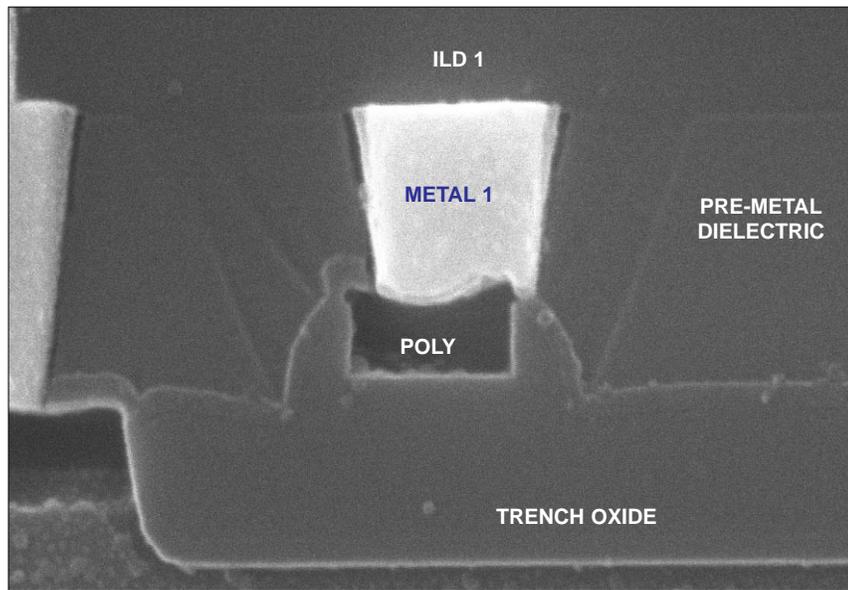


Mag. 30,000x

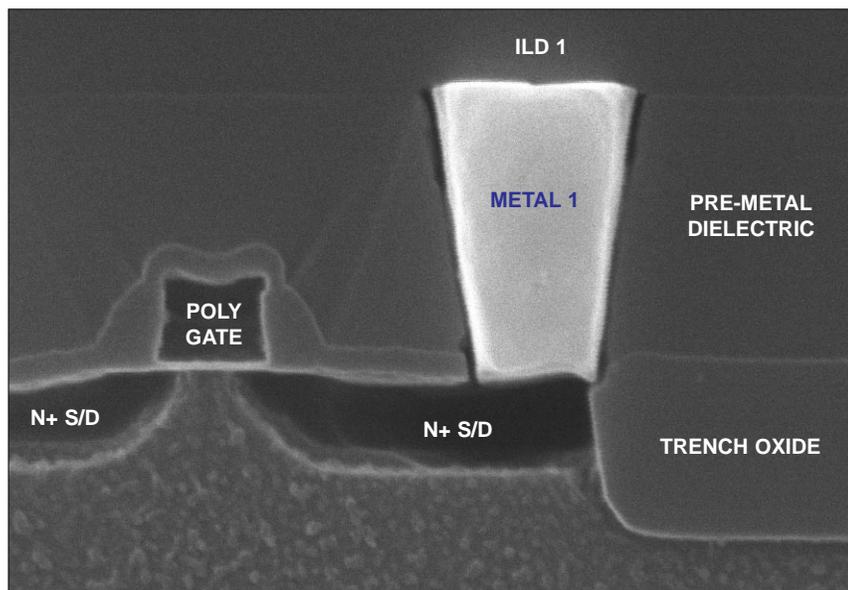
Figure 39. SEM views of general metal 1 coverage. 55°.



Mag. 20,000x

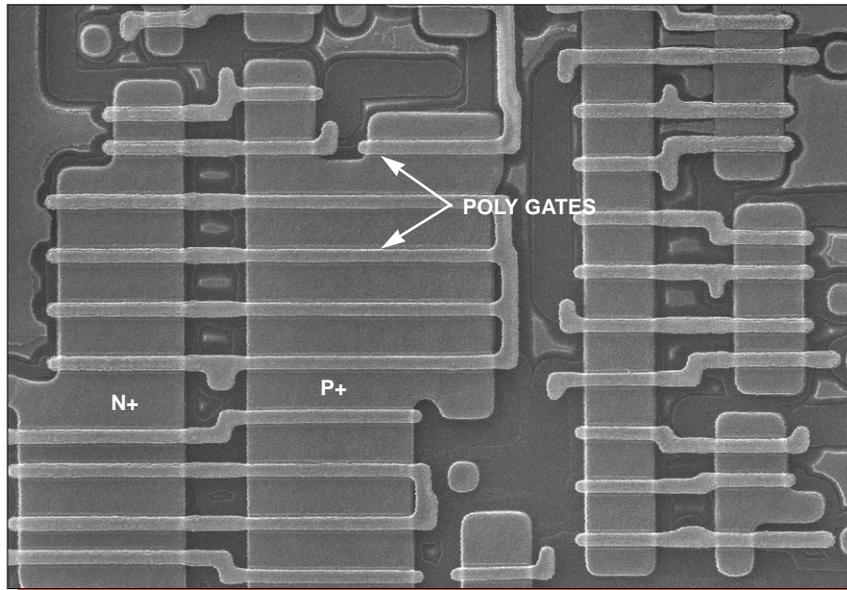


Mag. 52,000x

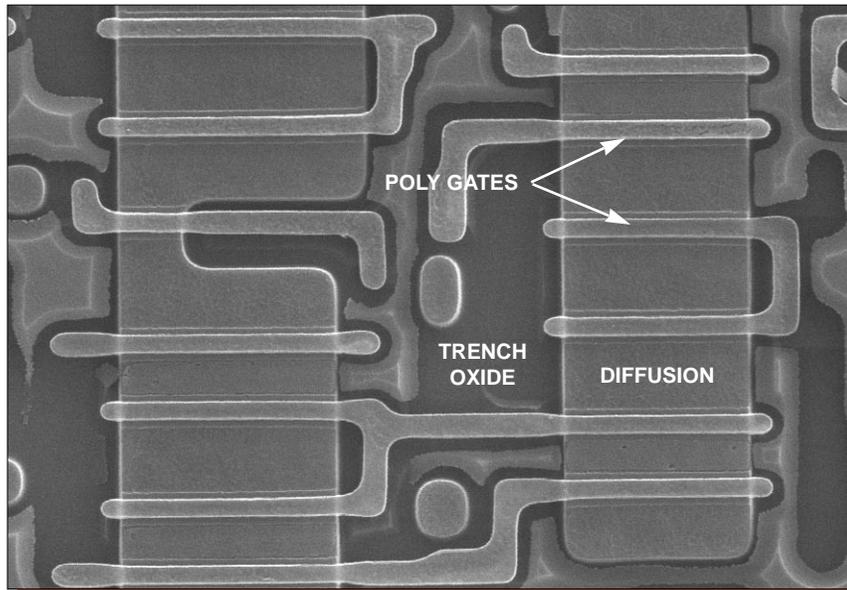


Mag. 50,000x

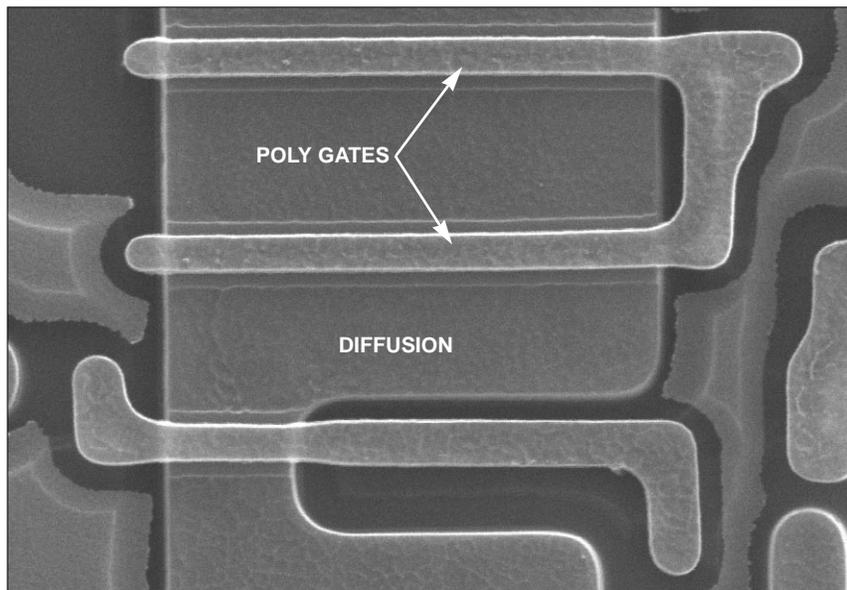
Figure 40. SEM section views of metal 1 contacts.



Mag. 4600x

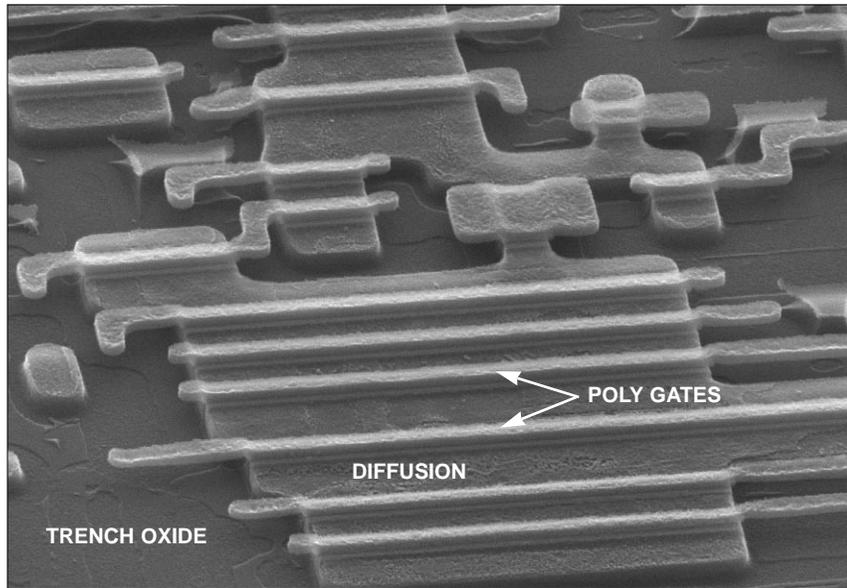


Mag. 8000x

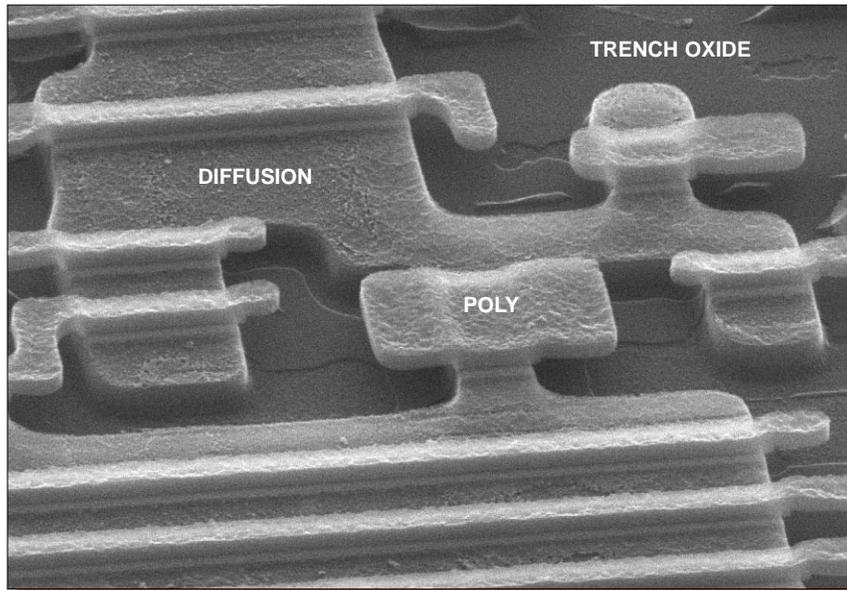


Mag. 16,000x

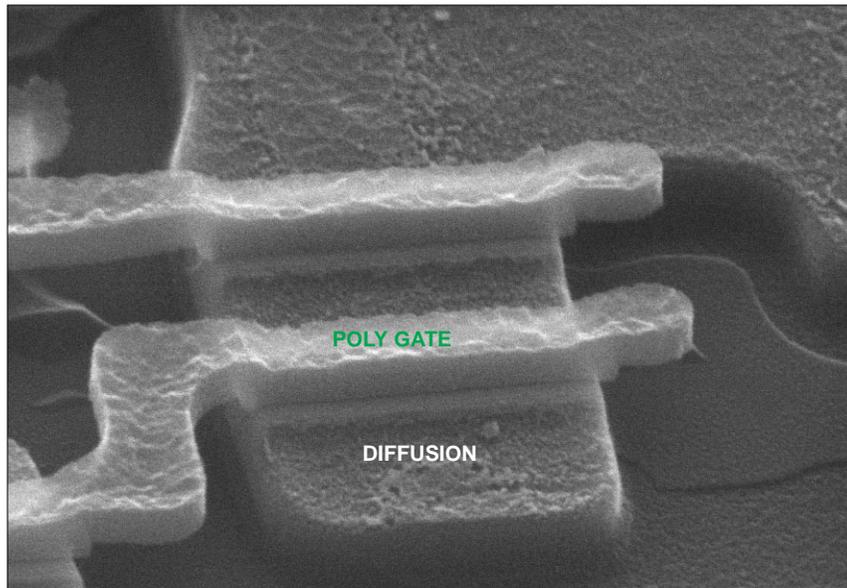
Figure 41. Topological SEM views of poly patterning. 0°.



Mag. 9000x

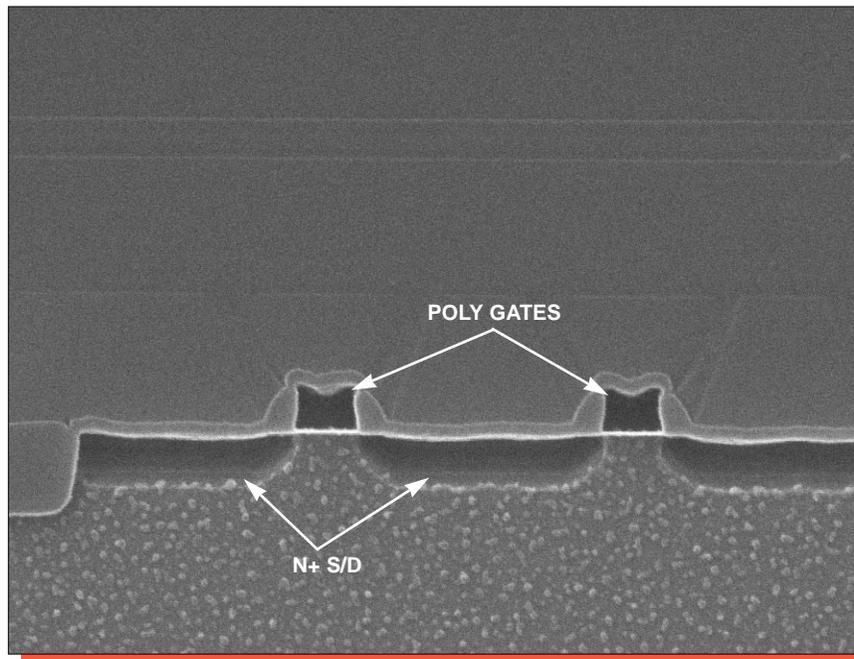


Mag. 15,000x

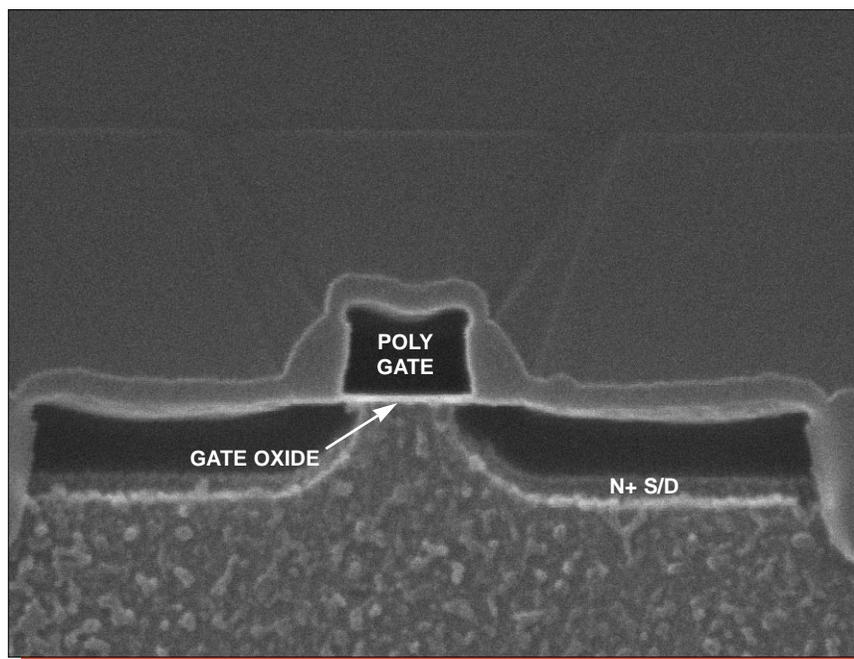


Mag. 35,000x

Figure 42. Perspective SEM views of poly coverage. 55°.

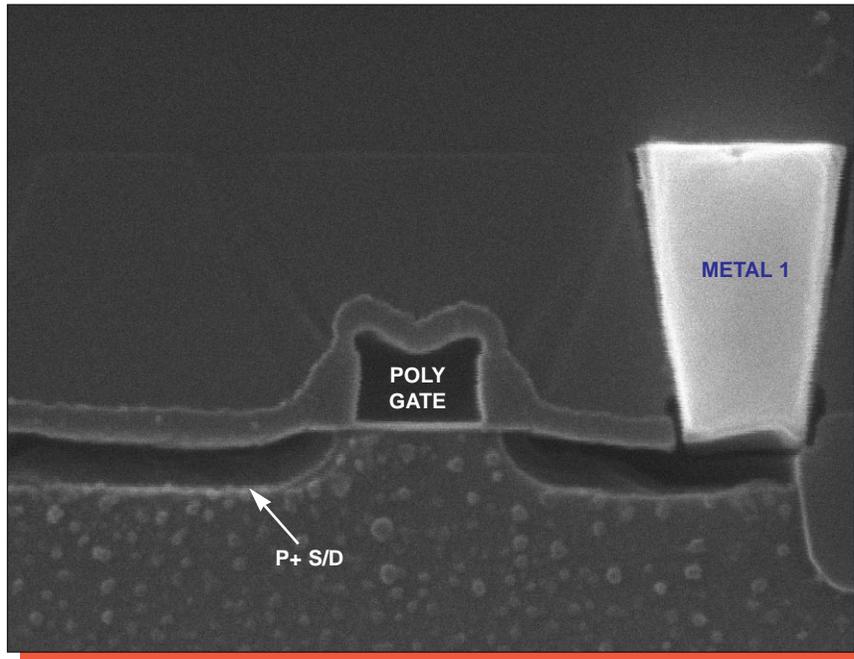


Mag. 26,000x

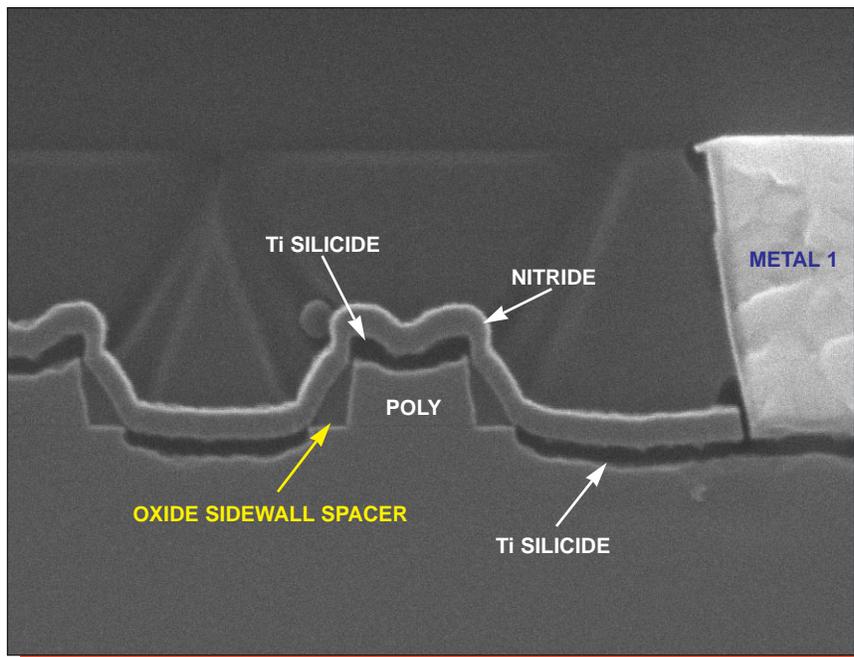


Mag. 52,000x

Figure 43. SEM section views of N-channel transistors.

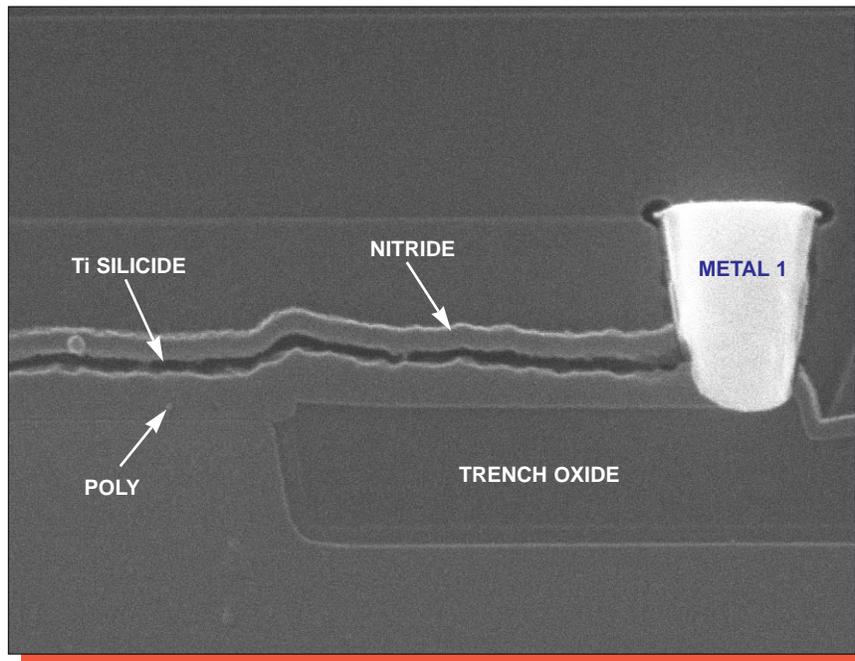


P-channel

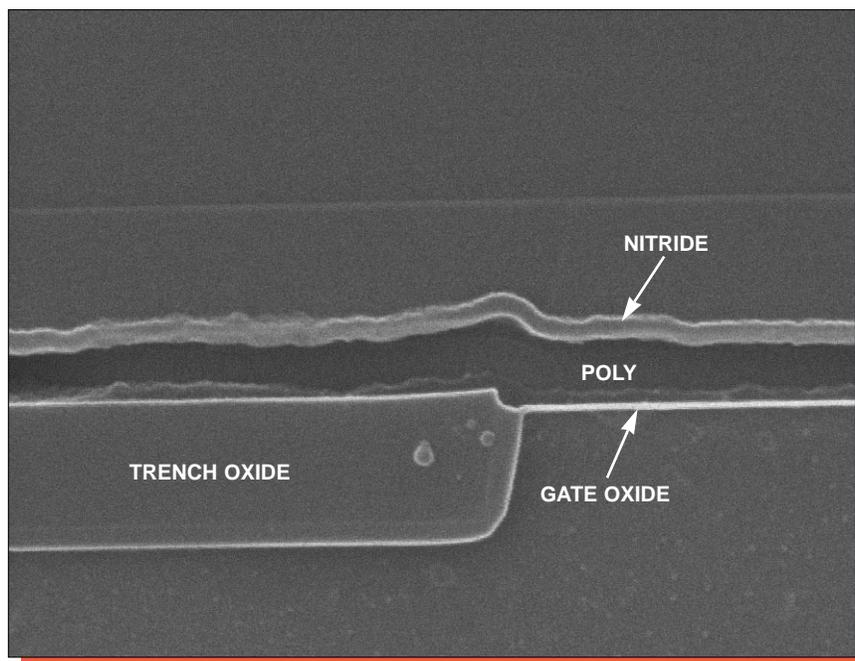


glass etch

Figure 44. SEM section views of typical transistors. Mag. 52,000x.



glass etch



silicon etch

Figure 45. SEM section views of trench oxide isolation. Mag. 40,000x.

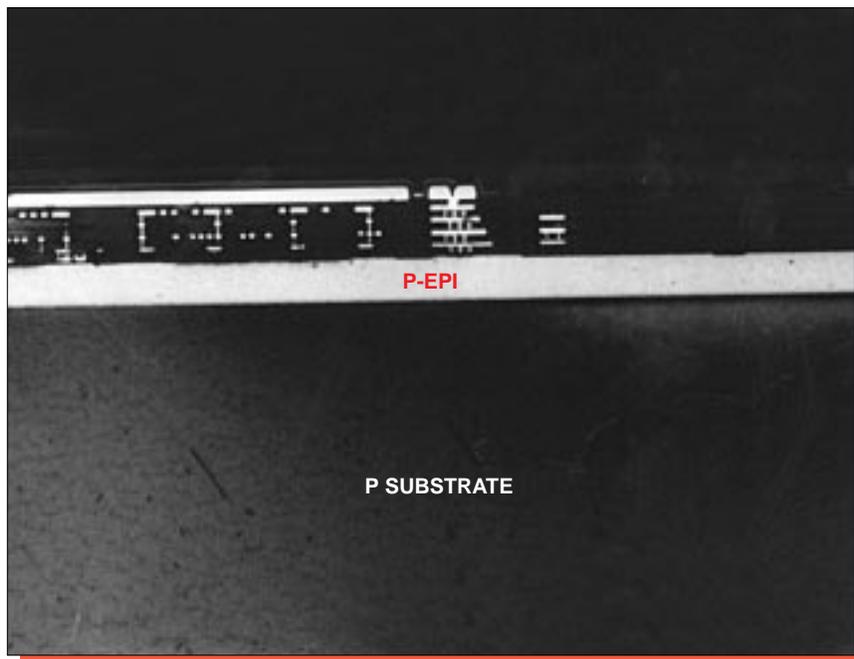
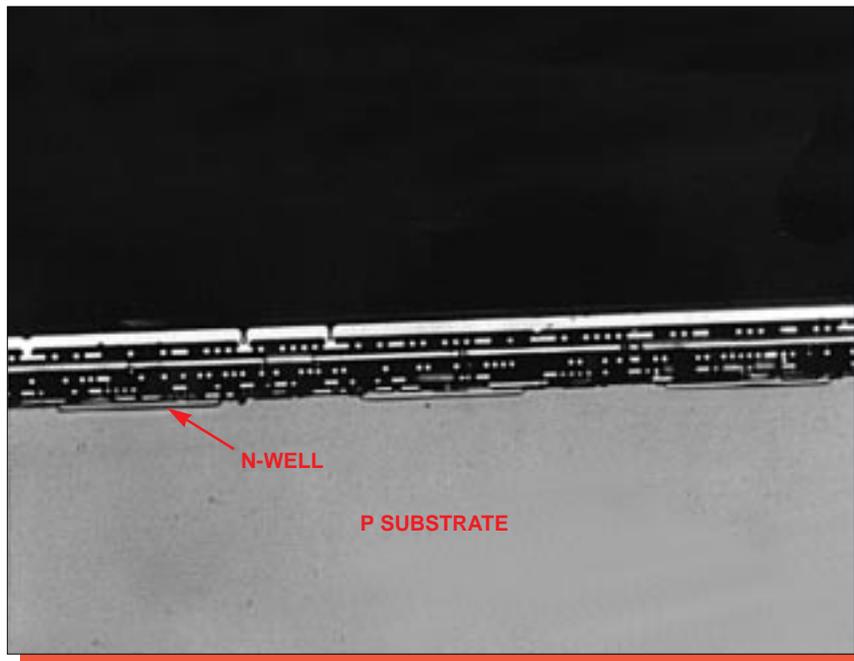
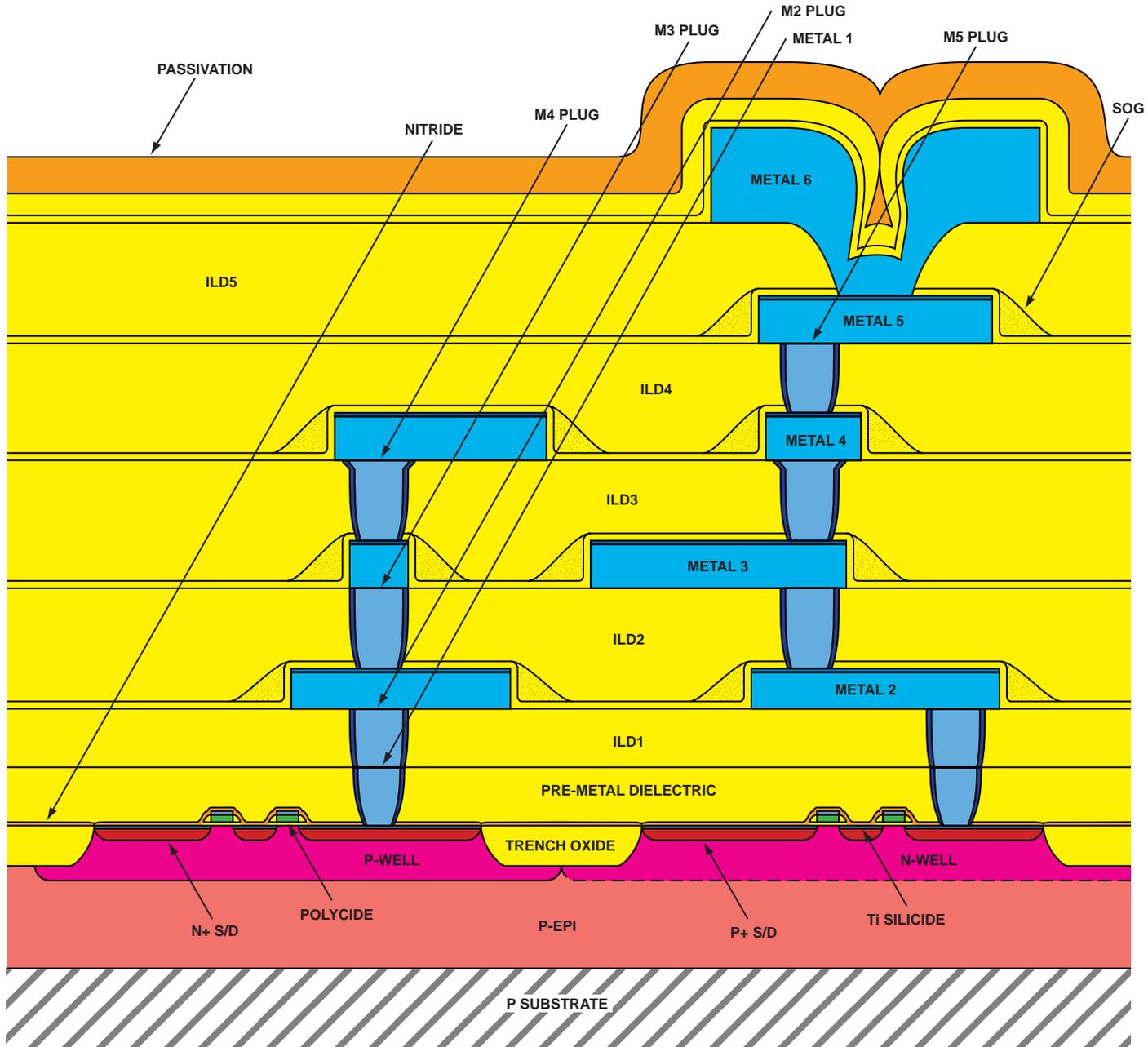
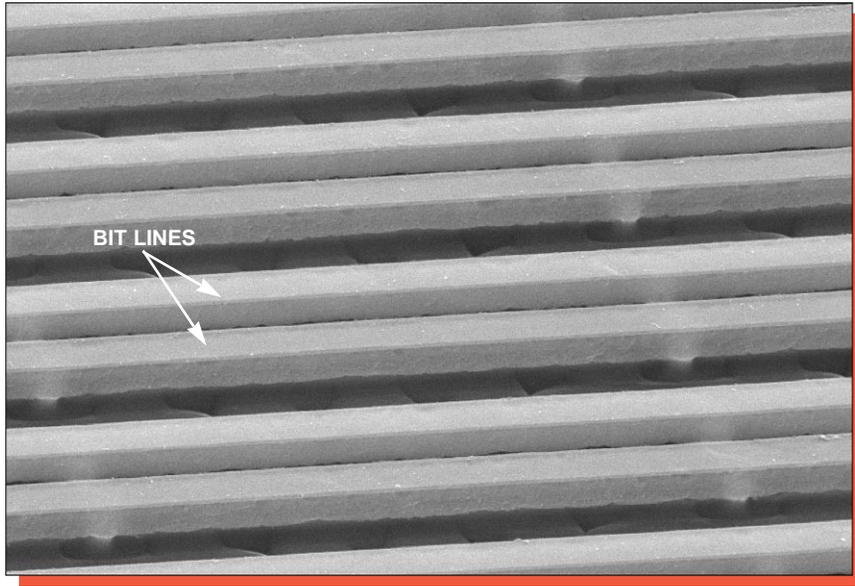


Figure 46. Optical section views of the epi and well structure. Mag. 800x.

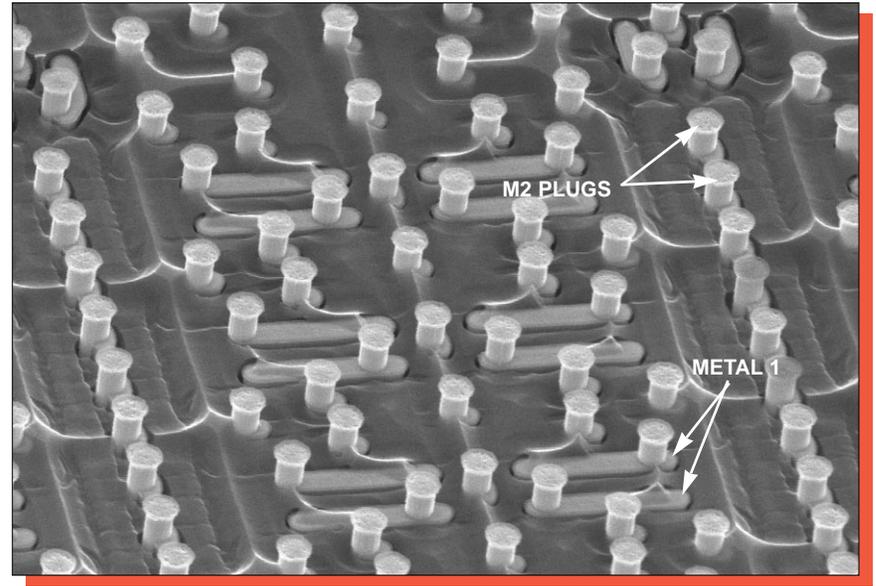


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

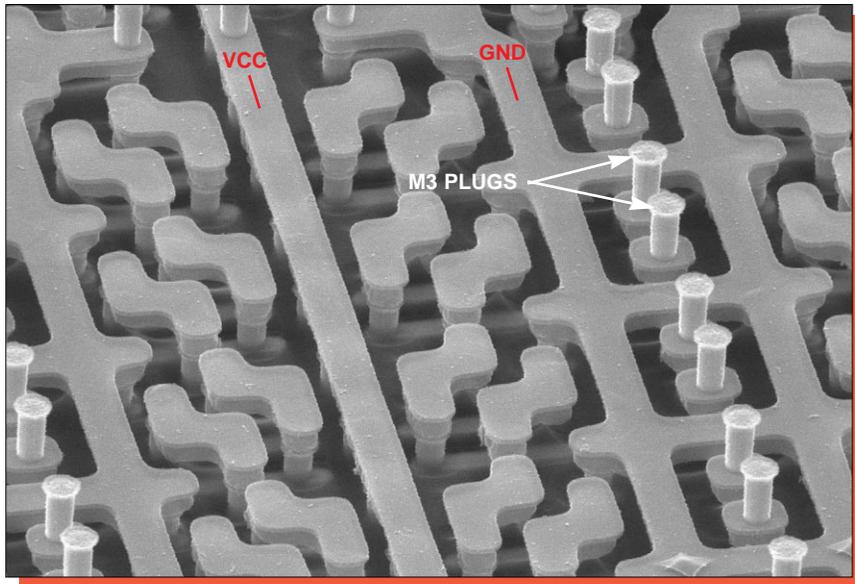
Figure 47. Color cross section drawing illustrating device structure.



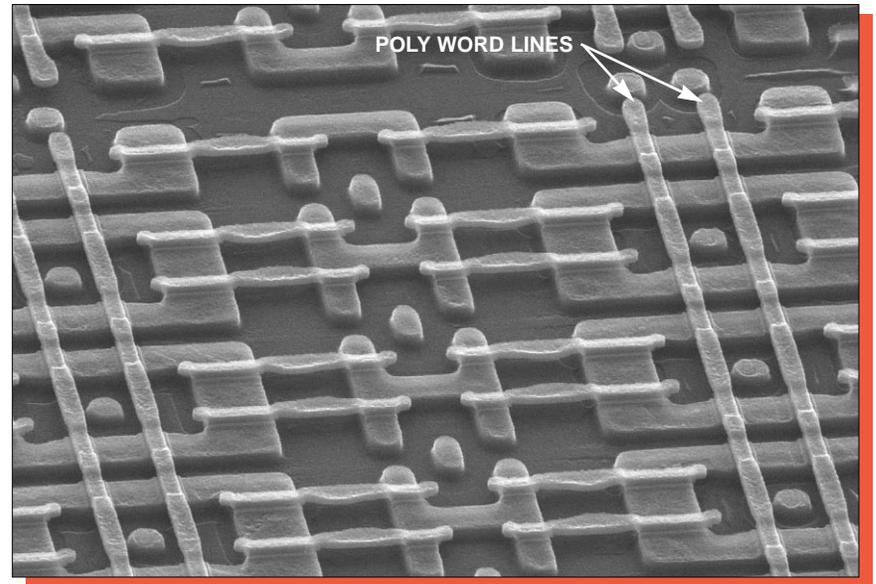
metal 3



metal 1

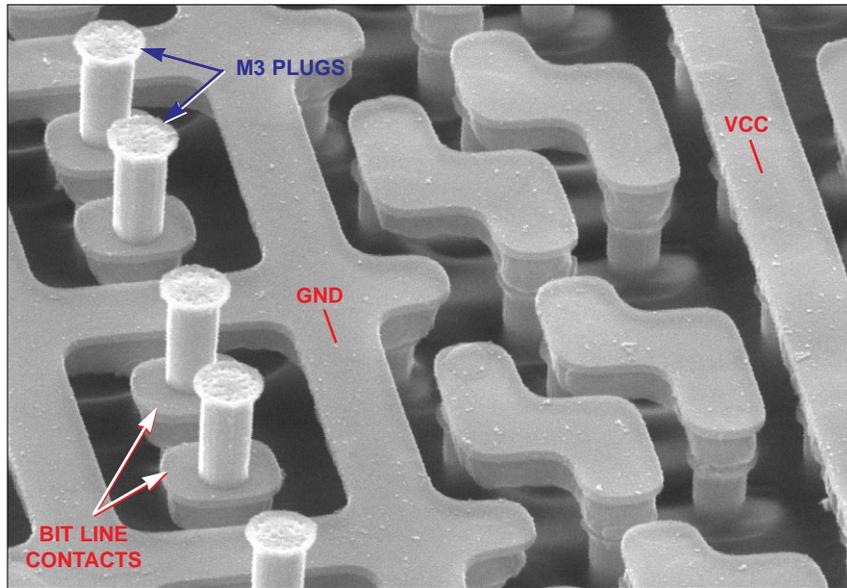


metal 2

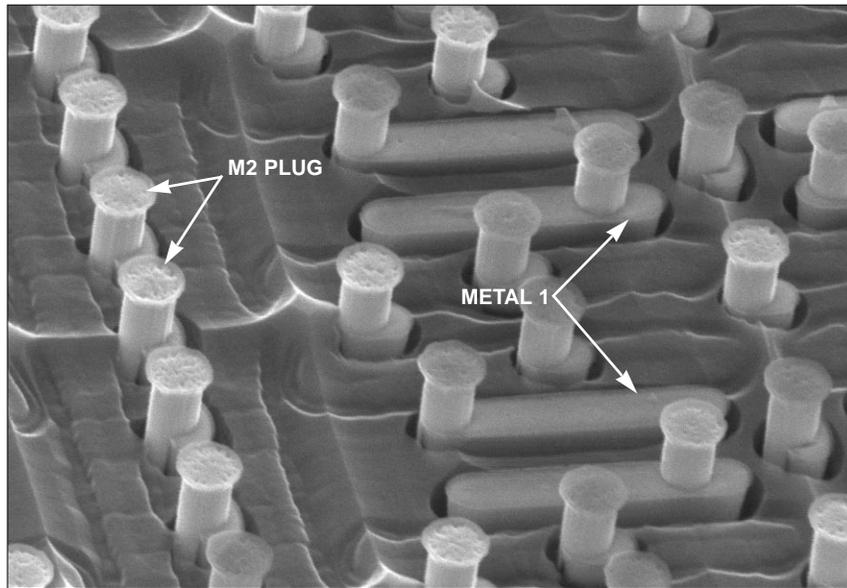


delayed

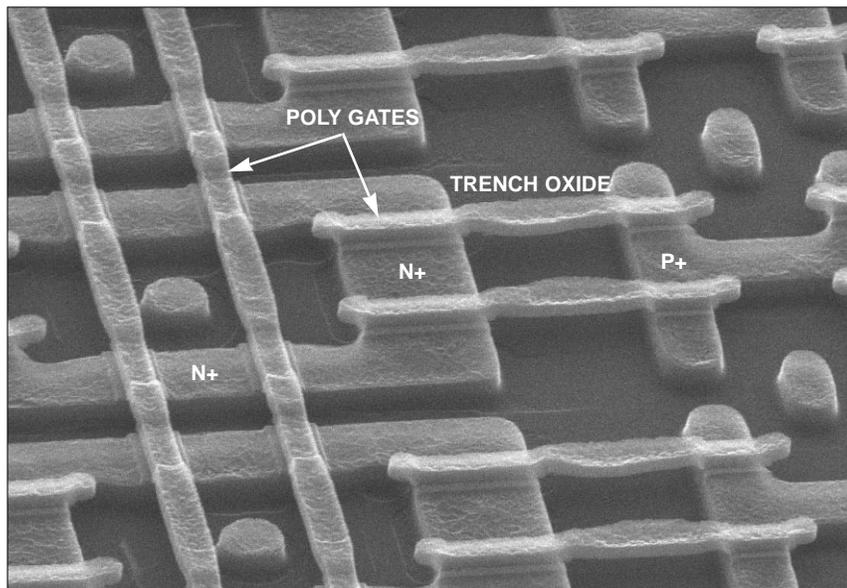
Figure 48. Perspective SEM views of the Cache SRAM array. Mag. 6500x, 55°.



metal 2

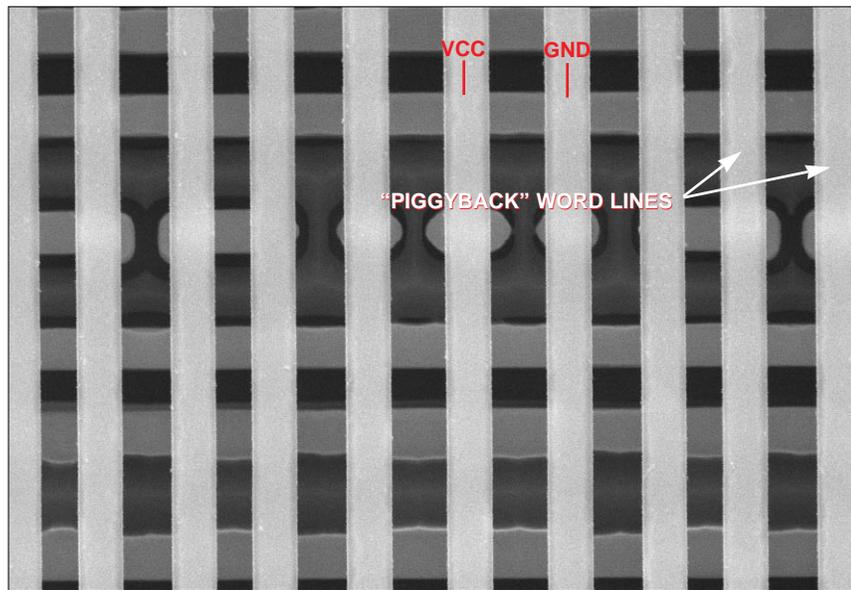


metal 1

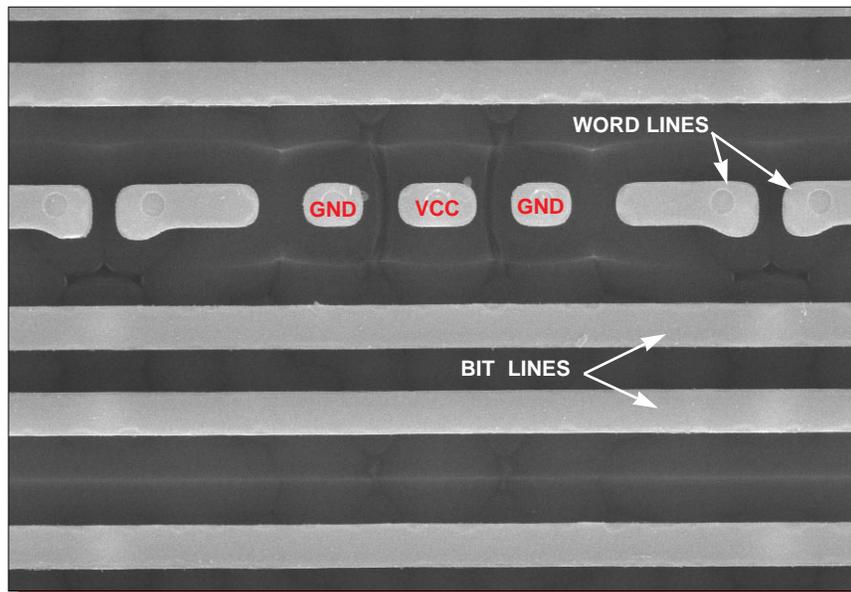


delayed

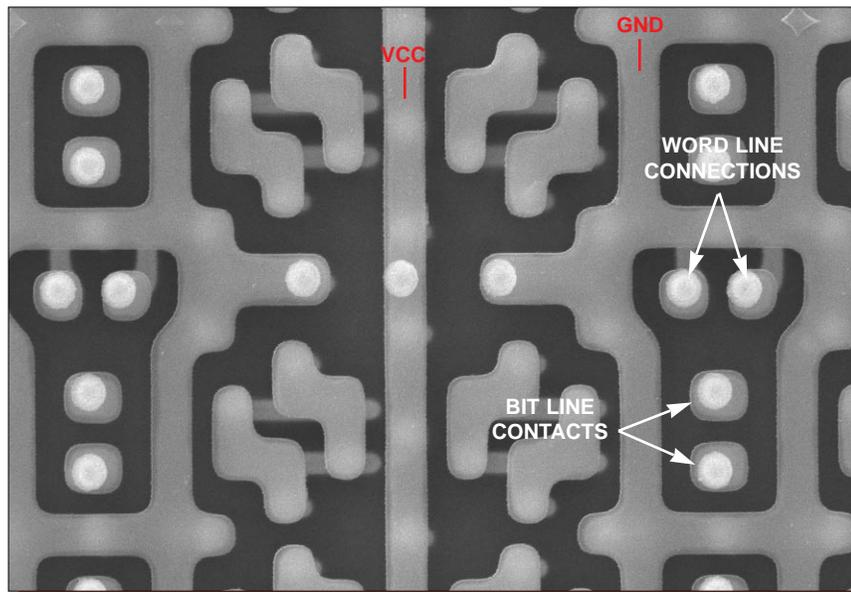
Figure 49. Detail SEM views of Cache SRAM cells. Mag. 12,000x, 55°.



metal 4

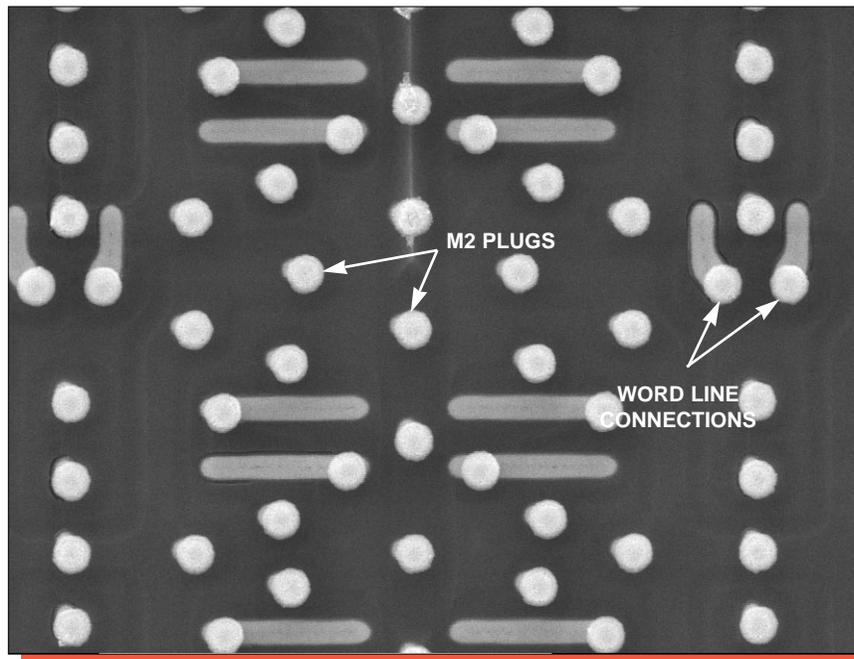


metal 3

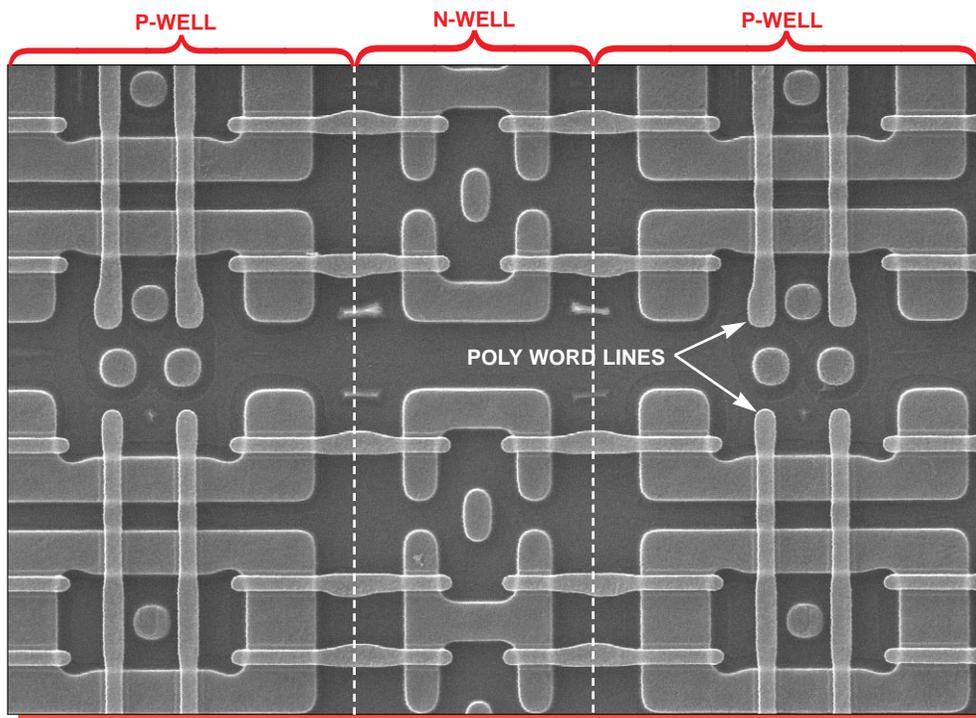


metal 2

Figure 50. Topological SEM views of the Cache SRAM array. Mag. 6200x, 0°.

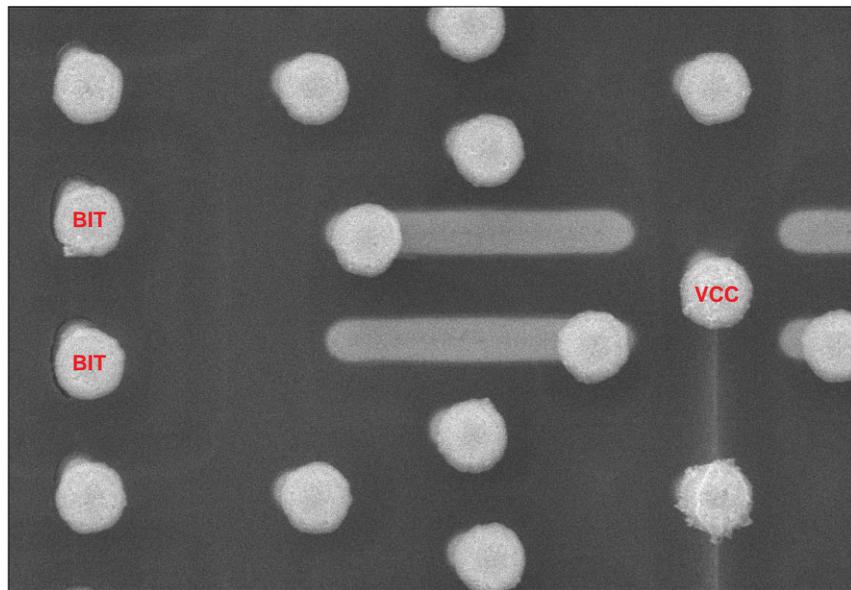


metal 1

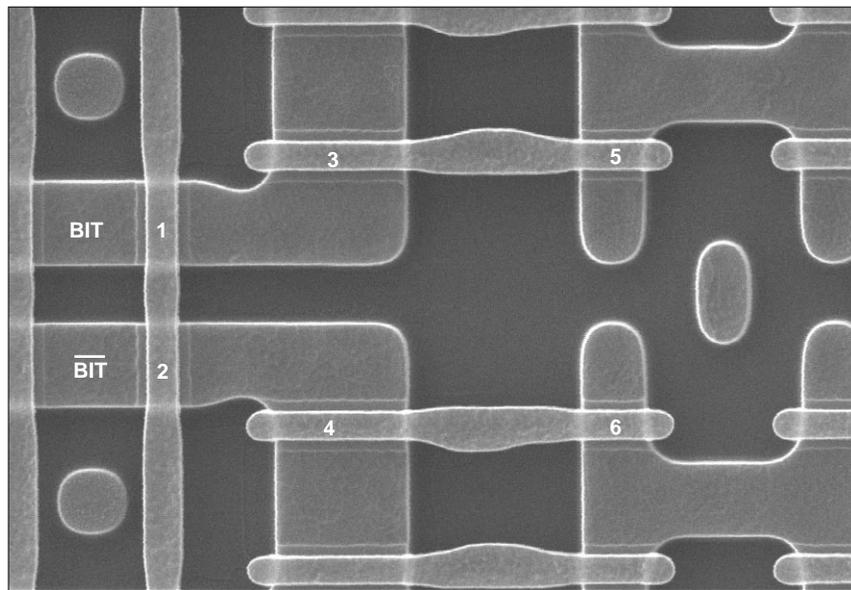


delayed

Figure 51. Topological SEM views of the Cache SRAM array. Mag. 6200x, 0°.



metal 1



delayed

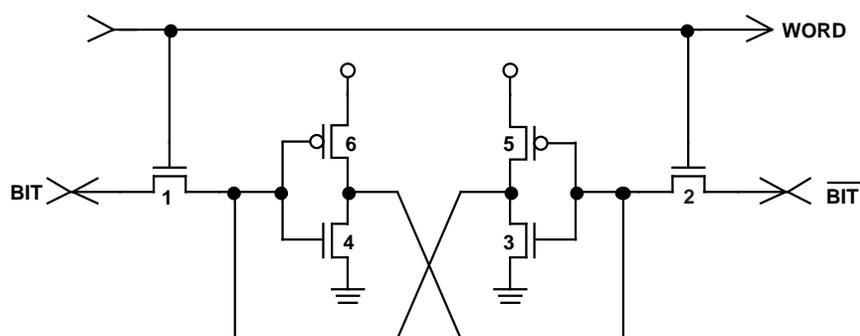


Figure 52. Topological SEM details and schematic of a Cache SRAM cell.
Mag. 12,000x, 0°.

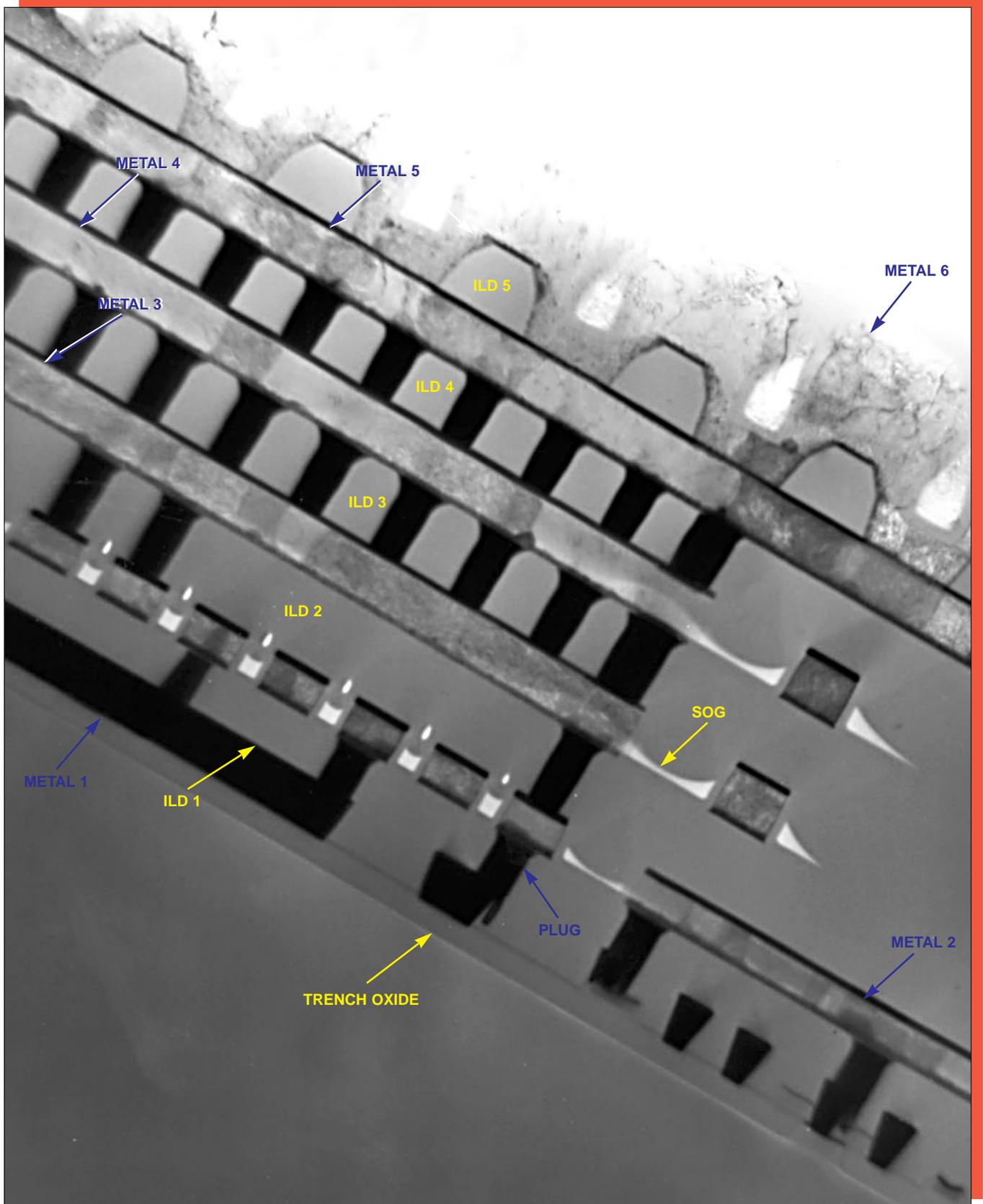
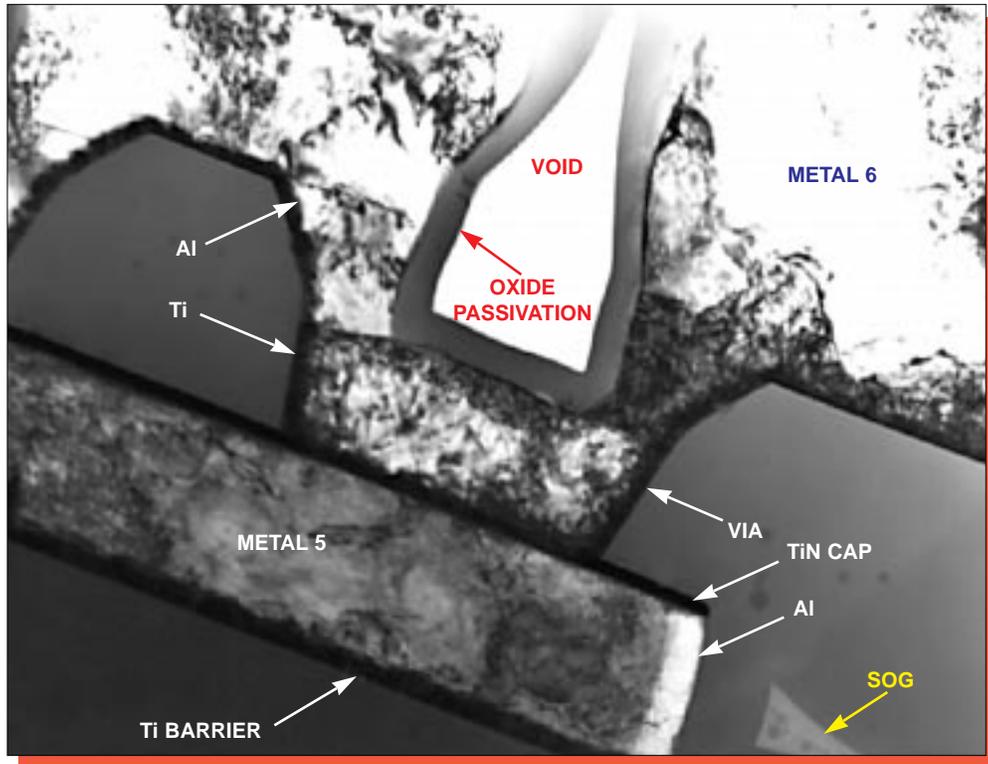
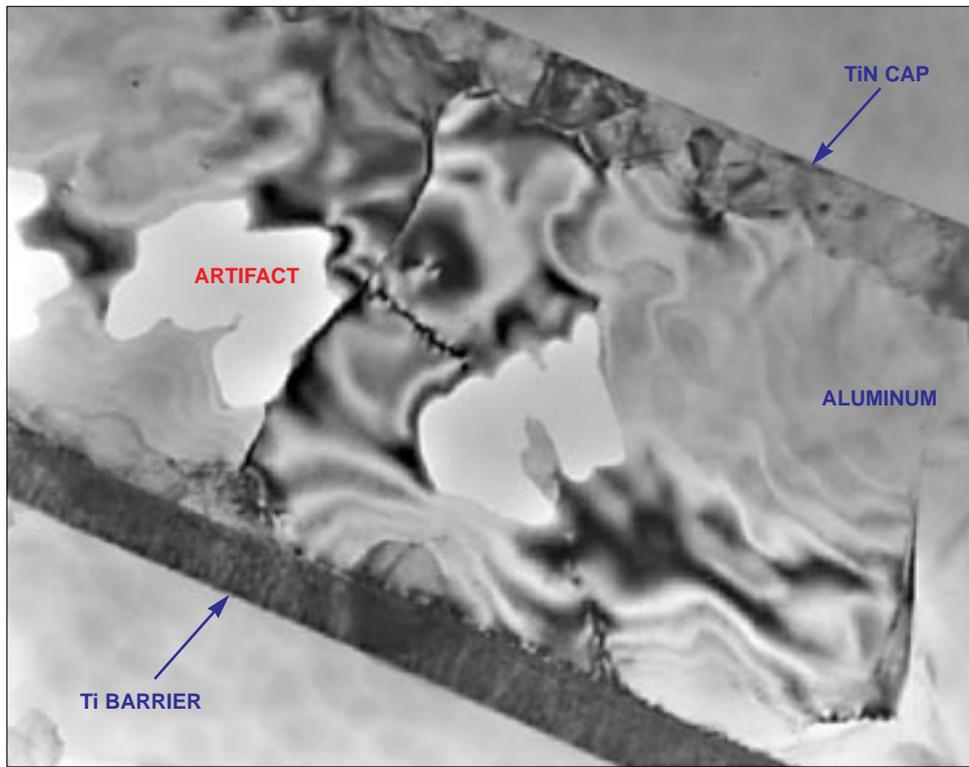


Figure T1. TEM overview of general structure. Mag. 12,400x.

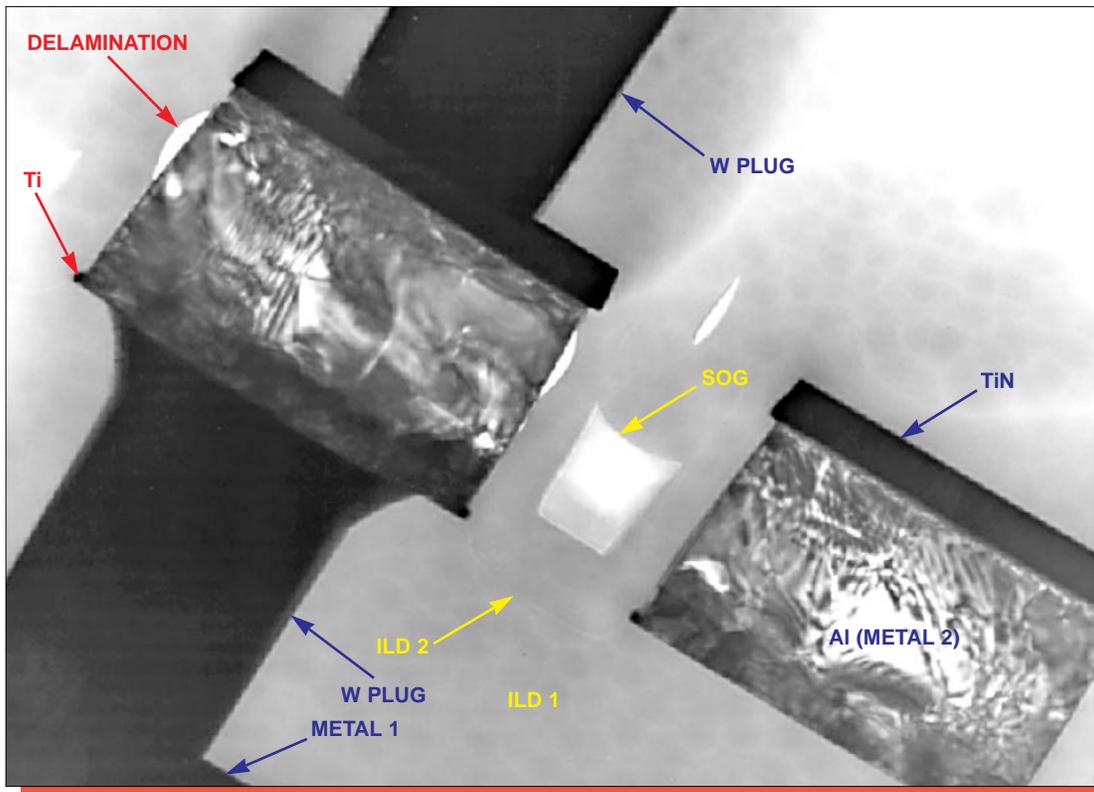


Mag. 29,750x

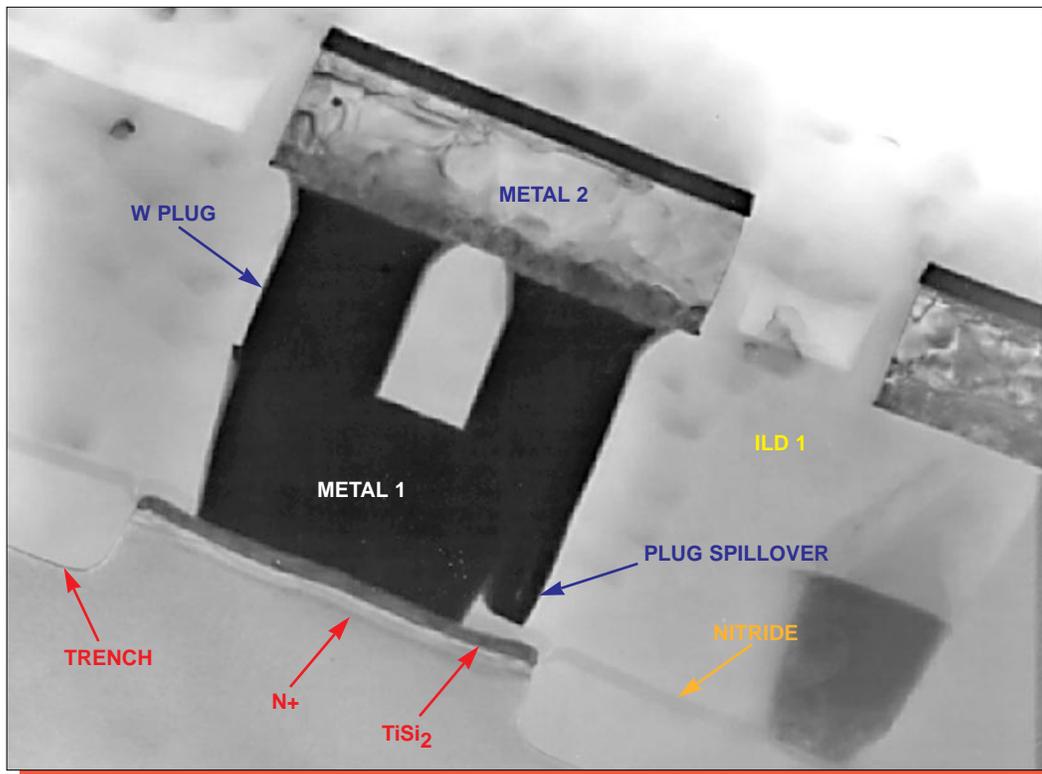


Mag. 93,500x

Figure T2. TEM section view of metal 6 with detail of cap and barrier.

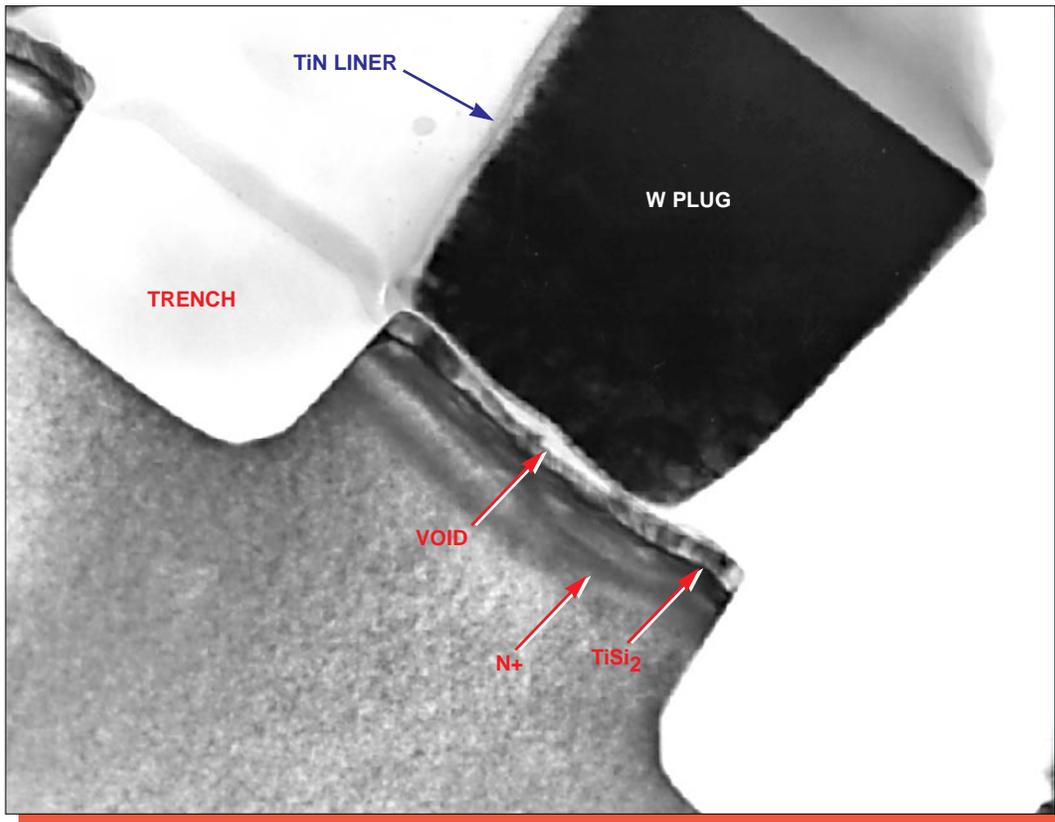


Mag. 57,600x

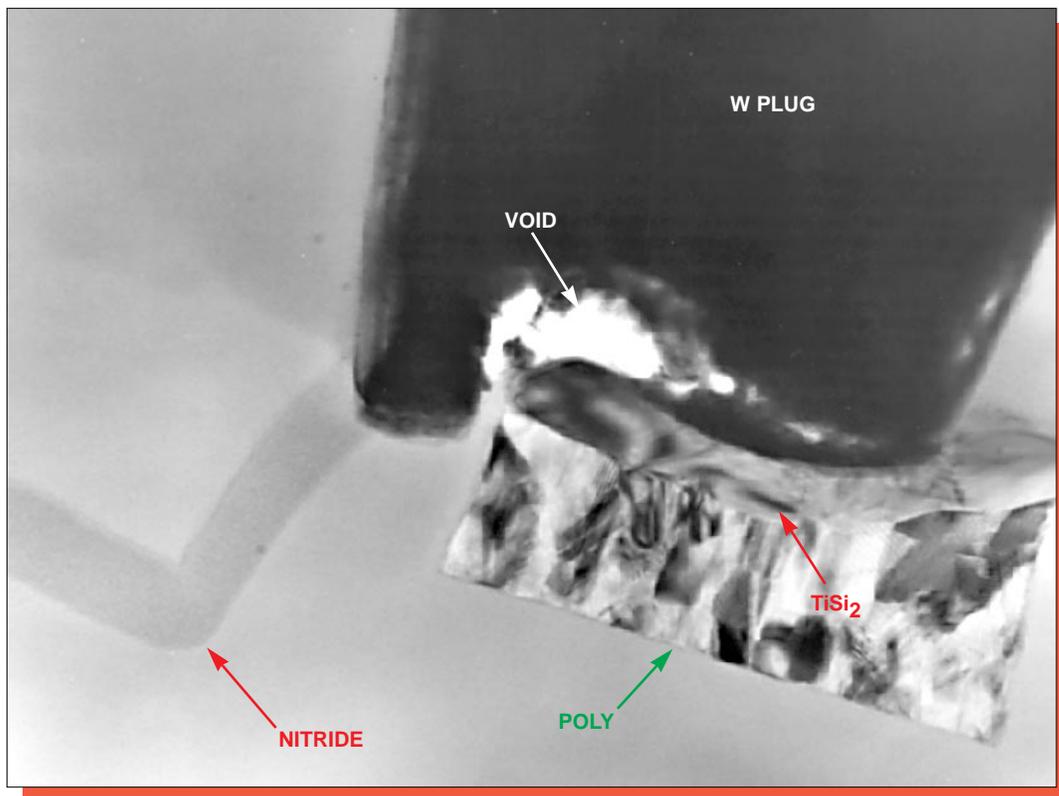


Mag. 31,500x

Figure T3. TEM section views of delamination at aluminum and contact structures.



Mag. 76,500x



Mag. 180,000x

Figure T4. TEM section views of contact voids.

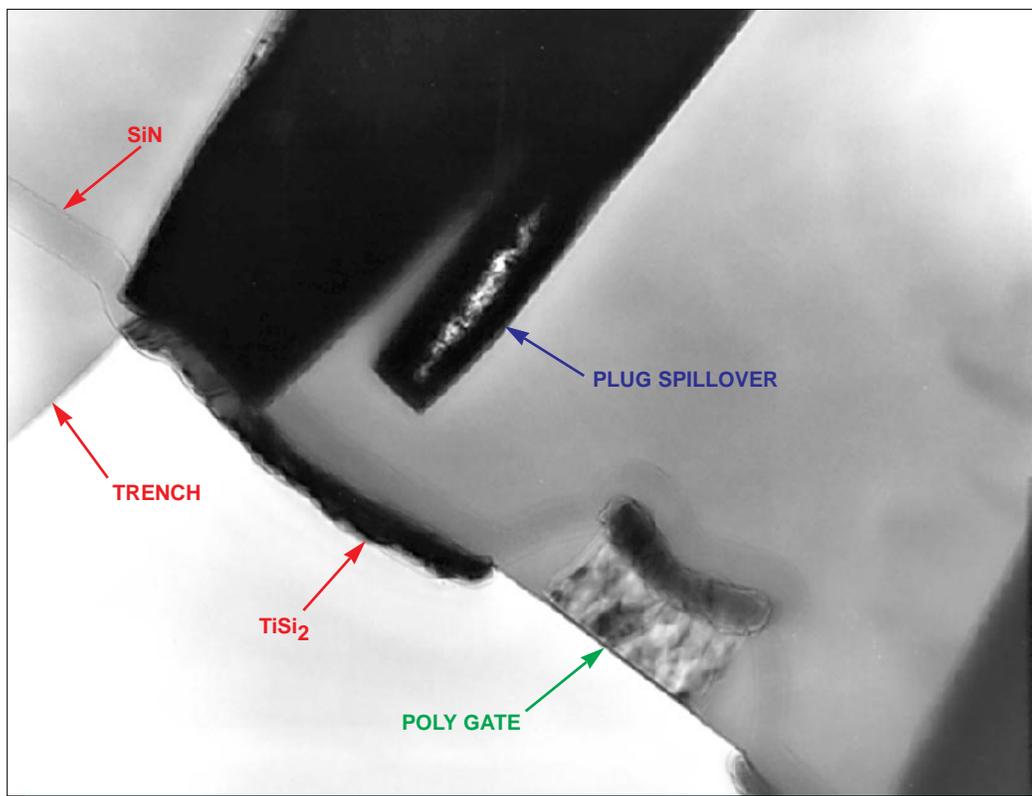
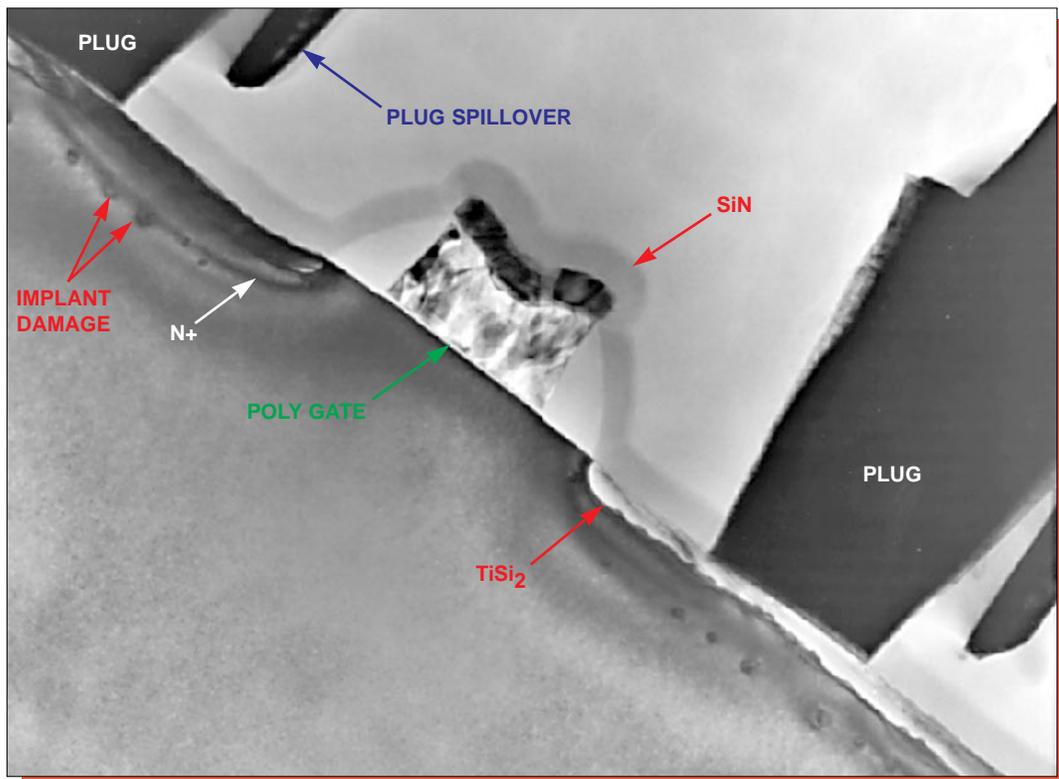
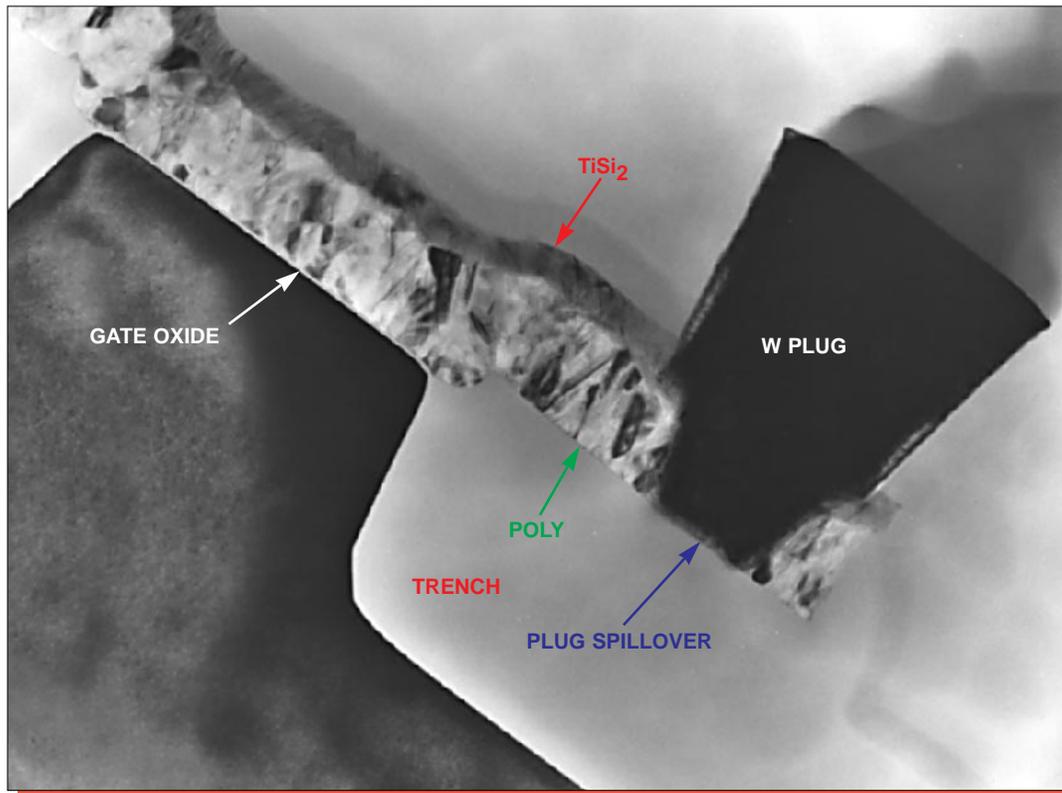
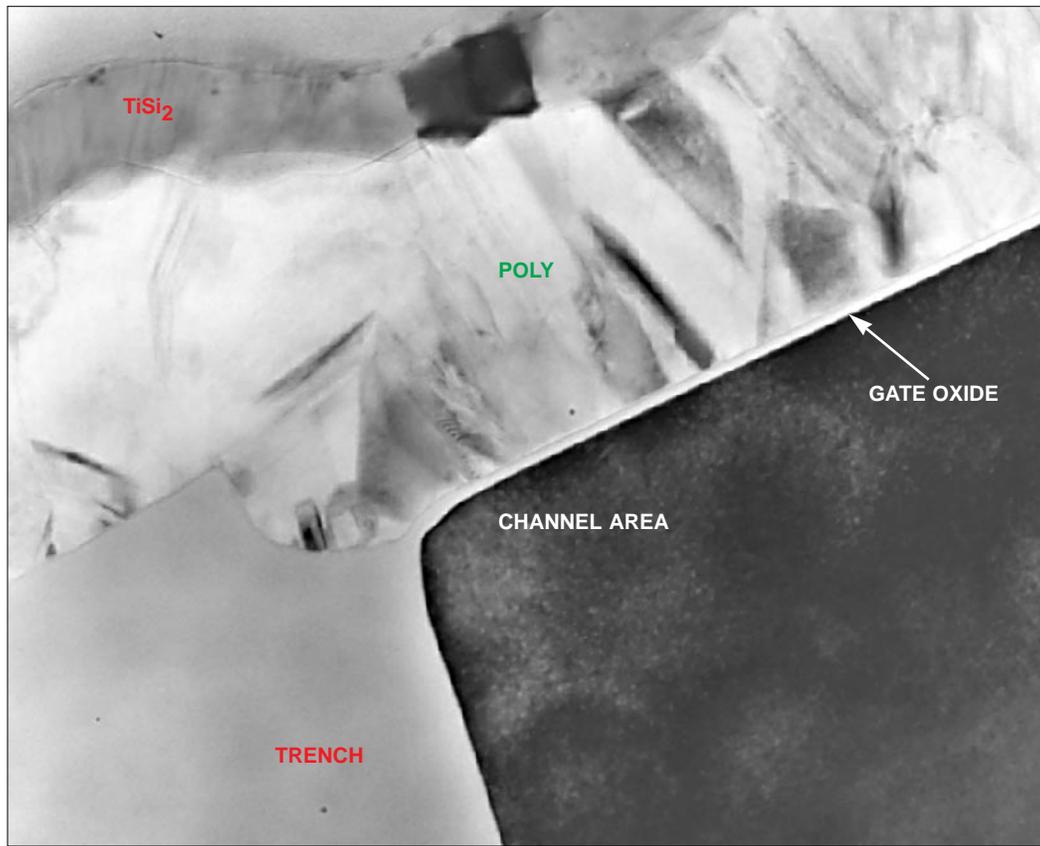


Figure T5. TEM section views of gate to contact relationship. Mag. 76,500x.

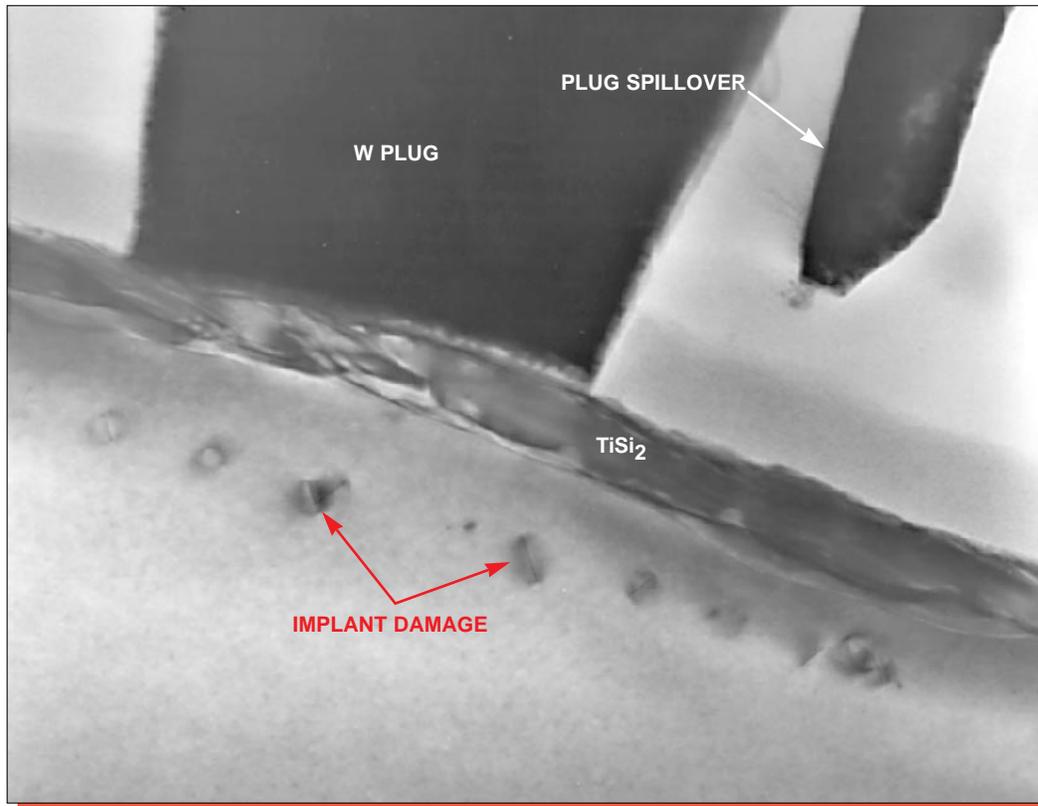


Mag. 76,500x

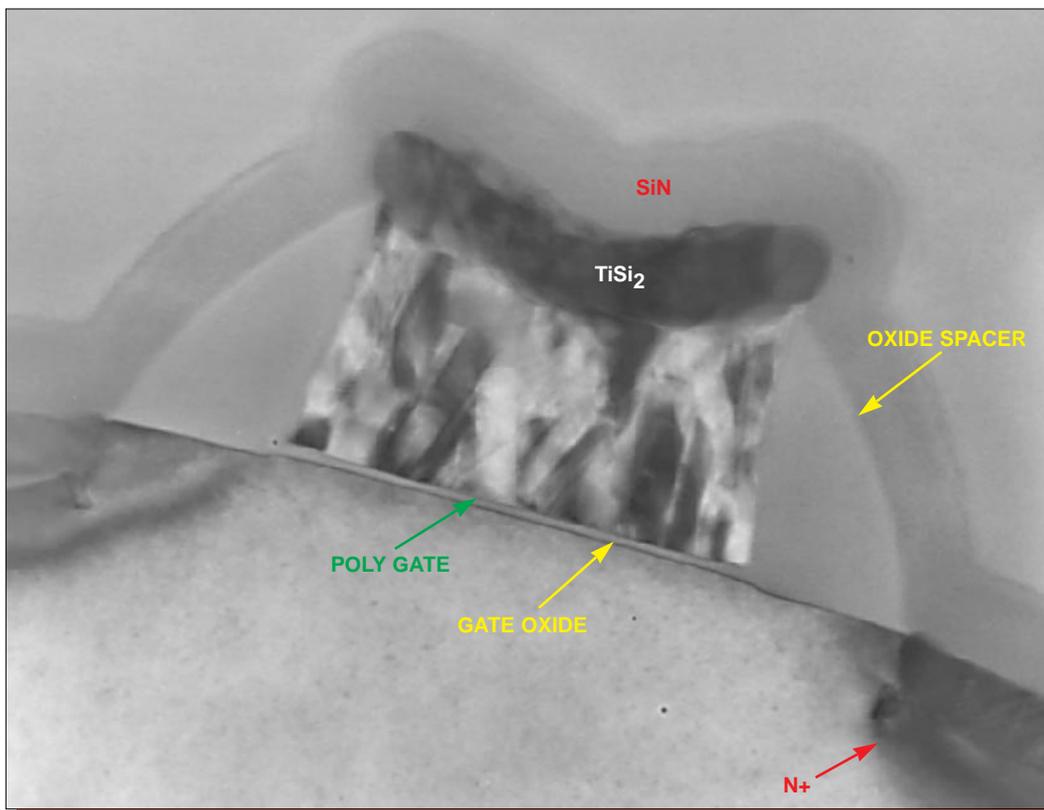


Mag. 243,000x

Figure T6. TEM section views of gate parallel to gate length.



Mag. 186,000x



Mag. 196,000x

Figure T7. TEM section details of diffusion contact and gate.