

Construction Analysis

Intel Pentium Processor W/MMX

Report Number: SCA 9706-540



INTEGRATED CIRCUIT ENGINEERING

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INDEX TO TEXT

<u>TITLE</u>	<u>PAGE</u>
INTRODUCTION	1
MAJOR FINDINGS	1
TECHNOLOGY DESCRIPTION	
Assembly	2
Die Process	2 - 3
ANALYSIS RESULTS I	
Assembly	4
ANALYSIS RESULTS II	
Die Process and Design	5 - 7
ANALYSIS PROCEDURE	8
TABLES	
Overall Evaluation	9
Package Markings	10
Die Material Analysis	10
Horizontal Dimensions	11
Vertical Dimensions	12

INTRODUCTION

This report describes a construction analysis of the Intel 200MHz Pentium Processor with MMX technology. One sample was used for the analysis. The device was received in a 296-pin, SPGA (Super PGA) with a metal heatsink.

MAJOR FINDINGS

Questionable Items:¹

- Quality of die manufacturing was good and we found no areas of quality or reliability concerns.

Special Features:

- Four metal, N-epi, CMOS process (not BiCMOS).
- All metal layers employed tungsten via/contact plugs. Metals 2 - 4 employed tungsten plugs with "stubs" underneath at vias, for improved contact. Stacked vias were employed at all levels.
- Chemical-mechanical planarization (CMP).
- Oxide-filled shallow-trench isolation.
- Titanium salicided diffusion structures.
- Aggressive feature sizes (0.3 micron gates).

Noteworthy Items:

- Layout of the Pentium with MMX differs from the previous Pentium designs (120, 133, and 166 MHz). Physical construction of the processors was basically the same (i.e. - Four metals, tungsten plugs at all levels, CMP planarization, 0.3 micron gate lengths). The most significant process difference appears to be no bipolar structures were used on the MMX device, but were present on the previously mentioned Pentium devices.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- The device was packaged in a 296-pin SPGA. A metal heatsink was employed on the top of the package. The die was mounted cavity down.
- Eight decoupling capacitors were present on top of the package.
- The PGA was constructed of fiberglass and was coated with a black epoxy-like material. The cavity was filled with black plastic material. Markings were etched into the plastic.
- Triple tier package lands plated with gold.
- Ultrasonic wedge wirebonding using gold wire.
- Sawn dicing (full depth). The edges of the die had been beveled at the surface.
- Silver-epoxy die attach. The backside of the die was plated with gold.

Die Process:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process apparently employing twin wells in a N-epi on an N substrate.
- Die coat: A thin patterned polyimide die coat was present over the entire die.
- Final passivation: A single layer of nitride.
- Metallization: Four levels of metal defined by dry-etch techniques. All consisted of aluminum with titanium-nitride caps. Metal 4 also employed a substantial titanium adhesion layer. There appeared to be evidence of very thin titanium adhesion layers under metals 1-3. Tungsten plugs were employed for vias and contacts under all metals. Metals 2 through 4 employed tungsten plugs with "stubs" underneath, for improved contact. The "stubs" penetrated into the metal

TECHNOLOGY DESCRIPTION (continued)

below the tungsten plugs. This is a unique processing feature. All plugs were lined with titanium-nitride. Stacked vias were employed at all levels.

- Interlevel dielectrics 1, 2, and 3: The interlevel dielectric between all metals consisted of the same structure. A very thin glass was deposited first, followed by two thick layers of glass. The third layer of glass was planarized by CMP which left the surface very planar.
- Pre-metal glass: A thick layer of glass followed by a thin layer of glass. This dielectric was also planarized by CMP.
- Polysilicon: A single layer of dry-etched polycide (poly and titanium-silicide). This layer was used to form all gates on the die. Nitride sidewall spacers were used to provide the LDD spacing.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Titanium was sintered into the diffusions (salicide process).
- Isolation: Local oxide isolation consisted of oxide-filled shallow-trench isolation. It was very planar with the diffused silicon surfaces.
- Wells: Twin-wells in an N-epi on an N substrate.
- SRAM: Level 1 on-chip data and code cache memory cell arrays (16KB each) were employed. The memory cells used a 6T CMOS SRAM cell design. Metal 3 formed the bit lines (via metal 1 and 2). Metal 2 distributed Vcc and formed “piggyback” word lines. Metal 1 distributed GND and was used as cell interconnect. Polycide formed the select and storage gates. Cell pitch was 4.6 x 4.2 microns (19 μm^2).
- No redundancy fuses were found.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 2

Questionable Items:¹ None.

Special Features:

- SPGA package

General Items:

- The device was packaged in a 296-pin SPGA. A metal heatsink was employed on top of the package. The die was mounted cavity down. The PGA was constructed of fiberglass and was coated with a black epoxy-like material. The cavity was filled-in with black plastic material.
- Overall package quality: Good. No defects were found on the external or internal portions of the packages. External pins were straight and placement was good. No voids were noted in the plastic cavity fill.
- Wirebonding: Ultrasonic wedge bond method using gold wire. A three tier package land structure was used. Wire spacing and placement was good. Bond pitch was very close (95 microns); however, no problems were noted.
- Die attach: Silver-epoxy die attach of good quality. No voids were noted in the die attach. The backside of the die was plated with gold.
- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die edges. The edges of the die had been beveled (see Figure 6). This is highly unusual and we do not know why it is done (or how).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 3 - 44a

Questionable Items:¹ None.

- No areas of concern were found in the area of die fabrication.

Special Features:

- Four metal, twin-well, N-epi, CMOS process.
- All metal layers employed tungsten via/contact plugs. Metals 2 - 4 employed tungsten plugs with "stubs" underneath at vias, for improved contact. Stacked vias were employed at all levels.
- Chemical-mechanical planarization (CMP).
- Oxide filled shallow-trench isolation.
- Titanium salicided diffusion structures.
- Aggressive feature sizes (0.3 micron gates).

General Items:

- Fabrication process: Oxide-filled shallow-trench isolation, CMOS process apparently employing twin-wells in an N-epi on an N substrate. No problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Design features: Slotted bus lines were employed to relieve stress. Anti-dishing patterns were employed for planarization purposes. Numerous unconnected metal 4 vias which appear to be used for probing purposes were present.

ANALYSIS RESULTS II (continued)

- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Die coat: A patterned polyimide die coat was present over the entire die surface.
- Final passivation: A single layer of nitride. Coverage was good. Edge seal was also good as the passivation extended into the scribe lane to seal the metallization.
- Metallization: Four levels of metallization. All consisted of aluminum with titanium-nitride caps. Metal 4 employed a fairly thick titanium adhesion layer. The other levels probably used a titanium layer too thin to detect. Tungsten plugs were employed with all metals. Holes were noted in the center of some tungsten plugs at metals 2-4. All plugs were lined with titanium-nitride underneath and the presumed titanium layer over top.
- Metal patterning: All metal layers were defined by a dry etch of good quality. Metal lines were widened (where needed), where vias made contact to them from above.
- Metal defects: None. No voiding, notching or cracking of the metal layers was found. No silicon nodules were found following removal of the metal layers.
- Metal step coverage: No metal (aluminum) thinning was present at the connections to the tungsten via plugs. The absence of thinning is due to the good control of plug height and the planarization technique employed.
- Vias and contacts: All via and contact cuts were defined by a dry and wet-etch of good quality. Again, alignment of the metals and plugs was very good. Metals 2 - 4 employed tungsten "stubs" at the bottom of the tungsten plugs. These unique features consisted of stubs of tungsten plug metallization that penetrated into the underlying aluminum. It is assumed that this represents a method to obtain good contact. Vias and contacts were placed directly over one another (stacked vias). No problems were noted.
- Interlevel dielectrics 1, 2, and 3: The interlevel dielectric between all metals consisted of the same oxide structure. A very thin glass was deposited first,

ANALYSIS RESULTS II (continued)

followed by two thick layers of glass. The third layer of glass was subjected to CMP which left the surface very planar. No problems were found with any of these layers.

- Pre-metal glass (under metal 1): A thick layer of silicon-dioxide followed by a thin layer of glass. This layer also appeared to have been planarized by chemical-mechanical planarization. No problems were found.
- Polysilicon: A single level of polycide (poly and titanium-silicide) was used. It formed all gates and word lines in the array. Definition was by a dry etch of good quality. Nitride sidewall spacers were used throughout and left in place. No problems were found.
- Isolation: The device used oxide-filled shallow-trench isolation which was quite planar with the silicon surface. No problems were present.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Titanium was sintered into the diffusions (salicide process) to reduce series resistance. An LDD process was used employing nitride sidewall spacers. No problems were found.
- Wells: Apparently twin-wells were used in a N-epi on a N substrate. Definition was normal.
- Buried contacts: Not used.
- SRAM: As mentioned, Level 1 on-chip data and code Cache memory cell arrays (16KB each) were employed on the device. The SRAM cell array used a 6T CMOS SRAM cell design. Metal 3 formed the bit lines (via metals 1 and 2). Metal 2 distributed Vcc and formed “piggyback” word lines. Metal 1 distributed GND and was used as cell interconnect. Polycide formed the word lines/select and storage gates. Cell pitch was 4.2 x 4.6 microns ($19\mu\text{m}^2$).
- No redundancy fuses were noted.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Die optical inspection

Delayer to metal 4 and inspect

Aluminum removal (metal 4) and inspect tungsten plugs

Delayer to metal 3 and inspect

Aluminum removal (metal 3) and inspect tungsten plugs

Delayer to metal 2 and inspect

Aluminum removal (metal 2) and inspect tungsten plugs

Delayer to metal 1 and inspect

Aluminum removal (metal 1) and inspect tungsten plugs

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by glass etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G (tight wirebond pitch)
Wirebond quality	N
Dicing quality	N
Die attach quality	G
Die attach method	Silver-epoxy
Dicing method:	Sawn
Wirebond method	Ultrasonic wedge bonds using gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N (incomplete fill of plugs)
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	G
Metal registration	G
Contact coverage	G
Via/contact registration	N
Etch control (depth)	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (partial)

TOP (heatsink)

Intel
Pentium
w/MMX™ Tech

BOTTOM (plastic)

Intel®
Pentium®
w/MMX™ Tech
Q019 ES/2.8V
m © '92 '95

DIE MATERIALS

Overlay passivation:	Single layer of nitride.
Metallization 4:	Aluminum with a titanium-nitride cap and a titanium adhesion layer.
Interlevel dielectrics 1, 2, and 3:	A thin layer of glass followed by two thick layers of glass.
Metallization 1 - 3:	Aluminum with a titanium-nitride cap and probably a very thin titanium adhesion layer.
Via/contact plugs (M1 - M4):	Tungsten (lined with titanium-nitride).
Intermediate glass:	Thick layer of silicon-dioxide followed by a thin glass. (No reflow glass).
Polycide:	Titanium-silicide on polysilicon.
Salicide on diffusions:	Titanium-silicide.

VERTICAL DIMENSIONS

Die thickness: (0.5 mm) 20 mils

Layers

Passivation:	0.7 micron
Metal 4 - cap:	0.03 micron (approximate)
- aluminum:	1.6 micron
- barrier:	0.1 micron
- plugs:	0.9 micron (not including "stub")
Interlevel dielectric 3 - glass 3:	0.5 - 1.4 micron
- glass 2:	0.4 micron
- glass 1:	0.07 micron (approximate)
Metal 3 - cap:	0.05 micron (approximate)
- aluminum:	0.75 micron
- plugs:	0.9 micron (not including "stub")
Interlevel dielectric 2 - glass 3:	0.55 - 1.5 micron
- glass 2:	0.3 micron
- glass 1:	0.07 micron (approximate)
Metal 2 - cap:	0.05 micron (approximate)
- aluminum:	0.8 micron
- plugs:	0.9 micron (not including "stub")
Interlevel dielectric 1 - glass 3:	0.35 - 1.15 micron
- glass 2:	0.35 micron
- glass 1:	0.07 micron (approximate)
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.55 micron
- plugs:	0.6 - 0.9 micron
Pre-metal glass - glass 2:	0.08 micron (approximate)
- glass 1:	0.45 - 0.8 micron
Polycide - silicide:	0.07 micron (approximate)
- poly:	0.2 micron
Trench oxide:	0.4 micron

N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.25 micron
N-epi:	1.6 microns

INDEX TO FIGURES

ASSEMBLY	Figures 1 - 2
DIE LAYOUT AND IDENTIFICATION	Figures 3 - 4
PHYSICAL DIE STRUCTURES	Figures 5 - 44a
COLOR DRAWING OF DIE STRUCTURE	Figure 40
MEMORY CELL	Figures 41 - 44a

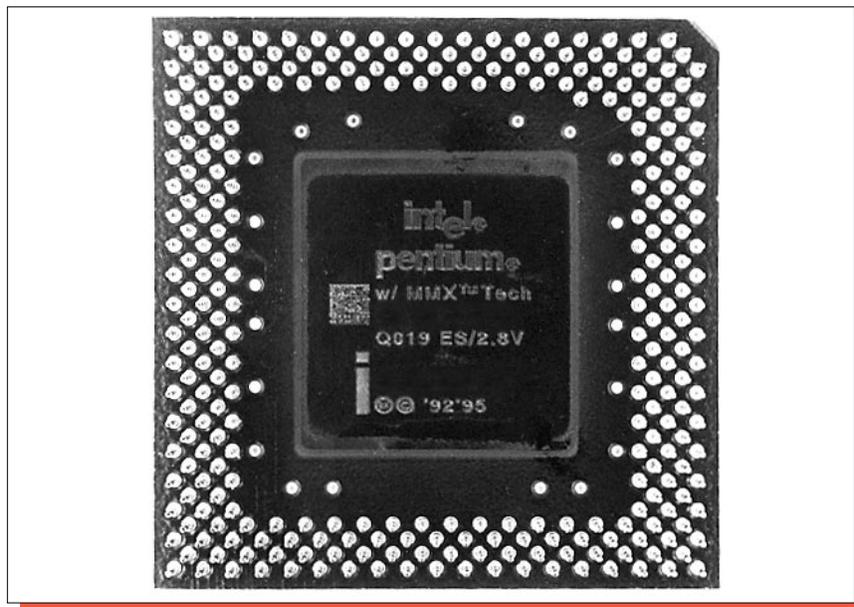
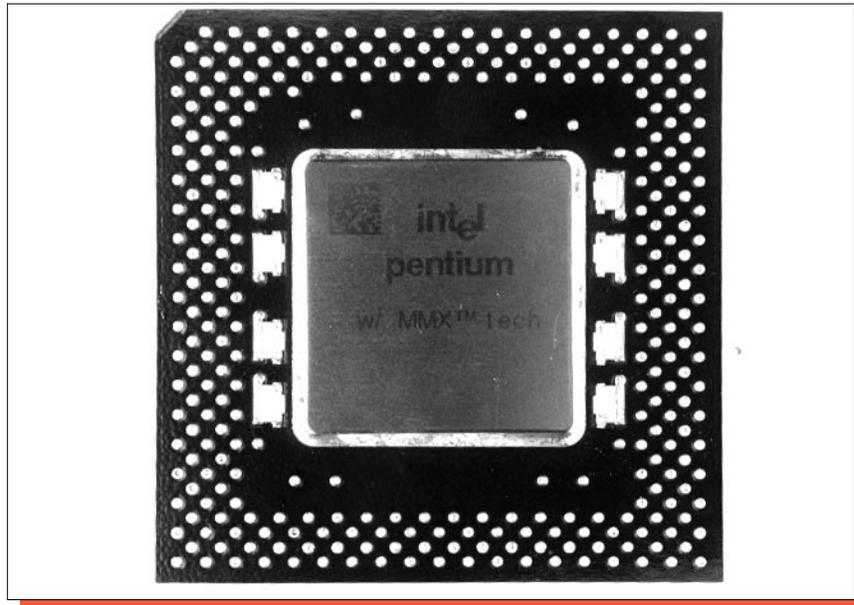


Figure 1. Package photographs of the Intel Pentium with MMX. Mag. 1.5x.

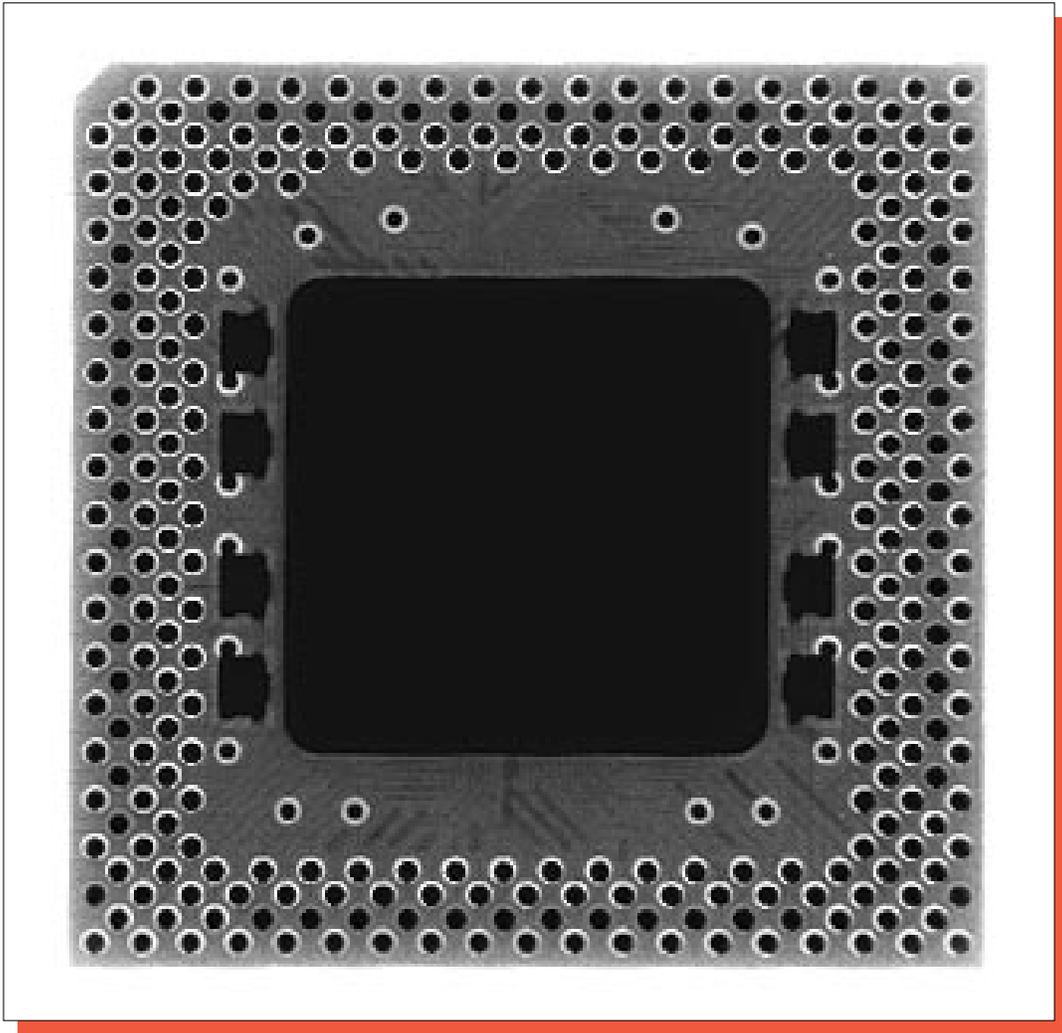


Figure 2. Topological x-ray view of the package. Mag. 2.5x.



Figure 3. Whole die photograph of the Intel Pentium with MMX. Mag. 16x.

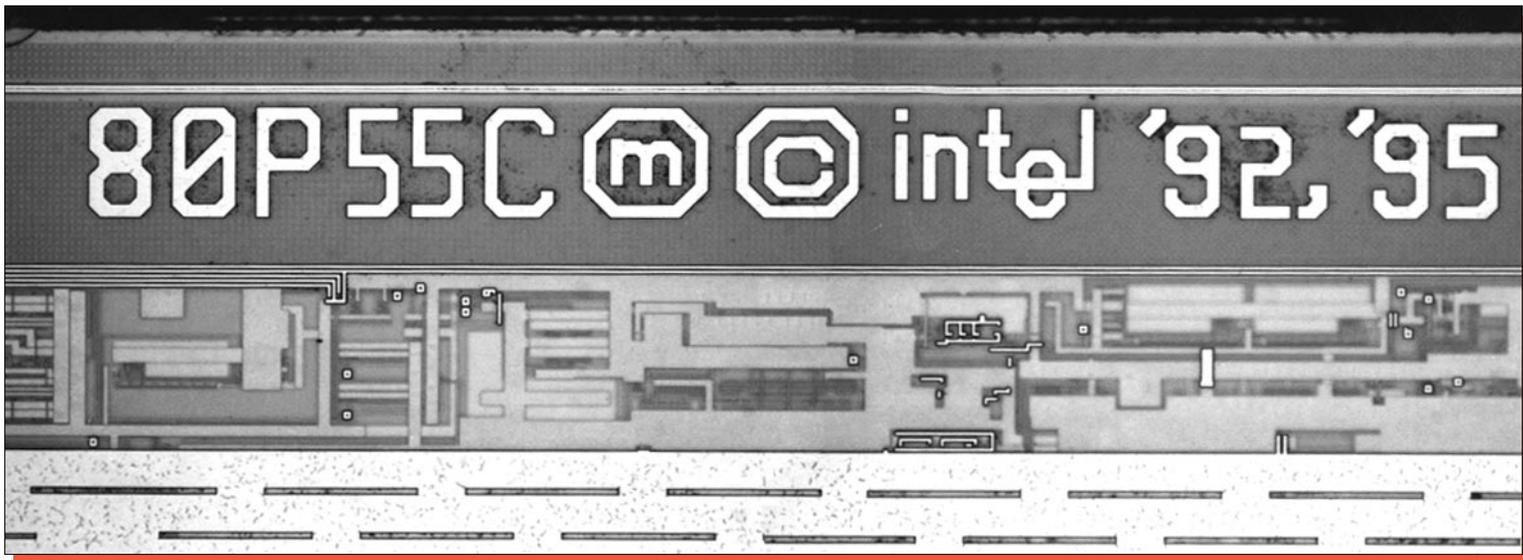


Figure 4. Die identification markings. Mag. 200x.

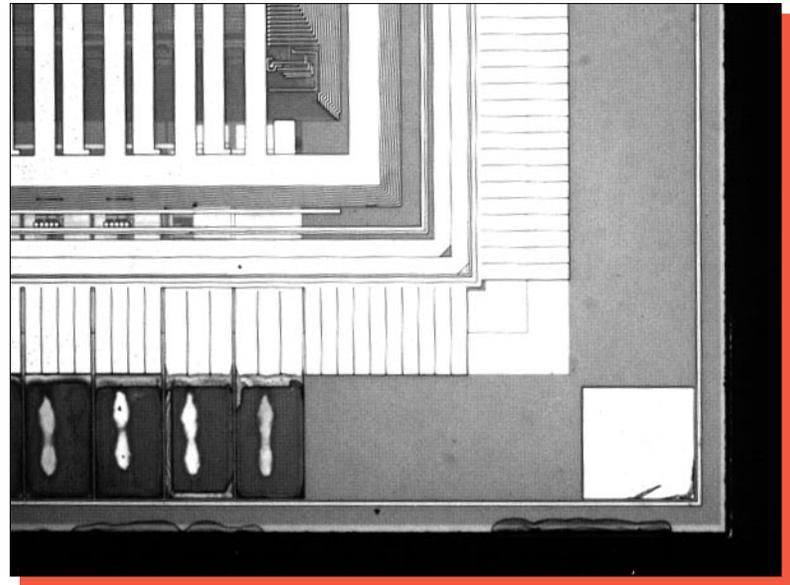
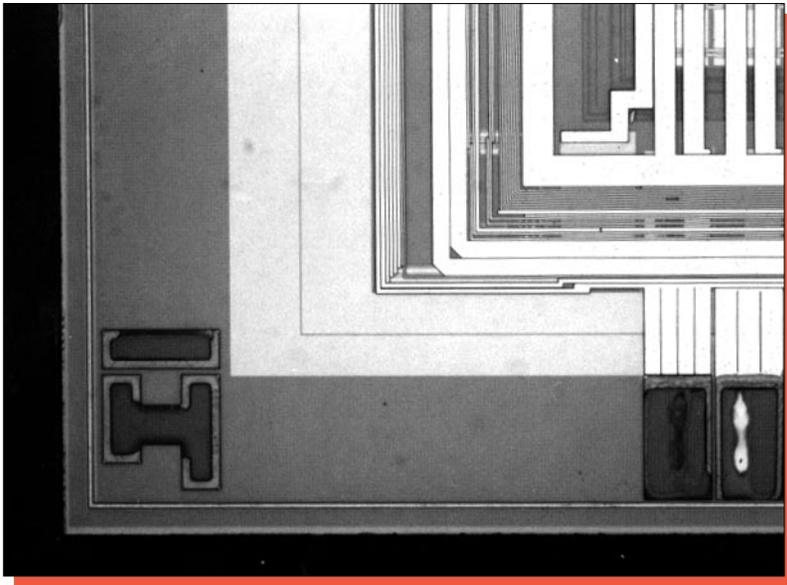
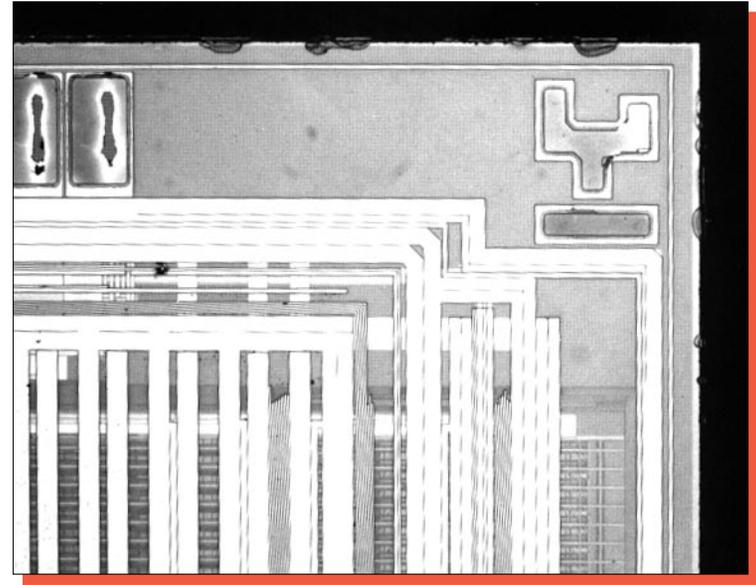
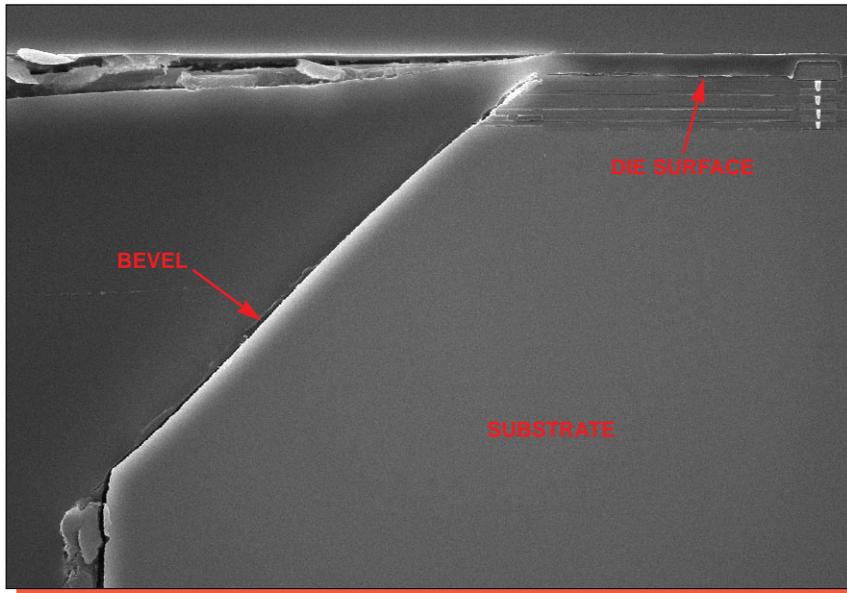
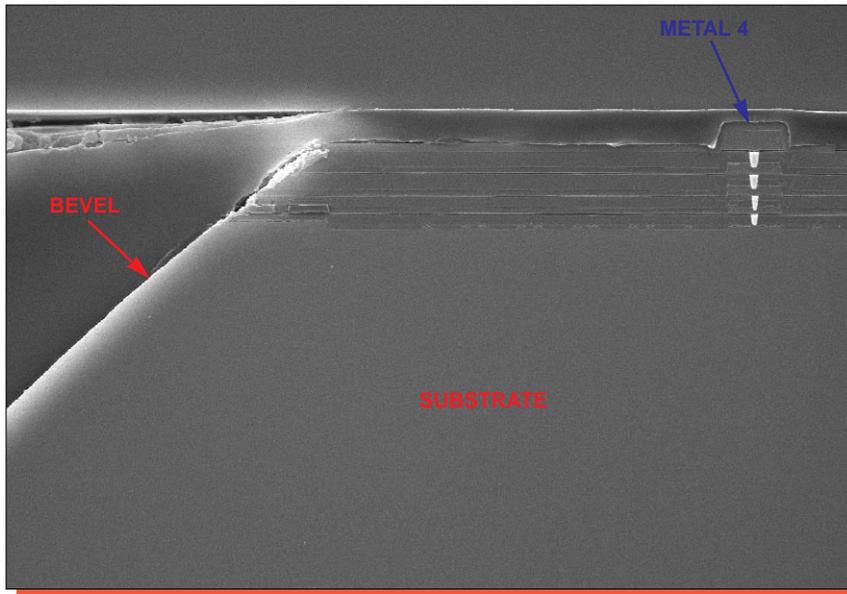


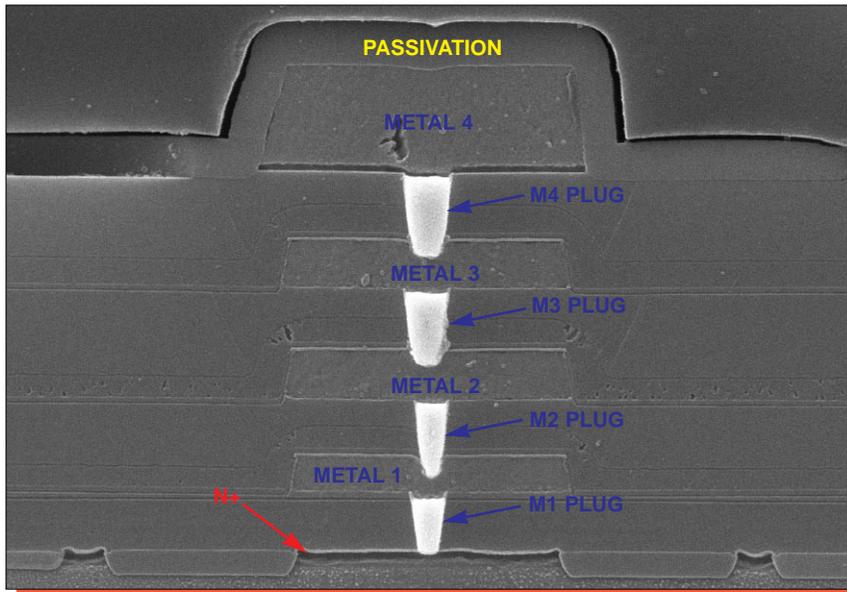
Figure 5. Optical views of the die corners. Mag. 100x



Mag. 1000x

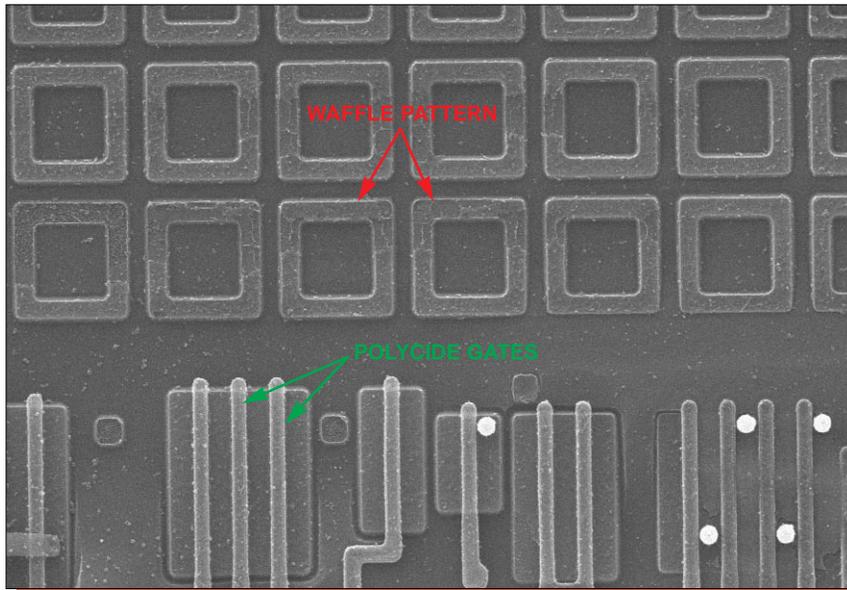


Mag. 1500x

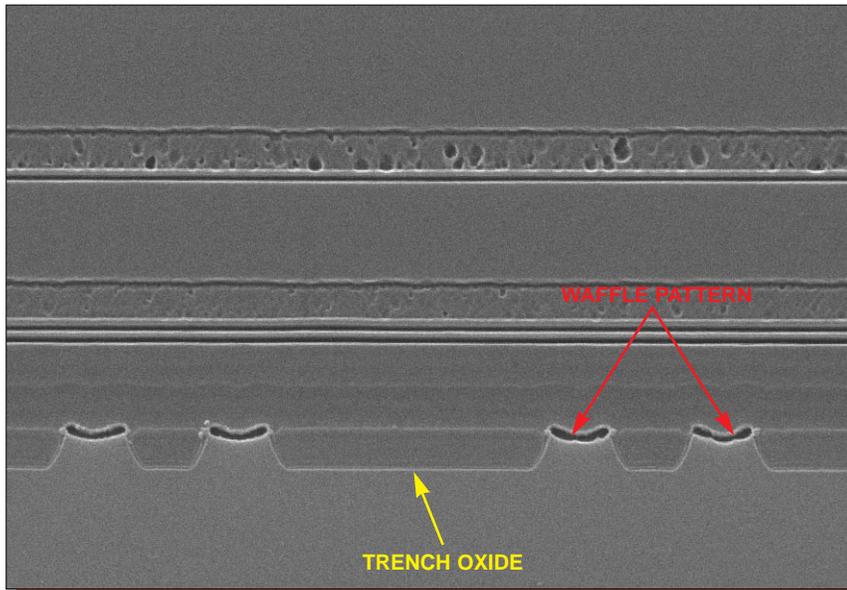


Mag. 8000x

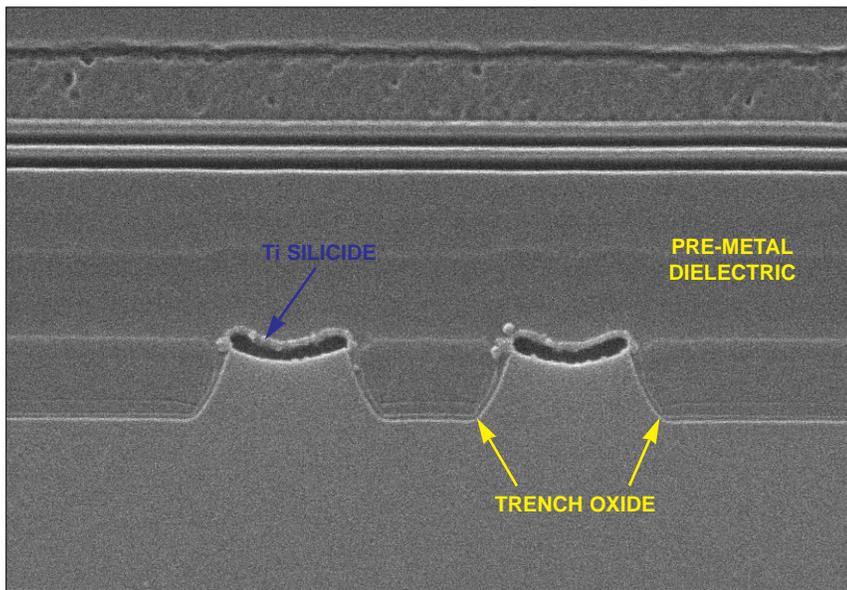
Figure 6. SEM section views of the edge seal structure.



Mag. 4000x, 0°

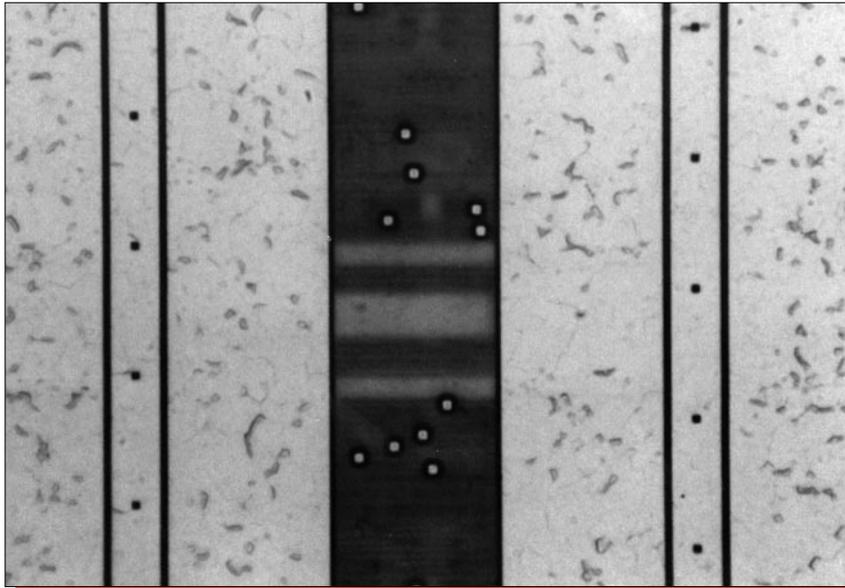


Mag. 13,500x

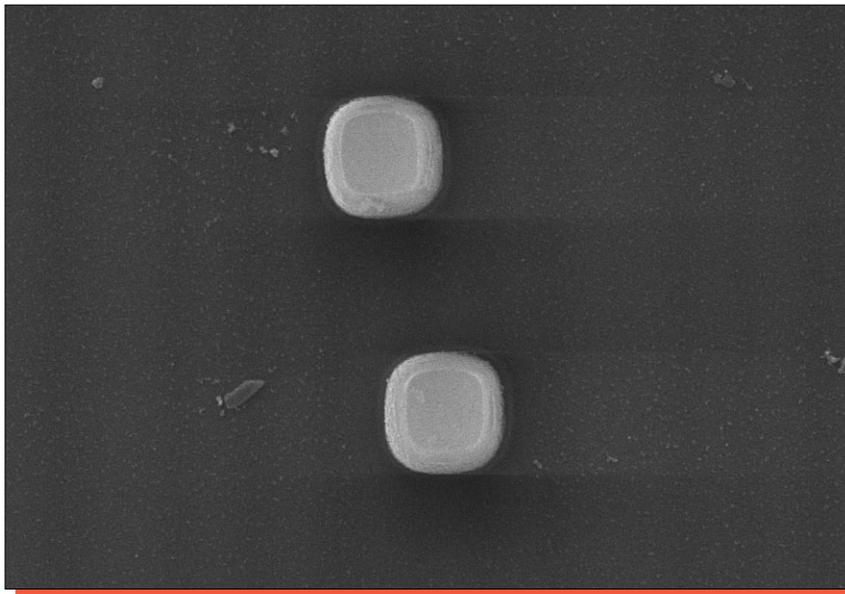


Mag. 27,000x

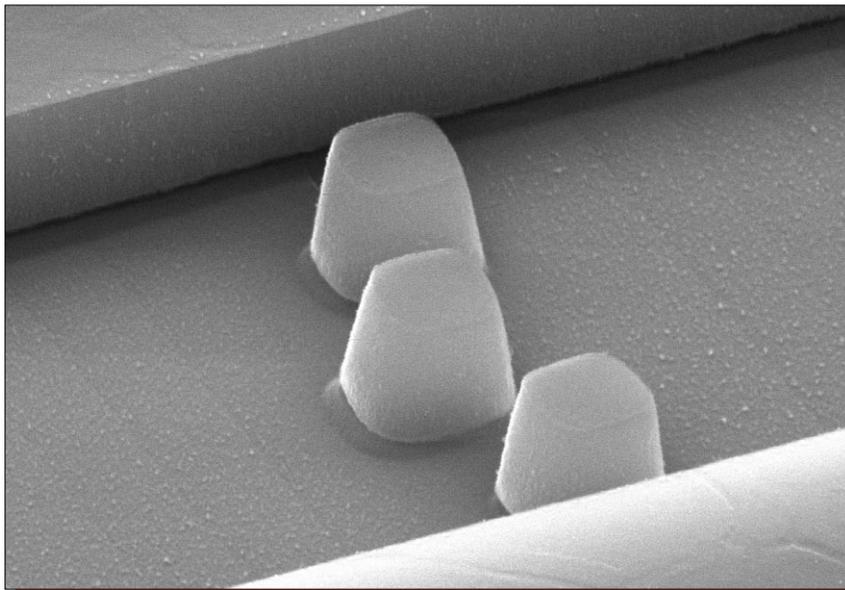
Figure 7. Topological and section views illustrating planarizing pattern.



Mag. 800x

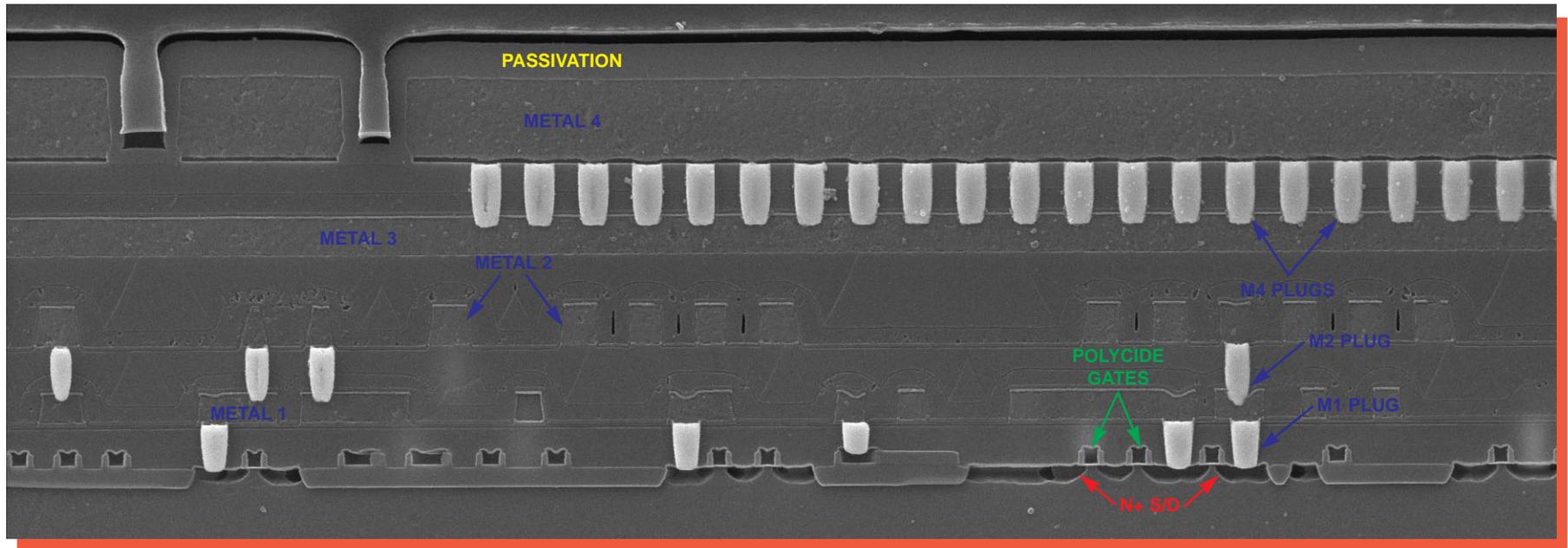


Mag. 7000x, 0°

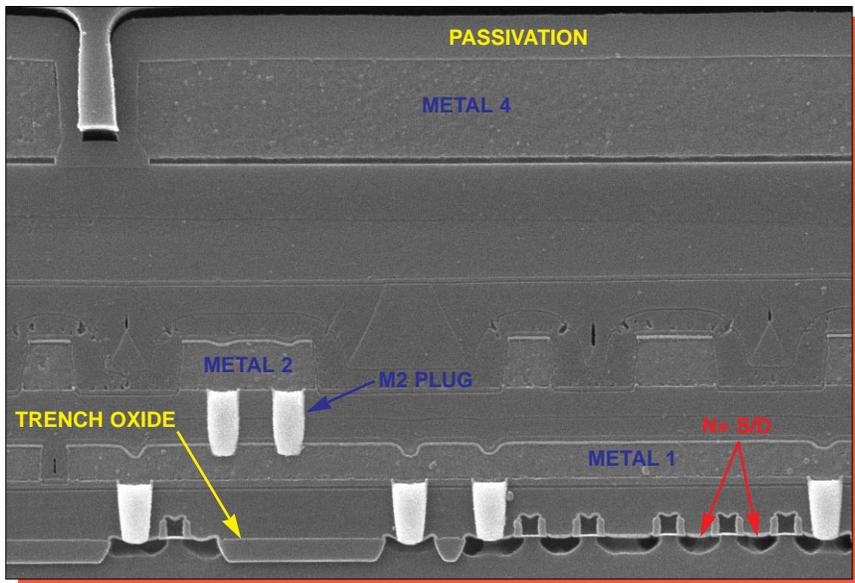


Mag. 10,000x, 55°

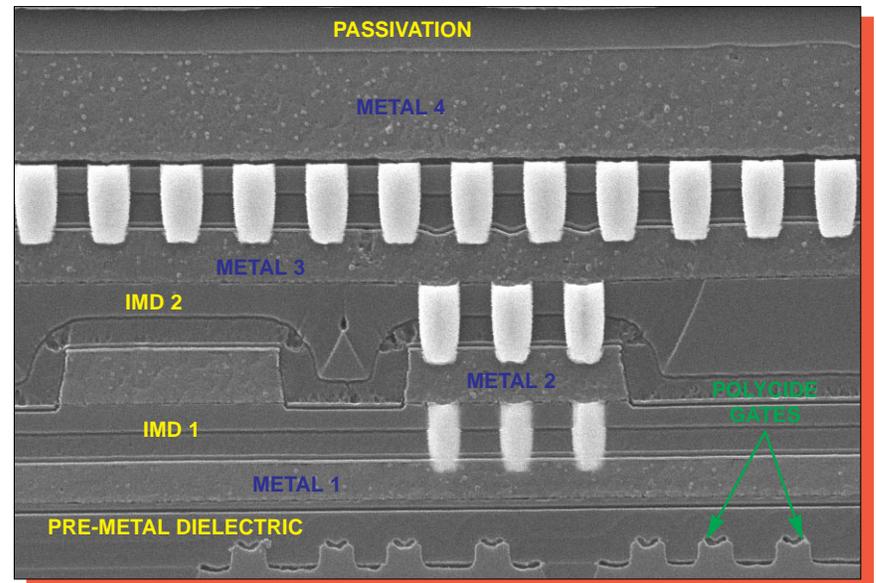
Figure 8. Optical and SEM views illustrating non-connected vias.



Mag. 7400x

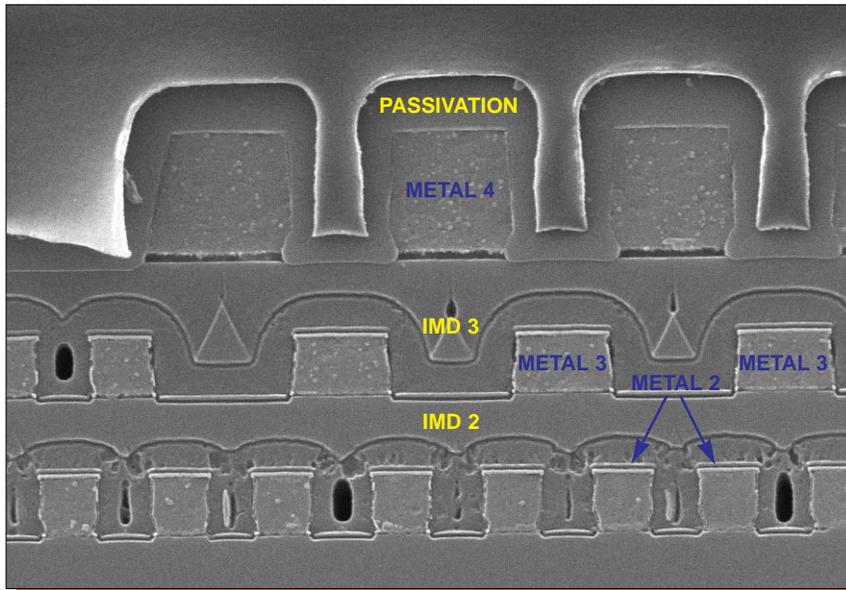


Mag. 8000x

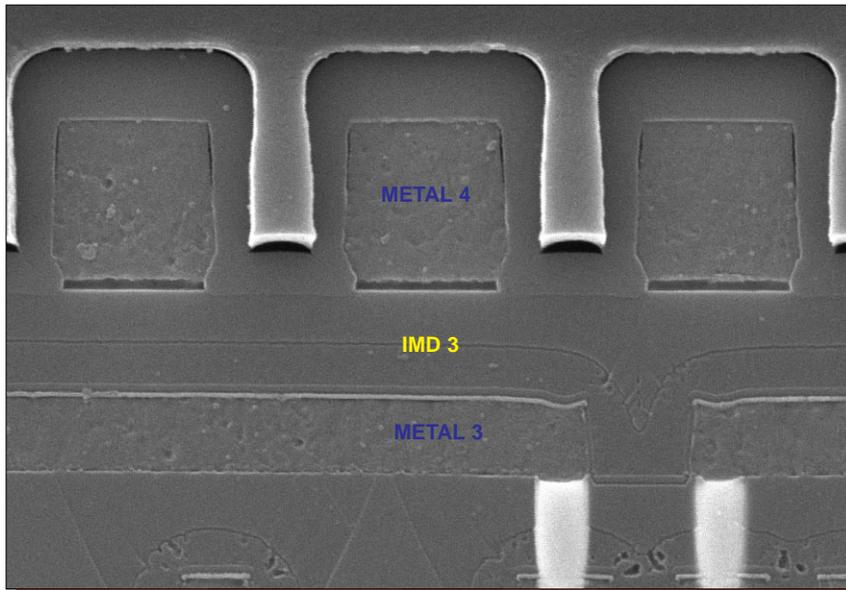


Mag. 9000x

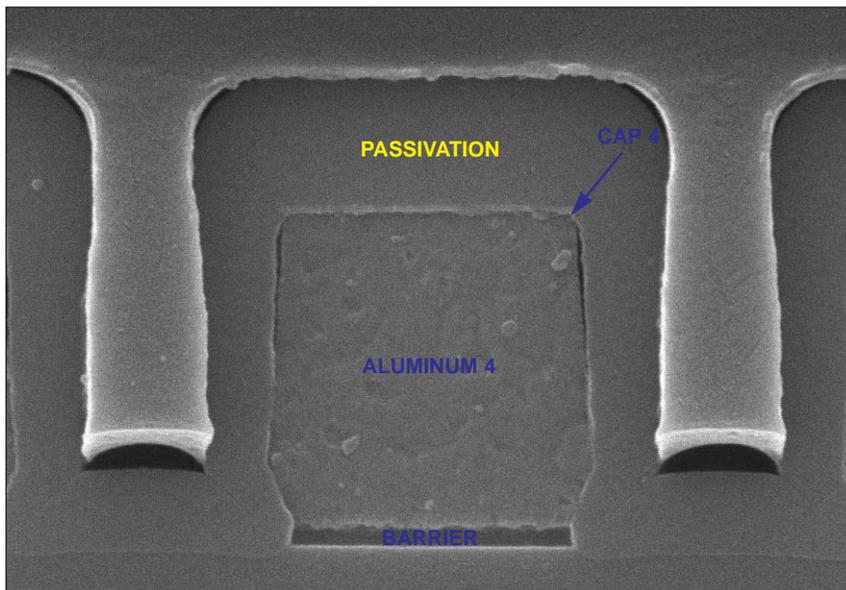
Figure 9. SEM section views illustrating general device structure.



Mag. 10,000x

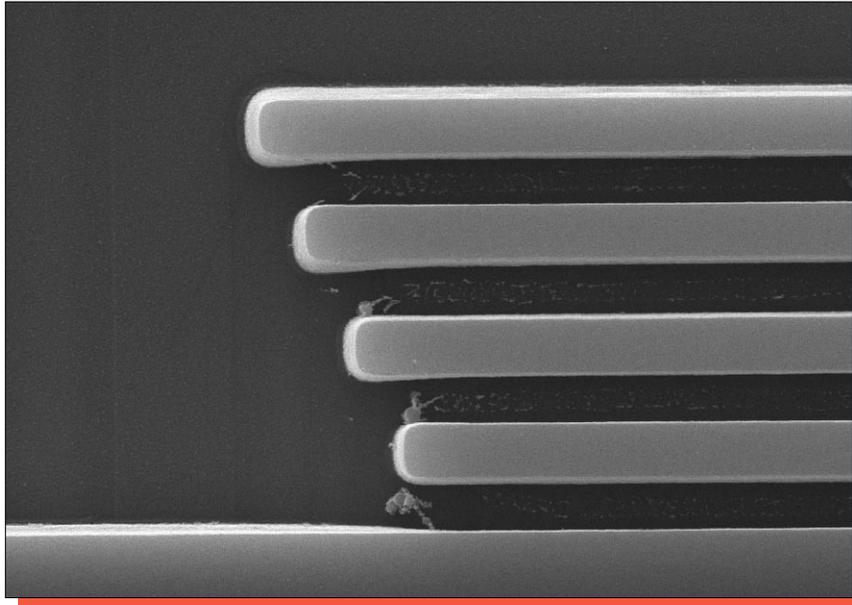


Mag. 13,000x

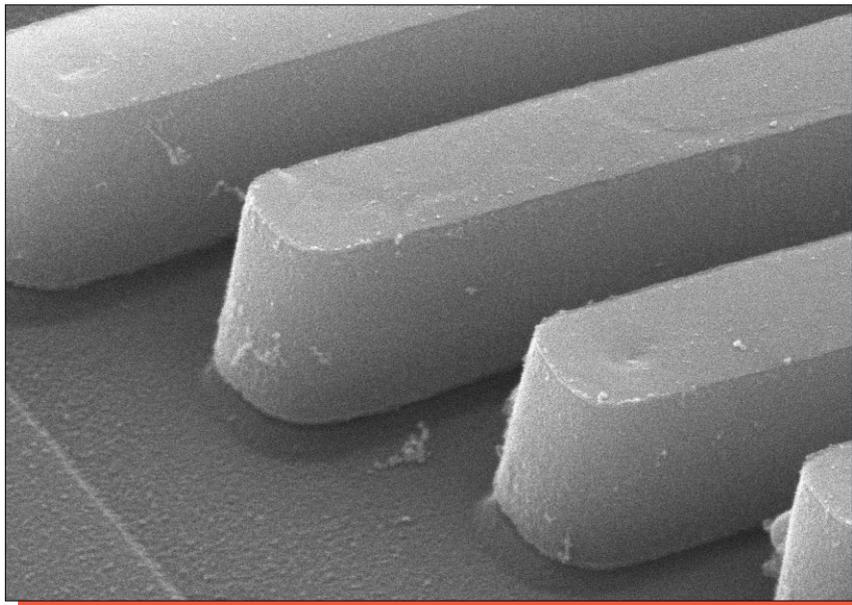


Mag. 26,000x

Figure 10. SEM section views of metal 4 line profiles.

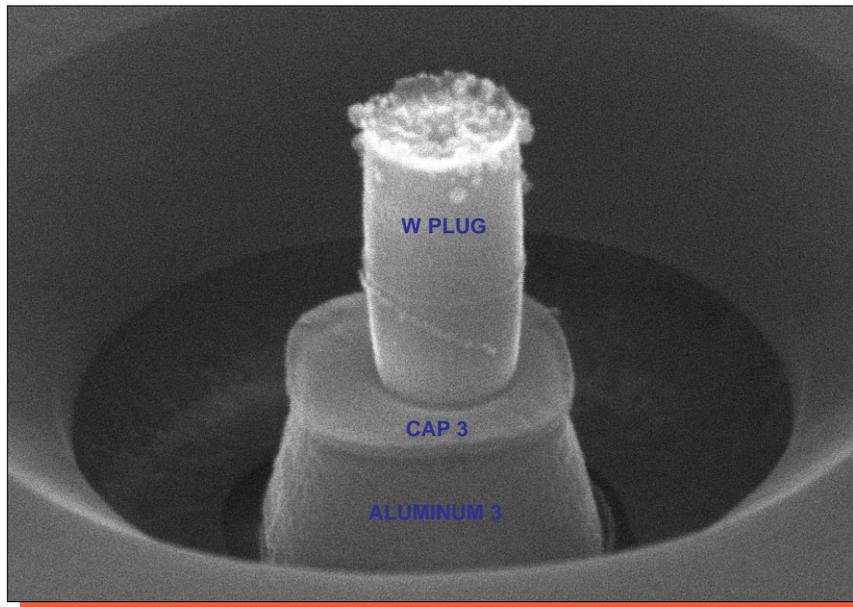


Mag. 5000x, 0°

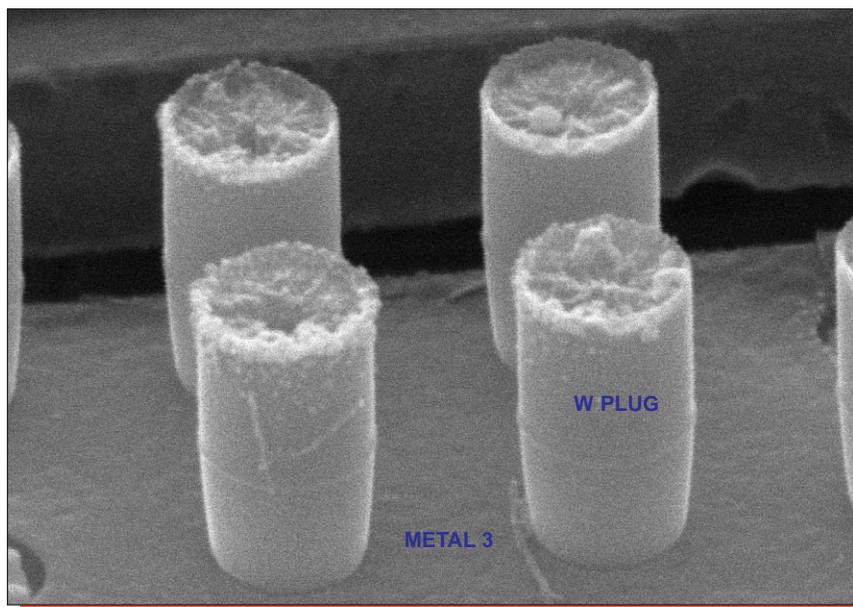


Mag. 15,000x, 55°

Figure 11. SEM views of metal 4 patterning and coverage.

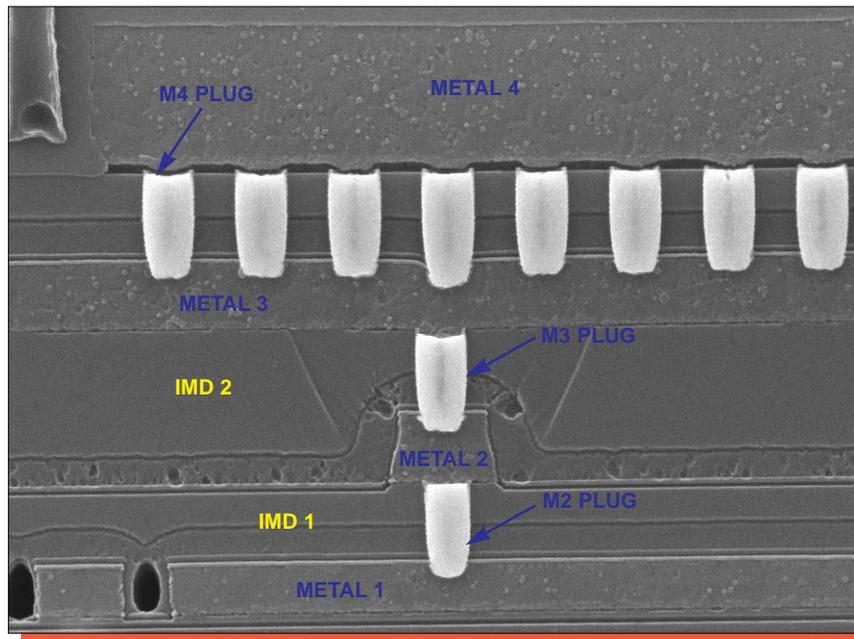


Mag. 35,000x

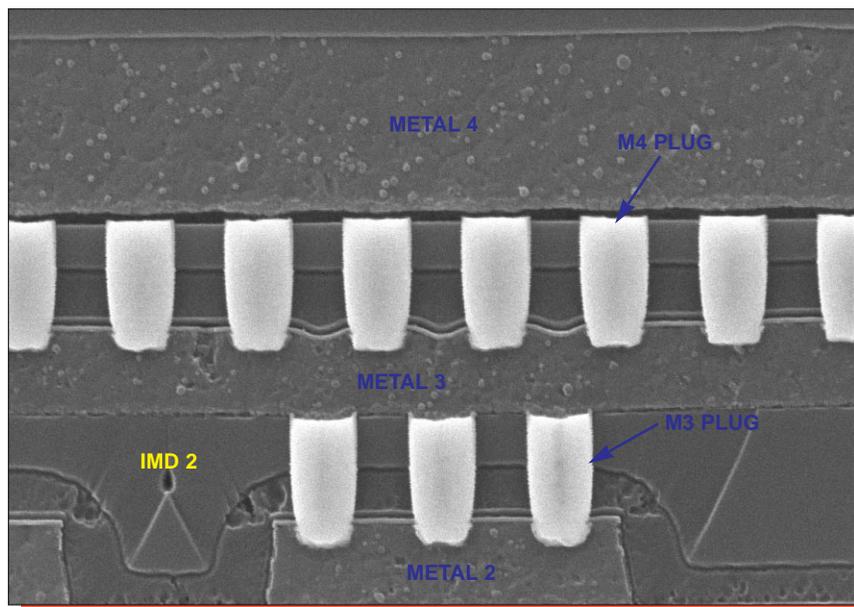


Mag. 40,000x

Figure 12. SEM views of metal 4 tungsten plugs. 55°.

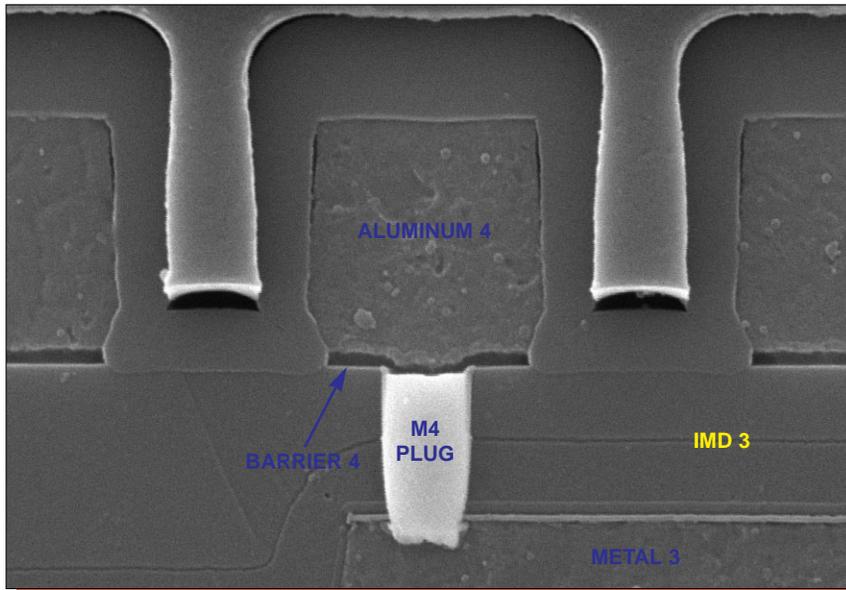


stacked vias, Mag. 11,000x

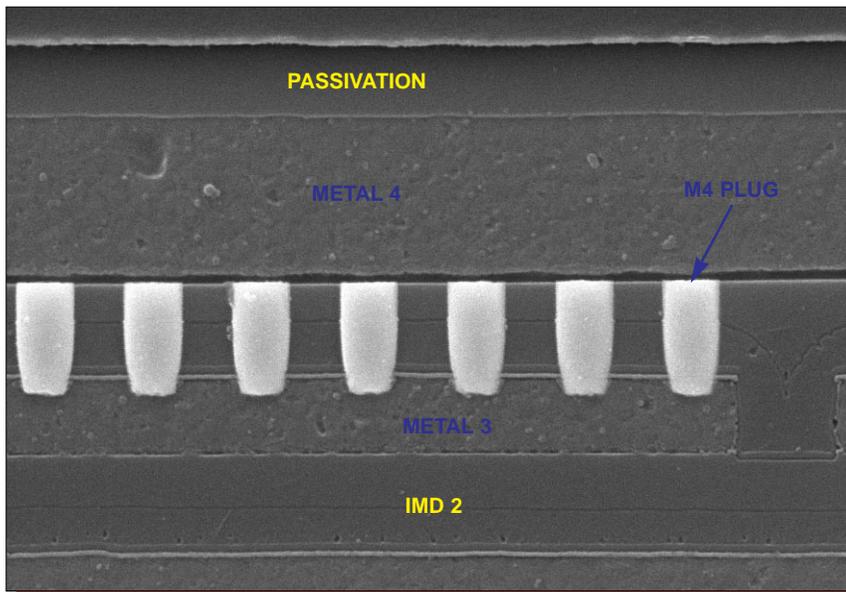


Mag. 15,000x

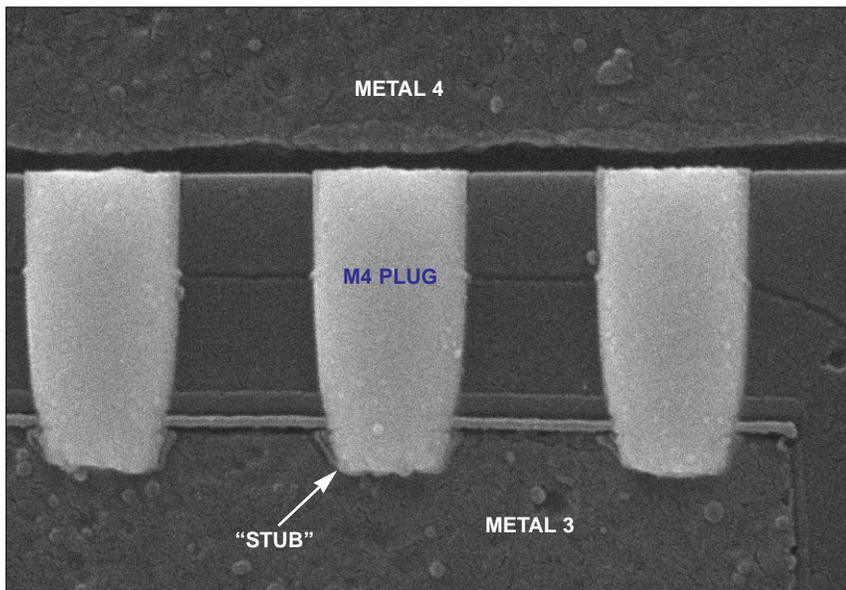
Figure 13. SEM section views of metal 4-to-metal 3 vias.



Mag. 20,000x

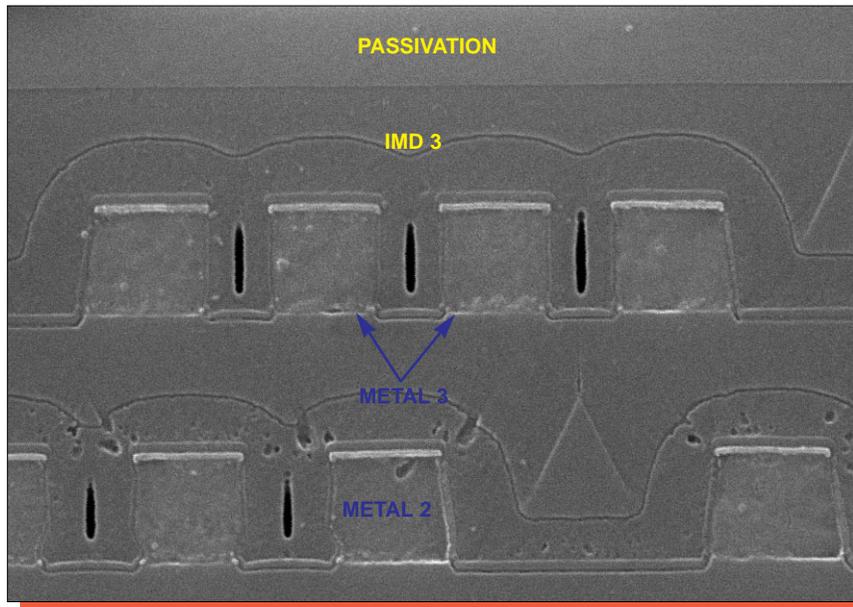


Mag. 13,000x

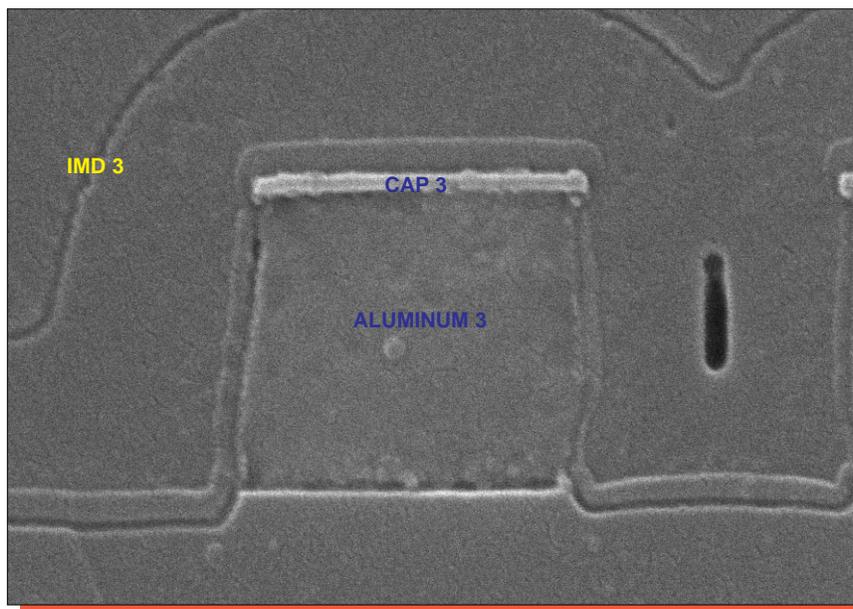


Mag. 35,000x

Figure 14. Additional SEM section views of metal 4-to-metal 3 vias.

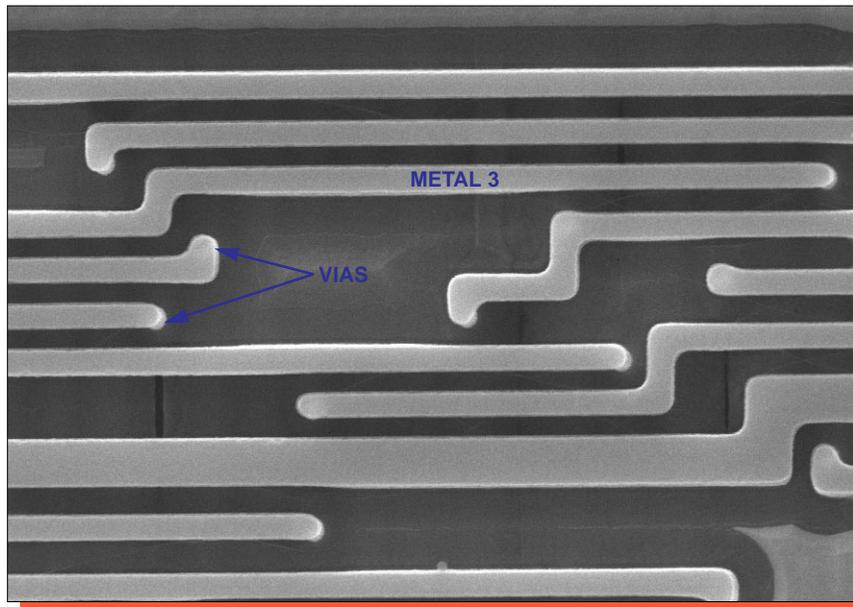


Mag. 17,600x

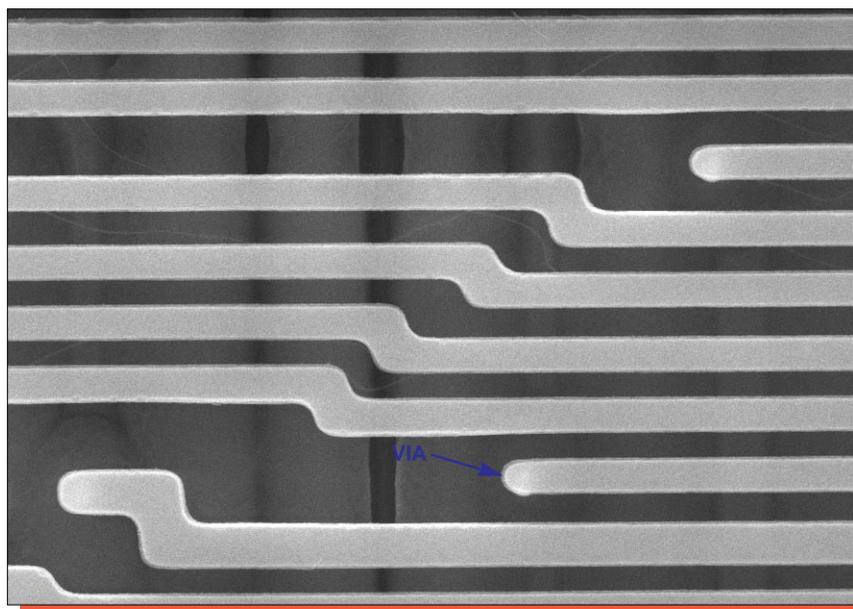


Mag. 52,000x

Figure 15. SEM section views of metal 3 line profiles.

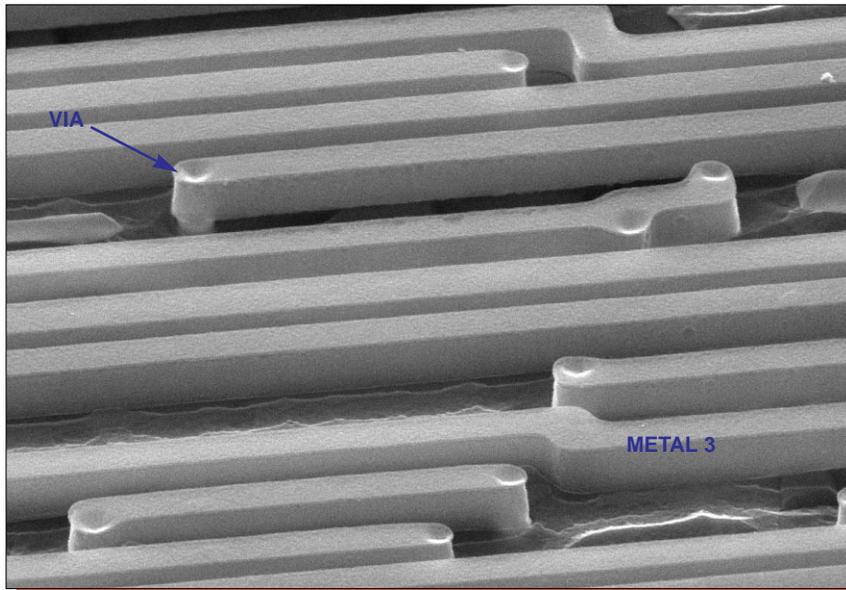


Mag. 5000x

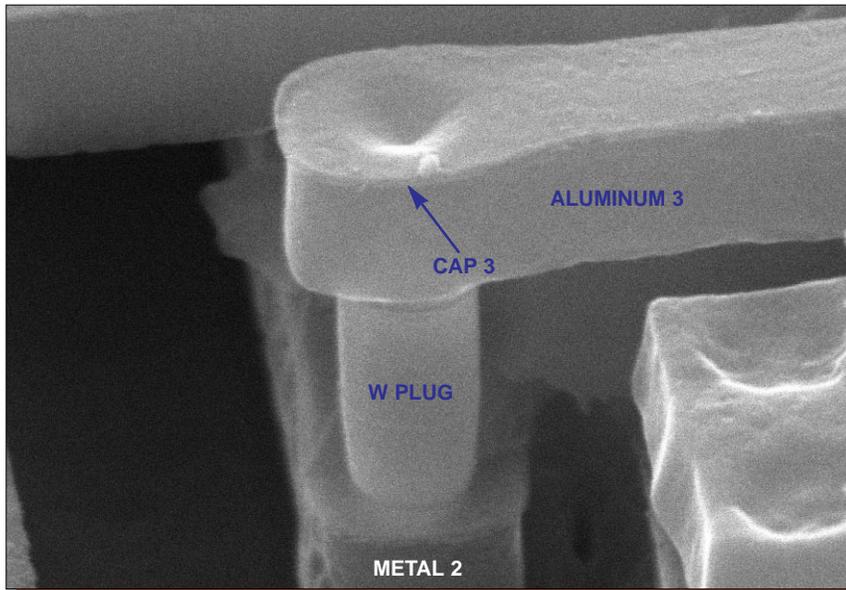


Mag. 6500x

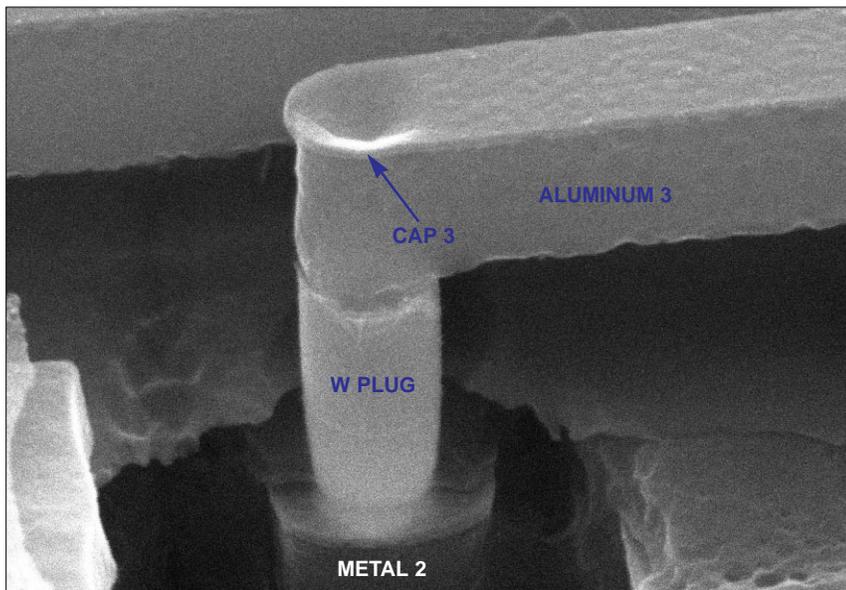
Figure 16. Topological SEM views of metal 3 patterning. 0°.



Mag. 8000x

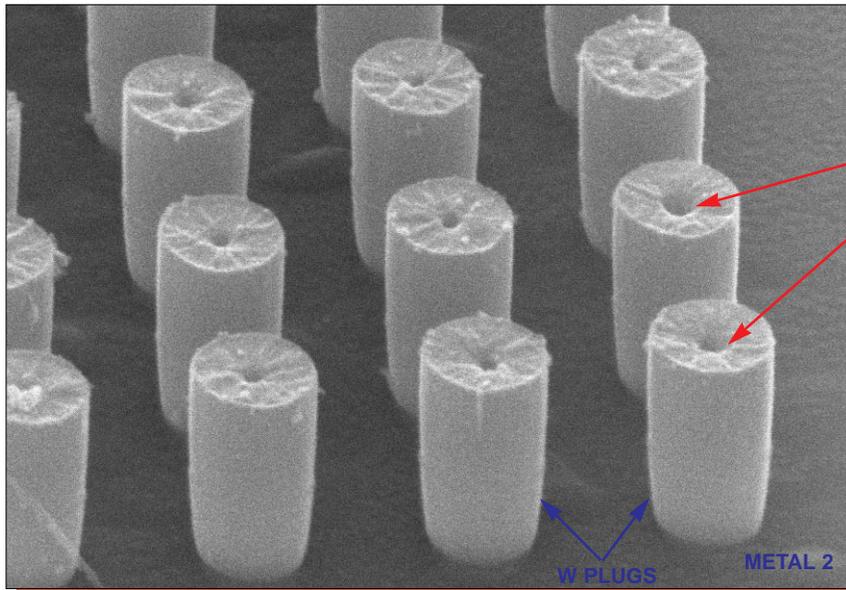


Mag. 31,000x



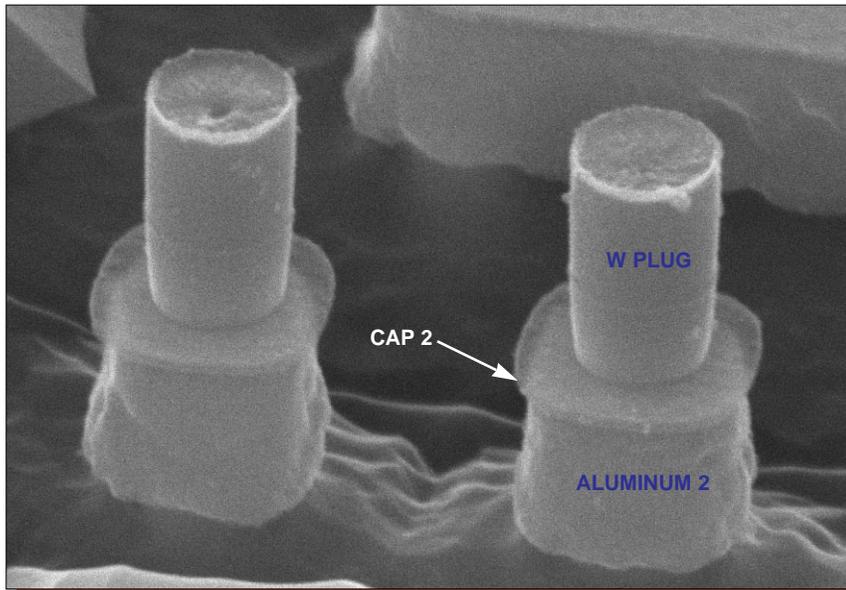
Mag. 31,000x

Figure 17. SEM views of general metal 3 integrity. 55°.

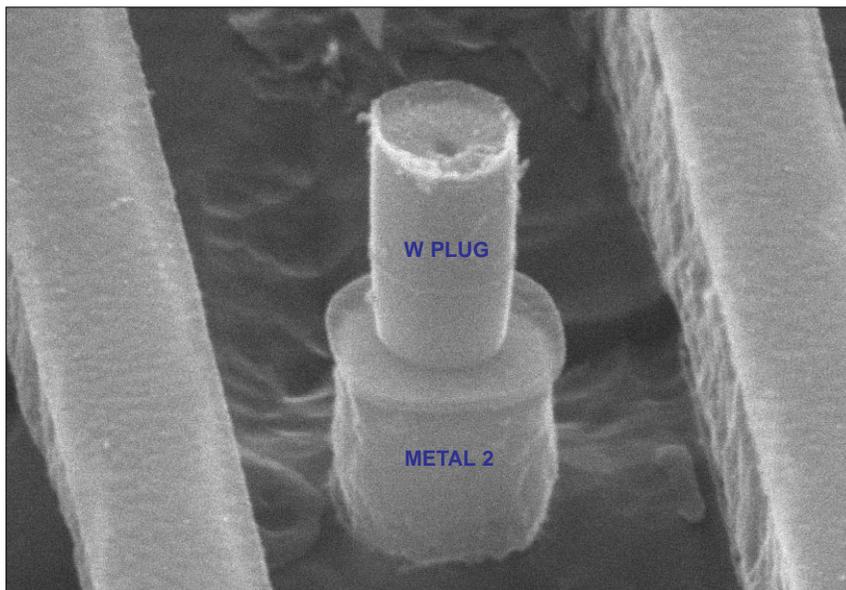


"HOLES"
(INCOMPLETE FILL)

Mag, 30,000x

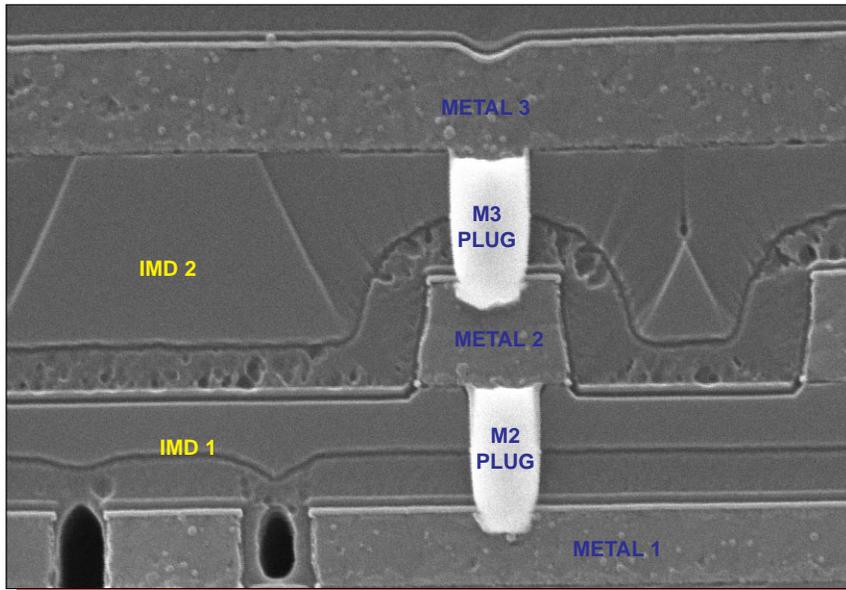


Mag. 35,000x

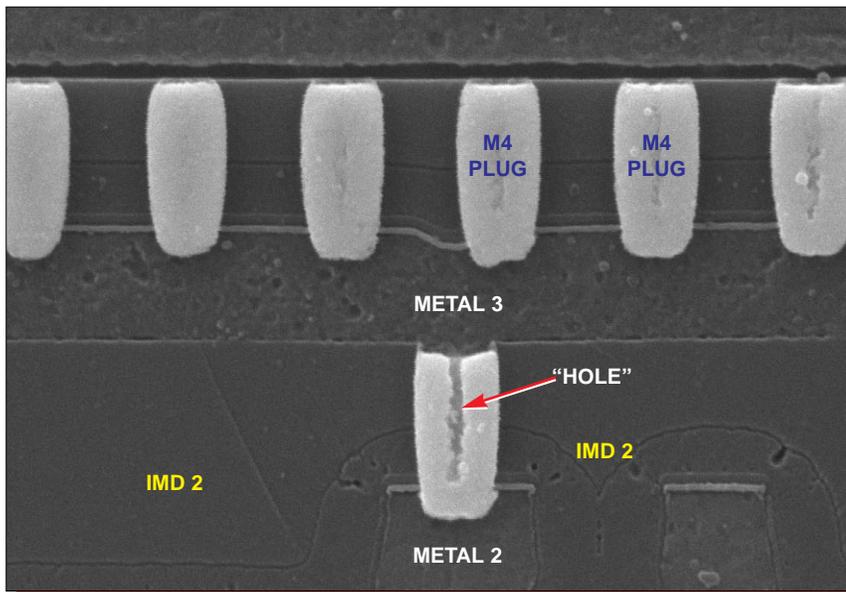


Mag. 35,000x

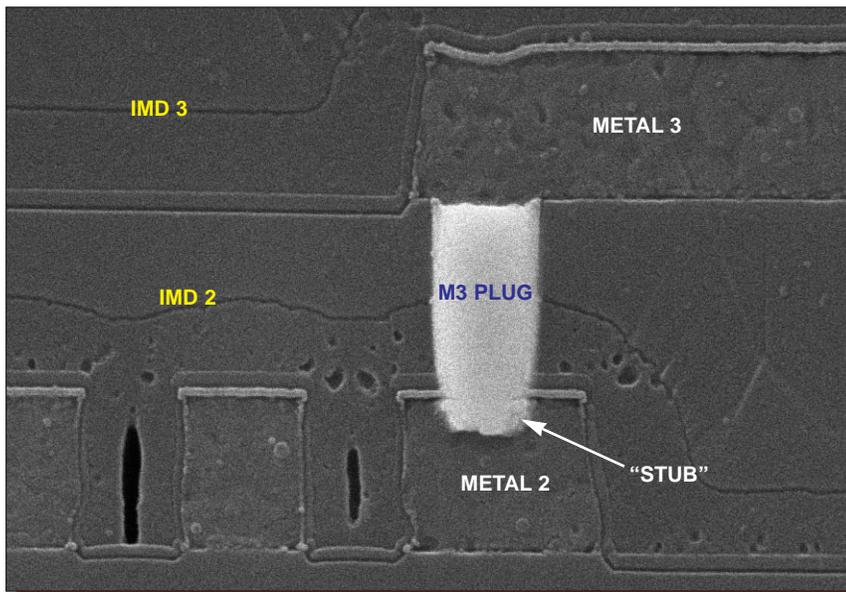
Figure 18. SEM views of metal 3 tungsten plugs. 55°.



Stacked vias,
Mag. 17,600x

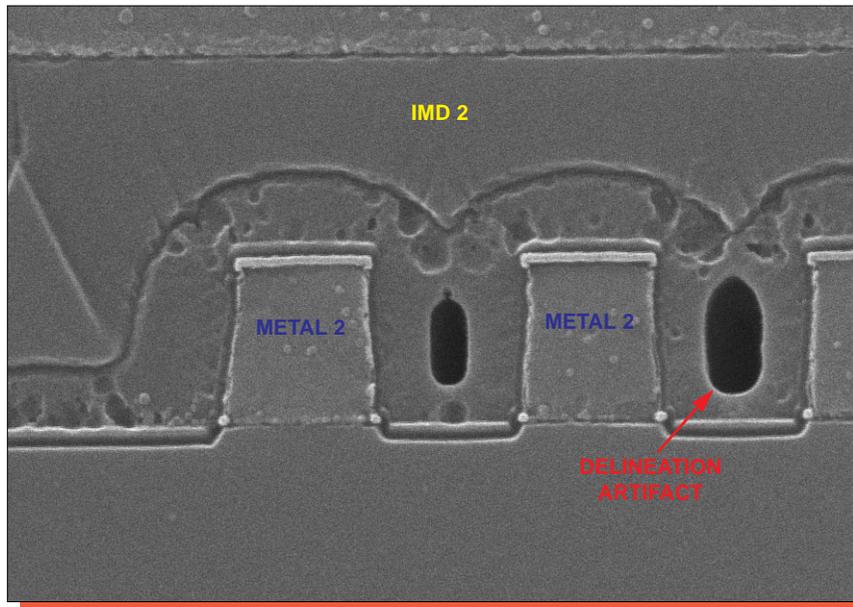


Mag. 20,000x

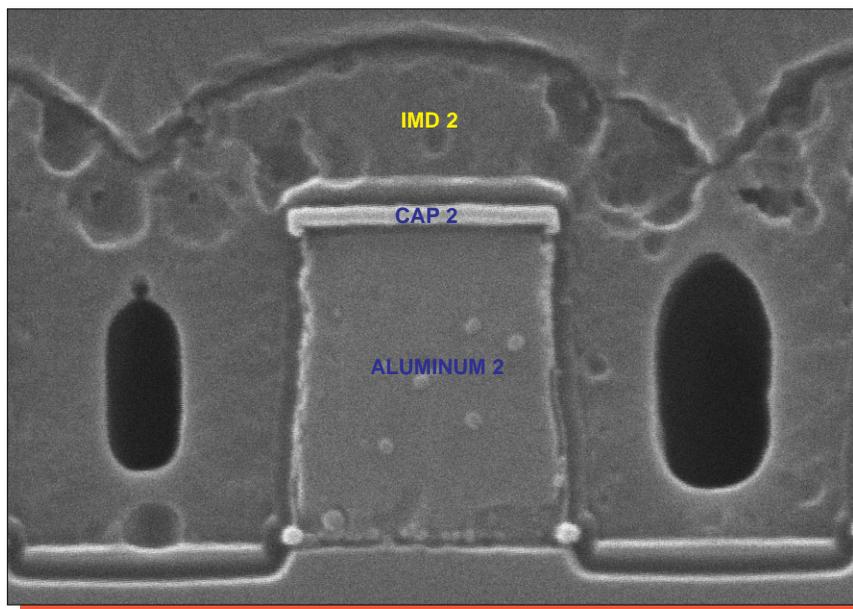


Mag. 26,000x

Figure 19. SEM section views of metal 3-to-metal 2 vias.

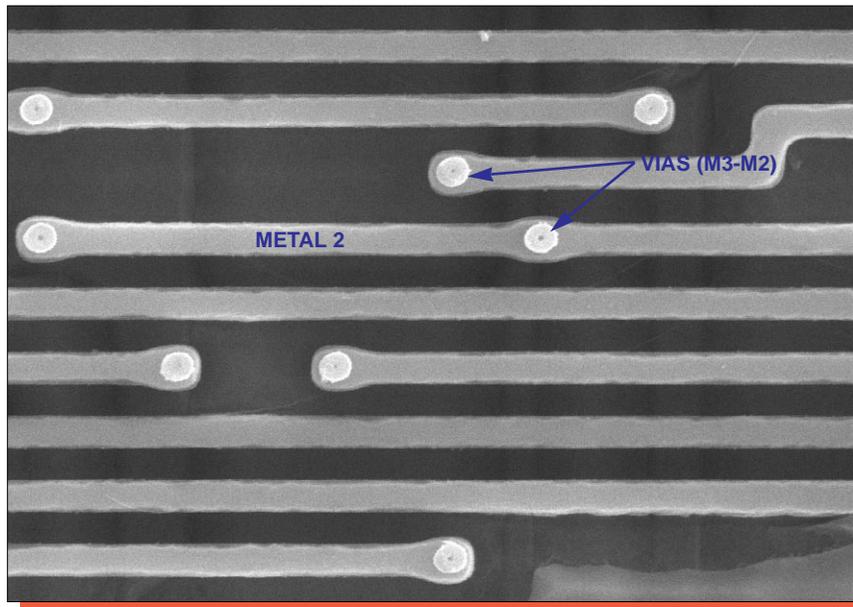


Mag. 26,000x

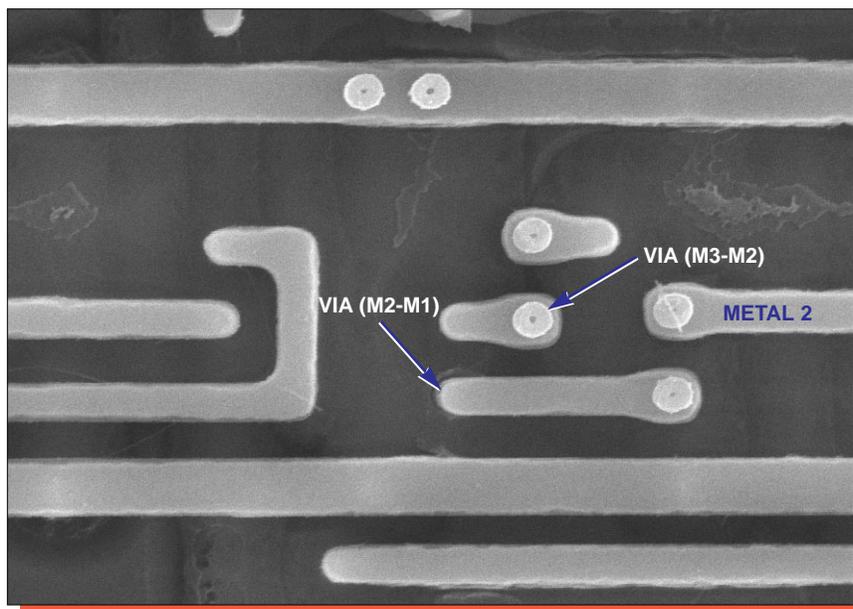


Mag. 52,000x

Figure 20. SEM section views of metal 2 line profiles.

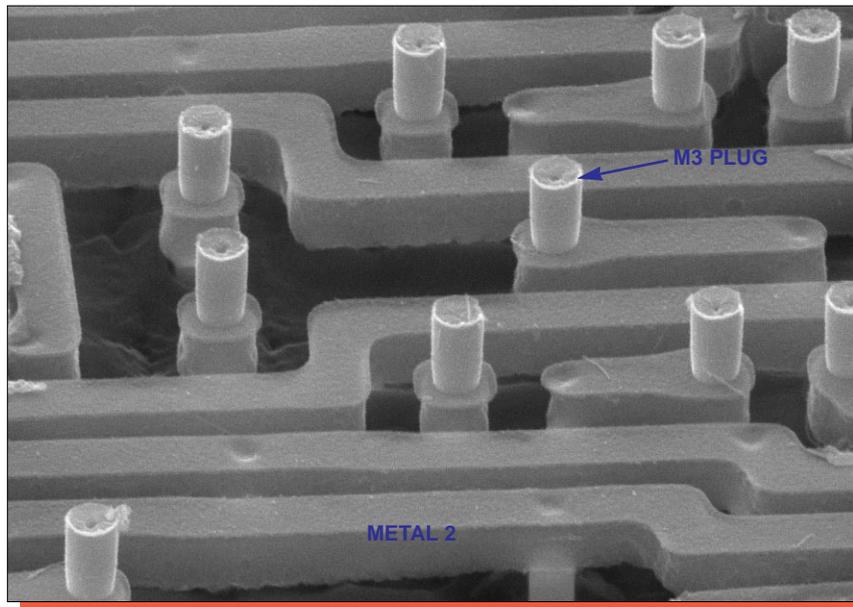


Mag. 7000x

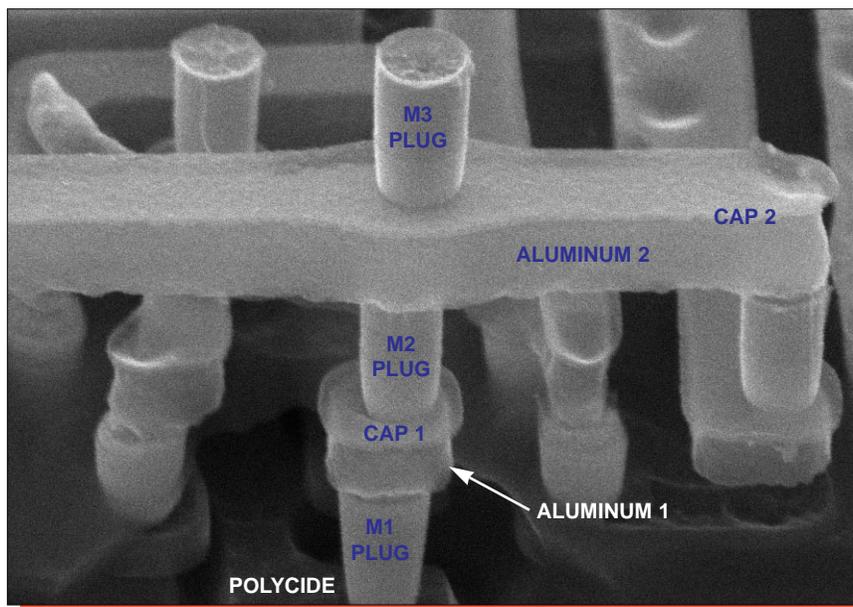


Mag. 9000x

Figure 21. Topological SEM views of metal 2 patterning. 0°.

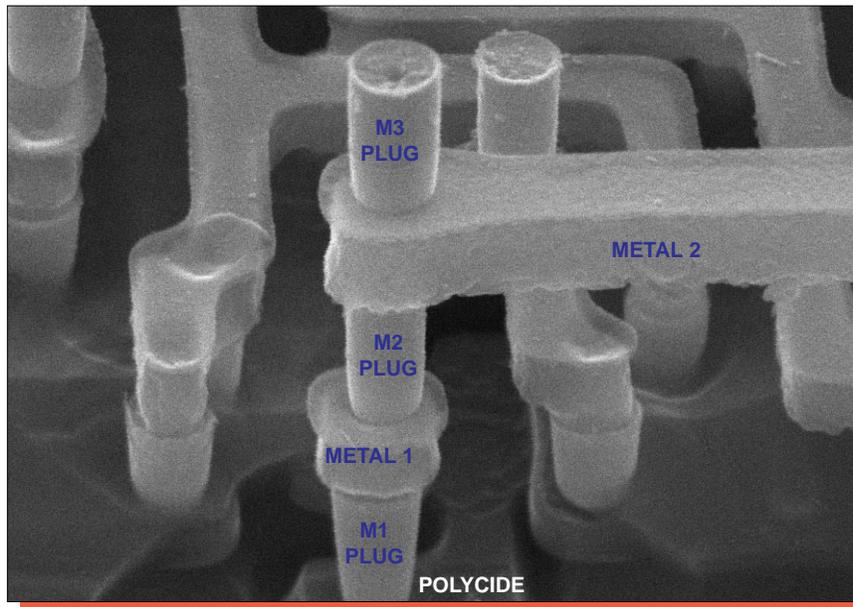


Mag. 12,000x

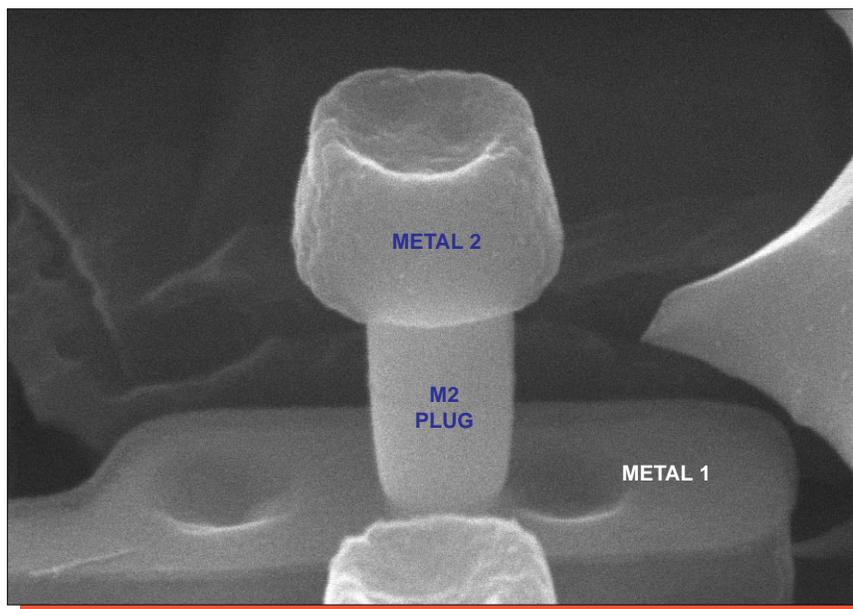


stacked structure, Mag. 22,000x

Figure 22. SEM views of general metal 2 coverage. 55°.

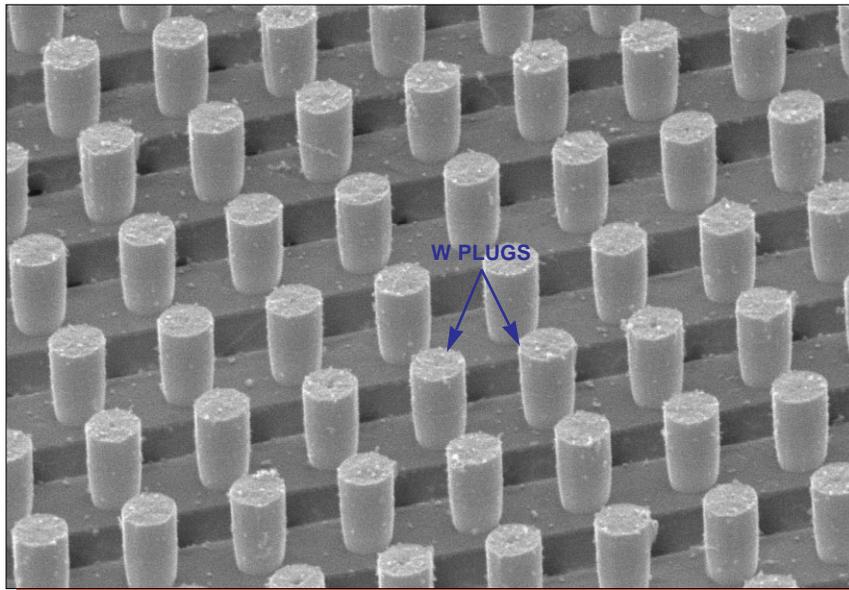


Mag. 23,000x

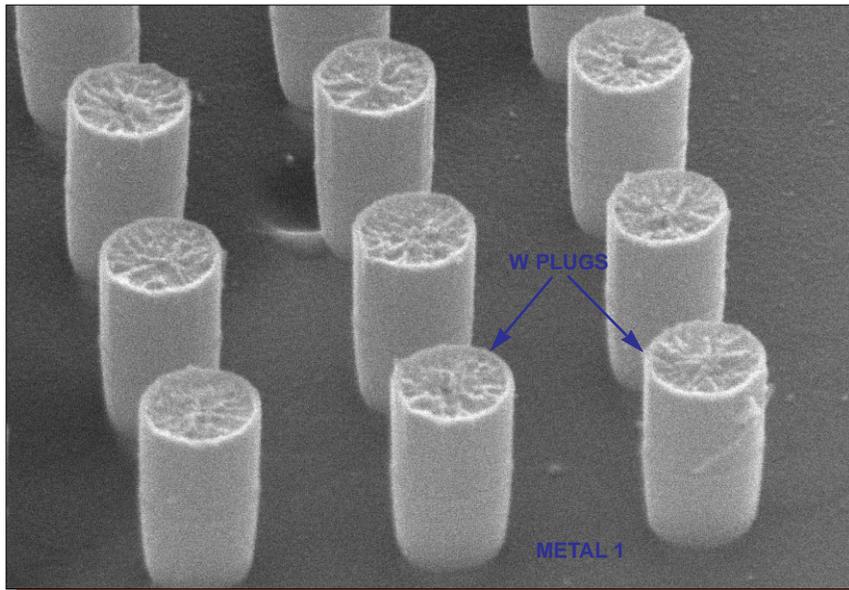


Mag. 35,000x

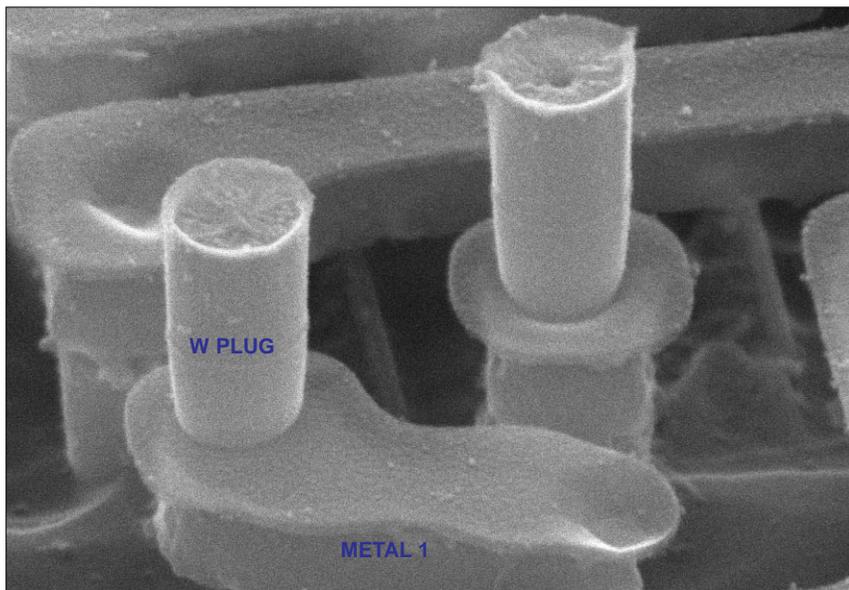
Figure 22a. SEM details of metal 2 coverage. 55°.



Mag. 13,000x

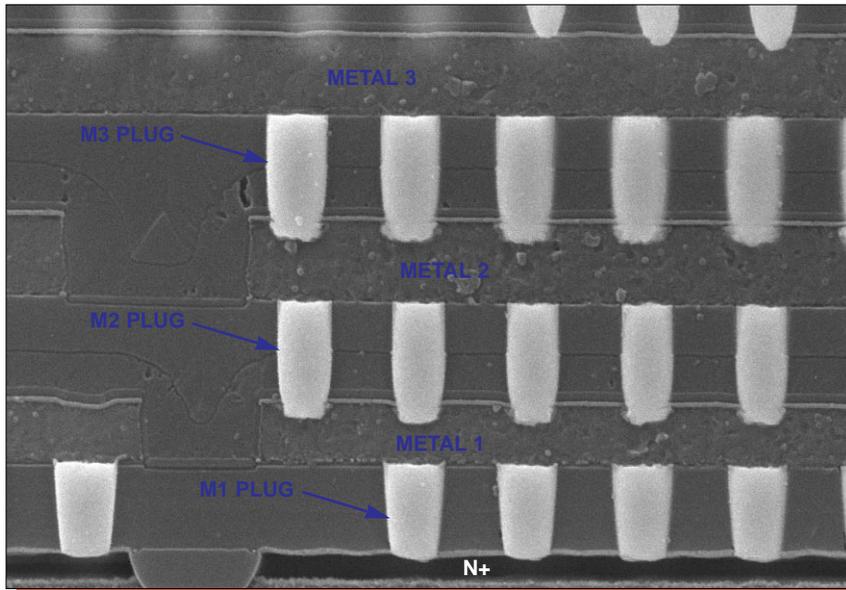


Mag. 33,600x

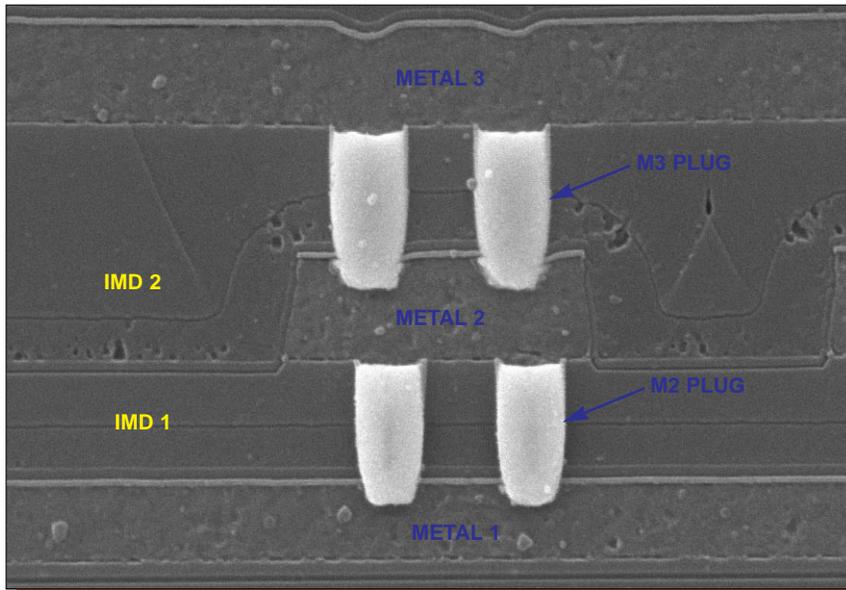


Mag. 40,000x

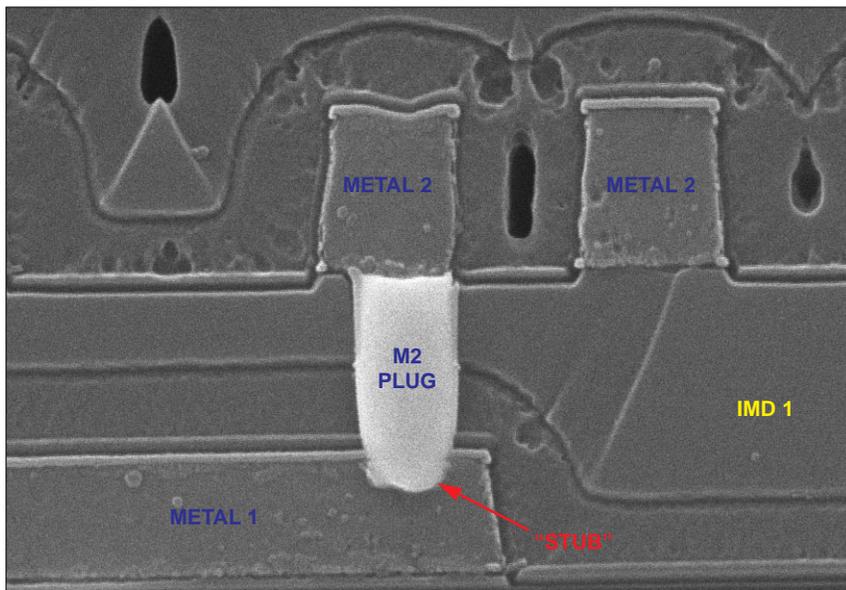
Figure 23. SEM views of metal 2 tungsten plugs. 55°.



stacked vias,
Mag. 13,500x

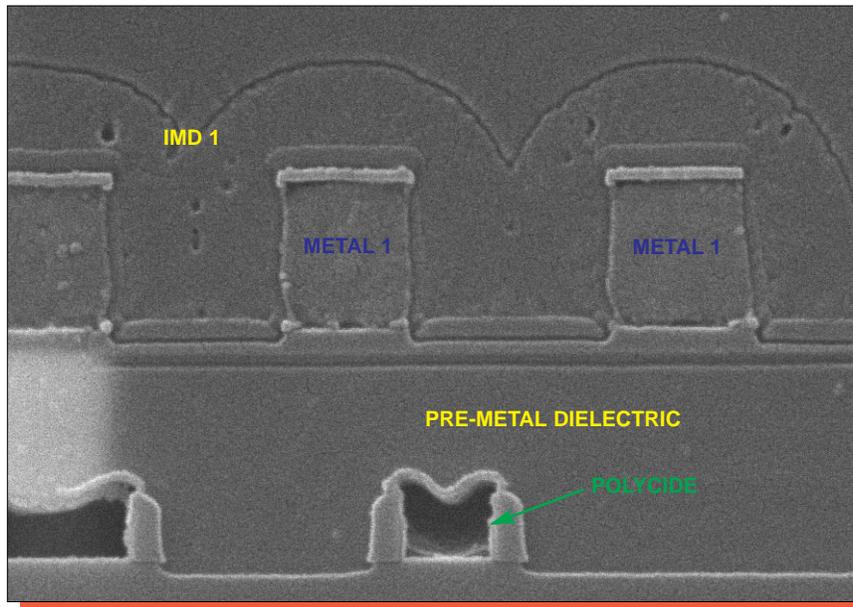


Mag. 17,600x

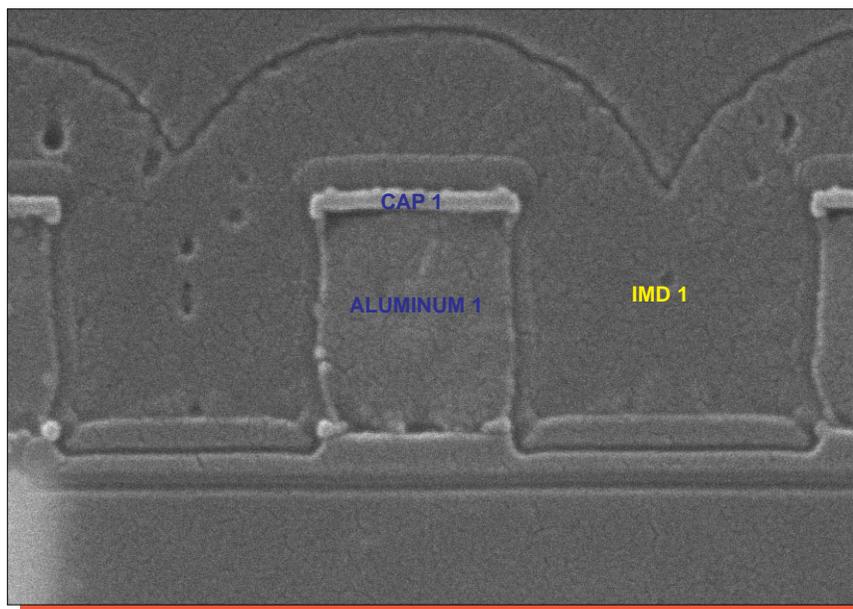


Mag. 26,000x

Figure 24. SEM section views of metal 2-to-metal 1 vias.



Mag. 35,000x



Mag. 52,000x

Figure 25. SEM section views of metal 1 line profiles.

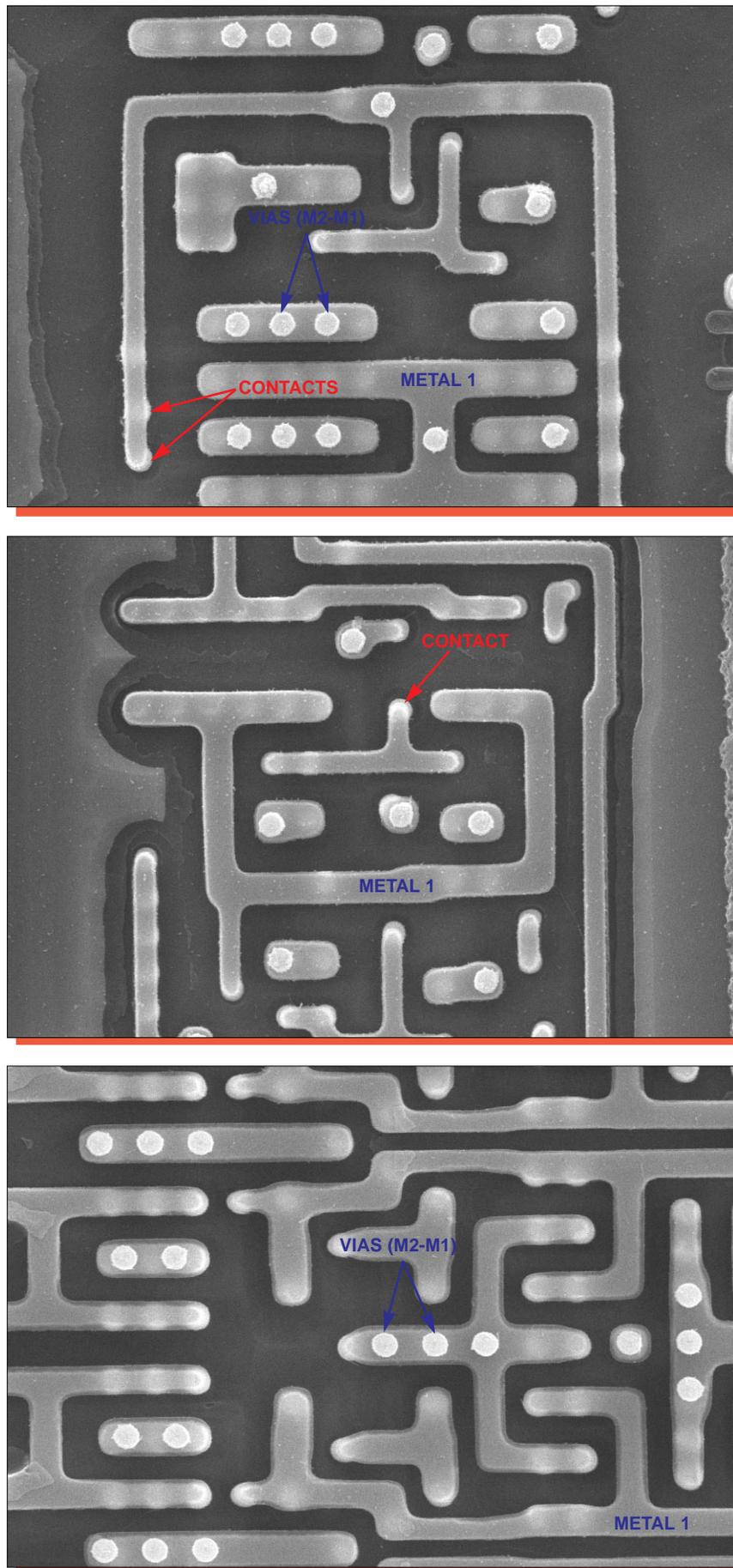
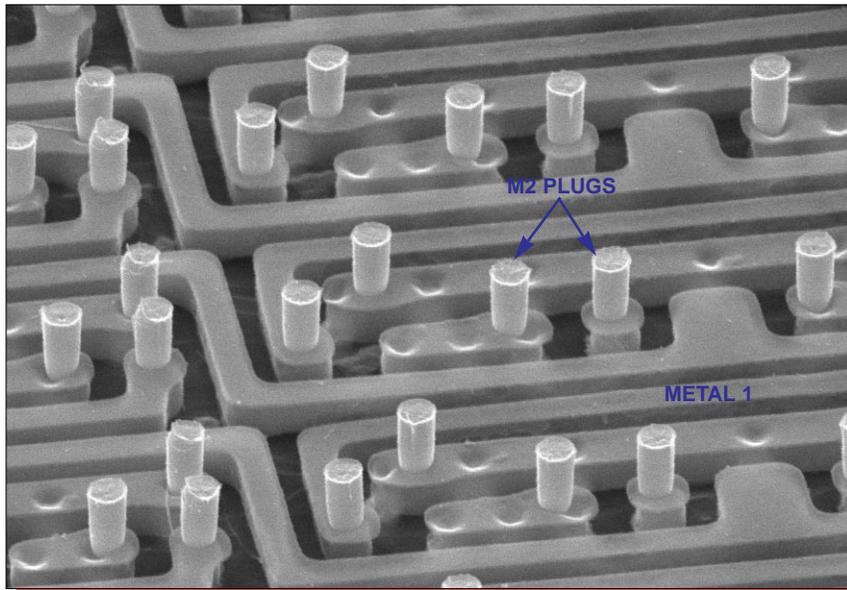
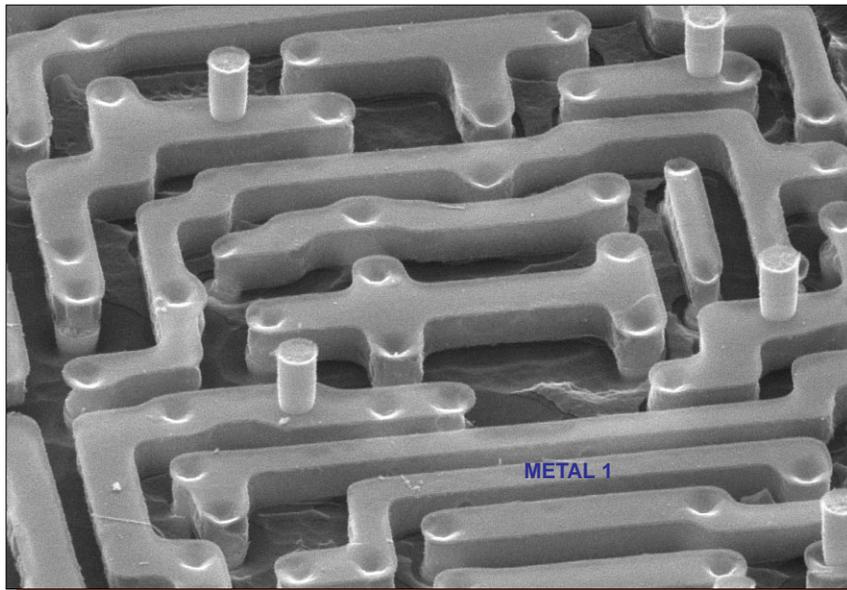


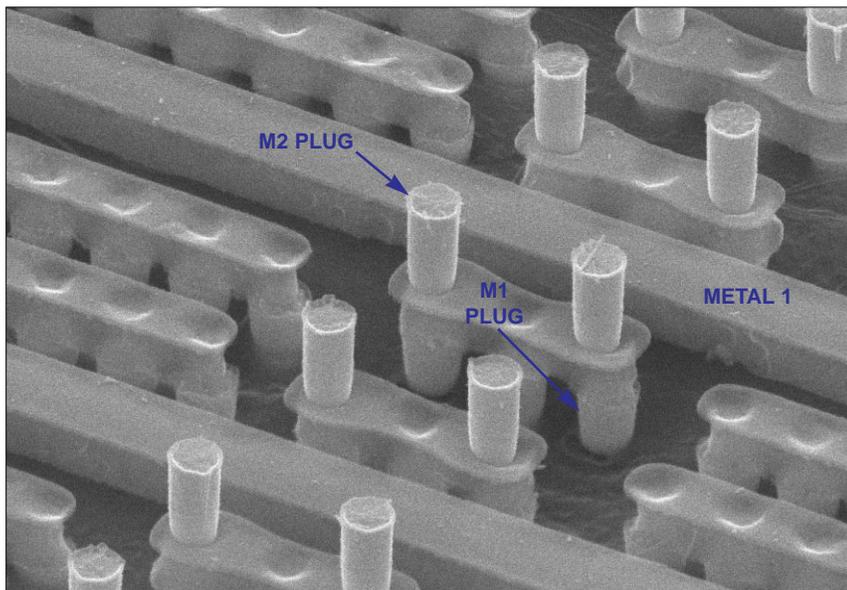
Figure 26. Topological SEM views of metal 1 patterning. Mag. 6500x, 0°.



Mag. 10,000x

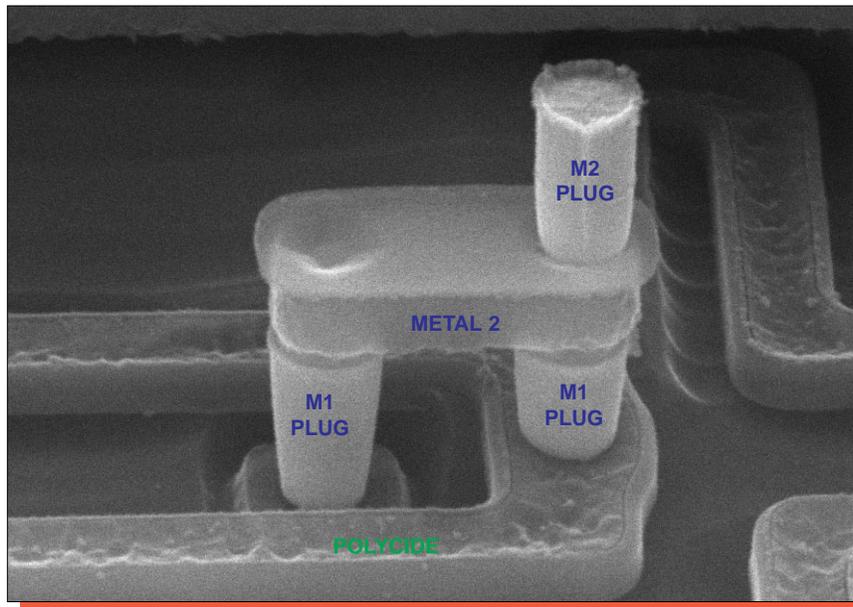


Mag. 10,000x

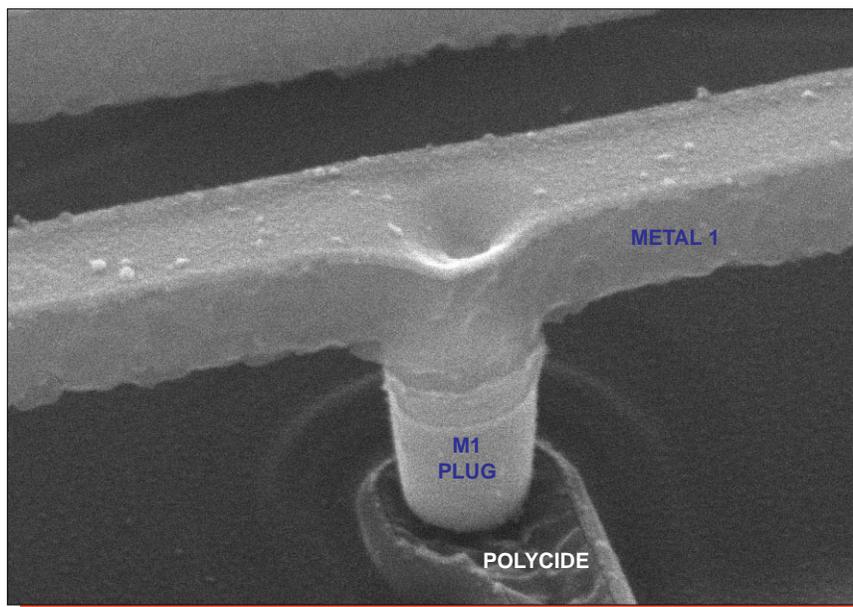


Mag. 15,000x

Figure 27. SEM views of general metal 1 coverage. 55°.

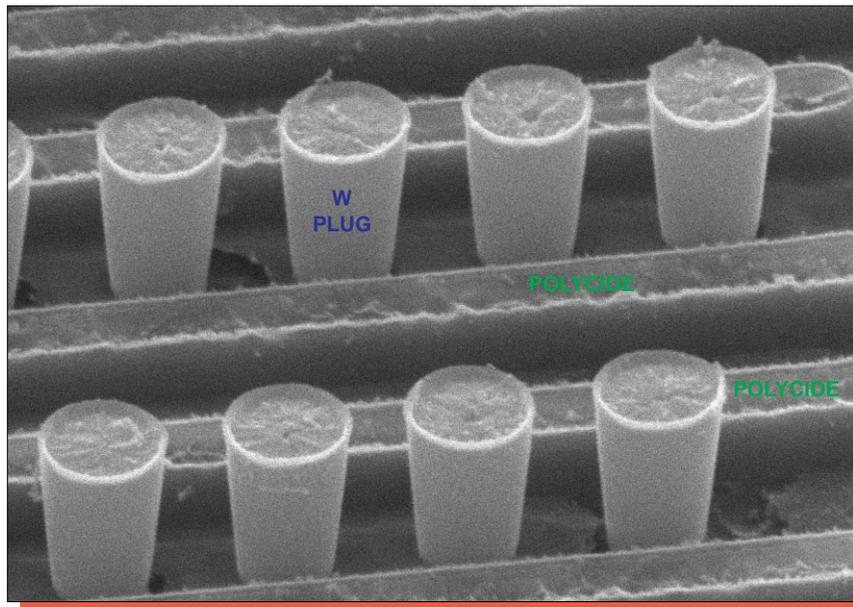


Mag. 27,000x

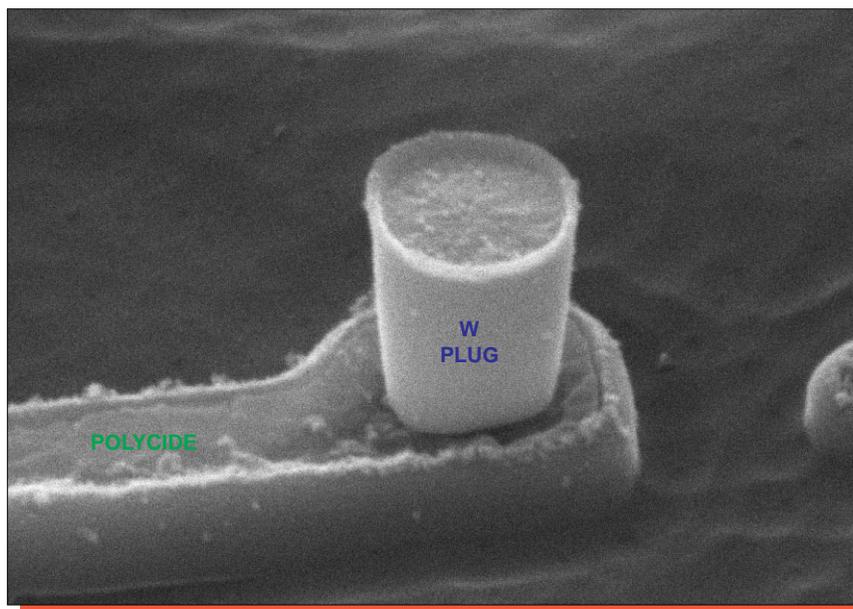


Mag. 35,000x

Figure 28. SEM details of metal 1 coverage. 55°.

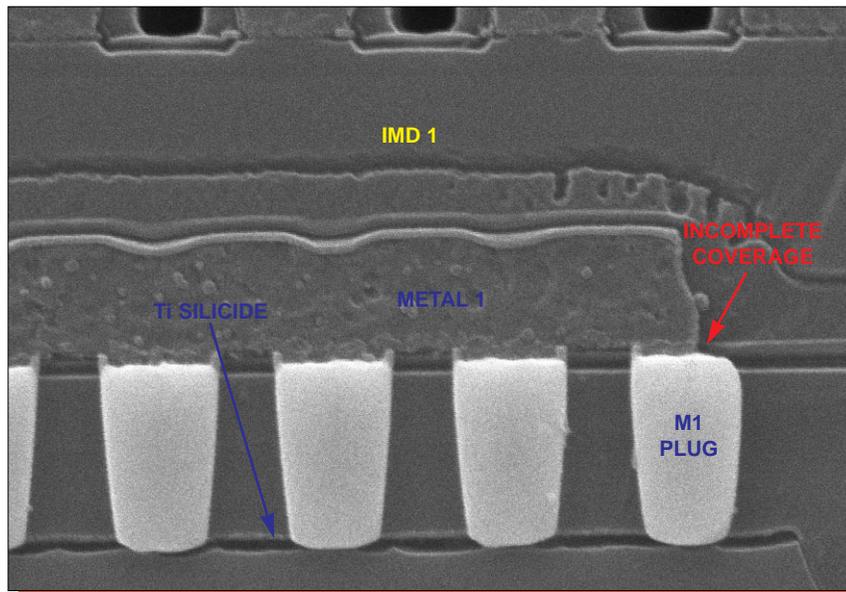


Mag. 30,000x

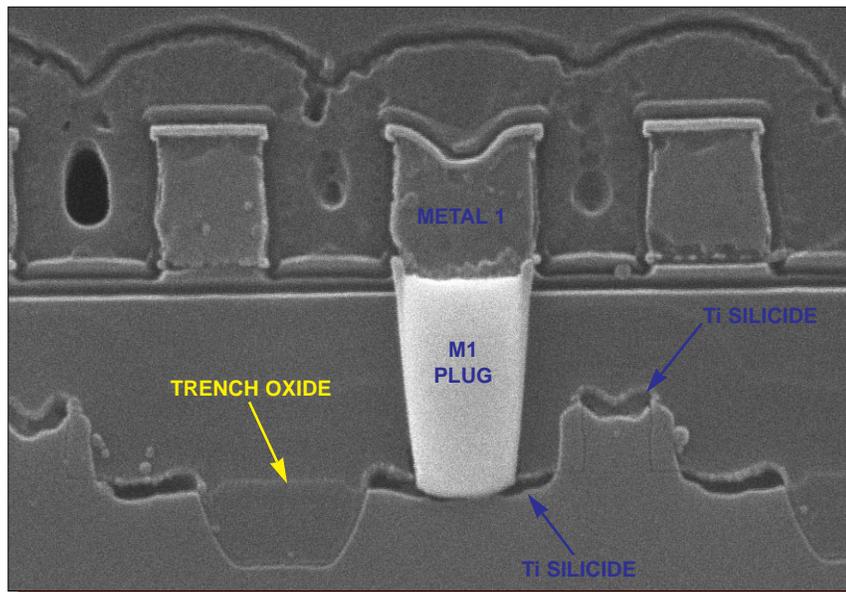


Mag. 52,000x

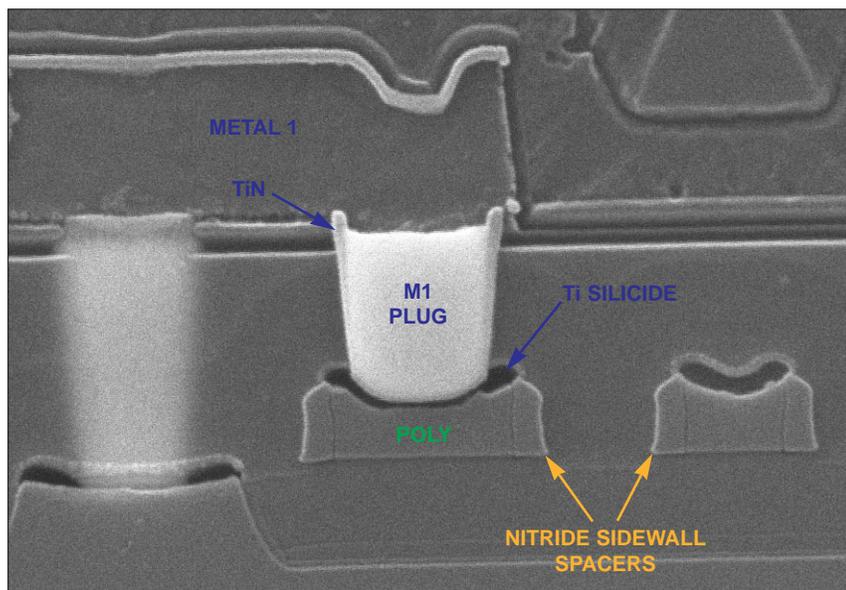
Figure 29. SEM views of metal 1 plugs. 55°.



metal-to-diffusion,
Mag. 26,000x

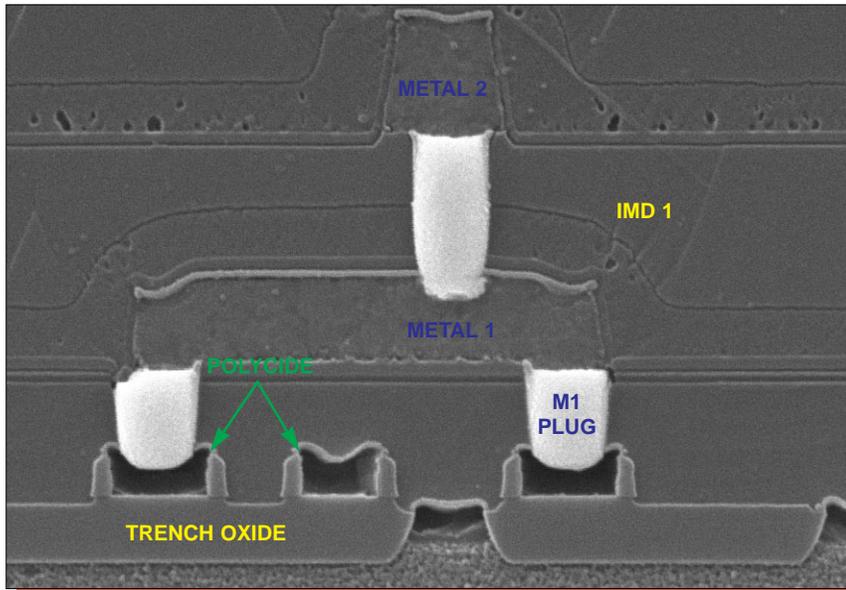


metal 1-to-diffusion,
Mag. 30,000x

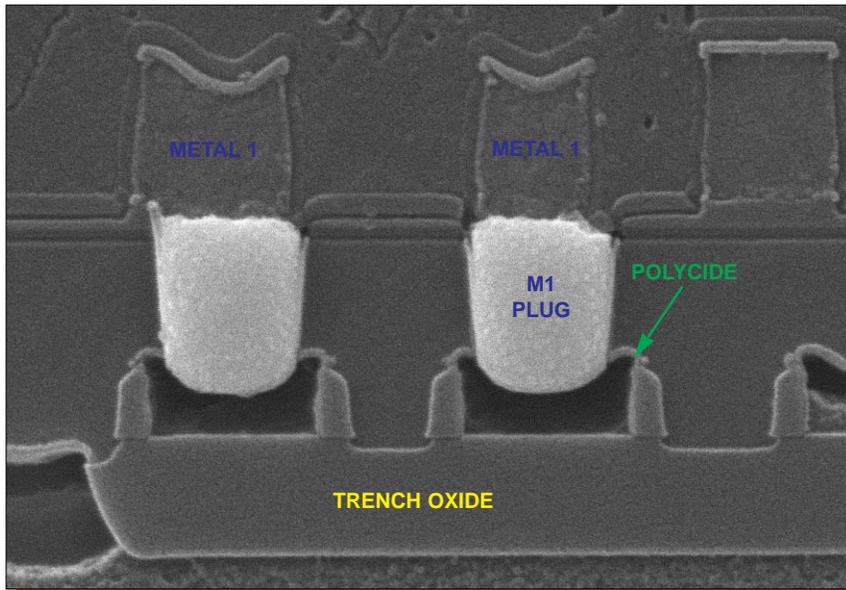


metal 1-to-polycide,
Mag. 35,000x

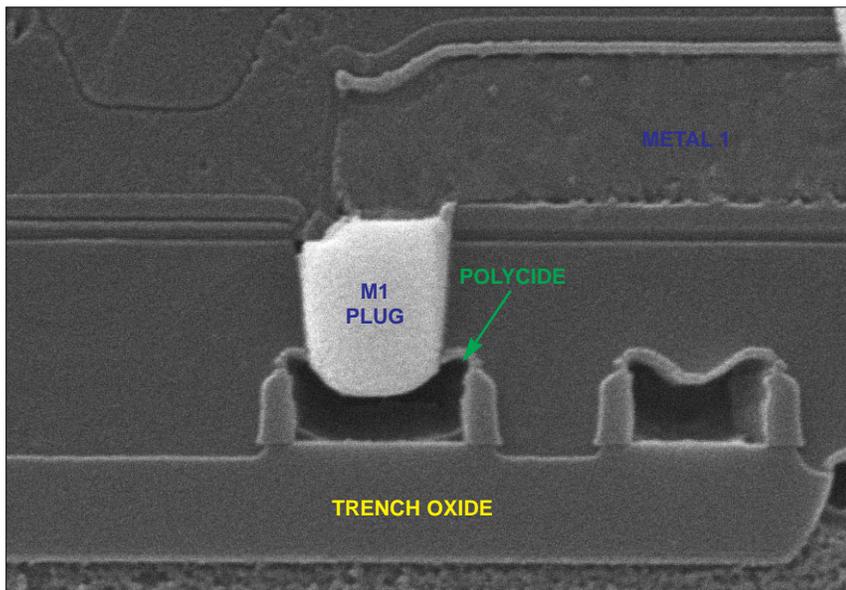
Figure 30. Glass etch section views of metal 1 contacts.



Mag. 20,000x

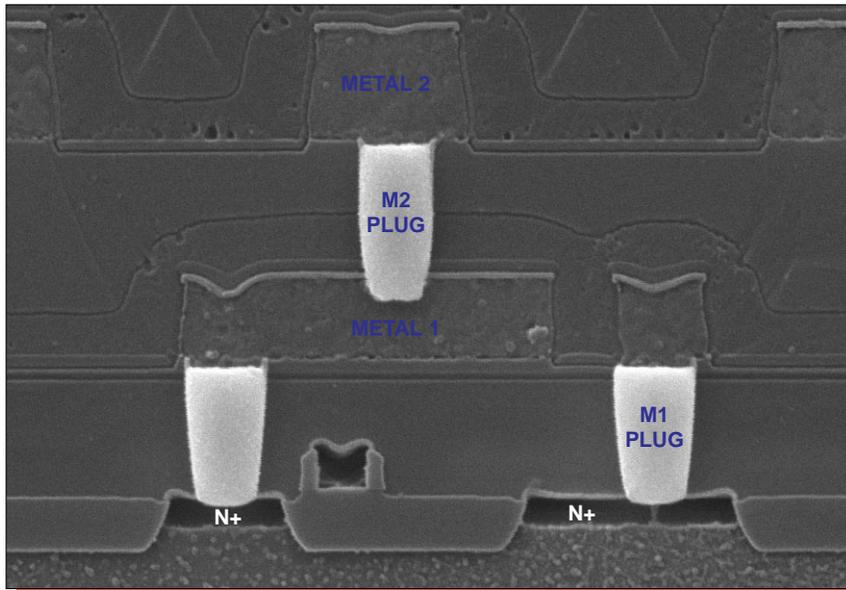


Mag. 35,000x

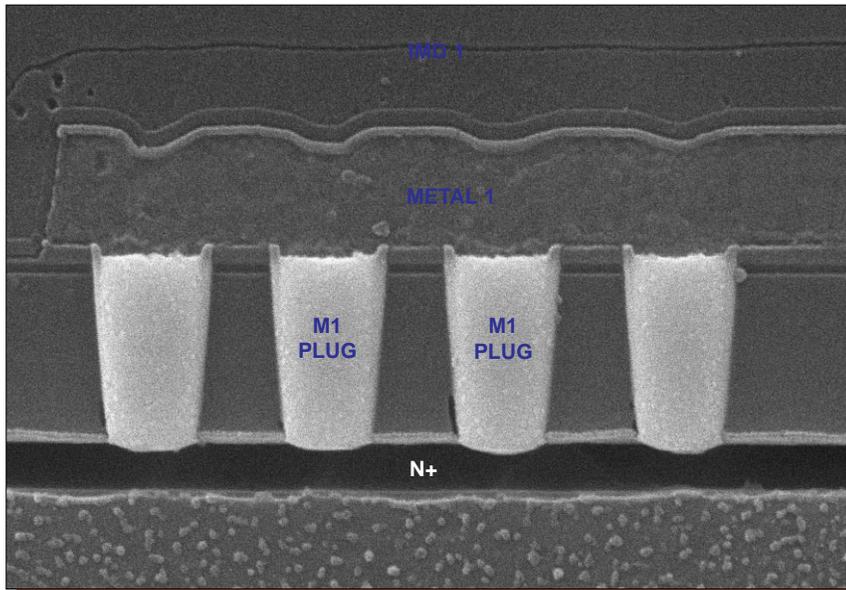


Mag. 35,000x

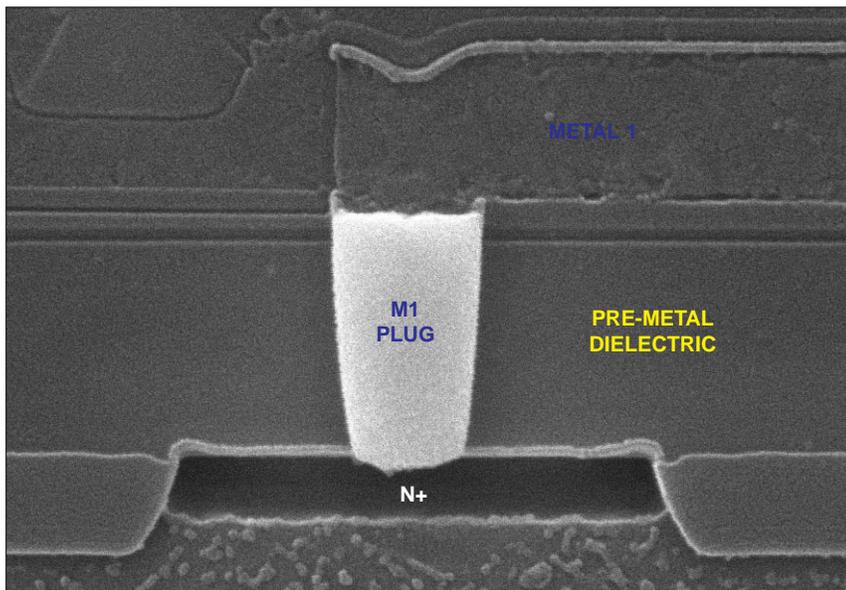
Figure 31. SEM section views of metal 1-to-polyicide contacts.



Mag. 20,000x

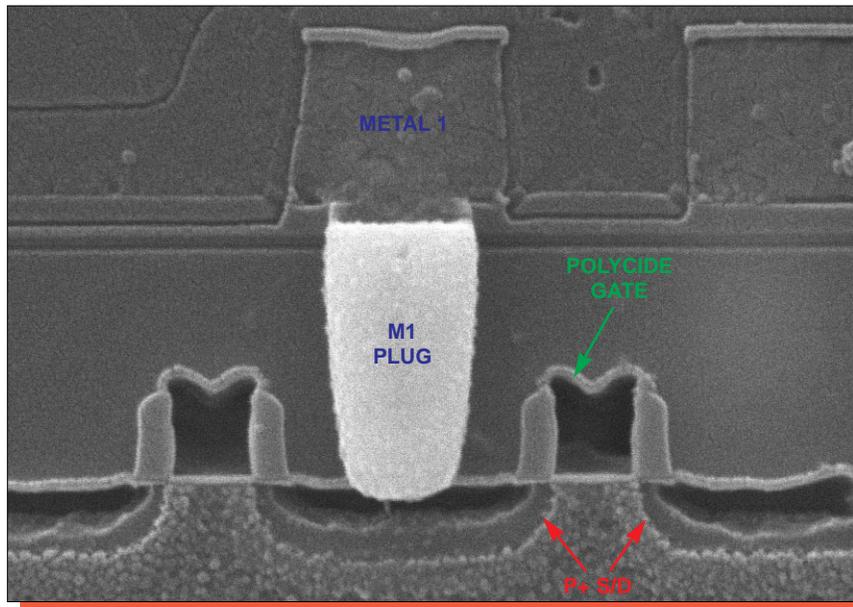


Mag. 26,000x

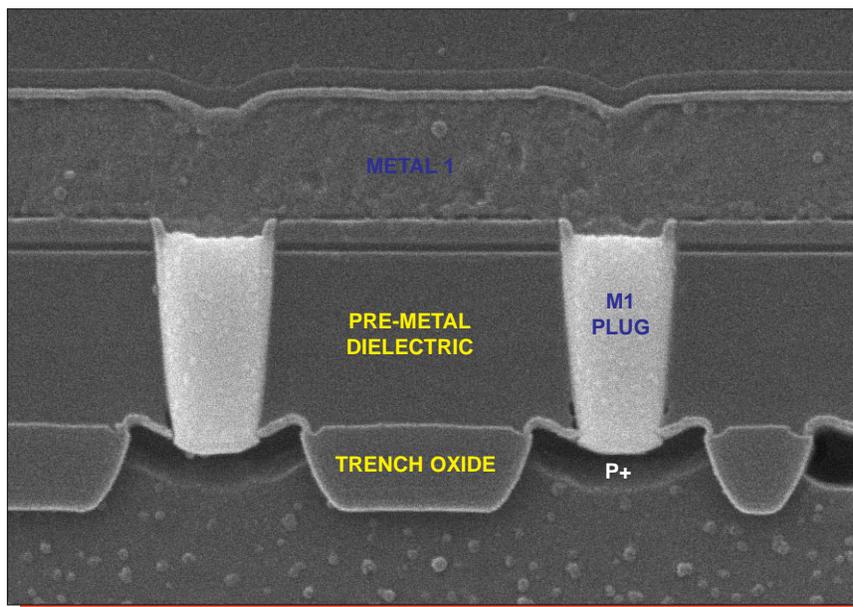


Mag. 35,000x

Figure 32. SEM section views of metal 1-to-N+ contacts.

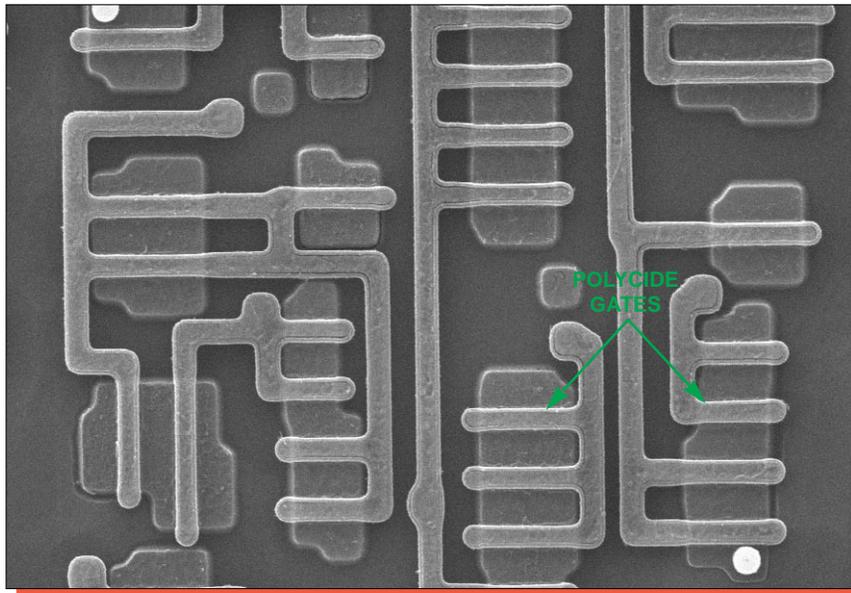


Mag. 40,000x

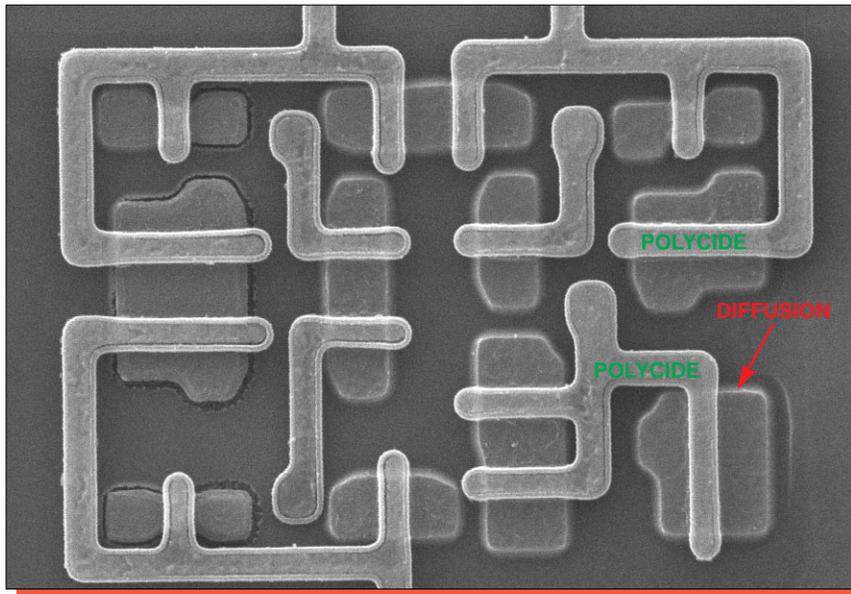


Mag. 30,000x

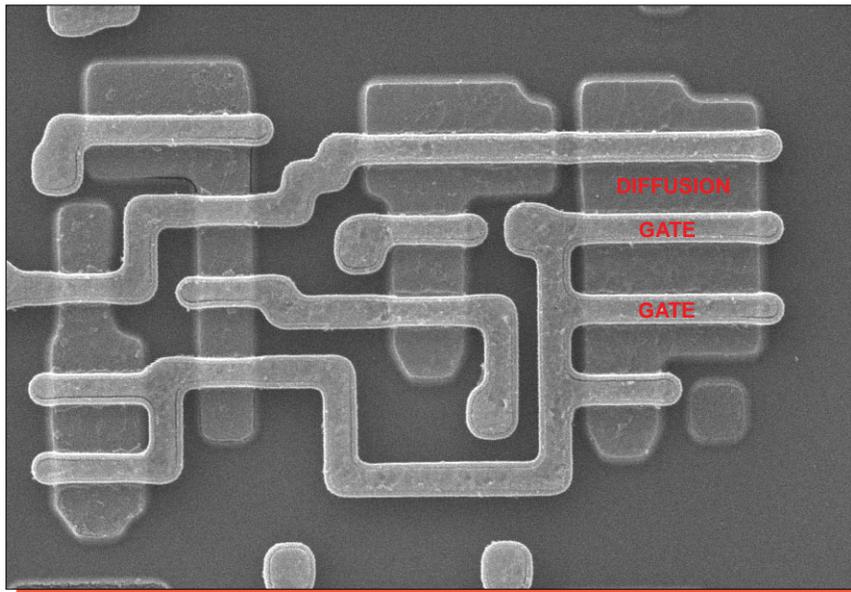
Figure 33. SEM section views of metal 1-to-P+ contacts.



Mag. 6000x

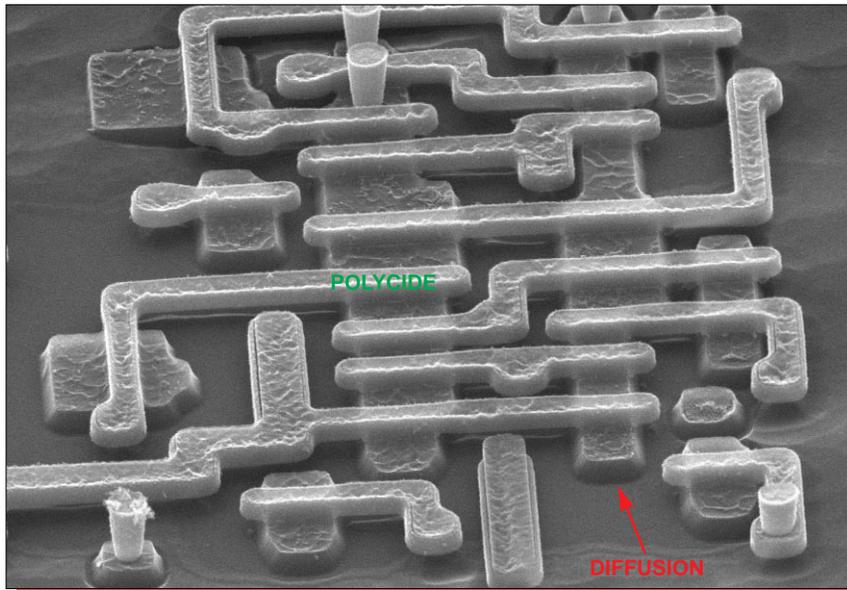


Mag. 8000x

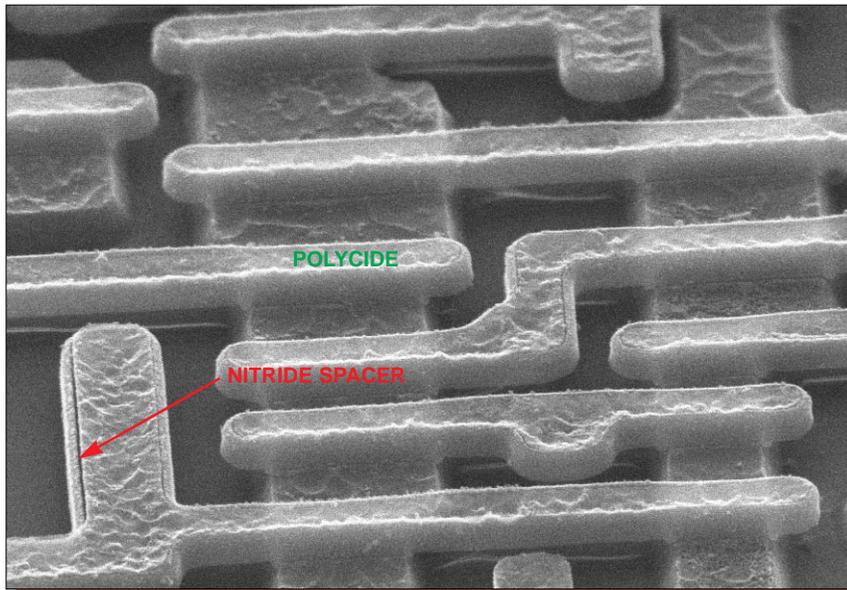


Mag. 8000x

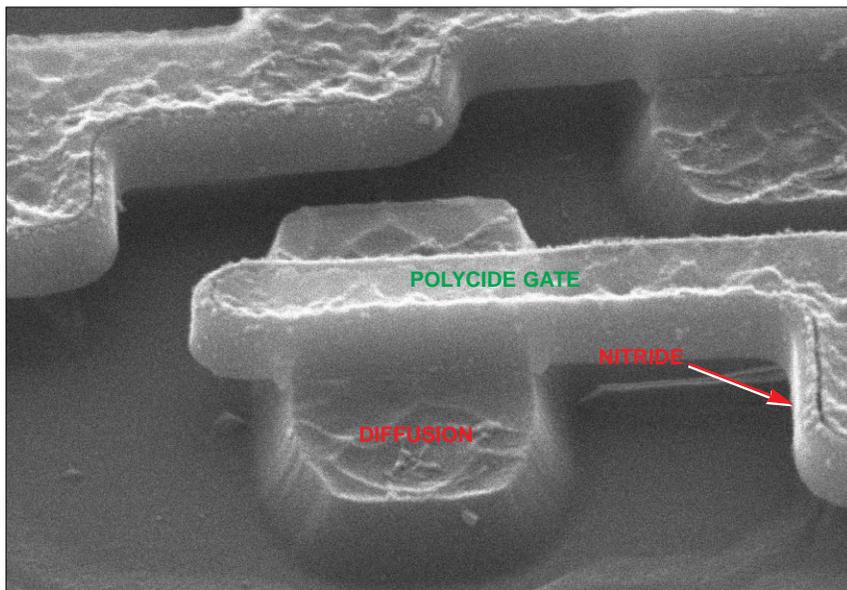
Figure 34. Topological SEM views of polycide gates. 0°.



Mag. 8000x

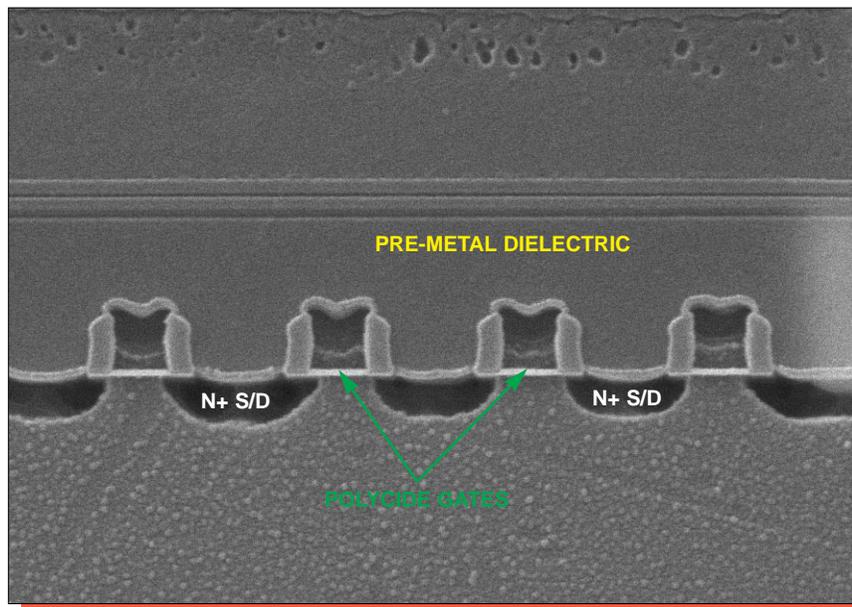


Mag. 15,000x

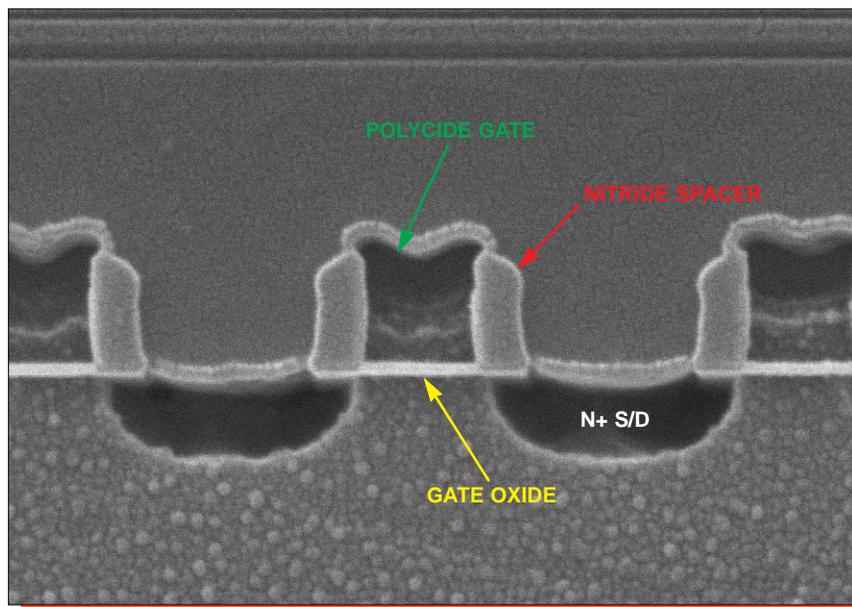


Mag. 30,000x

Figure 35. Perspective SEM views of polycide coverage. 55°.

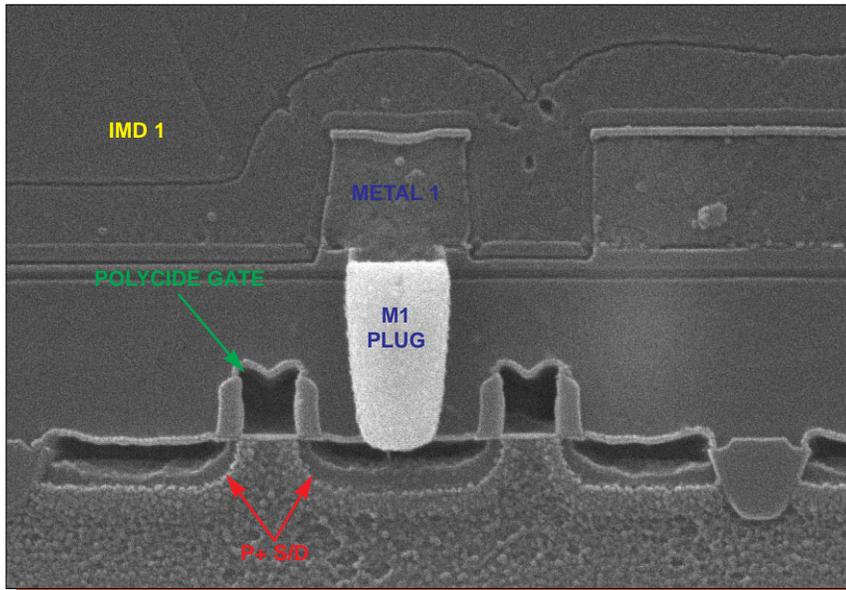


Mag. 26,000x

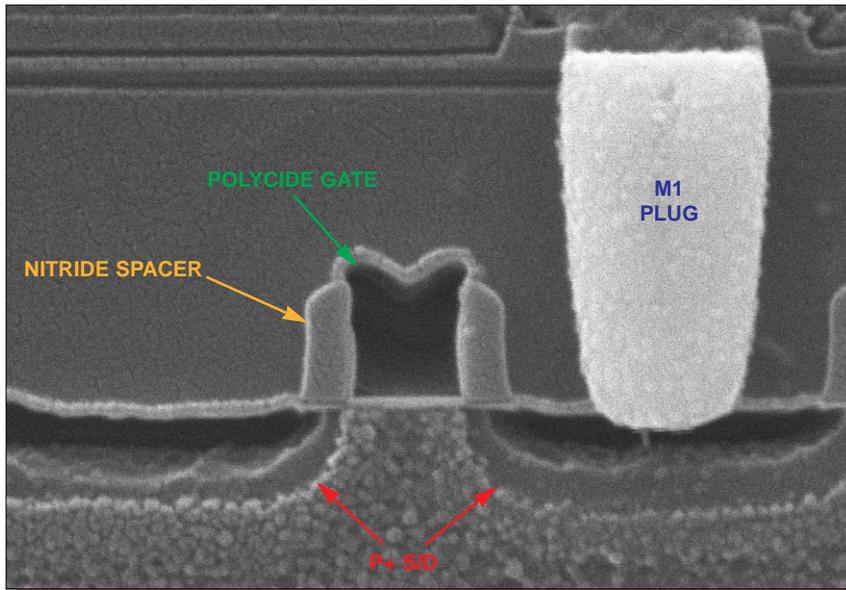


Mag. 52,000x

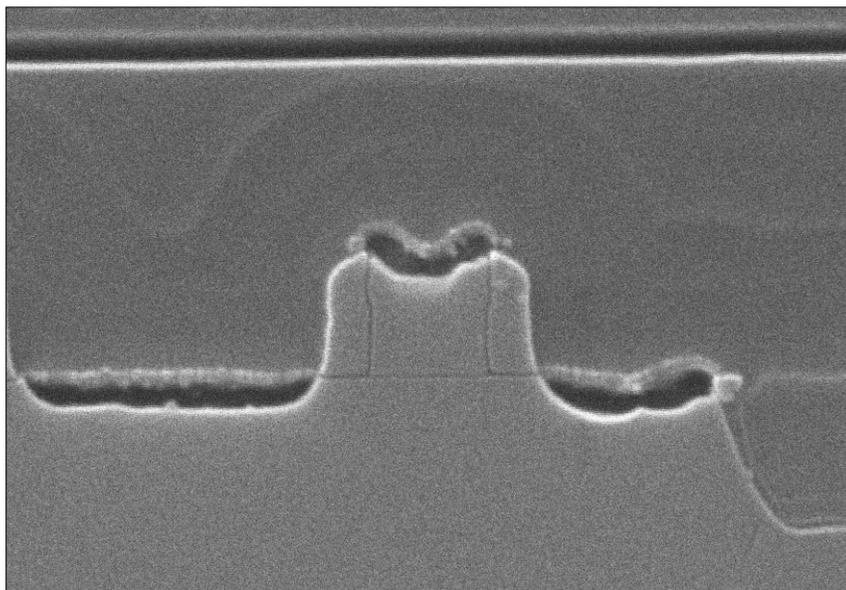
Figure 36. SEM section views of N-channel transistors.



Mag. 26,000x

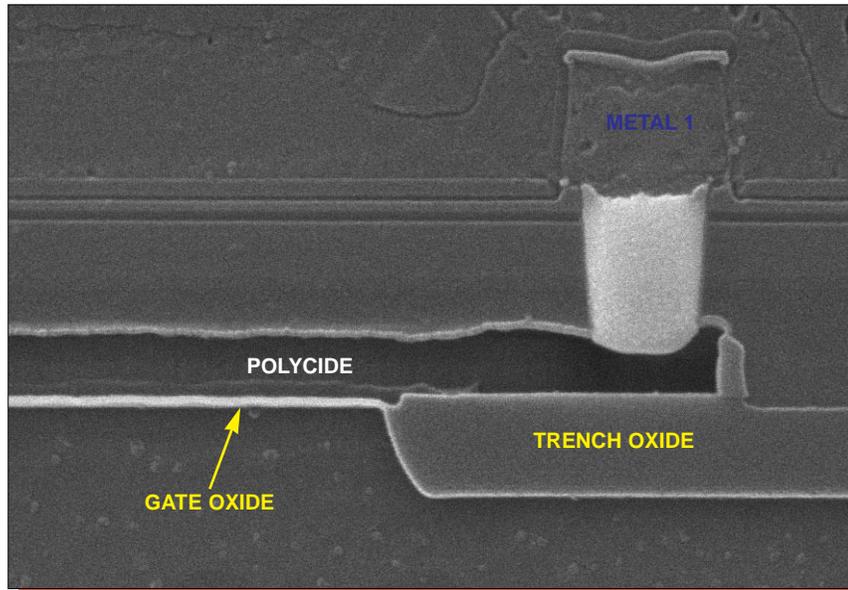


Mag. 52,000x

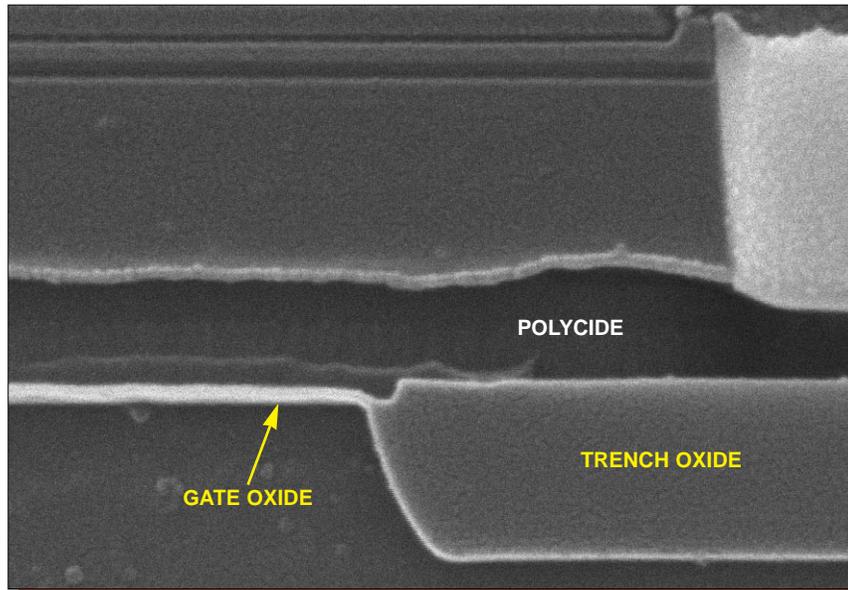


Mag. 52,000x

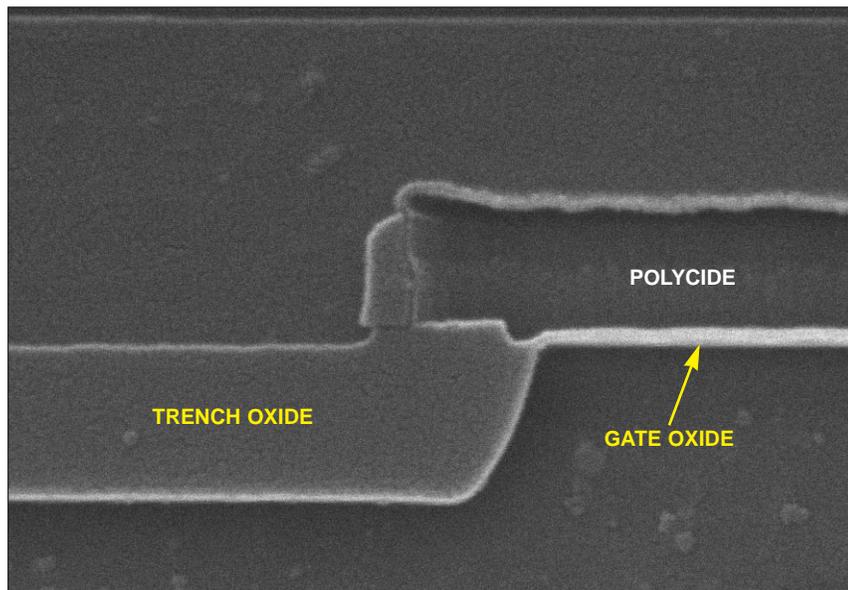
Figure 37. SEM section views of P-channel transistors.



Mag. 30,000x

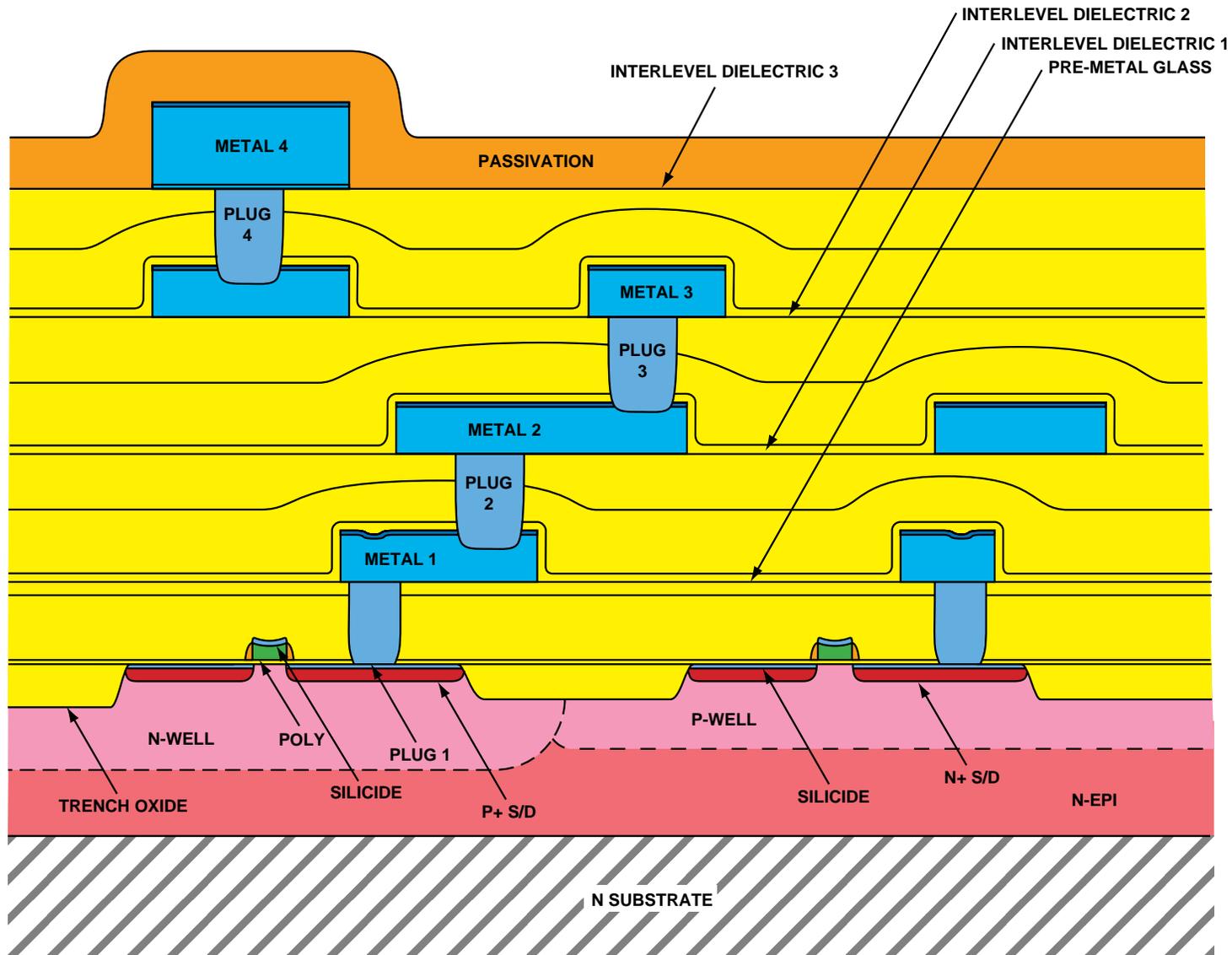


Mag. 52,000x



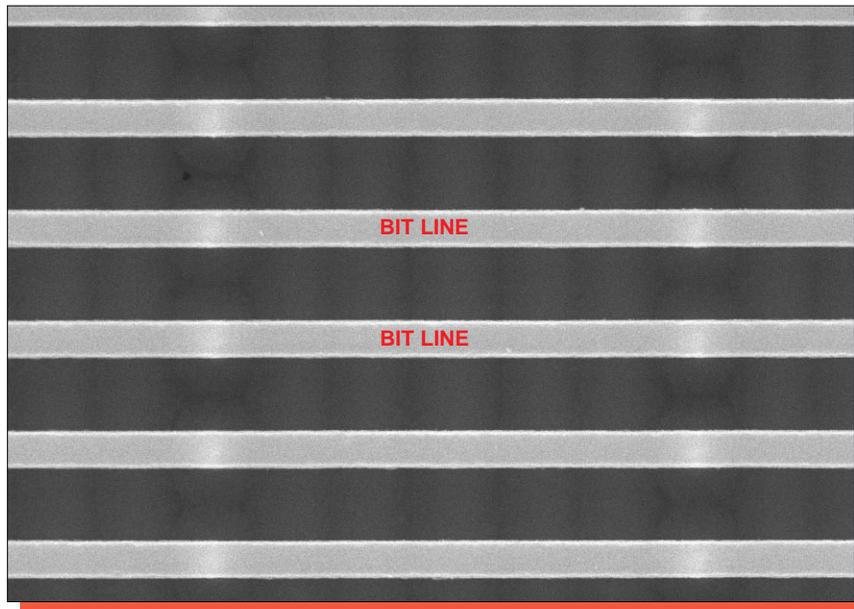
Mag. 52,000x

Figure 38. SEM section views of trench oxide isolation.

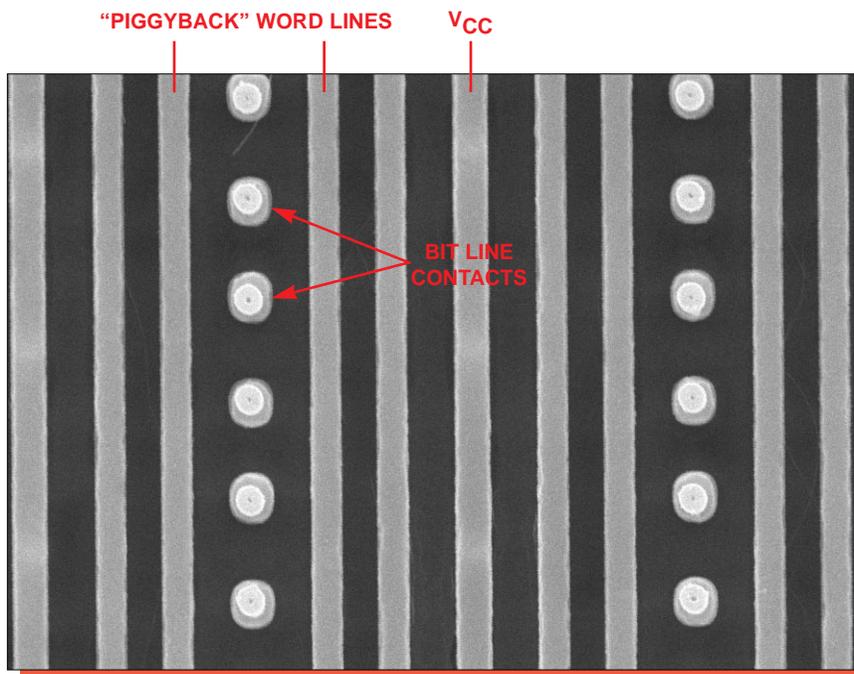


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

Figure 40. Color cross section drawing illustrating device structure.

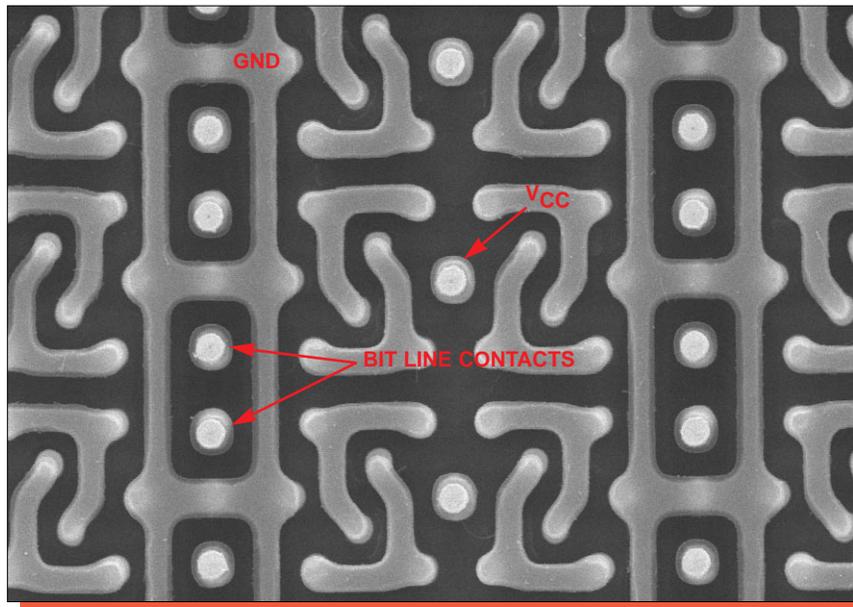


metal 3

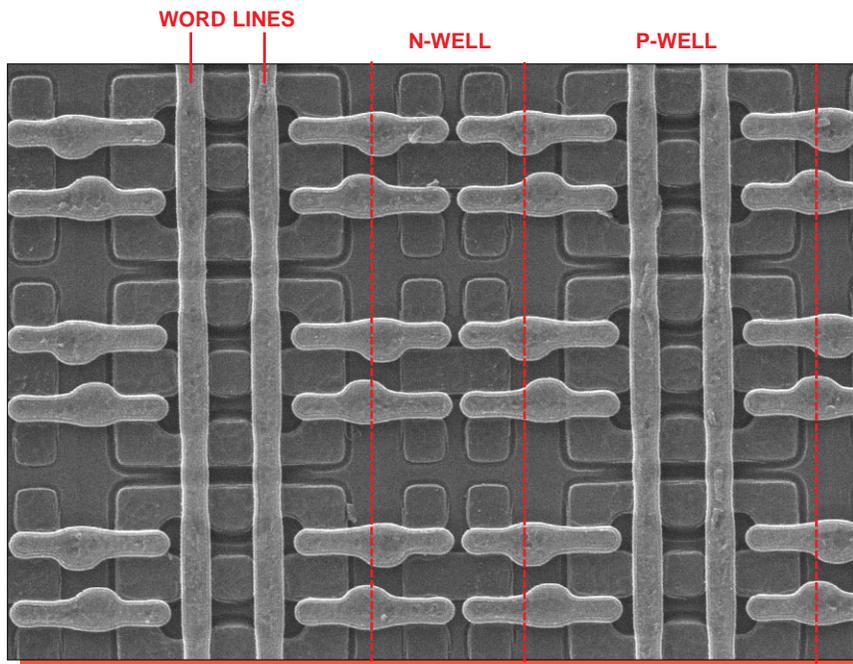


metal 2

Figure 41. Topological SEM views of the Cache SRAM array. Mag. 6500x, 0°.

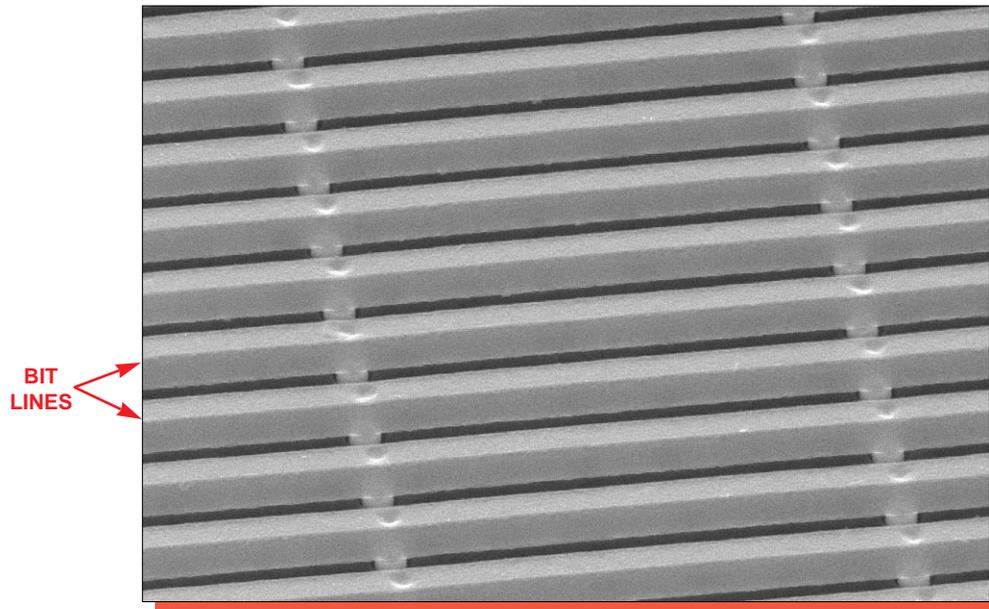


metal 1

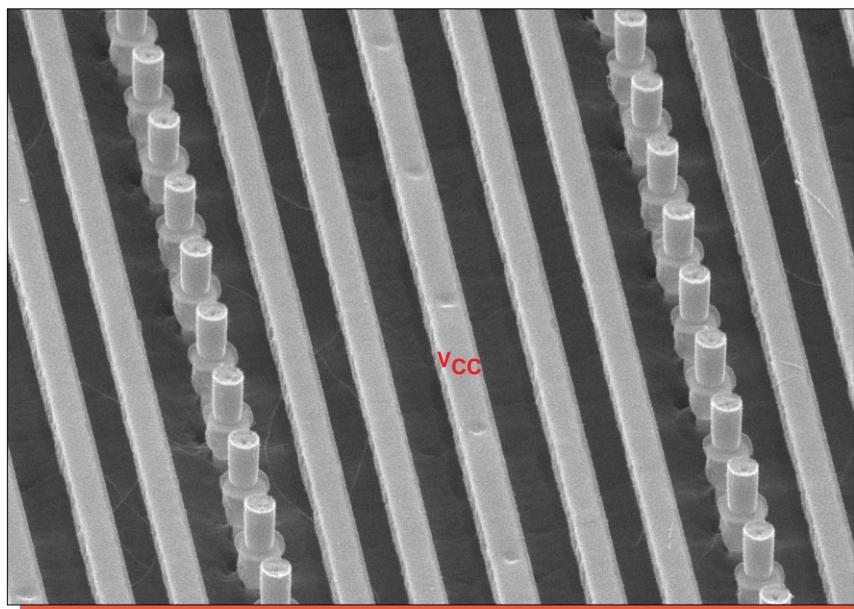


unlayered

Figure 41a. Topological SEM views of the Cache SRAM array. Mag. 6500x, 0°.

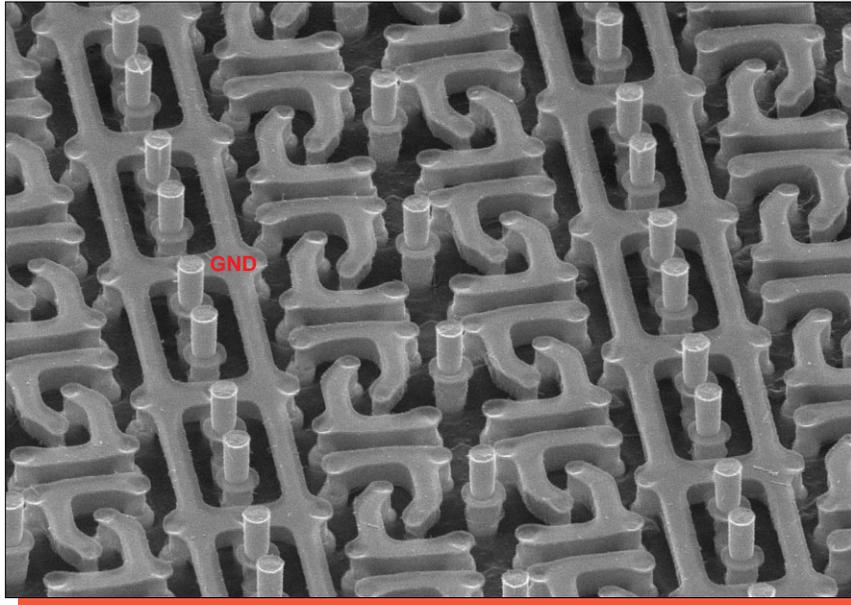


metal 3

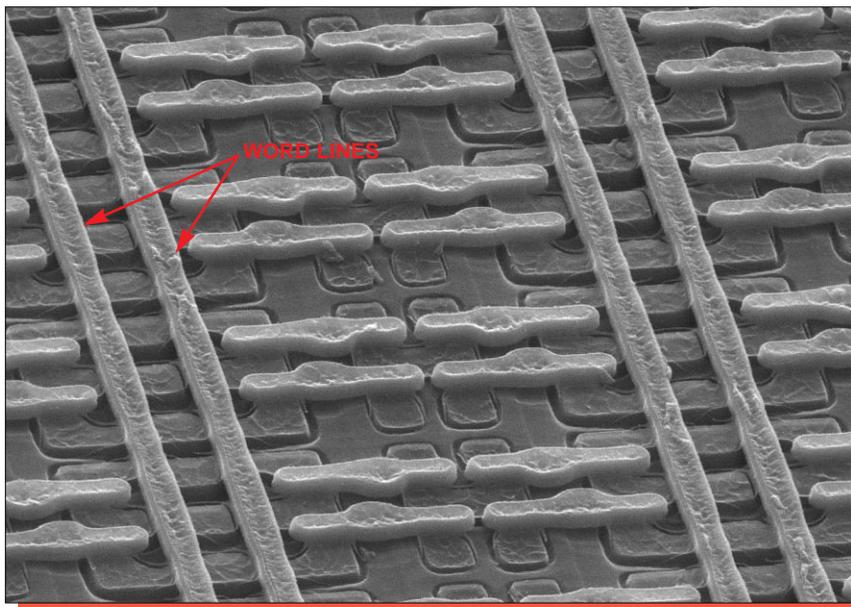


metal 2

Figure 42. Perspective SEM views of the Cache SRAM array. Mag. 7000x, 55°.

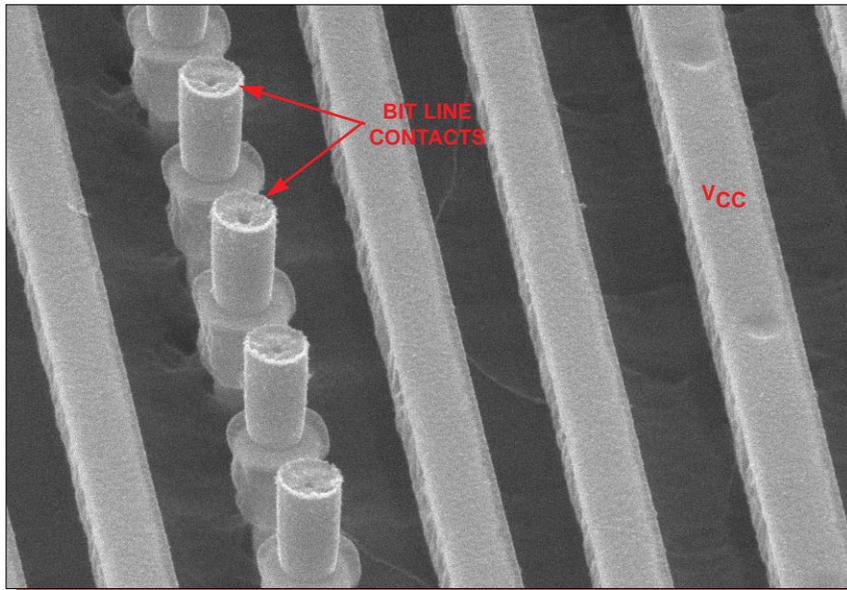


metal 1

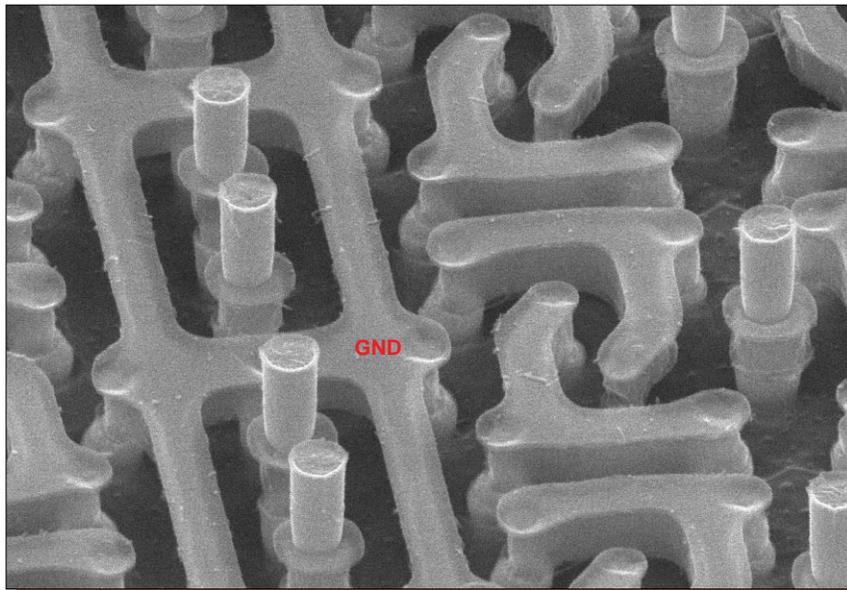


unlayered

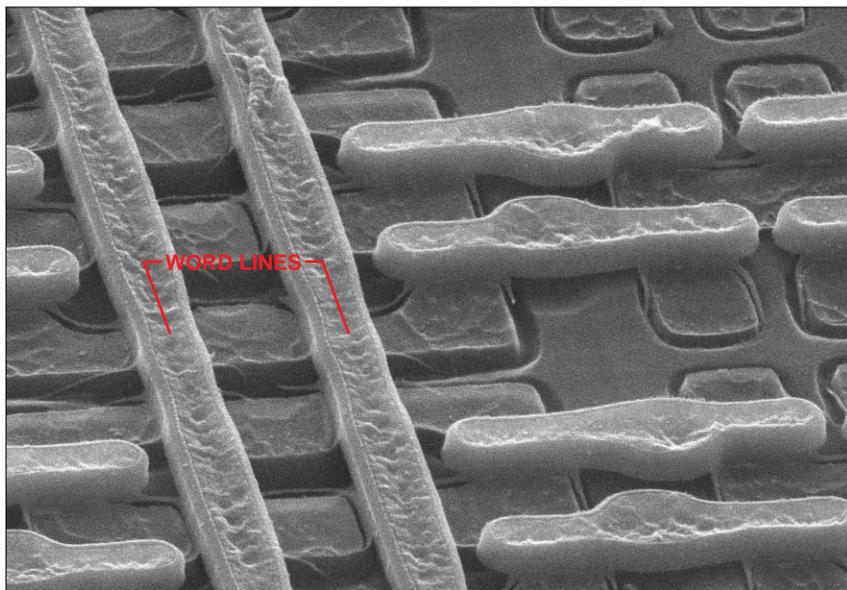
Figure 42a. Perspective SEM views of the Cache SRAM array. Mag. 7000x, 55°.



metal 2

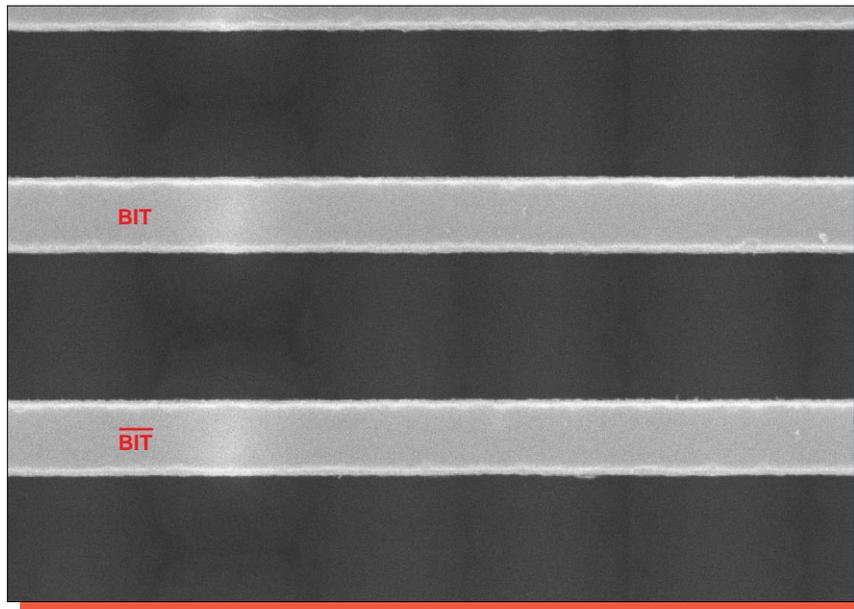


metal 1

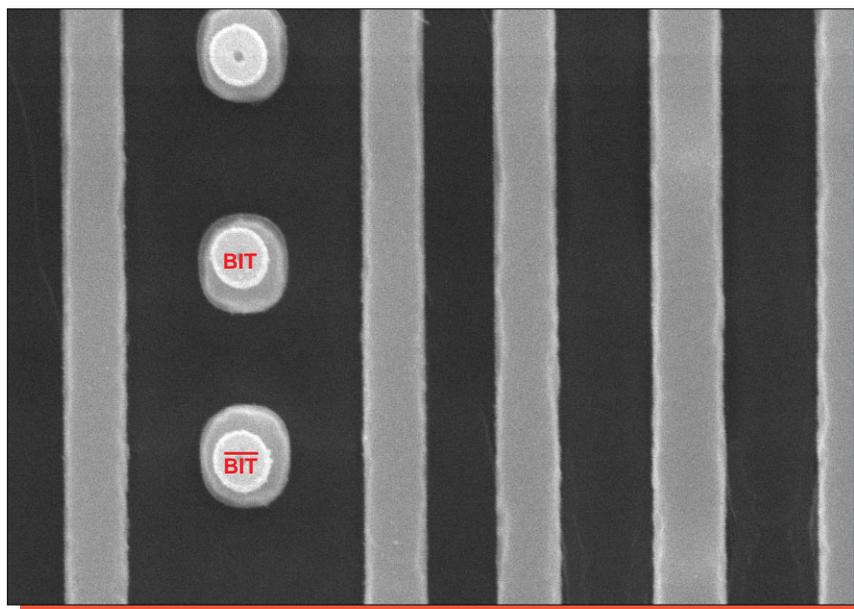


unlayered

Figure 43. Perspective SEM details of the Cache SRAM array. Mag. 15,000x, 55°.



metal 3



metal 2

Figure 44. Topological SEM views of a Cache SRAM cell. Mag. 13,000x, 0°.

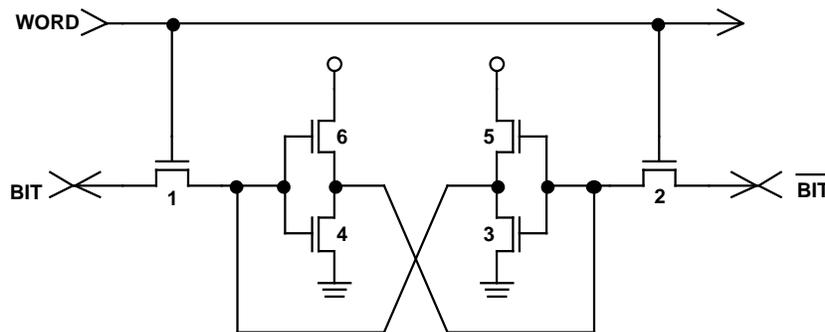
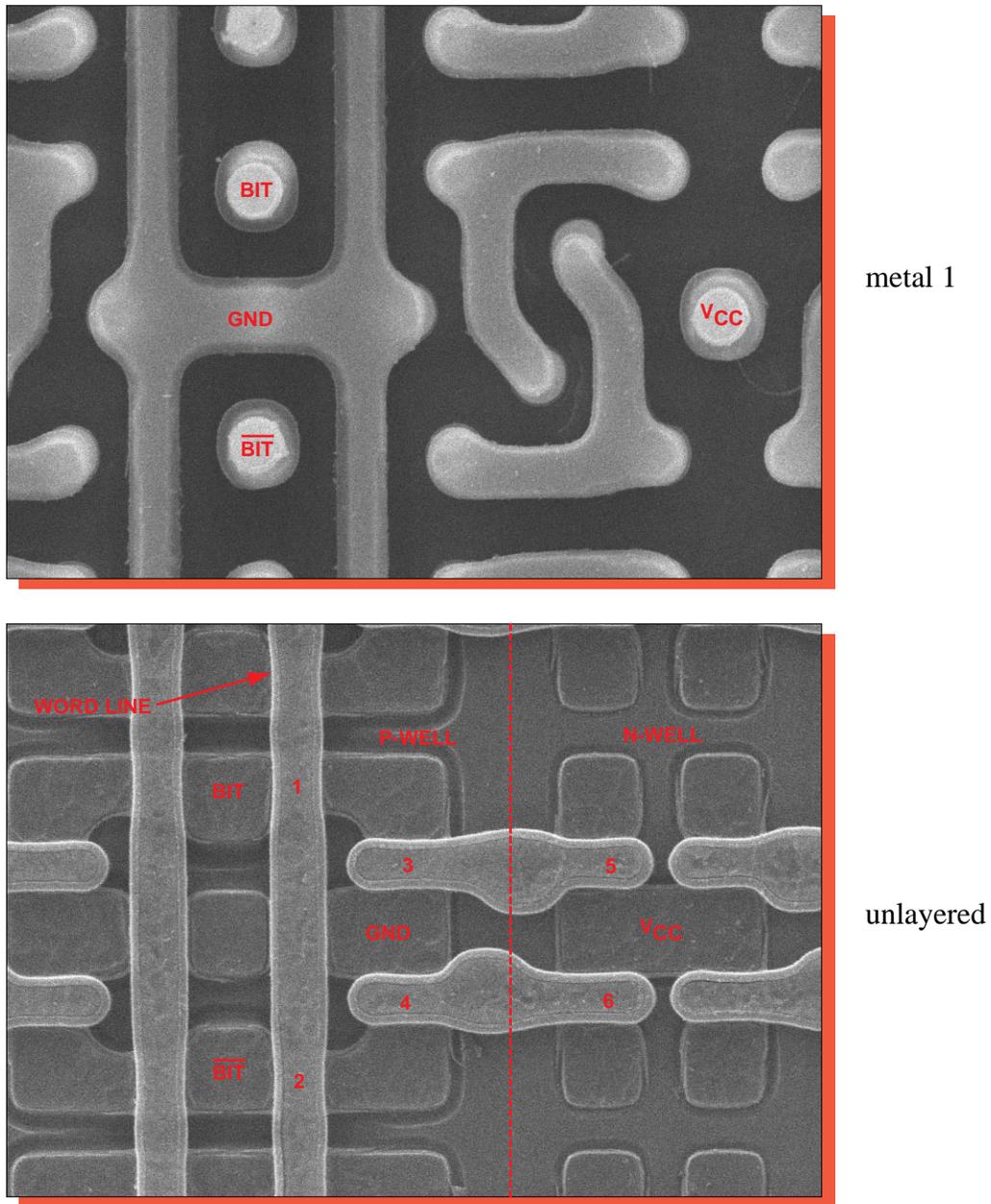


Figure 44a. Topological SEM views of a Cache SRAM cell with schematic.
Mag. 13,000x, 0°.