Construction Analysis

Micron Semiconductor MT4LC16M4H9 64Mbit DRAM

Report Number: SCA 9705-539

INTEGRATED CIRCUIT ENGINEERING

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INDEX TO TEXT

INTRODUCTION

This report describes a construction analysis of the Micron Technology MT4LC16M4H9 64Mbit DRAM engineering samples (ES). Two devices encapsulated in 32-pin Small Outline J-lead packages (SOJs) were supplied for the analysis. Both devices were date coded 9708.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 1 was very narrow and was not wide enough to cover plugs. This resulted in approximately 70 percent coverage at contact plugs and approximately 40 percent coverage[2] of plugs at metal line ends (see Figures 16 and 16a). Although improvements are desirable the coverage present is probably adequate.

Special Features:

- Textured poly 3 plates in the cell array for maximum capacitance per unit area.
- Very tall, slim tungsten contact plugs.
- Poly 2 plugs used as connecting links between the tungsten plugs at bit lines and under the poly 3 capacitor plates.
- Sub-micron geometries, 0.5 micron Metal 2, 0.3 micron Metal 1 (0.75 micron pitch), and 0.35 micron N-channel gates (0.25 micron wide).

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 32-pin plastic SOJs.
- Design of the leadframe was an LOCCB (Lead On Chip, Center Bonded). The leadframe was constructed of iron-nickel and spot-plated internally with silver.
- External lead tinning was by tin-lead solder.
- Wirebonding used the thermosonic ball bond method employing 1.2 mil O.D. gold wire.
- Pins 4 - 7 and 27 - 29 were not connected.
- Multiple leadframe fingers were employed at pins 6 and 27, both no-connects.
- Lead-locking provisions (anchors or holes) were not present at the pins, although the leadframe design provides some lead-locking structure at most pins. Pins 10 and 23 appear to be the major weak points.
- Sawn dicing was used.
- The die surface was attached to the bottom of the leadframe with an adhesive. No package paddle was employed.

Die Process

- Fabrication process: Selective oxidation CMOS process presumably employing twin-wells in a P substrate.
- Final passivation: A layer of nitride over a thick layer of silicon-dioxide over a separate thin layer of silicon-dioxide. The first layer appeared to have been subjected to an etchback. Evidence of an additional thin layer was present between the two layers of glass. It only remained in corner areas, having been mostly cleared during the back-etch.

TECHNOLOGY DESCRIPTION (continued)

- Metallization: Two layers of aluminum (no copper or silicon detected). Both metals employed a titanium-nitride cap. There was some slight evidence of a titanium barrier under both metals as well. Both metals were defined by dry-etch techniques. Standard vias were used under metal 2 and tungsten plugs were employed under metal 1.

- Intermetal dielectric: Two layers of silicon-dioxide. The first layer had been subjected to an etchback. Here also there was evidence of a thin layer between the two layers at the sidewalls of metal lines. It only remained at corners.

- Pre-metal dielectric: A very thick layer of glass over various densified oxides. This layer appeared to have been planarized by CMP.

- Polysilicon: Four layers of dry-etched polysilicon. Poly 4 (sheet) was used to form the common capacitor plate in the array. Poly 3 was textured and used exclusively for the individual cell capacitor plates in the array. Poly 2 was used for contact extension plugs in the array under bit line contacts and individual capacitor plates. Poly 1 (poly and tungsten-silicide) was used to form all gates on the die and word lines in the array.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. A process using oxide sidewall spacers was used at both N and P channel devices. Diffusions were not silicided.

- Wells: N-wells in a P substrate. No step was noted at the well boundaries.

- Memory cells: The memory cells consisted of a stacked capacitor DRAM cell design. Metal 1 was used for the bit lines. A poly 4 sheet formed the common plate of the capacitors and was tied to memory enable. Poly 3 was textured and formed the individual capacitor plates for each cell. The textured poly maximizes area and thus capacitance. Poly 1 formed the gates and word lines. Poly 2 was used as a contact link between the tungsten plugs and the diffusion at the bit line contacts and under the individual poly 3 plates as a link to the diffusion. It was also used at a few locations outside the memory (see Figure 20).

ANALYSIS RESULTS

Die Process and Design: **Figures 1 - 39**

Questionable Items:[1]

- Minimal metal interconnect coverage at many contact plugs.

Special Features:

- Textured poly 3 plates in the array to maximize capacitance.
- Tall and slim tungsten contact plugs in some cases on top of poly 2 plugs.
- Sub-micron geometries, 0.5 micron Metal 2, 0.3 micron Metal 1, and 0.35 micron N-channel gates.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate.
- Design and layout: Die layout was clean and efficient. Alignment was good at all levels.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.
- Final passivation: A layer of nitride over a thick layer of silicon-dioxide on a separate thin layer of silicon-dioxide. Integrity tests indicated defect-free passivation. Edge seal was good.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS (continued)

- Metallization: Two levels of metallization. Both metals consisted of aluminum with a titanium-nitride cap. There was some evidence of a titanium barrier under both metals as well. Standard vias were employed under metal 2 and tungsten plugs were used under metal 1 for contacts.

- Metal patterning: Both metals were defined by a dry etch of good quality. Metal line widths were sub-micron (0.5 micron Metal 2, 0.3 micron Metal 1). The lines were not widened at contacts (plugs) which resulted in only 70 percent coverage of the contacts and approximately 40 percent coverage at metal line ends on plugs (see Figures 16 and 16a). Manufacturer's design specifications should be verified.

- Metal defects: None. No voiding or notching of the metal layers was found. No silicon nodules were found following removal of the aluminum.

- Metal step coverage: Metal 2 aluminum thinned up to 75 percent at vias. For reference MIL-STD-883D allows up to 70 percent thinning at contacts of this size. Virtually no metal 1 thinning was present. This is due to the CMP planarization of the glass and the tungsten plugs.

- Vias and Contacts: Via and contact cuts were defined by a dry-etch. Some over-etching was present but it was not serious. Tungsten plugs were very tall and narrow. Some voiding was noted in the center of the plugs, but should not be a reliability concern. As mentioned poly 2 plugs were used under the tungsten plugs at bit contacts and at a few contacts in the decode. No problems were found.

- Intermetal dielectric: Two layers of silicon-dioxide. The first layer had been subjected to an etchback. There was evidence of a sacrificial layer between the two layers at the sidewalls of metal lines. No problems were found.

- Premetal dielectric: A very thick layer of glass over various densified oxides. This layer was planarized by CMP. No problems were found.

ANALYSIS RESULTS (continued)

- Polysilicon: Four levels of polysilicon were used. Poly 1 (poly 1 and tungsten silicide) formed all gates on the die and the word lines in the array. Poly 2 was used for contact extension plugs in the array under bit line contacts and individual capacitor plates. Poly 2 plugs were also used in the decode areas, but not in the periphery. Poly 3 was textured and formed the active individual plates of the capacitors in the cell array. A poly 4 sheet formed the common passive plate. Definition was by a dry etch of good quality.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeak or elsewhere.

- Diffusions: Standard implanted N+ and P+ diffusions were used for sources and drains. No problems were found. The process employed oxide sidewall spacers.

- Wells: Twin-wells were probably used (we could not delineate the P-wells). No step was present. Definition of the N-wells was normal.

- Epi: No epi layer was employed. No defects were found in the substrate silicon.

- Buried contacts: Direct poly-to-diffusion (buried) contacts were only used between the poly 2 contact links and diffusion in the array and decode.

- Fuses: No redundancy fuses were found.

- Memory cells: The memory cells employed a stacked capacitor DRAM cell design. Metal 1 was used for the bit lines. As mentioned above, a poly 4 sheet formed the common plate of the capacitors and was tied to memory enable. Poly 3 formed the individual cell plates. The poly 3 was textured to maximize capacitance. A thin capacitor dielectric was used between the poly 4 and poly 3. The dielectric was not positively identified but is assumed to be oxide-nitride. The poly 2 was used as a contact link between the tungsten plugs and the diffusion at bit line contacts and under the individual poly 3 plates as an extension down to the diffusion. Poly 1 formed the word lines and select gates. Cell size was 0.65 x 1.2 microns

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

Passivation integrity test

Wirepull test

Passivation removal

SEM inspection of metal 2

Metal 2 removal and inspect vias

Delayer to metal 1 and inspect

Metal 1 removal and inspect plugs

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	N
Package markings	G
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	G
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die attach method	Adhesive
Dicing method:	Sawn
Die surface integrity:	
Tool marks (absence):	G
Particles (absence):	G
Contamination (absence):	G
Process defects (absence):	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	N
Contact coverage	NP
Contact registration	N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP	BOTTOM
9708 C USA MT 4LC16M4H9 DJ -6 ES	HDFY

WIREBOND STRENGTH

Wire material: 1.2 mil diameter gold

Die pad material: aluminum

Material at package post: silver

Sample #

# of wires tested:	8
Bond lifts:	0
Force to break - high:	11g
- low:	9.5g
- avg.:	9.8g
- std. dev.:	0.5

DIE MATERIAL ANALYSIS

Passivation:	Silicon-nitride over two layers of silicon-dioxide.
Metal 2:	Aluminum with a titanium cap. Some evidence of a titanium barrier.
Interlevel dielectric:	Two layers of silicon-dioxide.
Metal 1:	Aluminum with a titanium cap. Some evidence of a titanium barrier.
Plugs:	Tungsten.
Pre-metal glass:	A thick layer of glass over densified oxides.
Poly 1:	Tungsten silicide.

HORIZONTAL DIMENSIONS

Die size:	8 x 15.3 mm (316 x 602 mils)
Die area:	122.7 mm^2 (190,232 $mils^2$)
Min pad size:	0.12 x 0.12 mm (4.7 x 4.7 mils)
Min pad window:	0.1 x 0.1 mm (4.1 x 4.1 mils)
Min pad space:	0.06 mm (2.3 mils)
Min metal 2 width:	0.5 micron
Min metal 2 space:	0.8 micron
Min metal 2 pitch:	1.3 micron
Min metal 1 width:	0.3 micron
Min metal 1 space:	0.4 micron
Min metal 1 pitch:	0.7 micron
Min via:	0.9 micron (round)
Min contact:	0.45 micron (round)
Min poly 3 space:	0.3 micron
Min poly 1 width:	0.25 micron
Min poly 1 space:	0.4 micron
Min gate length* - (N-channel):	0.35 micron
- (P-channel):	0.45 micron
Min gate width:	0.25 micron (Fig. 25).
Cell size:	0.8 $micron^2$
Cell pitch:	0.65 x 1.2 microns

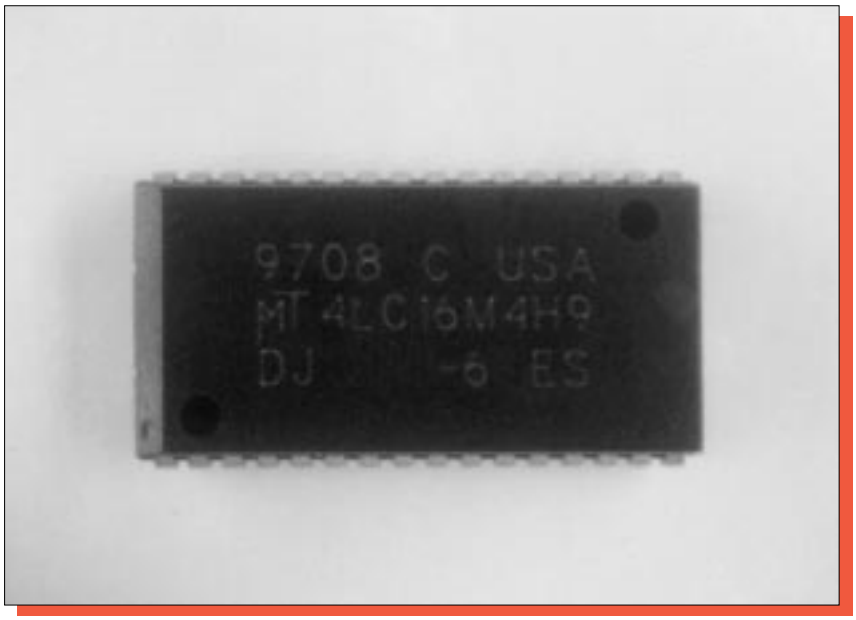
**Physical gate length*

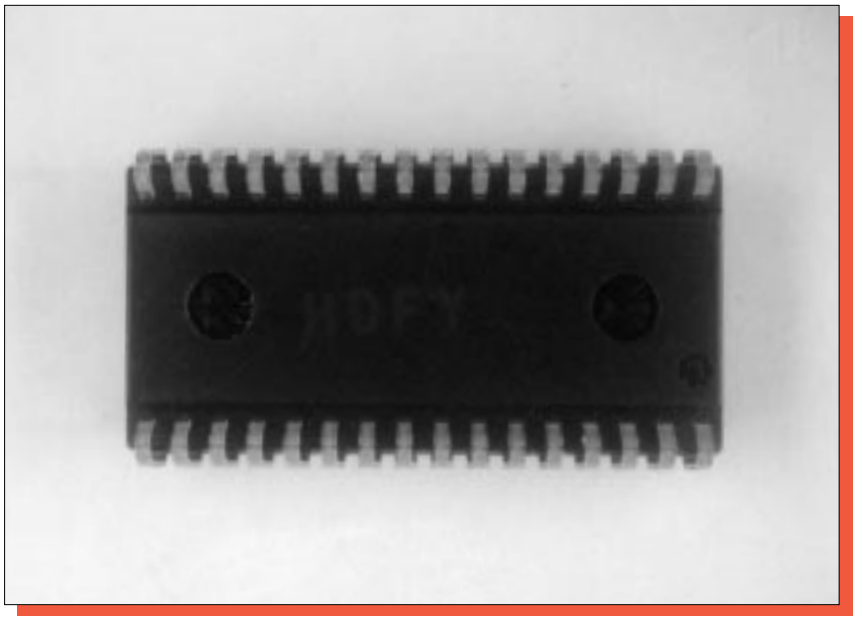
VERTICAL DIMENSIONS

Layers

Passivation 3:	0.5 micron
Passivation 2:	0.65 micron
Passivation 1:	0.15 micron
Metallization 2 - cap:	0.03 micron (approx.)
- aluminum:	0.8 micron
Interlevel dielectric - glass 2:	0.3 - 0.9 micron
- glass 1:	0.15 micron
Metallization 1 - cap:	0.05 micron (approx.)
- aluminum:	0.4 micron
Contact plugs:	1.5 - 2 microns
Pre-metal glass:	1.8 micron
Poly 4:	0.05 micron
Poly 3:	0.05 micron
Poly 2:	0.65 micron
Densified oxide (over poly 1):	0.25 micron
Poly 1 - silicide:	0.1 micron
- poly:	0.15 micron
Local oxide:	0.25 micron
N+ diffusion:	0.2 micron
P+ diffusion:	0.2 micron
N-well:	4.5 microns (approx.)
P-well:	Could not delineate.

INDEX TO FIGURES





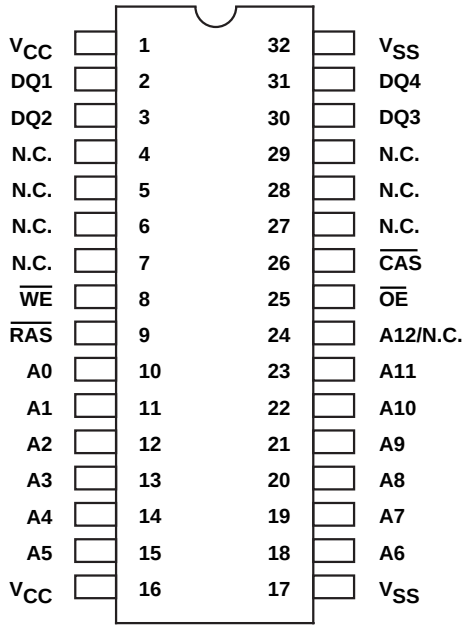


Figure 1. Package photographs and pinout diagram of the Micron MT4LC16M4H9. Mag. 4x.

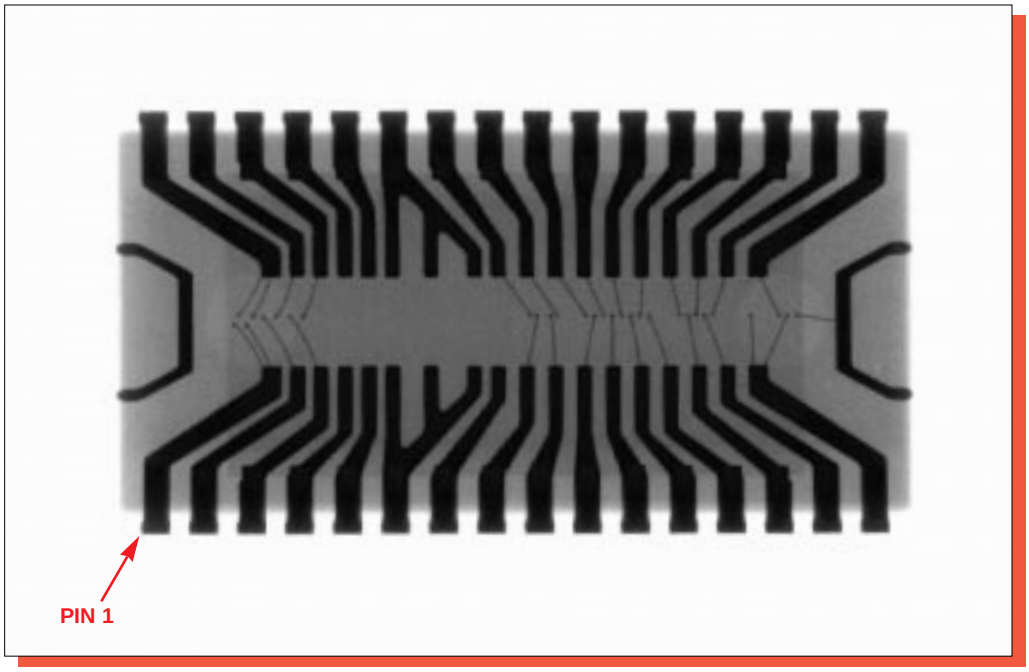


Figure 2. Topological and side x-ray views of the package. Mag. 5x.

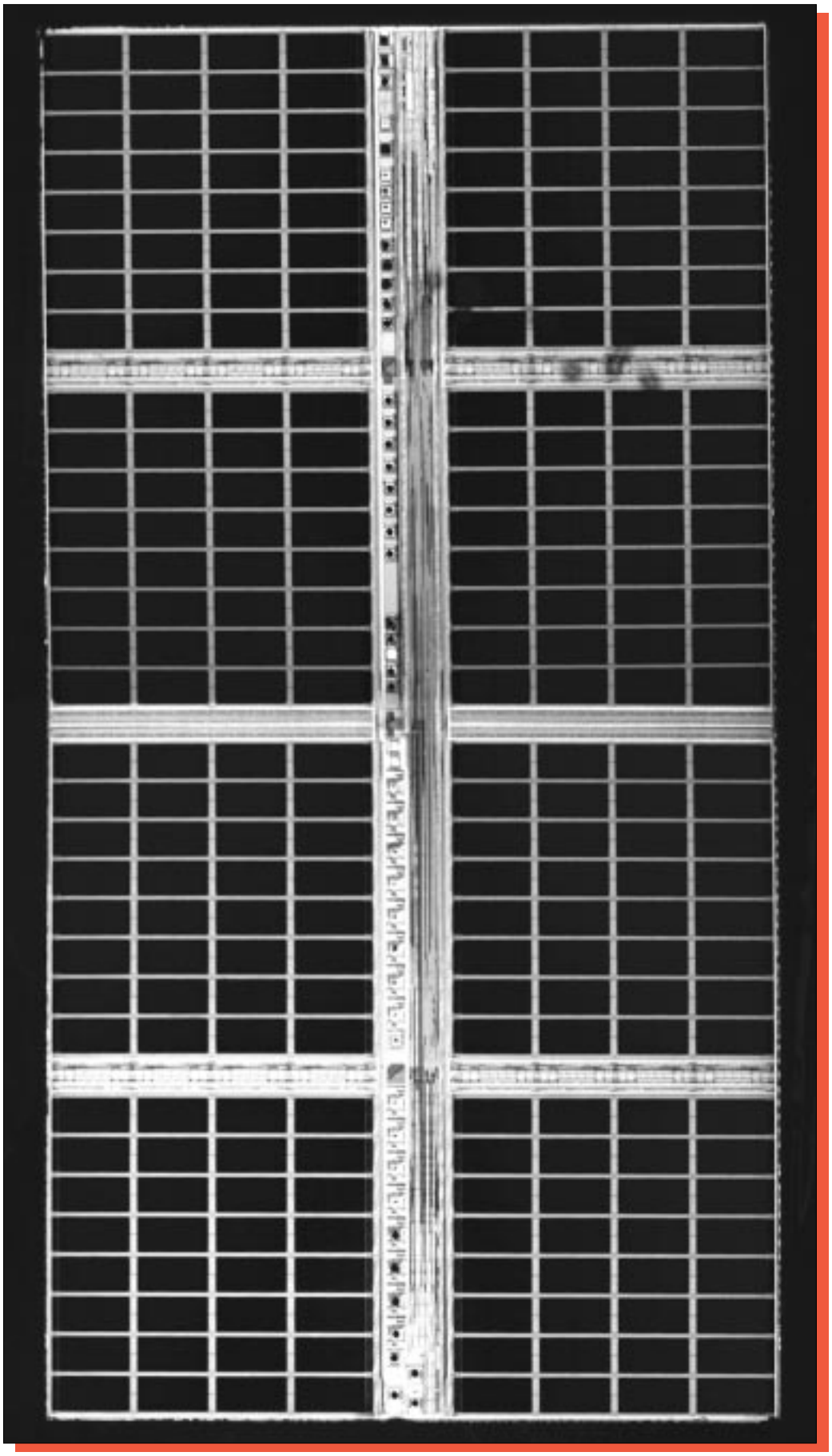


Figure 3. Whole die photograph of the Micron MT4LC16M4H9. Mag. 15x.

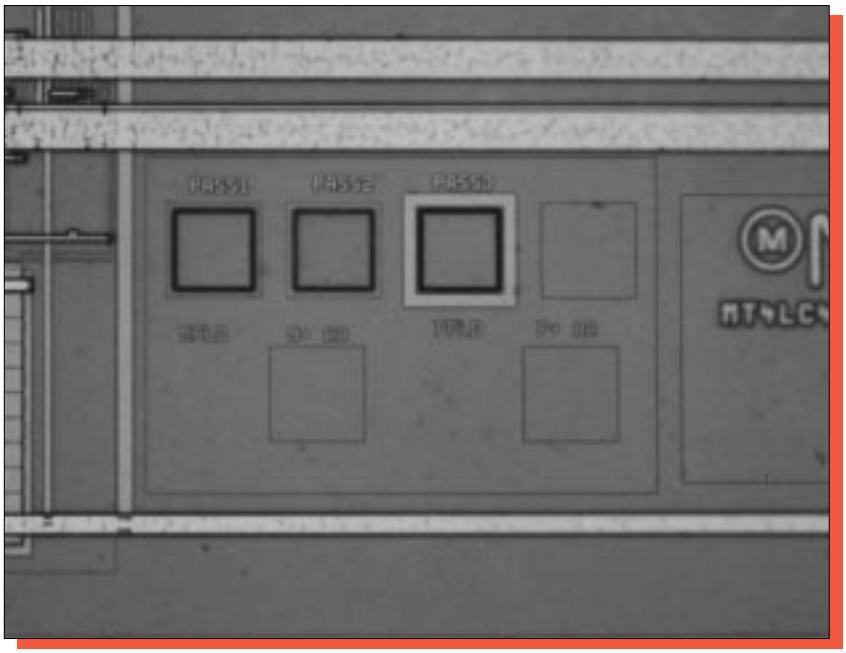
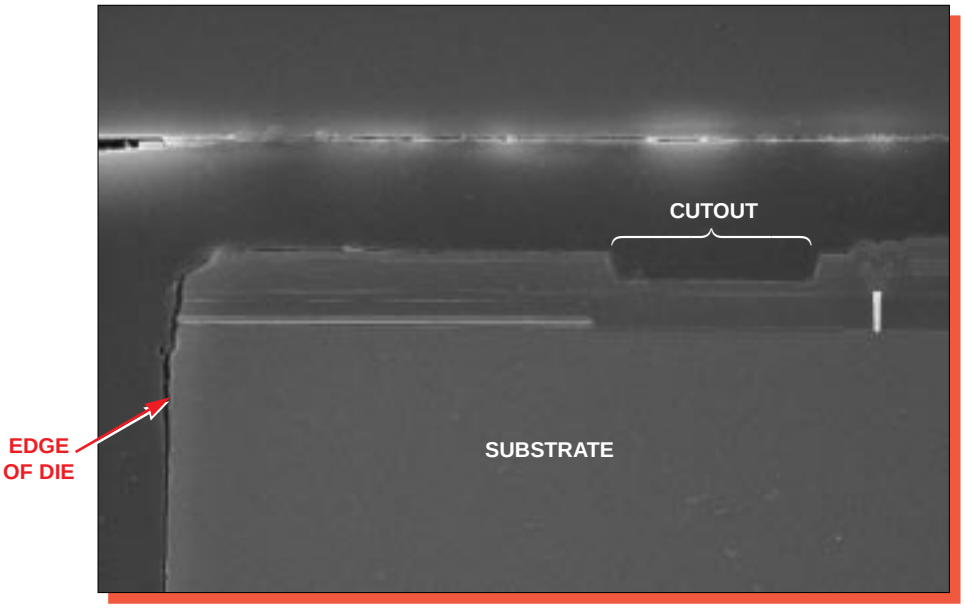
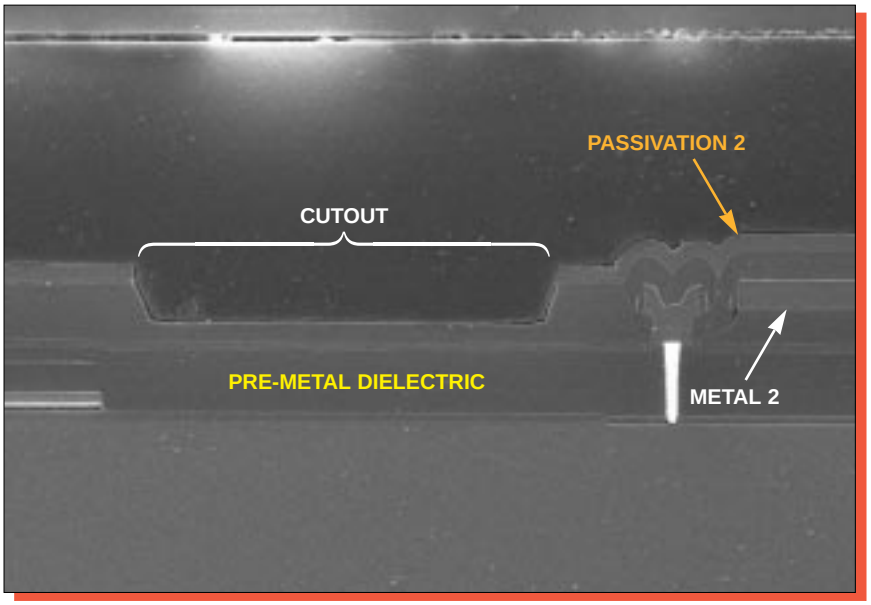


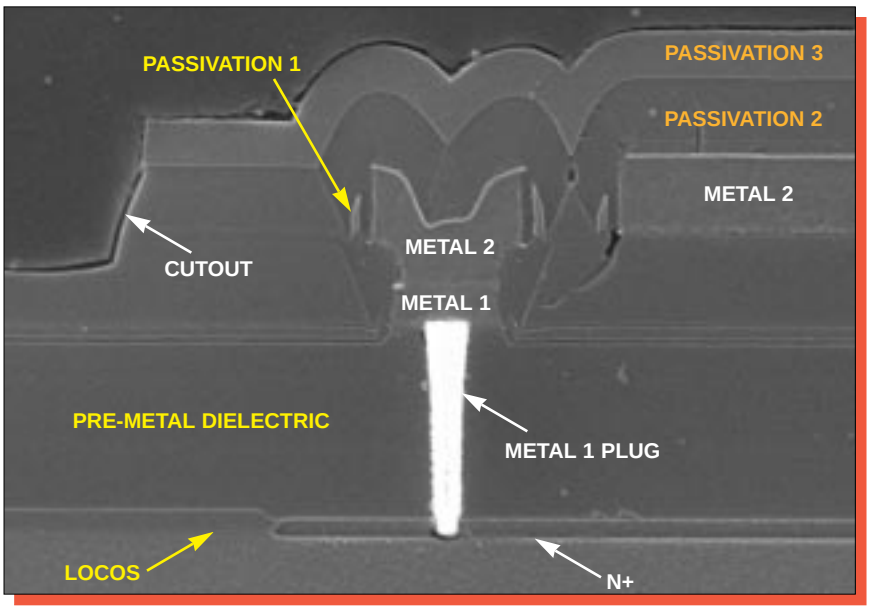
Figure 4. Optical views of die markings. Mag. 400x.



Mag. 2400x

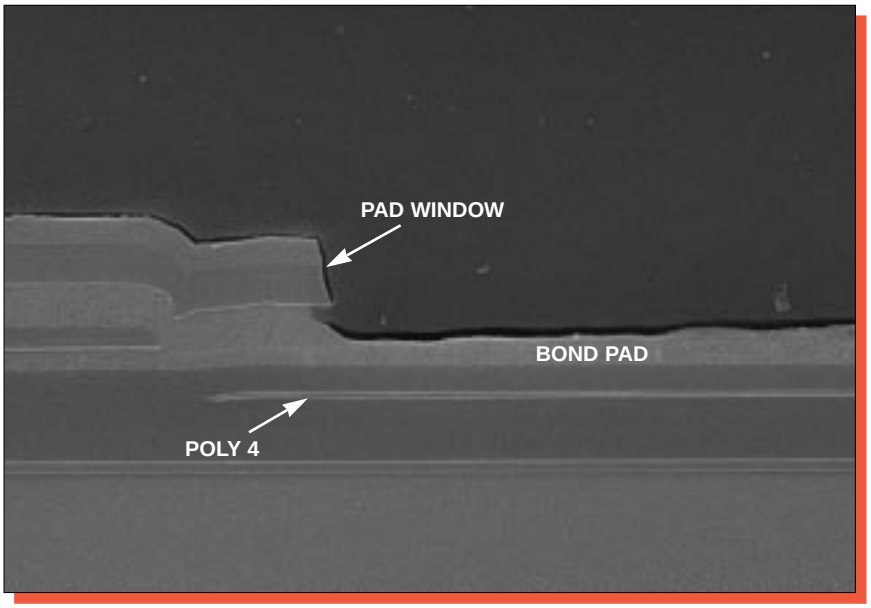


Mag. 4800x



Mag. 13,000x

Figure 5. SEM section views of the edge seal structure.



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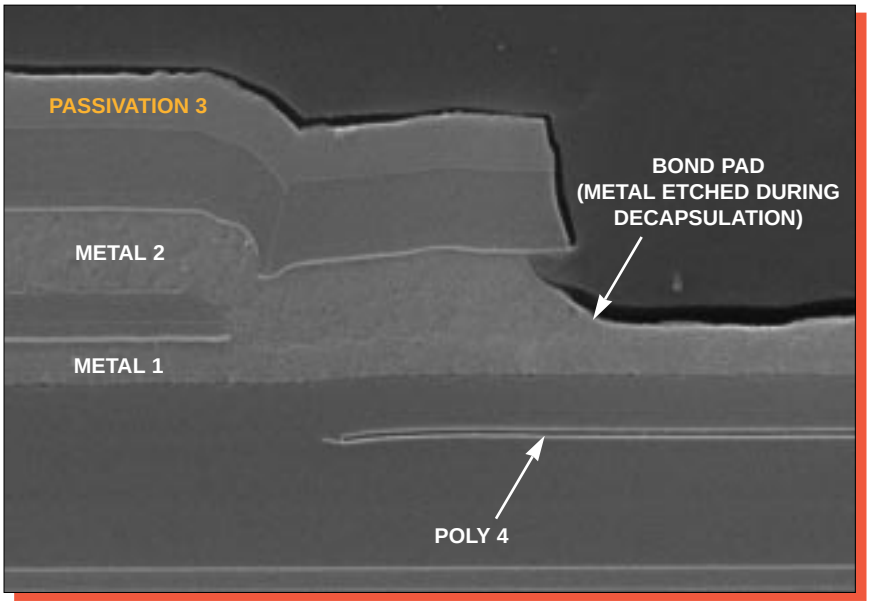

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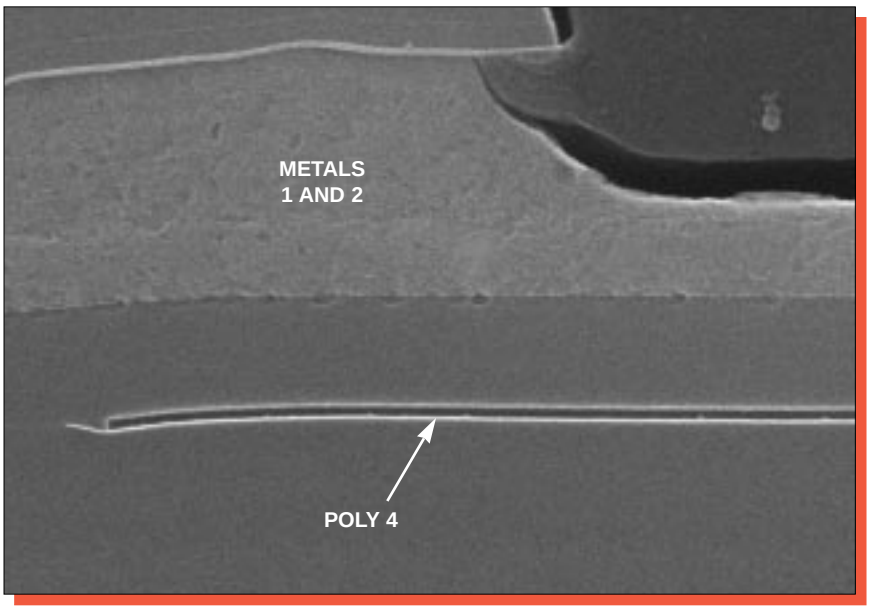


Mag. 26,000x

Figure 6. SEM section views of the bond pad structure.

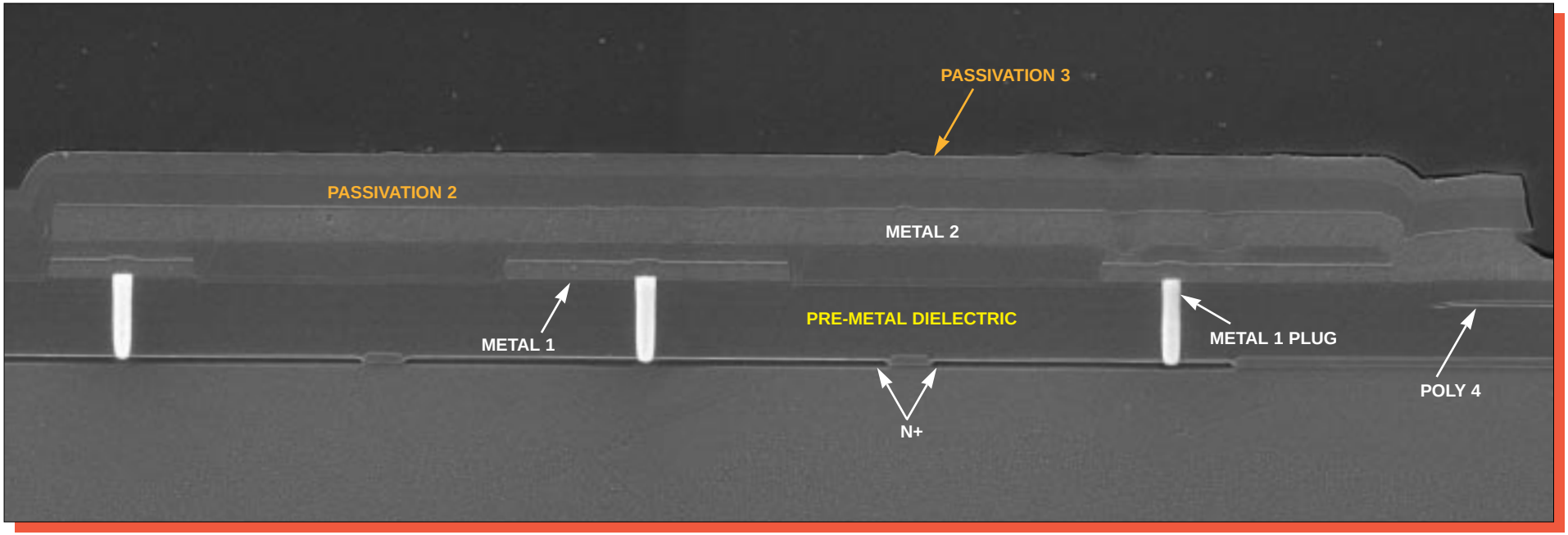
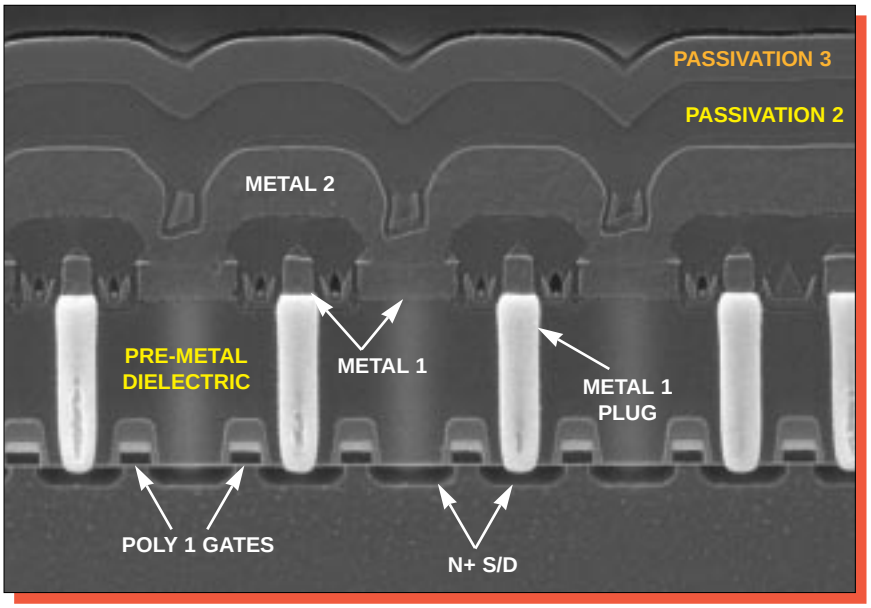


Figure 7. SEM section view of the structure at an input pad. Mag. 6500x.



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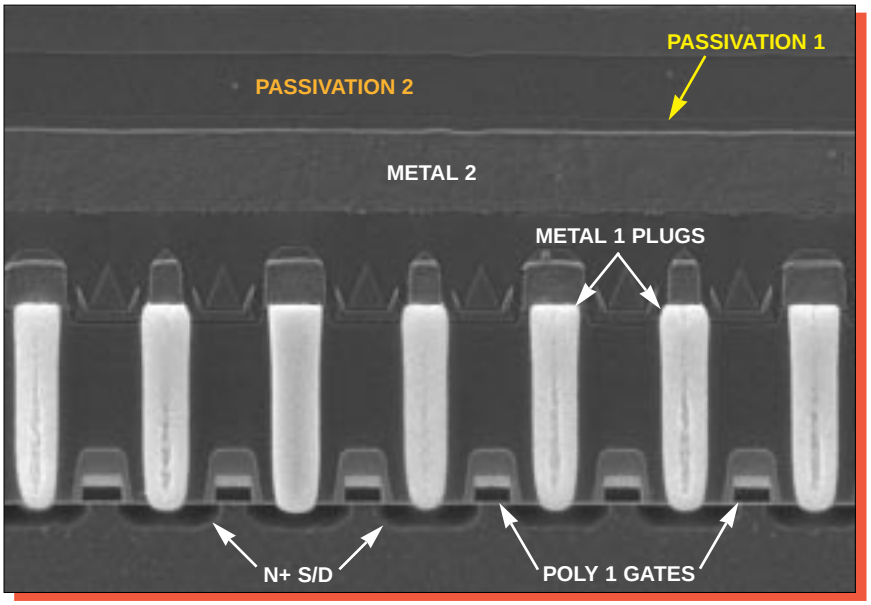

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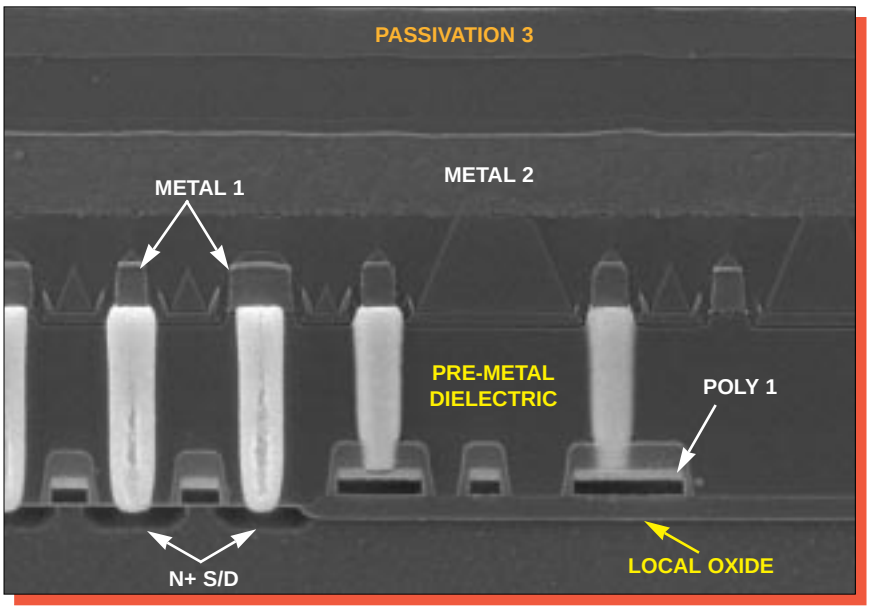
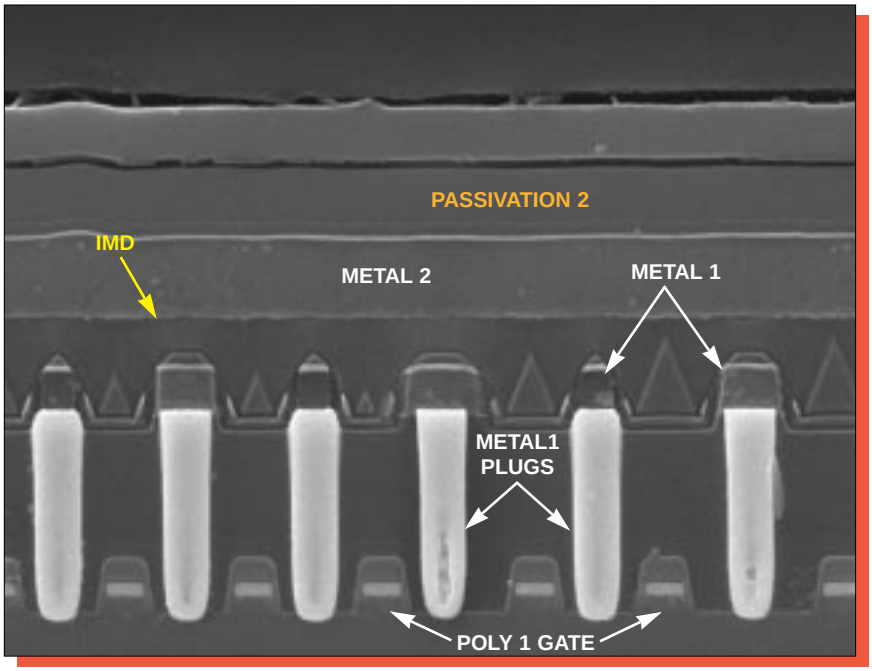


Mag. 13,000x

Figure 8. SEM section views illustrating general device structure.



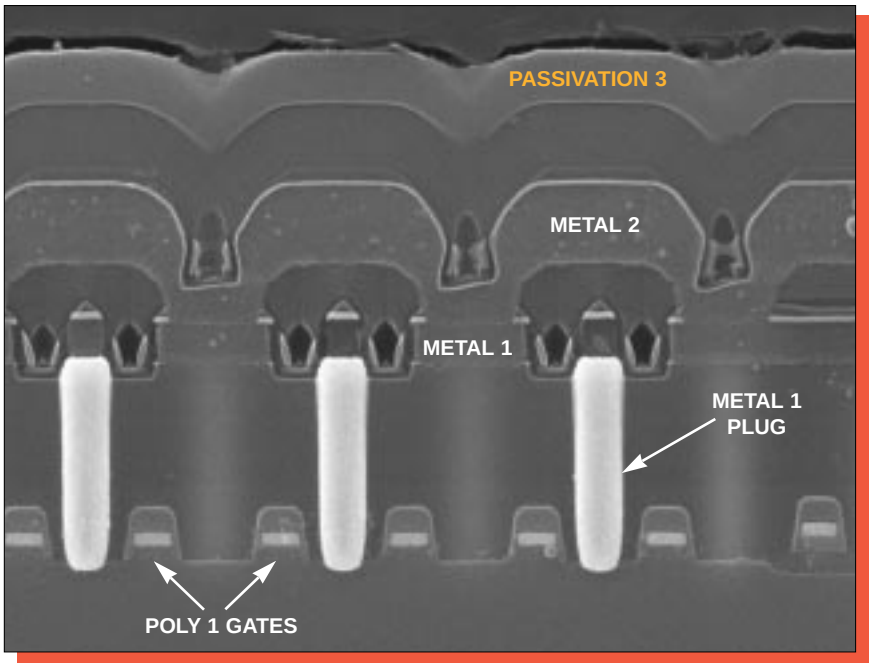
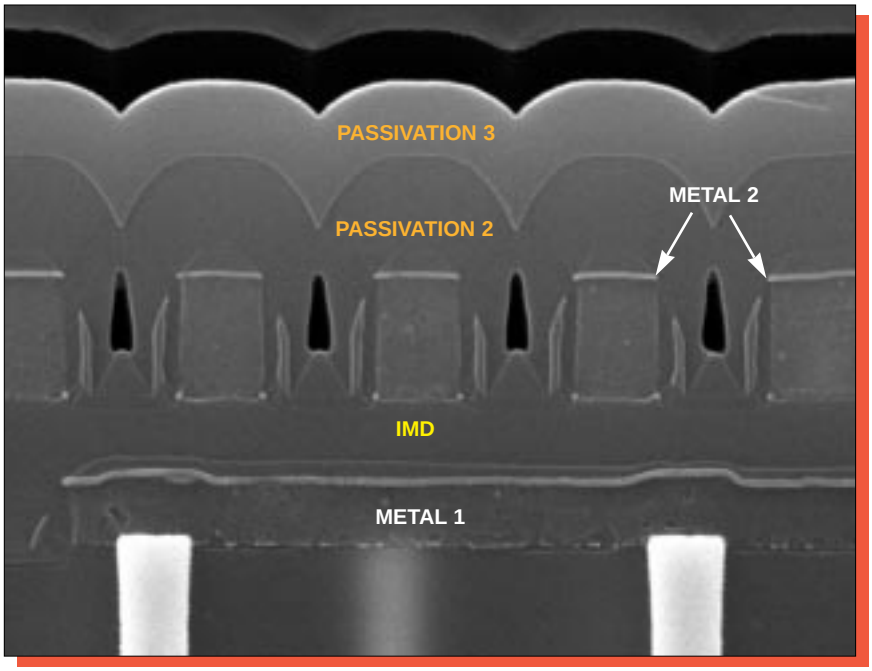
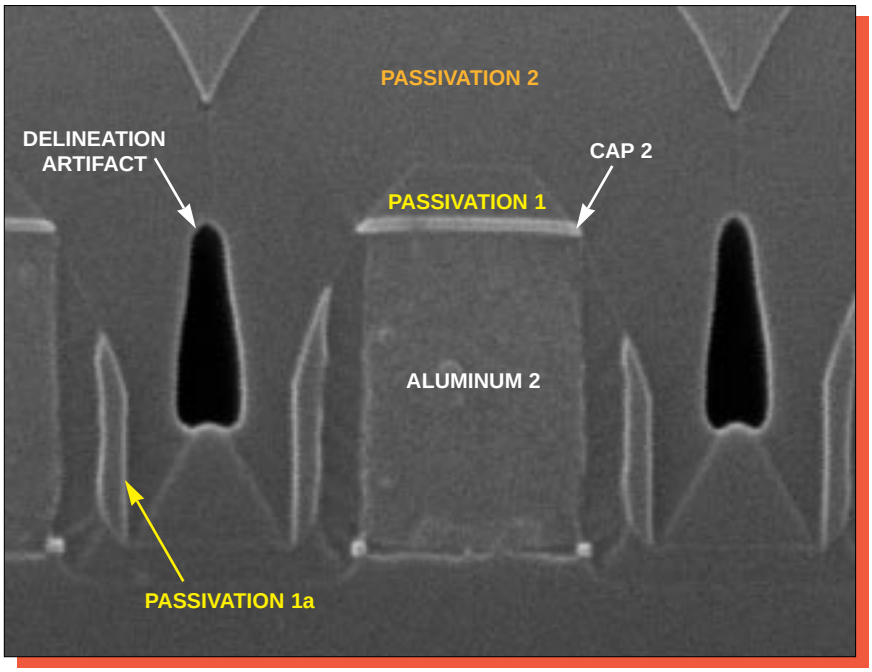


Figure 9. Glass etch section views illustrating general device structure. Mag. 13,000x.

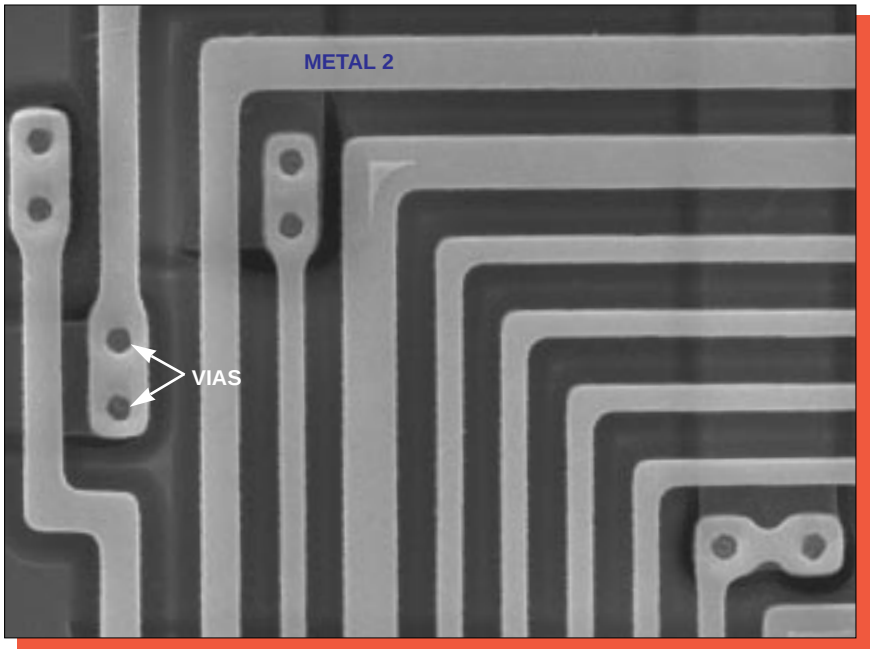


Mag. 20,000x



Mag. 52,000x

Figure 10. SEM section views of metal 2 line profiles.



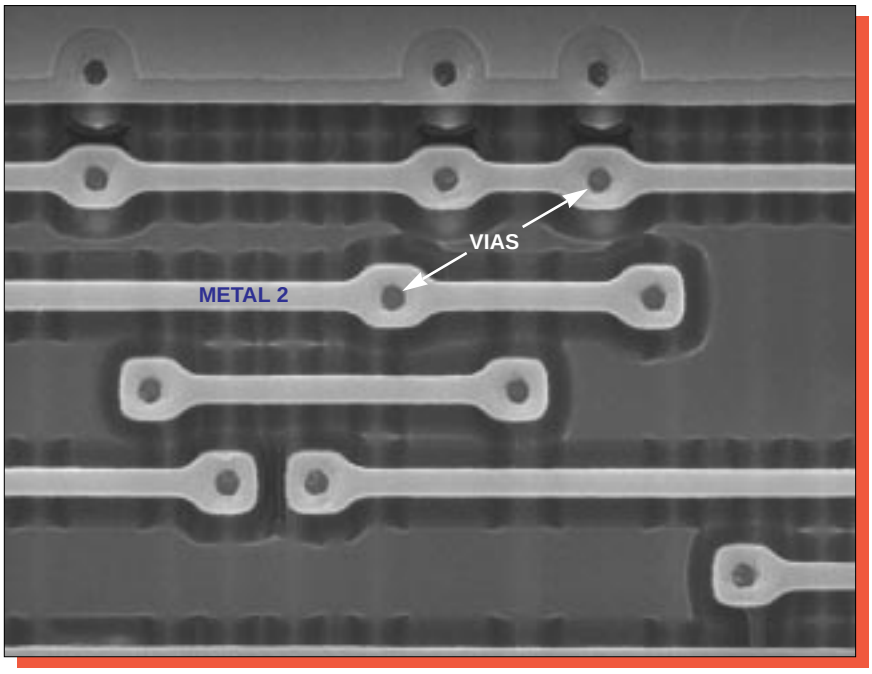
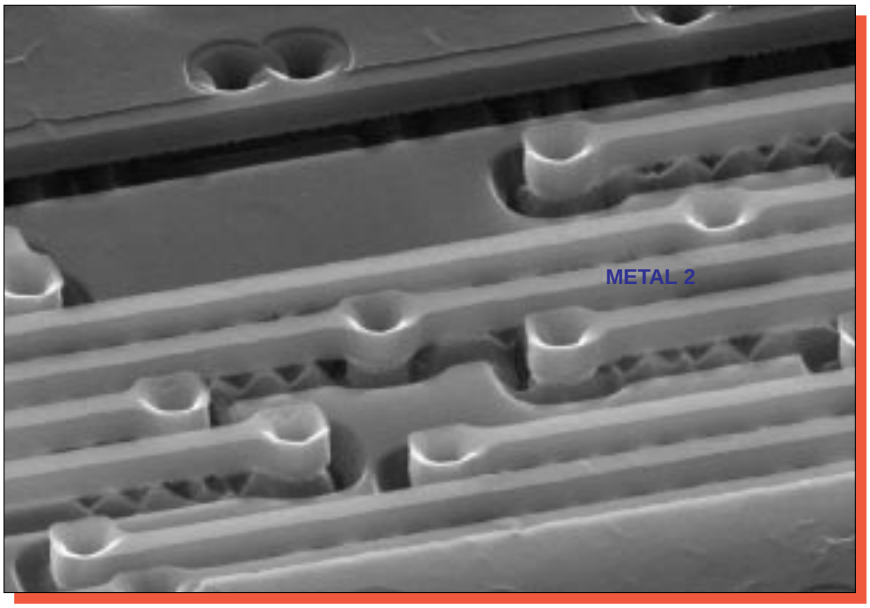
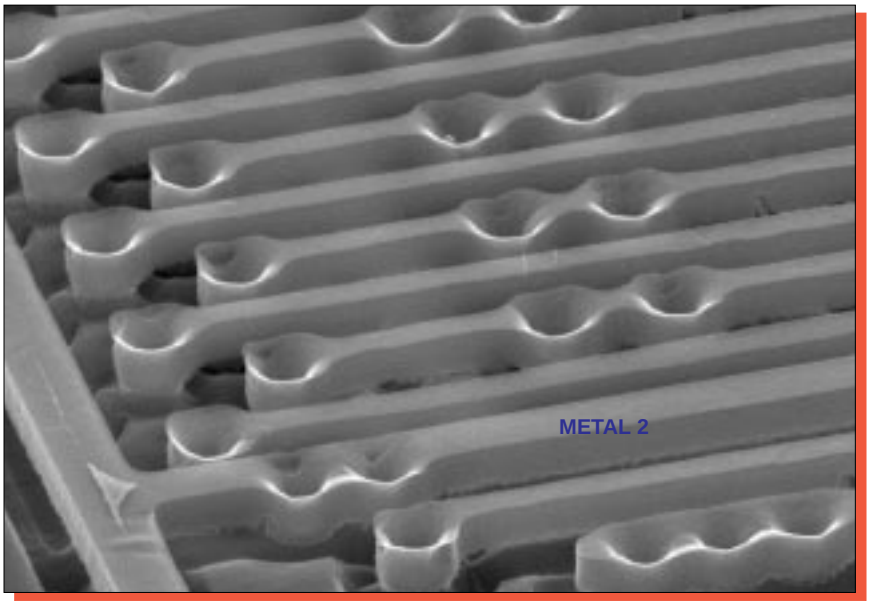


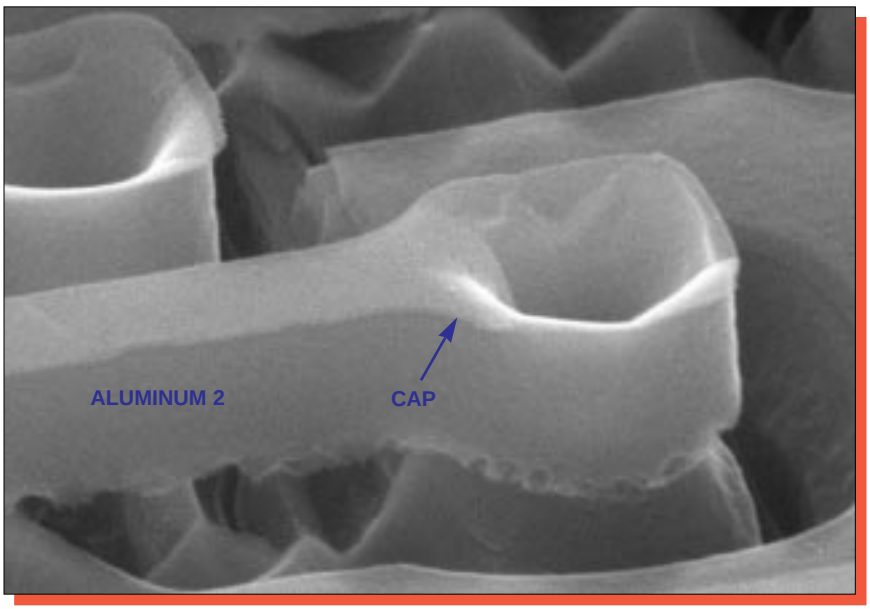
Figure 11. Topological SEM views of metal 2 patterning. Mag. 7000x, 0°.



Mag. 7000x

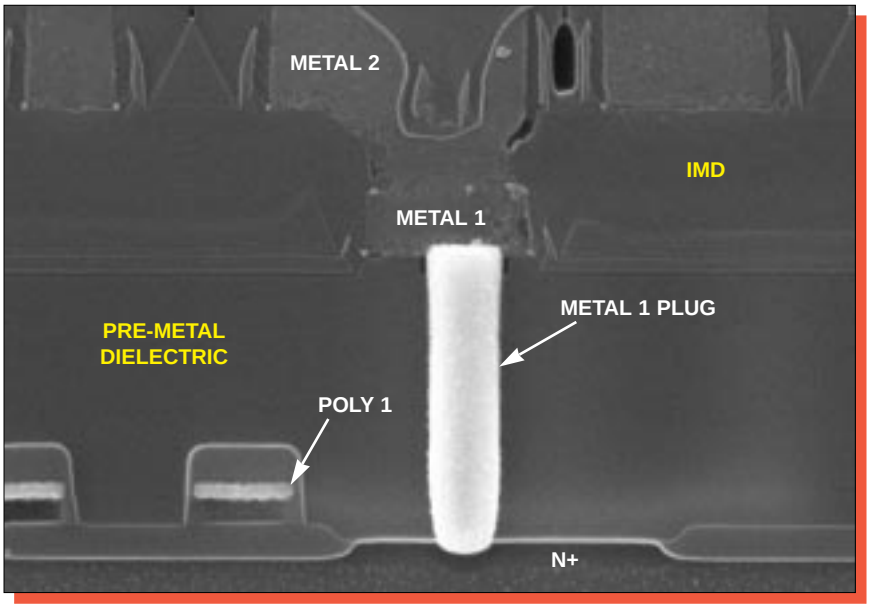


Mag. 9000x



Mag. 32,000x

Figure 12. SEM views of general metal 2 integrity. 60°.



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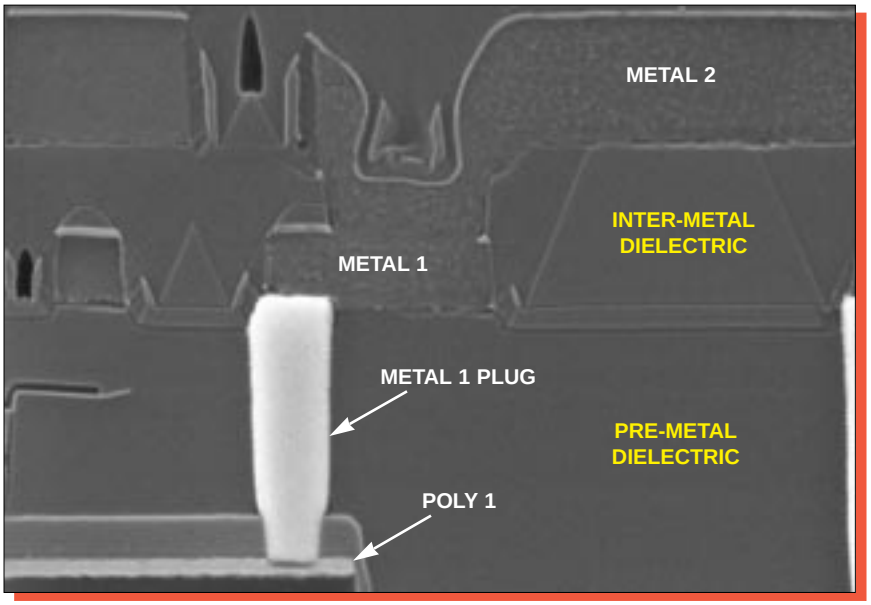

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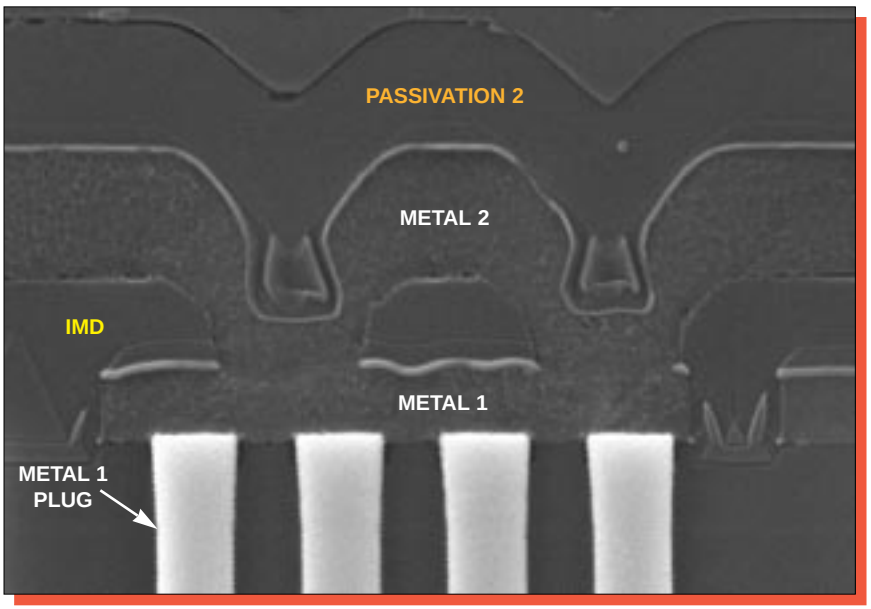
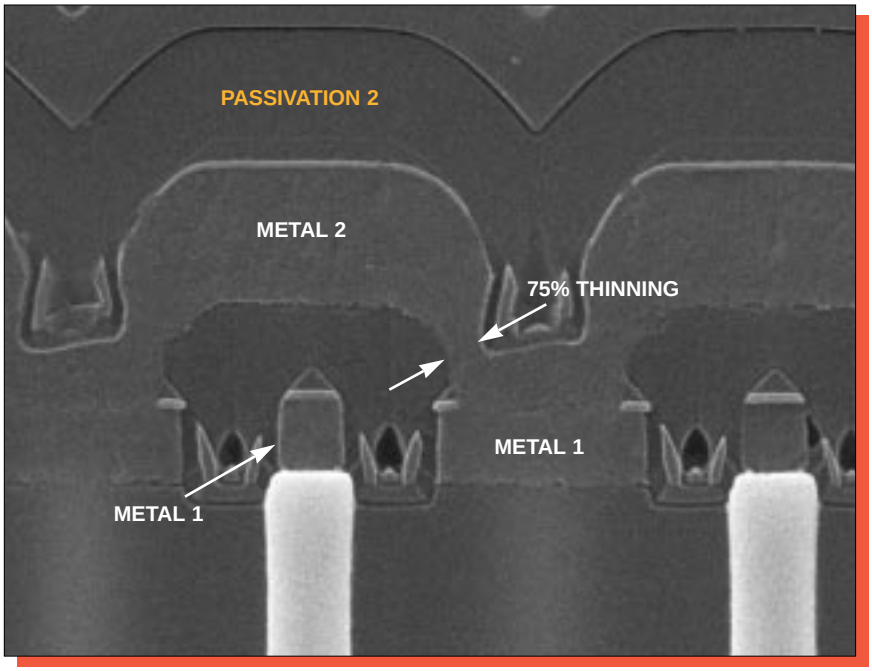
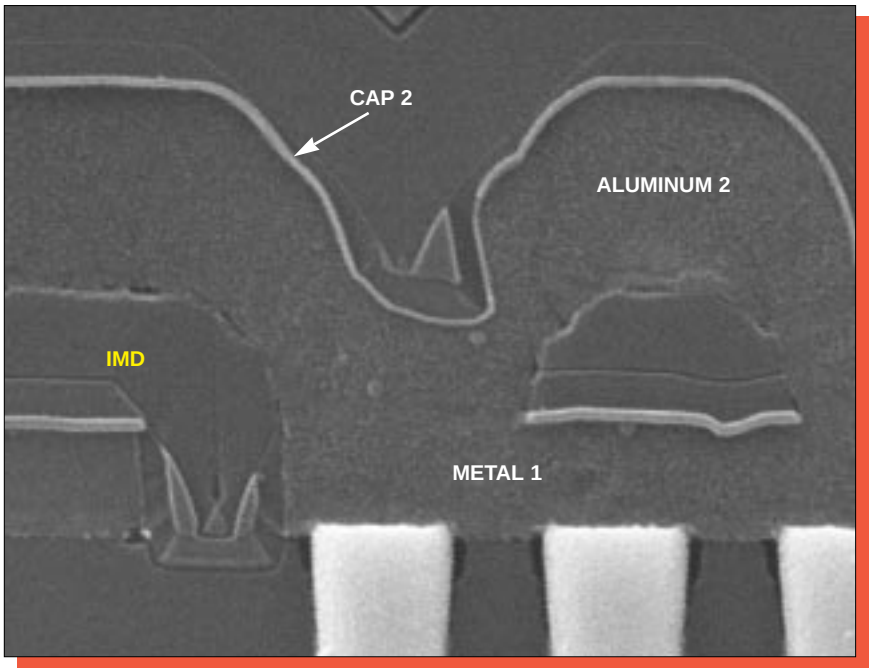


Mag. 22,000x

Figure 13. SEM section views of via (M2-M1) structures.

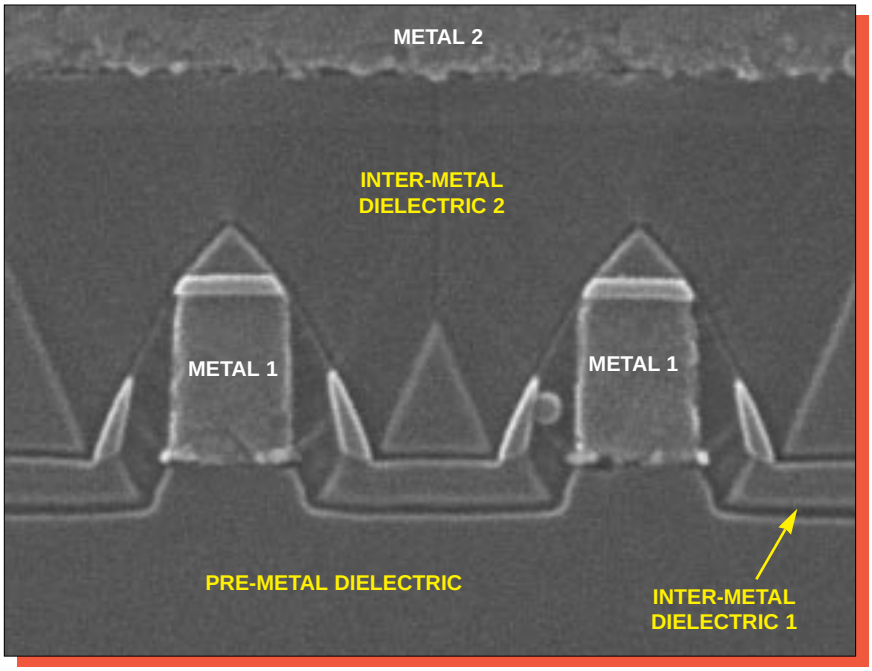


Mag. 25,000x



Mag. 35,000x

Figure 14. Detail SEM section views of vias.



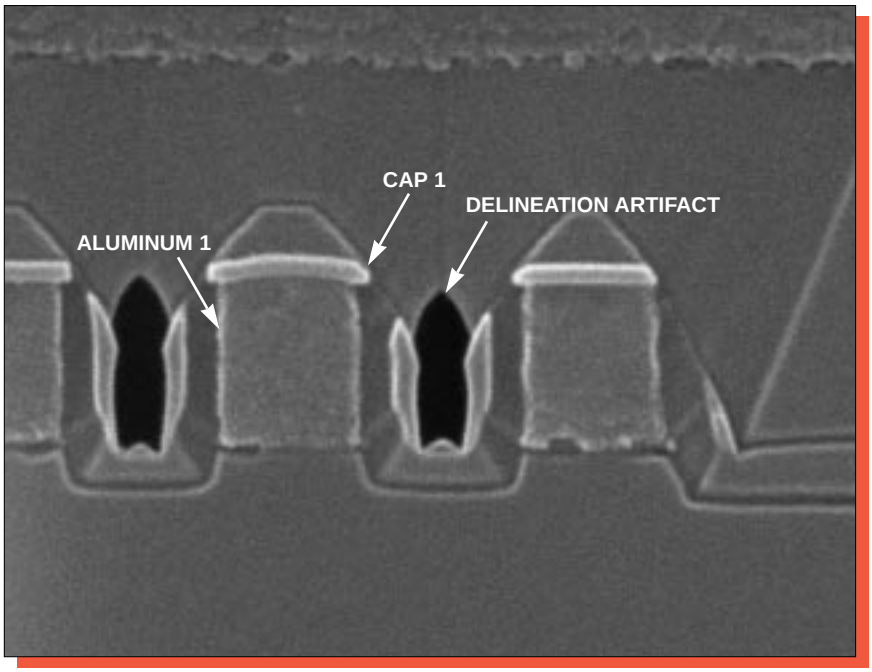
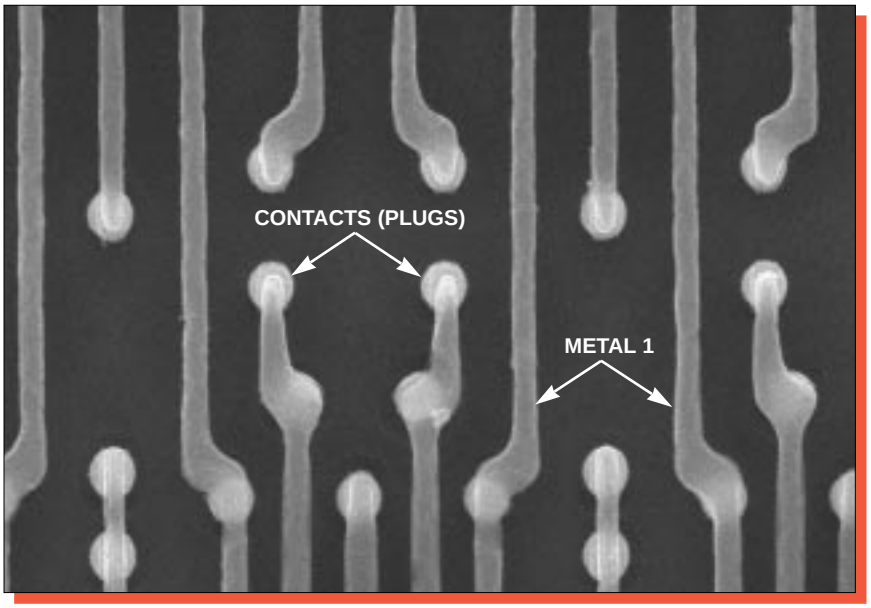
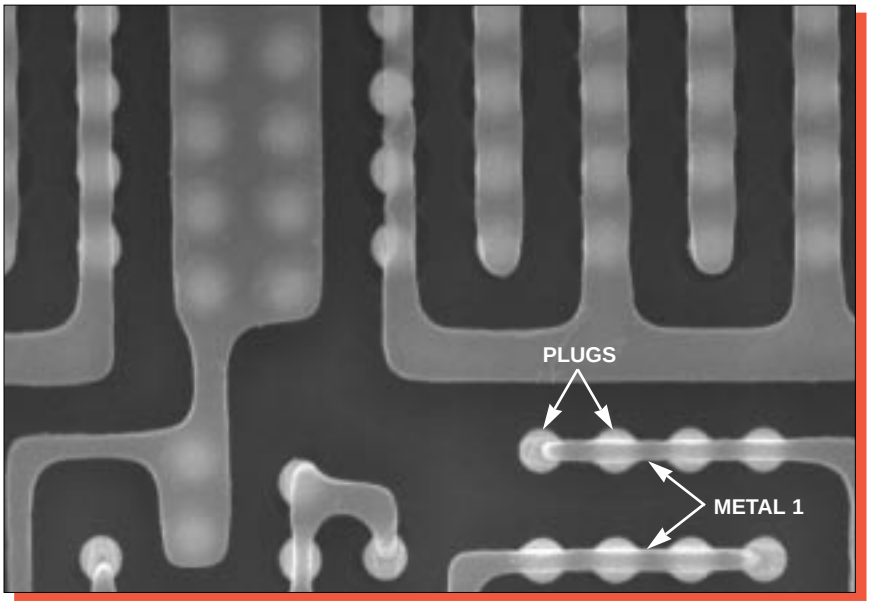


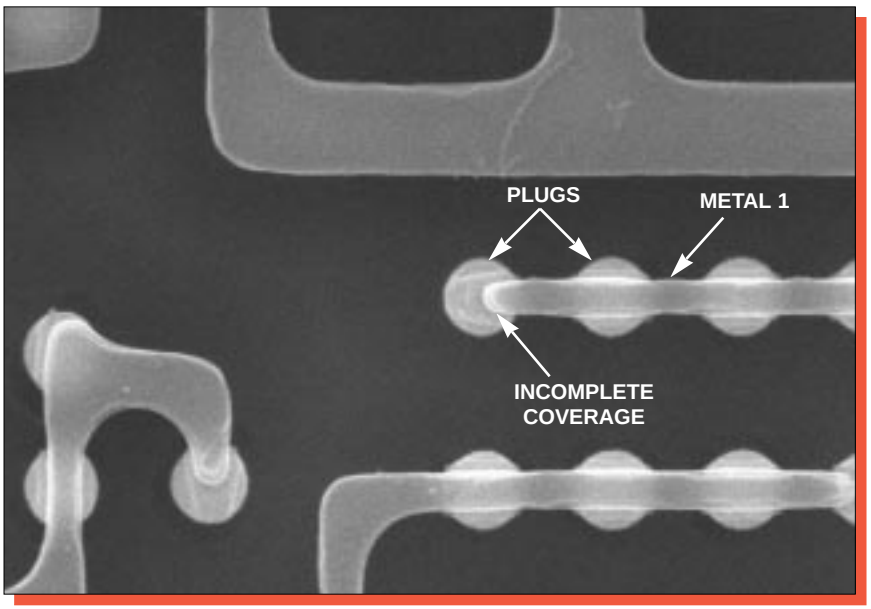
Figure 15. SEM section views of metal 1 line profiles. Mag. 52,000x.



Mag. 12,000x

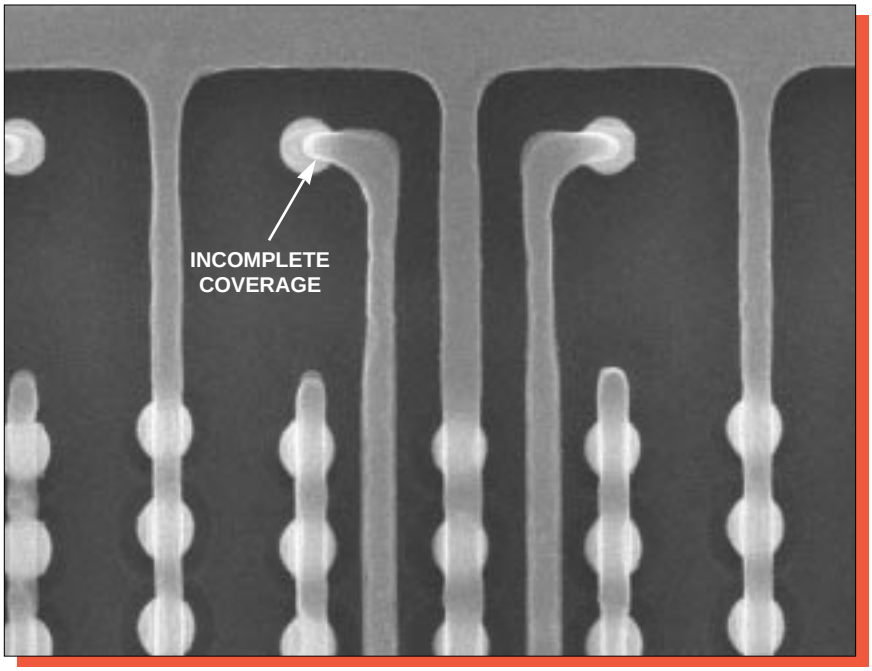


Mag. 12,000x

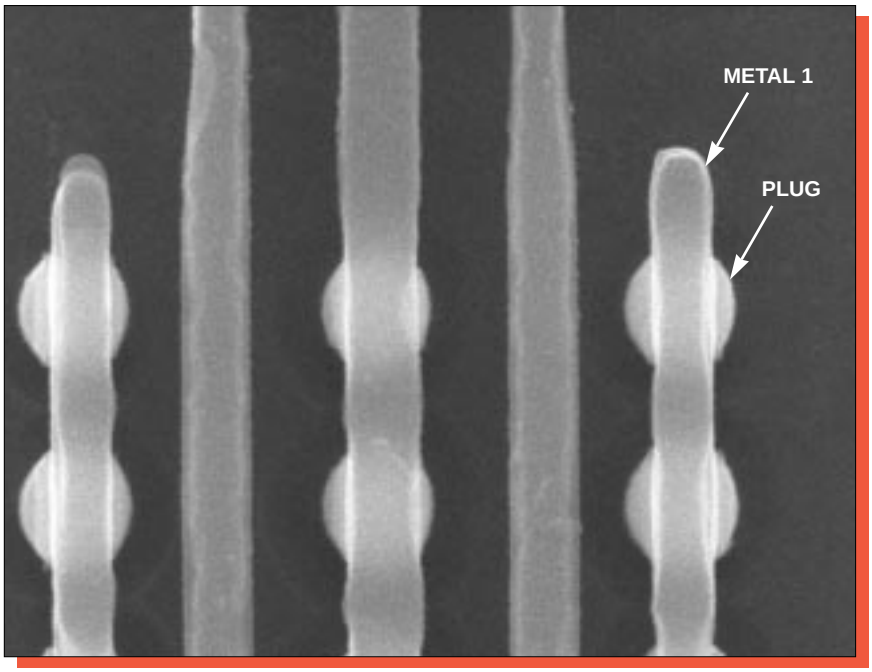


Mag. 20,000x

Figure 16. Topological SEM views of metal 1 patterning. 0°.

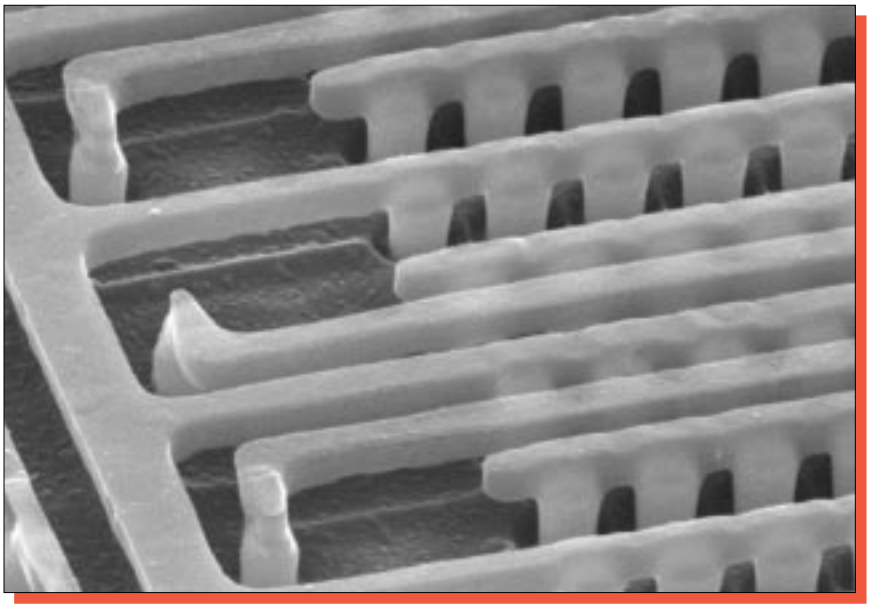


Mag. 15,000x

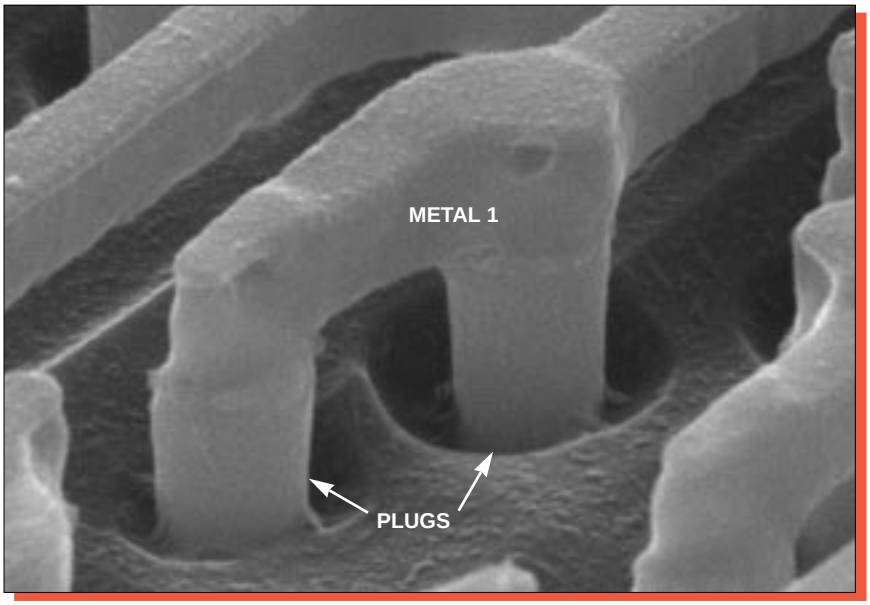


Mag. 30,000x

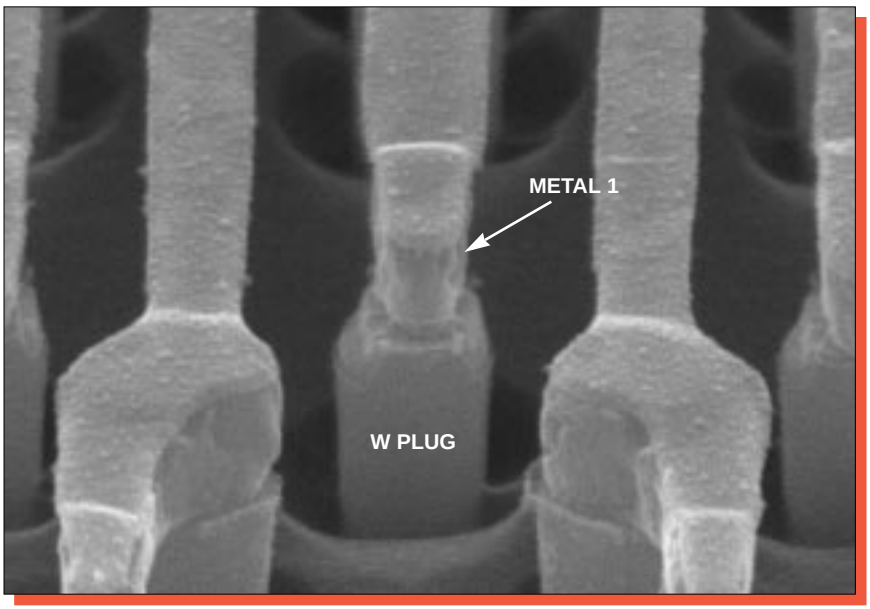
Figure 16a. Additional SEM views of metal 1 patterning. 0°.



Mag. 14,000x

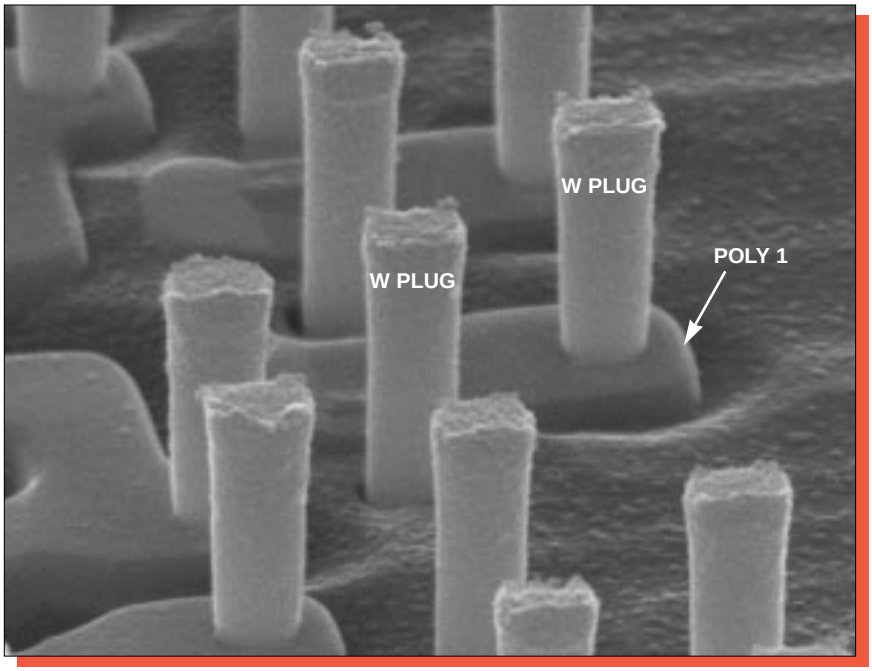


Mag. 40,000x



Mag. 40,000x

Figure 17. SEM views of general metal 1 integrity. 55°.



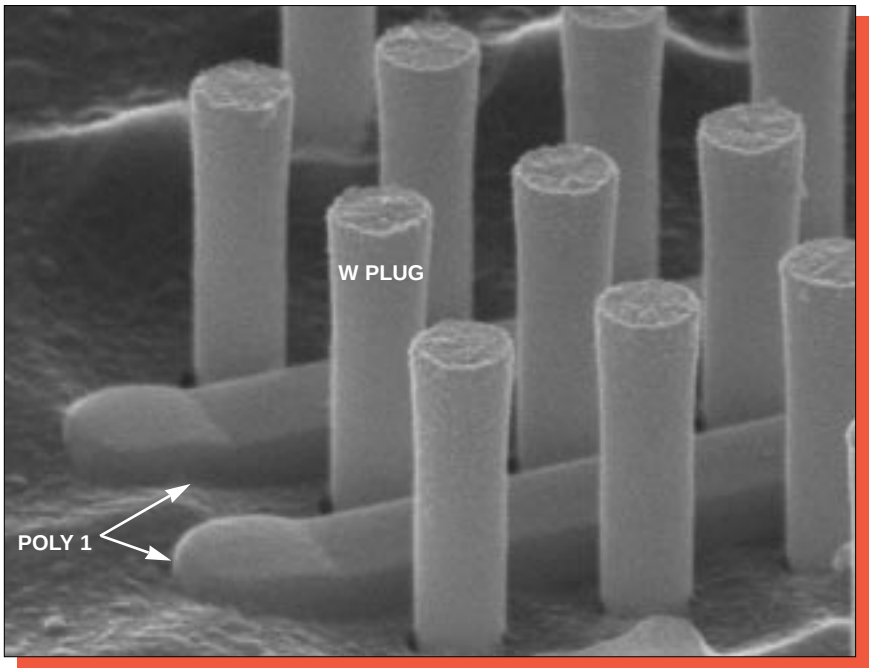
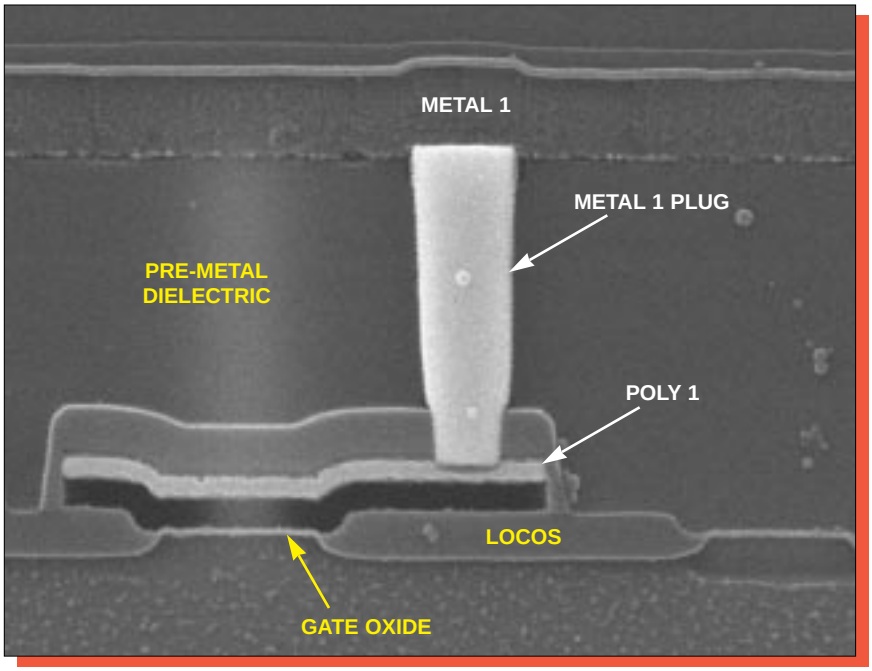


Figure 18. SEM views of metal 1 tungsten plugs. Mag. 25,000x, 60°.



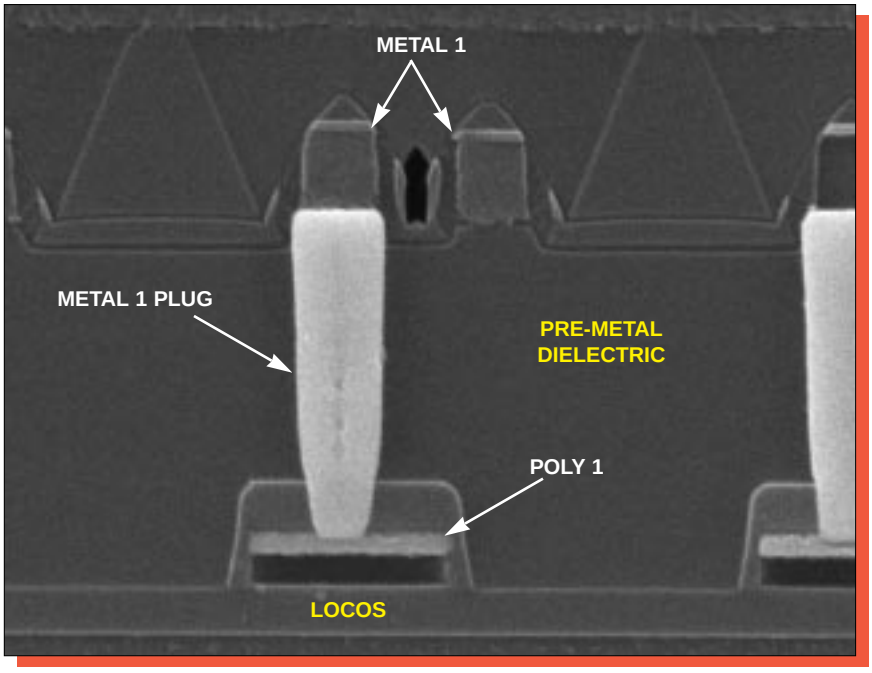
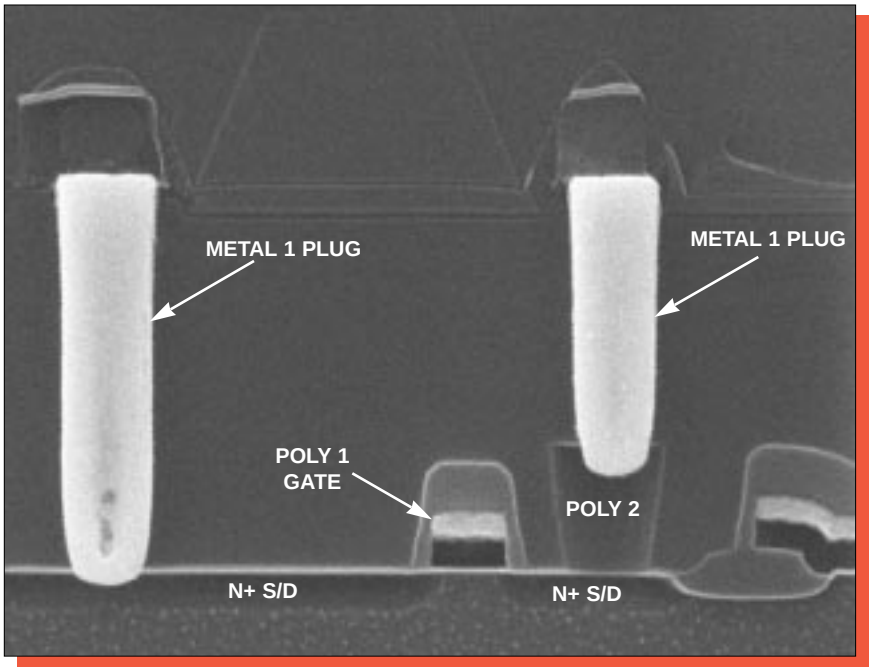
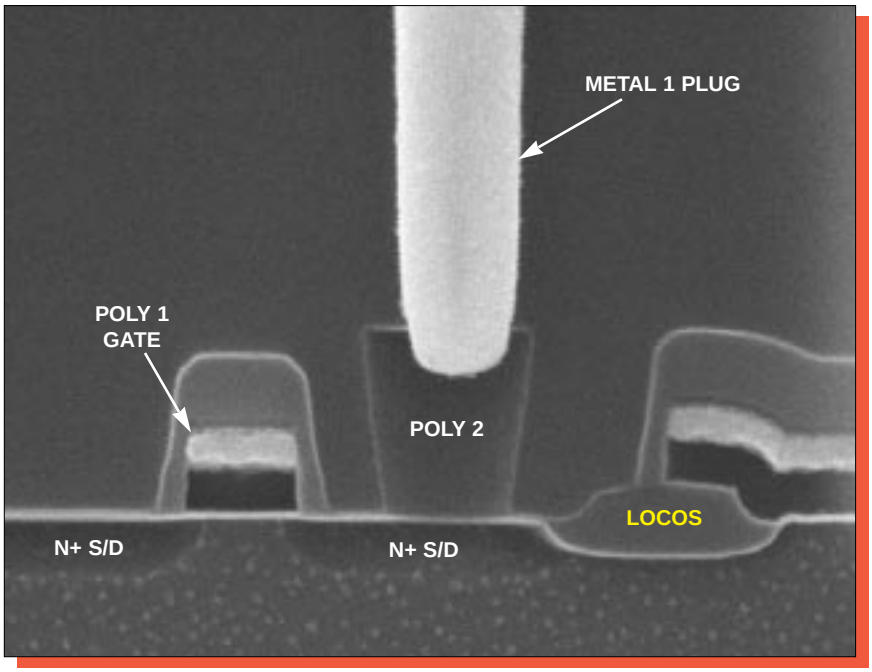


Figure 19. SEM section views of metal 1-to-poly 1 contacts. Mag. 26,000x.

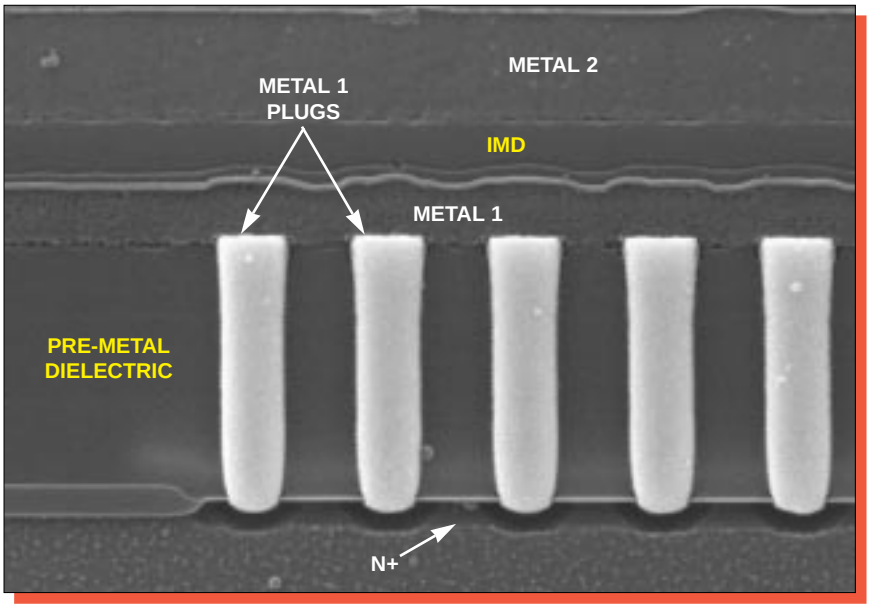


Mag. 26,000x

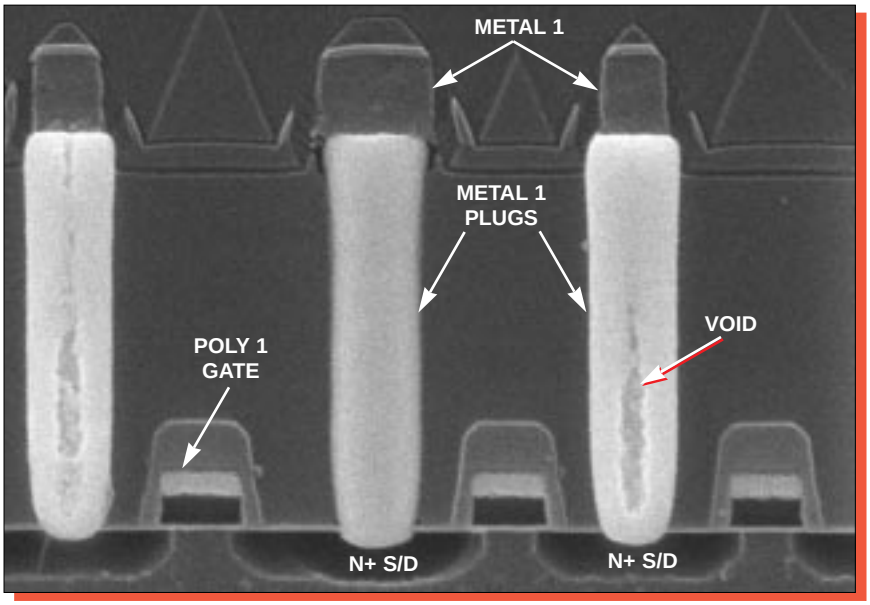


Mag. 40,000x

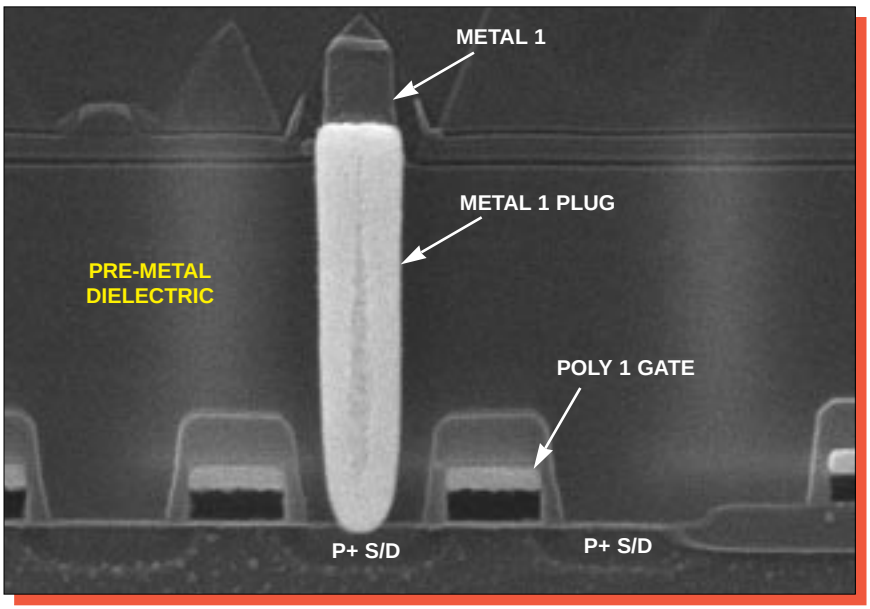
Figure 20. SEM section views of metal 1-to-diffusion contacts.



metal 1-to-N+,
Mag. 17,600x

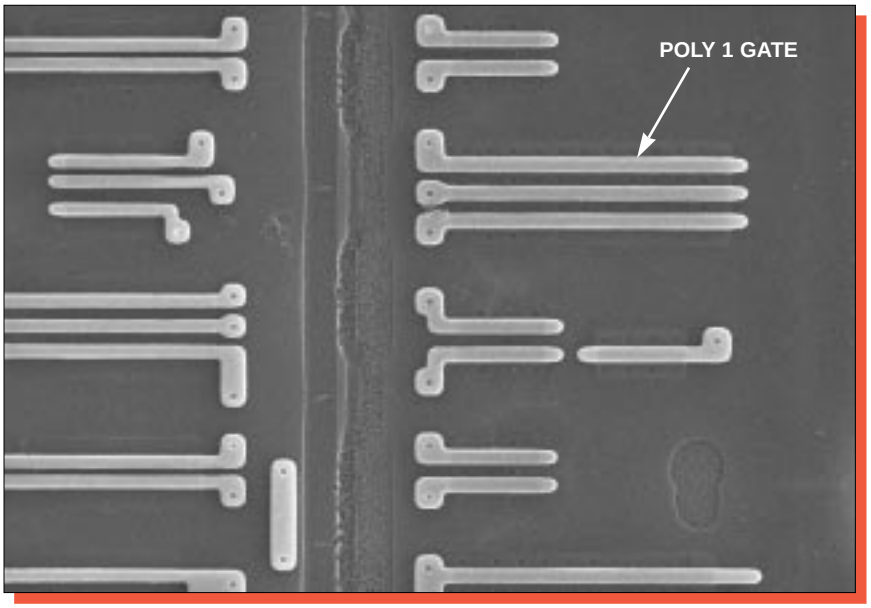


metal 1-to-N+,
Mag. 26,000x

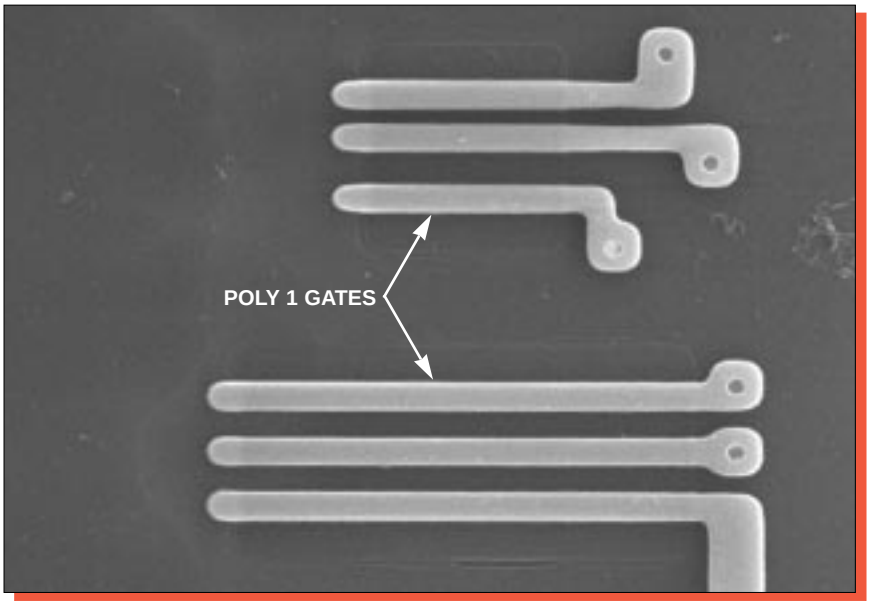


metal 1-to-P+,
Mag. 26,000x

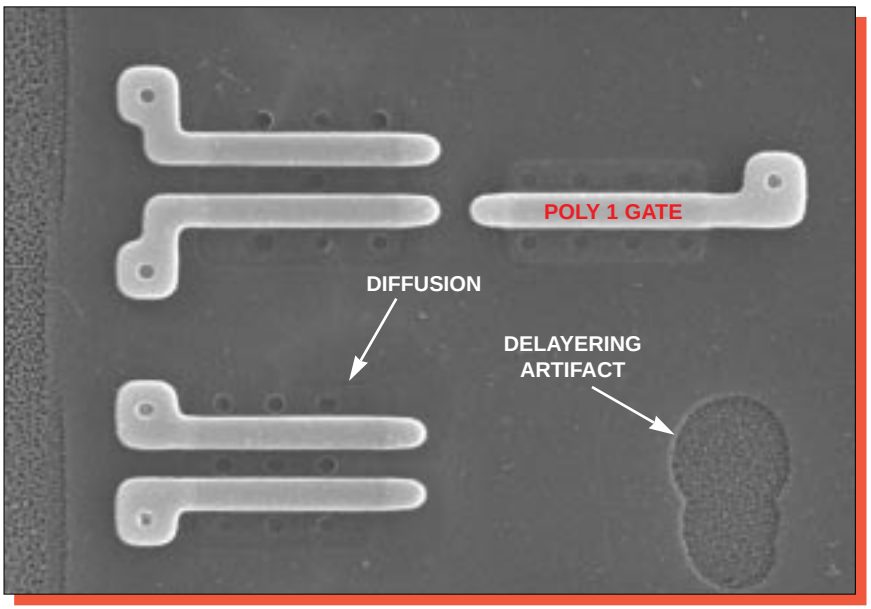
Figure 21. SEM section views of standard metal 1-to-diffusion contacts.



Mag. 3000x

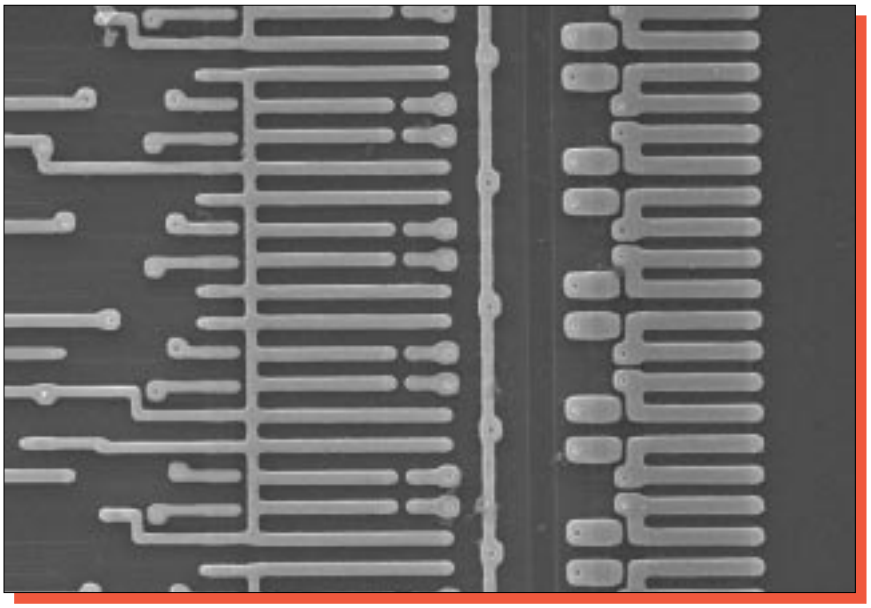


Mag. 6500x

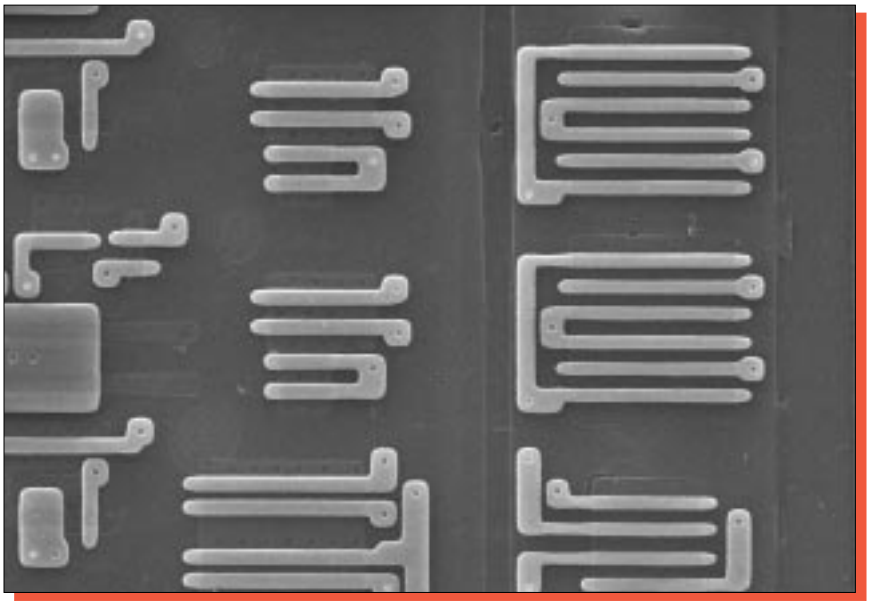


Mag. 6500x

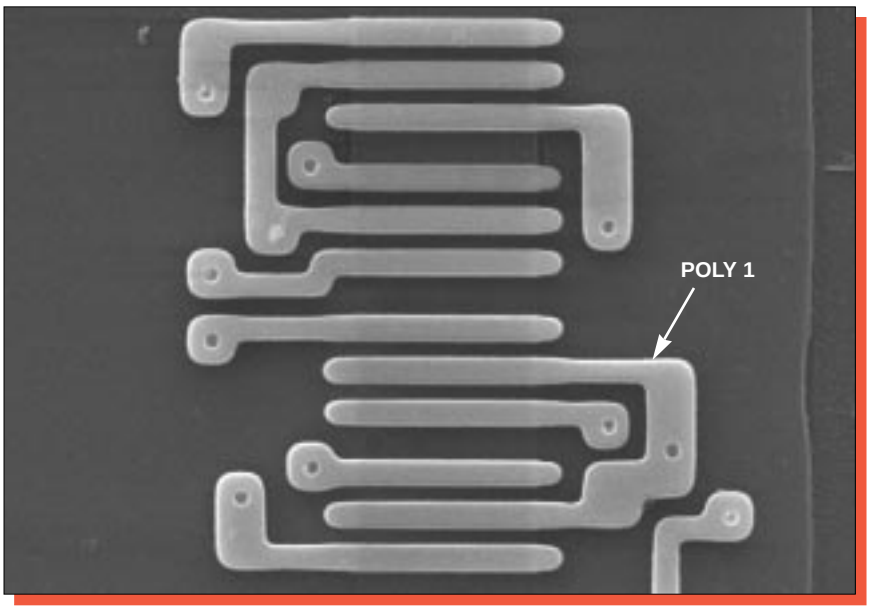
Figure 22. Topological SEM views of poly 1 patterning. 0°.



row decode,
Mag. 3000x

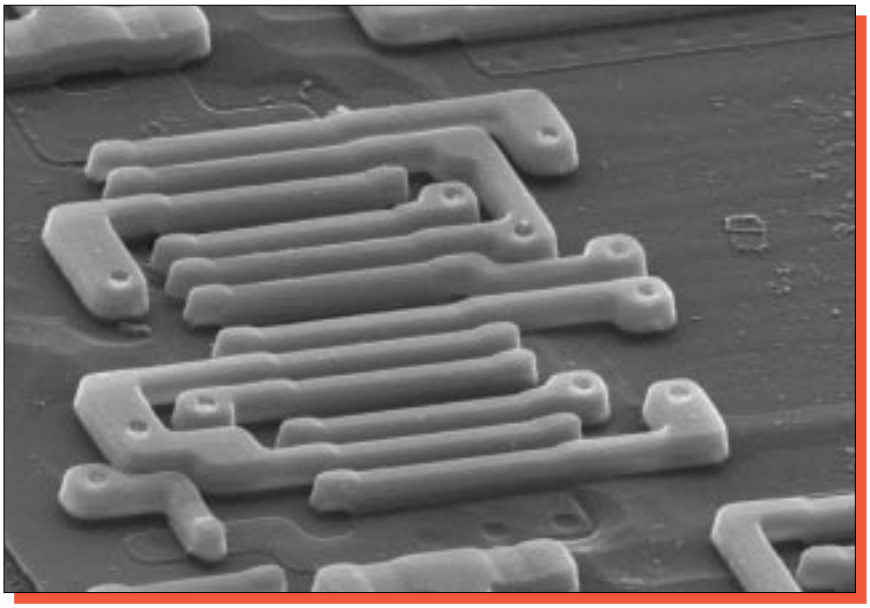


column decode,
Mag. 3000x

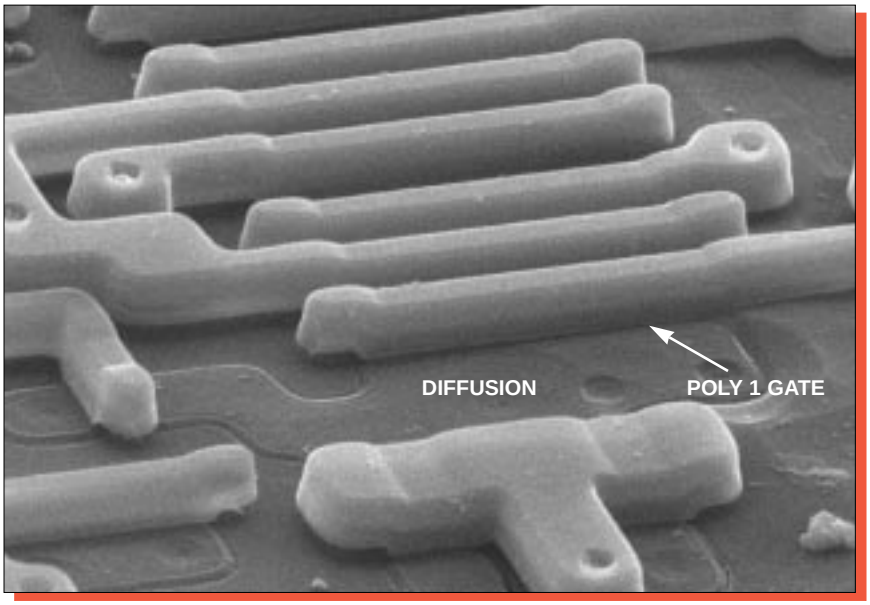


column decode,
Mag. 6000x

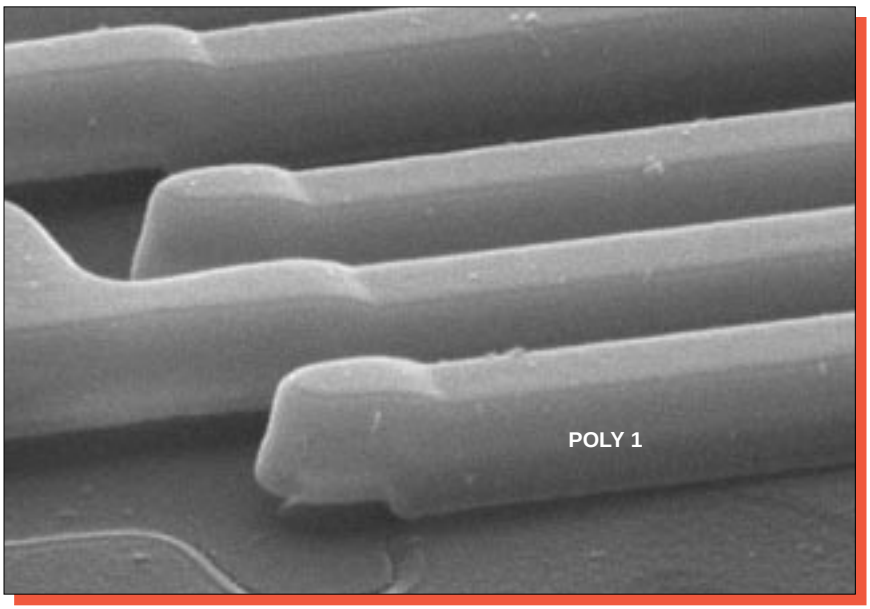
Figure 23. Topological SEM views of poly 1 patterning in the decode areas. 0°.



Mag. 8000x

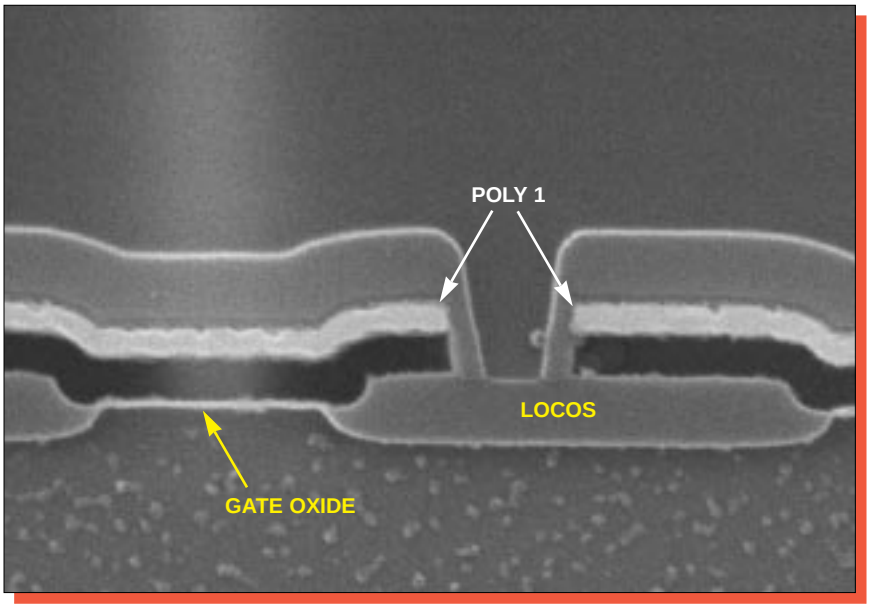


Mag. 13,000x

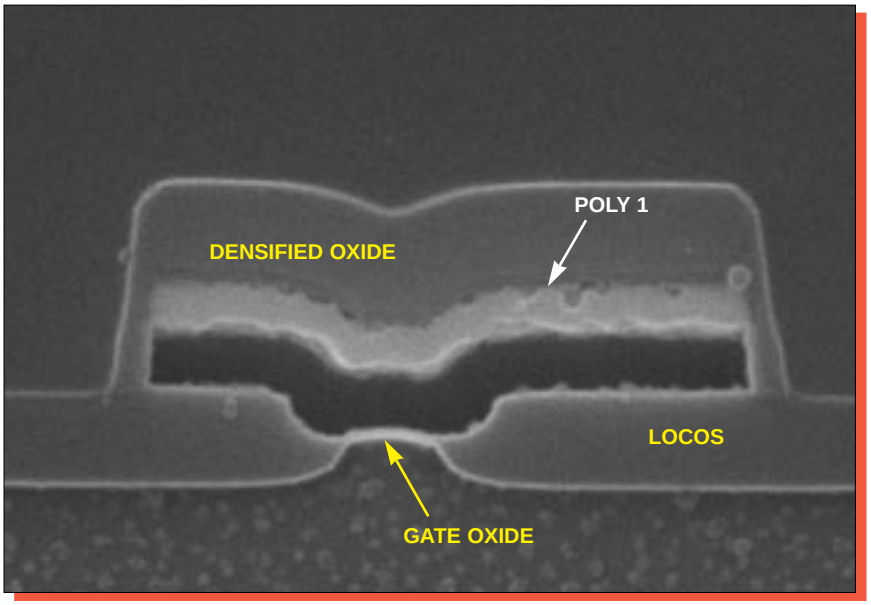


Mag. 30,000x

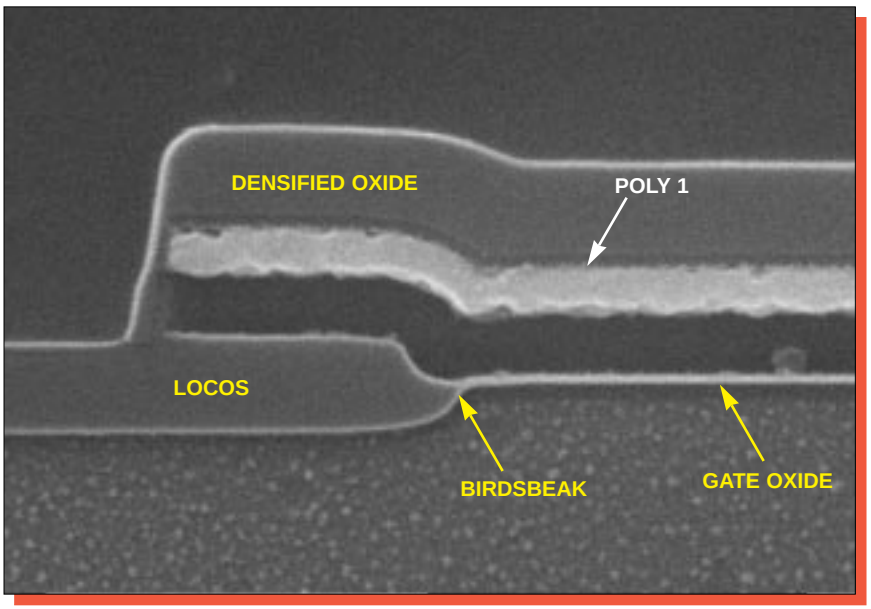
Figure 24. Perspective SEM views of poly 1 coverage. 60°.



Mag. 40,000x

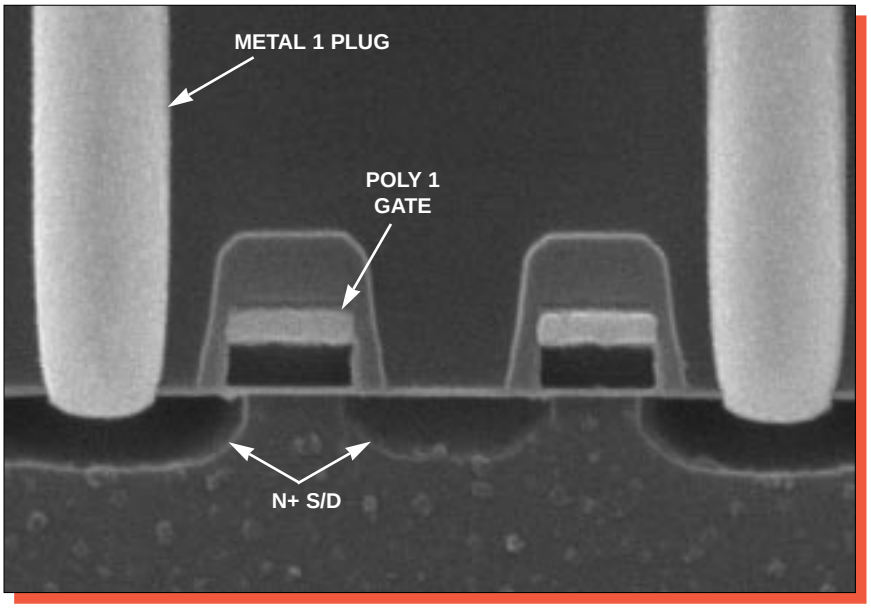


Mag. 52,000x

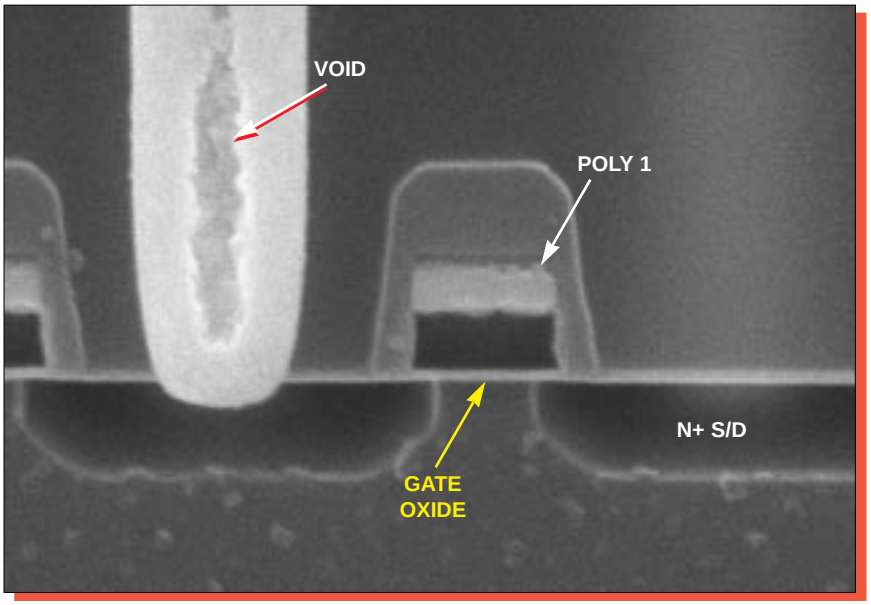


Mag. 52,000x

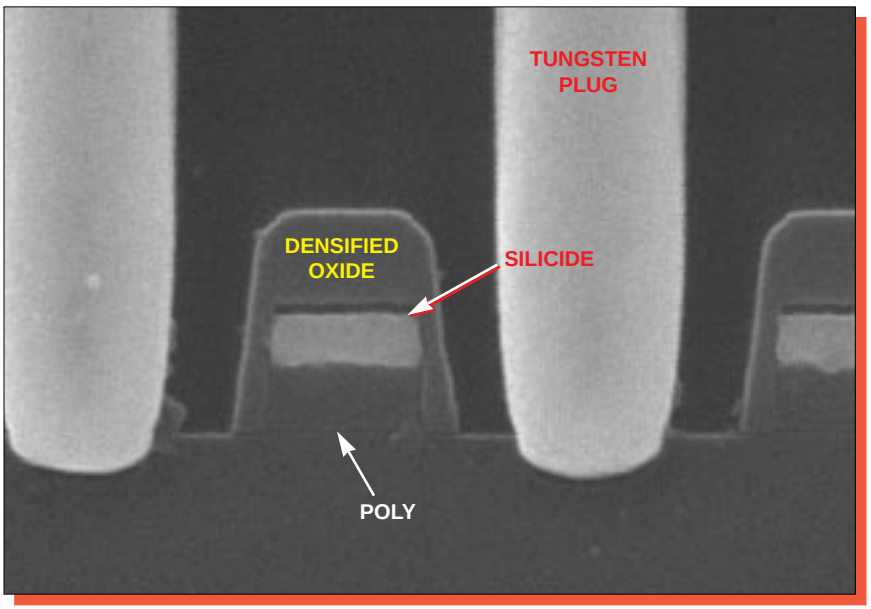
Figure 25. SEM section views of local oxide birdsbeak profiles.



Mag. 40,000x

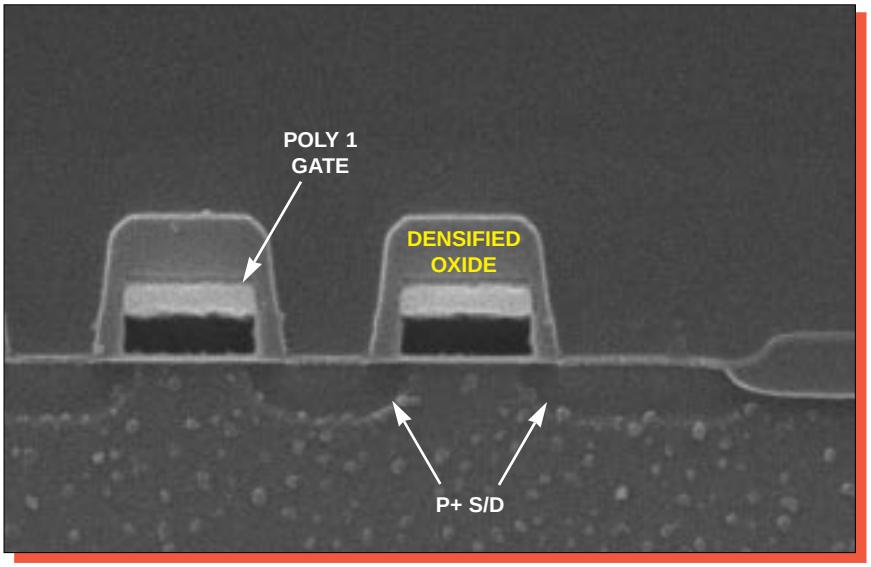


Mag. 52,000x

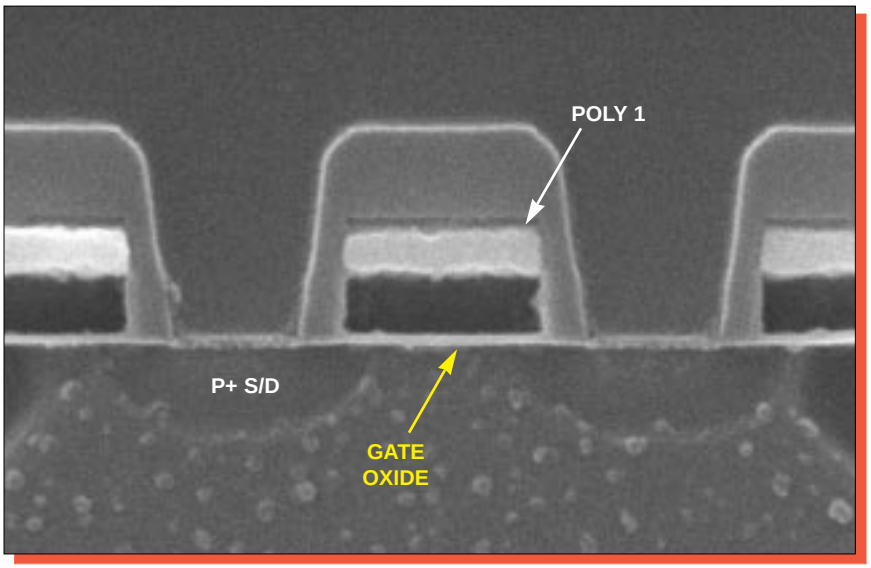


glass etch,
Mag. 52,000x

Figure 26. SEM section views of N-channel transistors.



Mag. 35,000x



Mag. 52,000x

Figure 27. SEM section views of P-channel transistors.

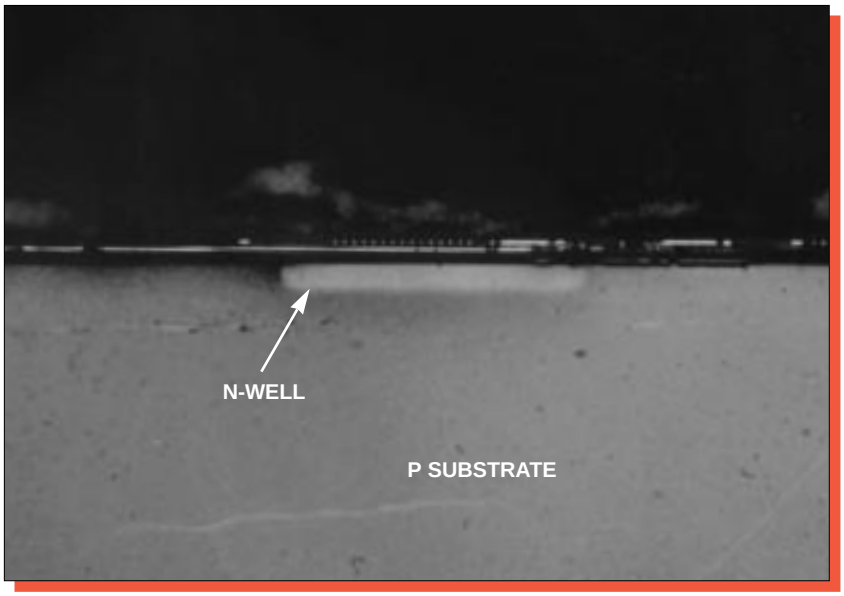
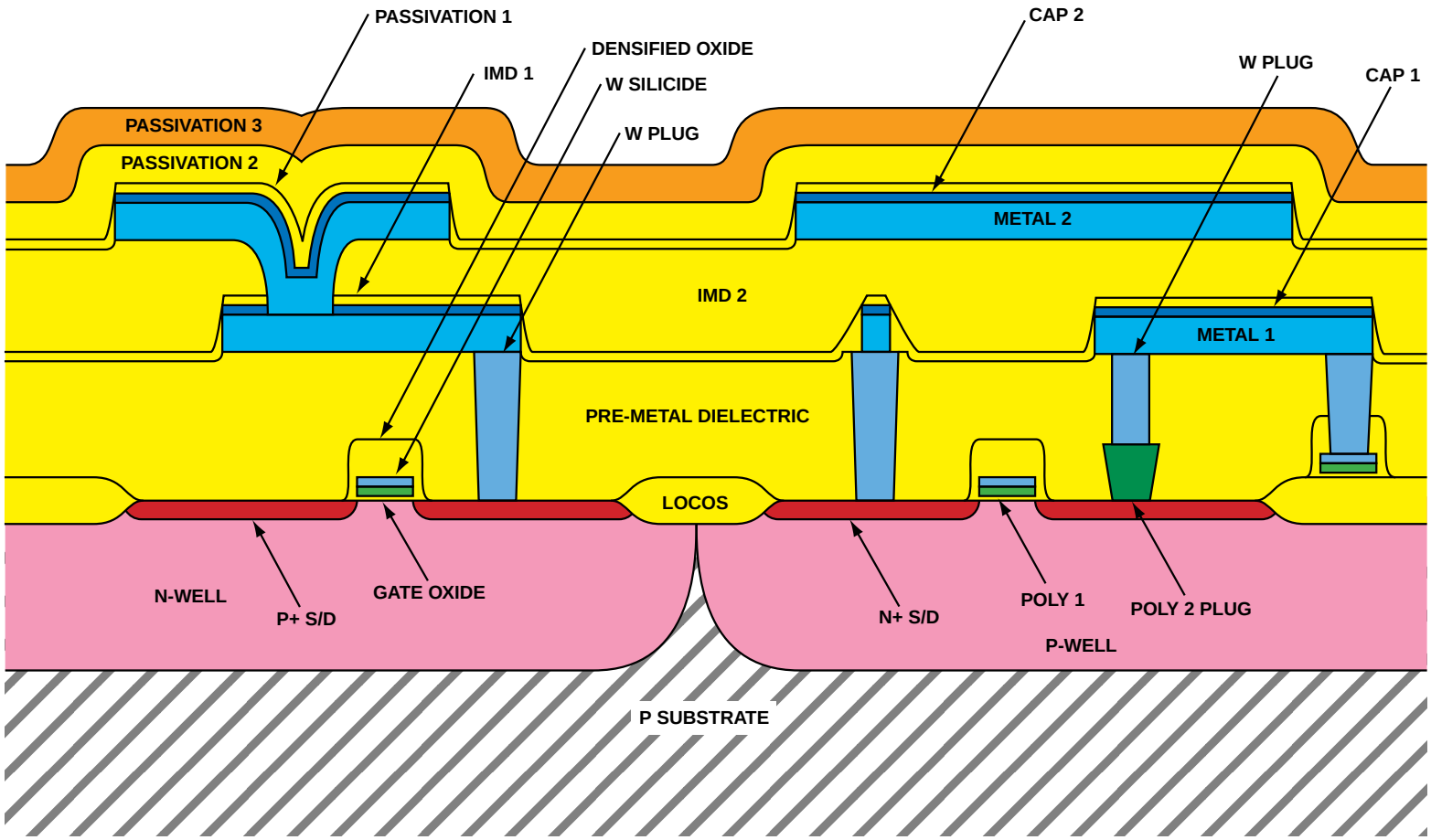


Figure 28. Optical view of the well structure. Mag. 800x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 29. Color cross section drawing illustrating device structure.

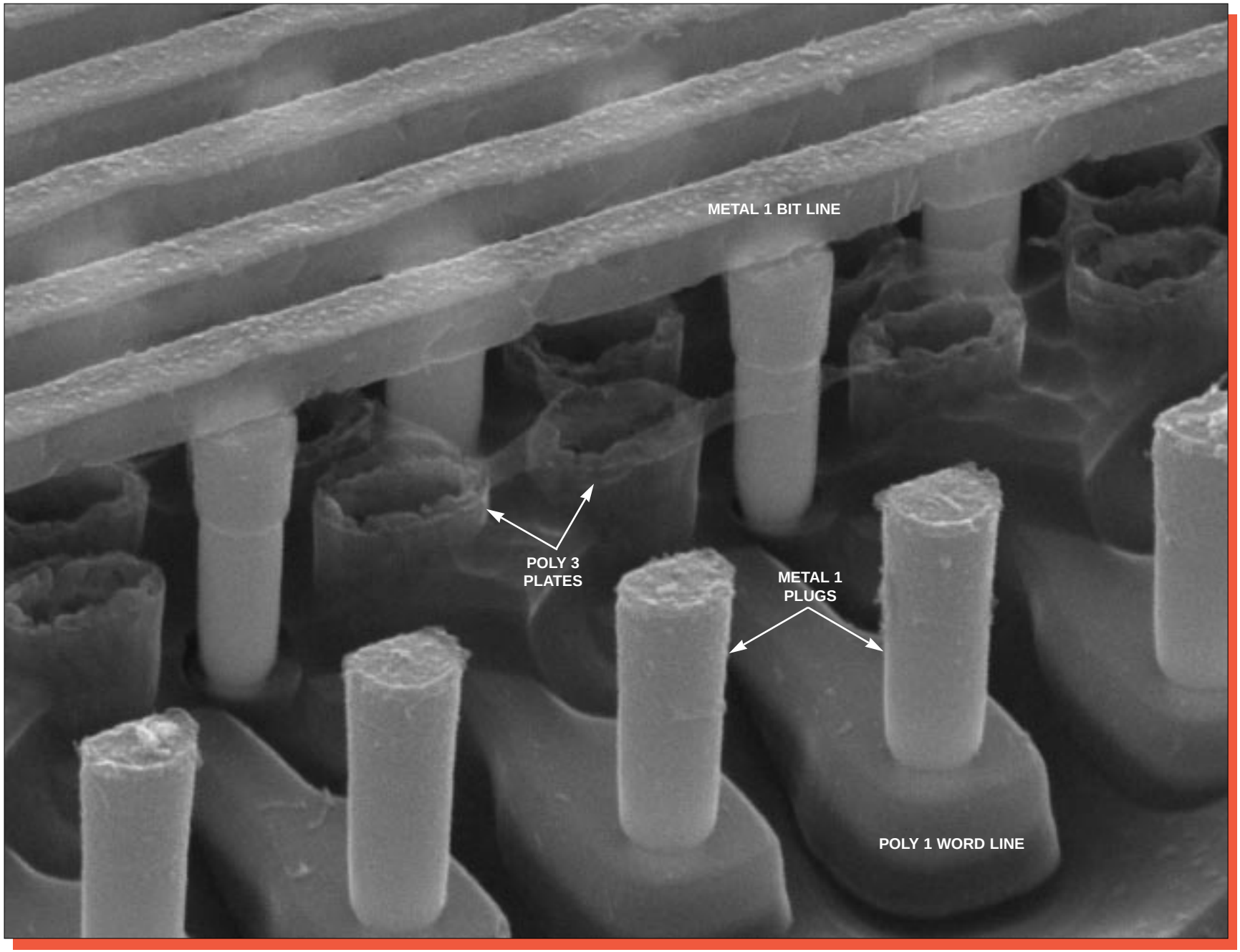
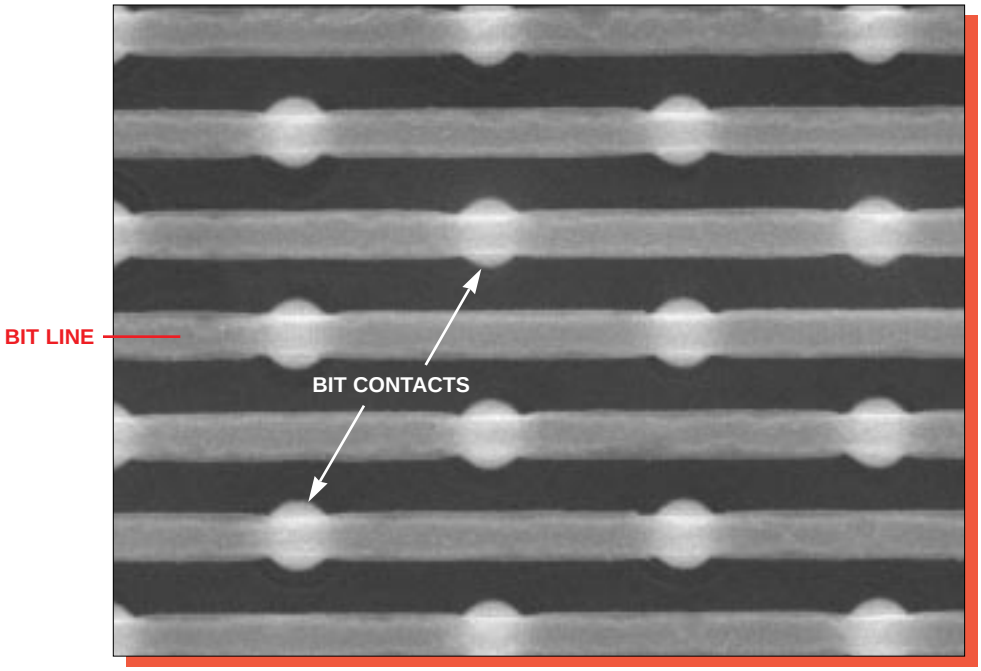
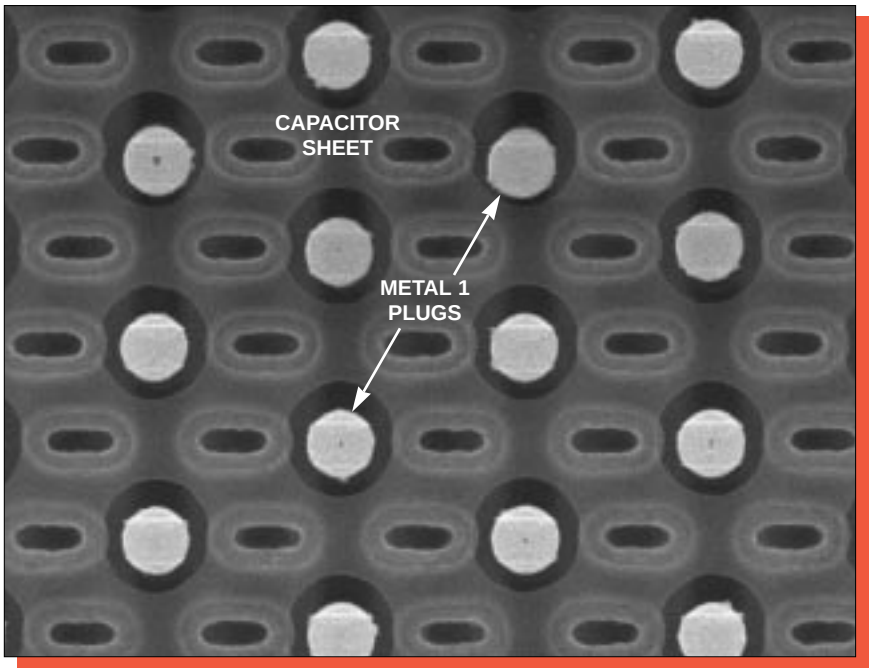


Figure 30. Perspective SEM view of the DRAM cell structure. Mag. 40,000x, 60°.

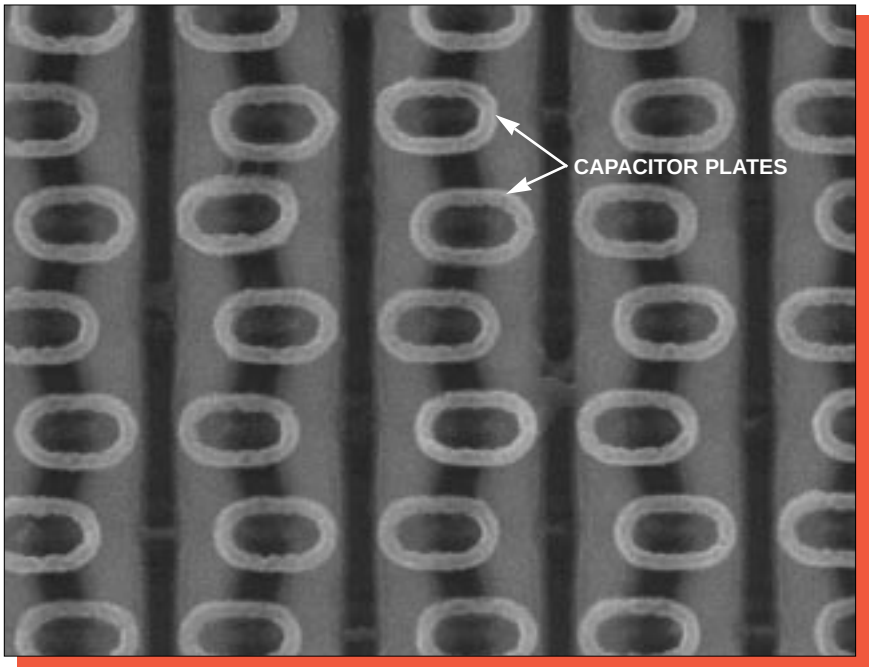


metal 1

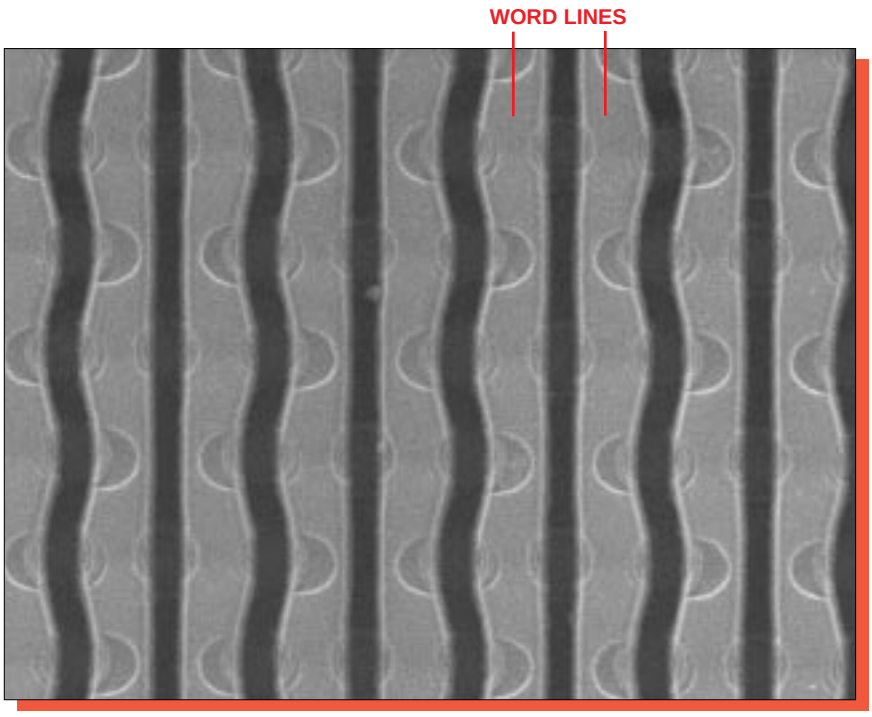


poly 4

Figure 31. Topological SEM views of the DRAM array. Mag. 20,000x, 0°.

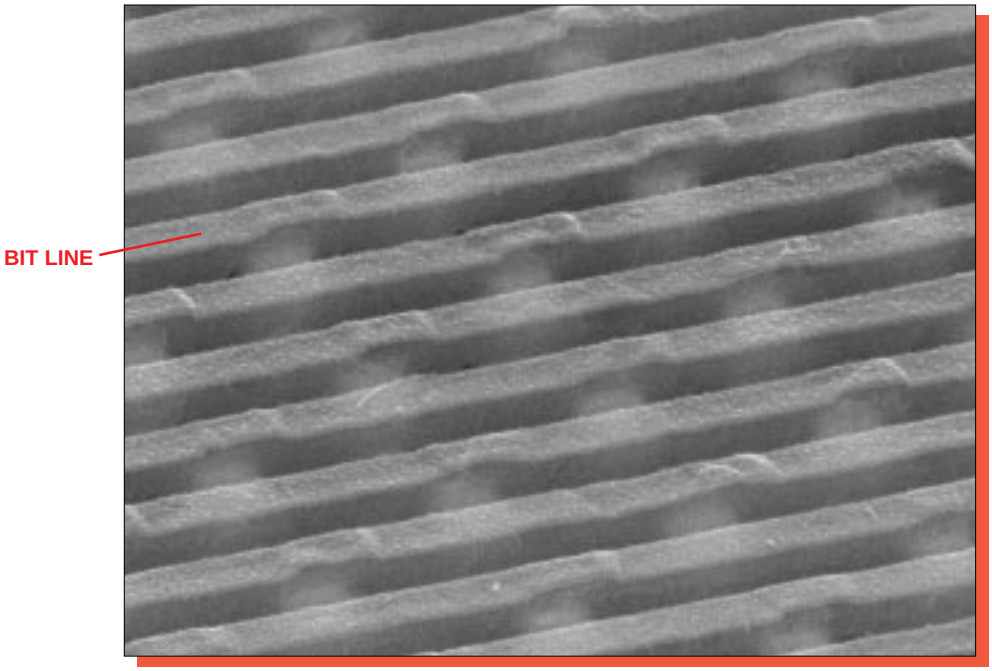


poly 3

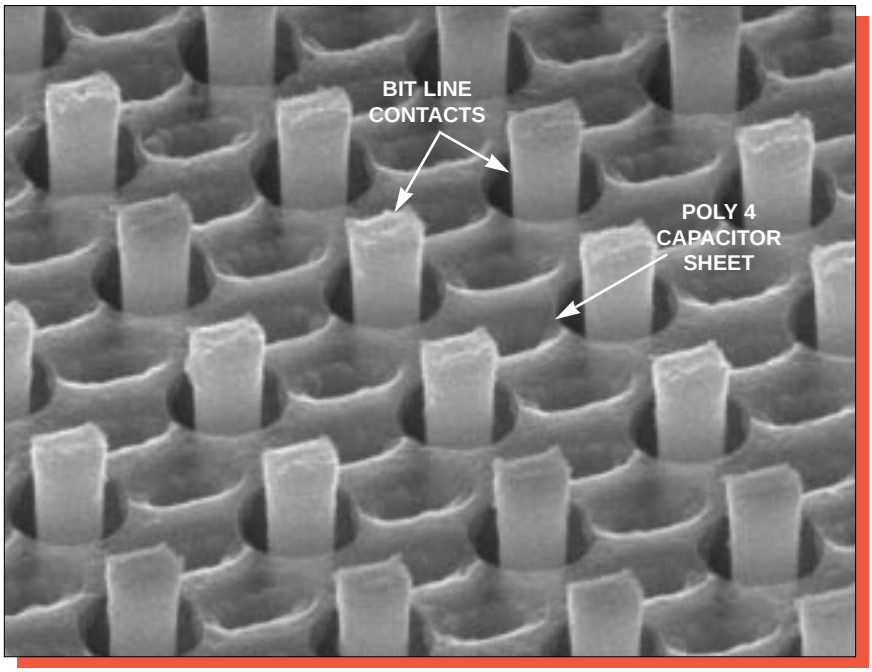


poly 1

Figure 31a. Topological SEM views of the DRAM array. Mag. 20,000x, 0°.

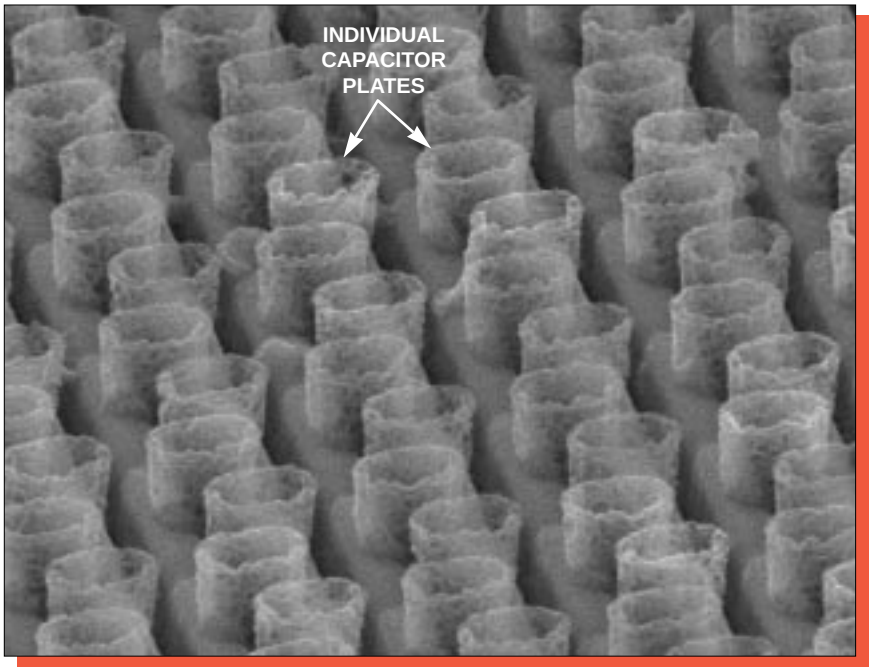


metal 1

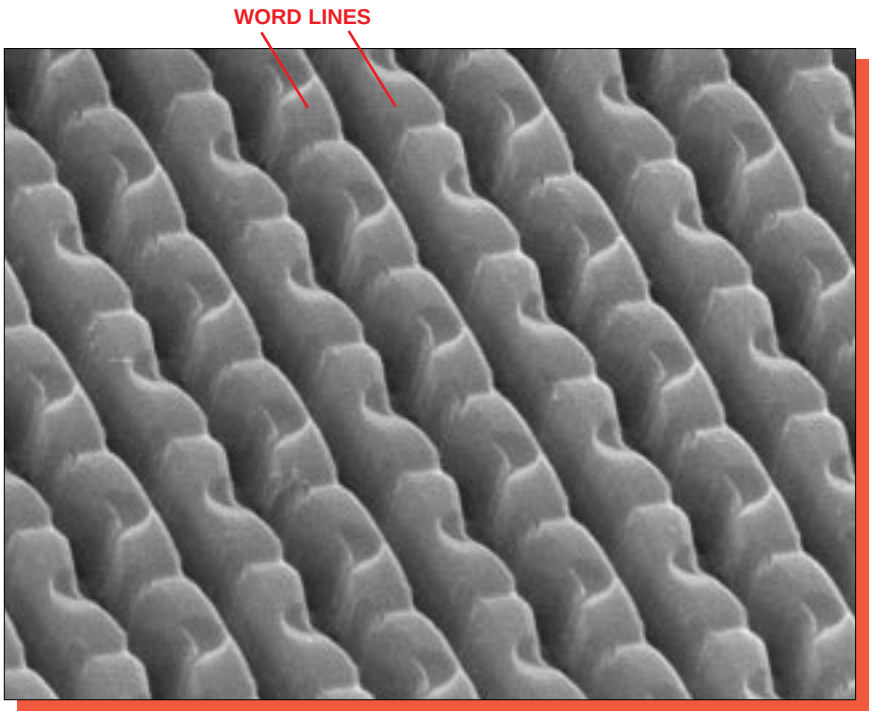


poly 4

Figure 32. Perspective SEM views of the DRAM array. Mag. 20,000x, 55°.

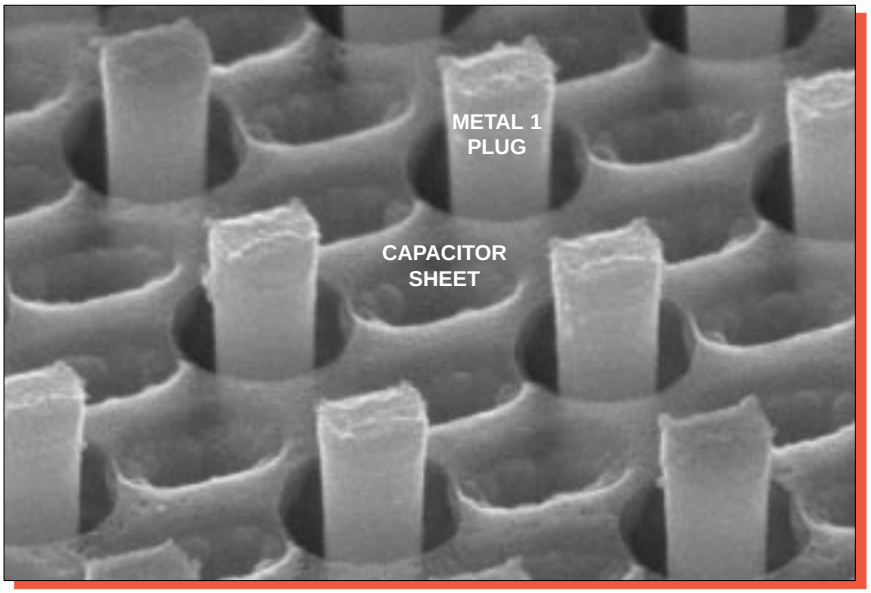


poly 3

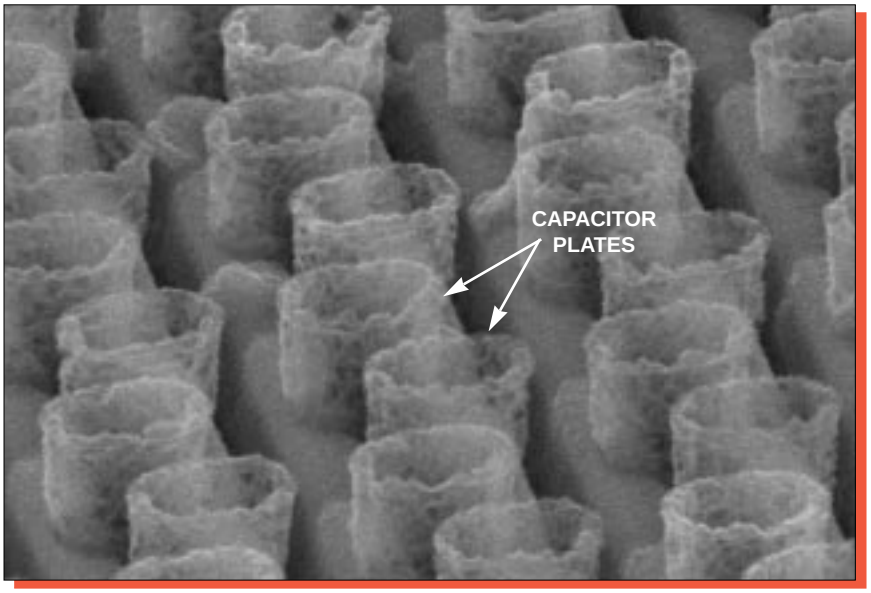


poly 1

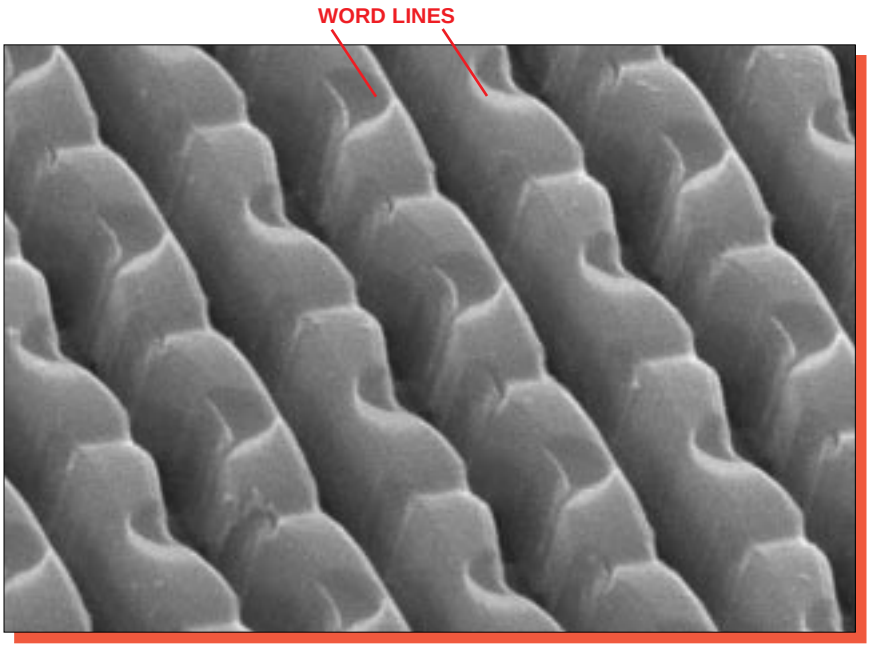
Figure 32a. Perspective SEM views of the DRAM array. Mag. 20,000x, 55°.



poly 4

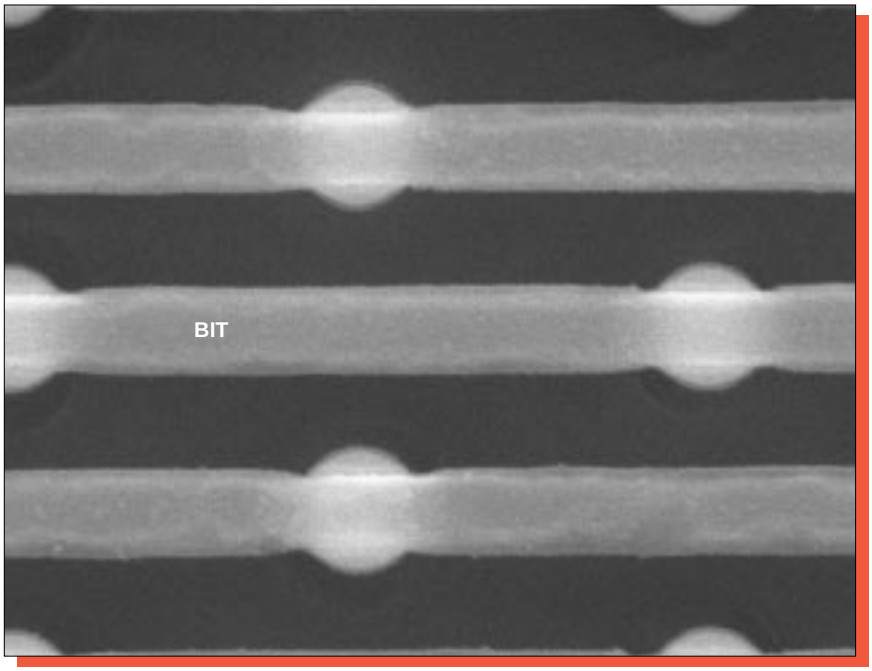


poly 3

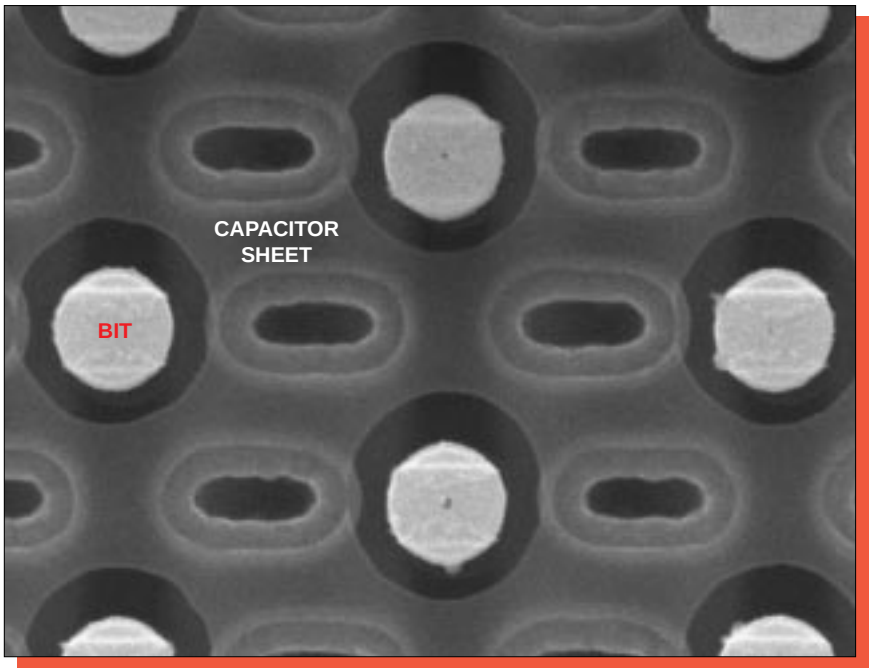


poly 1

Figure 33. Perspective SEM details of the array. Mag. 30,000x, 55°.

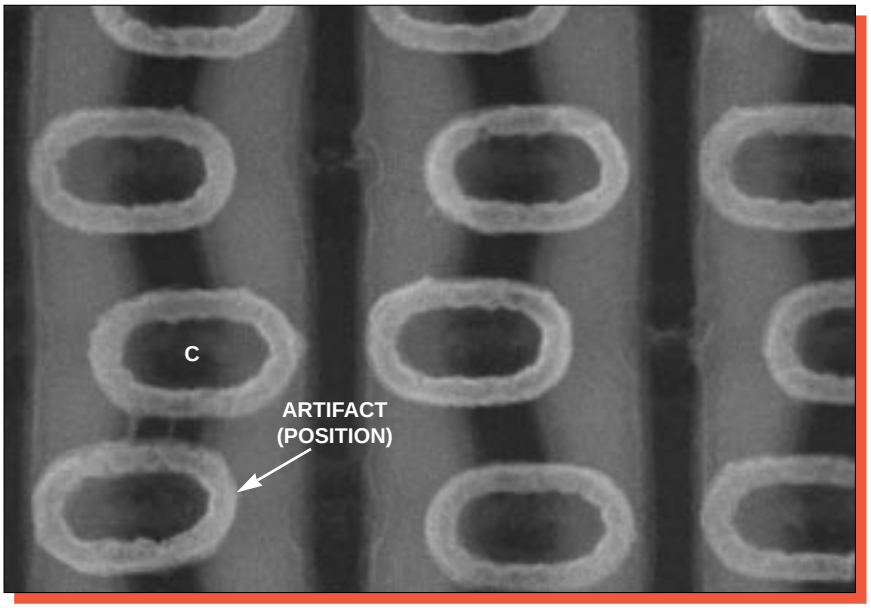


metal 1

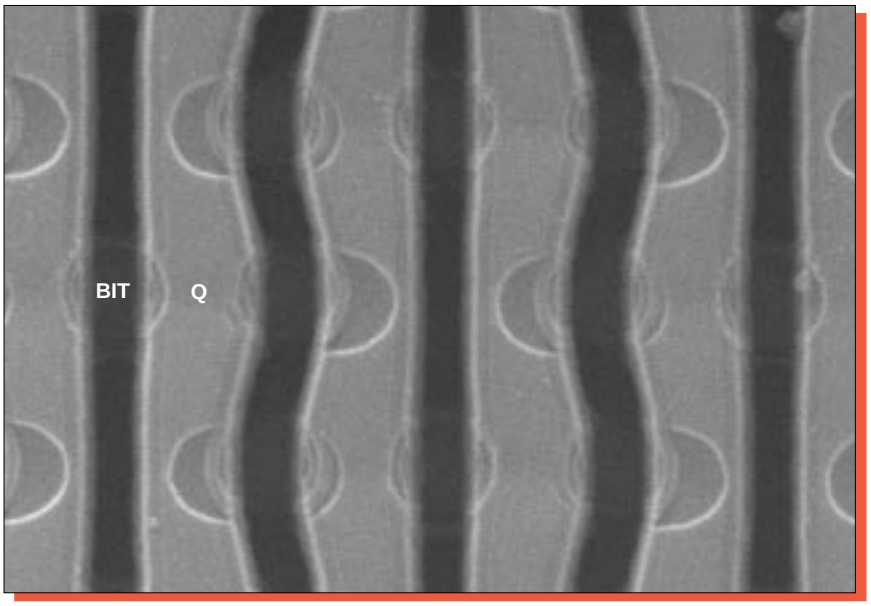


poly 4

Figure 34. Topological SEM views of DRAM cells. Mag. 35,000x, 0°.



poly 3



poly 1

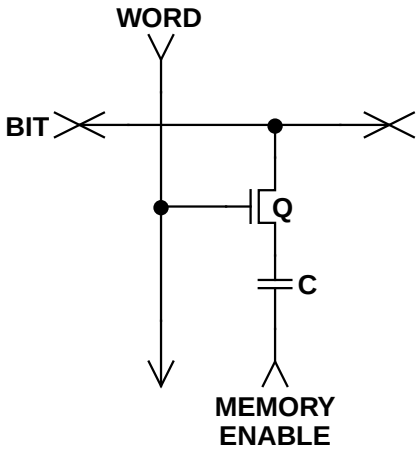
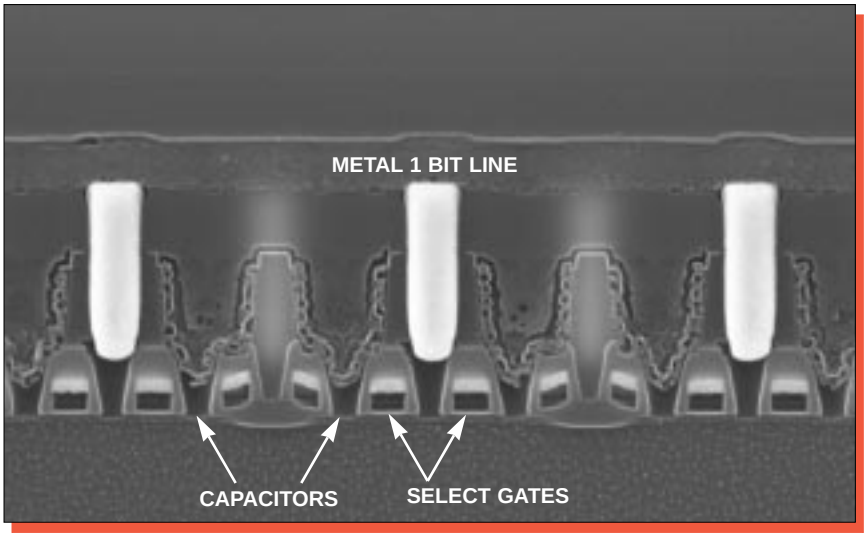
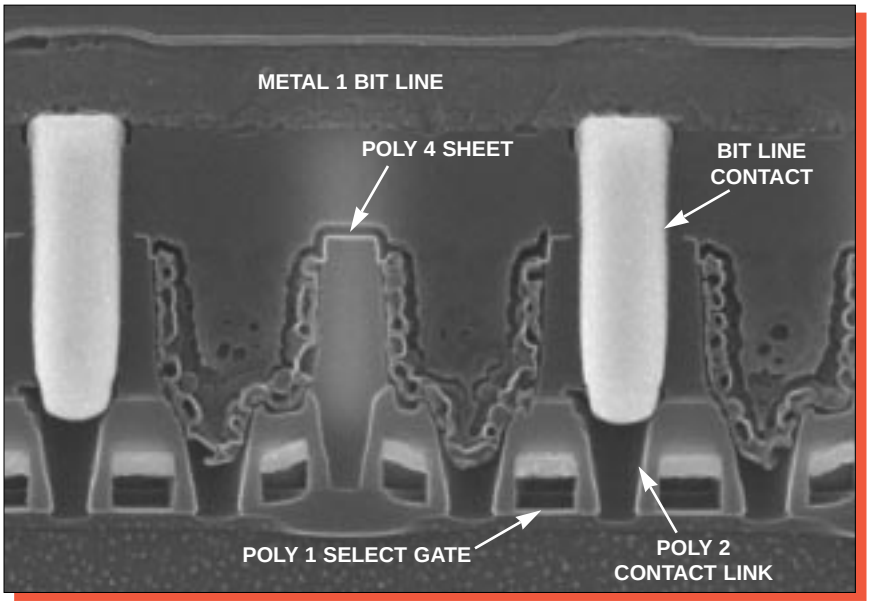


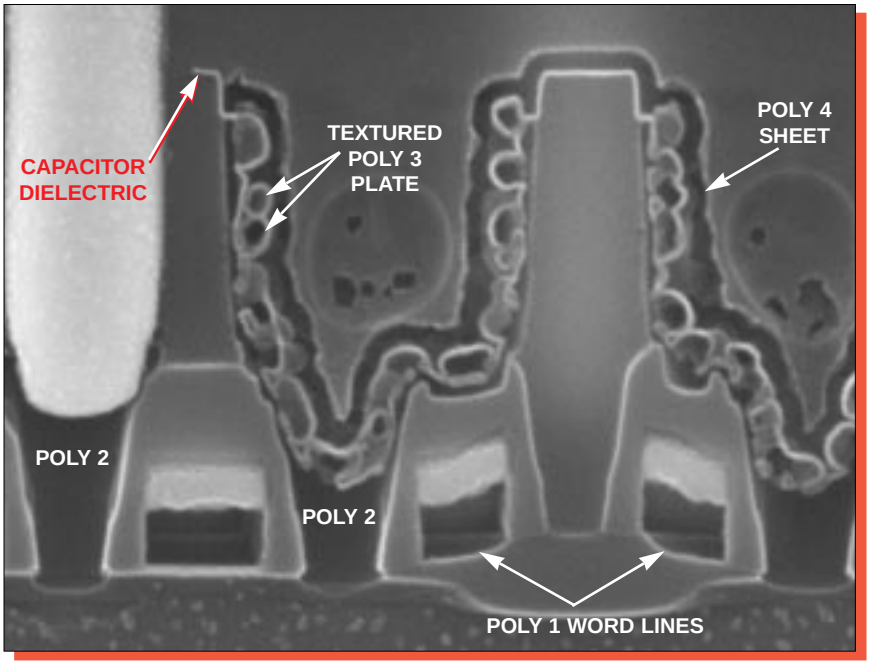
Figure 34a. Topological SEM views of DRAM cells with the schematic.
Mag. 35,000x, 0°.



Mag. 15,000x

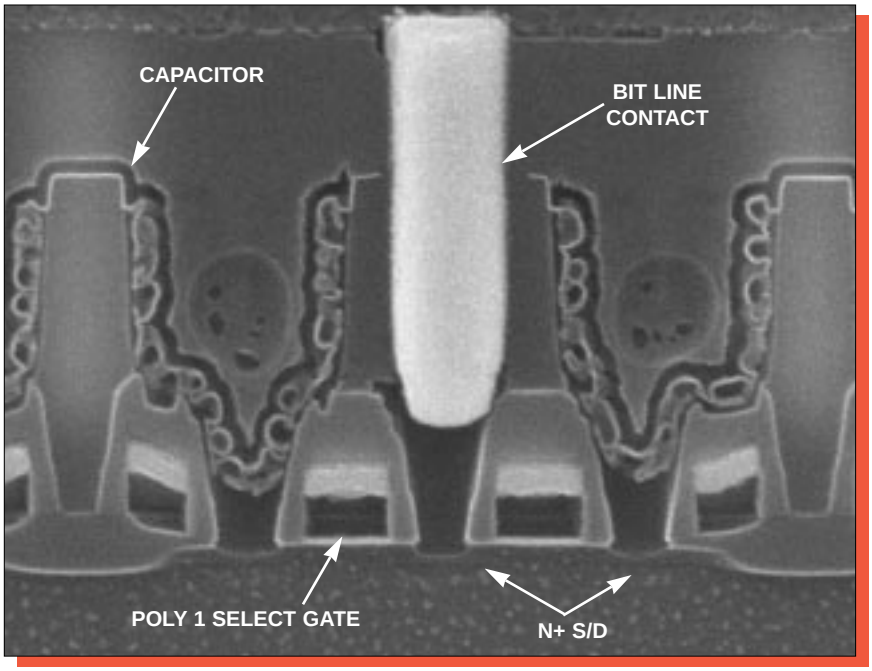


Mag. 26,000x

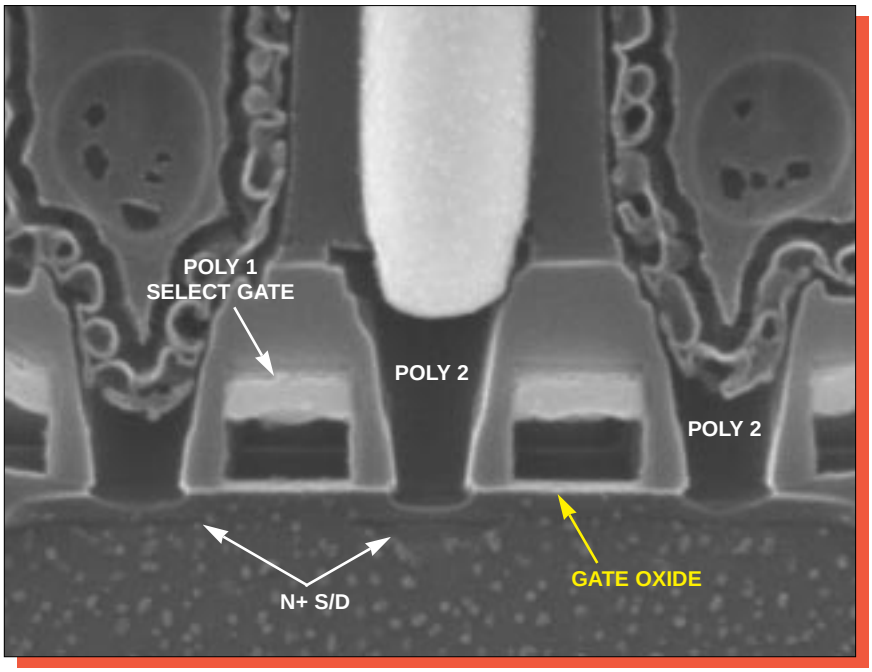


Mag. 50,000x

Figure 35. SEM section views of DRAM cells (parallel to bit lines).

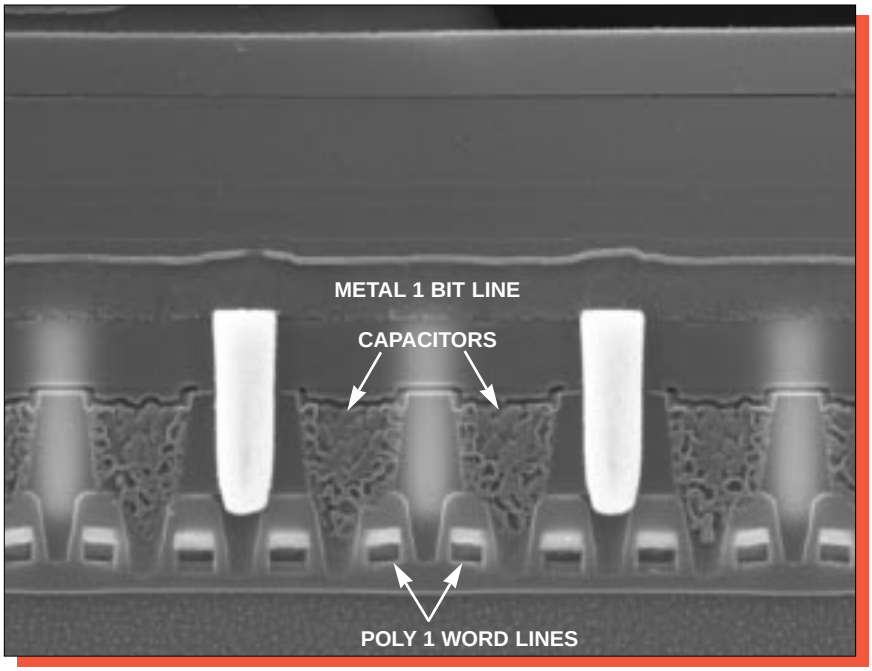


Mag. 35,000x

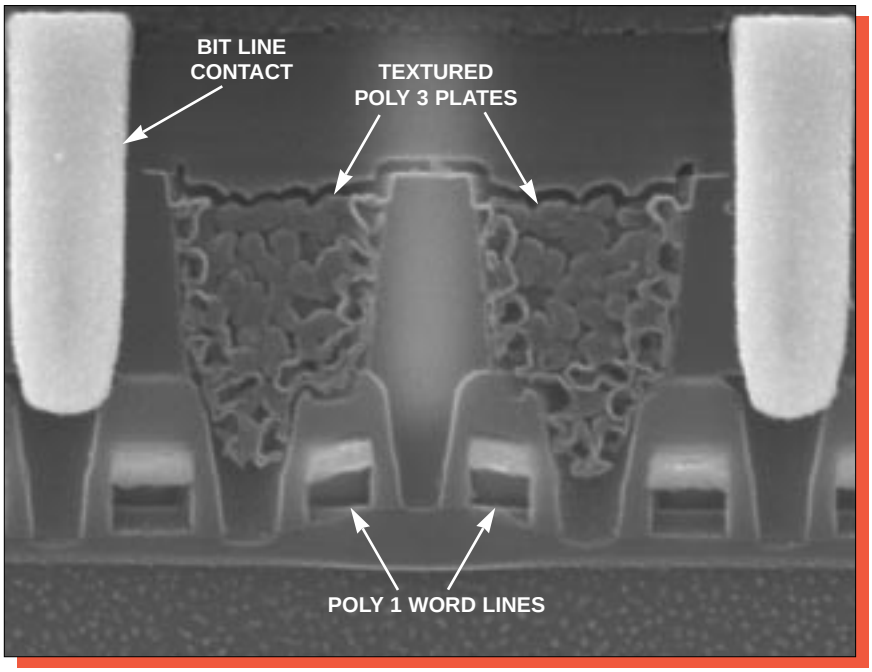


Mag. 52,000x

Figure 35a. SEM section details of DRAM cells.

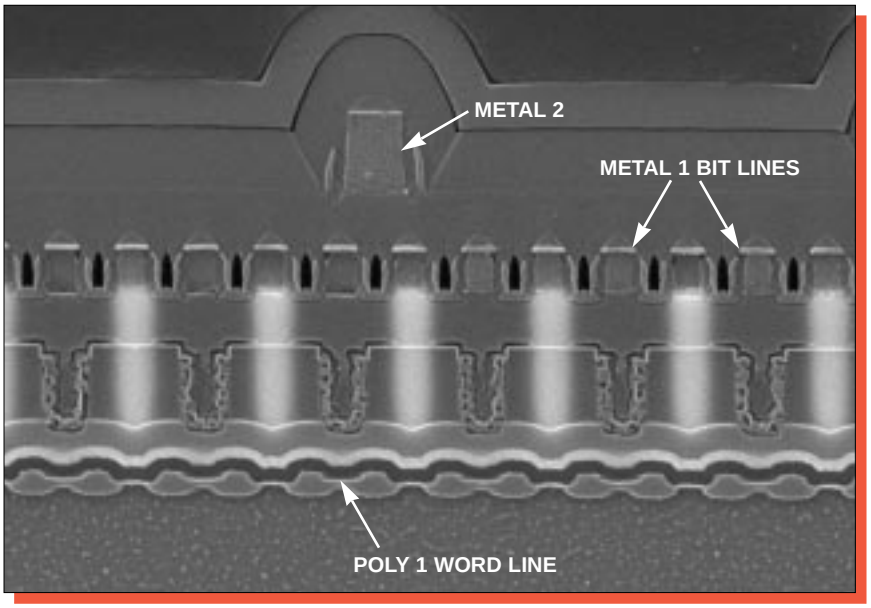


Mag. 17,600x

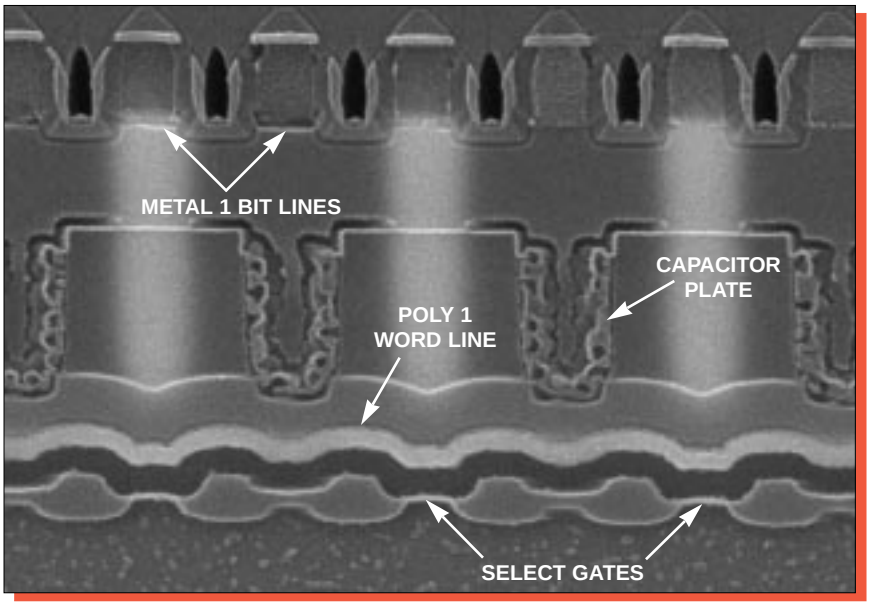


Mag. 34,000x

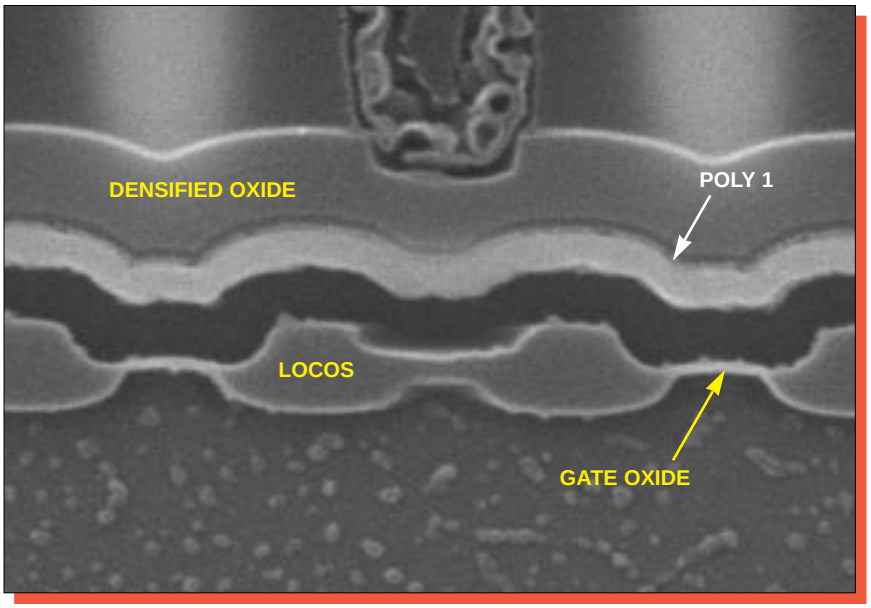
Figure 36. SEM section views of DRAM cells (parallel to bit lines).



Mag. 13,000x

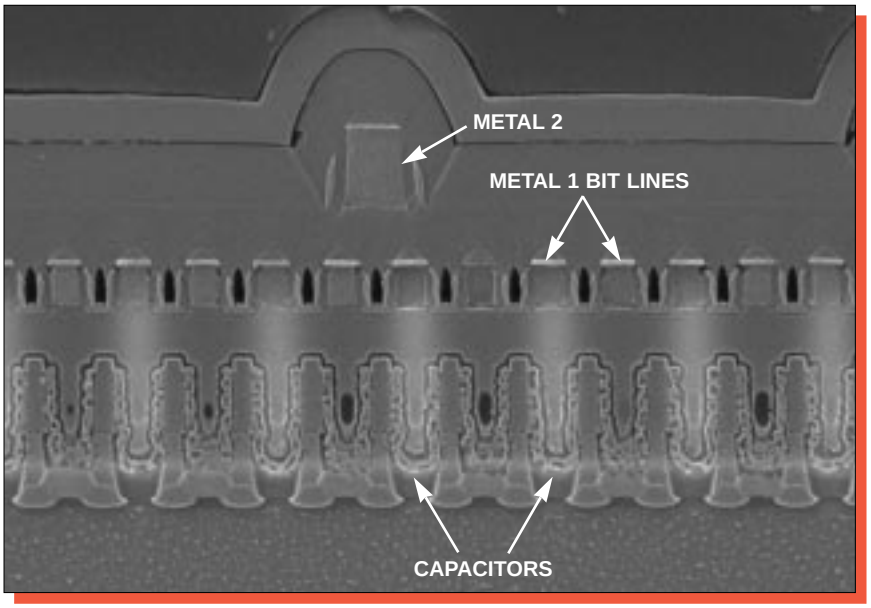


Mag. 26,000x

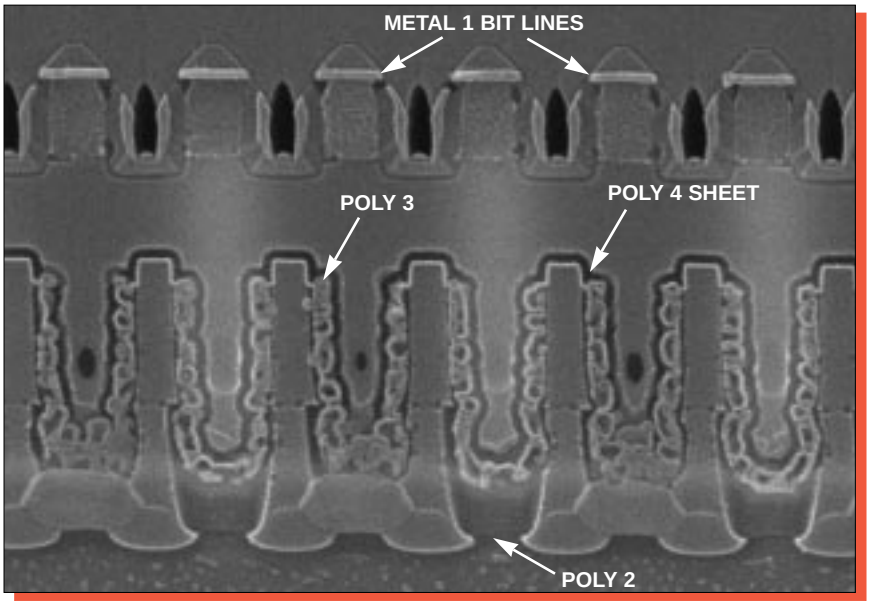


Mag. 52,000x

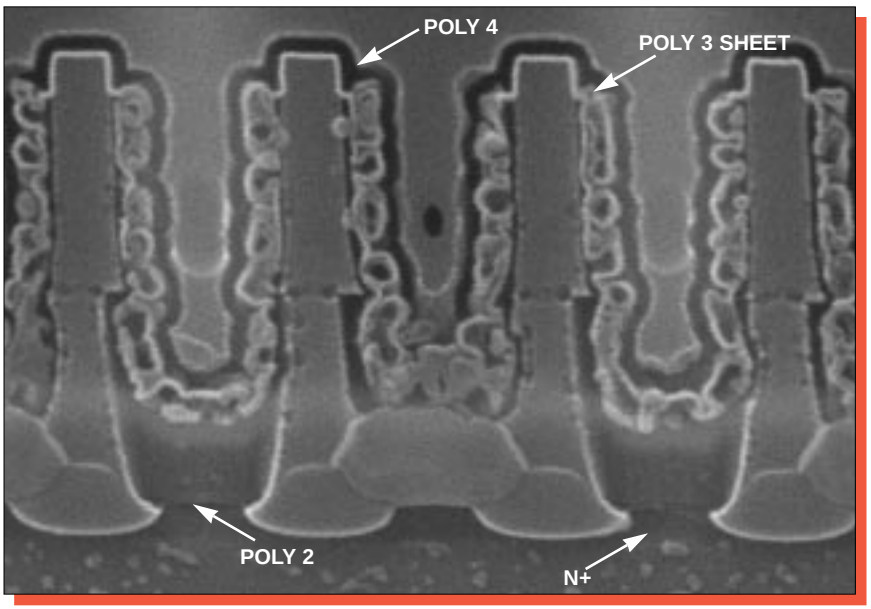
Figure 37. SEM section views of DRAM cells through the word line (perpendicular to bit lines).



Mag. 13,000x

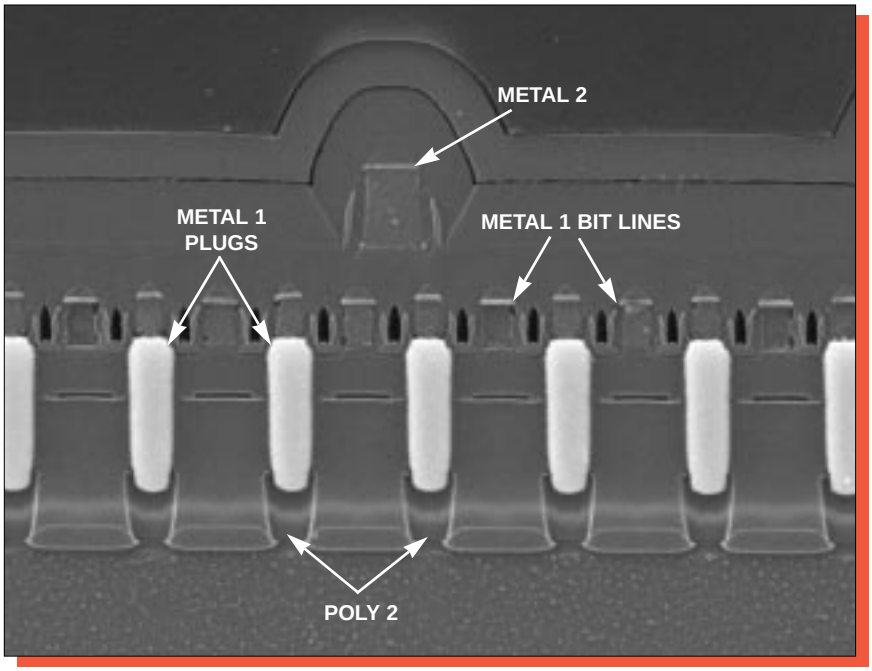


Mag. 26,000x

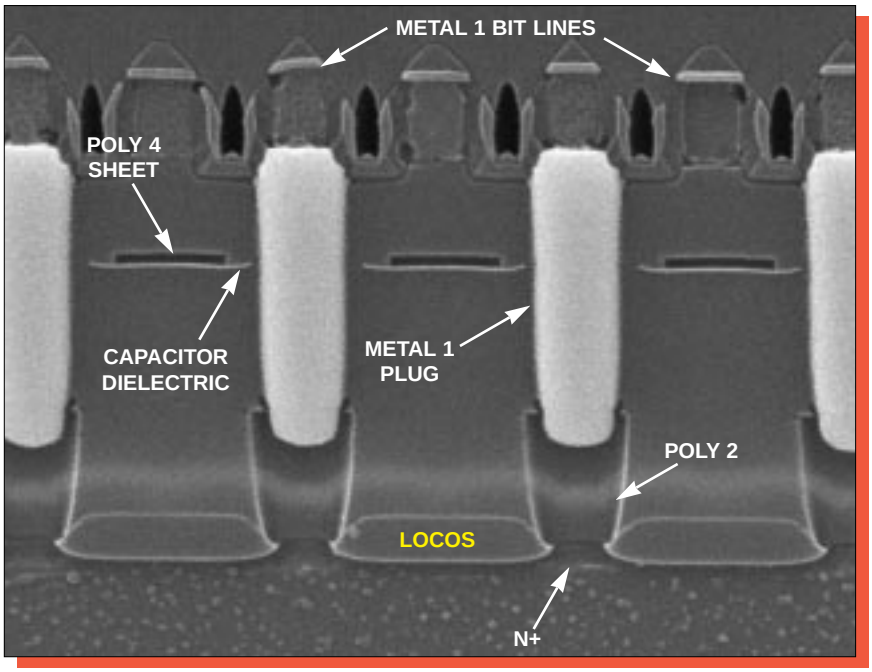


Mag. 45,000x

Figure 38. SEM section views of DRAM capacitors (perpendicular to bit lines).



Mag. 13,000x



Mag. 26,000x

Figure 39. SEM section views of bit line contacts (perpendicular to bit lines).