Construction Analysis

Lattice 3256A-90LM
PLD

Report Number: SCA 9705-538

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INTRODUCTION

This report describes a construction analysis of the Lattice 3256A-90LM Programmable Logic Device (PLD). One decapped device was received for the analysis. The device was date coded 9650.

MAJOR FINDINGS

Questionable Items:[1]

- Aluminum 1 thinning up to 100 percent[2] (Figure 15). Total metal 1 thinning was reduced to 90 percent with the addition of the cap and barrier.

Special Features:

- Sub-micron gate lengths (0.5 micron N-channel and 0.6 micron P-channel).

Design Features:

- Slotted and beveled metal 2 bus lines.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Die Process and Design:

- The device was fabricated using a selective oxidation, twin-well CMOS process in a P-substrate. No epi was used.

- Passivation consisted of a layer of nitride over a layer of silicon-dioxide.

- Metallization employed two levels of metal. Both consisted of aluminum with a titanium-nitride (TiN) cap and barrier. A thin titanium (Ti) adhesion layer was used under metal 1. Standard vias and contacts were used (no plugs).

- The interlevel dielectric consisted of two layers of glass with a spin-on-glass (SOG) between the two layers.

- Pre-metal glass consisted of a layer of reflow glass over various densified oxides. Glass was reflowed prior to contact cuts only.

- A single layer of polycide (tungsten silicide) was used to form one plate of the capacitors and all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A step was present at the edge of the well which indicates a twin-well process was used. No problems were noted.

- Two EEPROM cell arrays were used on the device. Both devices are programmed through an ultra thin (tunnel) oxide window. Metal 2 was used to form the bit lines and distribute ground on array B. Metal 1 was used for interconnect and to distribute ground on array A. Poly was used to form the gates and one plate of the capacitors and gates.

ANALYSIS RESULTS I

Die Process: **Figures 1 - 36**

Questionable Items:[1]

- Aluminum 1 thinning up to 100 percent[2] (Figure 15). Total metal 1 thinning was reduced to 90 percent with the addition of the cap and barrier.

Special Features:

- Sub-micron gate lengths (0.5 micron N-channel and 0.6 micron P-channel).

Design features:

- Slotted and beveled metal 2 bus lines.

General items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P-substrate. No epi was used.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage of contamination was found.

- Die coat: No die coat was present.

- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS I (continued)

- Metallization: Two levels of metal. Both consisted of aluminum with titanium-nitride (TiN) caps and barriers. A thin titanium (Ti) adhesion layer was present beneath metal 1. Standard vias and contacts were used (no plugs).

- Metal patterning: Both metal levels were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in the metal of either layer. Contacts and vias were completely surrounded by metal. No silicon nodules were noted following removal of either metal layer.

- Metal step coverage: Metal 2 aluminum thinned up to 75 percent at vias. Total metal 2 thinning was reduced to 65 percent with the addition of the cap and barrier. Metal 1 aluminum thinned up to 100 percent at some contacts. Total metal 1 thinning was reduced to 90 percent with the addition of the cap and barrier.

- Interlevel dielectric: Two layers of silicon-dioxide were present under metal 2 (interlevel dielectric). The first layer had been subjected to an etchback process. A layer of spin-on-glass (SOG) was present between the layers for planarization purposes.

- Pre-metal glass: A layer of reflow glass over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Contact and via cuts were defined by a two-step process. No over-etching of the contacts or vias was noted.

- A single layer of polycide (tungsten silicide) was used to form all gates on the die and one plate of the capacitors. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry-etch of normal quality.

ANALYSIS RESULTS I (continued)

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Local oxide (LOCOS) isolation was used with a step present at the well boundary indicating that a twin-well process was employed.

- Two EEPROM cell arrays were used on the device. Both use the same design (but different layout) and are programmed through an ultra thin (tunnel) oxide window. Metal 2 was used to form the bit lines and distribute ground on array B. Metal 1 was used for interconnect and to distribute ground in array A. Poly was used to form the gates and one plate of the capacitors. Cell size (array A): 9.0 x 9.5 microns. Cell size (array B): 13 x 36 microns

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection

SEM of passivation

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity*	N
Metal registration	N
Contact coverage	N
Contact registration	N

**Even with the isolated spots where metal 1 thins 100 percent we judge adequate metal remains around the contact perimeter.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIAL ANALYSIS

Final passivation:	A layer of silicon-nitride over a layer of glass.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier on a thin titanium (Ti) adhesion layer.
Silicide (poly):	Tungsten (W).

HORIZONTAL DIMENSIONS

Die size:	7.4 x 9.2 mm (290 x 364 mils)
Die area:	68 mm^2 (105,560 $mils^2$)
Min pad size:	0.1 x 0.1 mm (4.0 x 4.0 mils)
Min pad window:	0.09 x 0.09 mm (3.8 x 3.8 mils)
Min pad space:	28 microns
Min metal 2 width:	1.1 micron
Min metal 2 space:	1.1 micron
Min metal 2 pitch:	2.2 microns
Min metal 1 width:	0.8 micron
Min metal 1 space:	0.8 micron
Min metal 1 pitch:	1.6 micron
Min via:	0.85 micron
Min contact:	0.8 micron
Min polycide width:	0.5 micron
Min polycide space:	0.7 micron
Min gate length* - (N-channel):	0.5 micron
- (P-channel):	0.6 micron
Cell pitch (array A):	9.0 x 9.5 microns
Cell size (array A):	85.5 $microns^2$
Cell pitch (array B):	13 x 35 microns
Cell size (array B):	455 $microns^2$

**Physical gate length*

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (20 mils)

Layers:

Passivation 2:	0.45 micron
Passivation 1:	0.25 micron
Metal 2 - cap:	0.05 micron (approximate)
- aluminum:	0.8 micron
- barrier:	0.12 micron
Interlevel dielectric- glass 2:	0.4 micron
- glass 1:	0.3 micron (average)
Metal 1 - cap:	0.07 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.12 micron
Pre-metal dielectric:	0.75 micron (average)
Oxide on polycide:	0.15 micron
Polycide - silicide:	0.1 micron
- poly:	0.12 micron
Local oxide:	0.45 micron
N+ S/D:	0.13 micron
P+ S/D:	0.2 micron
N-well:	4.0 microns
P-well:	4.0 microns

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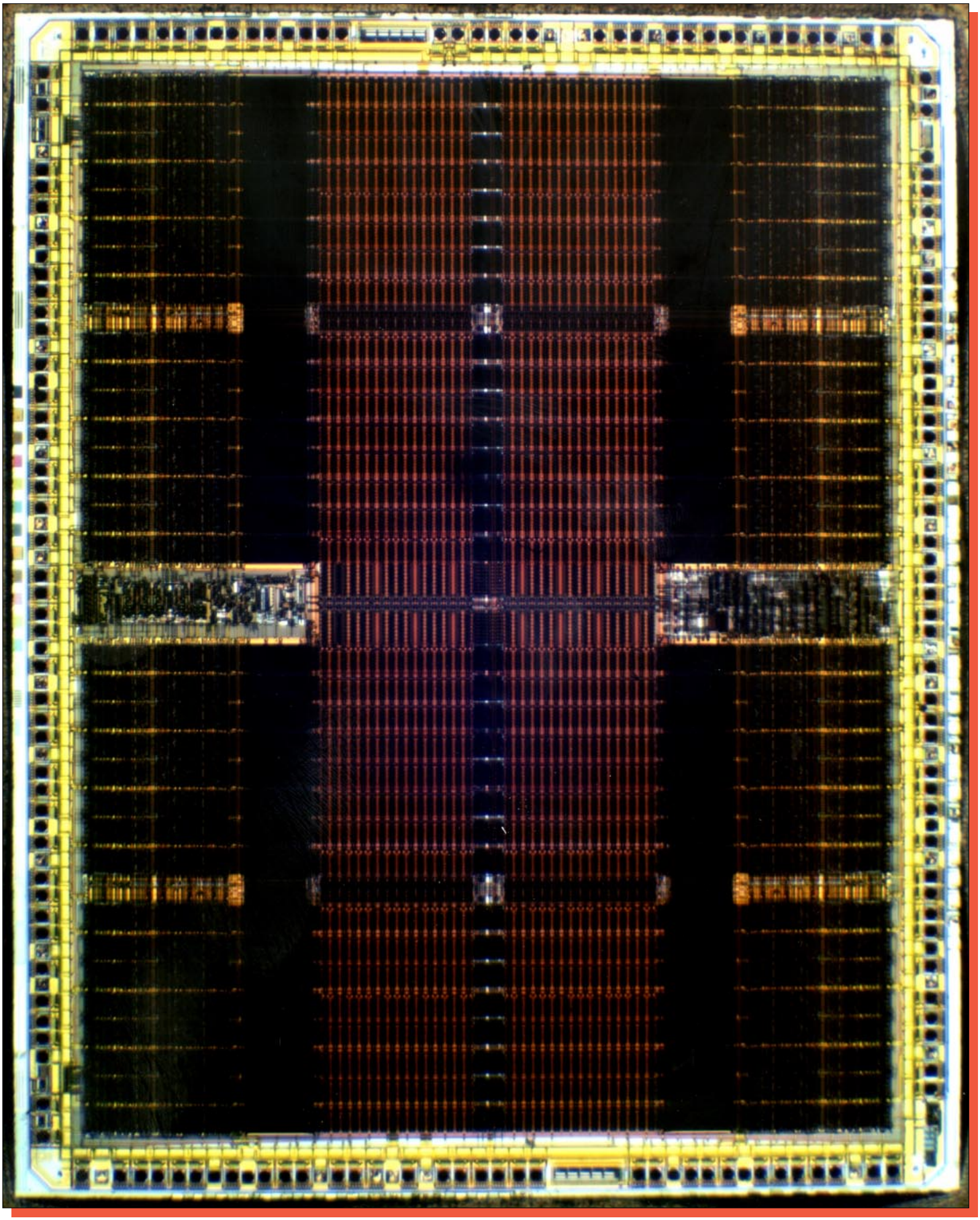


Figure 1. Whole die photograph of the Lattice 3256A-90LM. Mag. 25x.

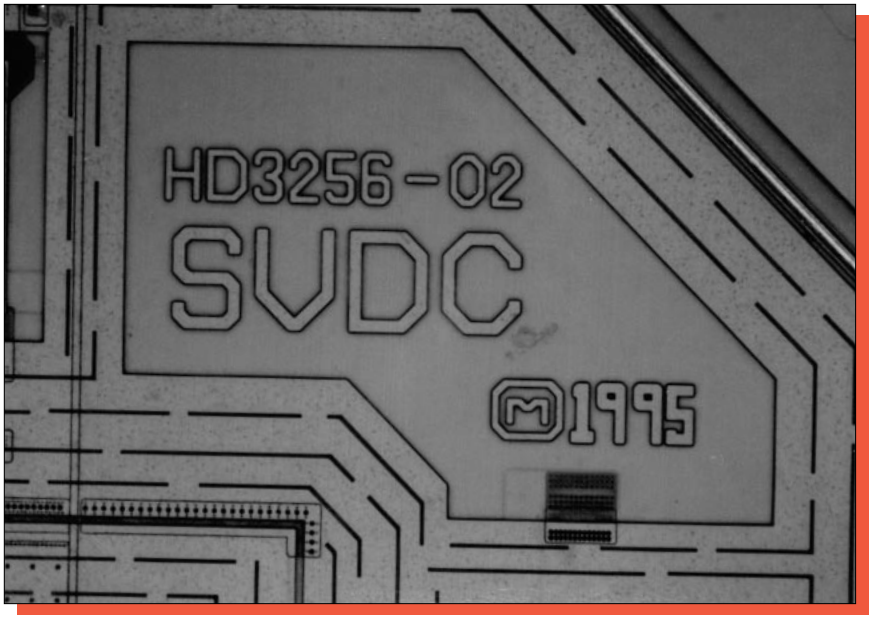


Figure 2. Markings from the die surface. Mag. 320x.

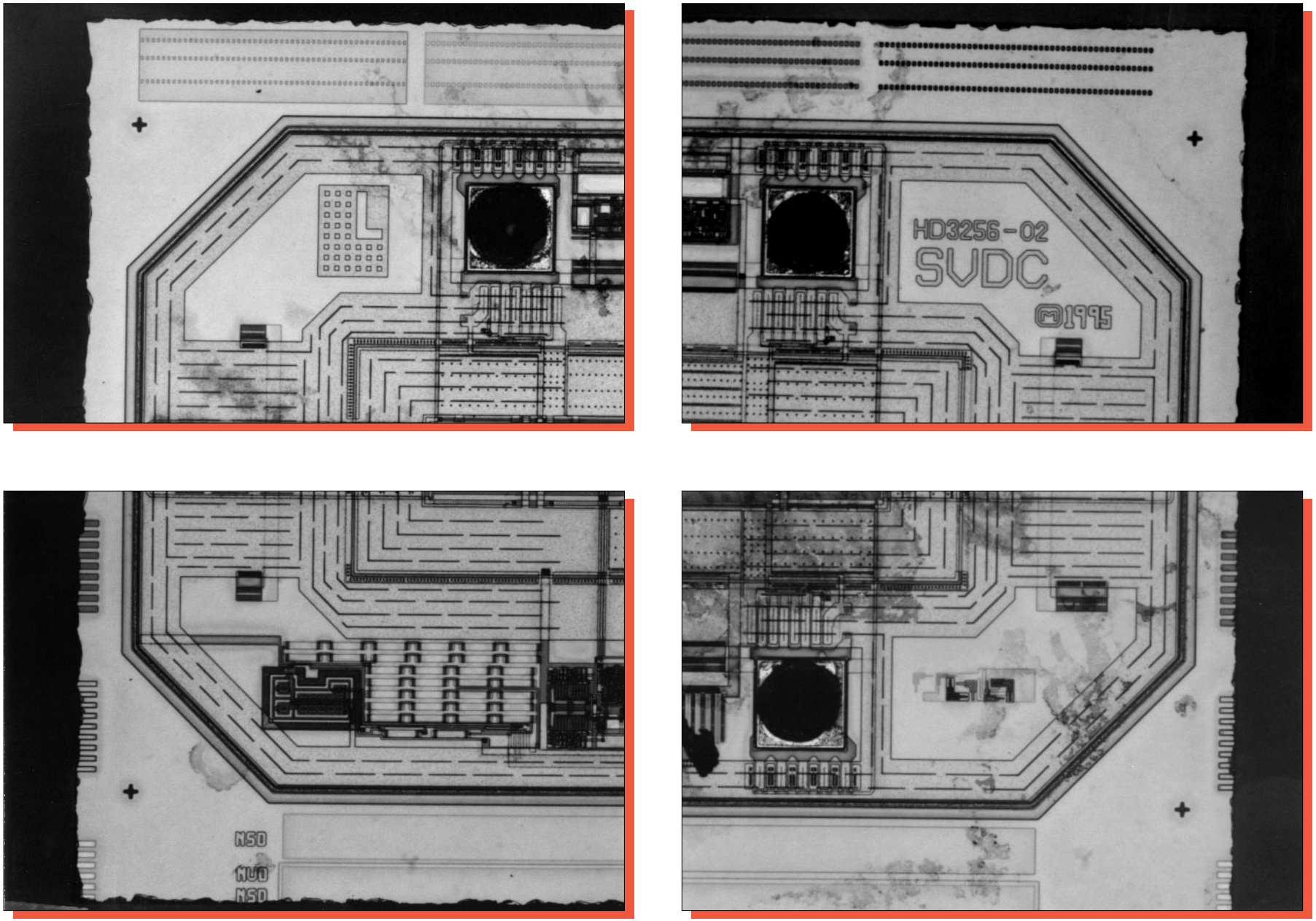
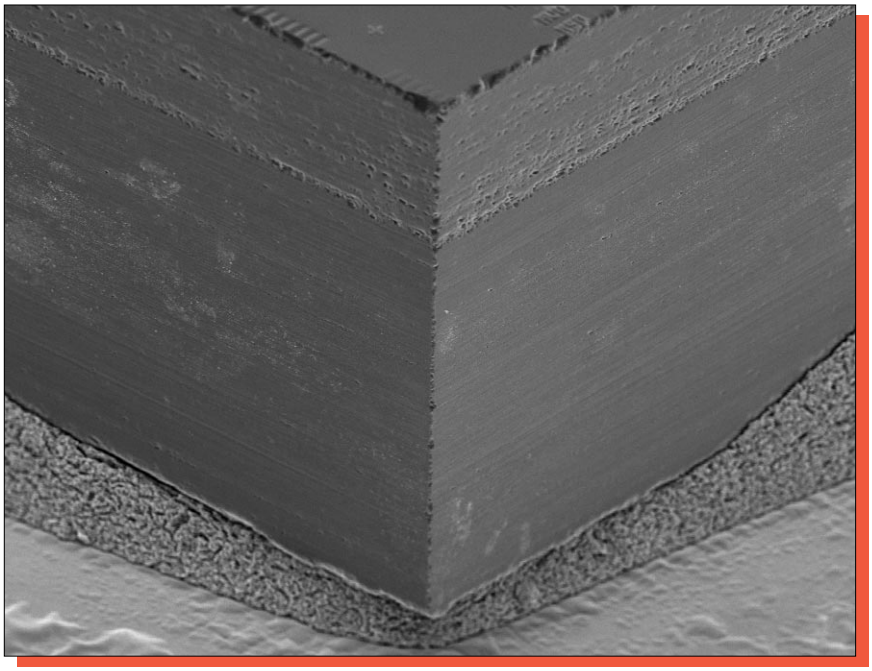
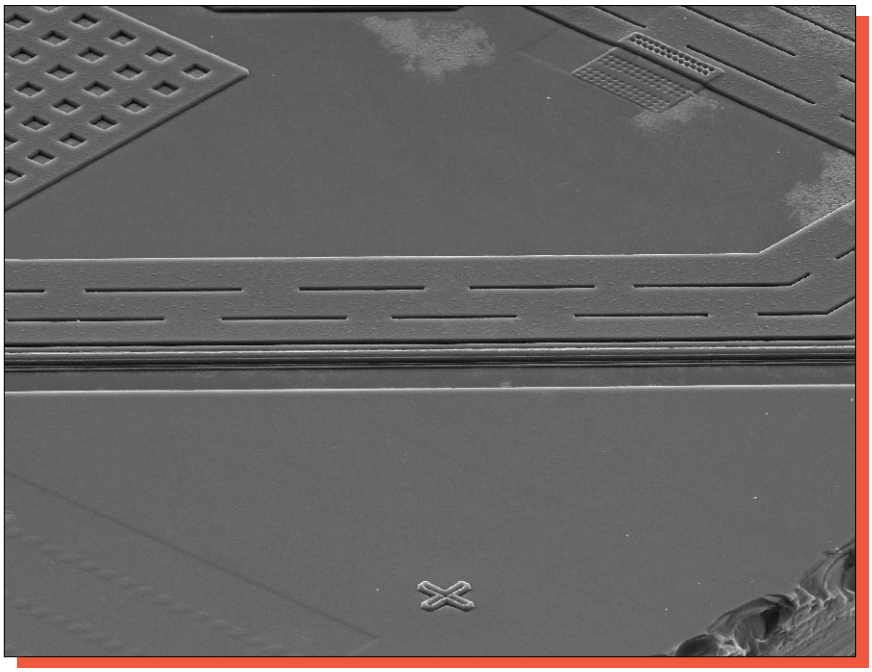


Figure 3. Optical views of the die corners on the Lattice 3256A-90LM. Mag. 160x.

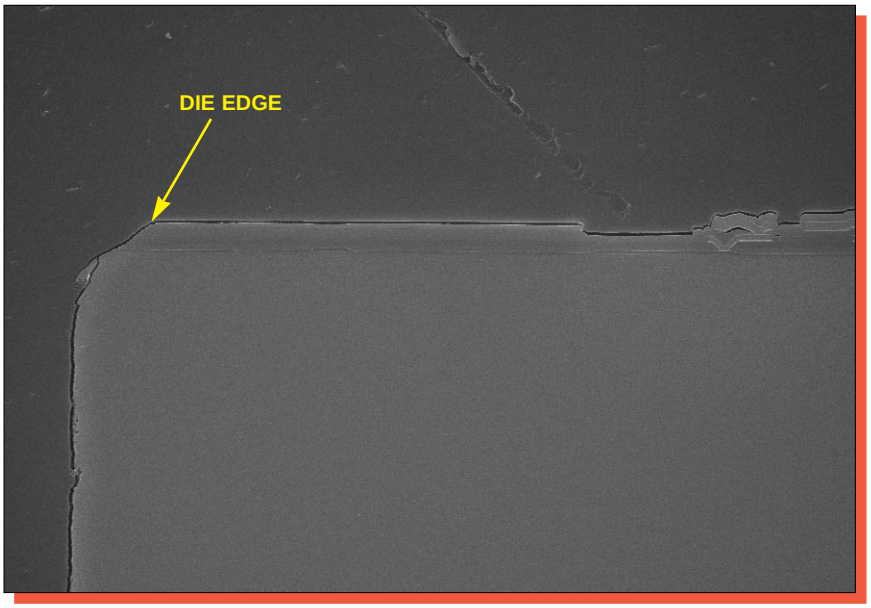


Mag. 170x

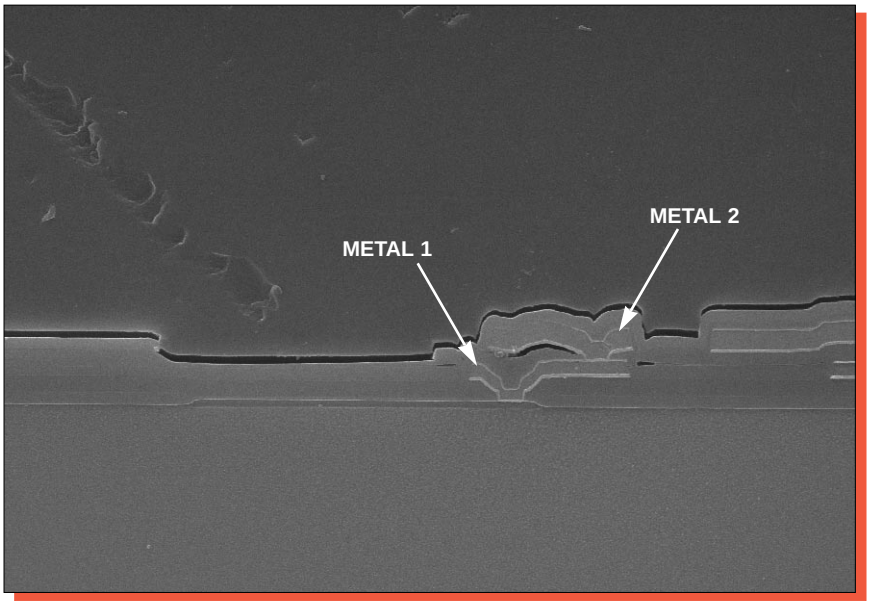


Mag. 600x

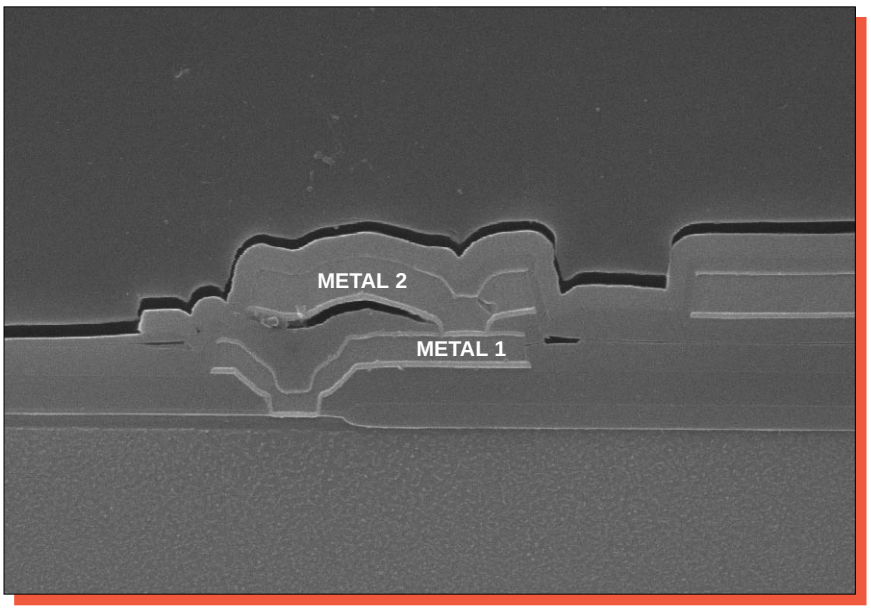
Figure 4. Perspective SEM views of dicing and edge seal. 60°.



Mag. 1400x

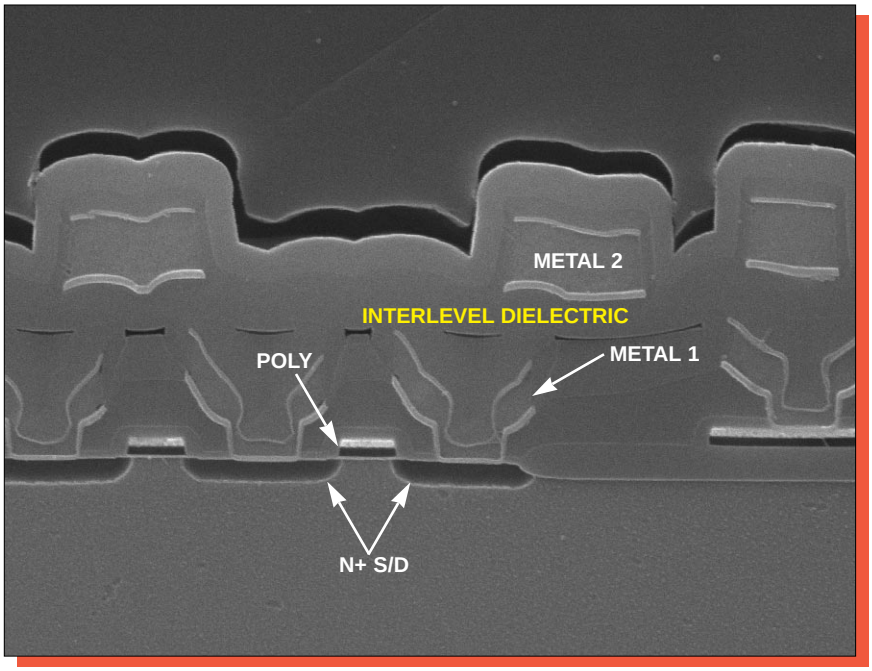


Mag. 3200x



Mag. 6500x

Figure 5. SEM section views of the edge seal.



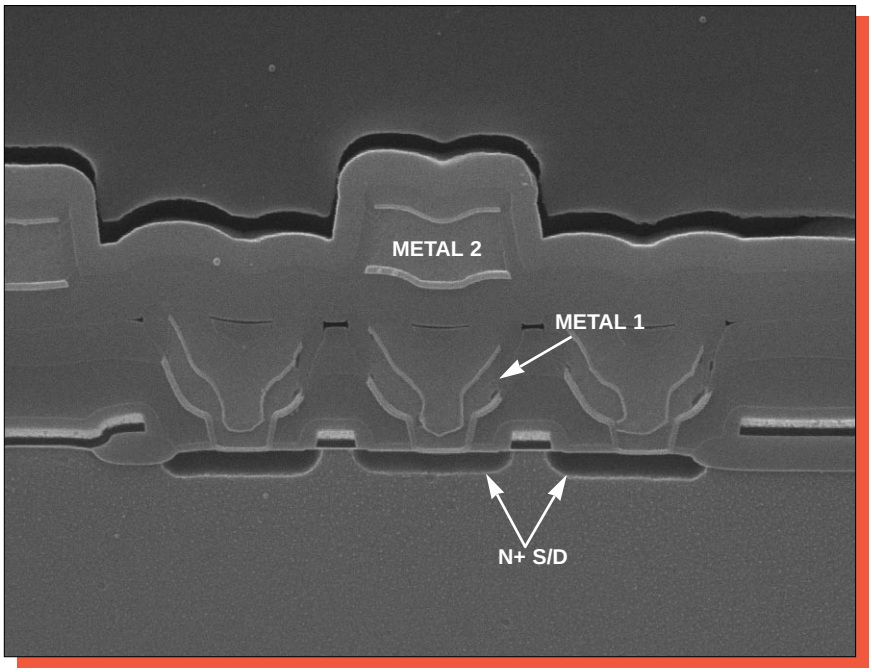
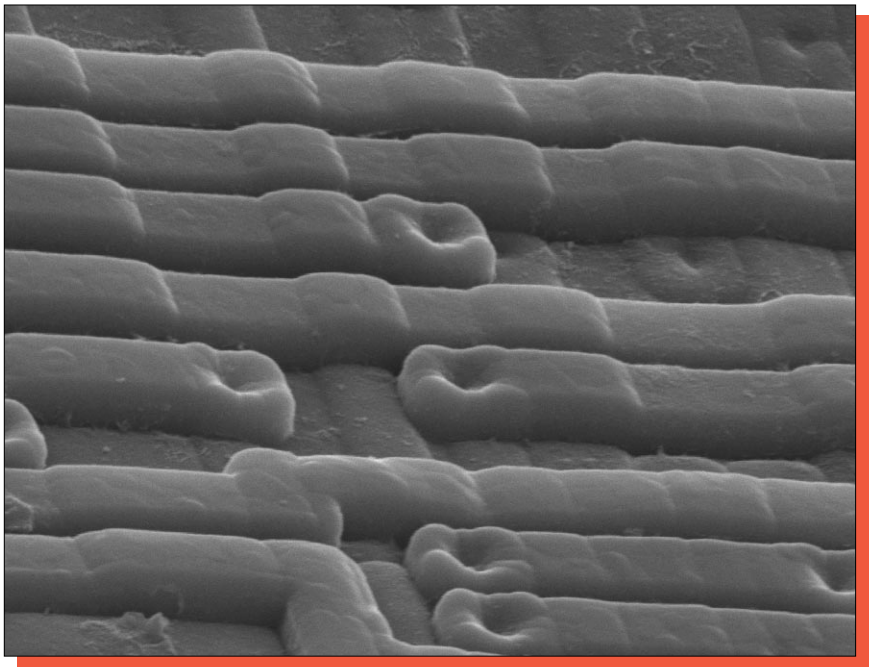
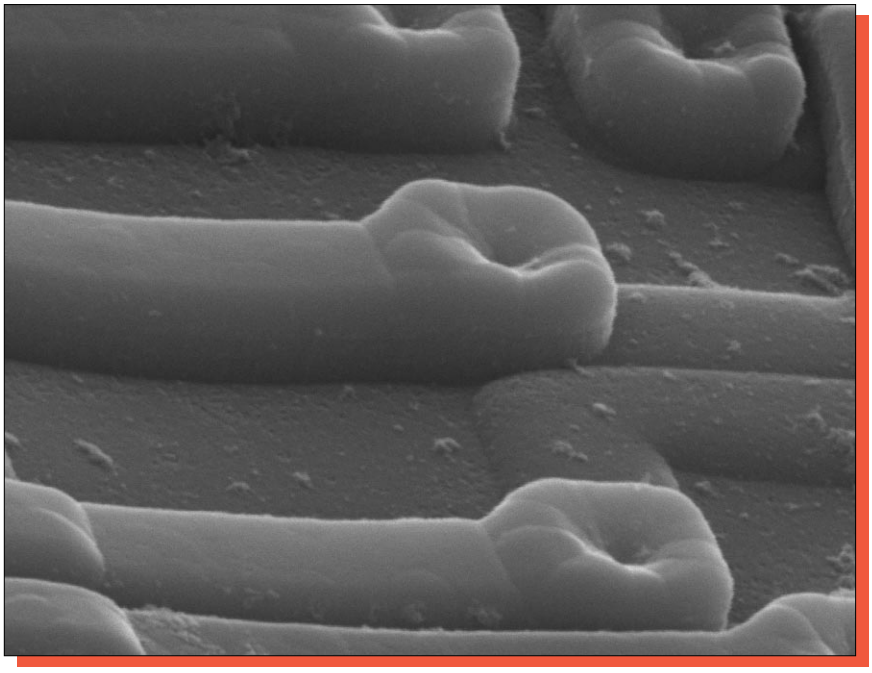


Figure 6. SEM section views of general device structure. Mag. 10,000x.

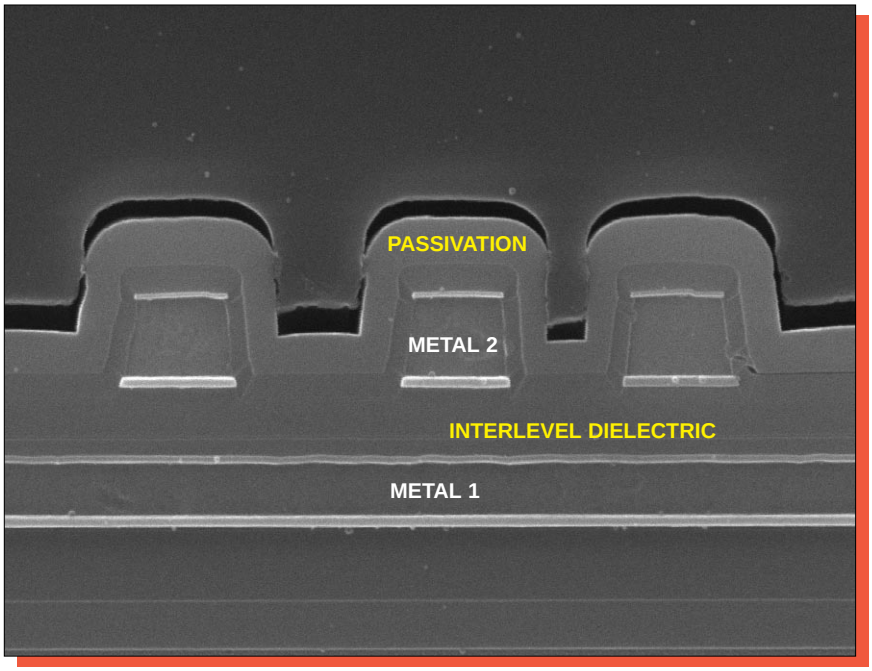


Mag. 5200x

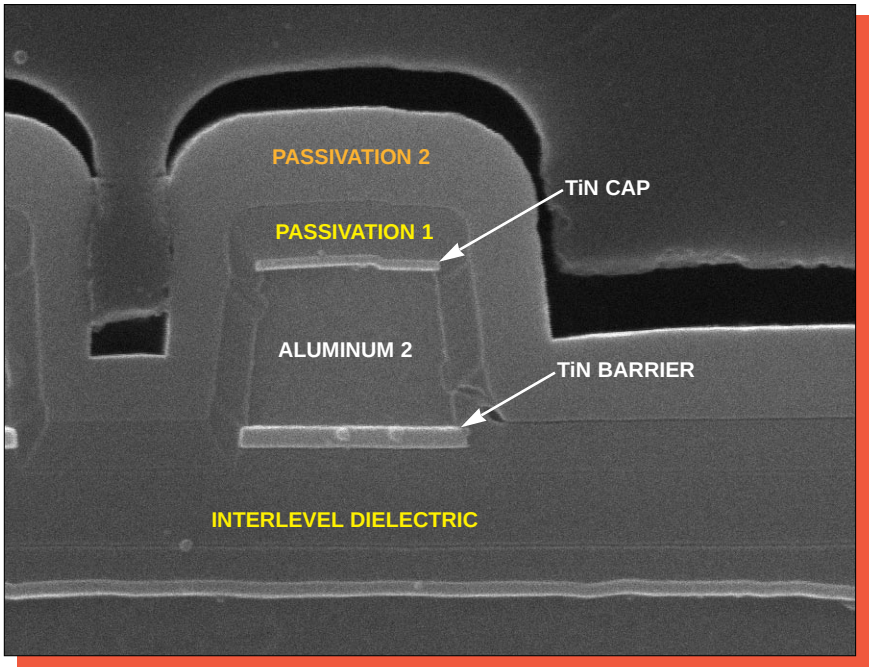


Mag. 10,000x

Figure 7. Perspective SEM views of overlay passivation coverage. 60°.

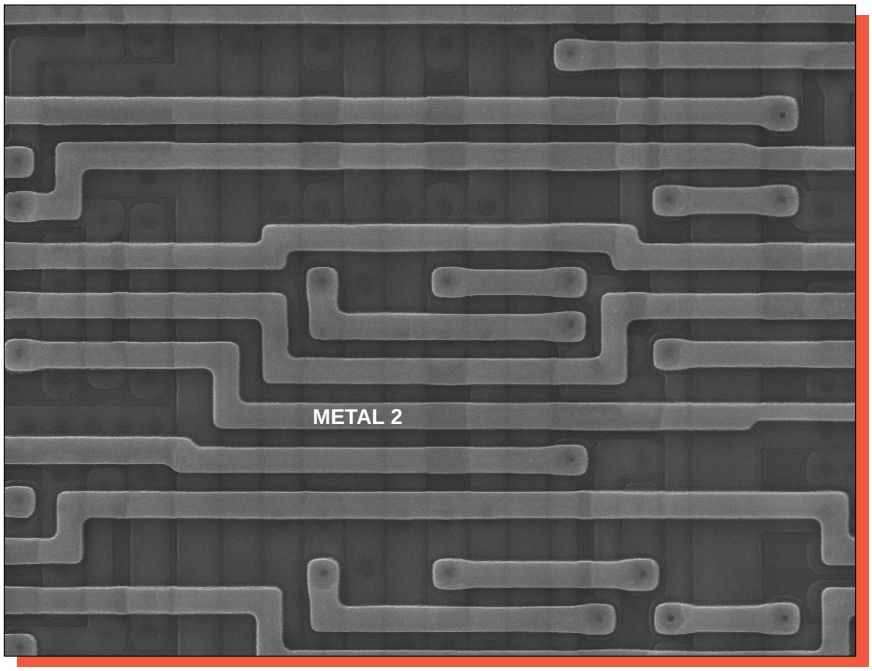


Mag. 13,000x

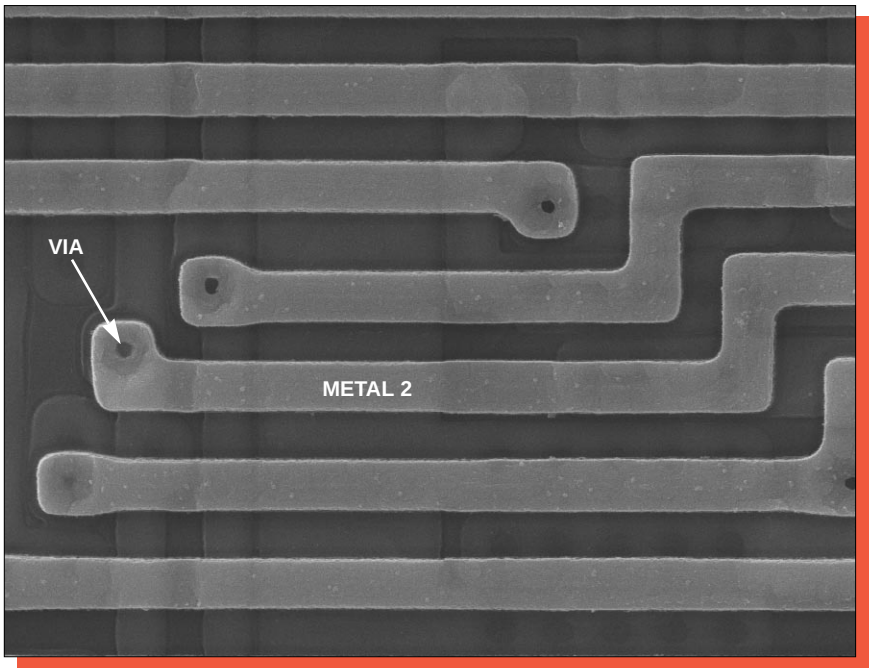


Mag. 26,000x

Figure 8. SEM section views of metal 2 line profiles.

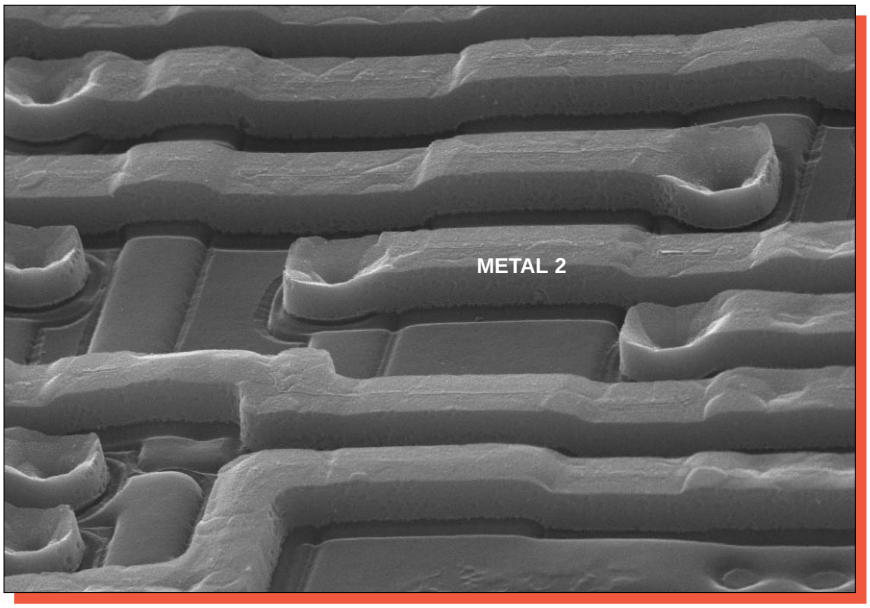


Mag. 2000x

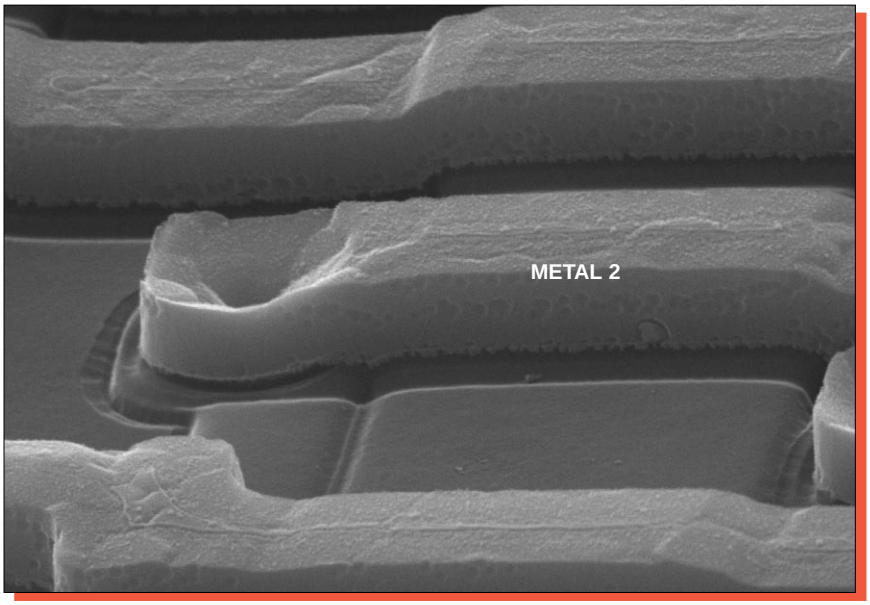


Mag. 4000x

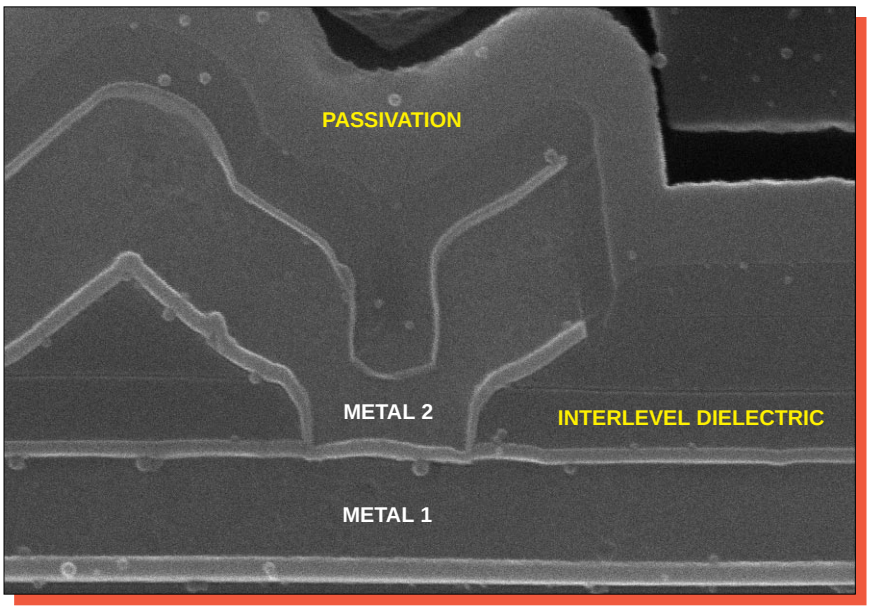
Figure 9. Topological SEM views of metal 2 patterning.



Mag. 6500x

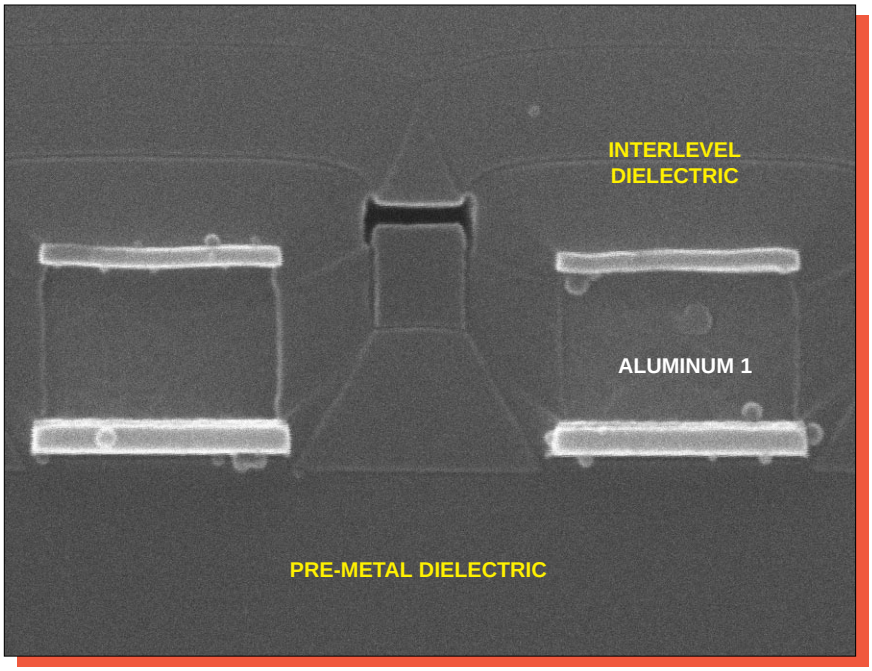


Mag. 13,000x

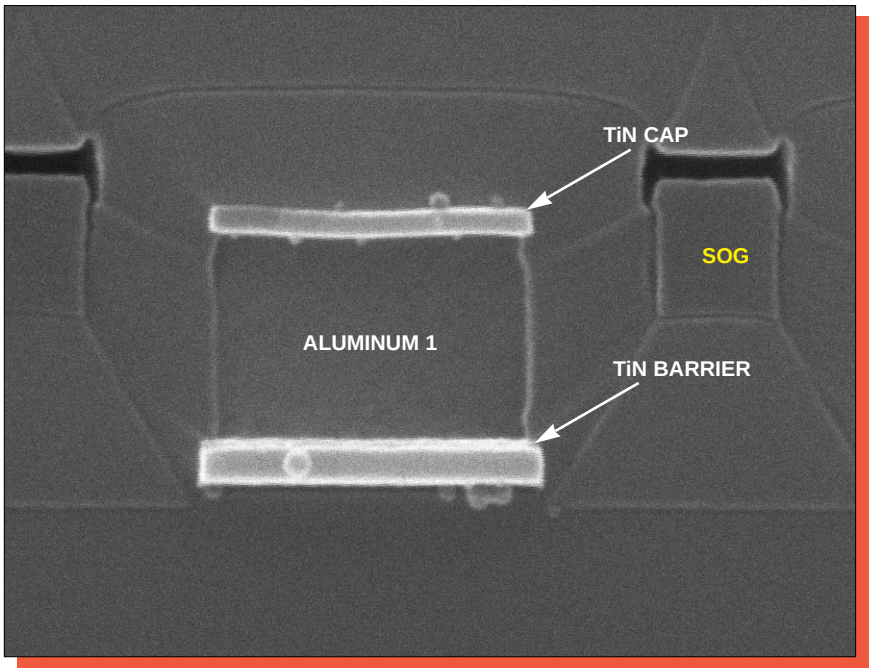


Mag. 26,000x

Figure 10. SEM views of metal 2 coverage and via.

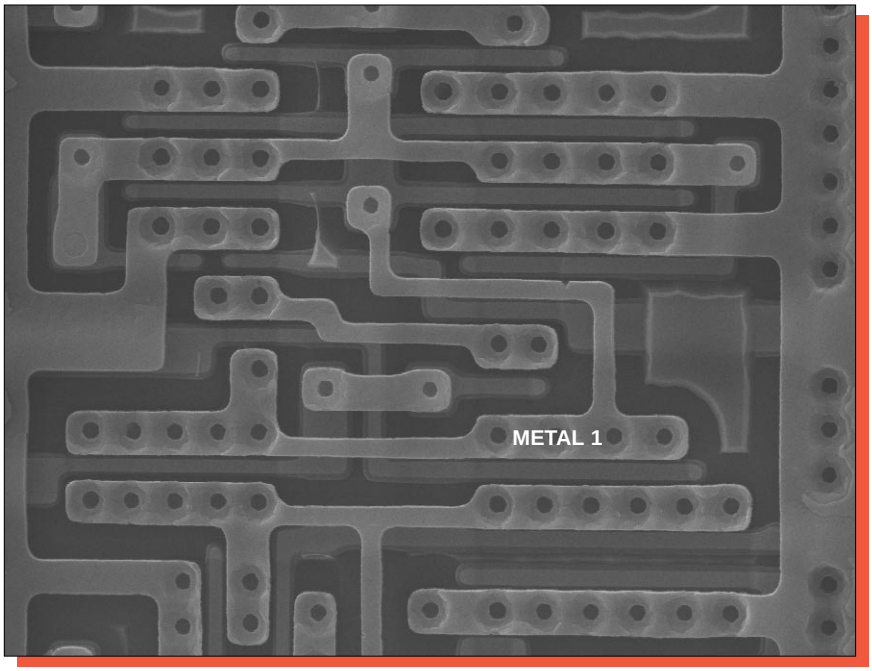


Mag. 40,000x

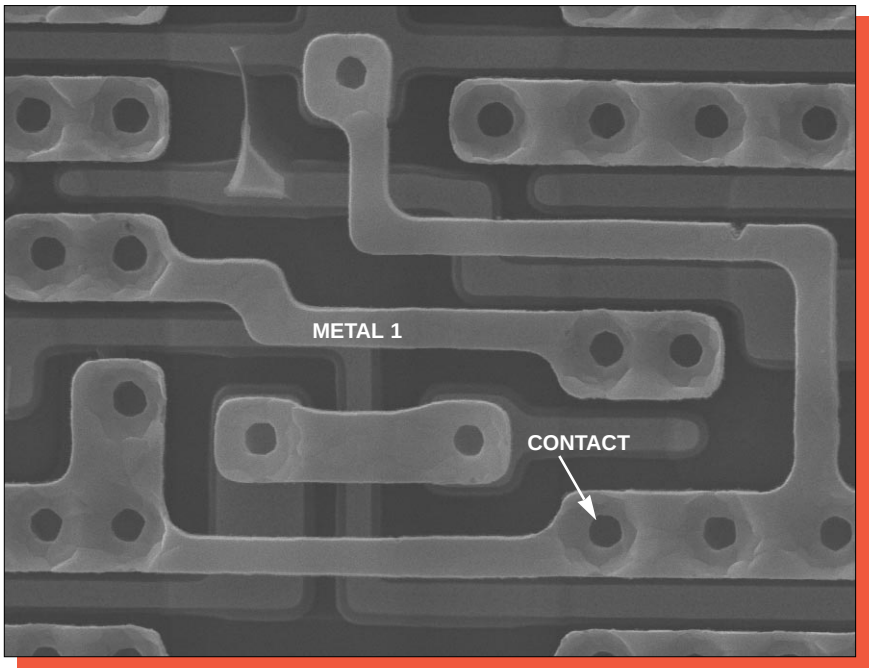


Mag. 52,000x

Figure 11. SEM section views of metal 1 line profiles.

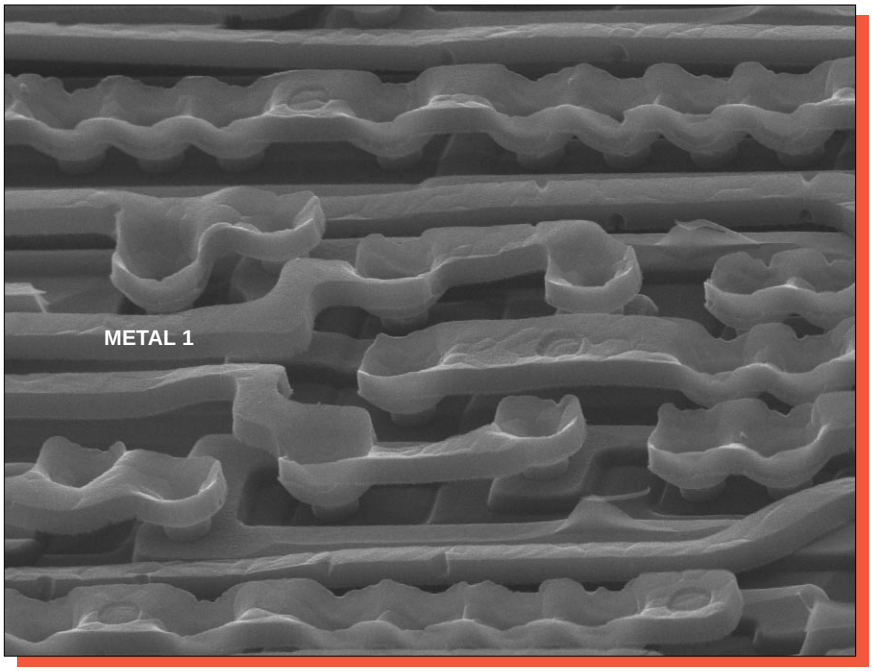


Mag. 3200x

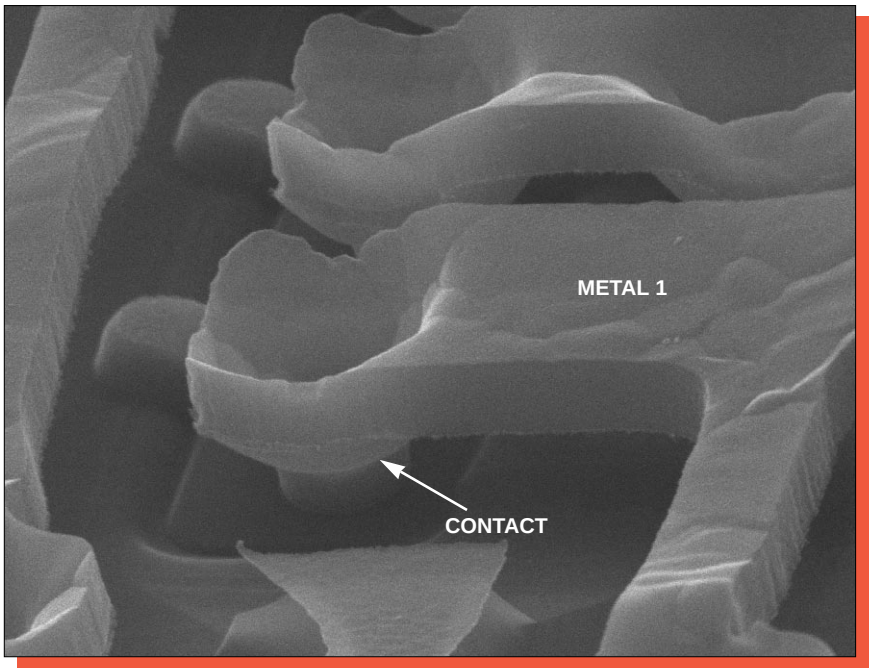


Mag. 6500x

Figure 12. Topological SEM views of metal 1 patterning. 0°.

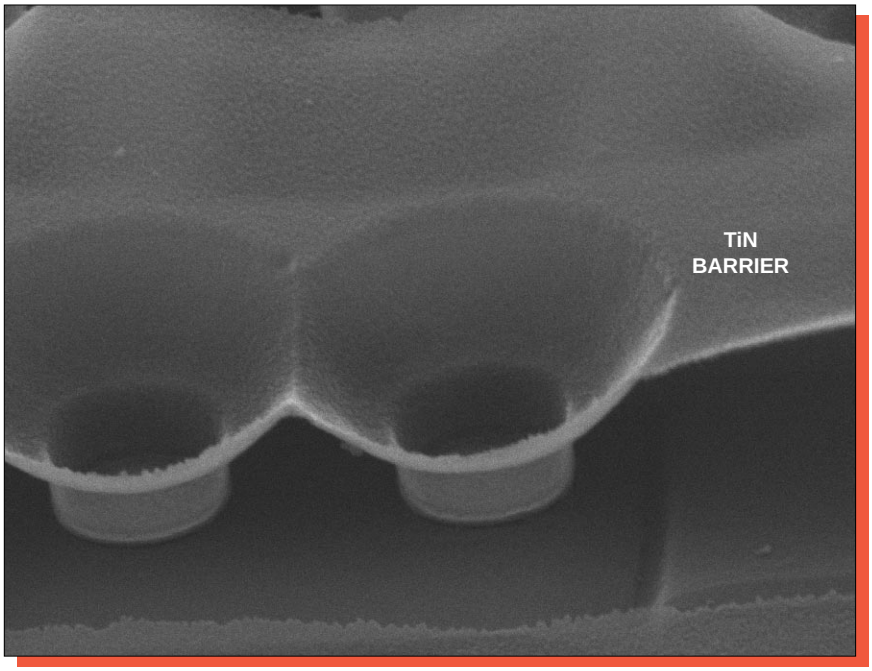


Mag. 6500x

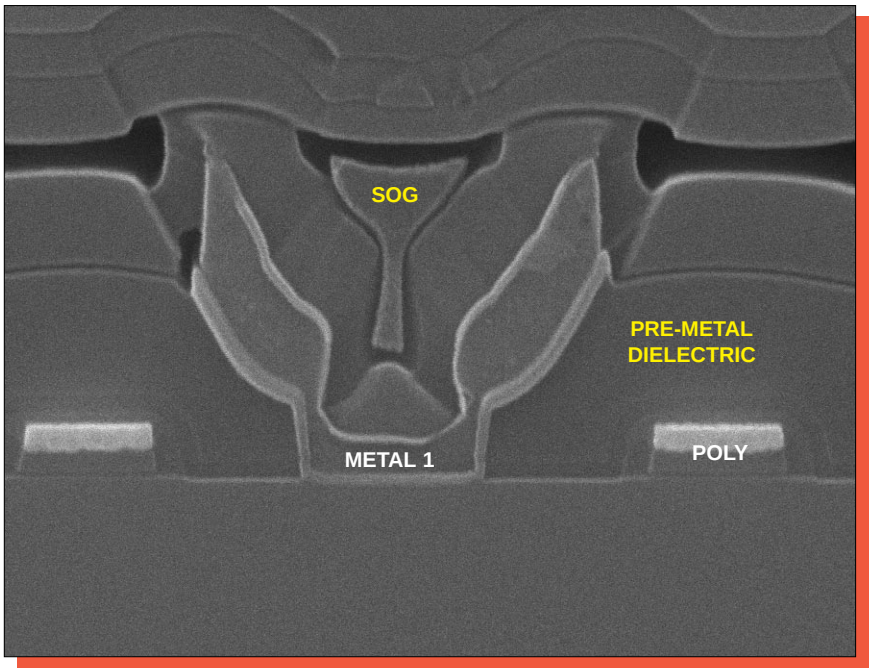


Mag. 20,000x

Figure 13. Perspective SEM views of metal 1 coverage. 60°.

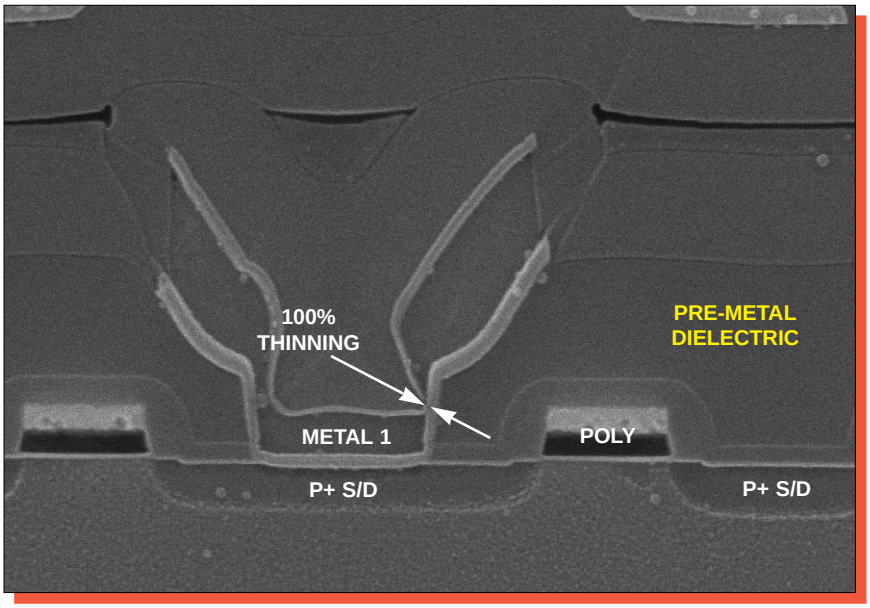


60°

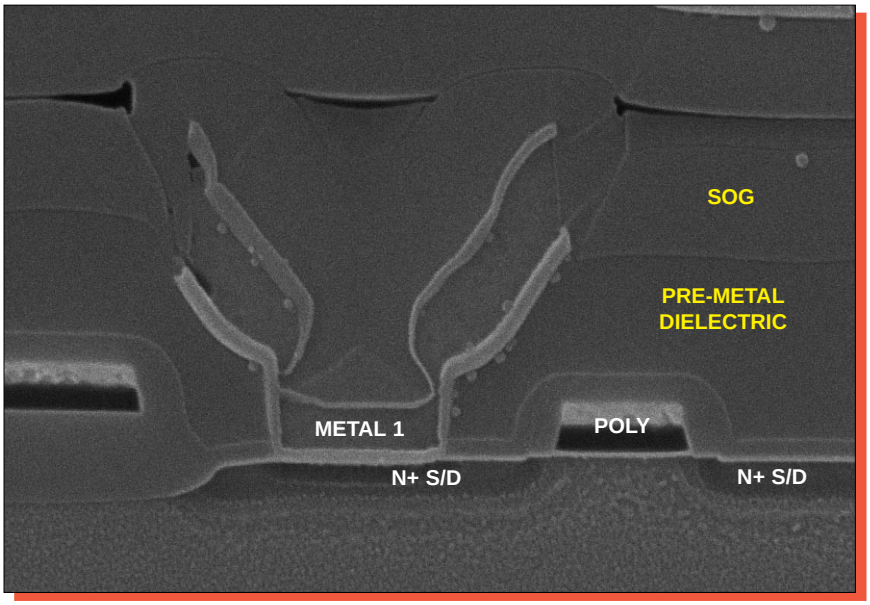


glass etch

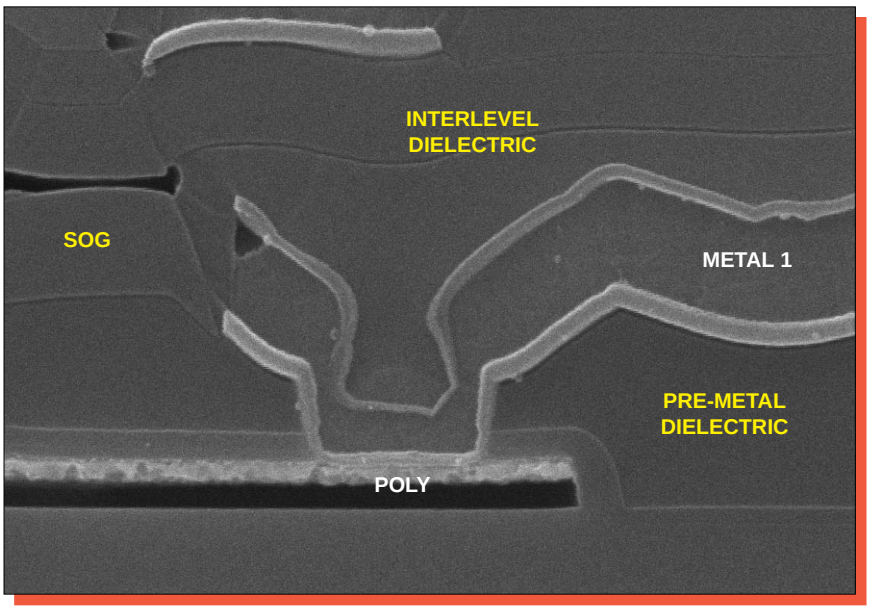
Figure 14. SEM views of barrier coverage and a metal contact. Mag. 26,000x.



metal 1-to-P+

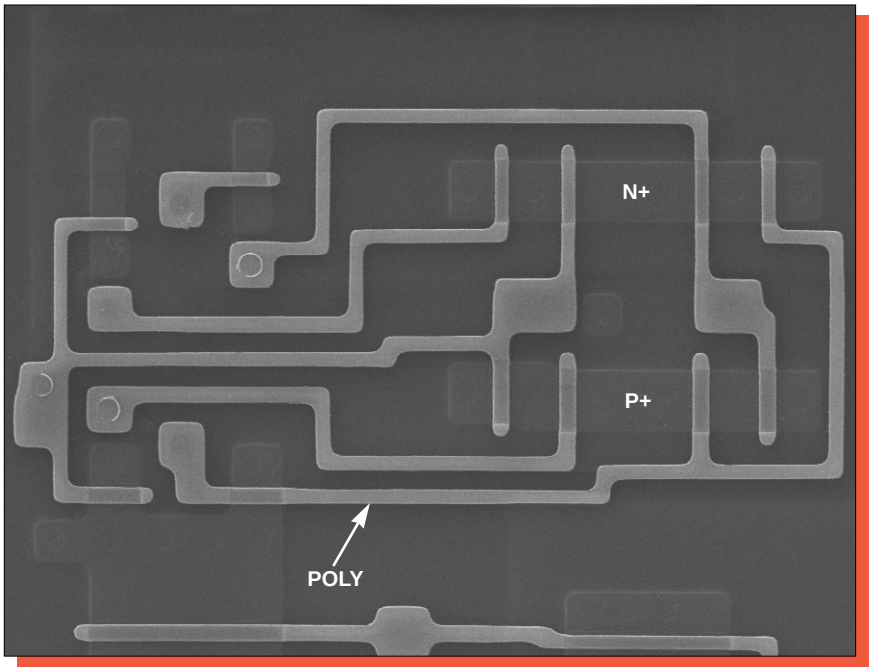


metal 1-to-N+

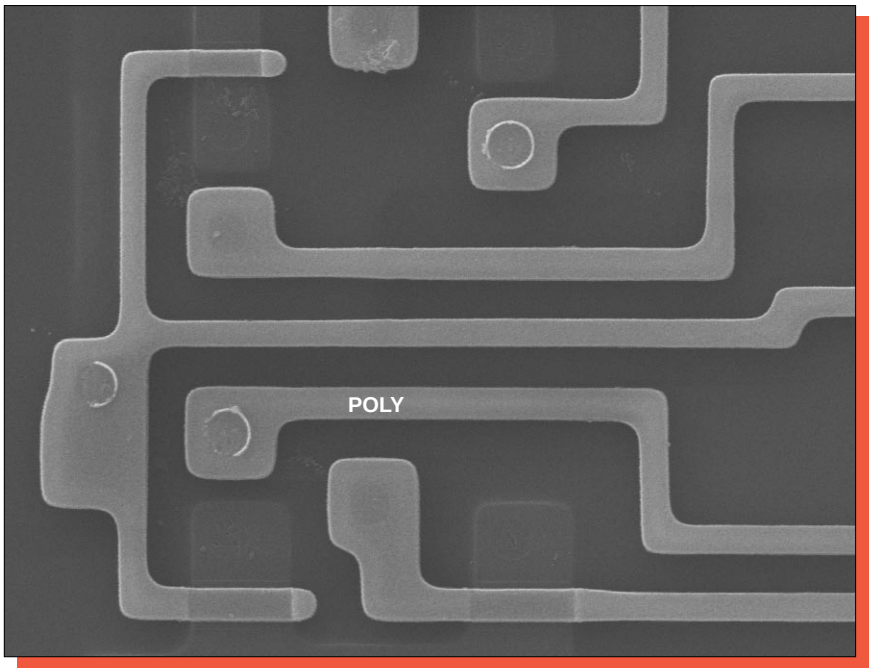


metal 1-to-poly

Figure 15. SEM section views of typical metal 1 contacts. Mag. 26,000x.

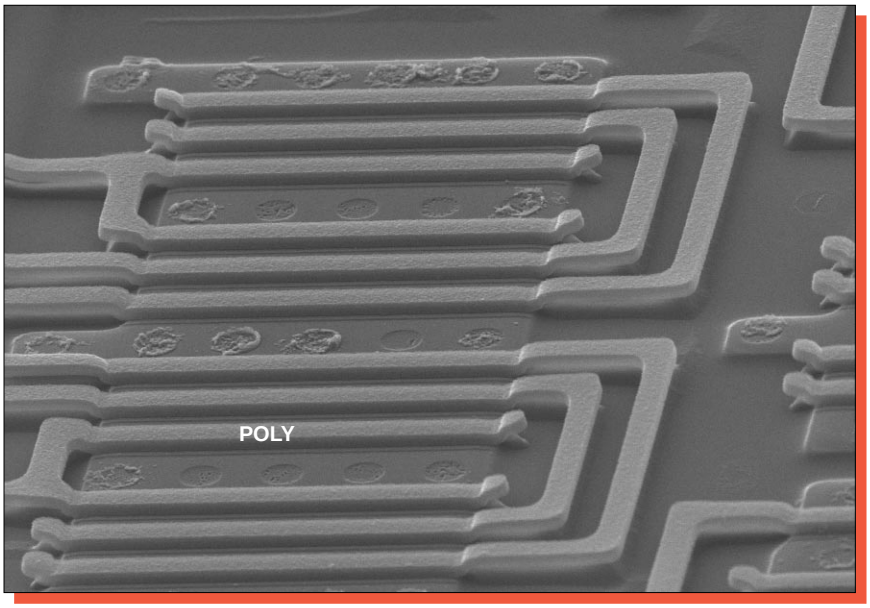


Mag. 3200x

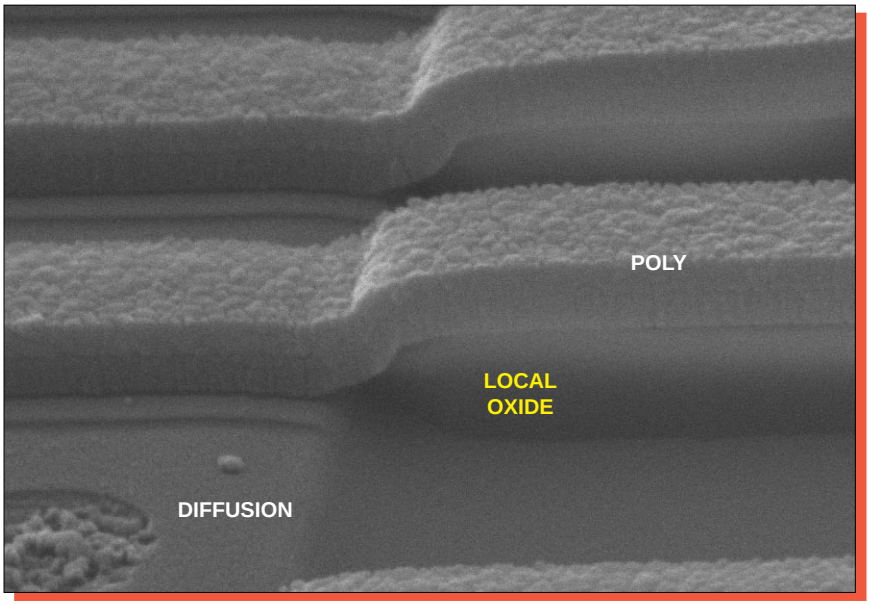


Mag. 6500x

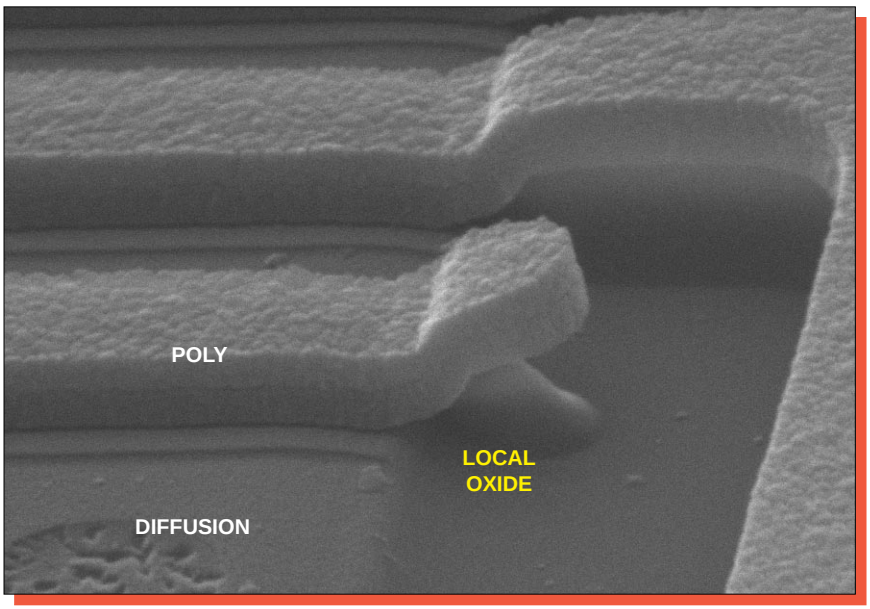
Figure 16. Topological SEM views of poly patterning. 0°.



Mag. 6500x

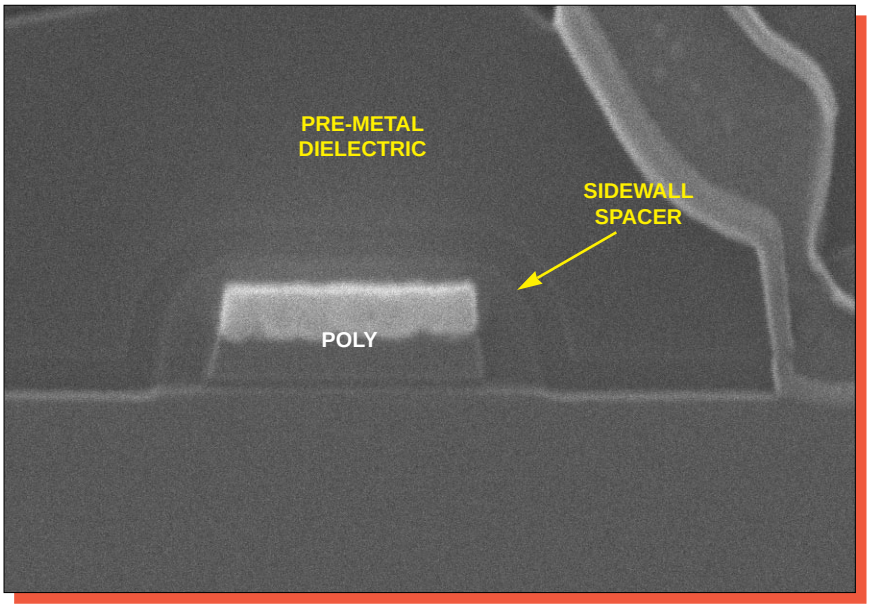


Mag. 40,000x

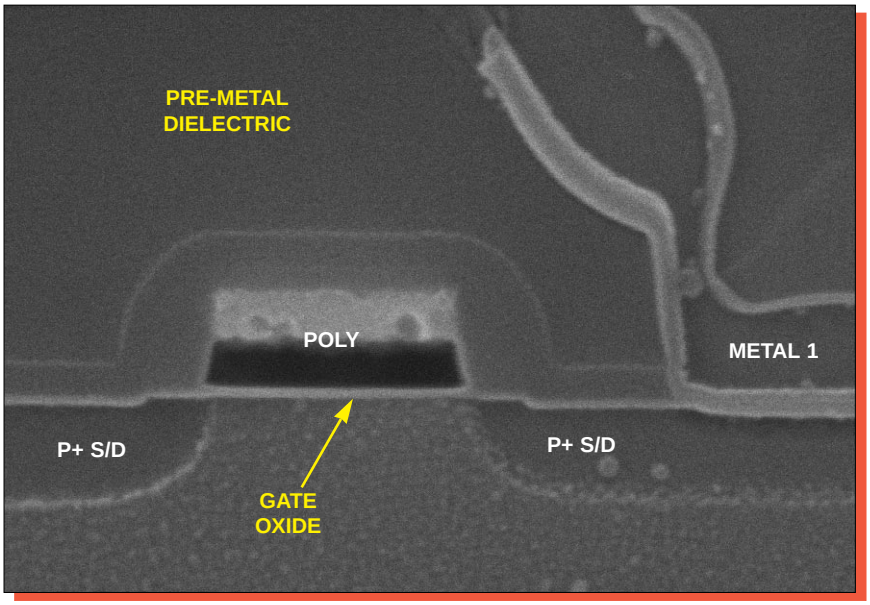


Mag. 40,000x

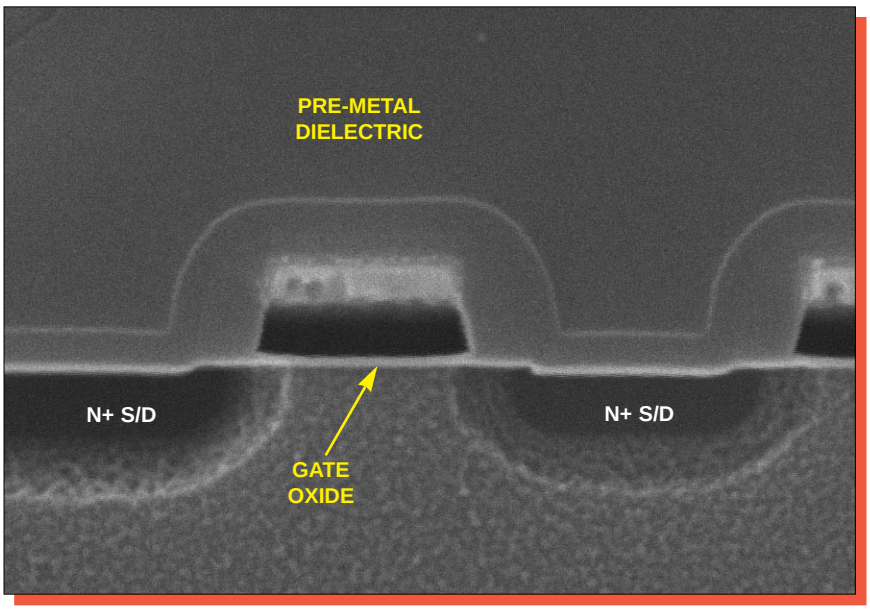
Figure 17. Perspective SEM views of poly coverage. 60°.



glass etch



P-channel



N-channel

Figure 18. SEM section views of typical transistors. Mag. 52,000x.

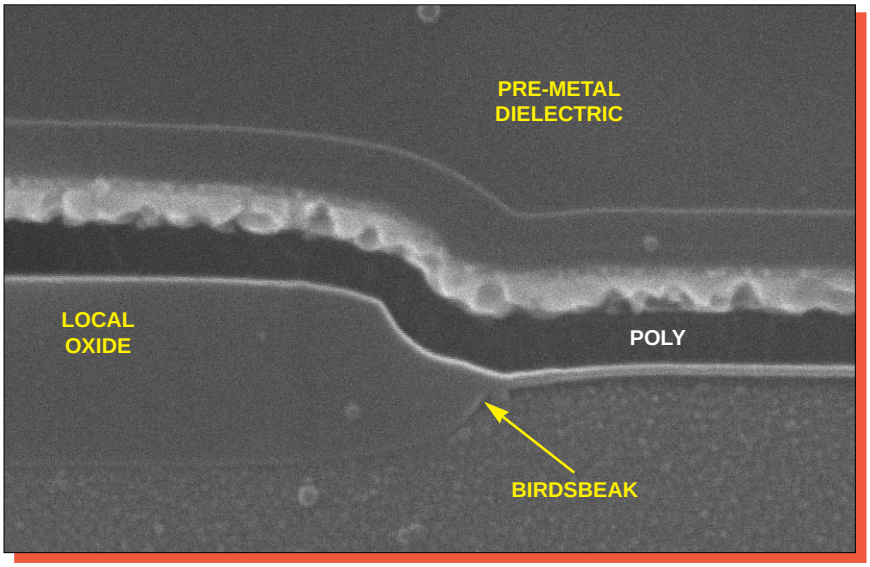
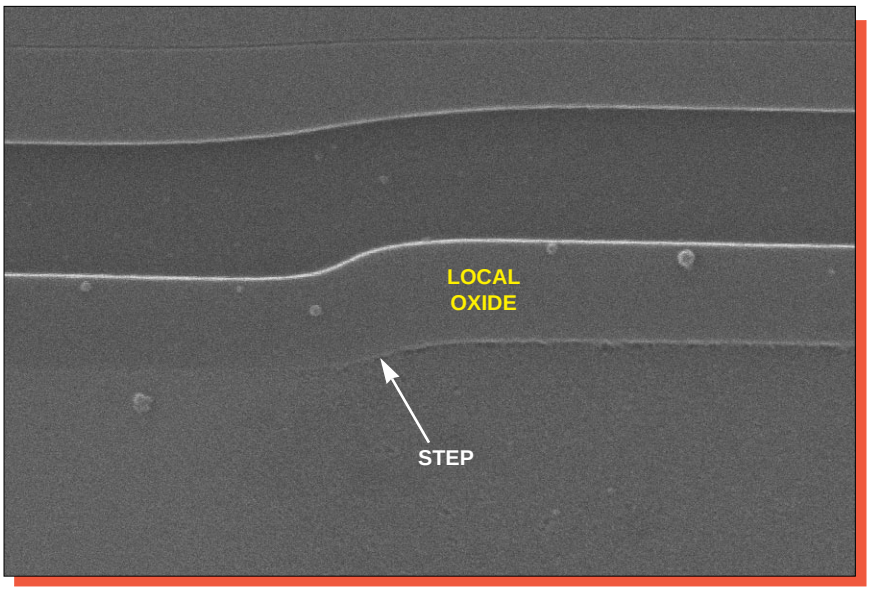
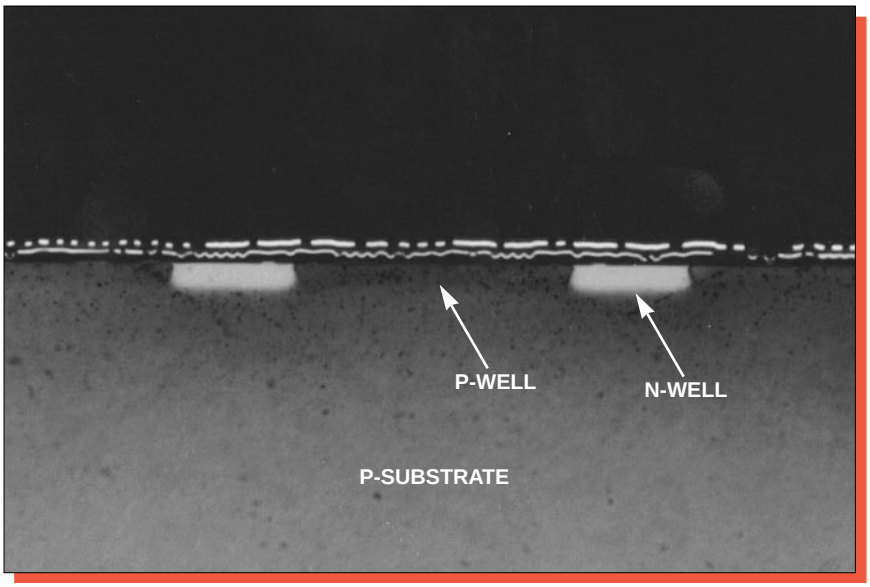


Figure 19. SEM section view of a local oxide birdsbeak. Mag. 52,000x.

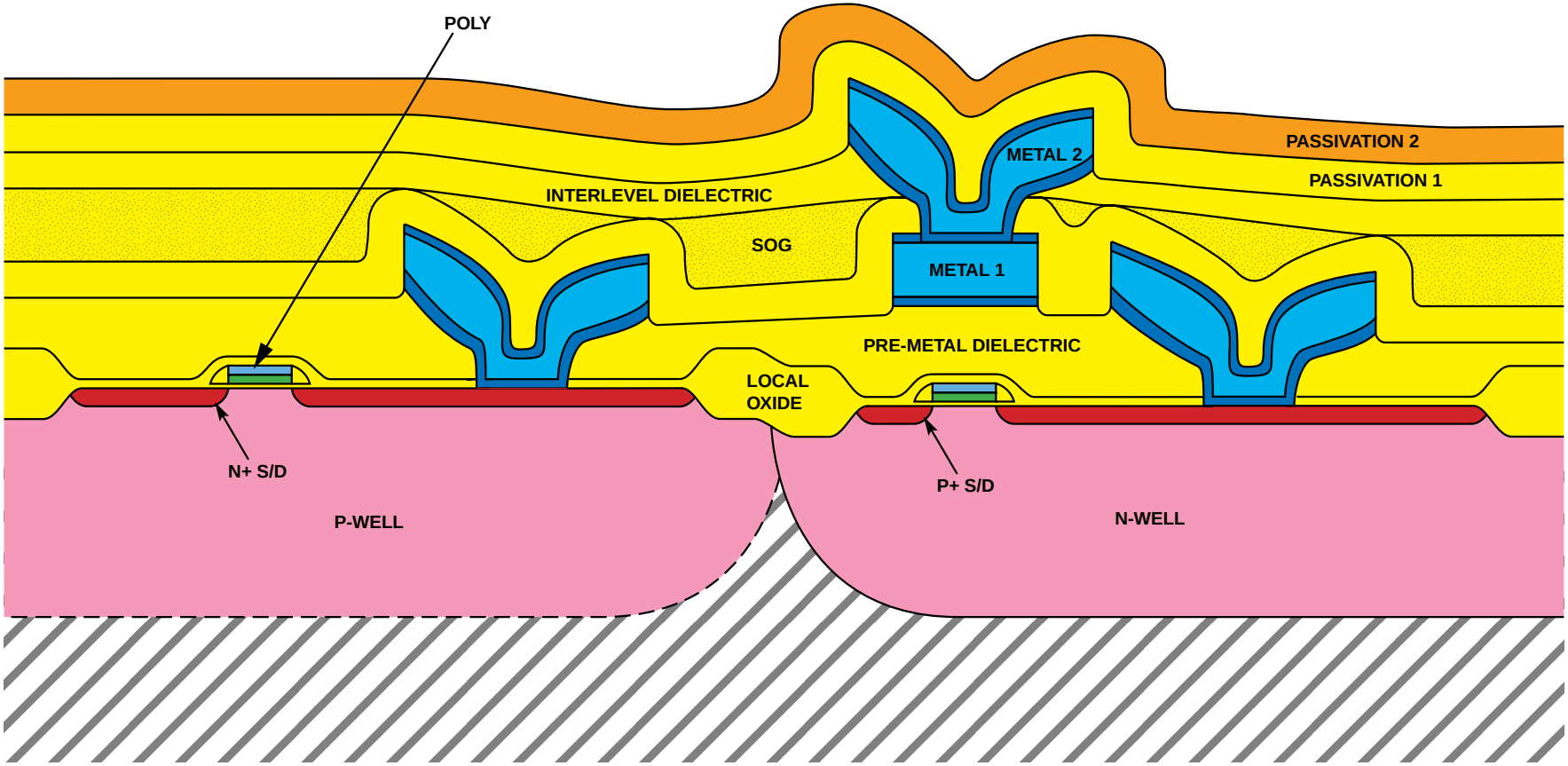


Mag. 26,000x



Mag. 800x

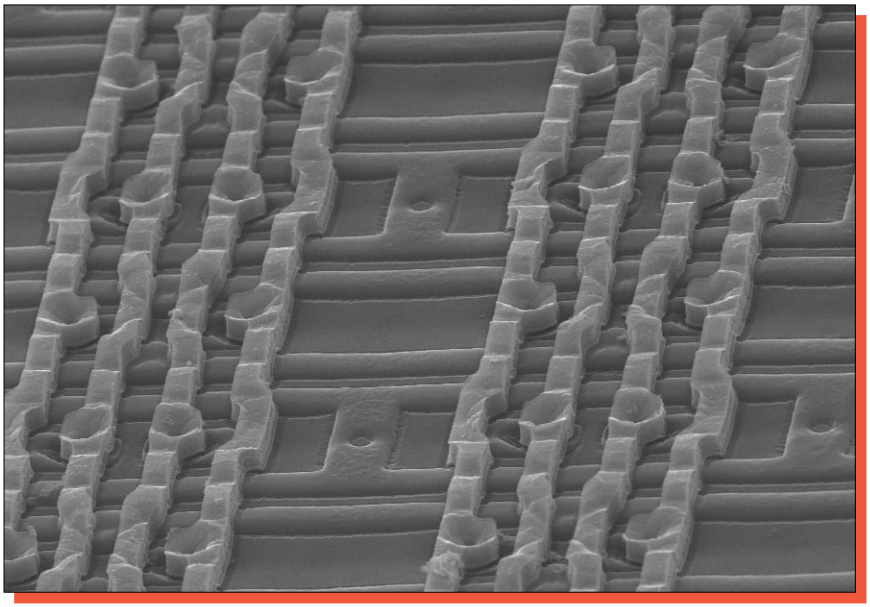
Figure 20. Section views of the well structure.



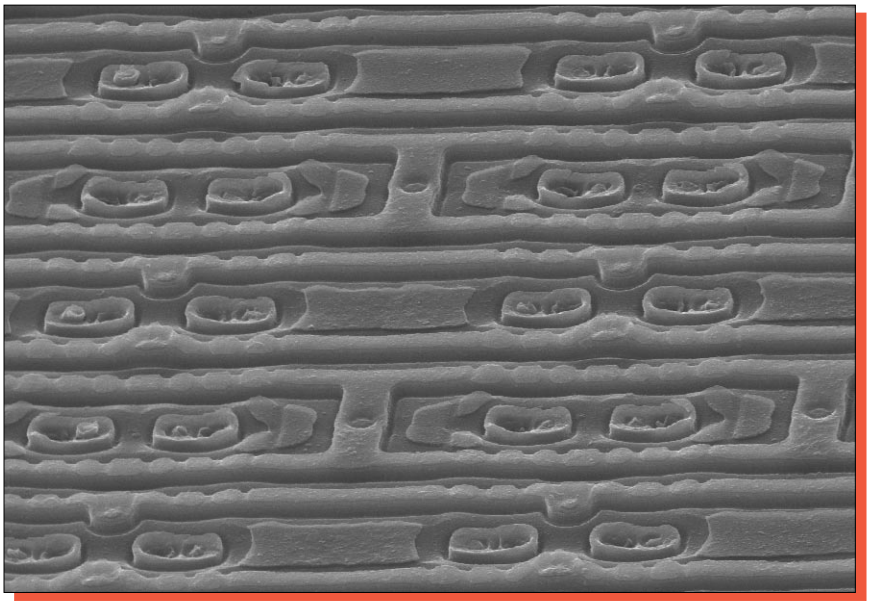
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

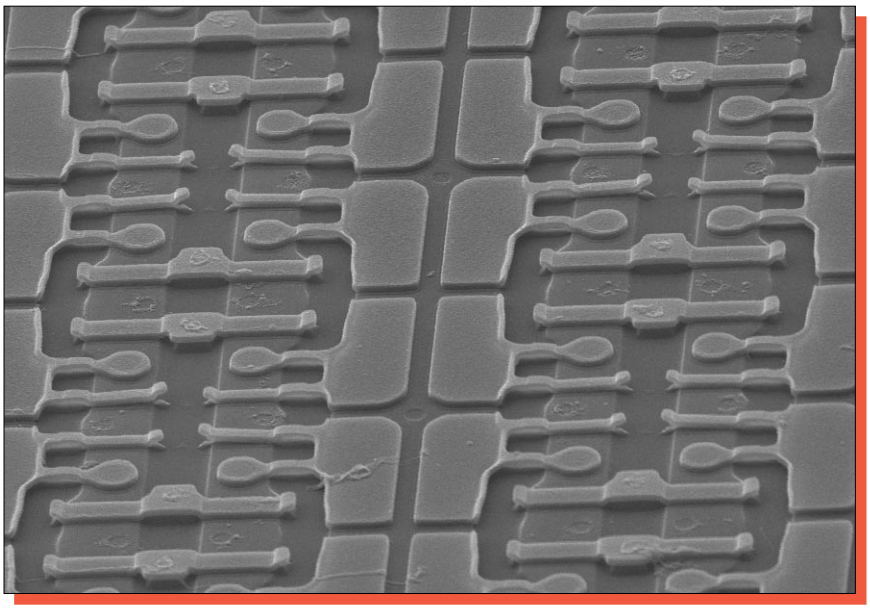
Figure 21. Color cross section drawing illustrating device structure.



metal 2

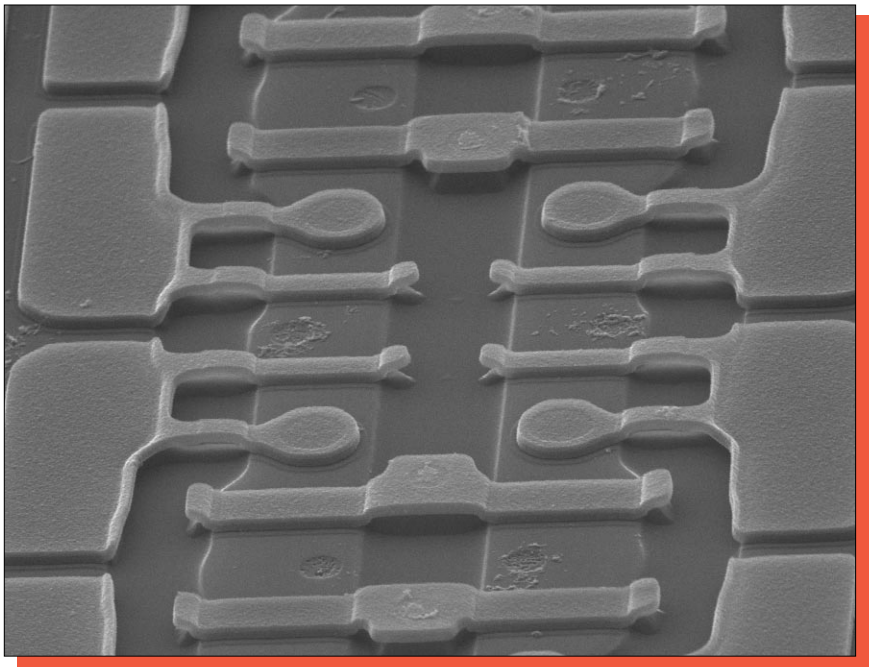


metal 1

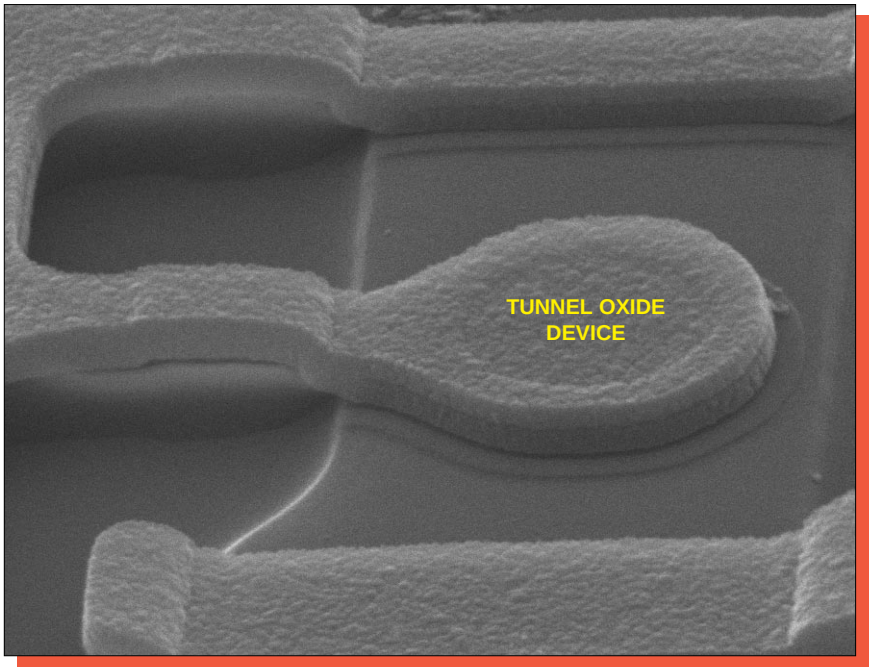


poly

Figure 22. Perspective SEM views of the EEPROM cell array. Array A, Mag. 3200x, 60°.

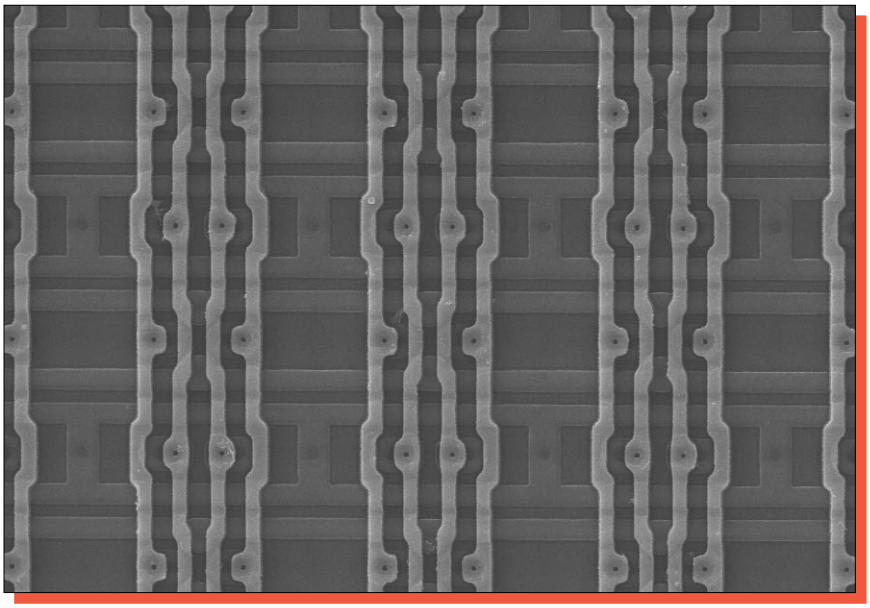


Mag. 6500x

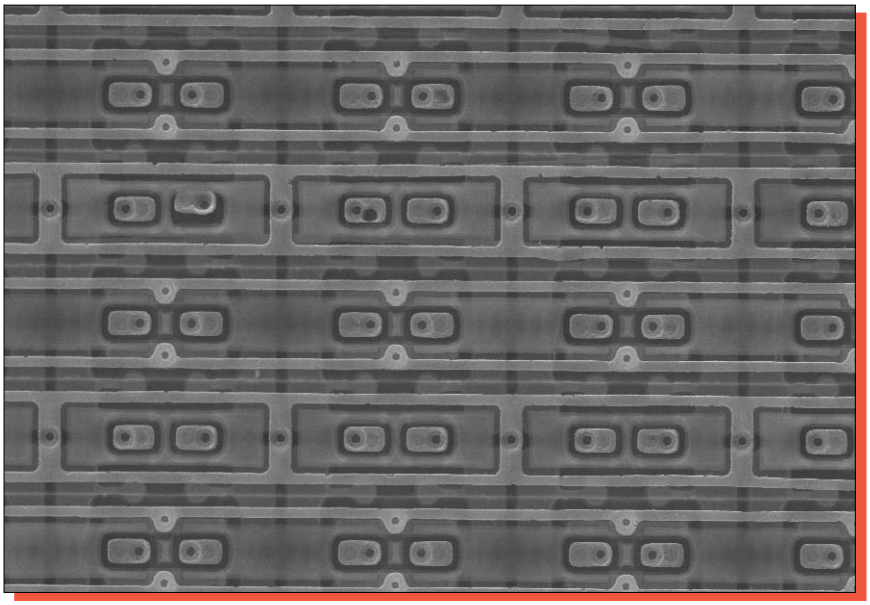


Mag. 26,000x

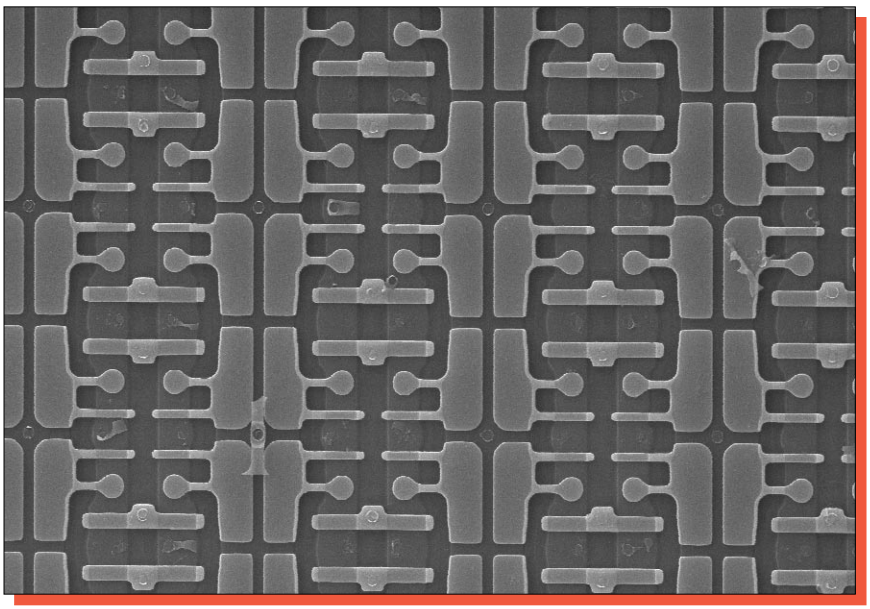
Figure 23. Detailed SEM views of the EEPROM cell array. Array A, 60°.



metal 2

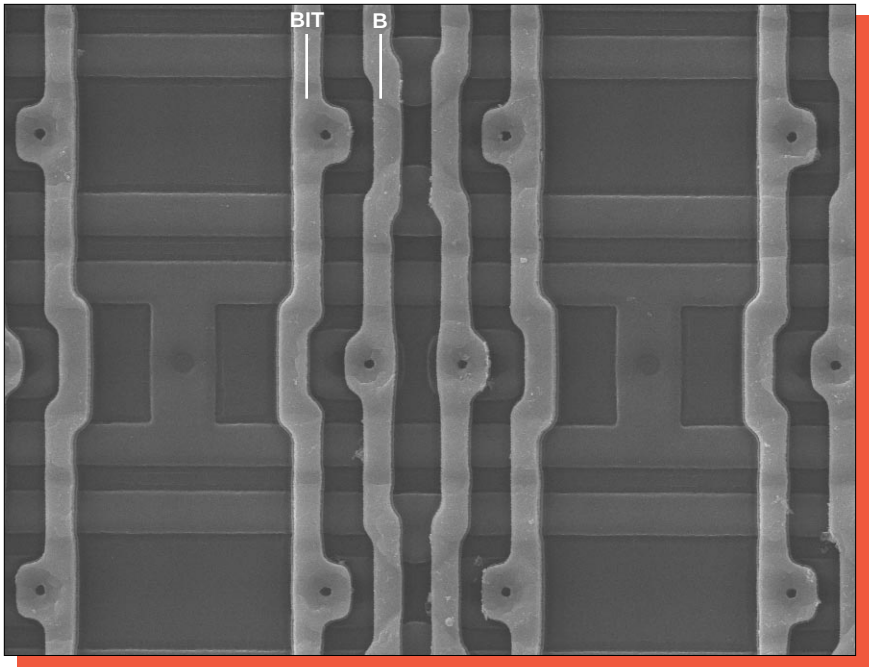


metal 1

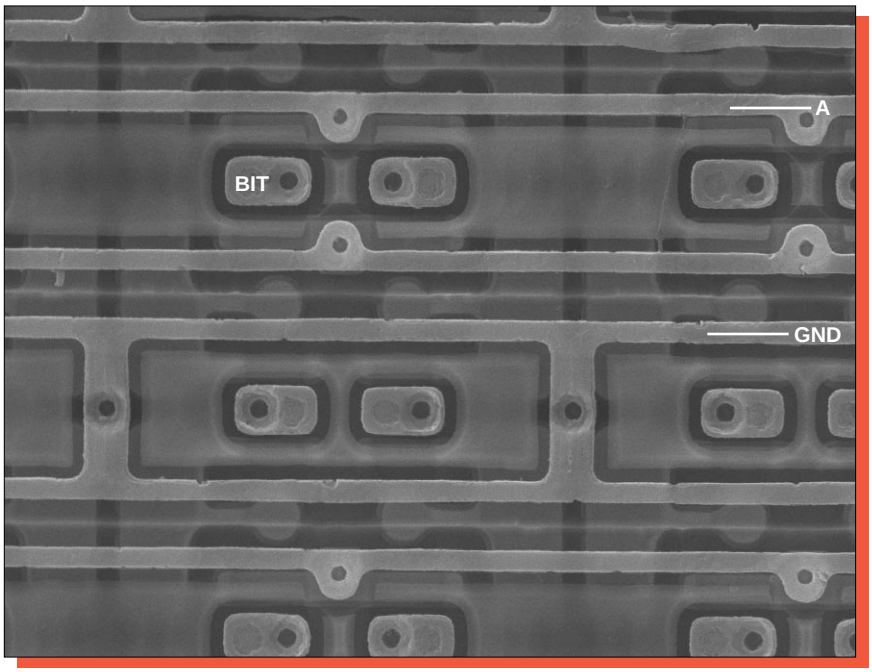


poly

Figure 24. SEM views of the EEPROM cell array. Array A, Mag. 1600x, 0°.

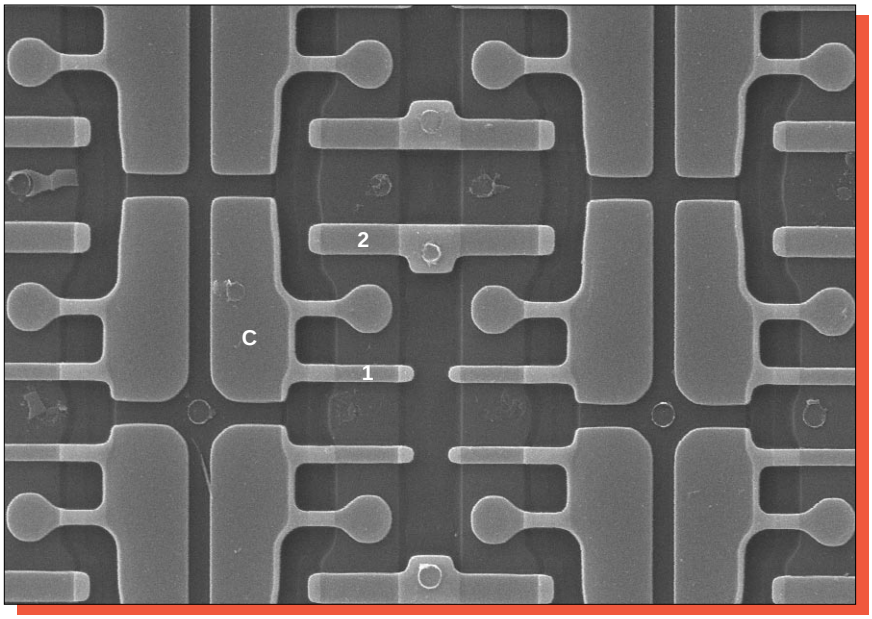


metal 2



metal 1

Figure 25. Additional SEM views of the EEPROM cell array. Array A, Mag. 3200x,



poly

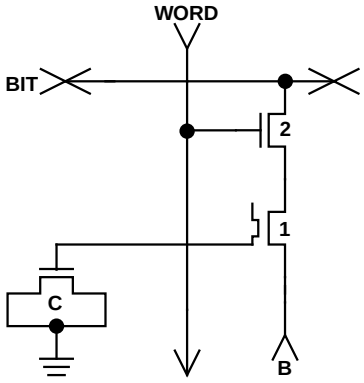


Figure 26. SEM view and schematic of the EEPROM cell. Array A, Mag. 3200x, 0°.

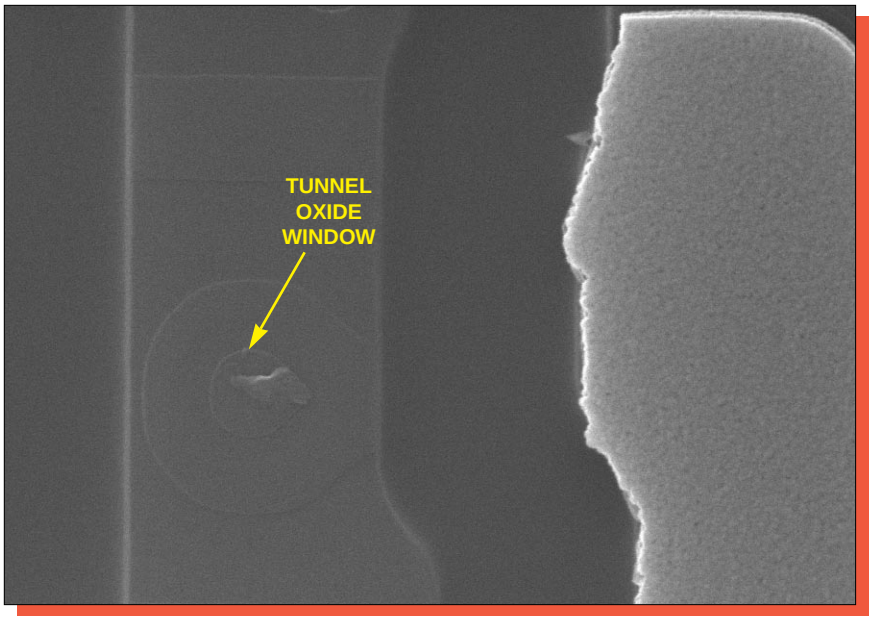
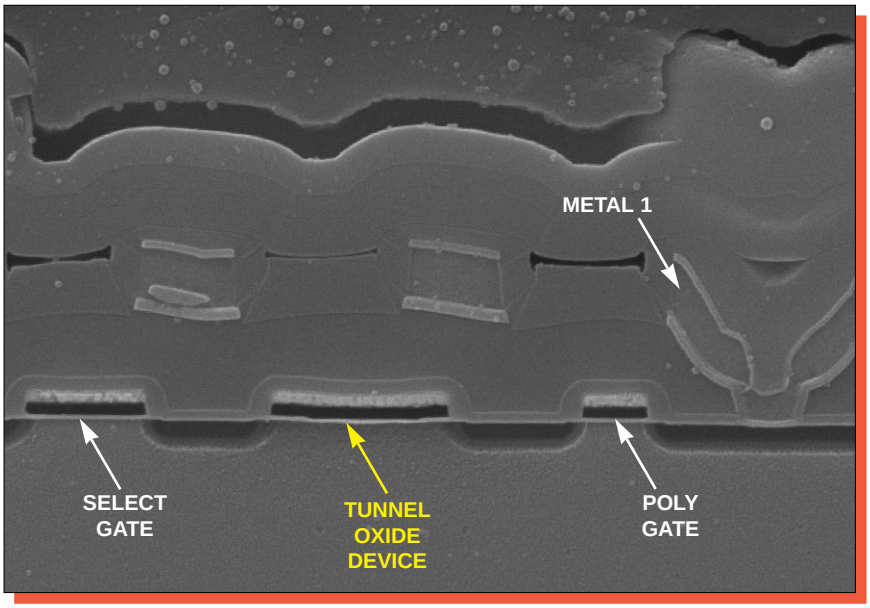
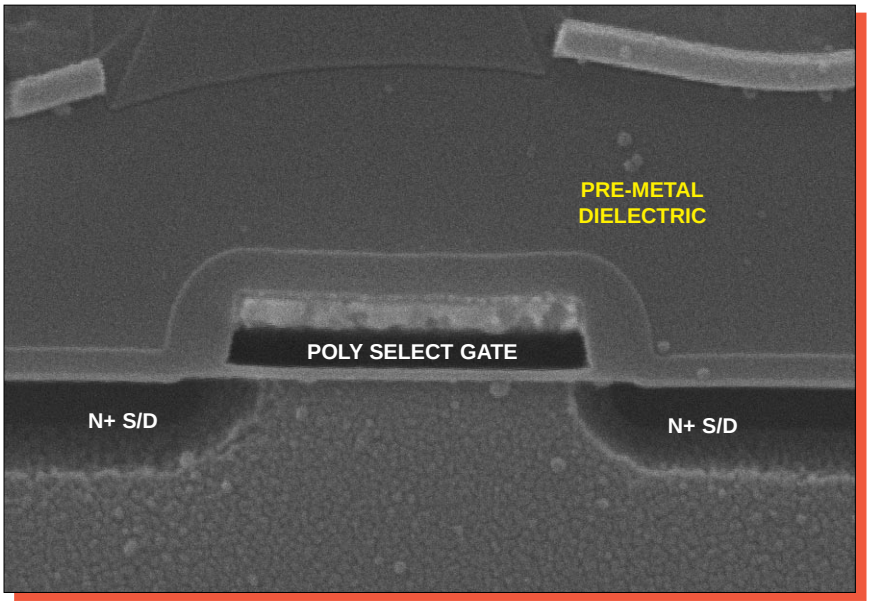


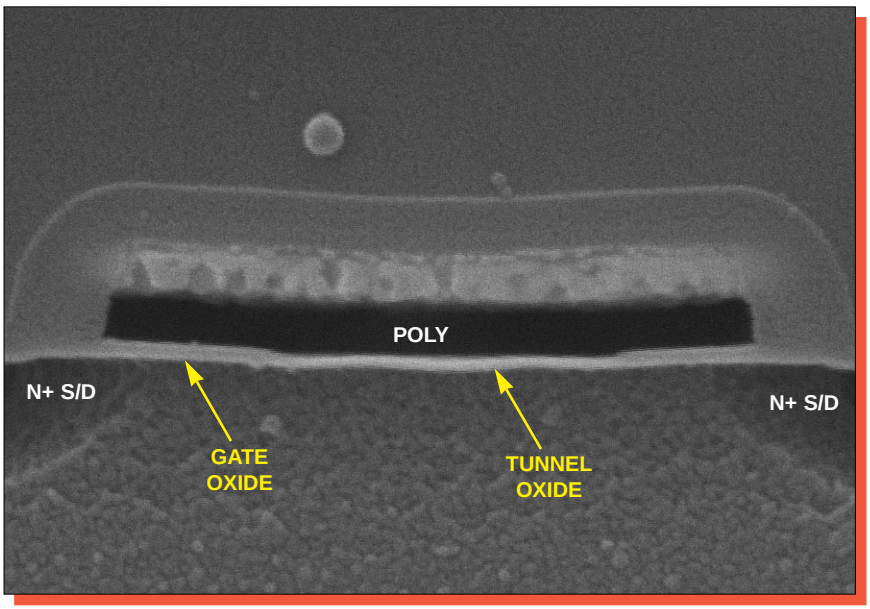
Figure 27. Topological SEM view of the tunnel oxide window. Array A, Mag. 13,000x, 0°.



Mag. 13,000x

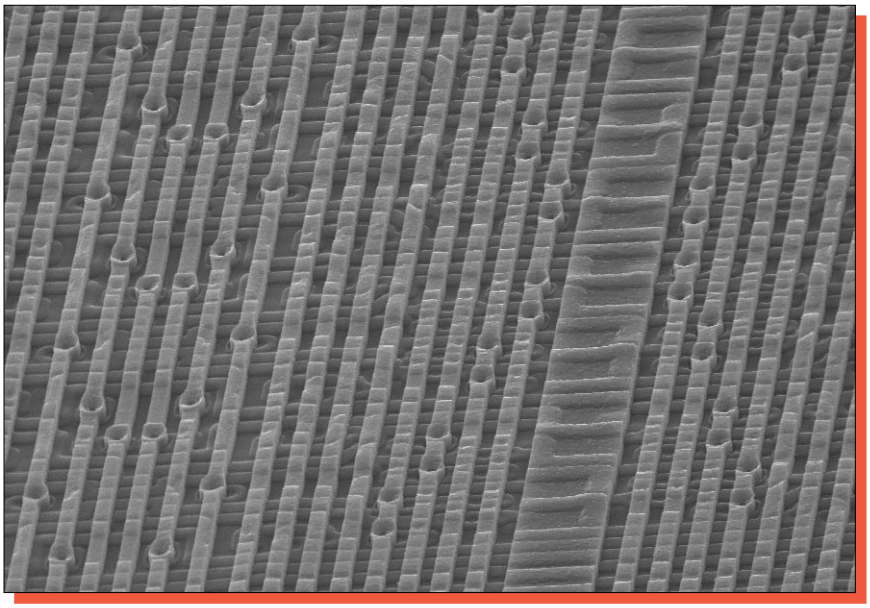


Mag. 40,000x

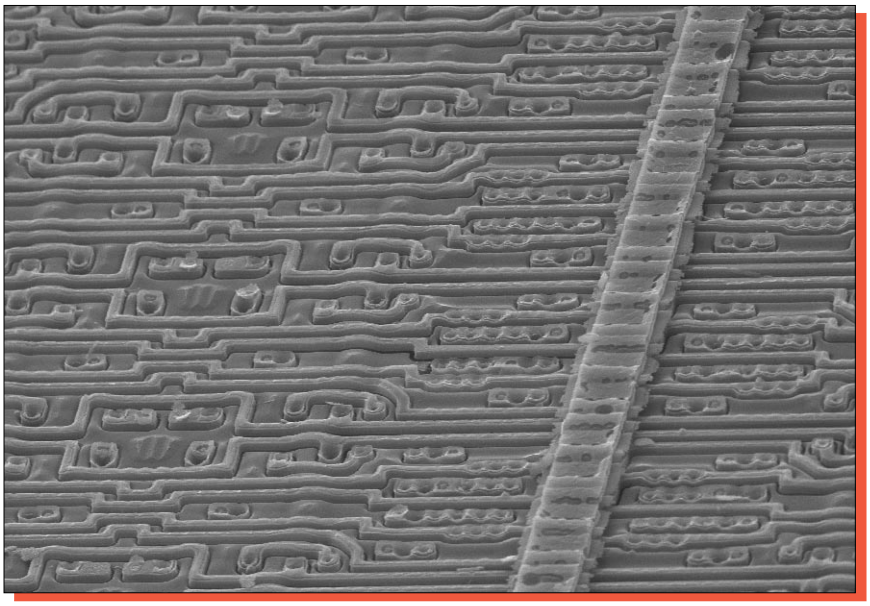


Mag. 52,000x

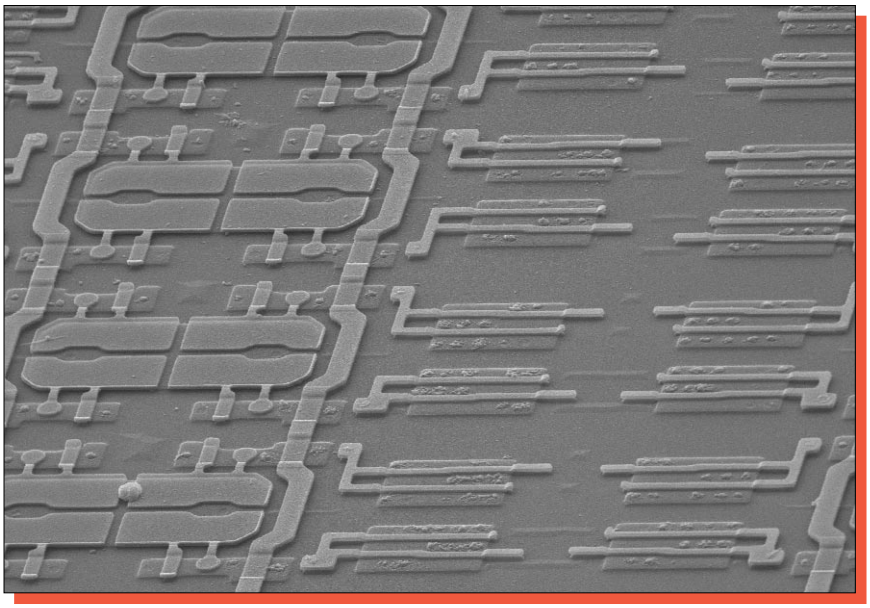
Figure 28. SEM section views of an EEPROM cell. Array A.



metal 2

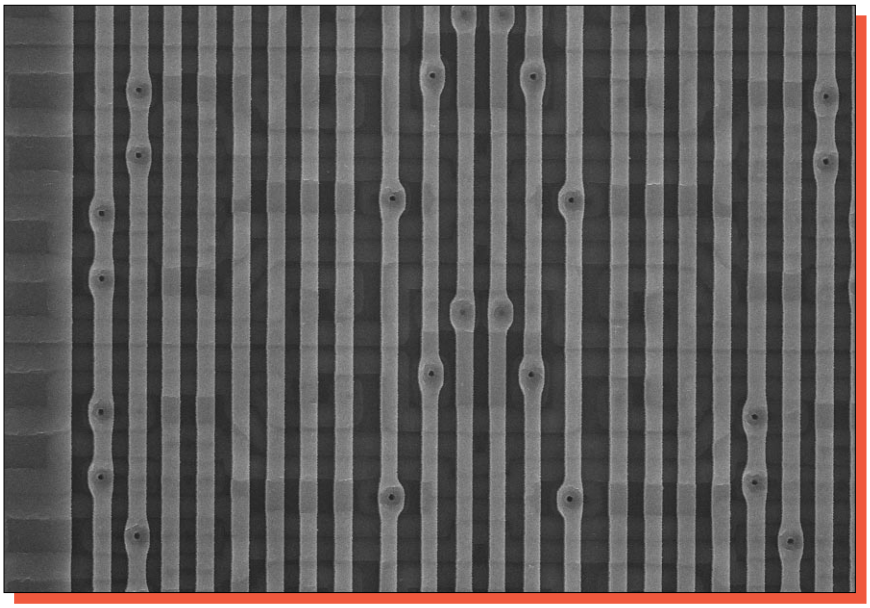


metal 1

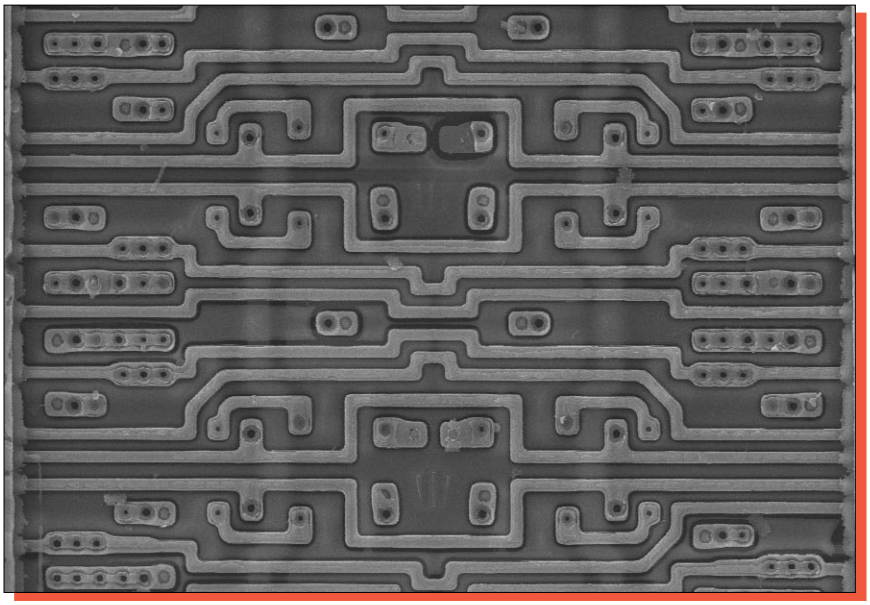


poly

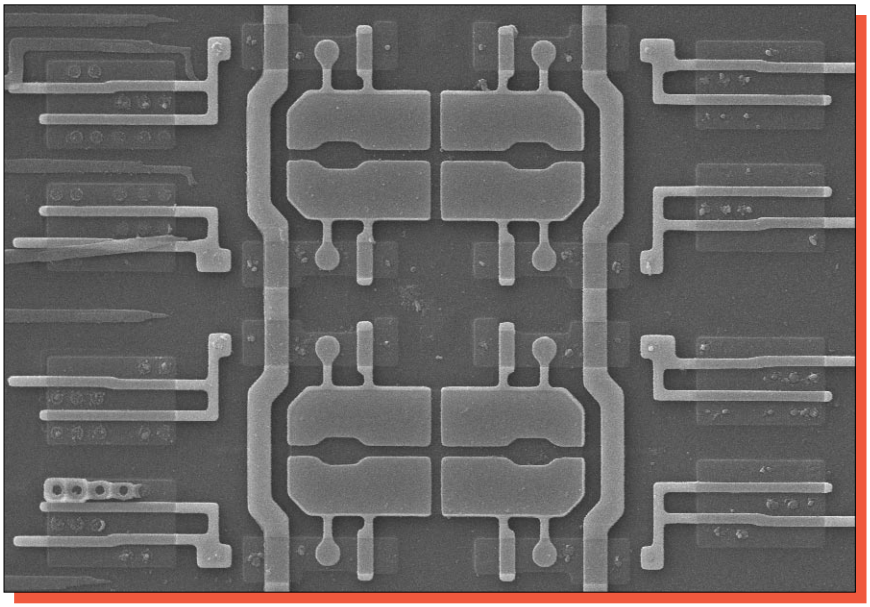
Figure 29. Perspective SEM views of the additional EEPROM cell array. Array B, Mag. 1600x, 60°.



metal 2

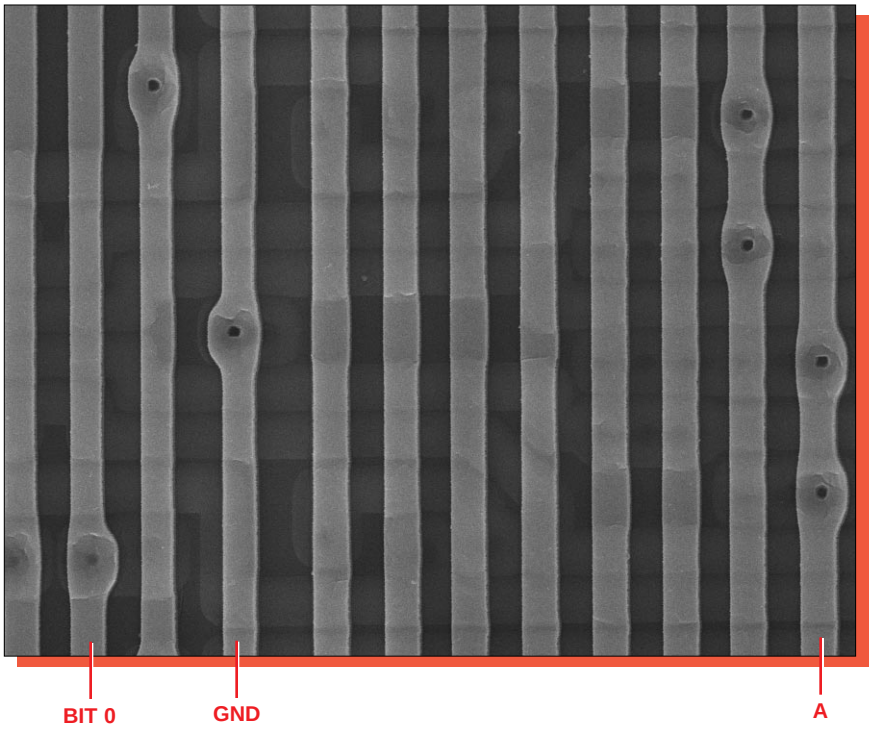


metal 1

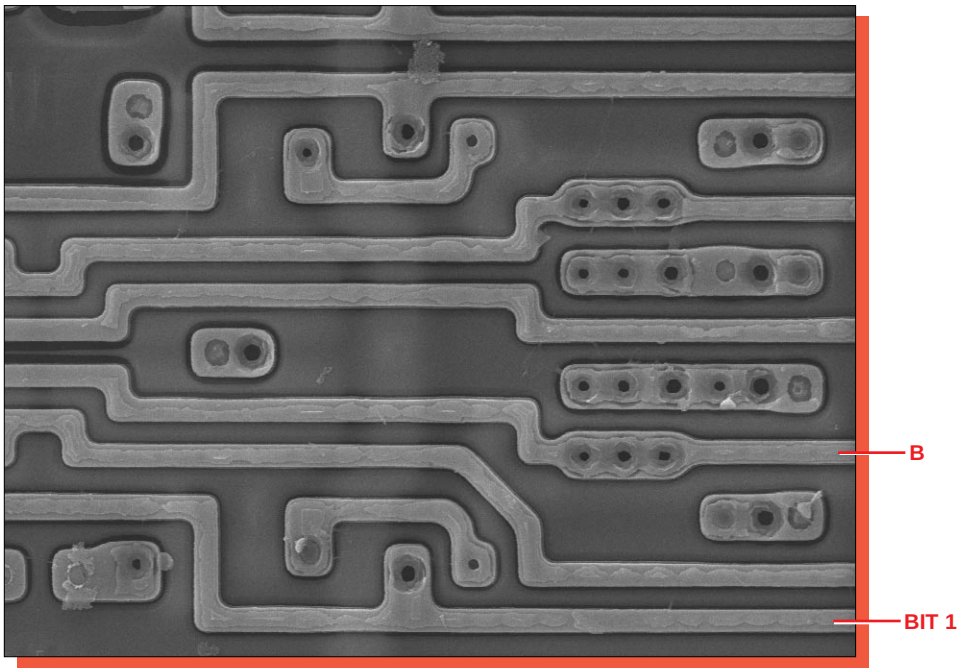


poly

Figure 30. SEM views of additional EEPROM cells. Array B, Mag. 1600x.

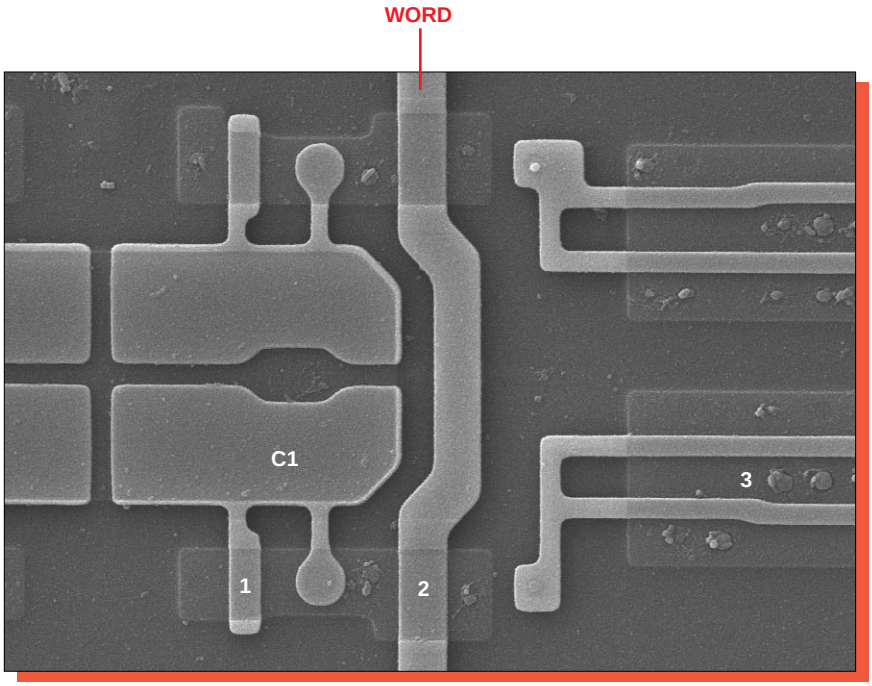


metal 2



metal 1

Figure 31. Detailed SEM views of additional EEPROM cell. Array B, Mag. 3200x. 0°.



poly

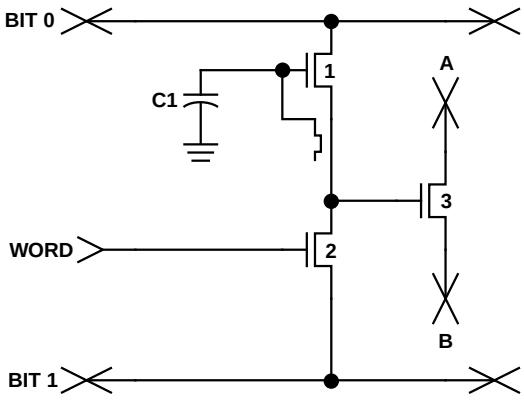
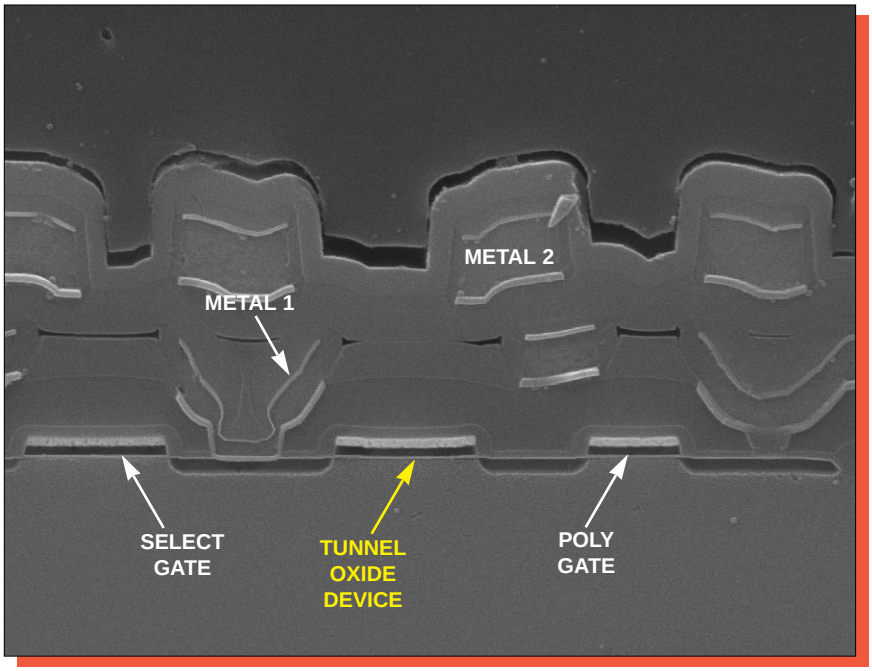
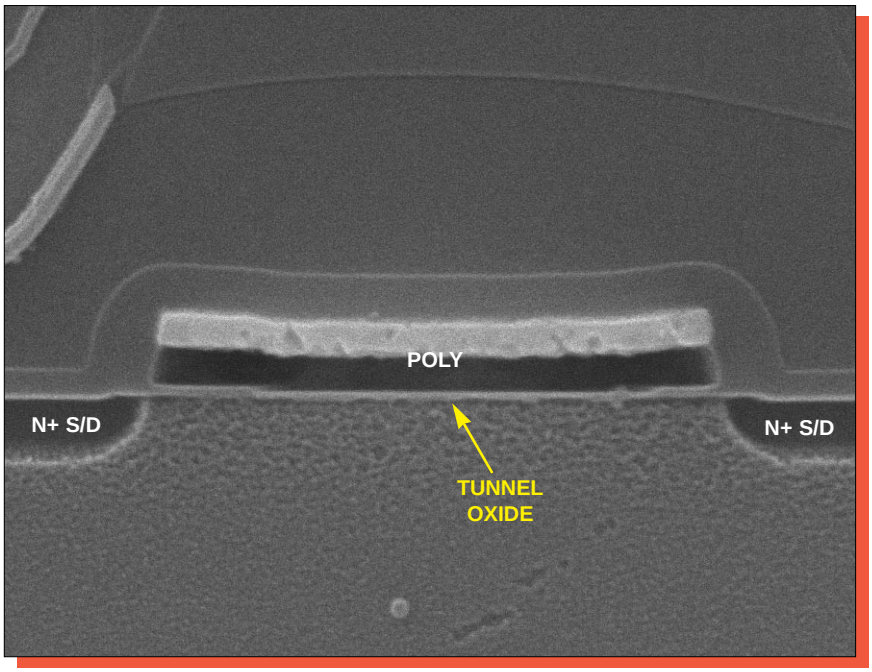


Figure 32. Detailed SEM view and schematic of additional EEPROM cell. Array B, Mag. 3200x, 0°.

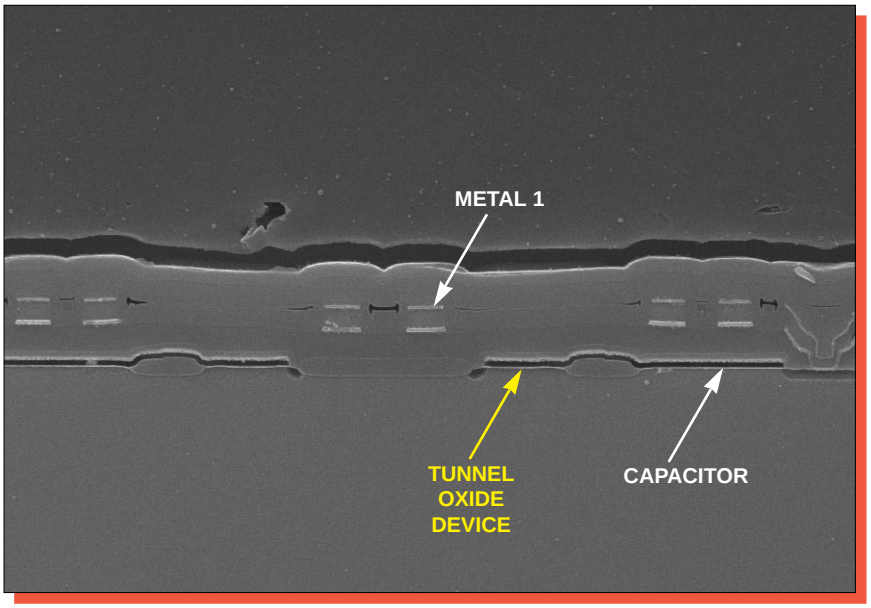


Mag. 10,000x

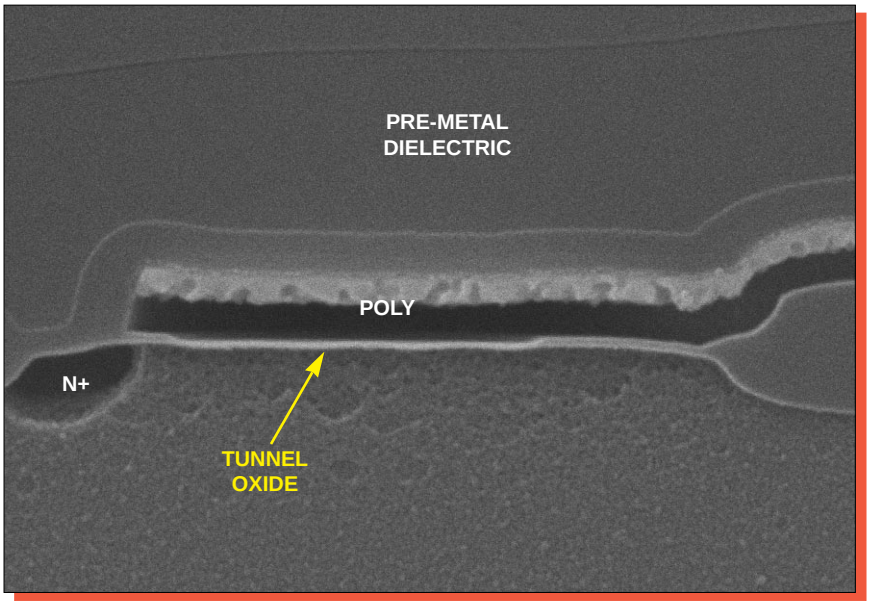


Mag. 40,000x

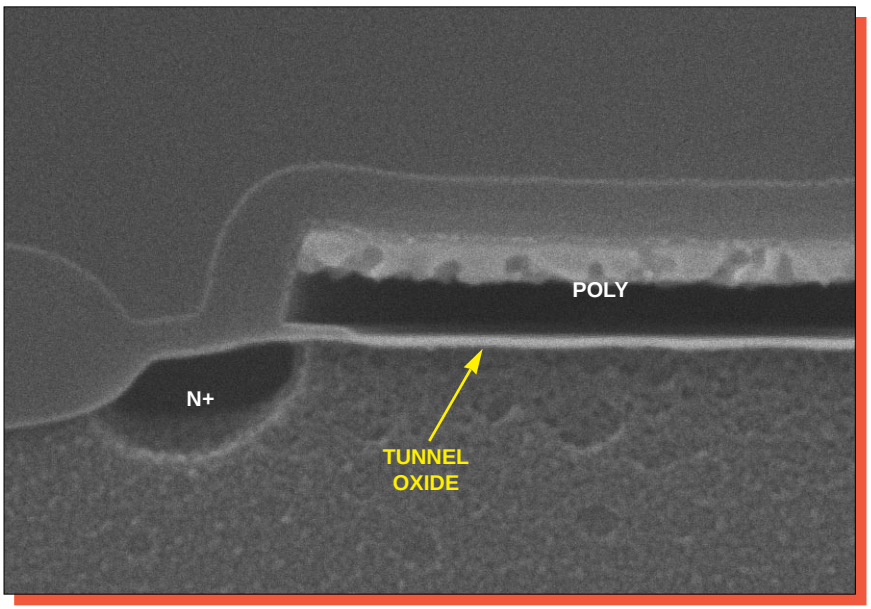
Figure 33. SEM section views of additional EEPROM cell. Array B.



Mag. 5000x

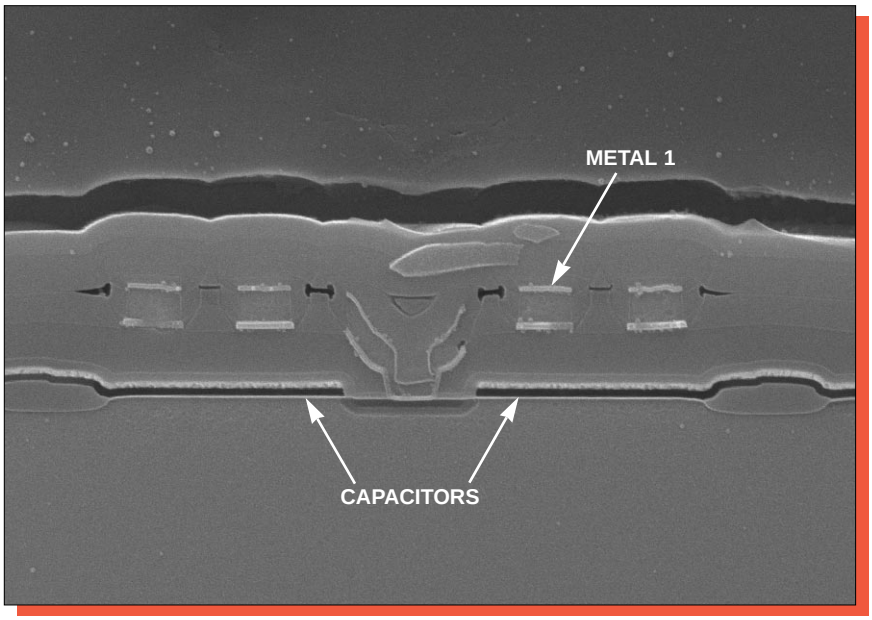


Mag. 37,000x

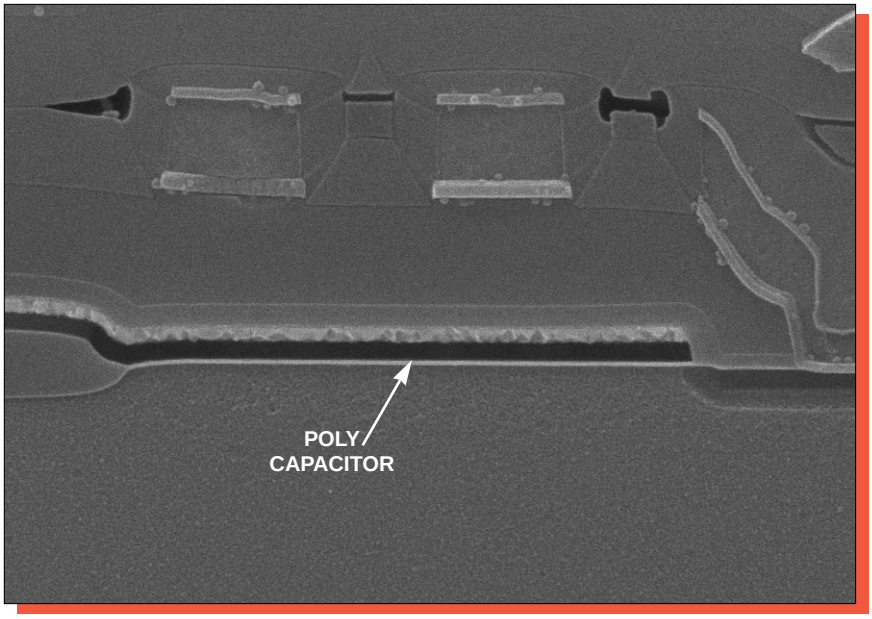


Mag. 52,000x

Figure 34. SEM section views of additional EEPROM cell. Array B.

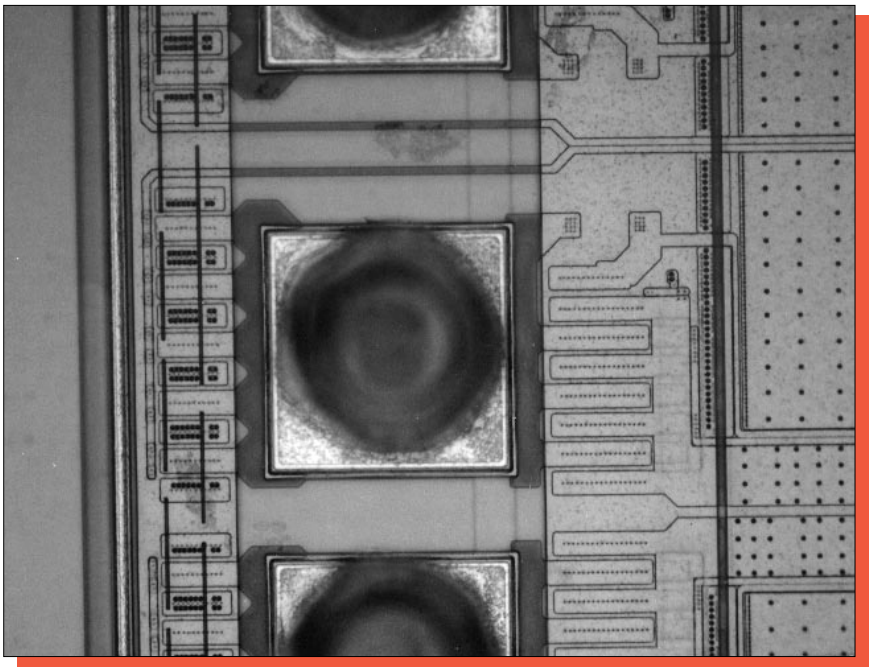


Mag. 8000x

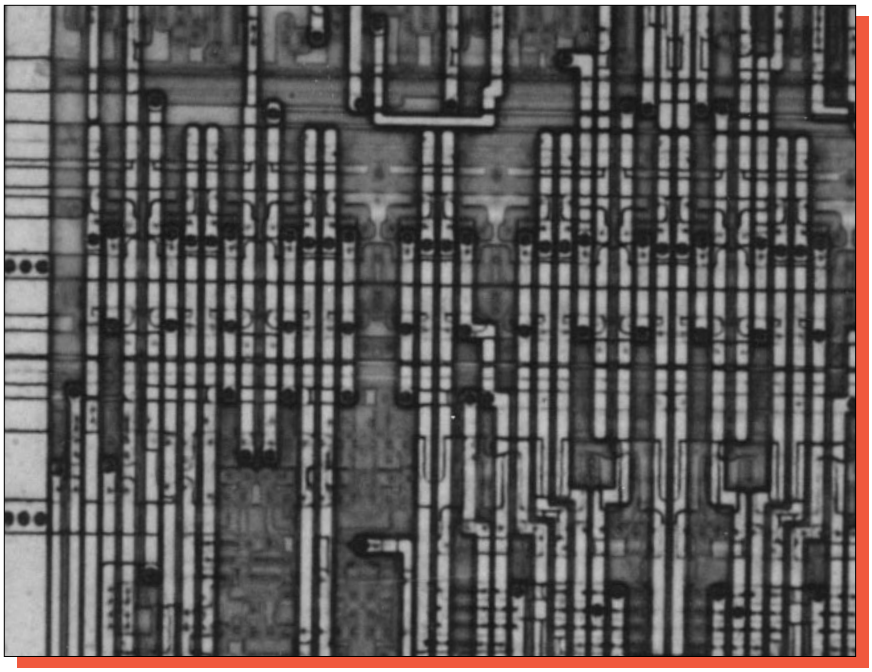


Mag. 20,000x

Figure 35. SEM section views of additional EEPROM cell through the capacitor region. Array B.



Mag. 320x



Mag. 800x

Figure 36. Optical views of an I/O structure and general circuitry.