

Construction Analysis

Analog Devices ADSP-21062-KS-160

Report Number: SCA 9704-537



INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Analog Devices ADSP-21062-KS-160 SHARC Digital Signal Processor. One device which was packaged in a 240-pin Plastic Quad Flat Package (PQFP) was received for the analysis. The device was date coded 9630.

MAJOR FINDINGS

Questionable Items:¹

- Metal 2 aluminum thinned up to 90 percent² at vias (Figure 16).

Special Features:

- Sub-micron gate lengths (0.55 micron).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- The device was packaged in a 240-pin Plastic Quad Flat Package (PQFP). A copper heat slug (heatsink) was employed on the top of the package (cavity down orientation). It was internally connected to ground to bias the substrate.
- Wirebonding method: A thermosonic ball bond technique employing 1.2 mil O.D. gold wire was used.
- Dicing: Sawn (full depth) dicing.
- Die attach: A silver epoxy compound.

Die Process

- Fabrication process: Selective oxidation CMOS process employing a twin-well process in a P substrate.
- Die coat: No die coat was used on the device.
- Final passivation: A layer of nitride over a layer of silicon-dioxide.
- Metallization: Two levels of metal defined by standard dry-etch techniques. Metal 2 consisted of aluminum with a titanium-nitride cap and a titanium barrier. Metal 1 consisted of aluminum, a titanium nitride cap and barrier, and a titanium adhesion layer. Standard vias were used between metal 2 and metal 1. Tungsten plugs were used as the vertical interconnect under metal 1.
- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing spin-on-glass (SOG) between them.

TECHNOLOGY DESCRIPTION (continued)

- Pre-metal dielectric: This dielectric consisted of a layer of reflow glass over densified oxide.
- Polysilicon: Two layers of polysilicon were used on the die. Poly 1 (polysilicon and tungsten silicide) was used to form redundancy fuses, all gates on the die, and word lines in the array. Poly 2 was used to form “pull-up” resistors in the cell array, and formed resistors in fuse blocks which were connected to one end of the poly 1 fuses. Both poly layers were defined by a dry-etch of good quality.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. No silicide was present on diffusions. An LDD process was used with the oxide sidewall spacers left in place. N+ diffusions were “pushed down” at tungsten contacts.
- Wells: Planar (no step in LOCOS) twin-well process in a P substrate. No epi layer.
- Redundancy: Fuses consisting of poly 1 were present on the die. Passivation and interlevel dielectric cutouts were made over the fuses. One end of the fuse structure was connected to metal 1, while the other end was connected to a poly 2 resistor. Some laser blown fuses were noted.
- Memory cells: The die employed a 2 Mbit SRAM array. The memory cells used a 4T CMOS SRAM cell design. Metal 2 distributed GND and Vcc (via Metal 1), and formed the bit lines using metal 1 links. Metal 1 was used as the “piggy-back” word lines. Poly 1 formed the word lines, select, and storage gates. Poly 2 formed “pull-up” resistors and distributed Vcc.
- Design features: Slotted and beveled Metal 2 bus lines were employed for stress relief. Both metals 1 and 2 were used in the bond pads.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 3

Questionable Items:¹ None.

Special Features: None.

General Items:

- Overall package: The device was packaged in a 240-pin PQFP. A large copper heat slug (heatsink) was employed on the top of the package (cavity down orientation). It was internally connected to GND and the substrate.
- Wirebonding method: A thermosonic ball bond technique employing 1.2 mil gold wire was used. All bonds were well formed and placed. Bond strengths were normal as determined by wire pull tests.
- Dicing: Sawn (full depth). No large chips or cracks were noted.
- Die attach: A silver epoxy compound of normal quality.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 4 - 45

Questionable Items:¹

- Metal 2 aluminum thinned up to 90 percent² at vias (Figure 16).

Special Features:

- Sub-micron gate lengths (0.55 micron).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate.
- Process implementation: Die layout was clean efficient. Alignment was good at all levels.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.
- Passivation: A layer of nitride over a layer of silicon-dioxide. Passivation coverage and edge seal were good.
- Metallization: Two levels of metallization. Metal 2 consisted of aluminum with titanium-nitride cap and titanium barrier. Metal 1 consisted of aluminum, titanium-nitride cap and barrier, and a titanium adhesion layer. Standard vias were used between metal 2 and 1. Tungsten plugs were employed under metal 1.

¹These items present possible quality concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

ANALYSIS RESULTS II (continued)

- Metal patterning: All metal layers were defined by a dry etch of good quality.
- Metal defects: None. No voiding, notching or cracking of the metal layers was found. No silicon nodules were found following removal of the aluminum.
- Metal step coverage: Metal 2 aluminum thinned up to 90 percent at most vias. The barrier aided in retaining the connections. Virtually no metal thinning was noted in metal 1. The tungsten plugs were nearly level with the oxide surface, so no large steps were present for the metal to cover.
- Vias and contacts: Vias were defined by a two step process while contacts were defined by a dry-etch. No significant over-etching was noted.
- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide with a spin-on-glass (SOG) to aid in planarization.
- Pre-metal dielectric: This dielectric consisted of a layer of reflow glass over densified oxide. No problems were found.
- Polysilicon: Two layers of polysilicon were employed. Poly 1 (polysilicon and tungsten silicide) formed the redundancy fuses, all gates on the die, and word lines in the array. Poly 2 was used to form resistors in the cell array and outside the fuse blocks. Definition was by a dry etch of good quality. No problems were found.
- Isolation: LOCOS (local oxide isolation). No problems were noted and no step was present at the well boundaries.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Deep (pushed down) N+ diffusions were noted under contacts in N regions. Diffusions were not silicided. No problems were found.

ANALYSIS RESULTS II (continued)

- Wells: Twin-wells were employed in a P substrate. No step was present at the well boundaries, but both wells were delineated by a silicon etch. No problems were noted.
- Buried contacts: Direct poly-to-diffusion (buried) contacts were only used in the SRAM array. No problems were found in these areas.
- Redundancy: Poly 1 fuses were present along the row and column decode logic outside the array. Passivation and interlevel dielectric cutouts were made over the fuses. Laser blown fuses were noted.
- Memory cells: The die employed a 2 Mbit SRAM array. The memory cells used a 4T CMOS SRAM cell design. Metal 2 distributed GND and Vcc, and formed the bit lines using metal 1 links. Metal 1 was used as the “piggy-back” word lines. Poly 1 formed the word lines, select, and storage gates. Poly 2 formed “pull-up” resistors and distributed Vcc. Cell size was 3.3 x 5.7 microns (19 microns²).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Delid

SEM of passivation

Passivation integrity test (chemical)

Wirepull test

Passivation removal

SEM inspection of metal 2

Aluminum 2 removal

Delayer to metal 1 and inspect

Aluminum 1 removal and inspect barrier

Delayer to polycide/substrate and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity:	G
Die placement:	G
Die attach quality:	G
Wire spacing:	N
Wirebond placement:	N
Wirebond quality:	G
Dicing quality:	G
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die attach method	Silver-epoxy
Dicing	Sawn (full depth)
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Contact registration	G

*Metal 2 aluminum thinning up to 90 percent.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

(LOGO) ANALOG DEVICES
ADSP-21062
9630 KS-160
HD/BA5454.1-1.2 (SHARC LOGO)

BOTTOM

S6 2A2
HONG KONG

WIREPULL TEST

<u>Sample</u>	1
# of wires tested:	22
Bond lifts:	0
Force to break - high:	12g
- low:	8g
- avg.:	9.1g
- std. dev.:	0.5

DIE MATERIAL IDENTIFICATION

Overlay passivation:	Nitride over silicon-dioxide.
Metallization 2:	Aluminum with a titanium-nitride cap and a titanium barrier.
Interlevel dielectric:	Multiple layers of silicon-dioxide.
Metallization 1: barrier, and a	Aluminum with a titanium-nitride cap and titanium adhesion layer.
Plugs:	Tungsten.
Pre-metal glass:	Silicon-dioxide.
Silicide (Poly 1):	Tungsten.

VERTICAL DIMENSIONS

Die thickness: 0.5 mm (21 mils)

Layers

Passivation 2: 0.6 micron

Passivation 1: 0.15 micron

Metal 2 - cap: 0.05 micron (approx.)

- aluminum: 0.75 micron

- barrier: 0.17 micron

Interlevel dielectric - glass 2: 0.5 micron (average)

- glass 1: 0.15 micron (average)

Metal 1 - cap: 0.05 micron (approx.)

- aluminum: 0.5 micron

- barrier: 0.1 micron

- plugs: 0.6 - 1.0 micron

Pre-metal glass: 0.6 micron (average)

Polycide - silicide: 0.1 micron

- poly: 0.13 micron

Local oxide: 0.4 micron

N+ S/D diffusion: 0.2 micron

Deep N+ S/D diffusion: 0.4 micron

P+ S/D diffusion: 0.2 micron

N-well: 2.0 microns (approx.)

P-well: 2.5 microns (approx.)

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EEPROM MEMORY CELL STRUCTURES	Figures 32 - 40
CIRCUIT LAYOUT AND I/O	Figures 41 - 46

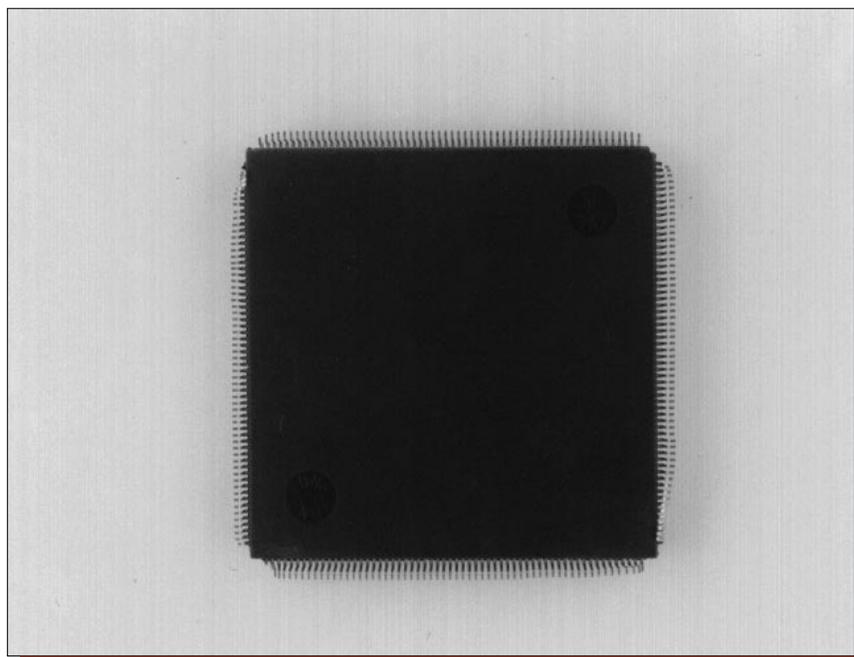
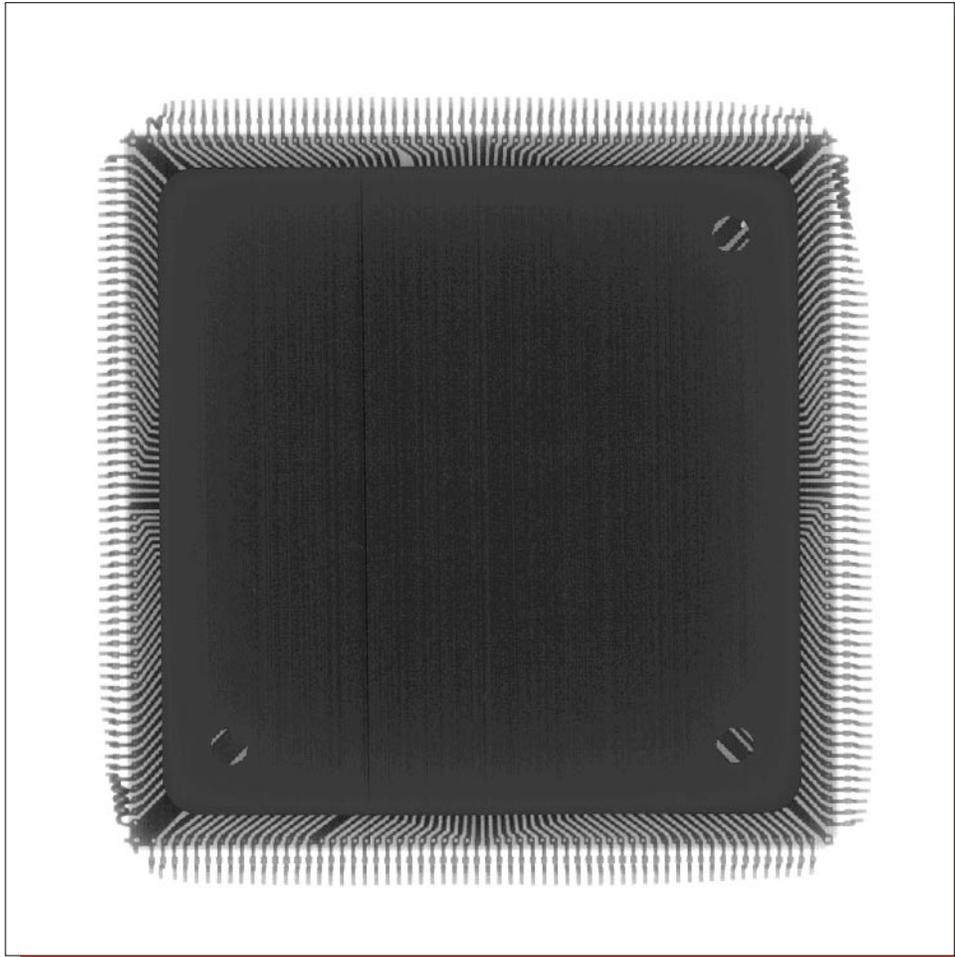


Figure 1. Package photographs of the Analog Devices ADSP-21062-KS-160 SHARC Digital Signal Processor. Mag. 1.5x.

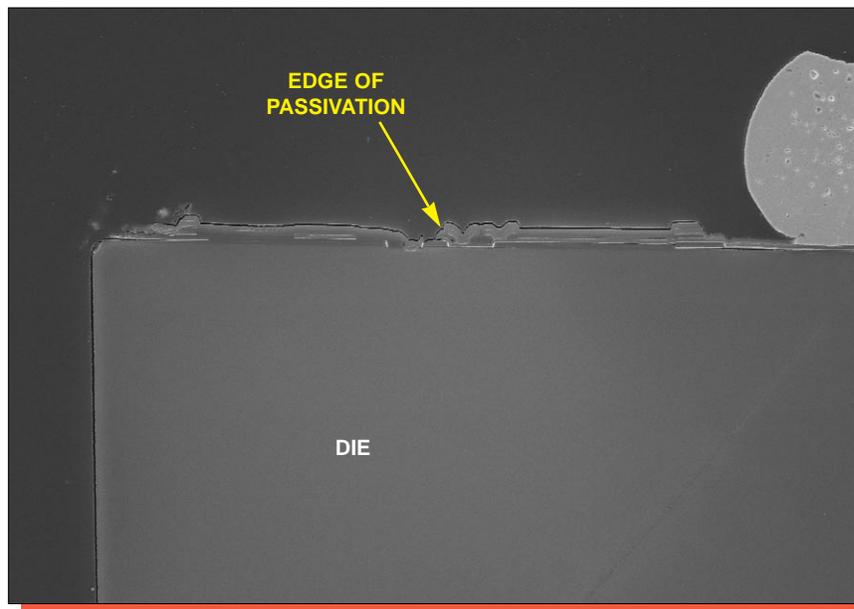


top

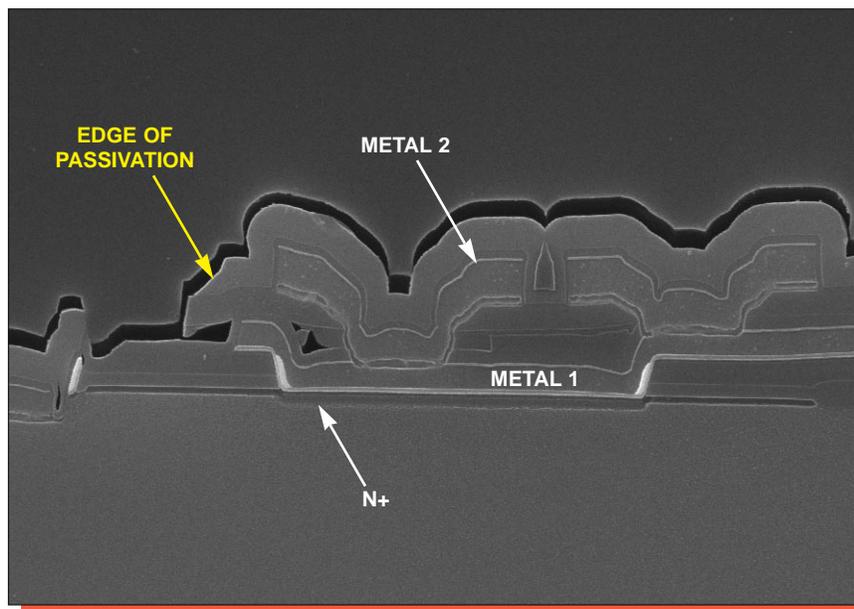


side

Figure 2. X-ray views of the package. Mag. 3x.



Mag. 800x



Mag. 6500x

Figure 3. SEM section views of the edge seal.

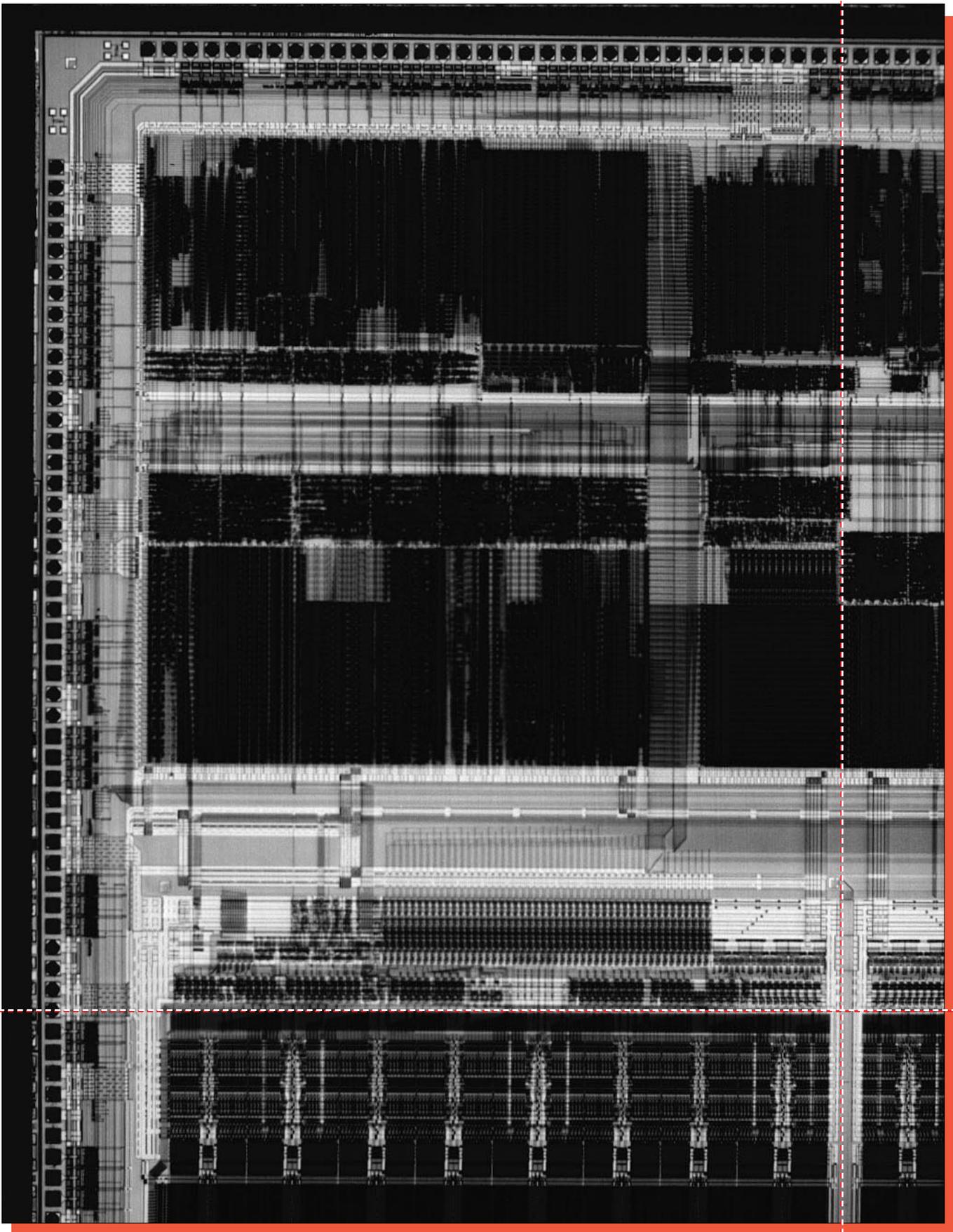


Figure 4. Portion of the Analog Devices ADSP-21062-KS-160 whole die. Mag. 26x.

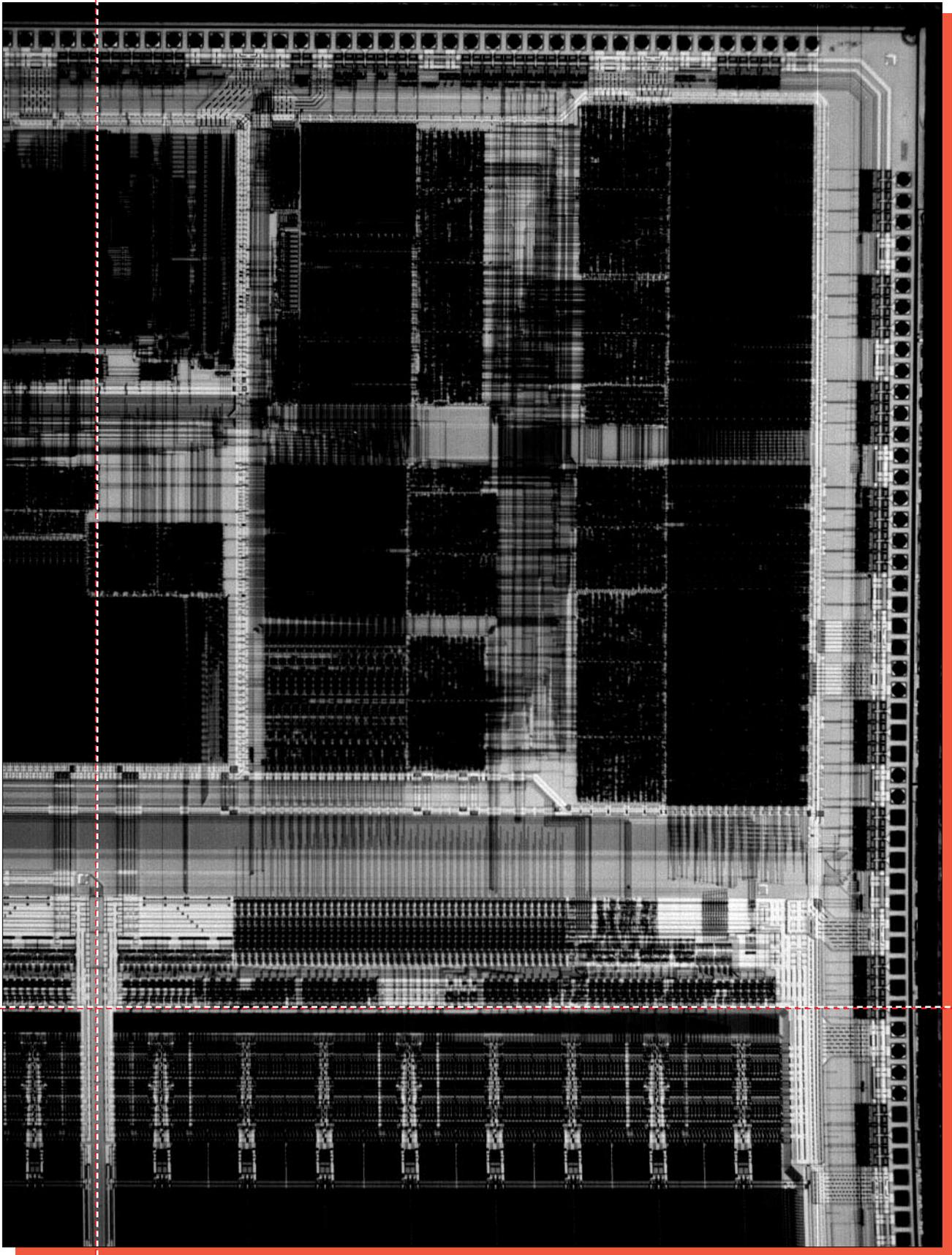


Figure 5. Portion of the Analog Devices ADSP-21062-KS-160 whole die. Mag. 26x.

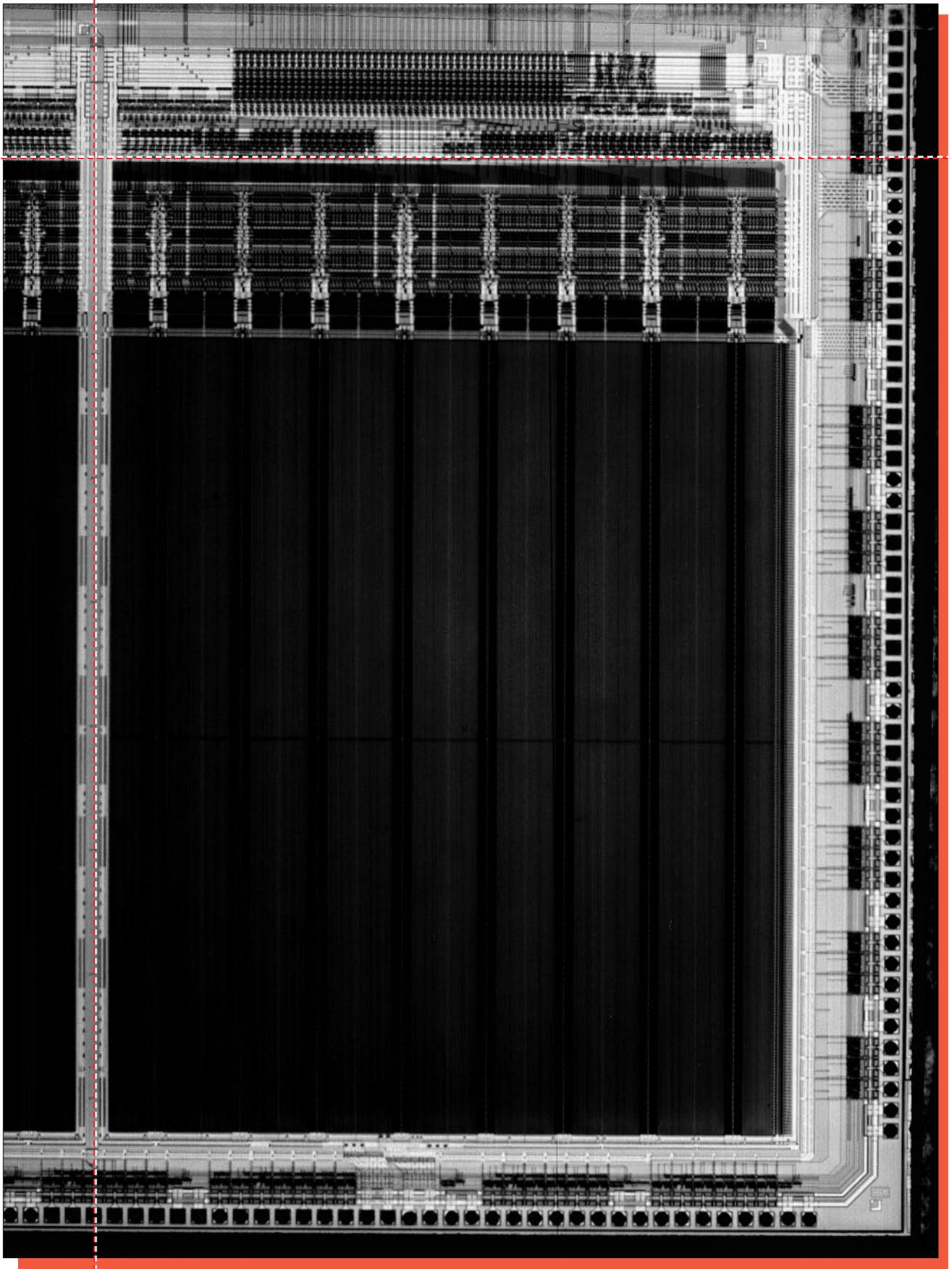


Figure 6. Portion of the Analog Devices ADSP-21062-KS-160 whole die. Mag. 26x.

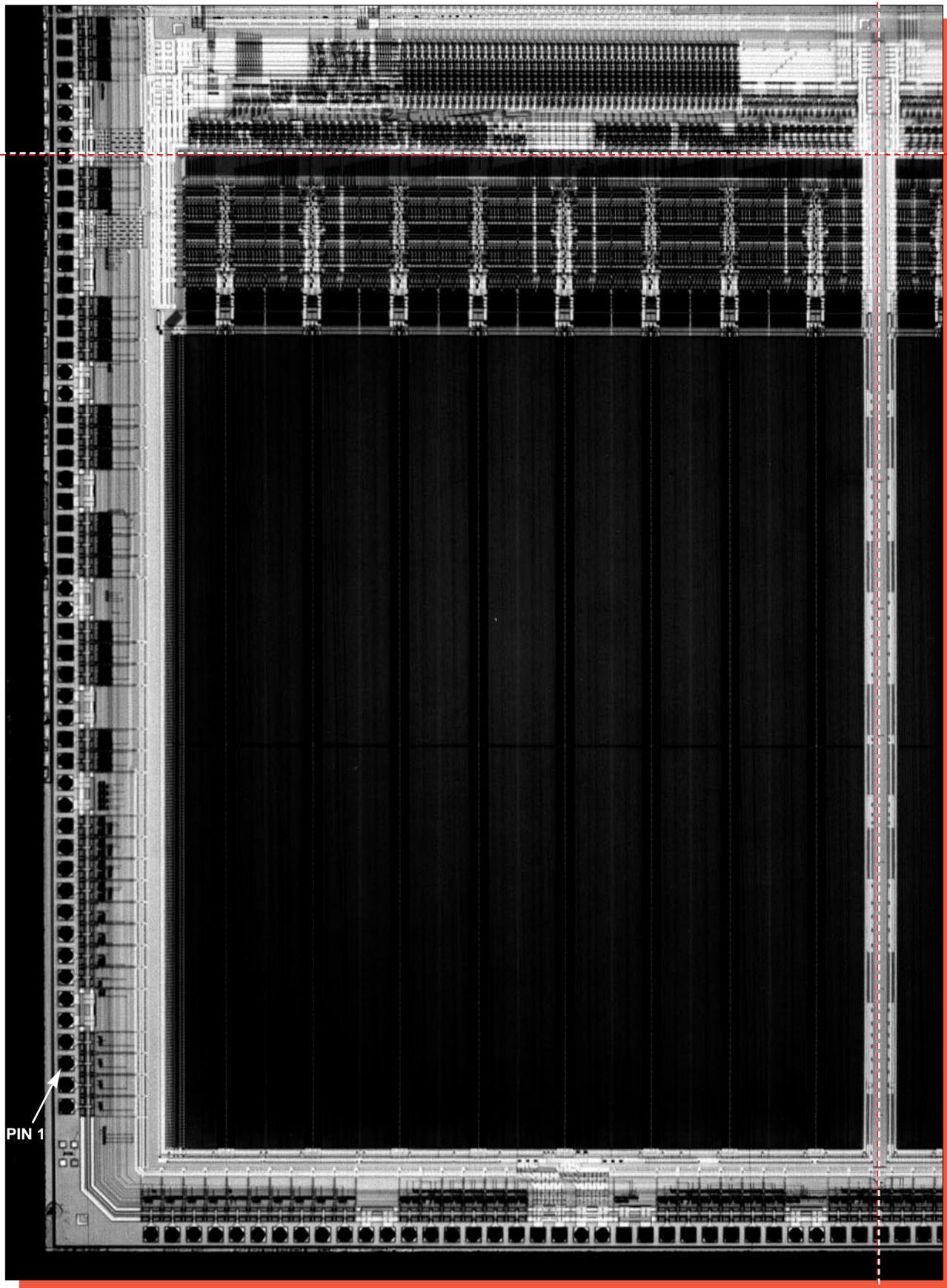


Figure 7. Remaining portion of the Analog Devices ADSP-21062-KS-160 whole die. Mag. 26x.

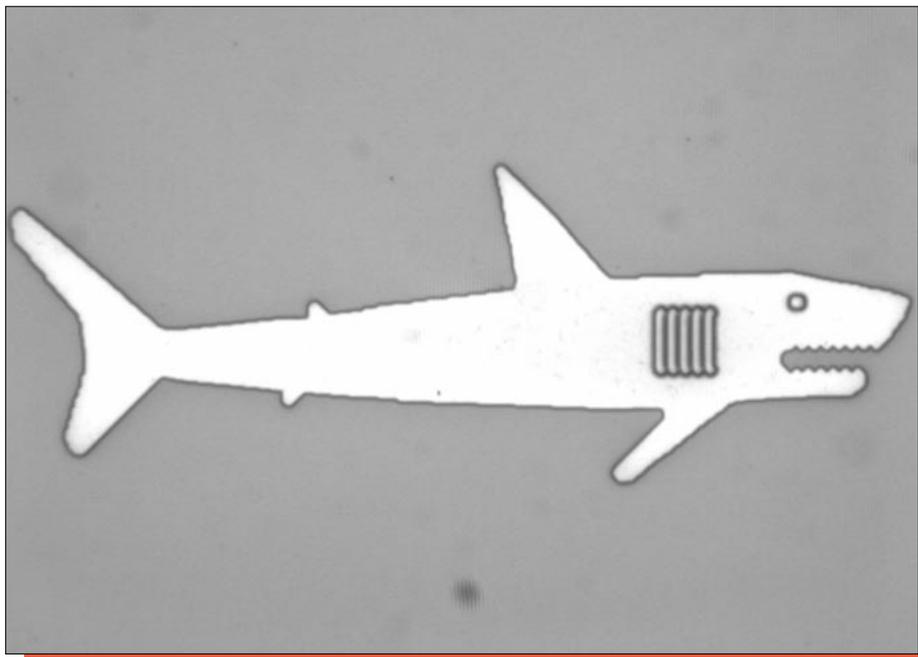


Figure 8. Optical views of die markings. Mag. 750x.

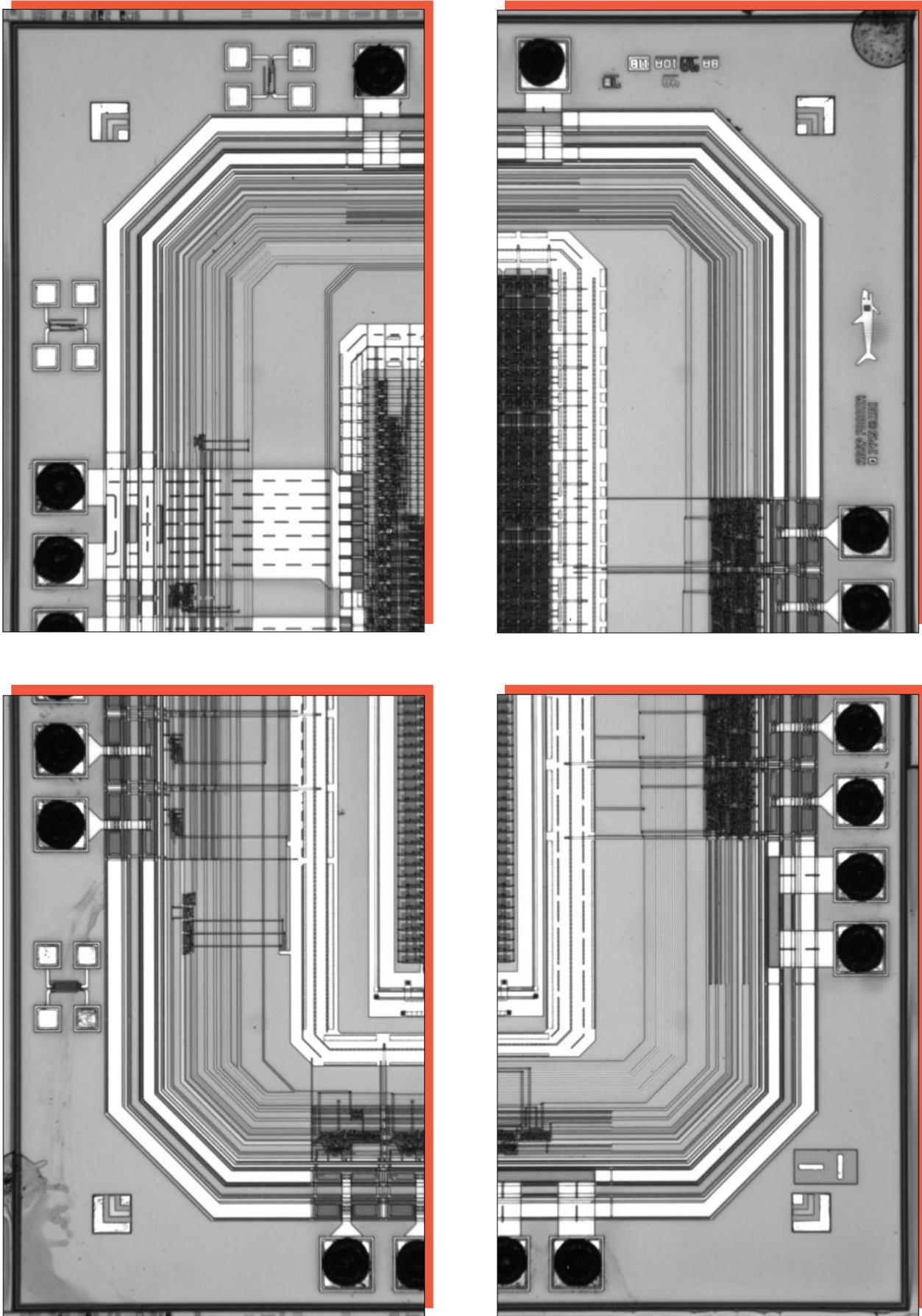


Figure 9. Optical views of die corners. Mag. 80x.

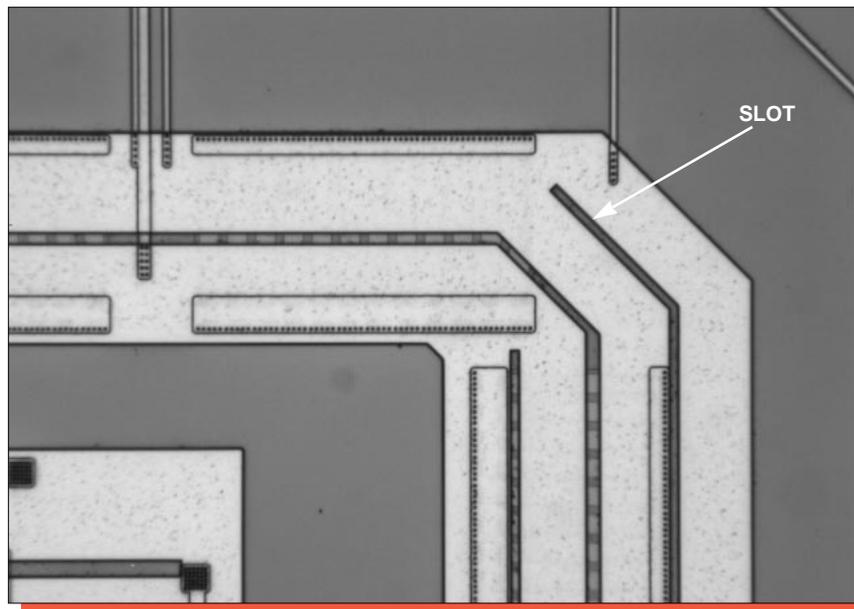
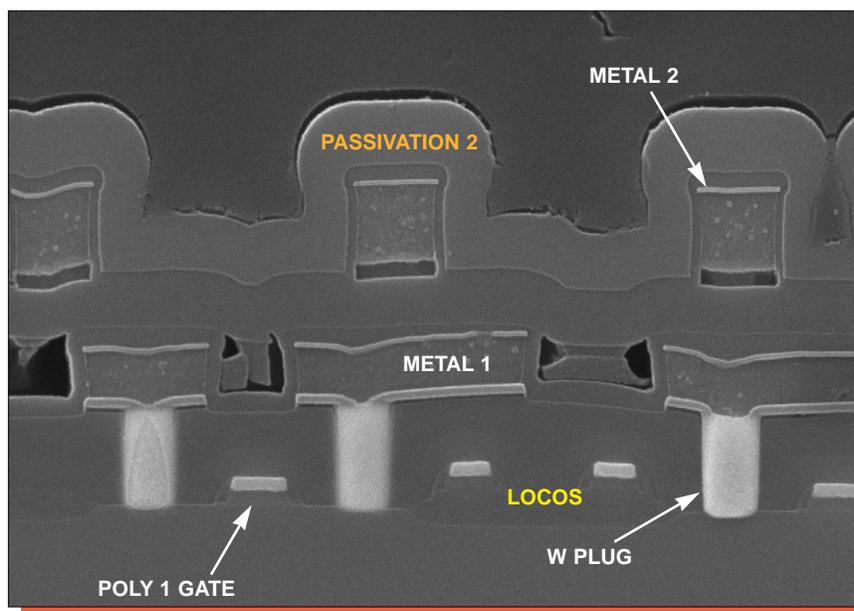
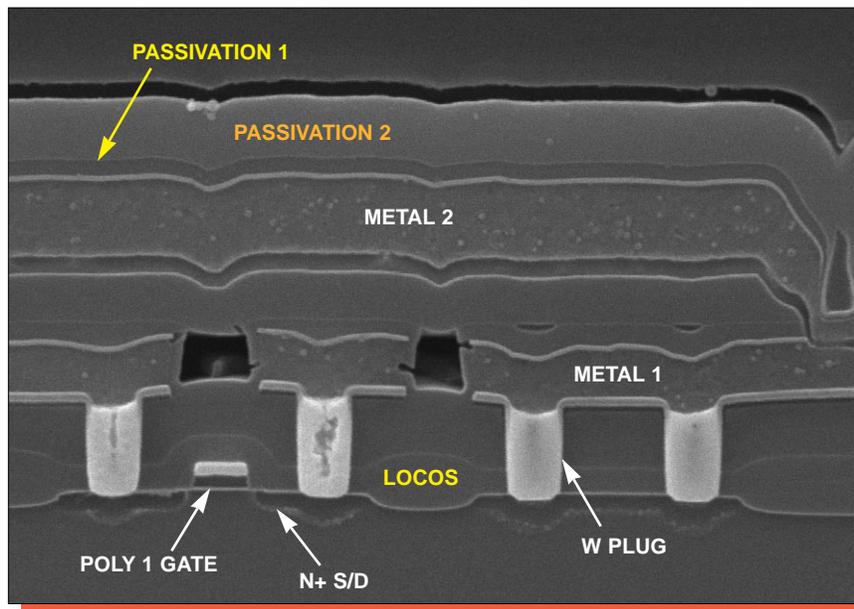
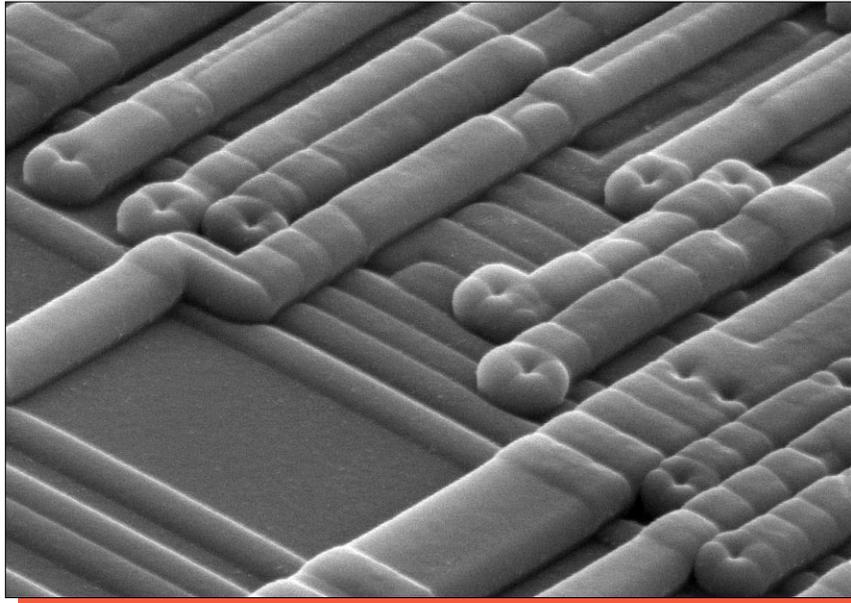


Figure 10. Optical views illustrating a slotted bus line and resolution patterns.
Mag. 410x.

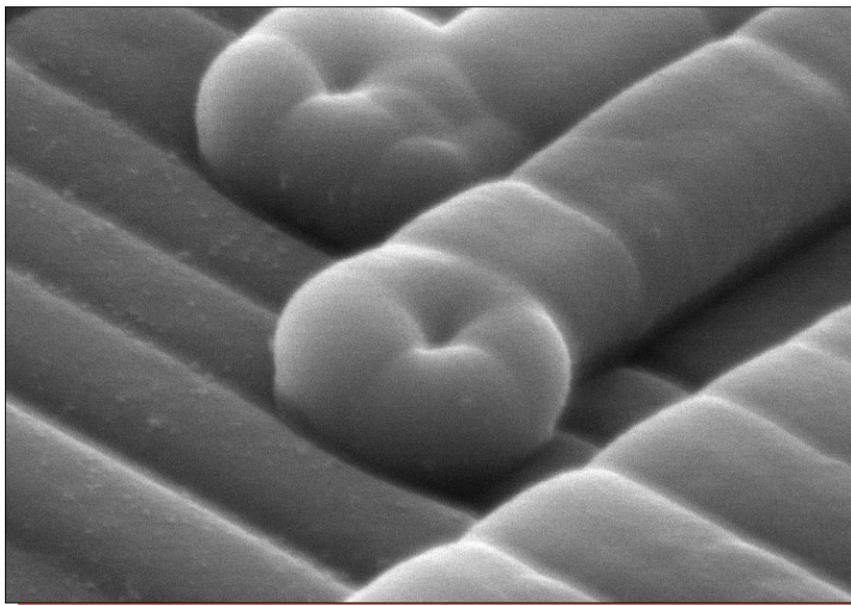


glass etch

Figure 11. SEM section views illustrating general structure. Mag. 13,000x.

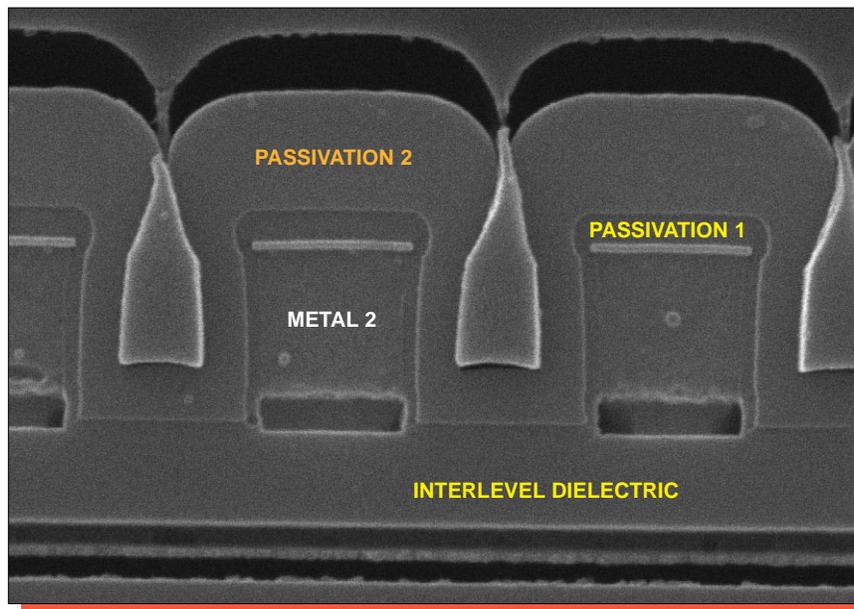


Mag. 4600x

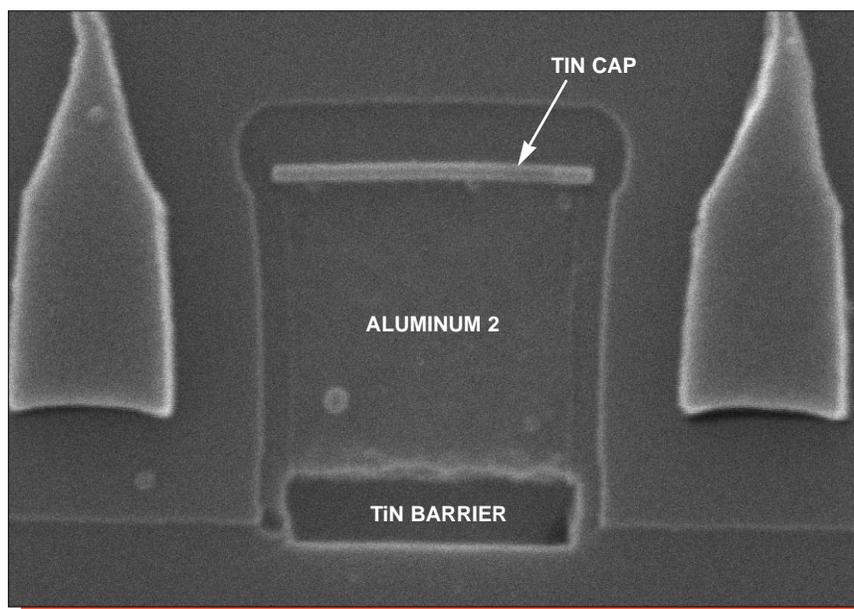


Mag. 15,000x

Figure 12. SEM views illustrating final passivation. 60°.

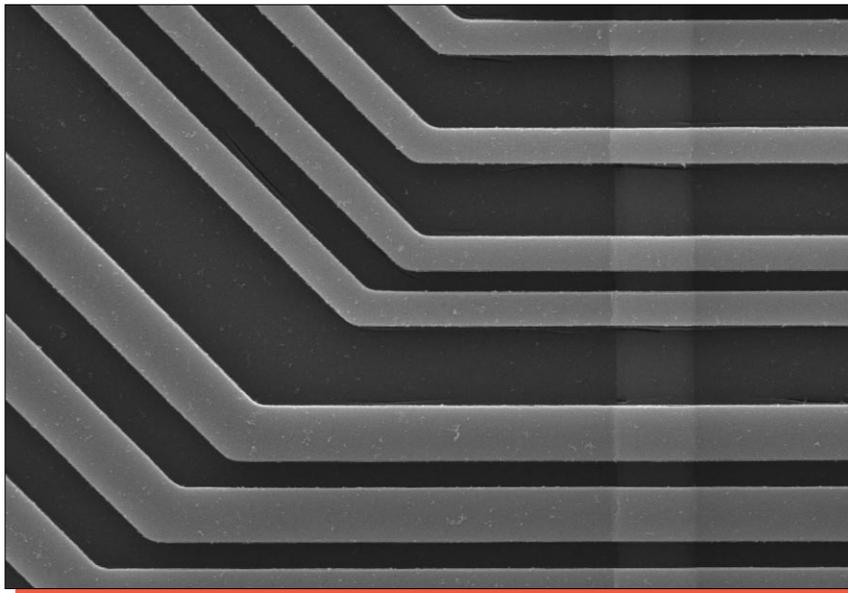


Mag. 26,000x

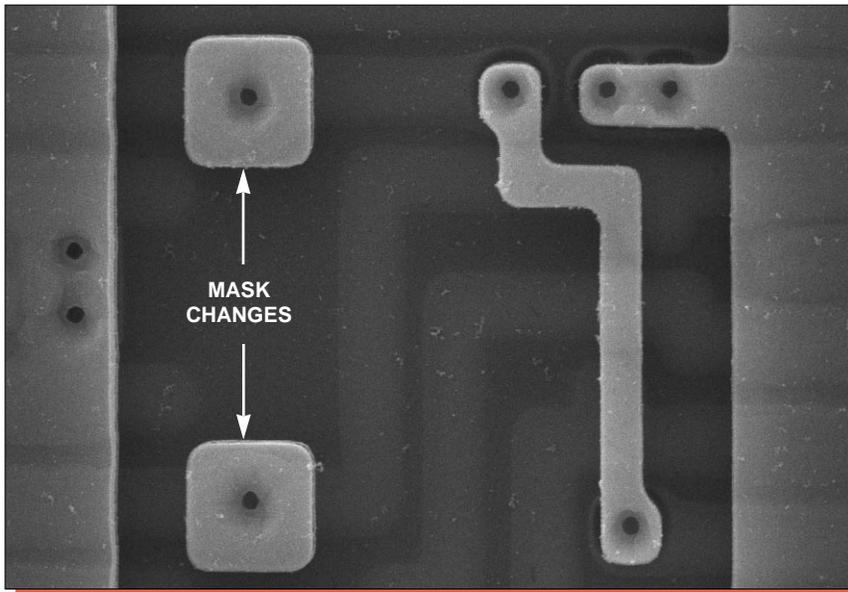


Mag. 52,000x

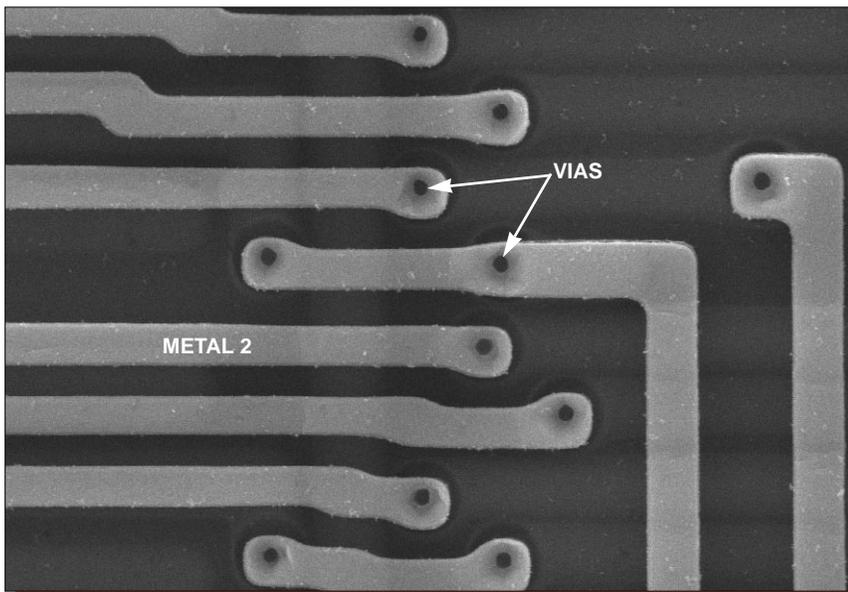
Figure 13. SEM section views illustrating metal 2 line profiles.



Mag. 3200x

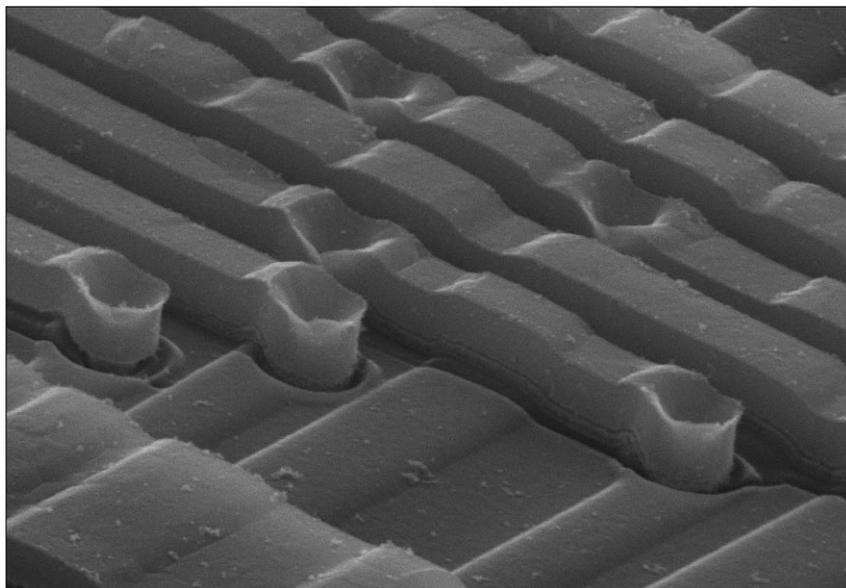


Mag. 6500x

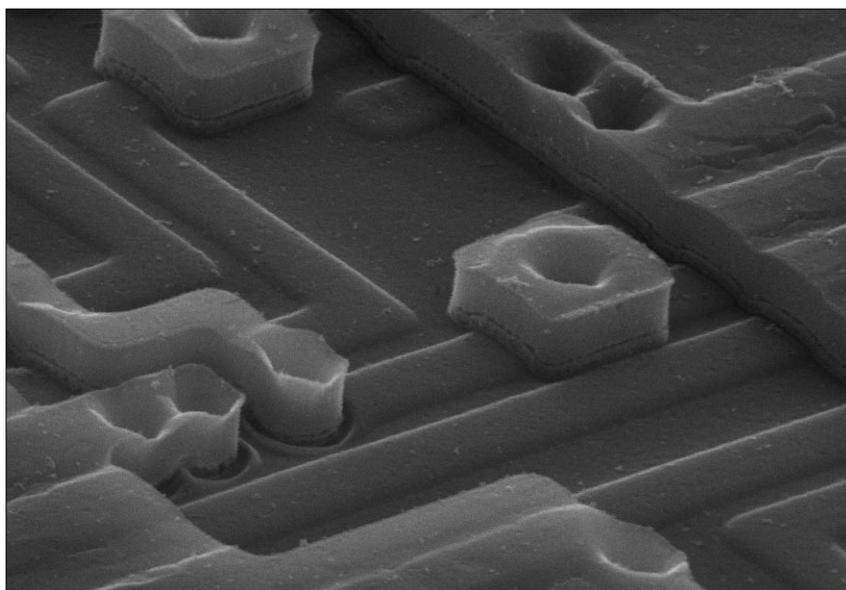


Mag. 6500x

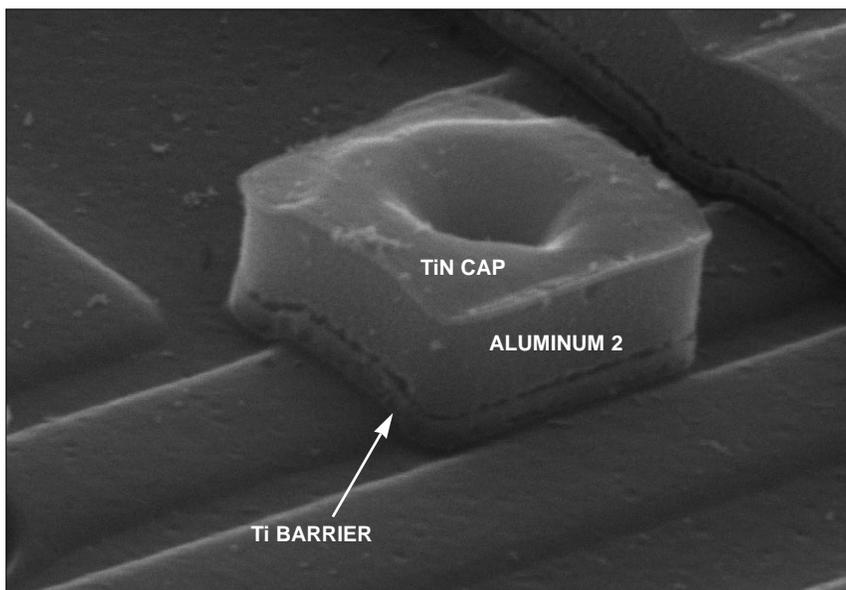
Figure 14. Topological SEM views of metal 2 patterning. 0°.



Mag. 10,000x

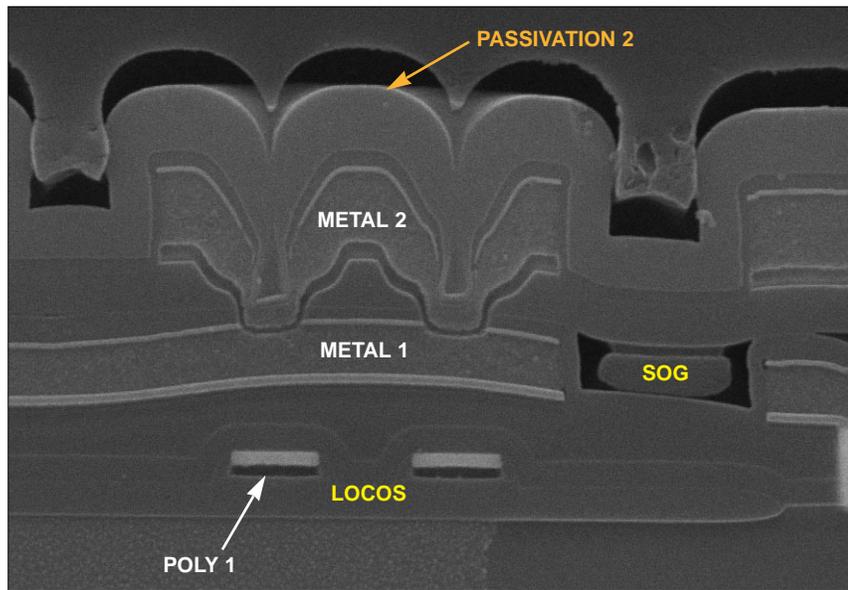


Mag. 10,000x

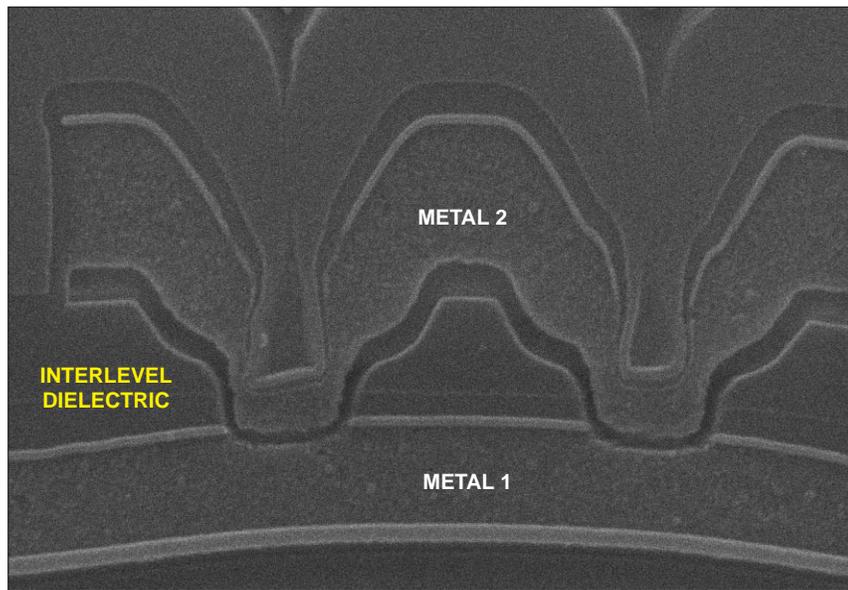


Mag. 20,000x

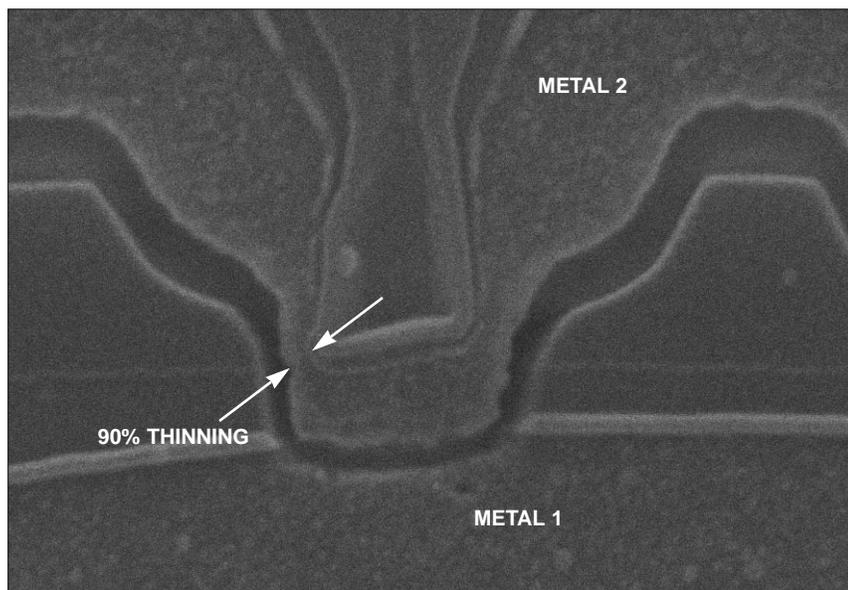
Figure 15. Perspective SEM views of metal 2 step coverage. 60°.



Mag. 13,000x

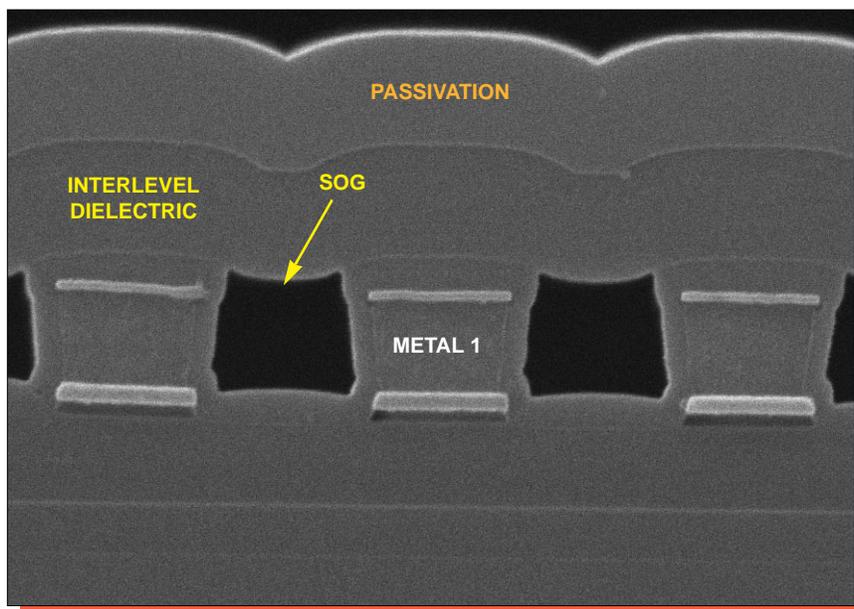


Mag. 26,000x

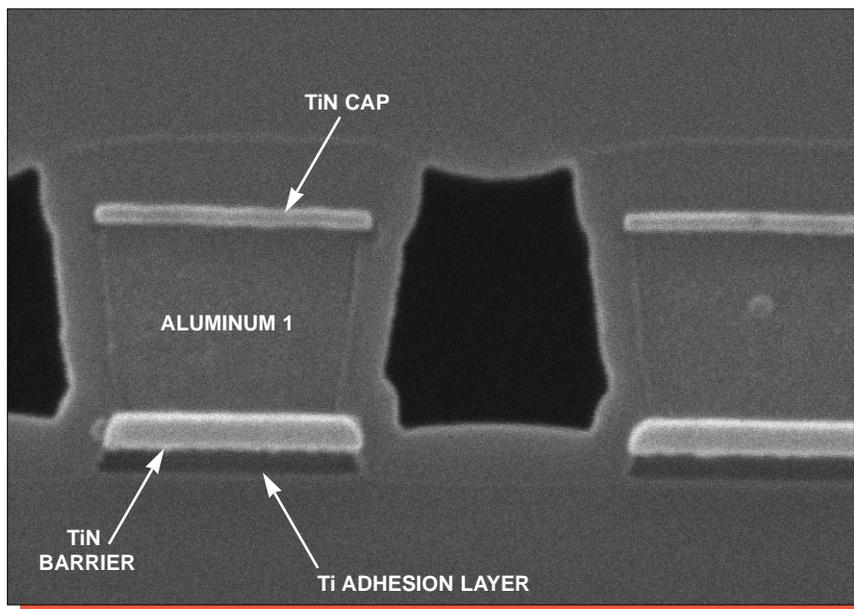


Mag. 52,000x

Figure 16. SEM section views of typical vias.



Mag. 26,000x



Mag. 52,000x

Figure 17. SEM section views of metal 1 line profiles.

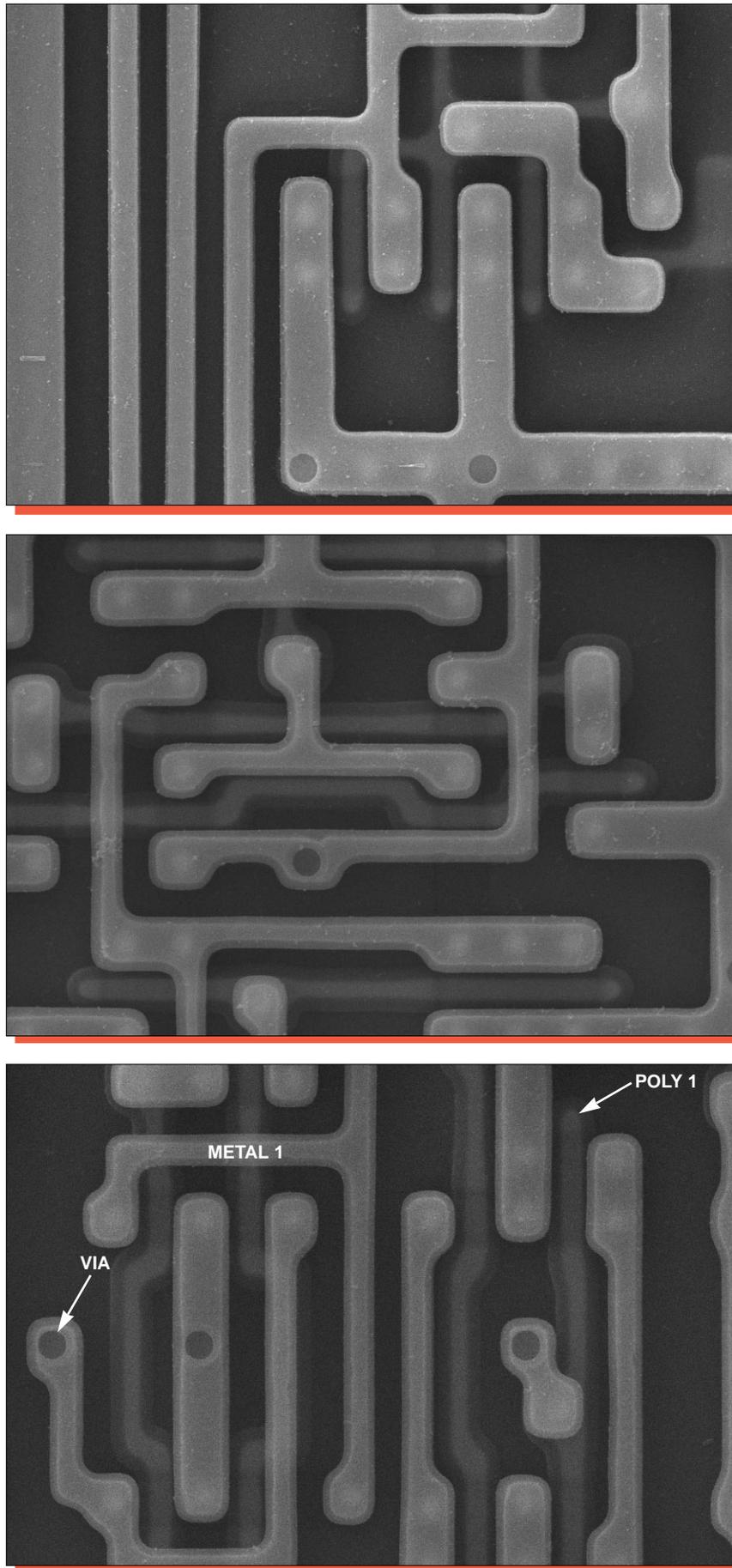
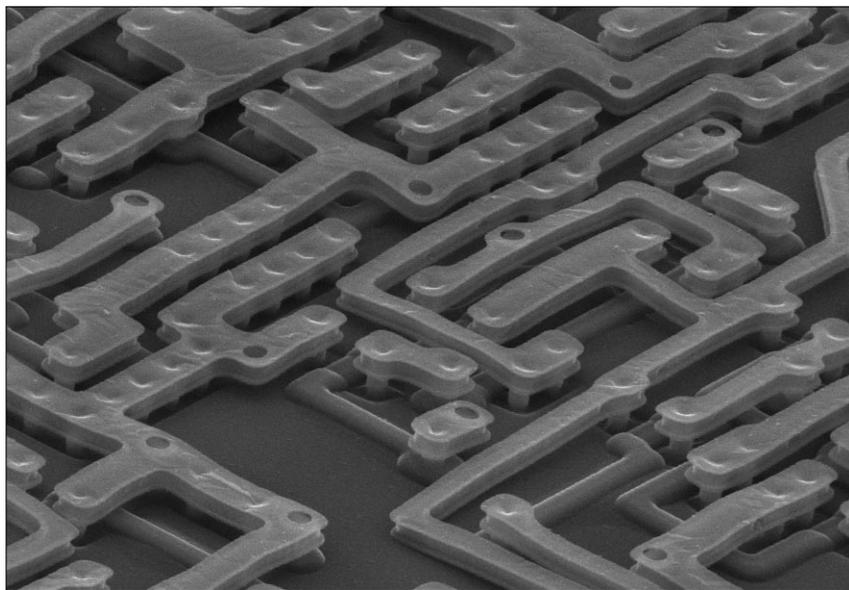
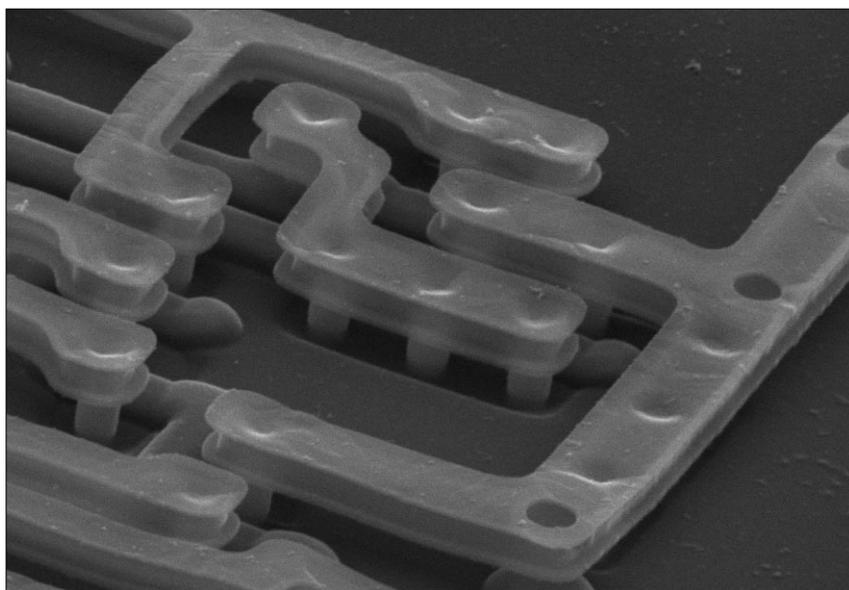


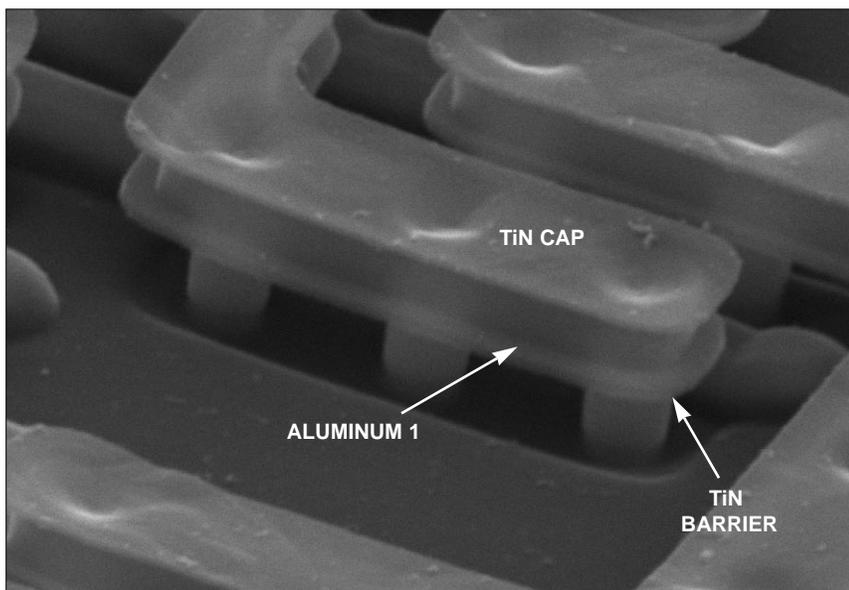
Figure 18. Topological SEM views of metal 1 patterning. Mag. 6500x, 0°.



Mag. 5000x

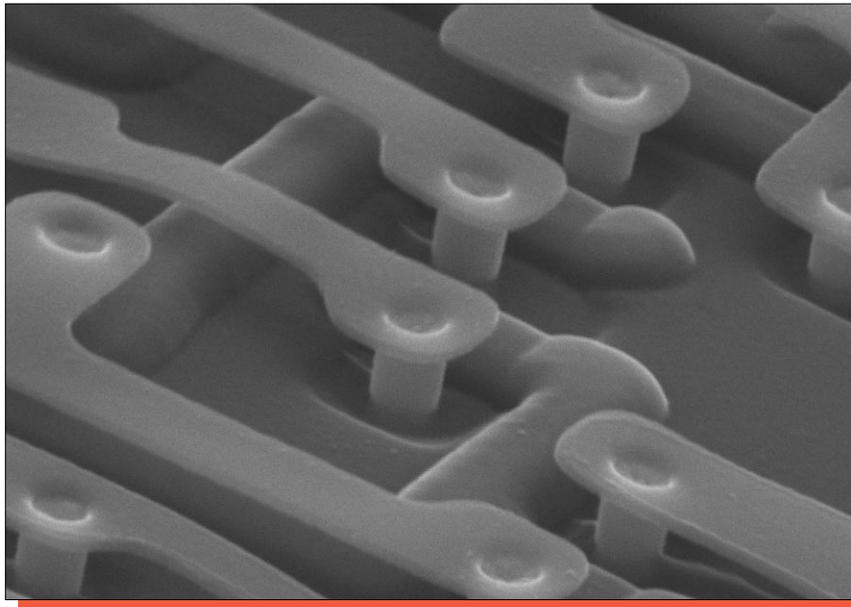


Mag. 10,000x

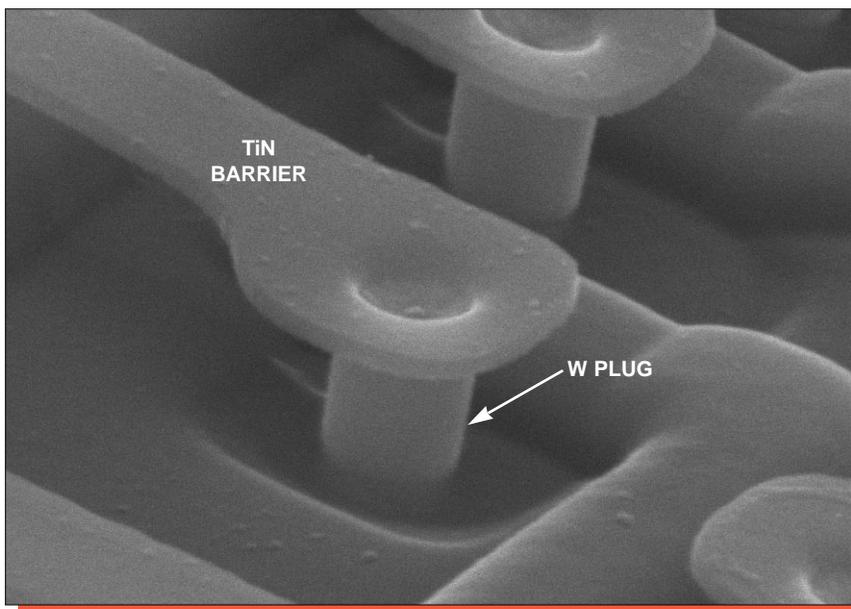


Mag. 20,000x

Figure 19. Perspective SEM views of metal 1 step coverage. 60°.



Mag. 16,000x



Mag. 32,000x

Figure 20. Perspective SEM views of metal 1 barrier and plug. 60°.

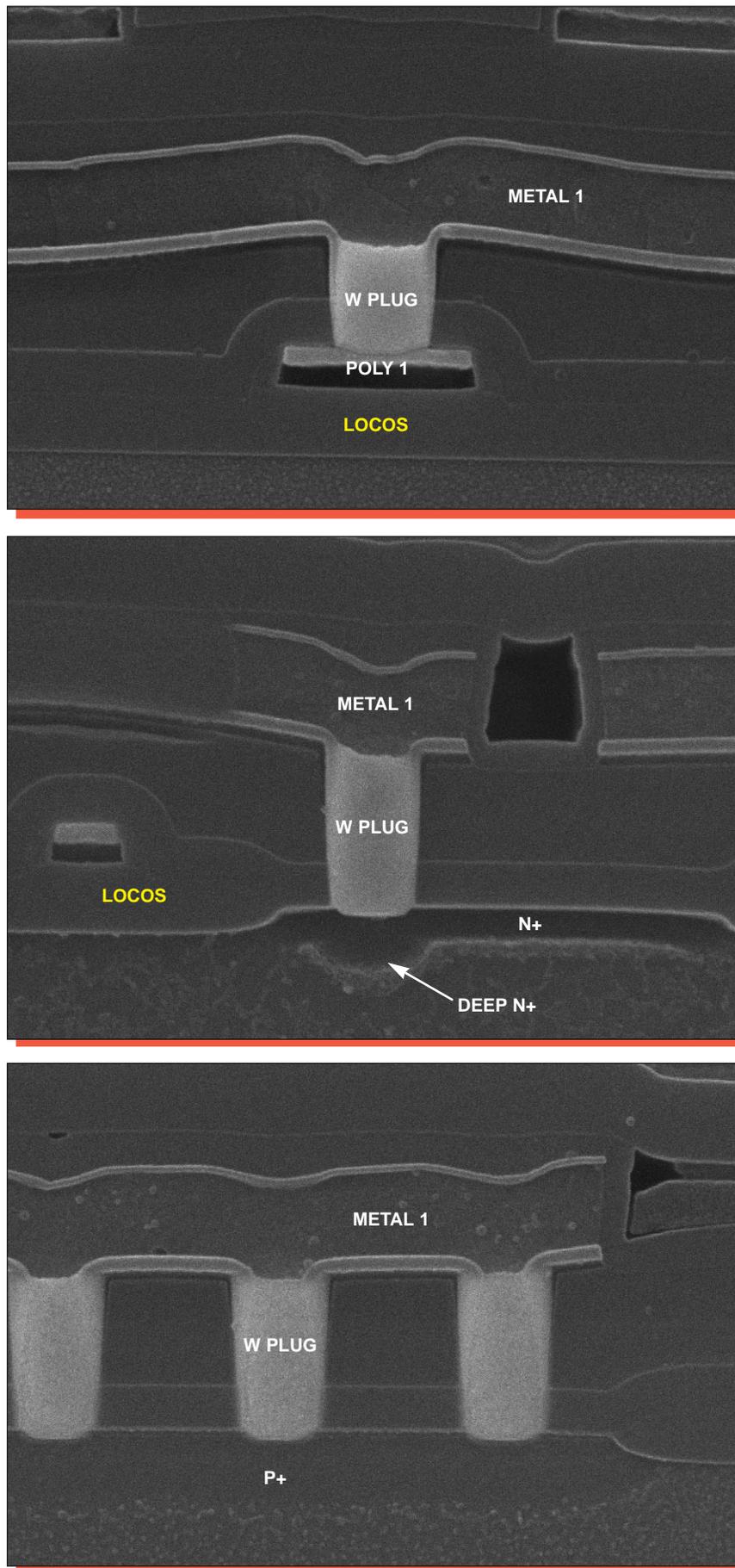
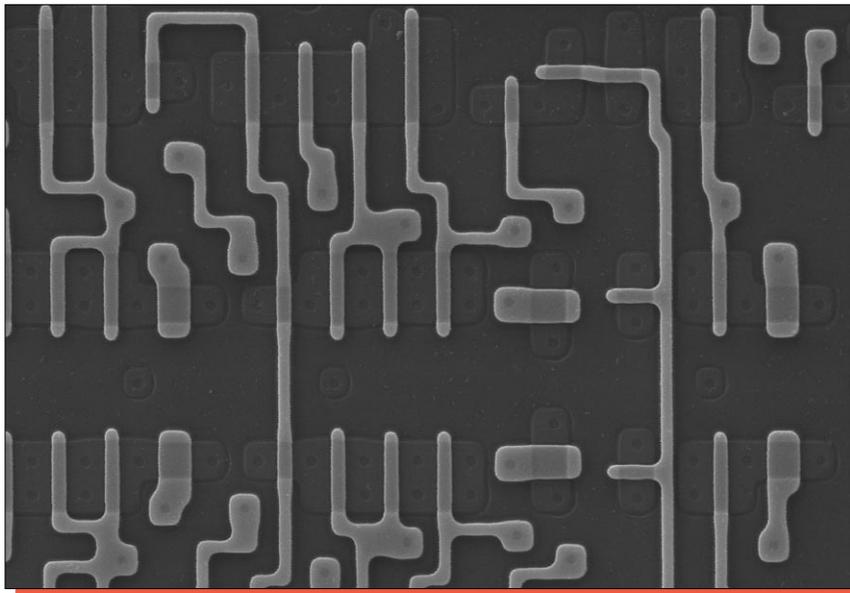
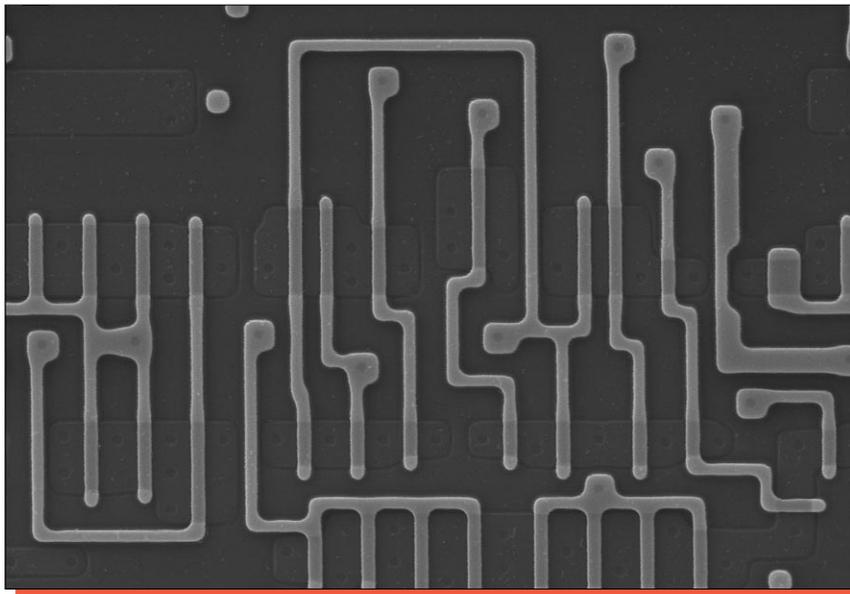


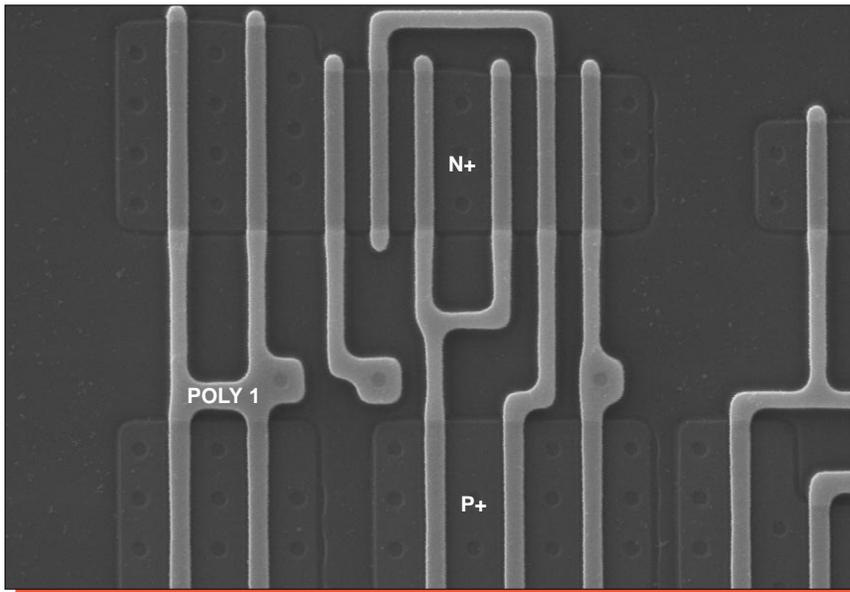
Figure 21. SEM section views illustrating typical metal 1 contacts. Mag. 26,000x.



Mag. 3200x

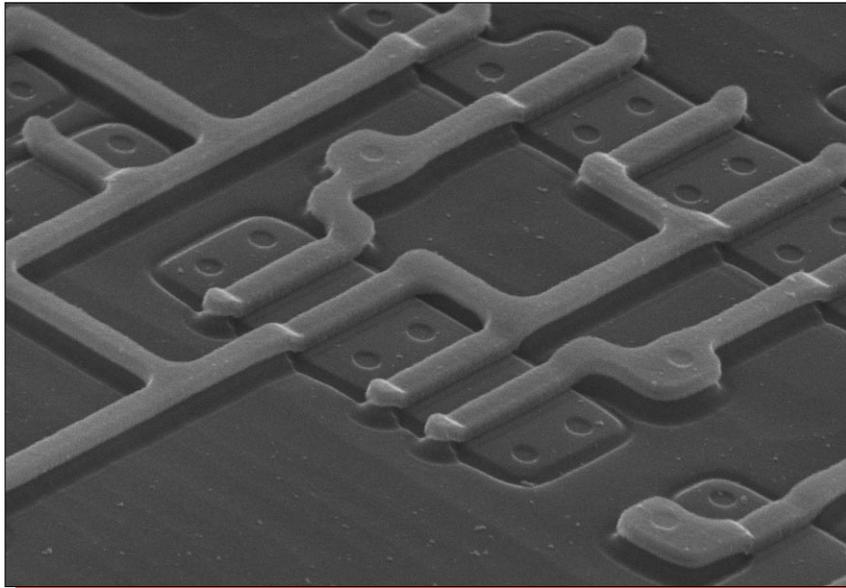


Mag. 3200x

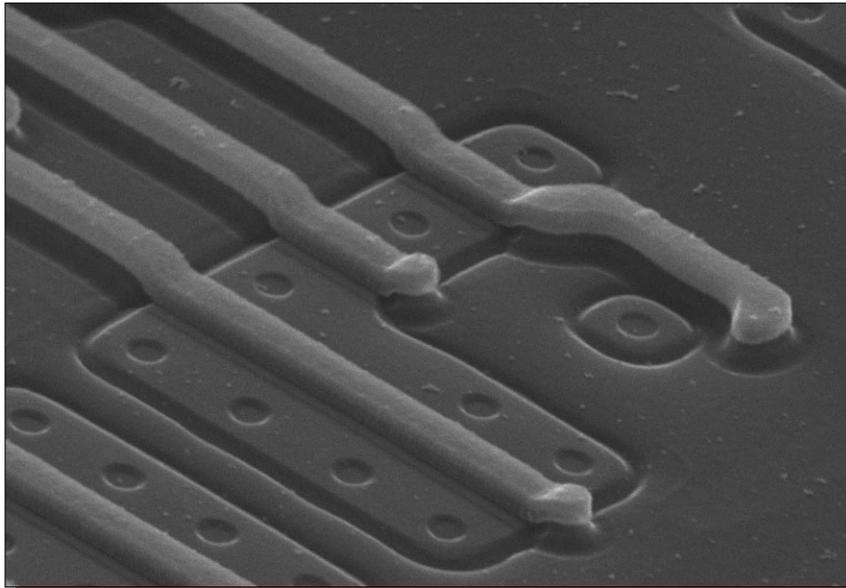


Mag. 5000x

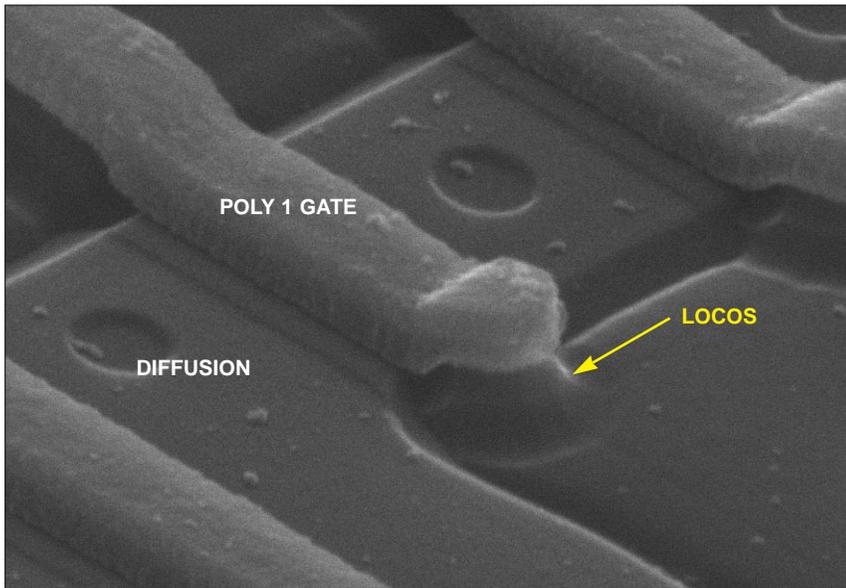
Figure 22. Topological SEM views of poly 1 patterning. 0°.



Mag. 8000x



Mag. 12,000x



Mag. 32,000x

Figure 23. Perspective SEM views of poly 1 coverage. 60°.

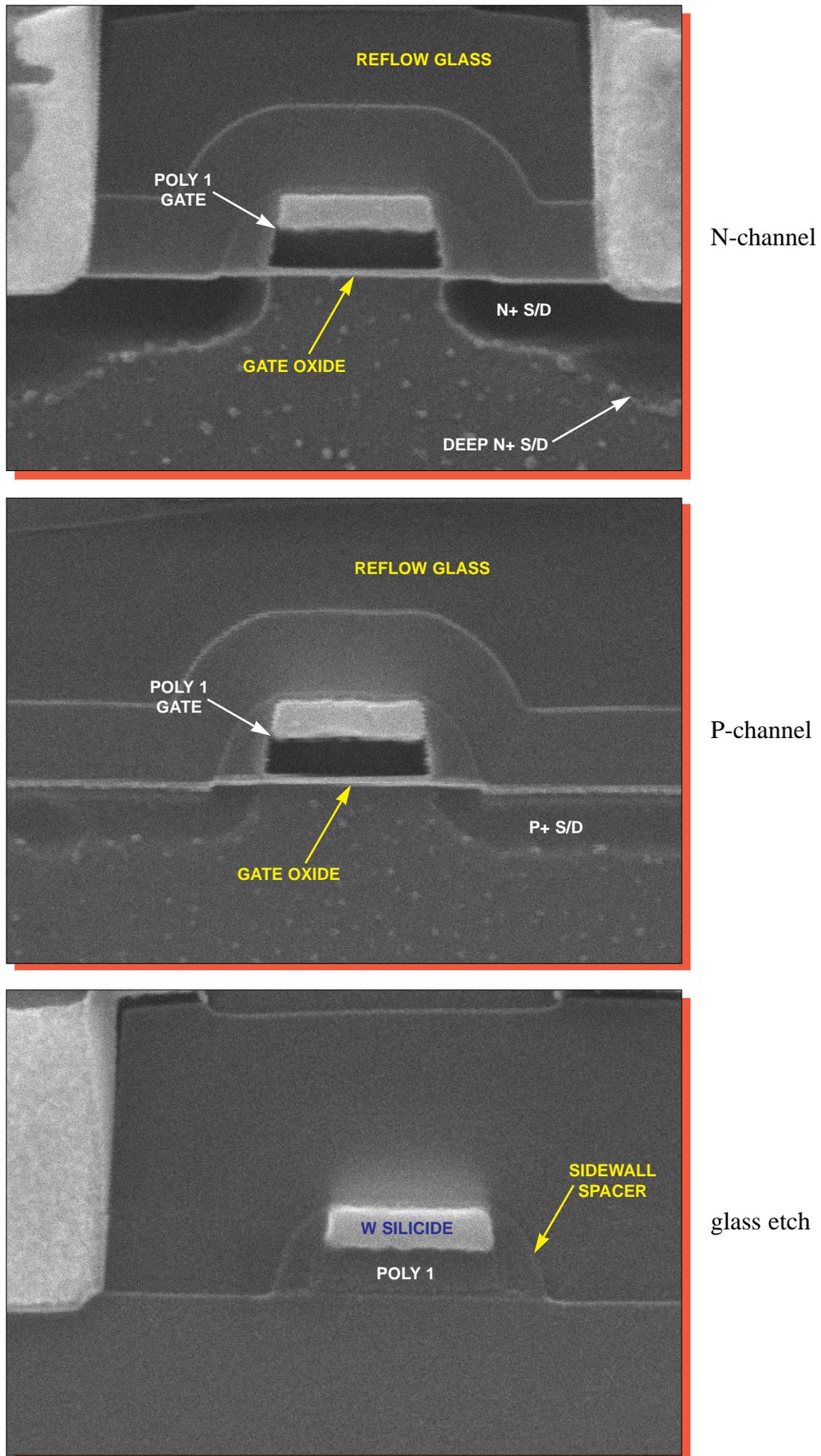


Figure 24. SEM section views of typical transistors. Mag. 52,000x.

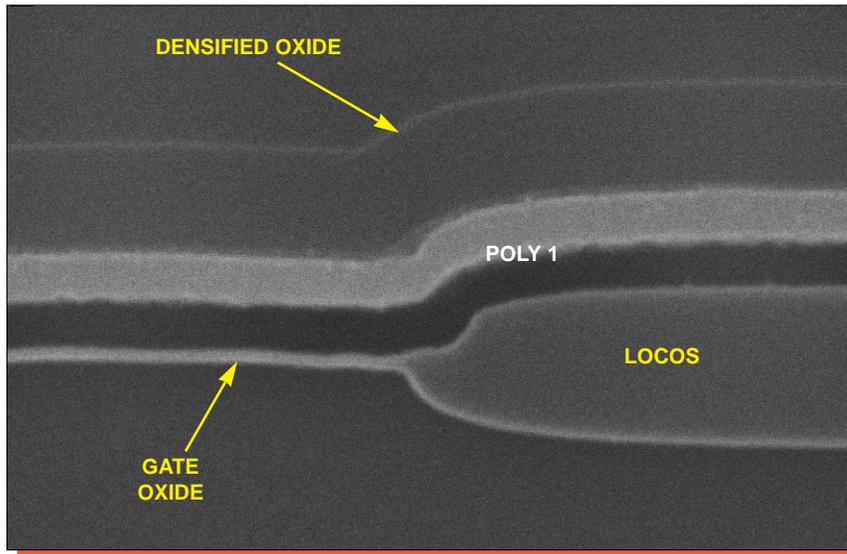
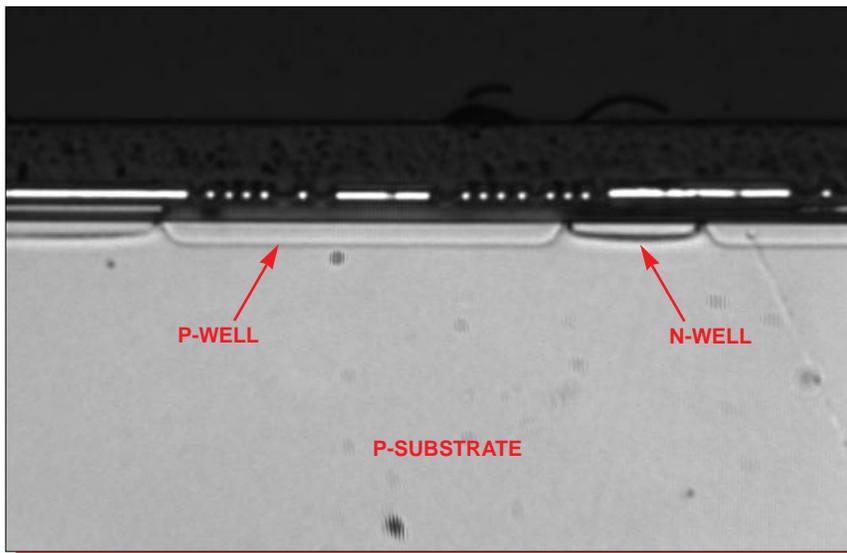
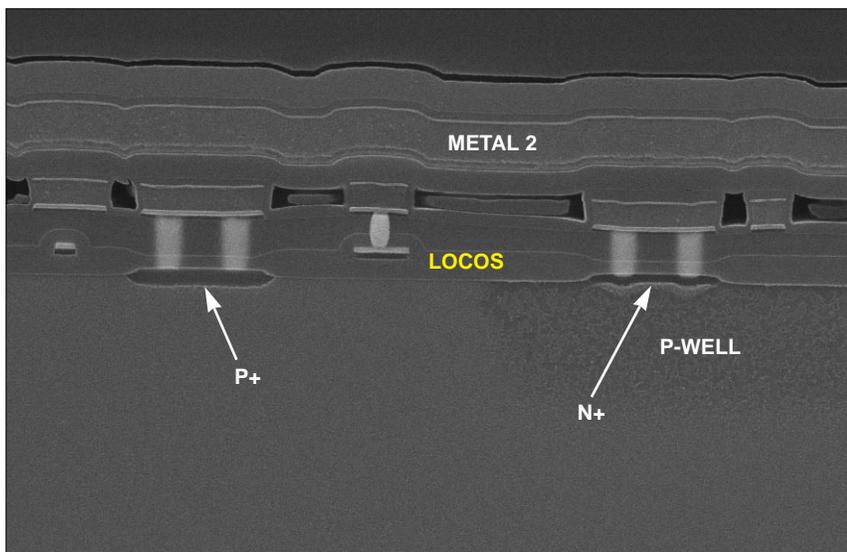


Figure 25. SEM section view of a typical birdsbeak. Mag. 52,000x.

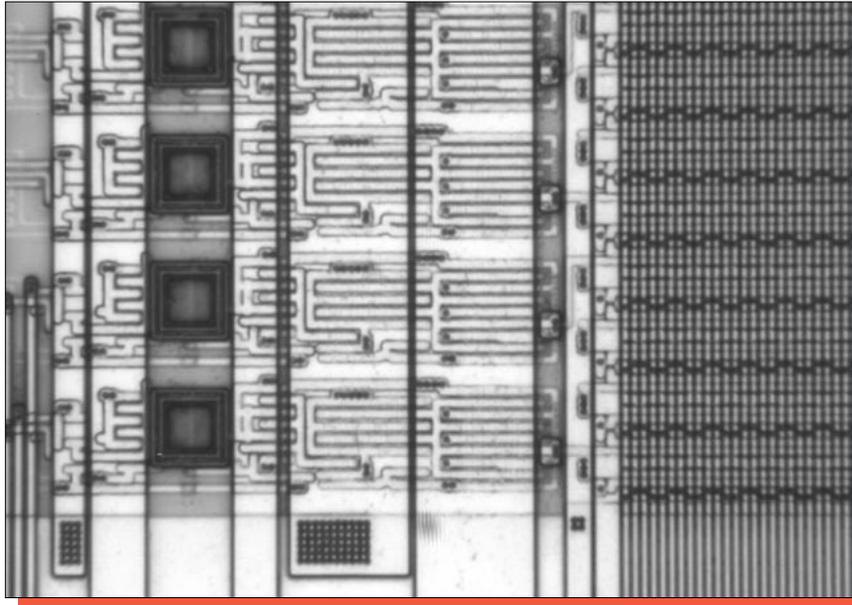


Mag. 1200x

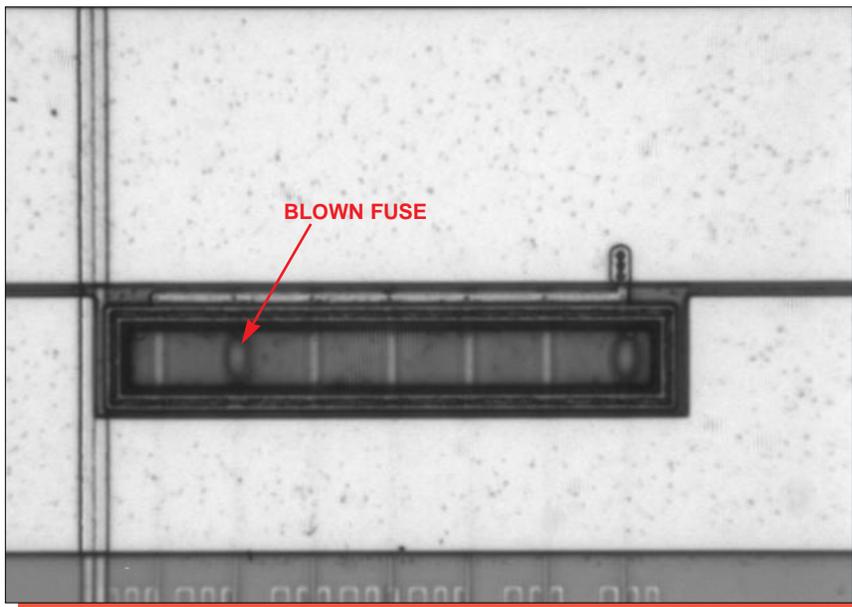


Mag. 6500x

Figure 26. Section views illustrating well structure.

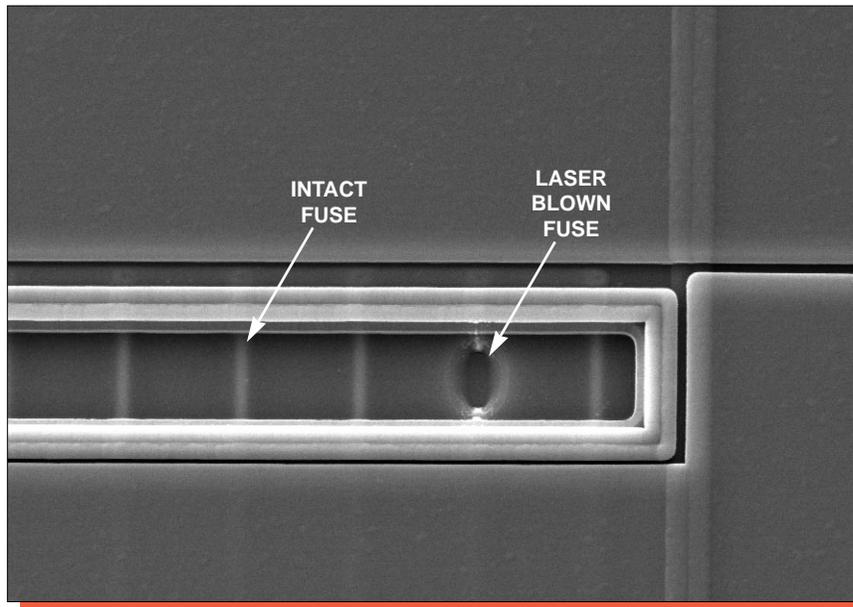


Mag. 750x

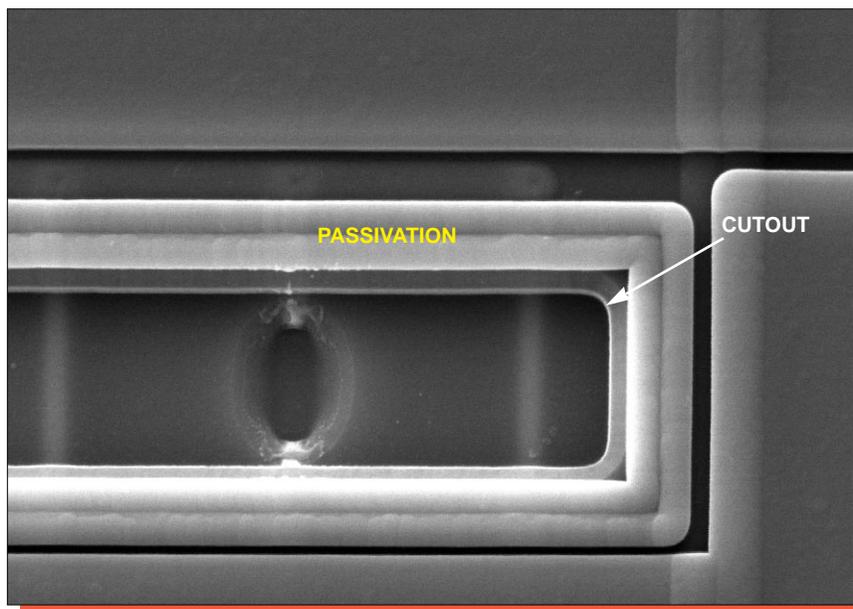


Mag. 1000x

Figure 27. Optical views of typical fuses.

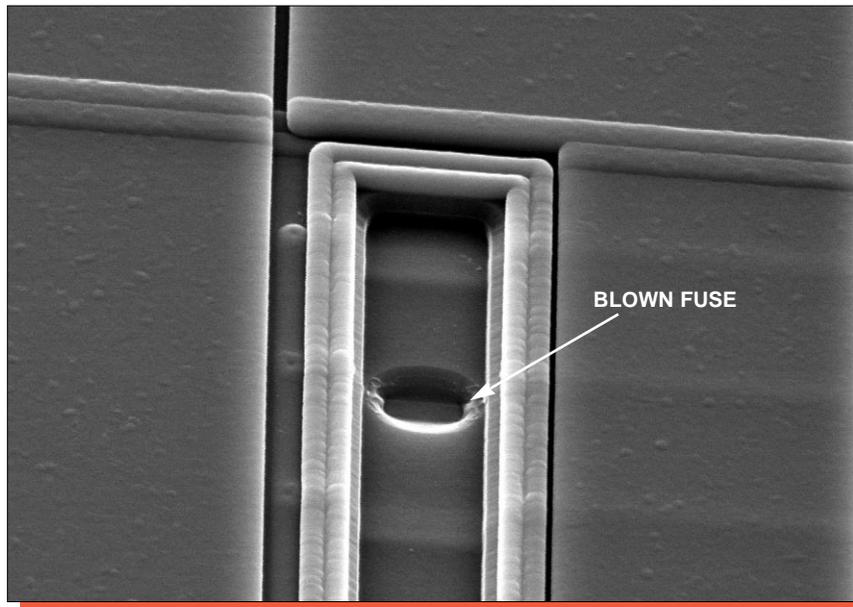


Mag. 1600x

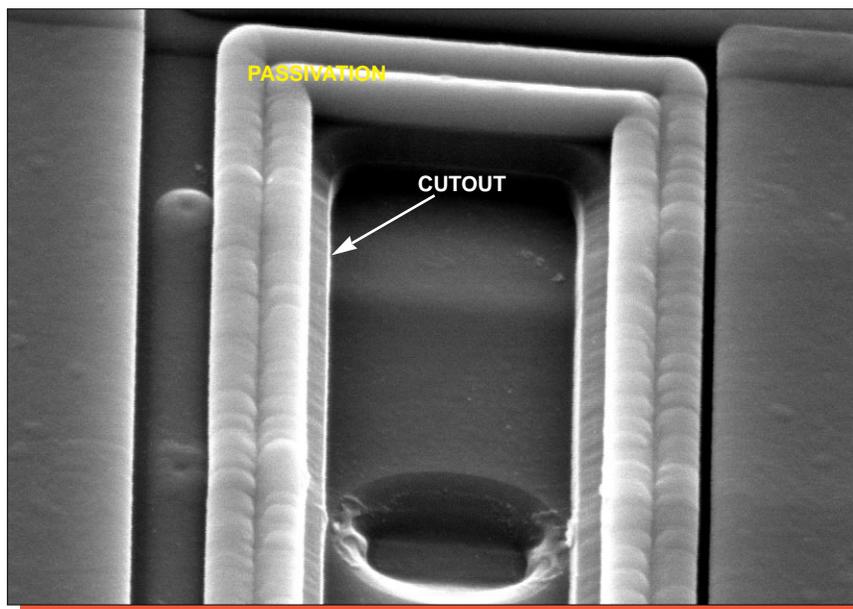


Mag. 3200x

Figure 28. Topological SEM views of typical fuses. 0°.



Mag. 2400x



Mag. 4800x

Figure 29. Perspective SEM views of typical fuses. 60°.

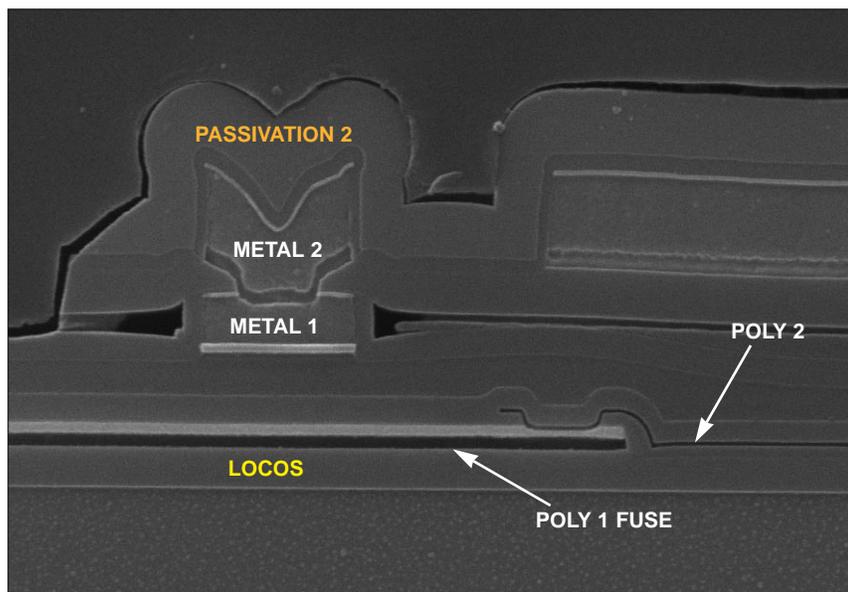
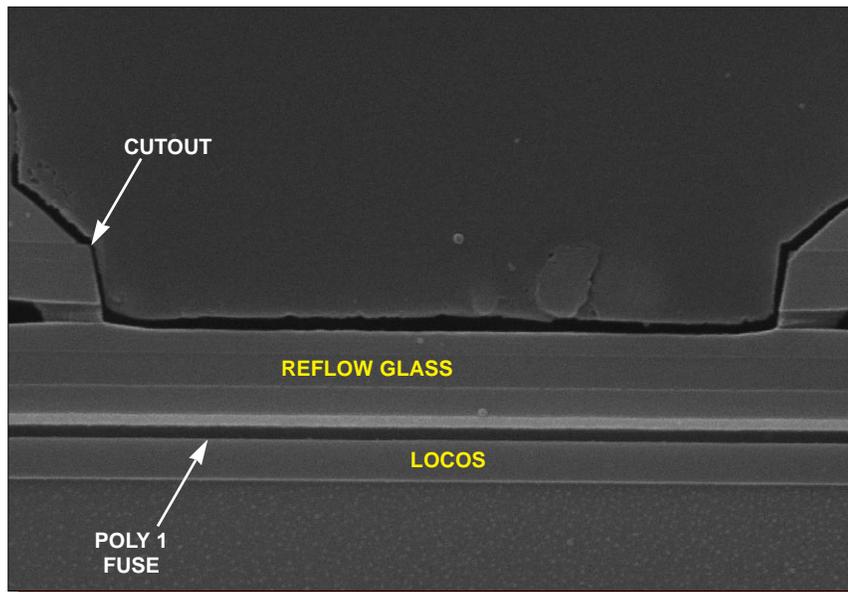
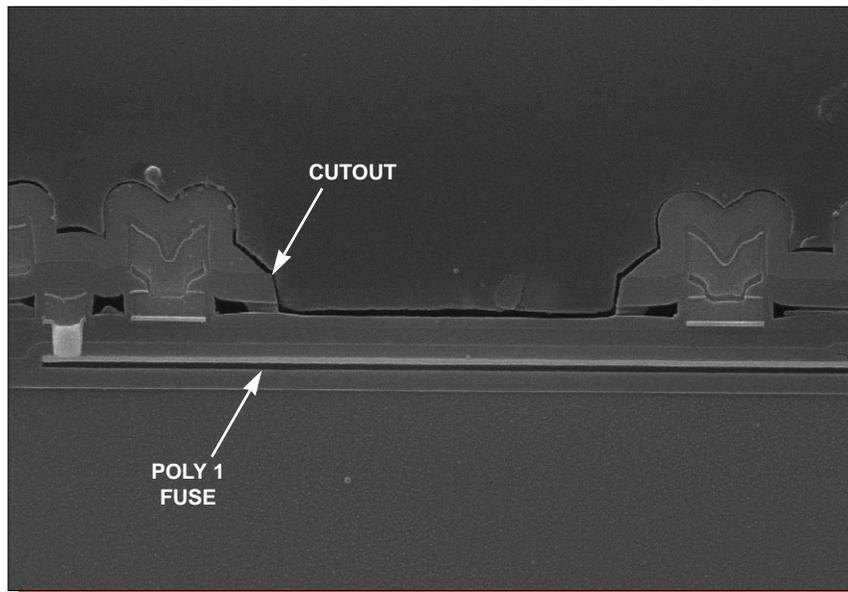
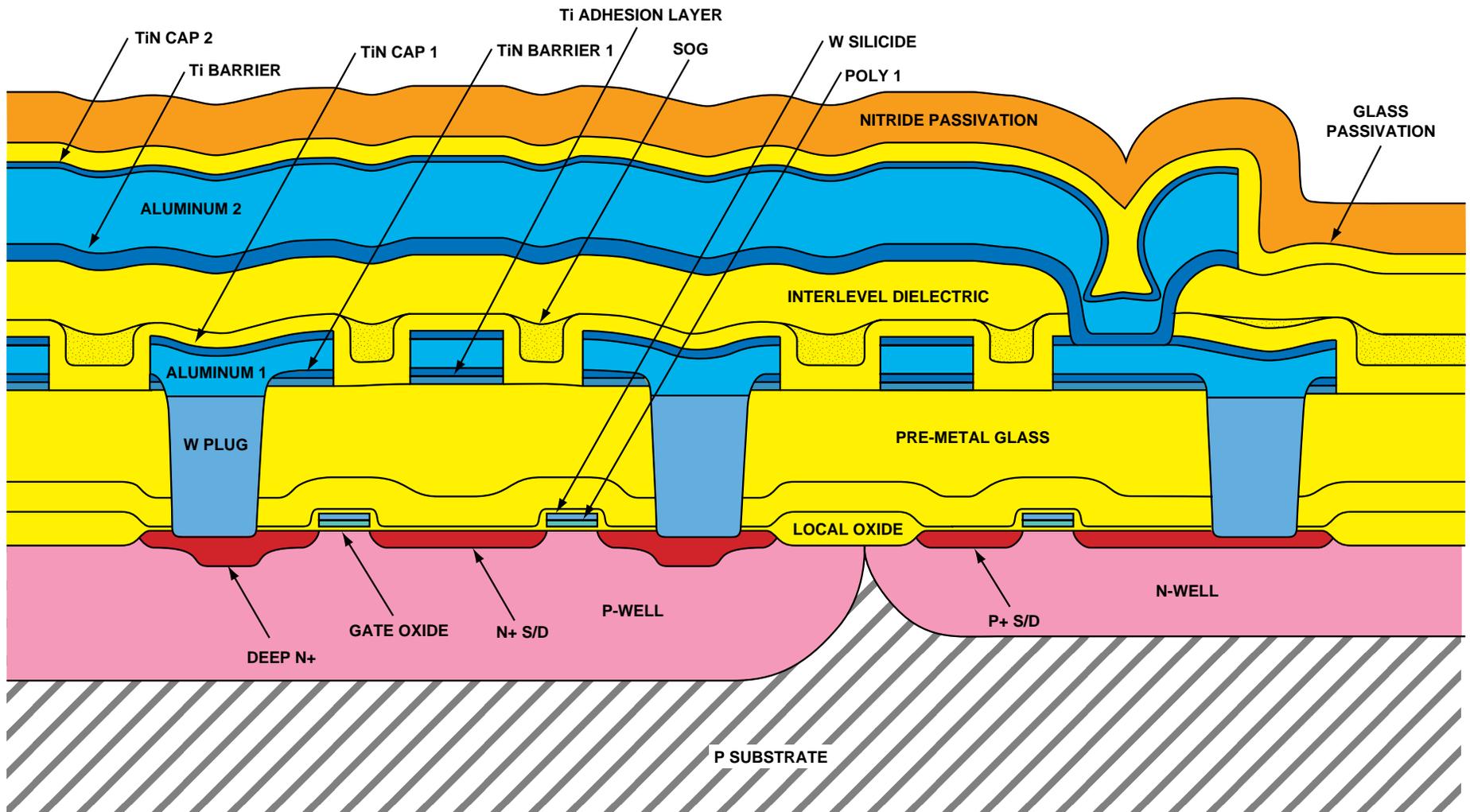
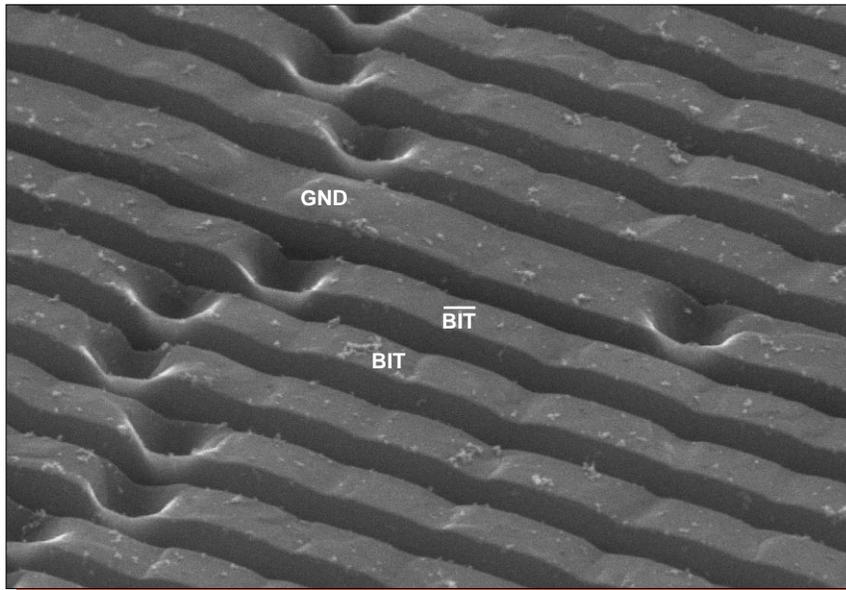


Figure 30. SEM section views of a poly 1 fuse.

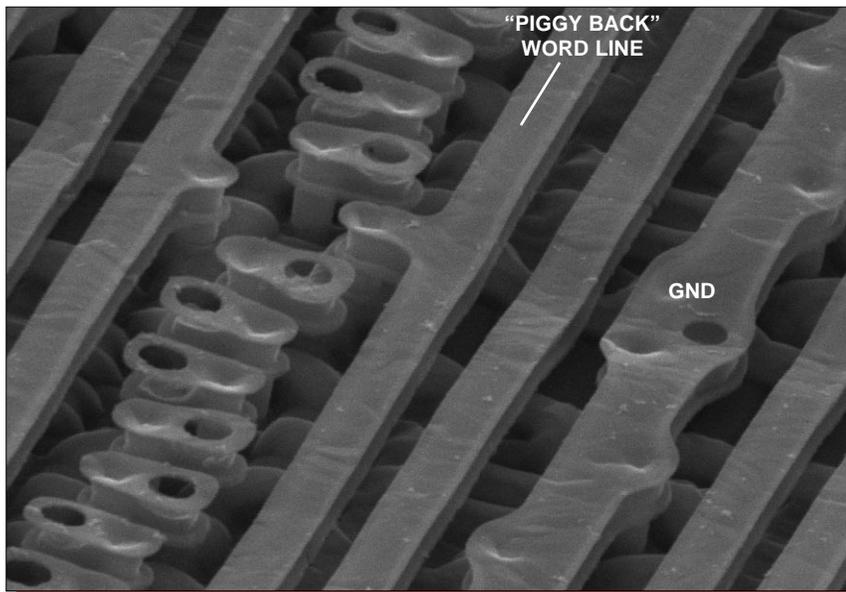


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

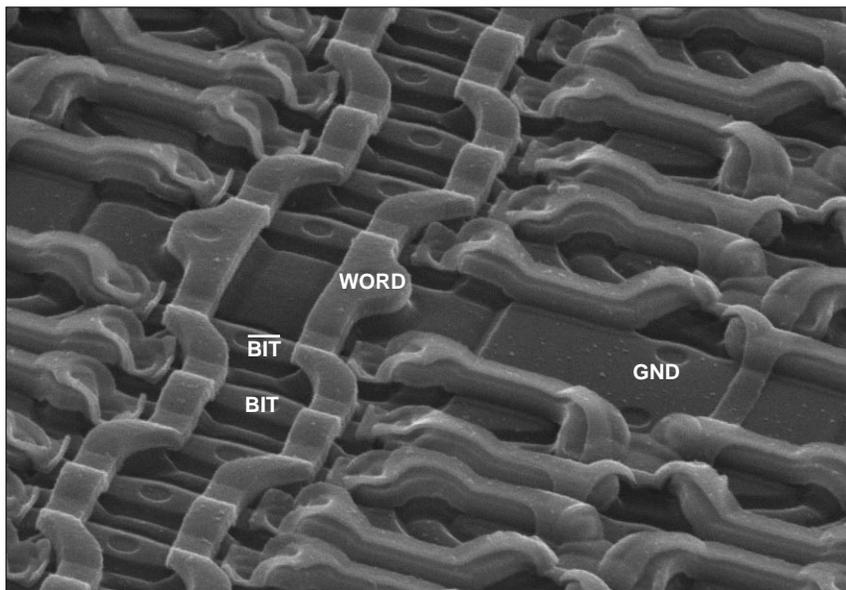
Figure 31. Color cross section drawing illustrating device structure.



metal 2



metal 1



unlayered

Figure 32. Perspective SEM views of the SRAM cell array. Mag. 10,000x, 60°.

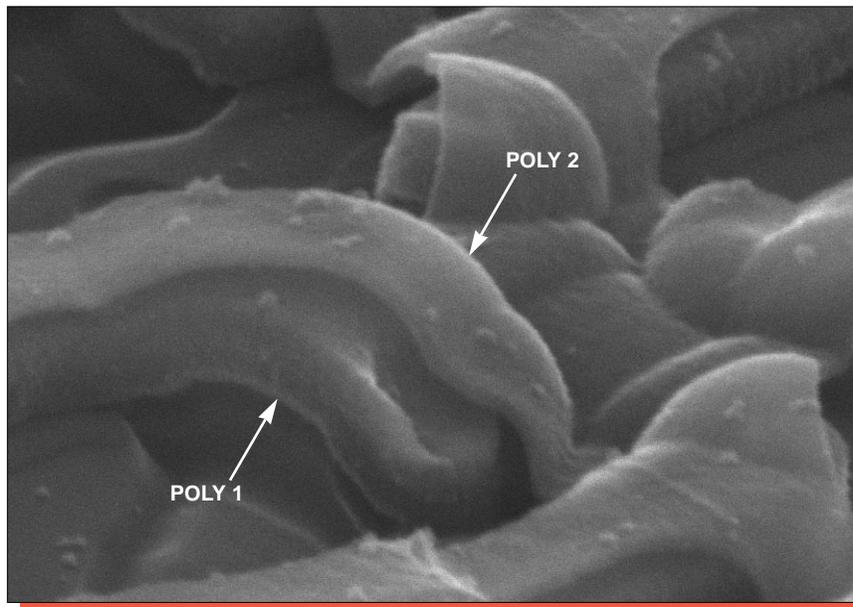
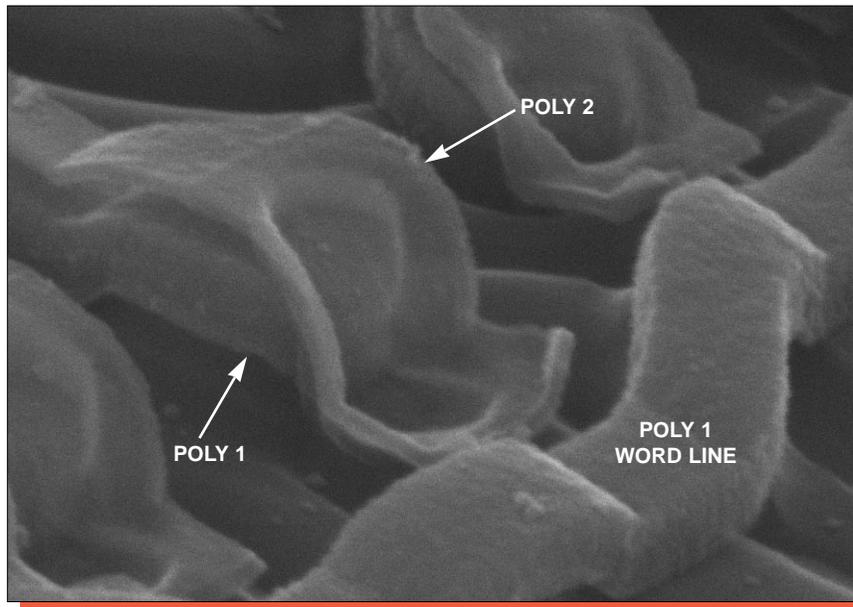


Figure 33. Detailed SEM views of the SRAM cell structures (unlayered).
Mag. 42,000x, 60°.

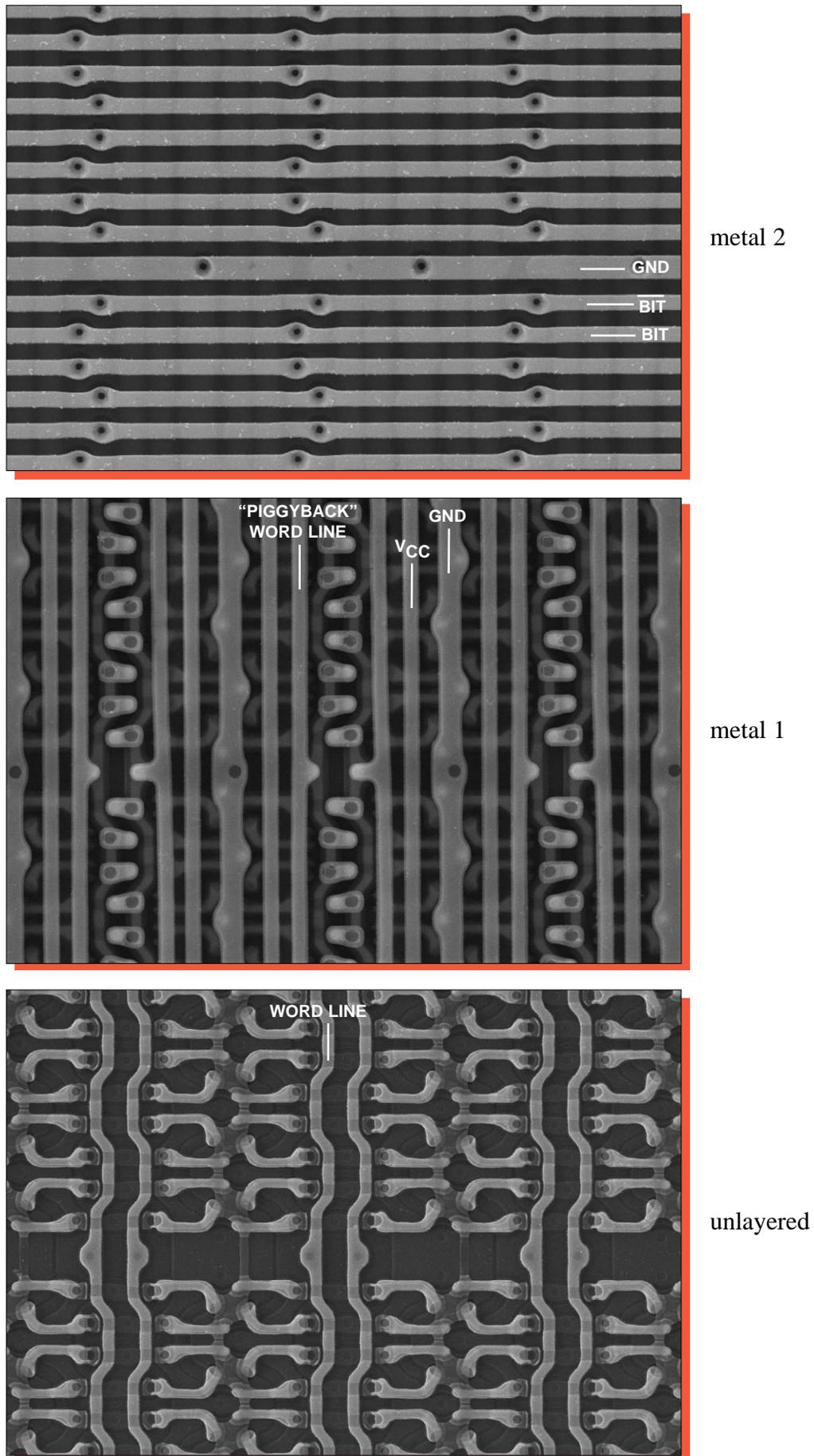
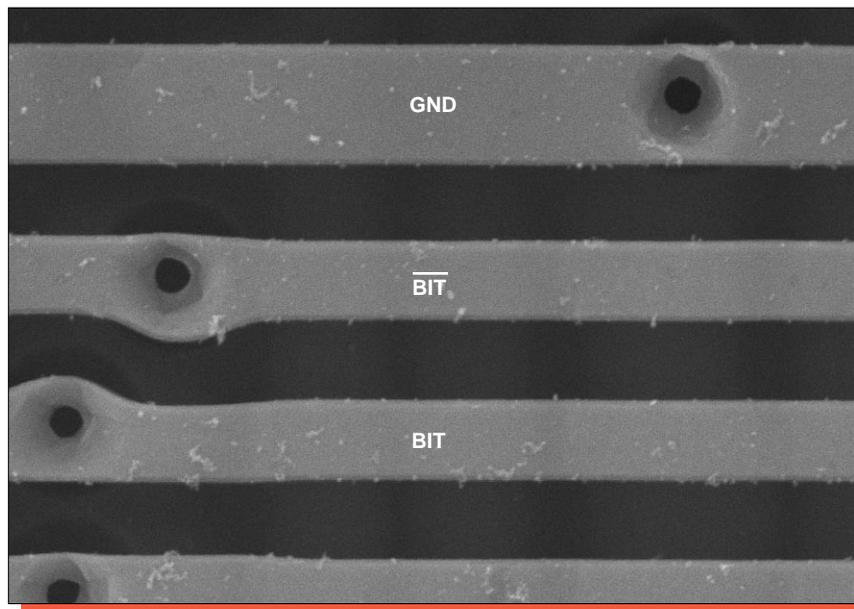
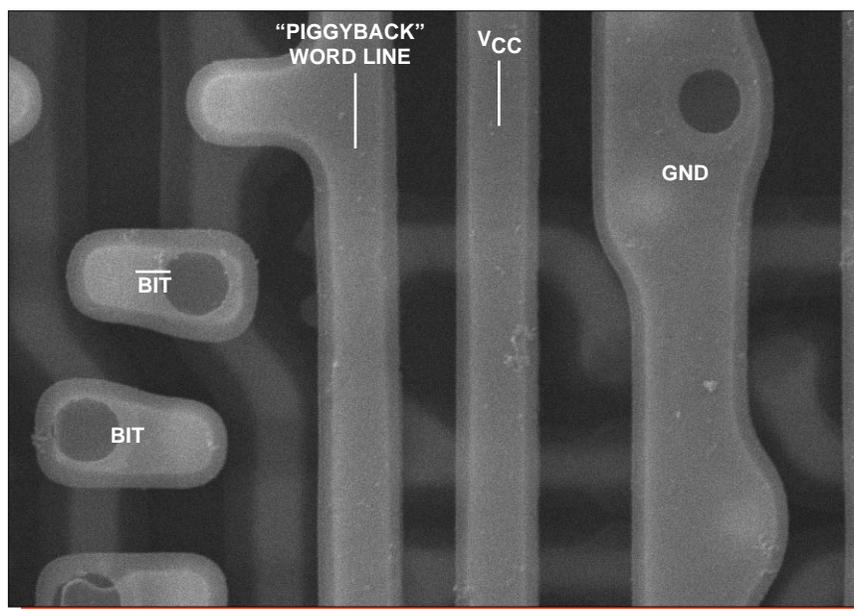


Figure 34. Topological SEM views of the SRAM cell array. Mag. 3200x, 0°.

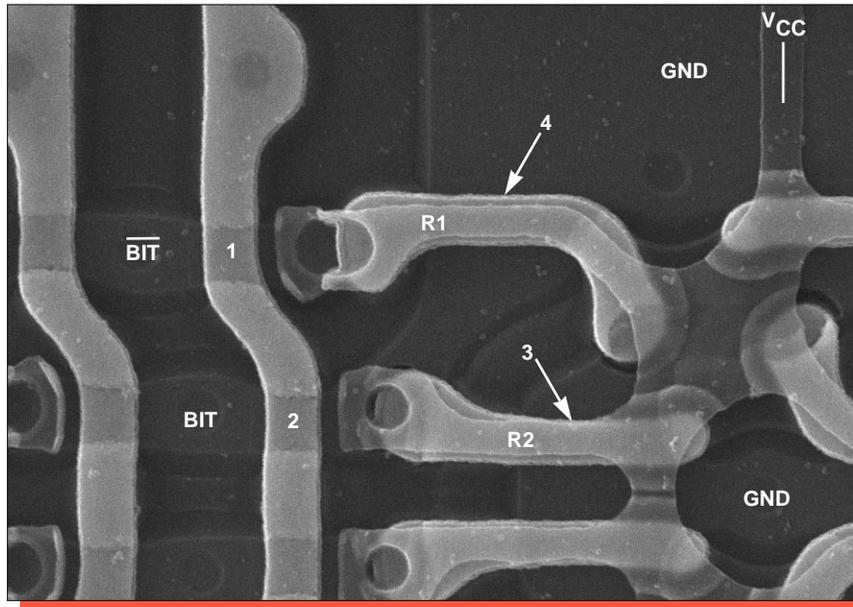


metal 2



metal 1

Figure 35. Detailed topological SEM views of an SRAM cell. Mag. 13,000x, 0°.



unlayered

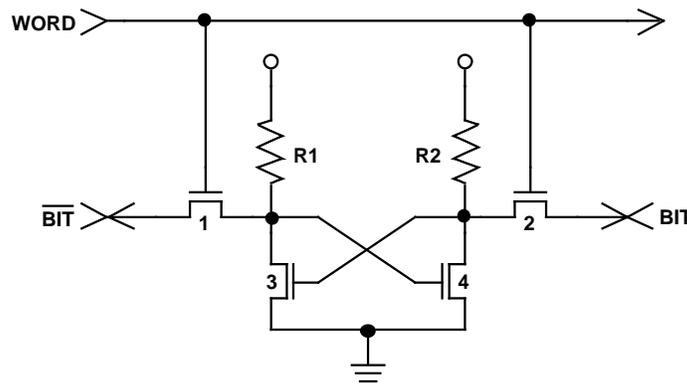
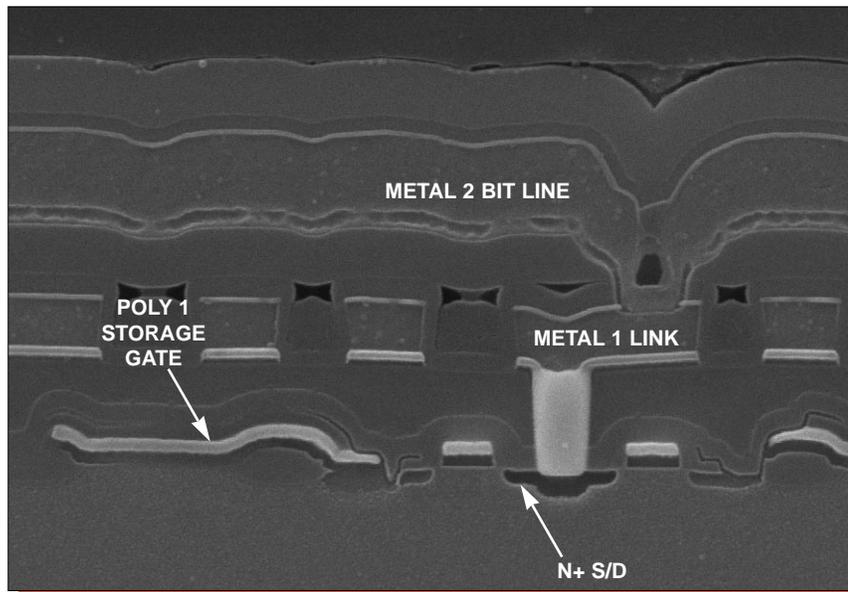
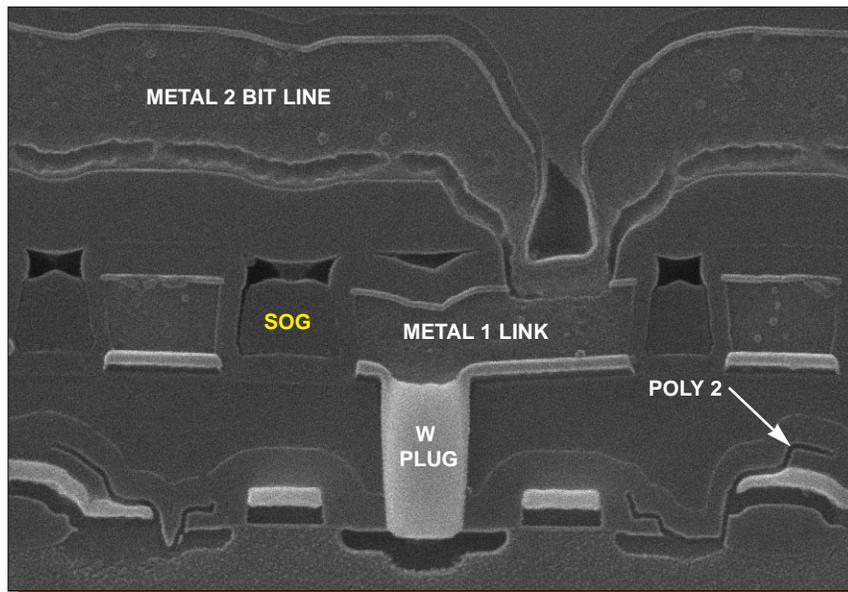


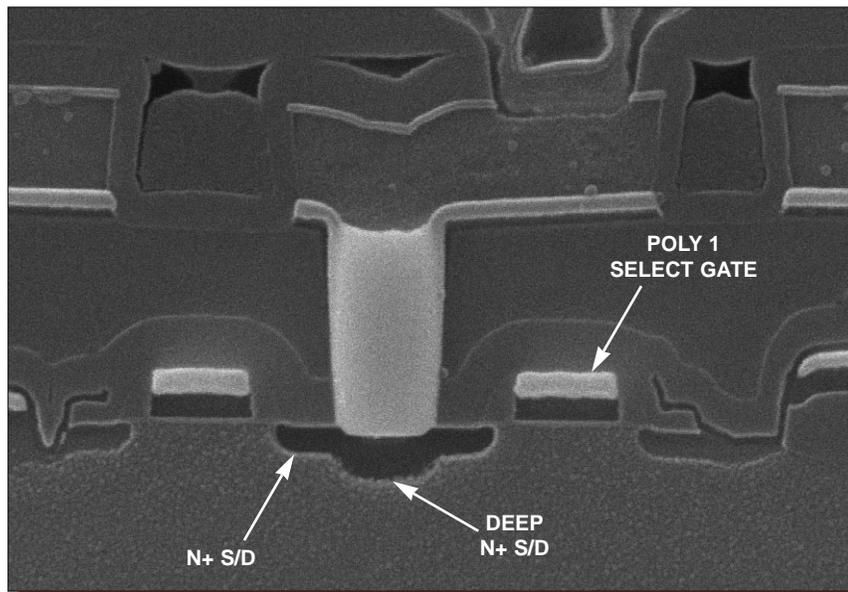
Figure 36. Detailed topological SEM view and schematic of an SRAM cell.
Mag. 13,000x, 0°.



Mag. 13,000x

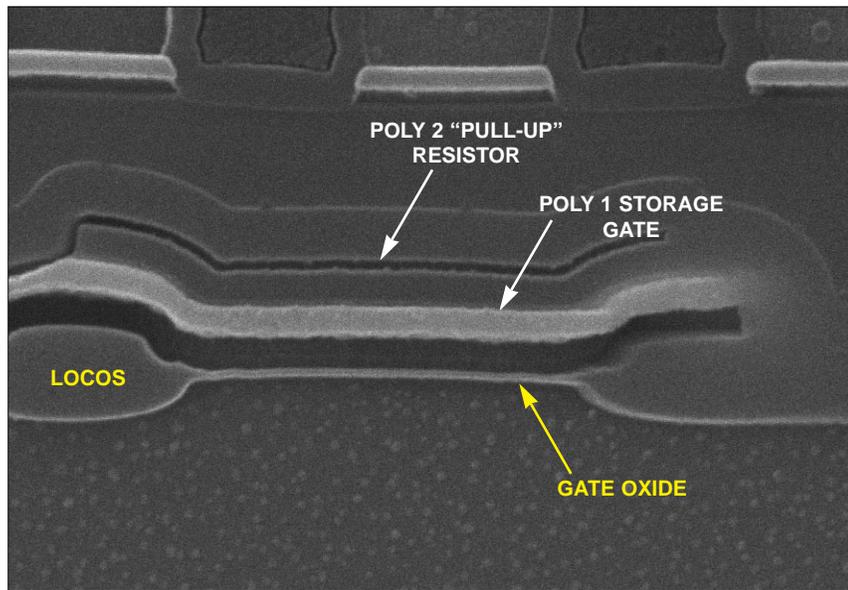


Mag. 20,000x

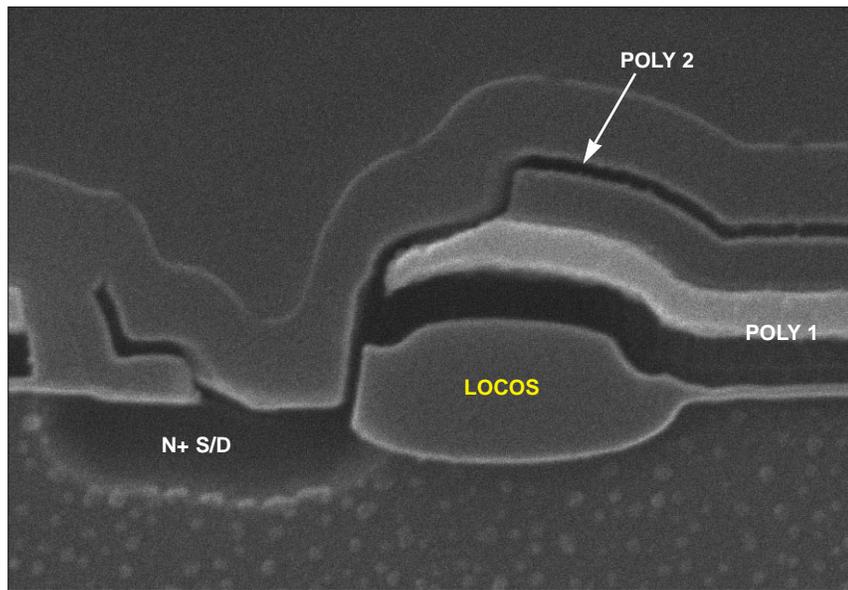


Mag. 26,000x

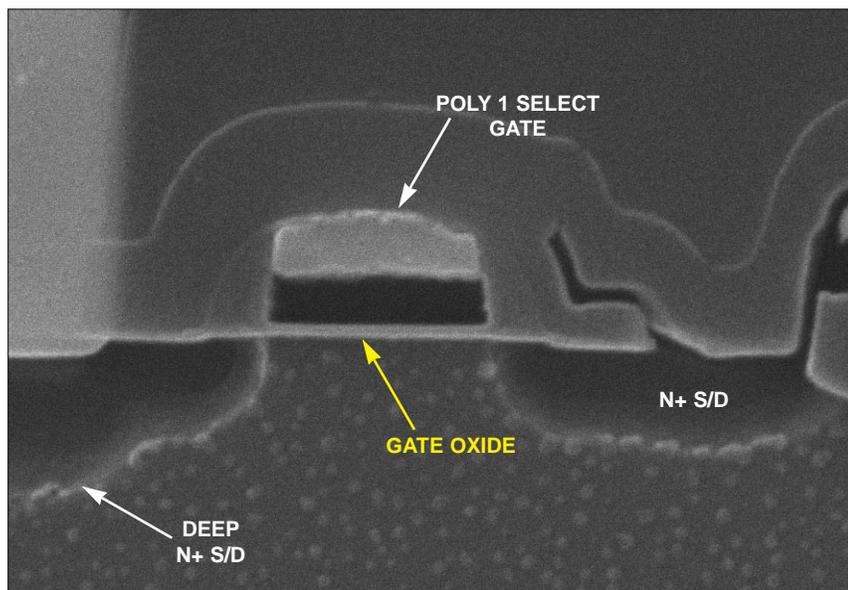
Figure 37. SEM section views of an SRAM cell (parallel to bit line).



Mag. 35,000x

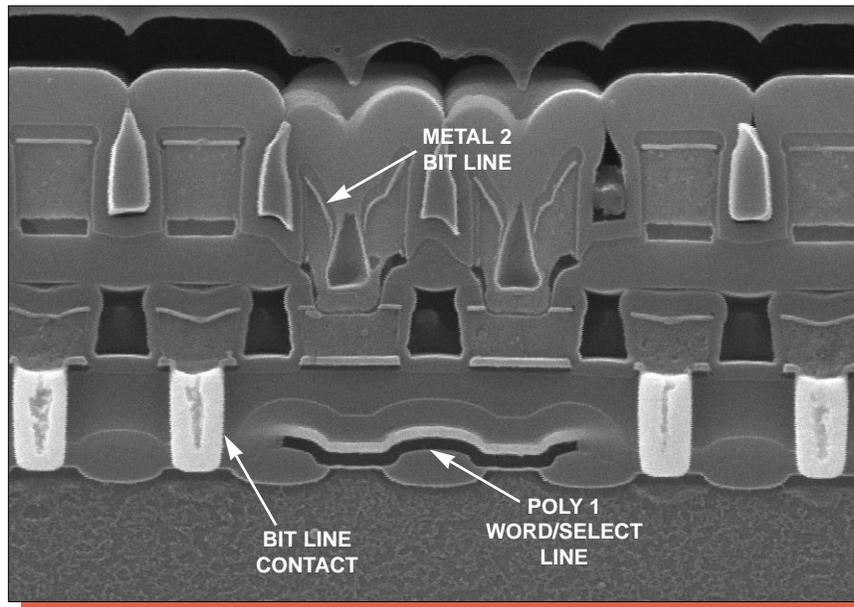


Mag. 52,000x

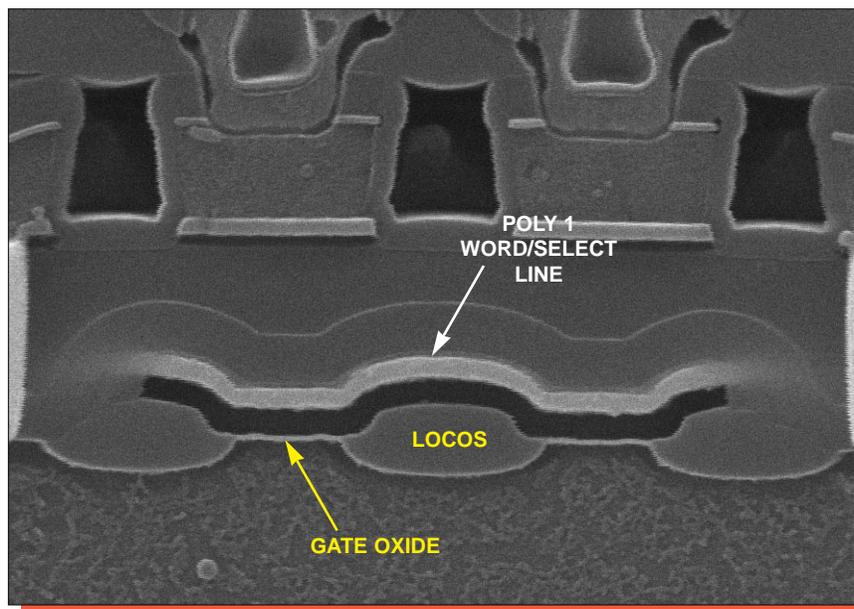


Mag. 52,000x

Figure 38. SEM section views of SRAM cell details (parallel to bit line).

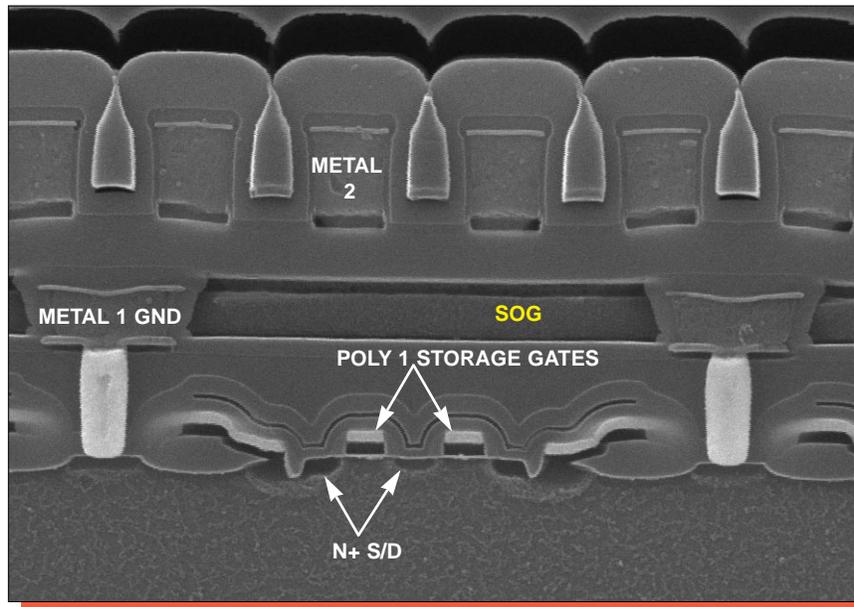


Mag. 13,000x

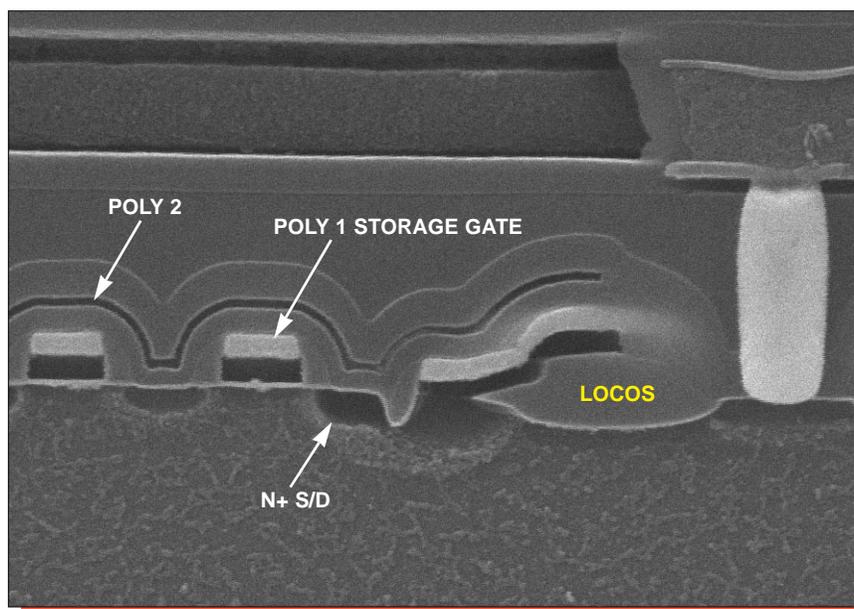


Mag. 26,000x

Figure 39. SEM section views of the SRAM cell array (perpendicular to bit lines).

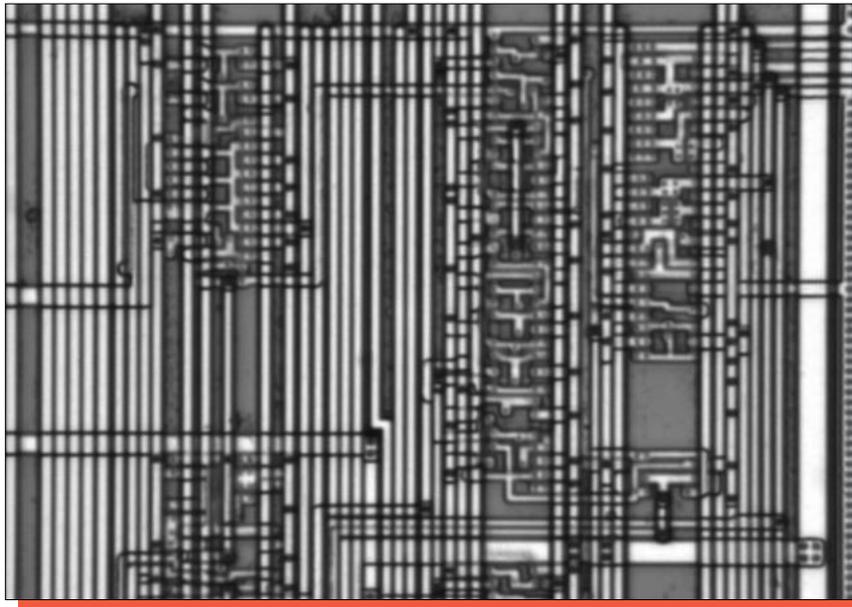


Mag. 13,000x

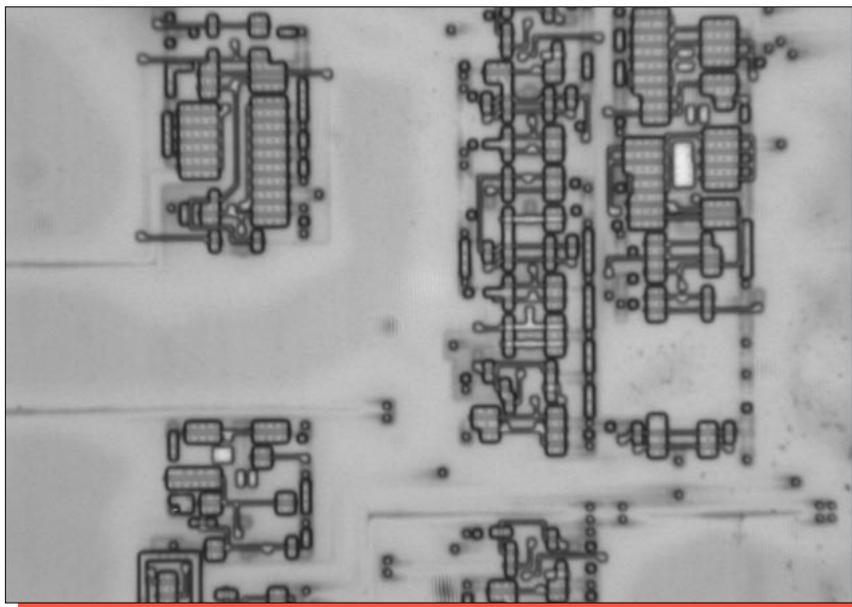


Mag. 26,000x

Figure 40. SEM section views of the SRAM cell array (perpendicular to bit lines).

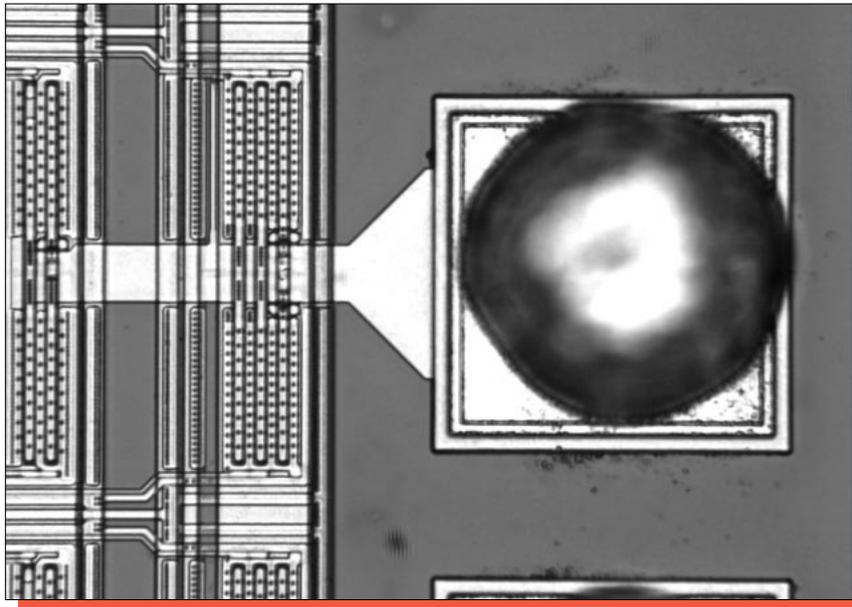


intact

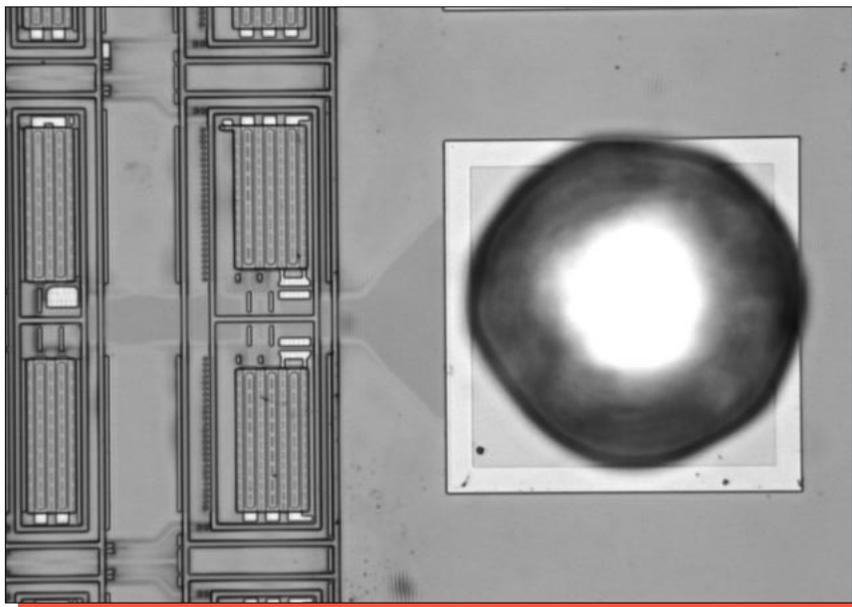


unlayered

Figure 41. Optical views of typical device circuit layout. Mag. 820x.

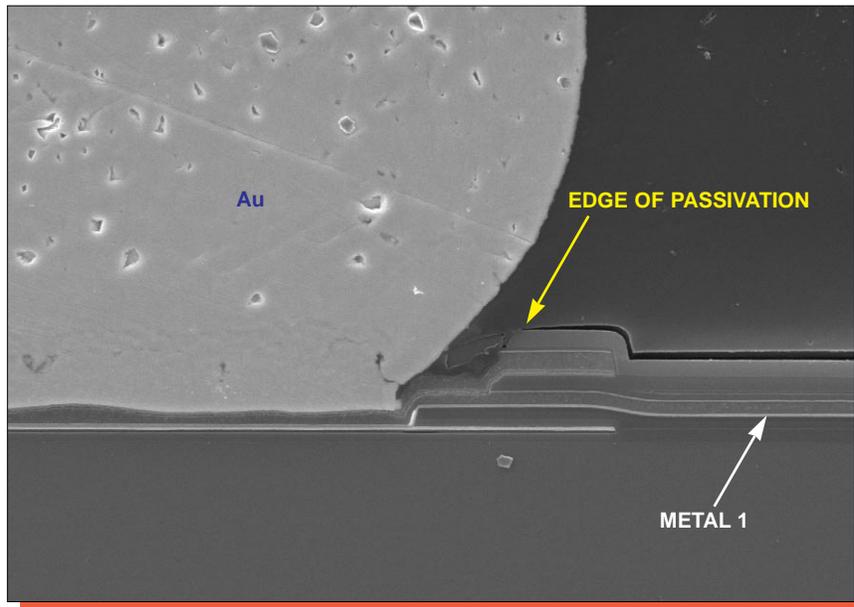


intact

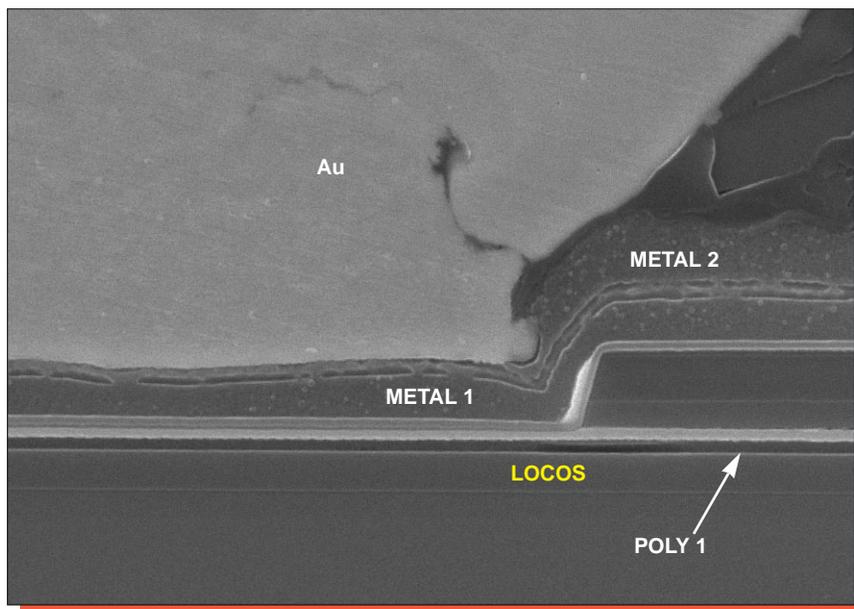


unlayered

Figure 42. Optical views of typical I/O circuitry. Mag. 400x.

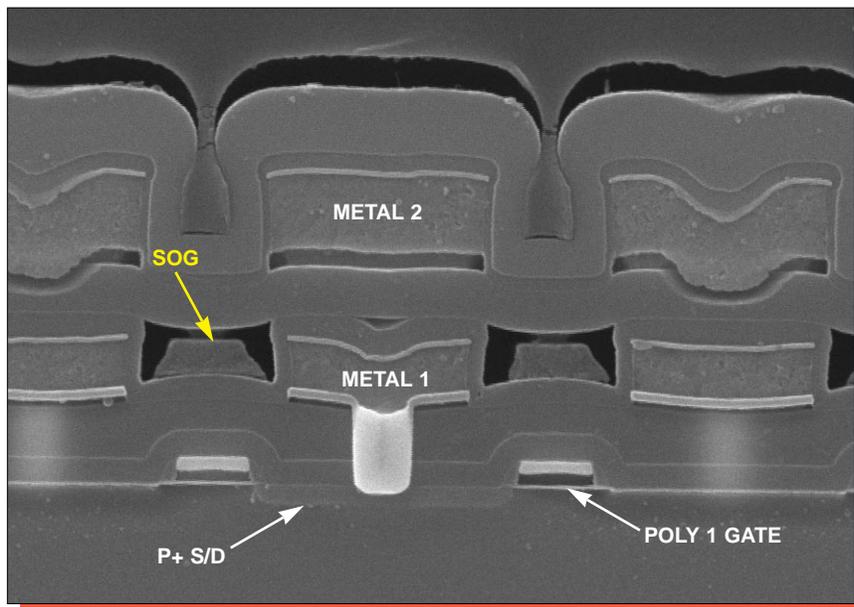


Mag. 3200x

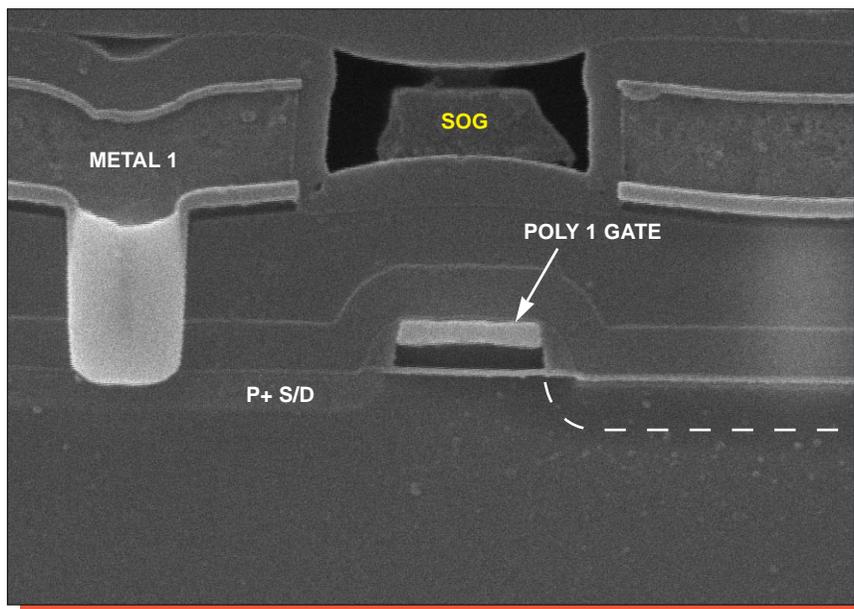


Mag. 13,000x

Figure 43. SEM section views illustrating wirebond interface.

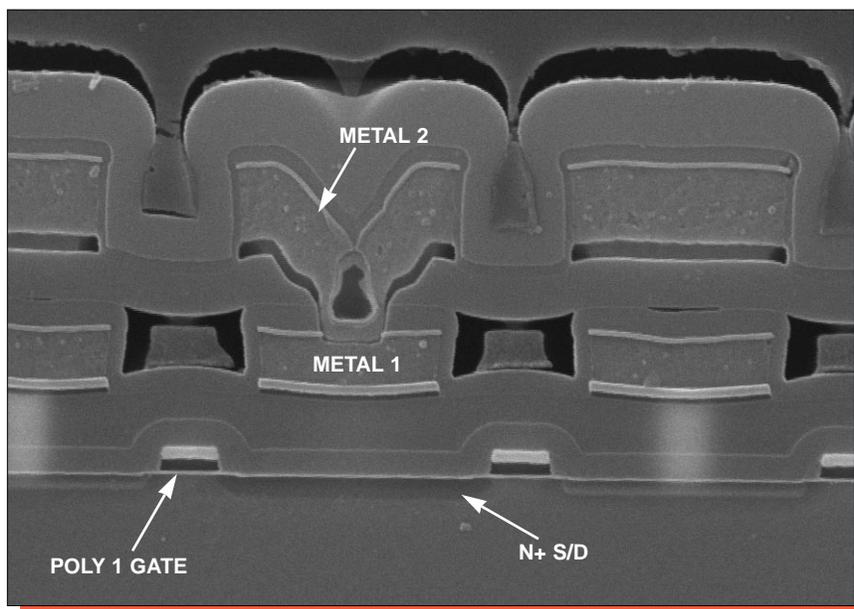


Mag. 13,000x

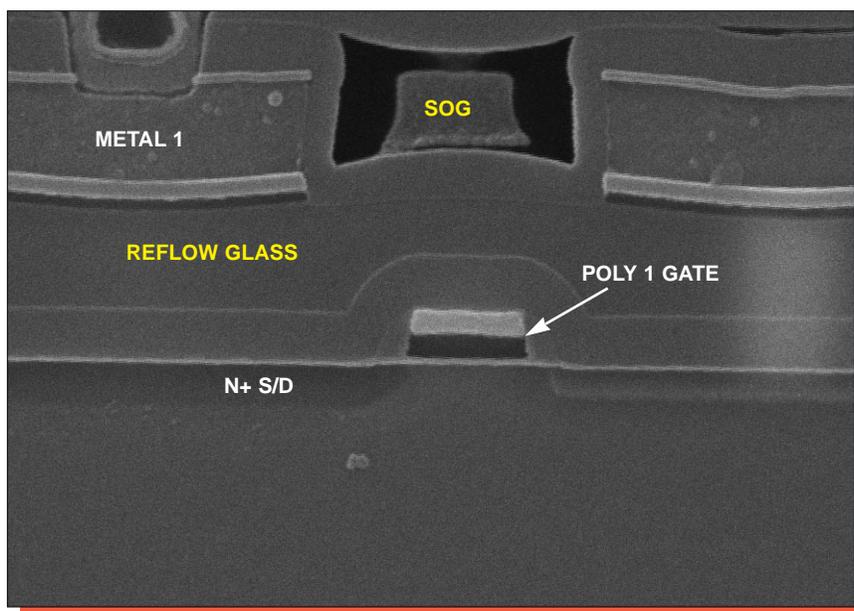


Mag. 26,000x

Figure 44. SEM section views of P-channel I/O circuitry.

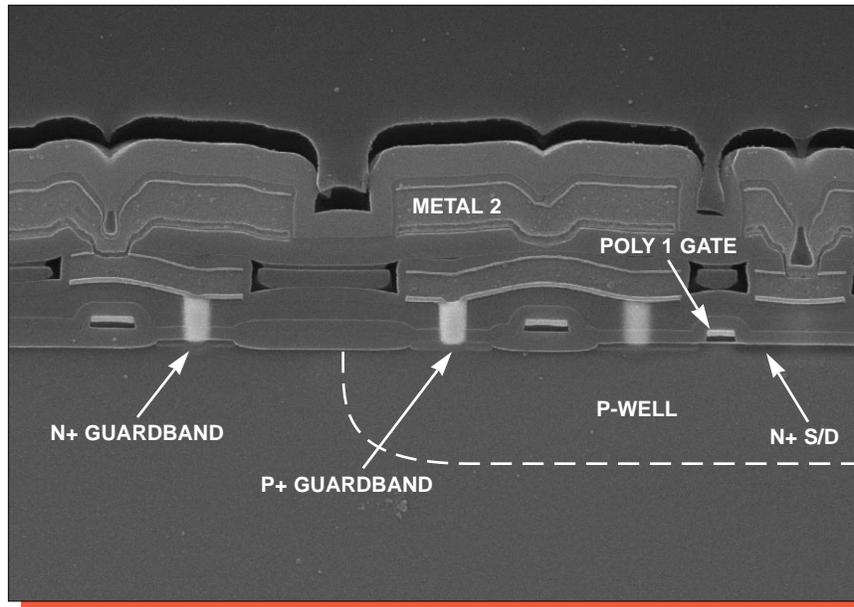


Mag. 13,000x

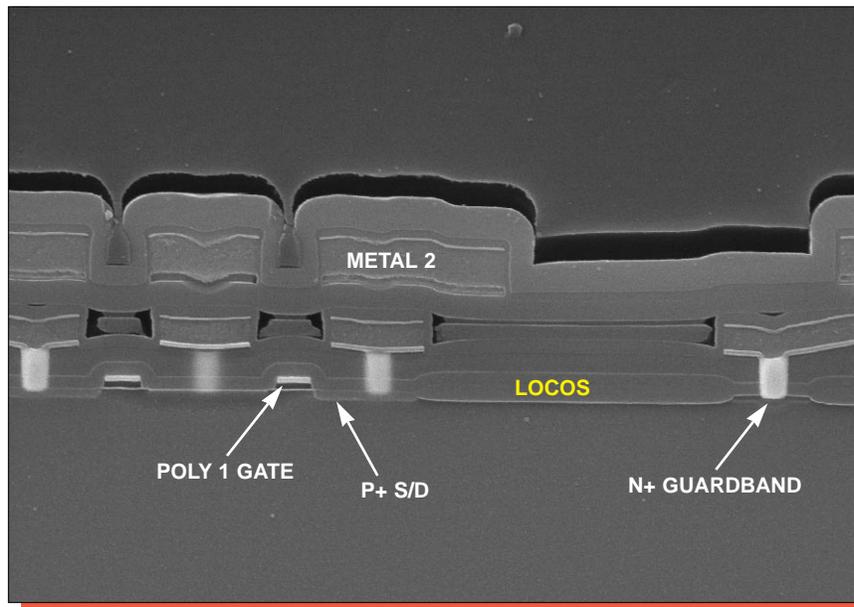


Mag. 26,000x

Figure 45. Additional SEM section views of N-channel I/O circuitry.



N-channel



P-channel

Figure 46. SEM section views illustrating guardbands at the edge of the I/O circuitry. Mag. 6500x.