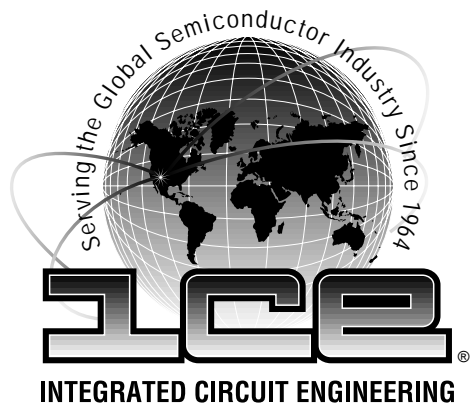


Construction Analysis

Hitachi HM5293206FP10 8Mbit SGRAM

Report Number: SCA 9702-529



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INDEX TO TEXT

<u>TITLE</u>	<u>PAGE</u>
INTRODUCTION	1
MAJOR FINDINGS	1
TECHNOLOGY DESCRIPTION	
Die Process and Design	2 - 3
ANALYSIS RESULTS	
Die Process and Design	4 - 6
ANALYSIS PROCEDURE	7
TABLES	
Overall Evaluation	8
Package Markings	9
Die Material Analysis	9
Horizontal Dimensions	10
Vertical Dimensions	11

INTRODUCTION

This report describes a construction analysis of the Hitachi HM5283206FP10, 8 Meg SGRAM. One device packaged in a 100-pin plastic QFP package was received for the analysis. The package was date coded 9625.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

- Sub-micron gate lengths (0.35 micron, in array).
- Stacked capacitor DRAM cell design.
- Four layers of poly (three layers effective).
- Tungsten metal 1.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-substrate (no epi was used).
- Final passivation: A thick layer of nitride over a layer of glass.
- Metallization: Metal 2 and 3 consisted of aluminum defined by a dry-etch technique. Both metals employed a titanium-nitride cap and barrier. Metal 1 consisted of tungsten with a titanium-nitride barrier. Tungsten plugs were used at Metal 3 and Metal 2 vias. Standard contacts were used in the periphery and poly plugs were used at metal 1 bit contacts in the array. Metal 3 employed beveled corners and multiple contact arrays.
- Intermetal dielectric 1 and 2: Both intermetal dielectrics (IMD 1 and IMD 2) consisted of the same dielectric structure. A layer of glass followed by a spin-on-glass (SOG) and another layer of glass. The SOG layer had been subjected to an etchback.
- Pre-metal dielectric: A single thick layer of reflow glass over a densified oxide.
- Polysilicon: Four layers of polysilicon (three effective) were employed. Poly 3 (sheet) and Poly 2 (which uses two poly depositions) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die. No silicides were used with any of the poly layers.

TECHNOLOGY DESCRIPTION (continued)

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Combination nitride/oxide sidewall spacers were used for the LDD process. Nitride sidewalls were partially removed.
- Wells: Twin-wells in a P-substrate (no epi). A step in the local oxide was noted at the edge of the well boundaries. This step indicates a twin-well process was employed although, the P-well could not be delineated.
- Fuses: All Poly 1 redundancy fuses had passivation and oxide cutouts over them. No blown fuses were present. Guardband diffusions were present around the fuse blocks.
- Memory cells: Stacked capacitor DRAM design. Metal 2 formed “piggyback” word lines and metal 1 distributed the bit lines. Metal 3 was not used directly with the cells. Three layers of polysilicon were employed. Poly 3 (sheet) was used to form the common plate of the capacitors and was tied to memory enable. Poly 2 formed the individual plate of the capacitors. As mentioned, Poly 2 is made using two separate depositions (one for each “wing” of the cell plate); but we refer to all of it as Poly 2 for convenience. Poly 1 provided word lines/select gates.

ANALYSIS RESULTS

Die Process and Design:

Figures 1 - 46b

Questionable Items:¹ None.

Special Features:

- Sub-micron gate lengths (0.35 micron, in array).
- Stacked capacitor DRAM cell design.
- Four layers of poly (counted as three).
- Tungsten metal 1.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-substrate (no epi was used). No significant problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A thick layer of nitride over a layer of glass. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS (continued)

- Metallization: Metal 2 and 3 consisted of aluminum defined by a dry-etch technique. Both metals employed a titanium cap and barrier. Metal 1 consisted of tungsten with a titanium-nitride barrier. Tungsten plugs were used at Metal 3 and Metal 2 vias. Standard contacts were used in the periphery and poly plugs were used at Metal 1 bit contacts in the array.
- Metal patterning: All three metal layers were defined by a dry-etch of good quality.
- Metal defects: None. No notching or voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.
- Metal step coverage: No significant thinning of Metal 2 or 3 was noted, due to the use of tungsten plugs. Virtually no Metal 1 tungsten thinning was present at contacts in the periphery and no thinning was present in the array due to the use of poly plugs.
- Vias and contacts: Via and contact cuts appeared to be defined by a dry etch. No over-etching or other contact problems were found. Multiple contact arrays were employed.
- Intermetal dielectrics 1 and 2: Both intermetal dielectrics (between M3-M2 and M2-M1) consisted of a layer of glass followed by a spin-on-glass (SOG) for planarization, and another layer of glass. The SOG layer had been subjected to an etchback. No problems were found with these layers.
- Pre-metal dielectric: A single layer of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array.

ANALYSIS RESULTS (continued)

- Polysilicon: Four layers of polysilicon were employed. Poly 3 (sheet) and Poly 2 (two layers) were used exclusively in the cell array and formed the plates of the capacitors. Poly 1 formed all gates and word lines on the die. No silicides were used with any layers. Poly 1 “neckdown” was noted at the gate/local oxide transition. Although this indicates somewhat poor definition control no problems are anticipated.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries. This indicates a twin-well process was employed.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. Combination oxide/nitride sidewall spacers were used for the LDD process. Nitride sidewalls were partially removed. No problems were found in any of these areas.
- Wells: Twin-wells were used in a P substrate (no epi was present). The P-well could not be delineated. No problems were found.
- Fuses: All Poly 1 redundancy fuses had passivation and oxide cutouts over them. No blown fuses were present. Guardband diffusions were present around the fuse blocks.
- Memory cells: Stacked capacitor DRAM design. Metal 2 formed “piggyback” word lines and Metal 1 distributed the bit lines. Three layers of polysilicon were employed. Poly 3 was used to form the common plate of the capacitors (sheet) and was tied to memory enable. Poly 2 formed the dual individual plates of the capacitors. As mentioned, Poly 2 consisted of two separate layers connected together. Poly 1 formed all gates and word lines. Definition was good and no problems were noted. Cell pitch was 1.1 x 1.9 micron (2.1 microns²).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM inspection of passivation

Passivation integrity test

Delayer to metal 3 and inspect

Aluminum removal (metal 3)

Delayer to metal 2 and inspect

Aluminum removal (metal 2)

Delayer to metal 1 and inspect

Delayer to poly/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	NP*
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	G
Contact coverage	G
Contact registration	G

**Neckdown of poly I gates.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

(logo) HM5283206FP10

JAPAN 9625

0003933

BOTTOM (Molded)

32 DC

DIE MATERIAL ANALYSIS

Overlay passivation:	A thick layer of nitride over a layer of glass.
Metallization 2 and 3:	Aluminum with a titanium-nitride cap and barrier.
Intermetal dielectrics (IMD1 and IMD2):	Two layers of silicon-dioxide with a filler glass (SOG) between.
Metallization 1:	Tungsten with a titanium-nitride (TiN) barrier.
Pre-metal glass:	A single layer of reflow glass over a densified oxide.

HORIZONTAL DIMENSIONS

Die size:	7.5 x 7.8 mm (295 x 308 mils)
Die area:	58 mm ² (90,860 mils ²)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.1 x 0.1 mm (4.1 x 4.1 mils)
Min pad space:	0.05 mm (2 mils)
Min metal 3 width:	1.0 micron
Min metal 3 space:	1.0 micron
Min metal 3 pitch:	2.0 microns
Min via 2:	0.6 micron
Min metal 2 width:	0.6 micron
Min metal 2 space:	0.6 micron
Min metal 2 pitch:	1.2 micron
Min via 1:	0.6 micron
Min metal 1 width:	0.3 micron
Min metal 1 space:	0.6 micron
Min metal 1 pitch:	0.9 micron
Min contact:	0.5 micron
Min poly 2 width:	0.6 micron
Min poly 2 space:	0.5 micron
Min poly 1 width - (cell):	0.35 micron
Min poly 1 space:	0.45 micron
Min gate length* - (N-channel):	0.35 micron (in cell)
- (N-channel):	0.5 micron (in periphery)
- (P-channel):	0.5 micron
Cell area:	2.1 microns ²
Cell size:	1.1 x 1.9 micron

**Physical gate length.*

VERTICAL DIMENSIONS

Layers

Passivation 2:	1.2 micron
Passivation 1:	0.2 micron
Metal 3 - cap:	0.07 micron
- aluminum	0.6 micron
- barrier	0.1 micron
- plugs	0.6 micron
Intermetal dielectric 2 - glass 2:	0.35 micron
- SOG:	0 - 0.55 micron
- glass 1:	0.35 micron
Metal 2 - cap:	0.1 micron
- aluminum:	0.35 micron
- barrier:	0.1 micron
- plugs:	0.7 micron
Intermetal dielectric 1 - glass 2:	0.35 micron
- SOG:	0 - 0.4 micron
- glass 1:	0.35 micron
Metal 1 - tungsten	0.2 micron
- barrier:	0.1 micron
Reflow glass:	0.6 micron (average)
Poly 3 (sheet):	0.05 micron (approximate)
Poly 2 - 2nd layer:	0.06 micron (approximate)
- 1st layer:	0.06 micron (approximate)
Poly 1:	0.15 micron
Local oxide:	0.38 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.2 micron
N-well:	5 microns

INDEX TO FIGURES

ASSEMBLY	Figures 1 - 2
EDGE SEAL STRUCTURE	Figure 3
DIE LAYOUT AND IDENTIFICATION	Figures 4 - 6
PHYSICAL DIE STRUCTURES	Figures 7 - 40
COLOR DRAWING OF DIE STRUCTURE	Figure 29
REDUNDANCY FUSES	Figures 30 - 31
MEMORY CELL STRUCTURES	Figures 32 - 40
OPTICAL VIEWS OF CIRCUIT BLOCKS	Figures 41 - 46b

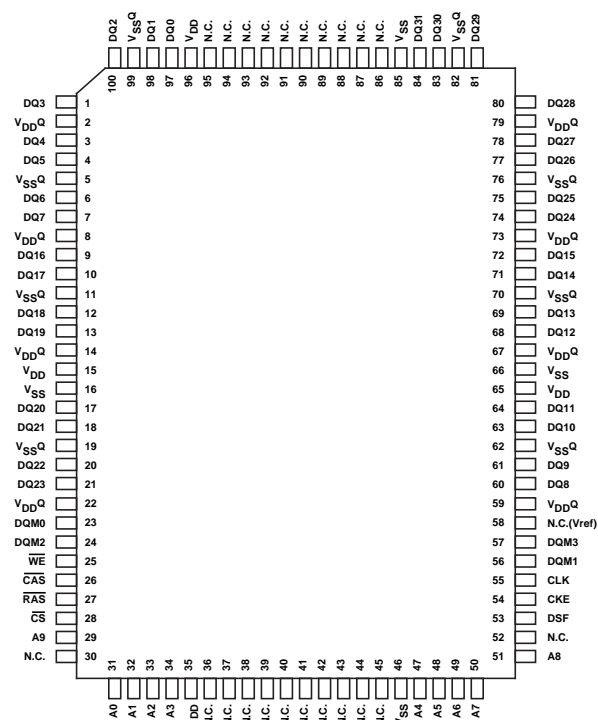
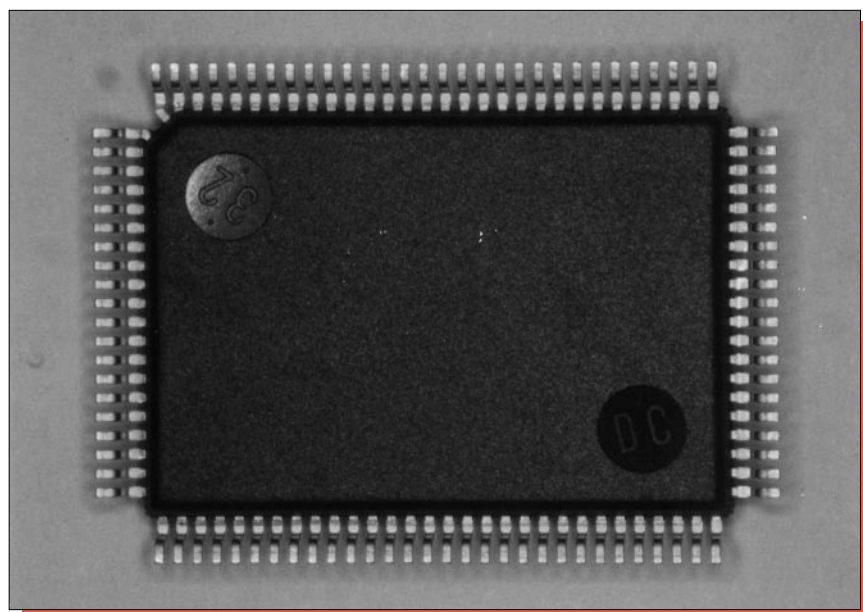
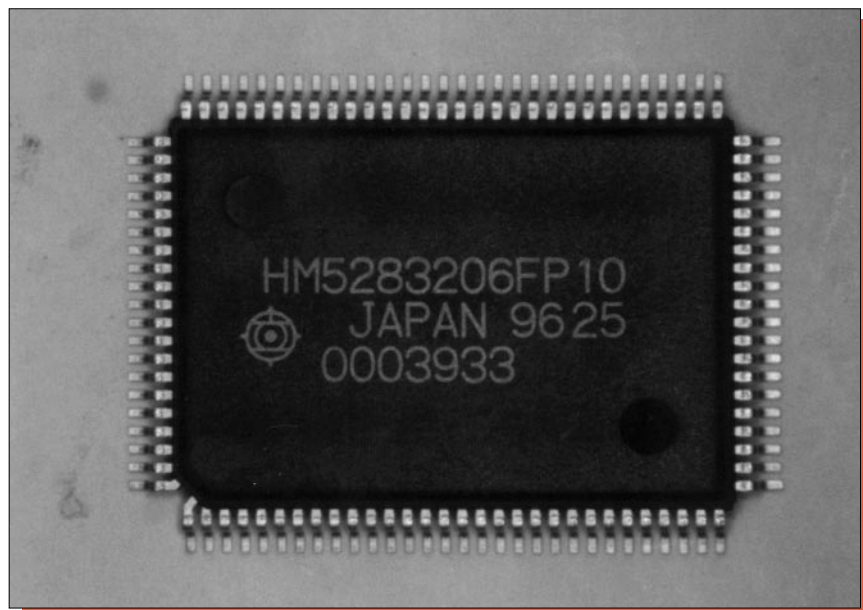
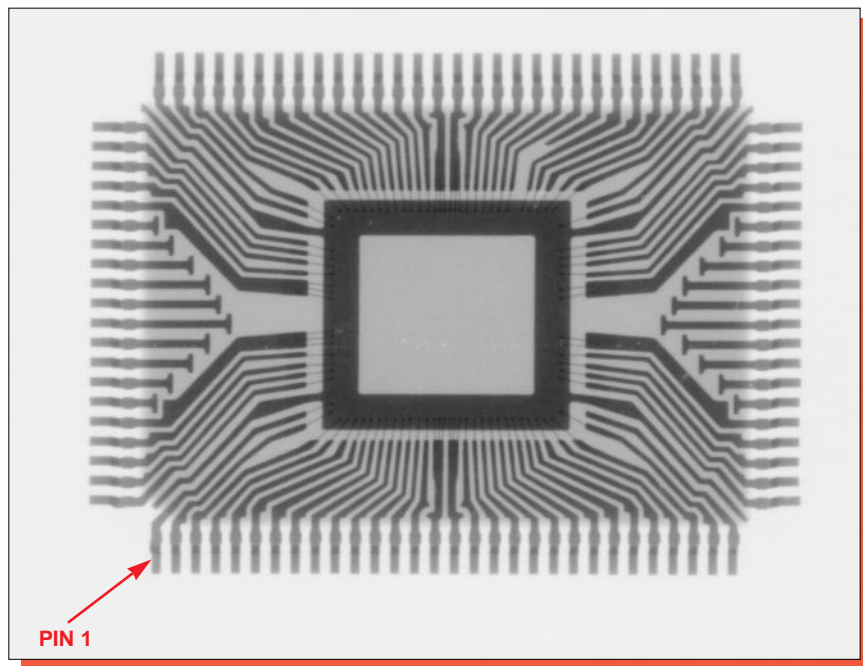
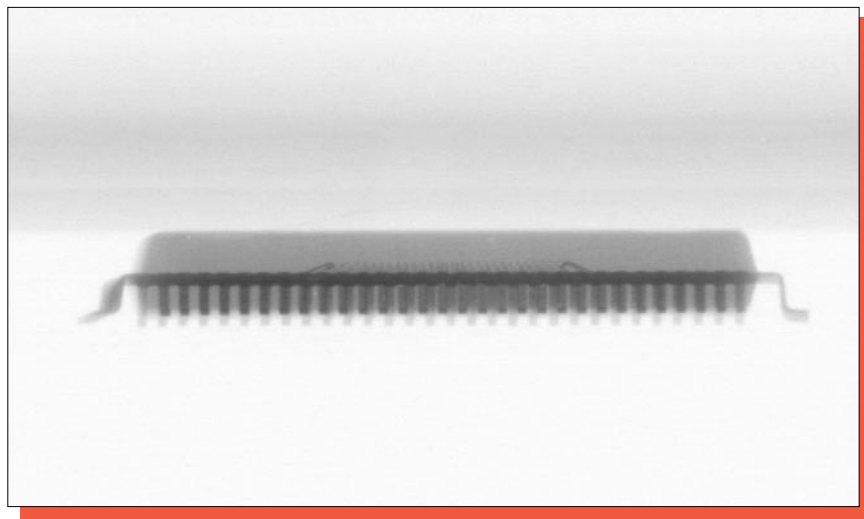


Figure 1. Package photographs and pinout of the Hitachi HM5283206FP10 8M Graphic RAM. Mag. 3.6x.

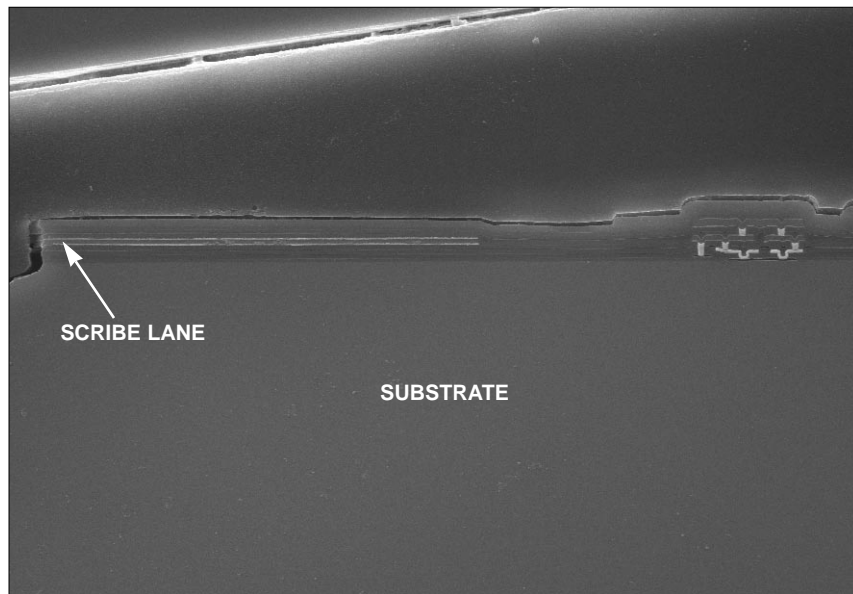


top

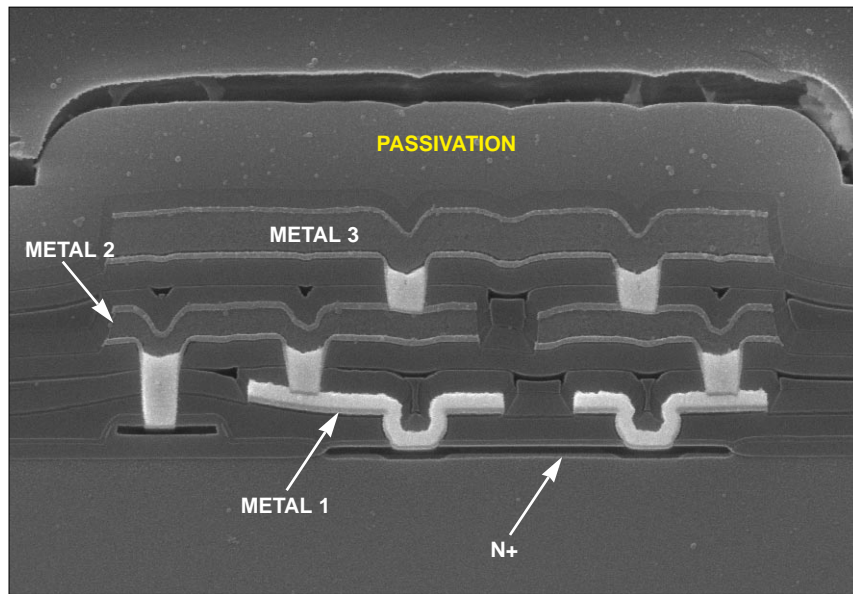


side

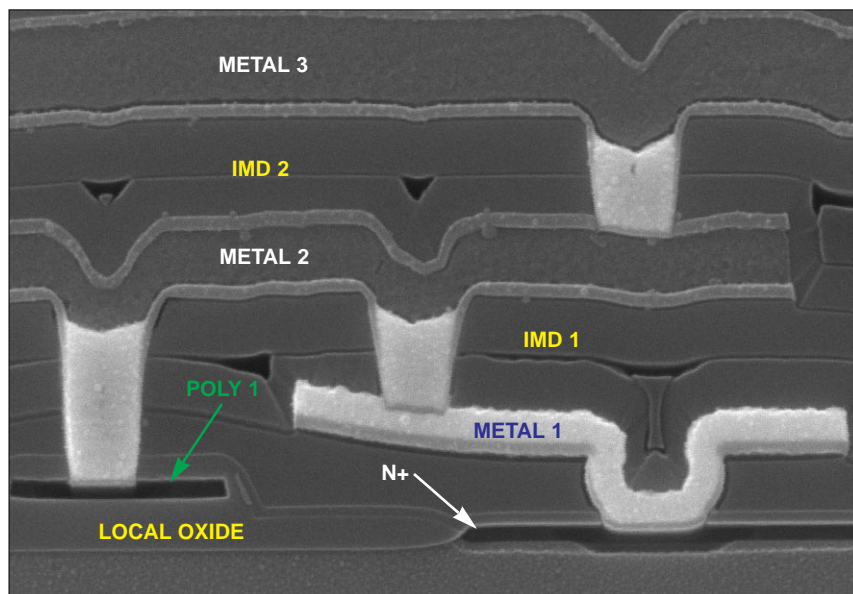
Figure 2. Topological and side x-ray views of the package. Mag. 4x.



Mag. 1500x



Mag. 9000x



Mag. 20,000x

Figure 3. SEM section views of the edge seal structure.

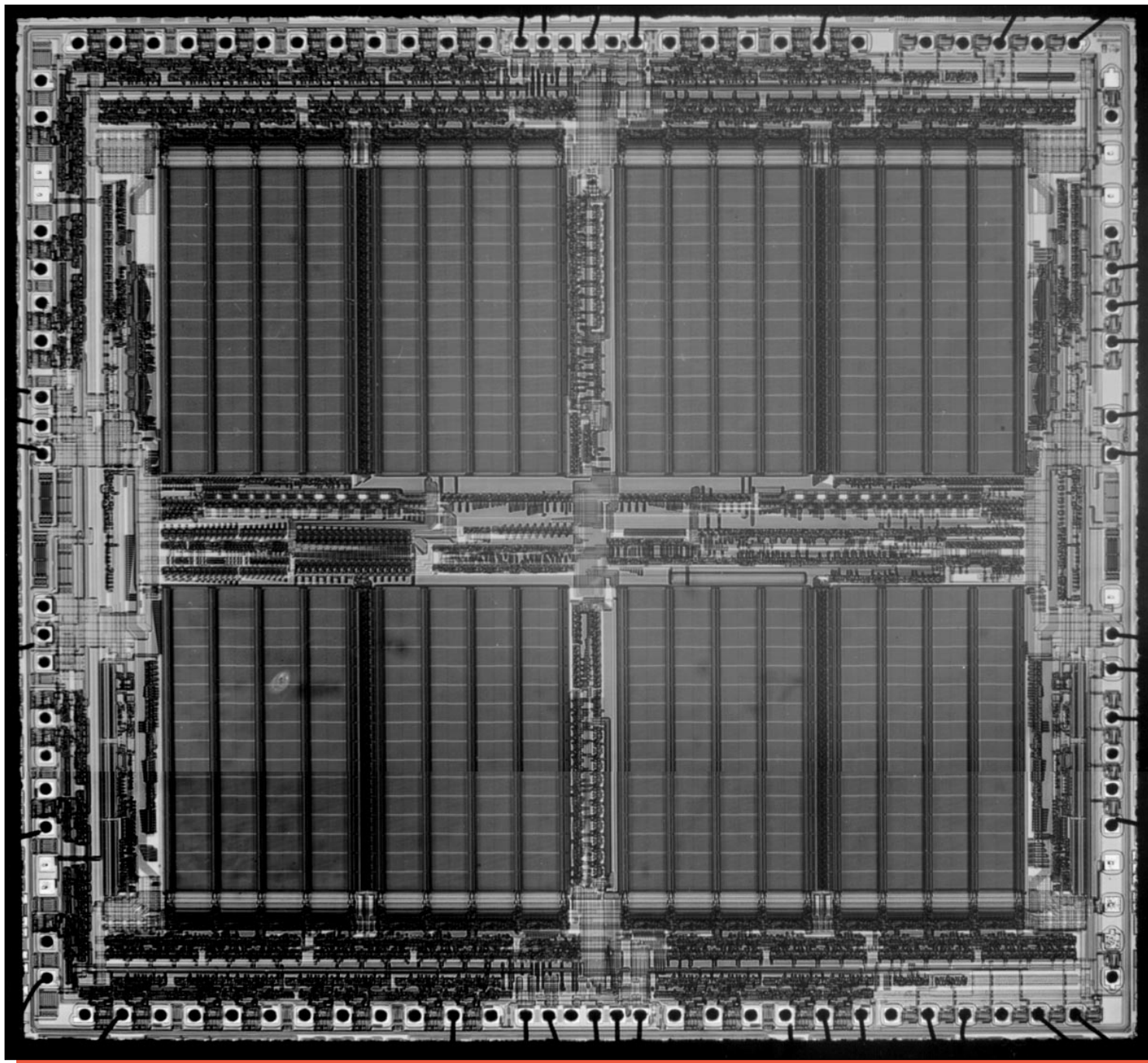


Figure 4. Whole die photograph of the Hitachi HM5283206FP10 8M Graphic RAM. Mag. 26x.



Figure 5. Optical view of the die markings from the surface. Mag. 320x.

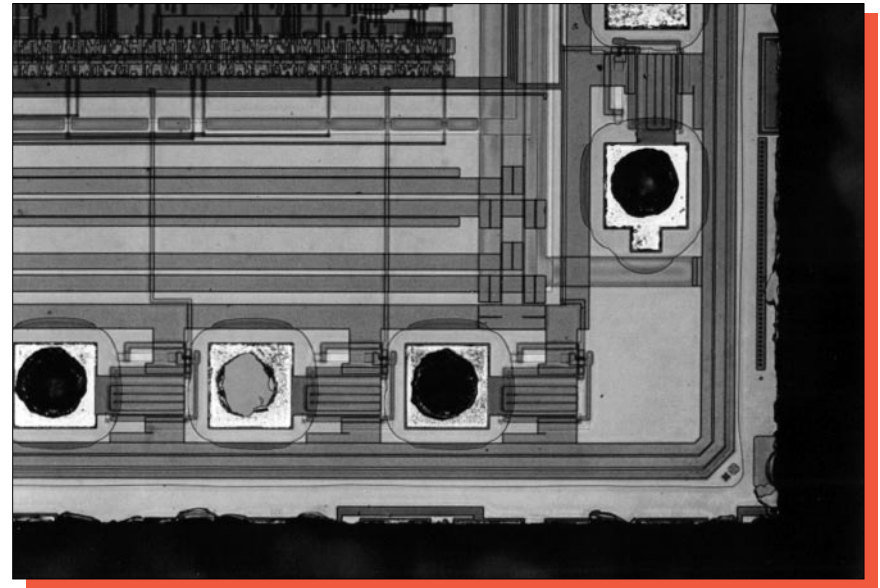
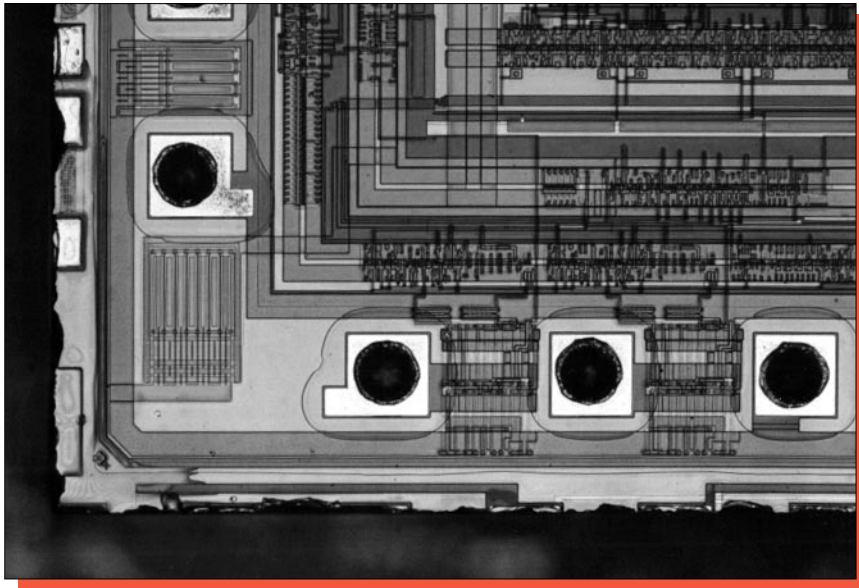
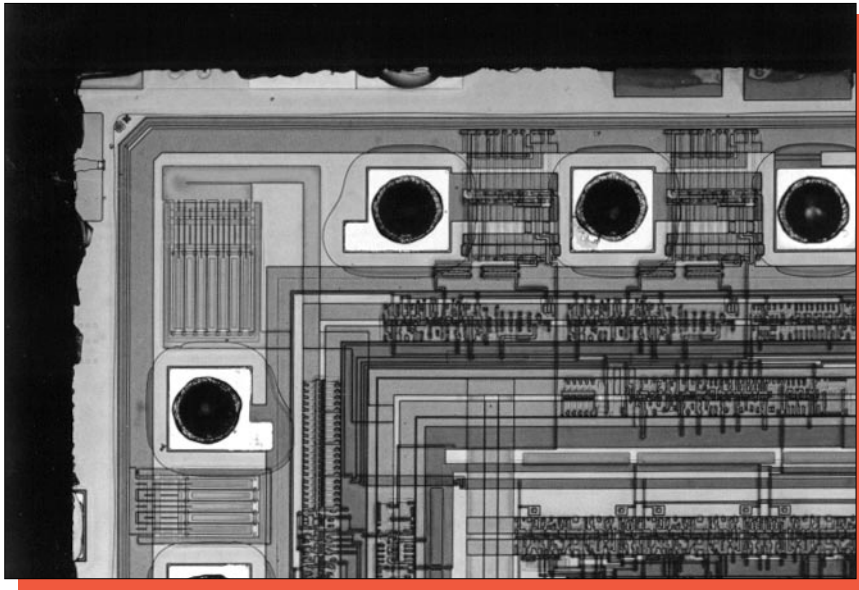


Figure 6. Optical views of the die corners. Mag. 100x

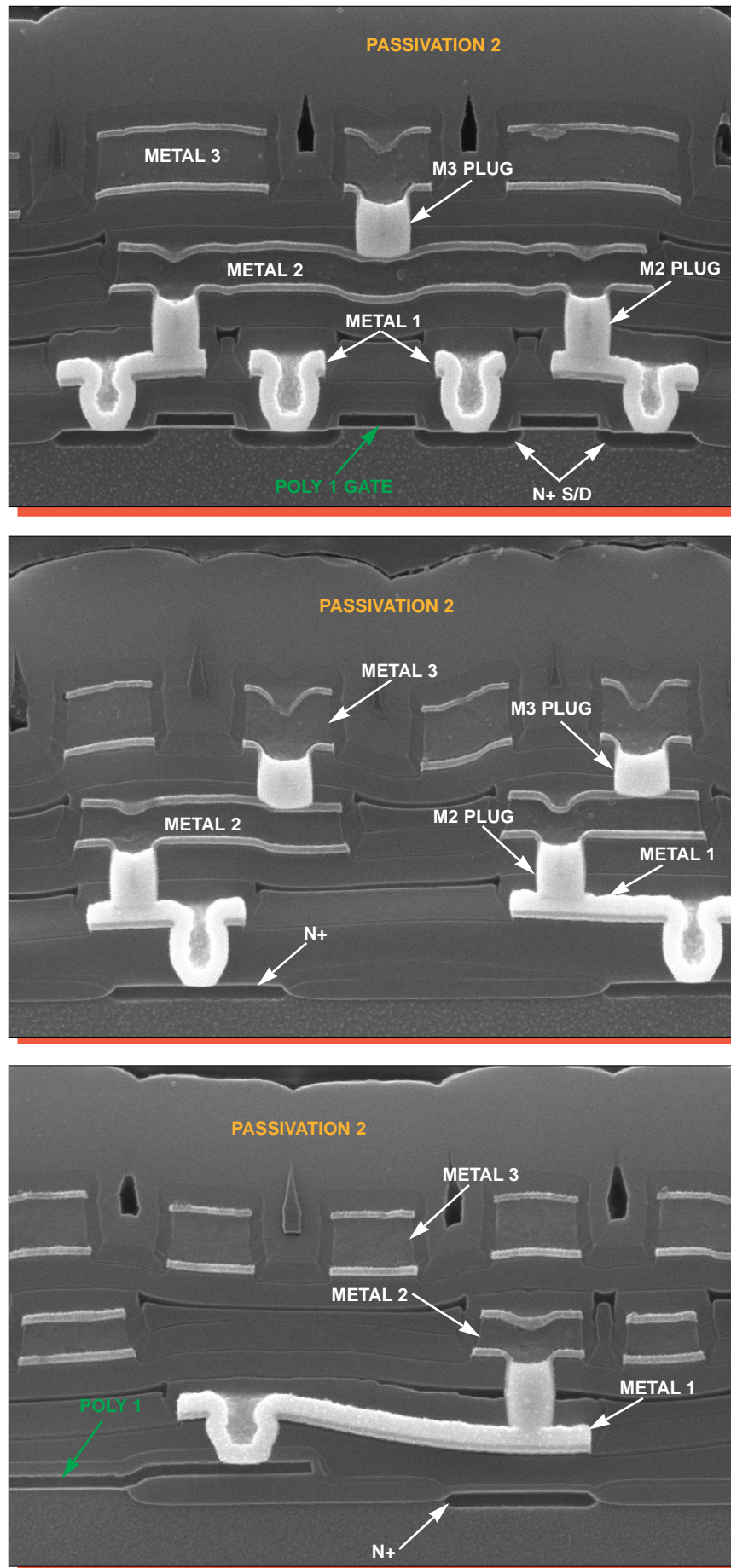


Figure 7. Silicon etch section views of general structure. Mag. 13,000x.

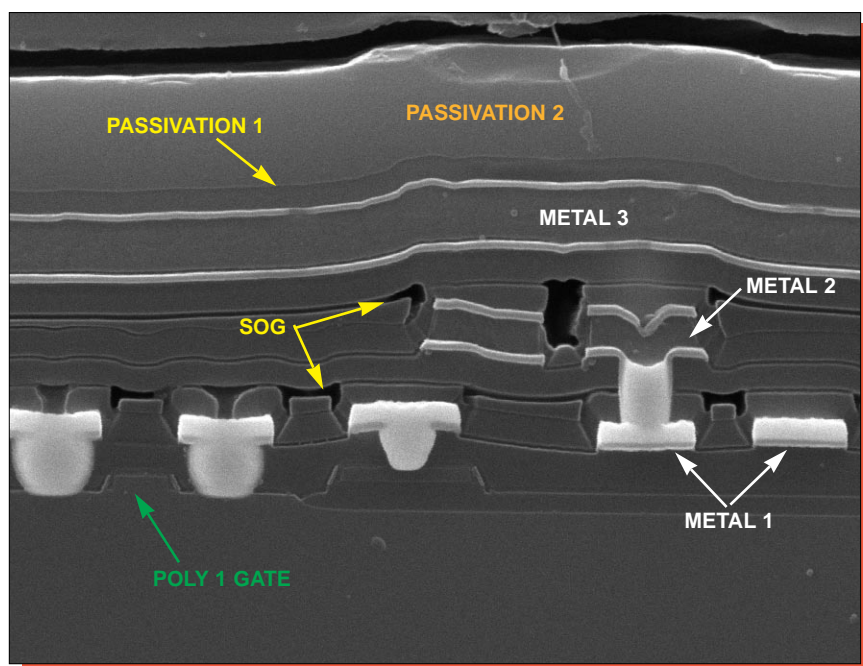
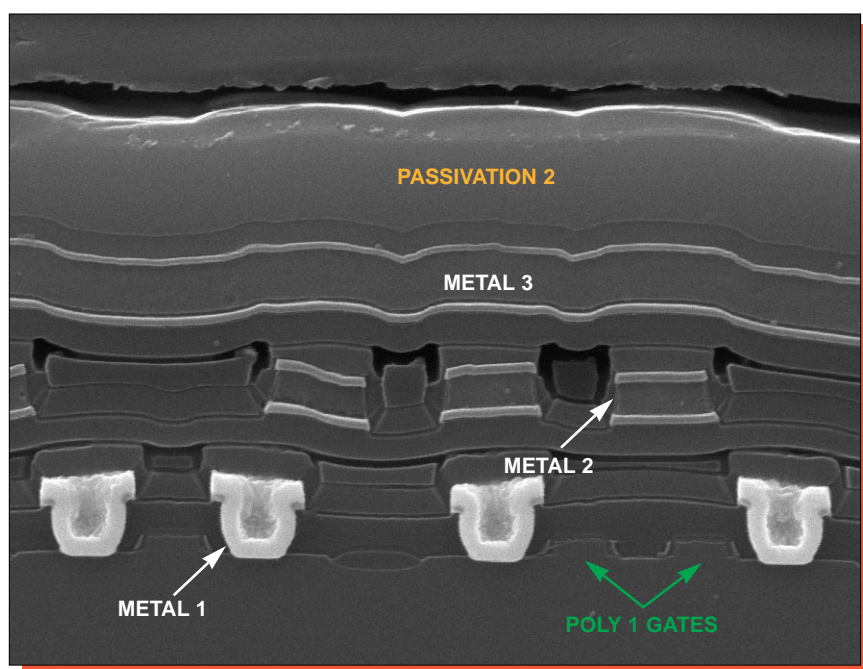
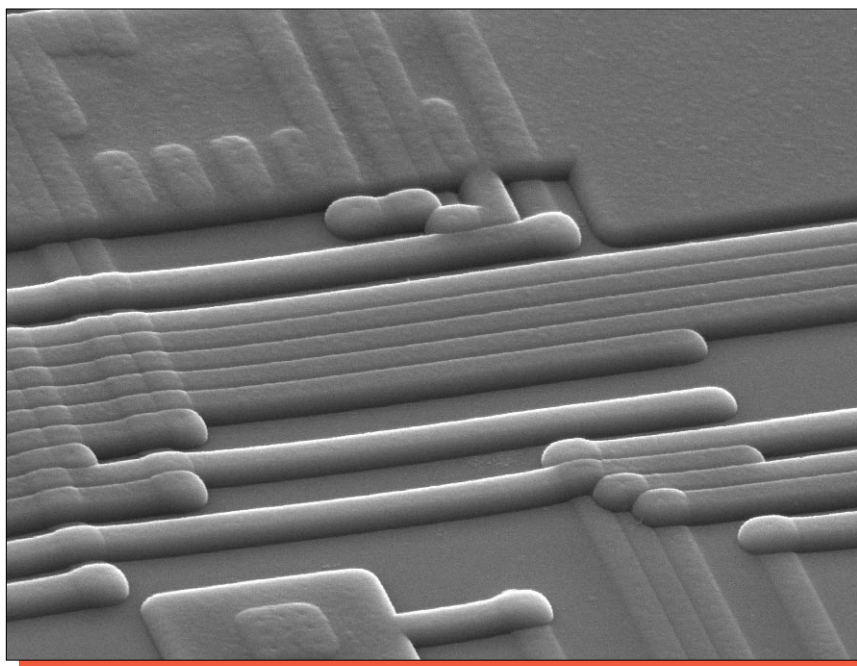
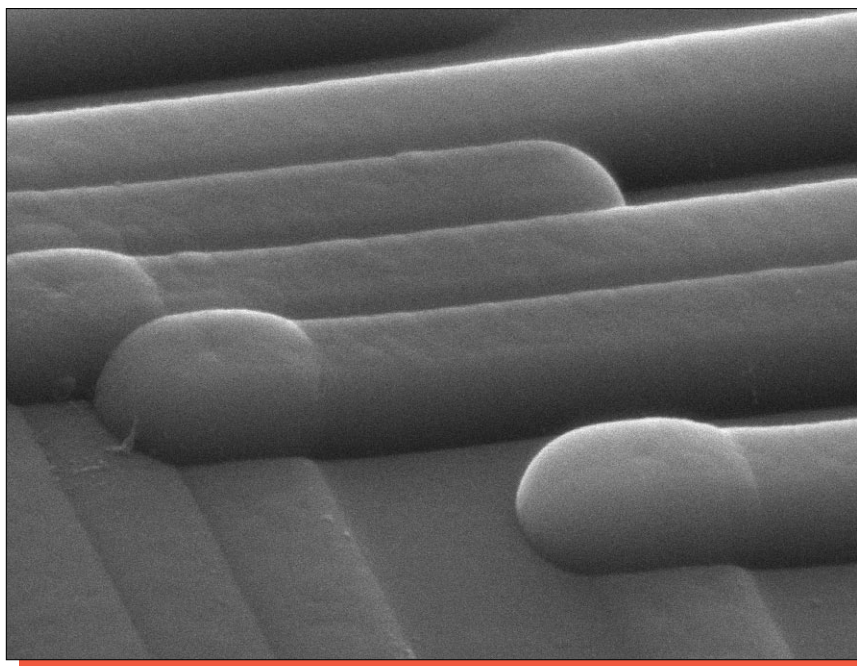


Figure 7a. Glass-etch section views of general structure. Mag. 12,000x.

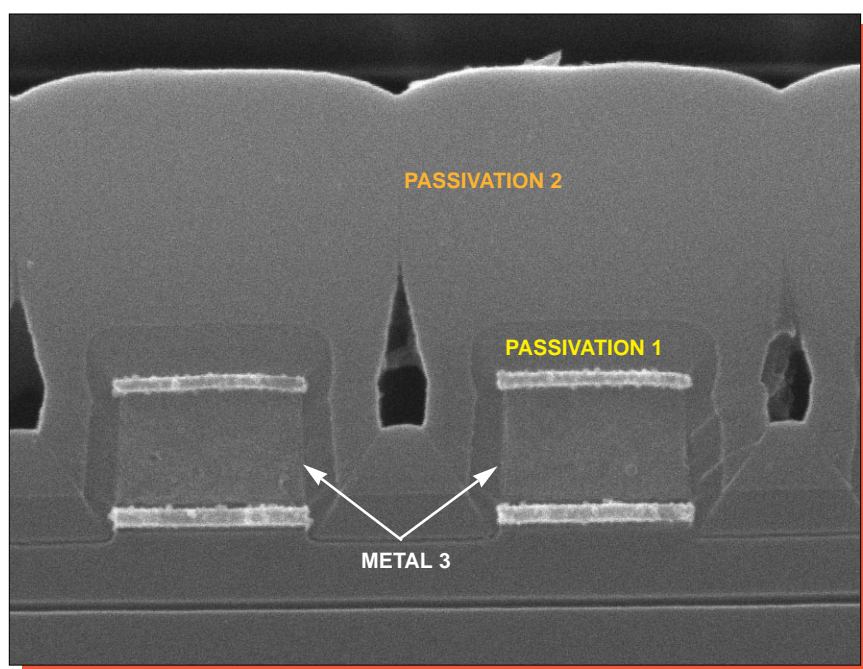


Mag. 2000x

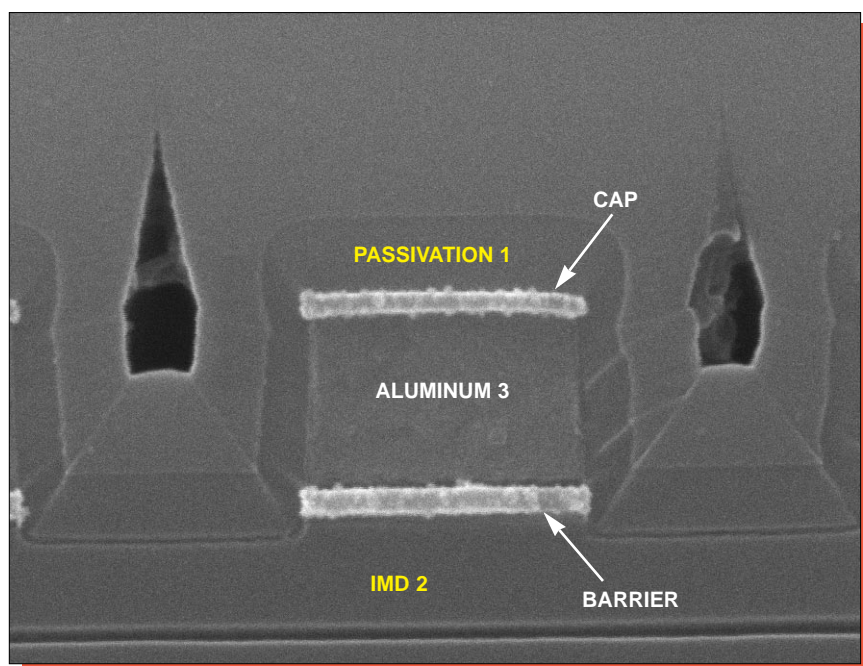


Mag. 8400x

Figure 8. SEM views of overlay passivation coverage. 60°.

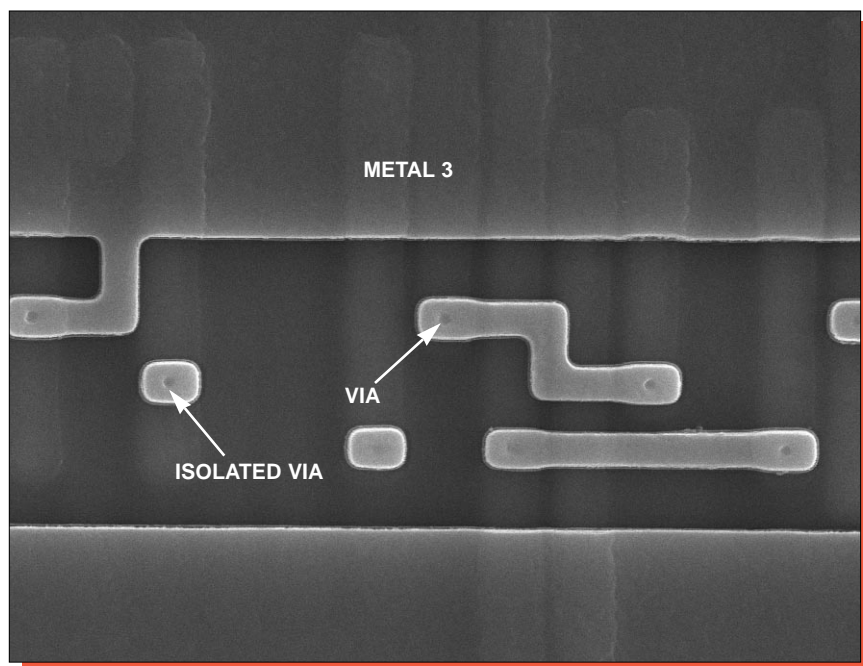


Mag. 26,000x

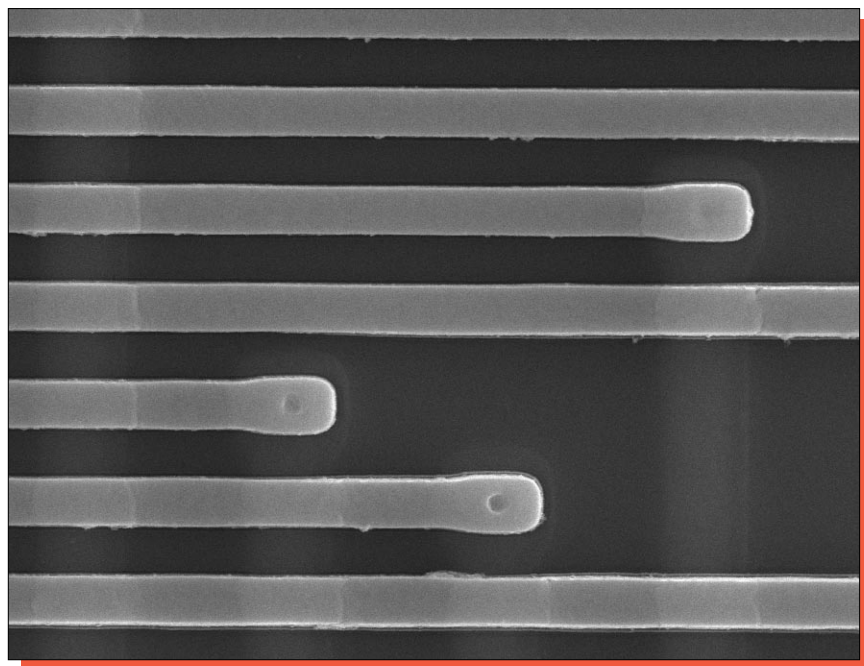


Mag. 40,000x

Figure 9. SEM section views of metal 3 line profiles.

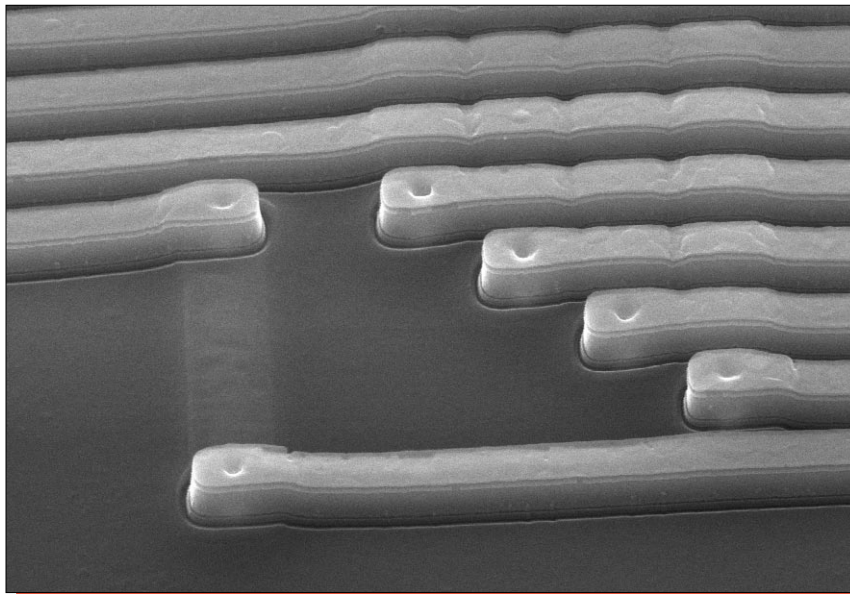


Mag. 4600x

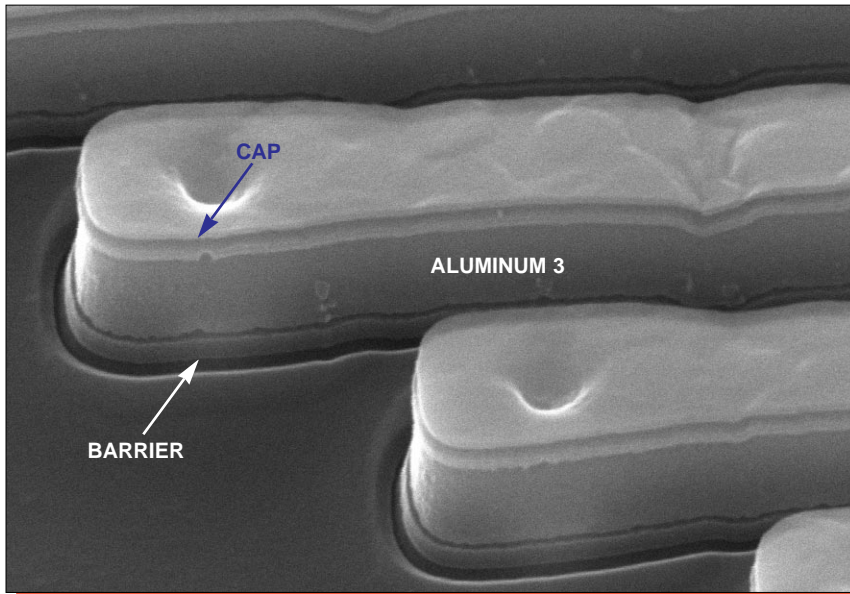


Mag. 7000x

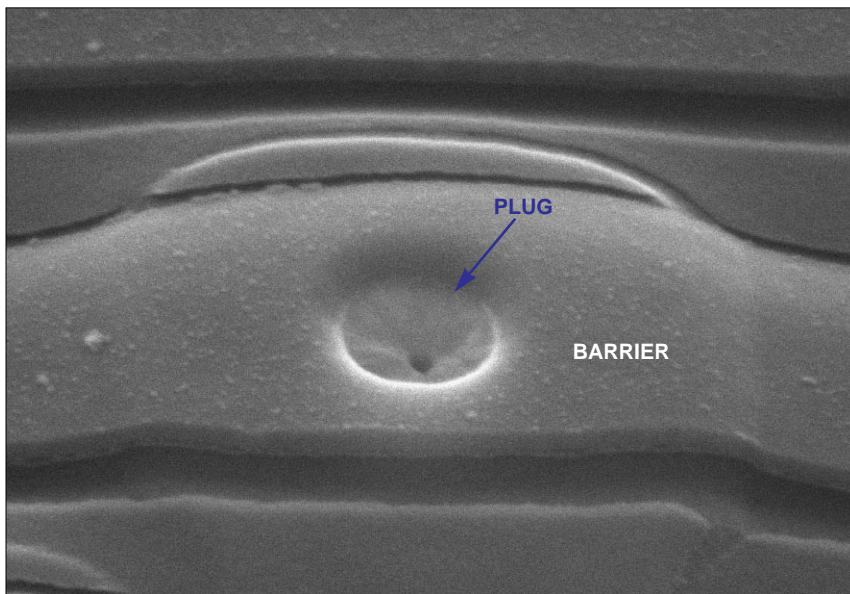
Figure 10. Topological SEM views of metal 3 patterning. 0°.



Mag. 6500x

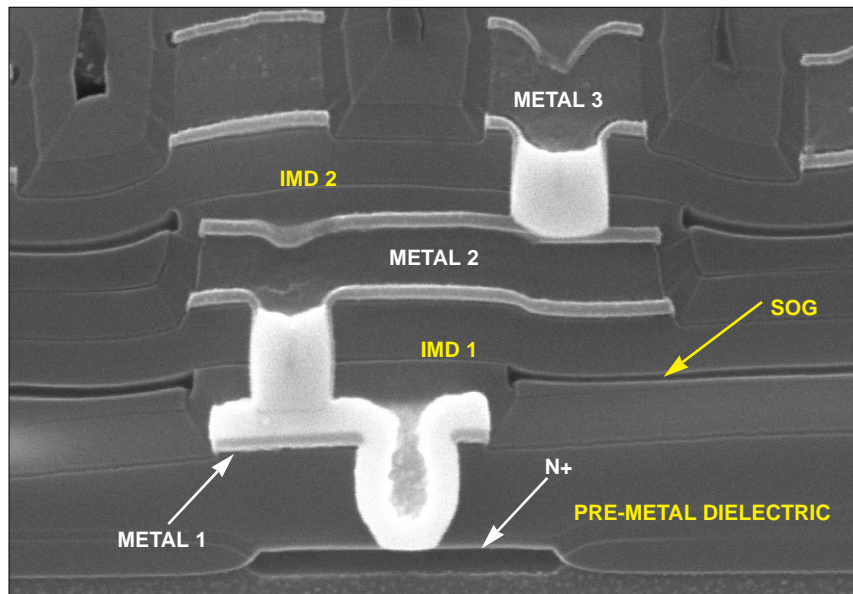


Mag. 23,000x

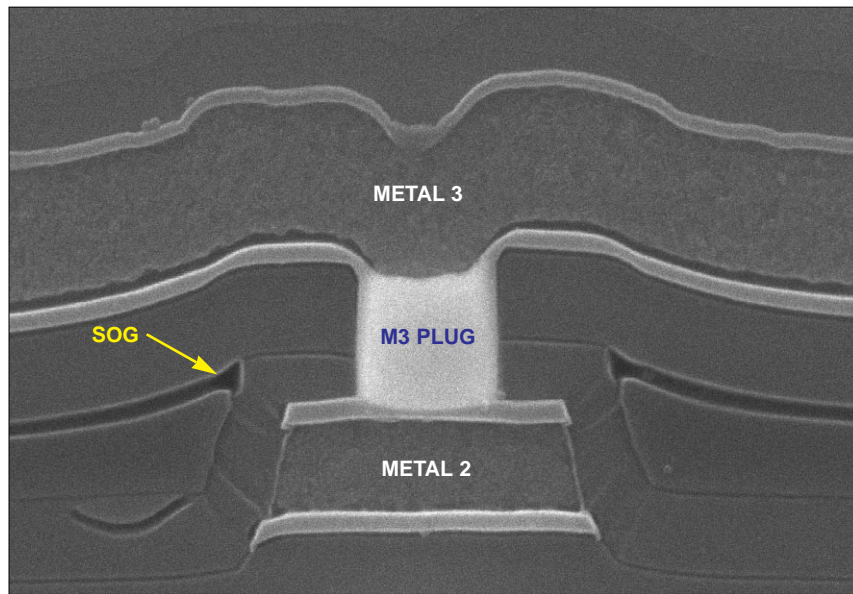


Mag. 40,000x

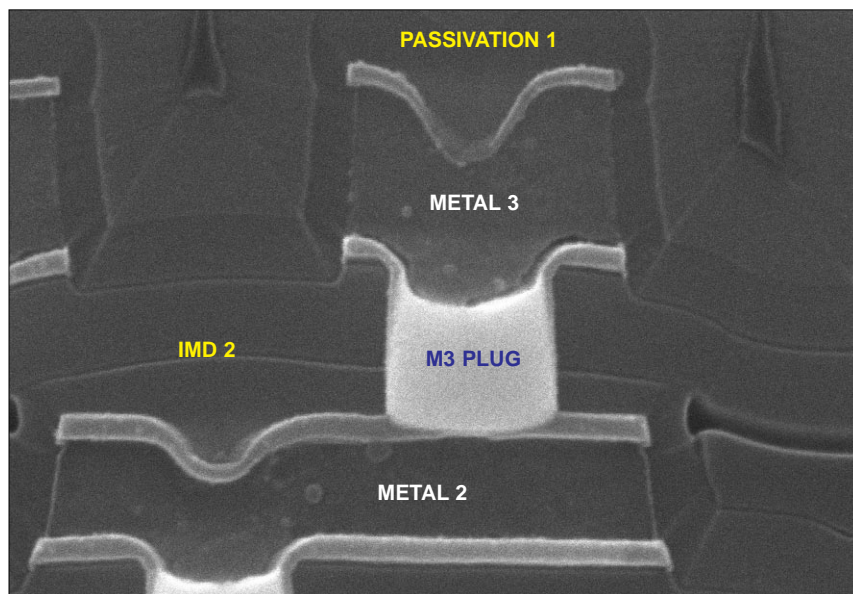
Figure 11. Perspective SEM views of metal 3 coverage. 60°.



Mag. 20,000x

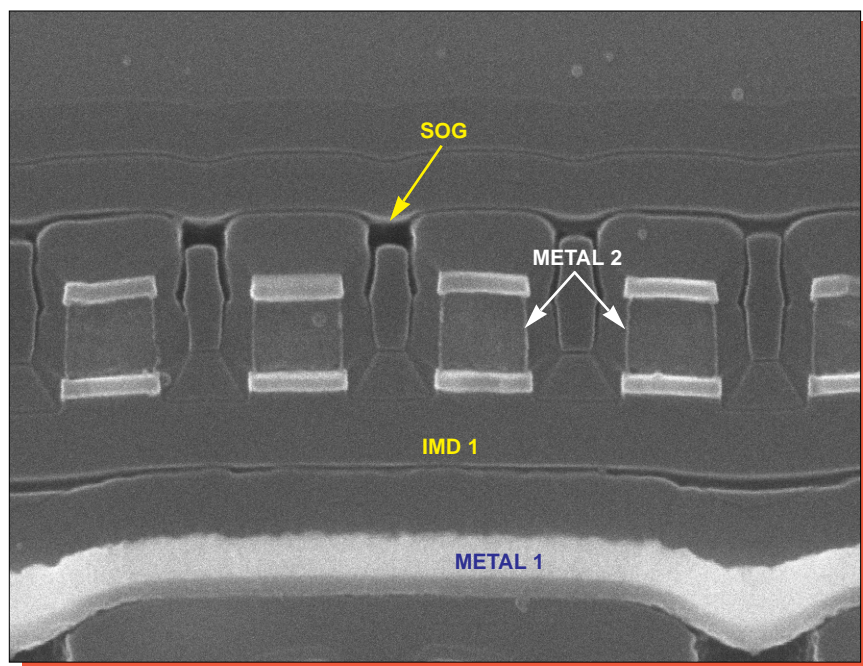


Mag. 30,000x

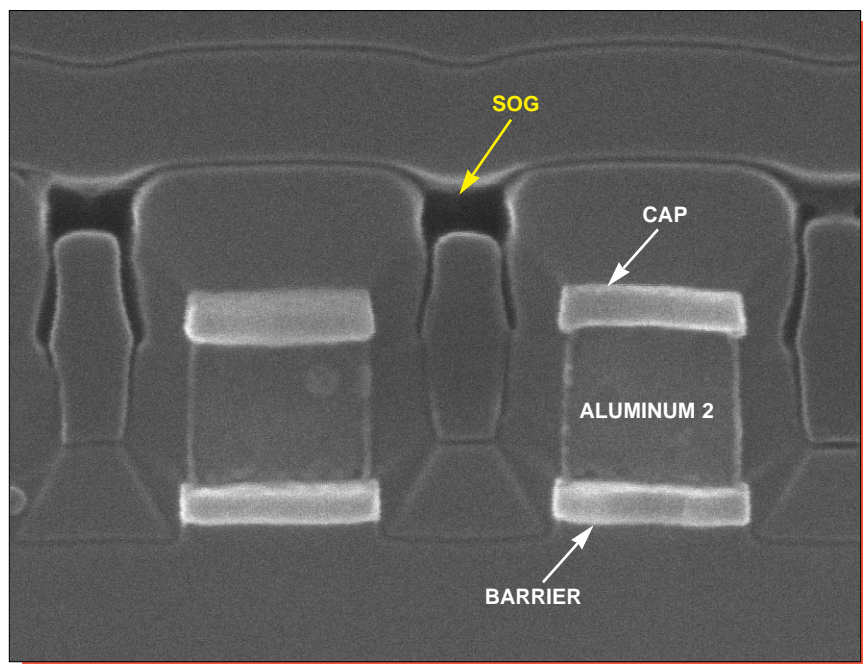


Mag. 35,000x

Figure 12. SEM section views of metal 3-to-metal 2 vias.

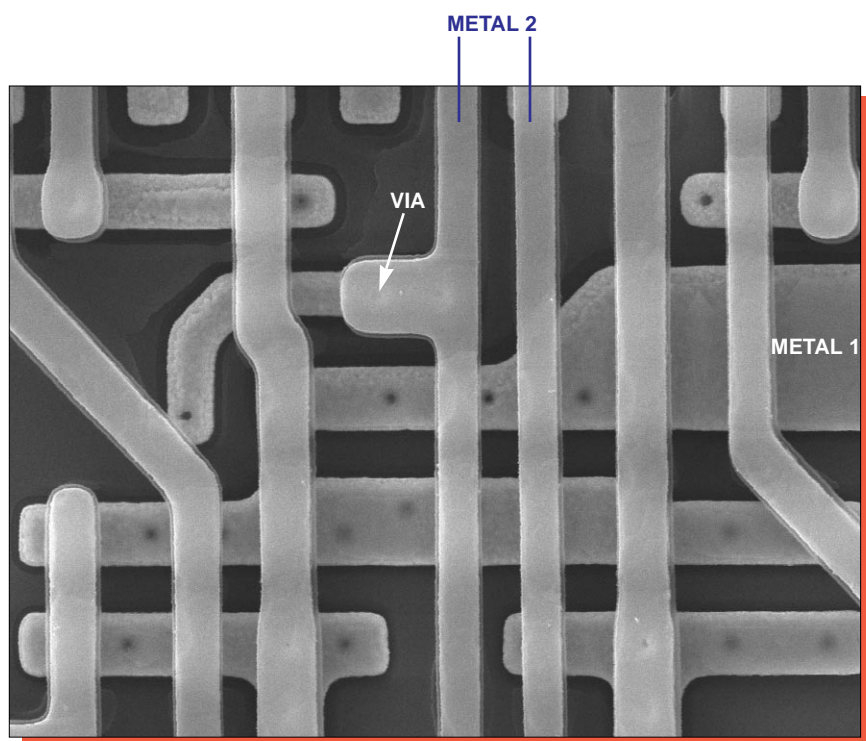


Mag. 26,000x

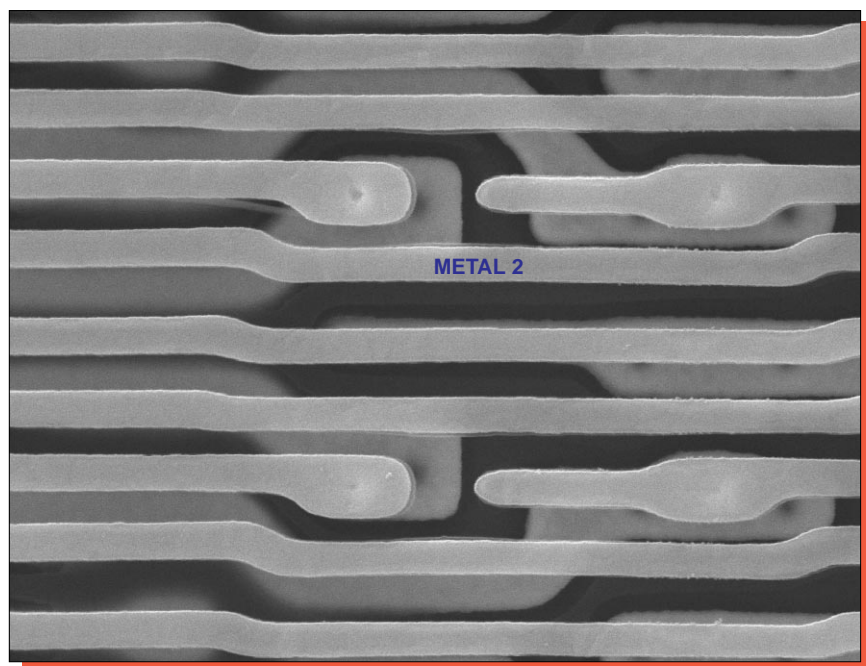


Mag. 52,000x

Figure 13. SEM section views of metal 2 line profiles.

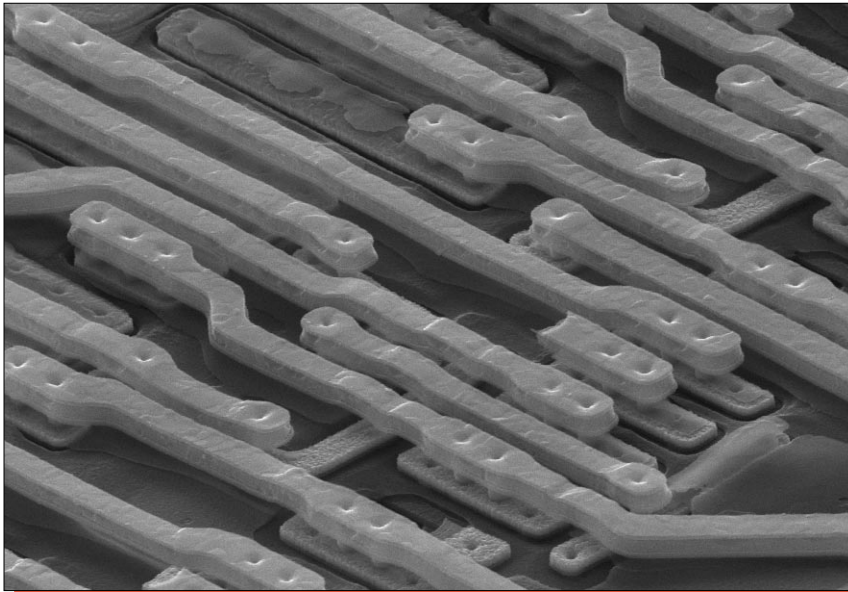


Periphery, Mag. 6500x

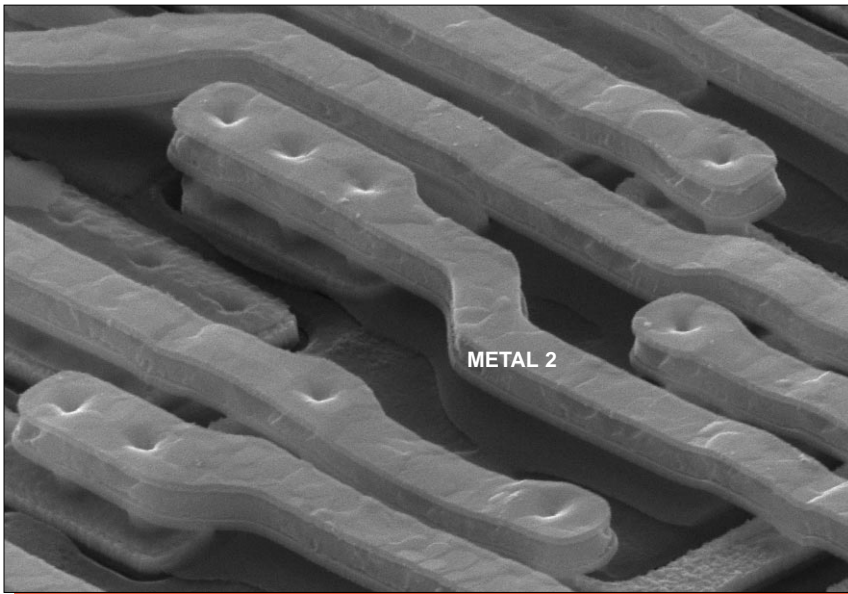


Row Decode, Mag. 10,000x

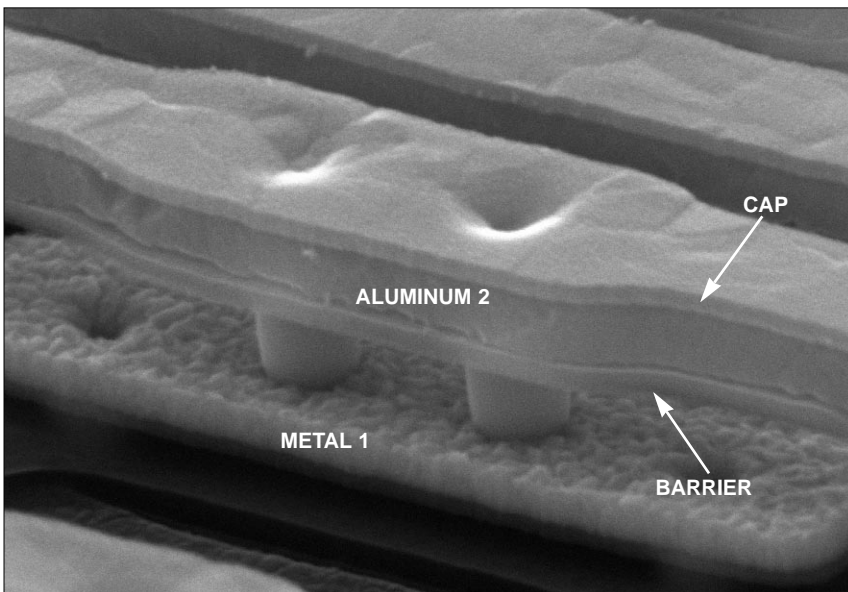
Figure 14. Topological SEM views of metal 2 patterning. 0°.



Mag. 5000x

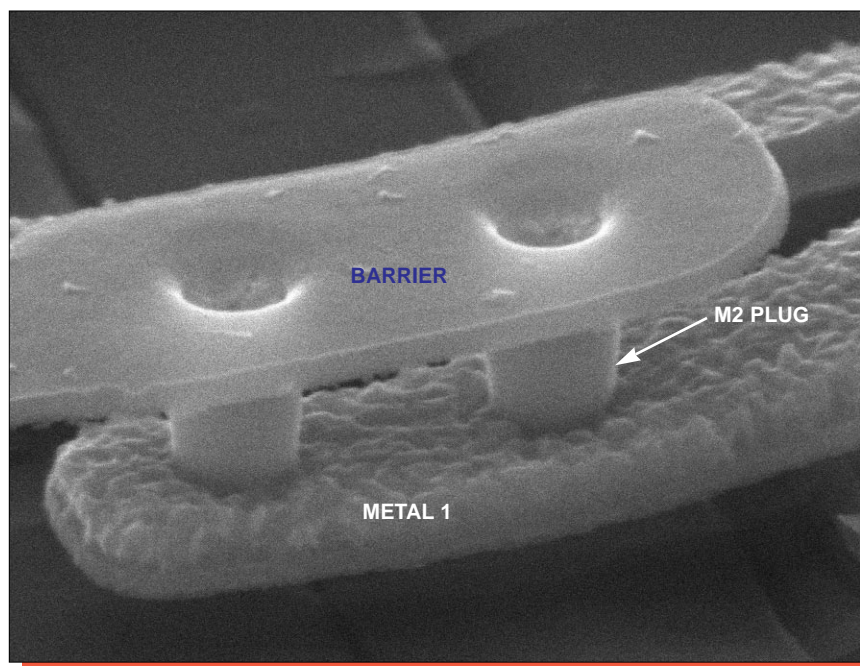


Mag. 10,000x

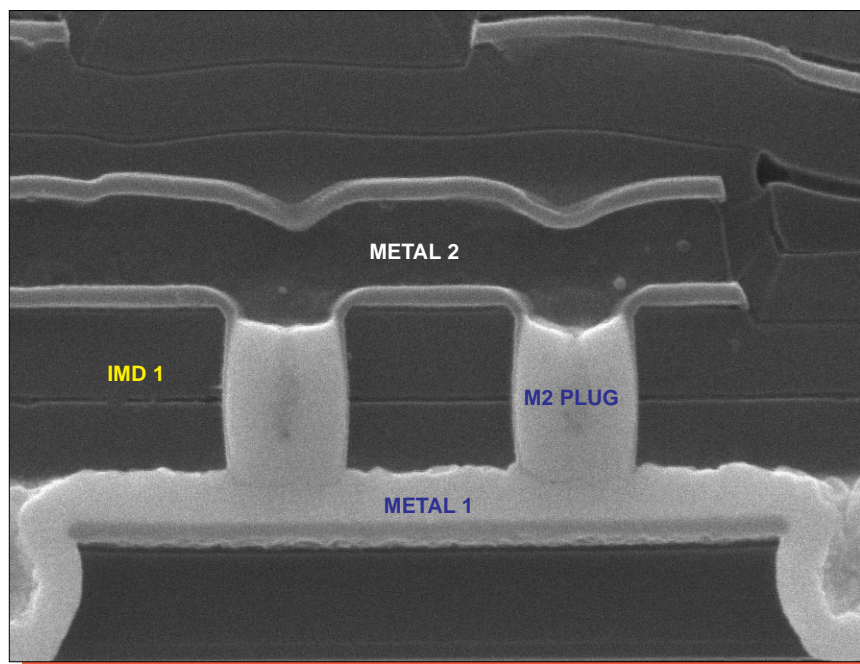


Mag. 25,000x

Figure 15. Perspective SEM views of metal 1 coverage. 60°.

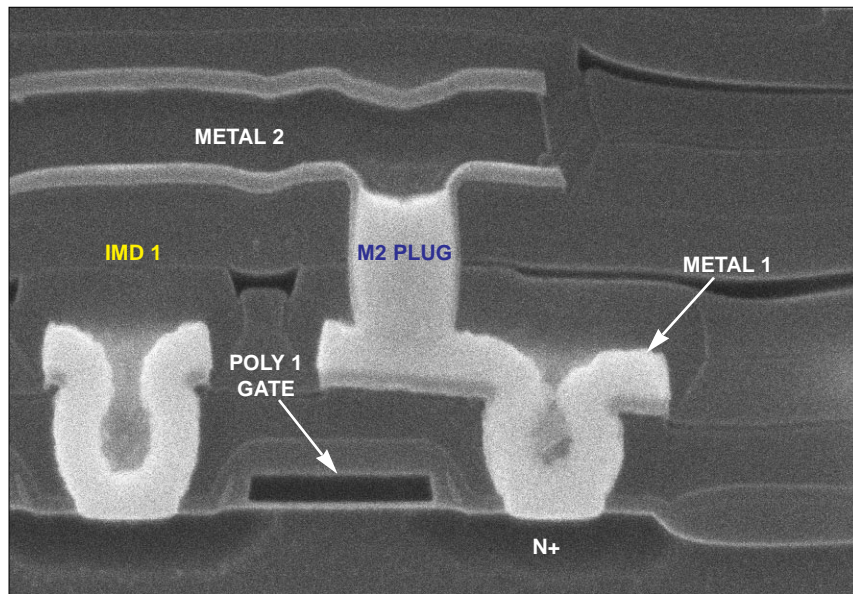


Mag. 35,000x, 60°

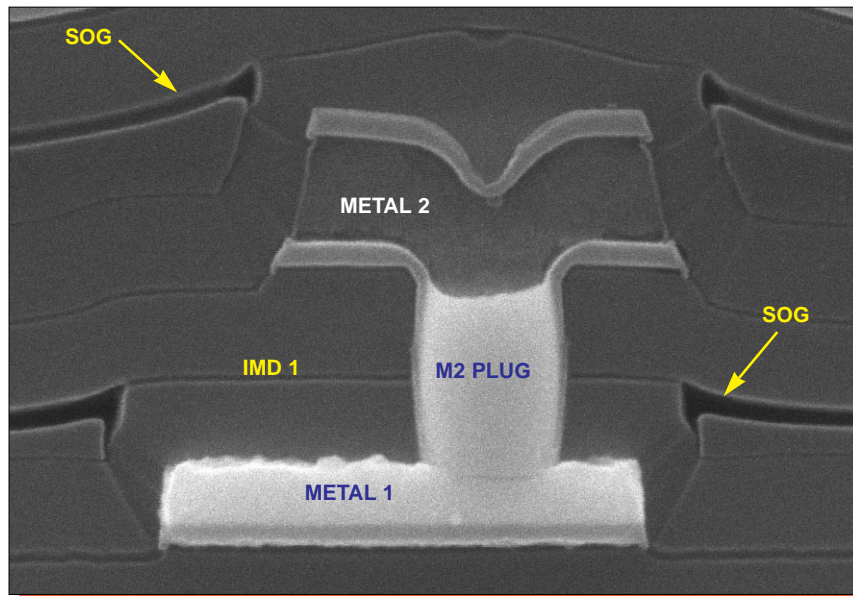


Mag. 31,000x

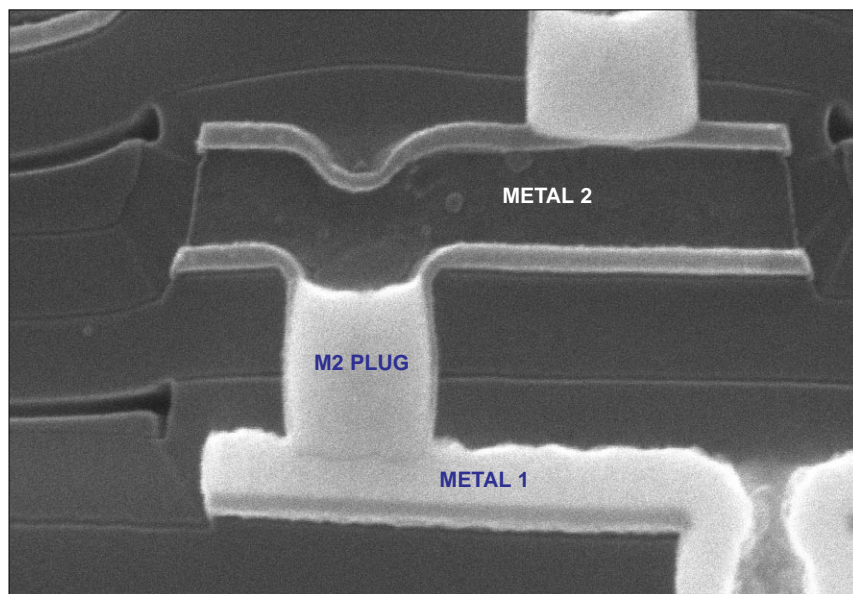
Figure 16. SEM views of metal 2 barrier and metal 2-to-metal 1 vias.



Mag. 26,000x

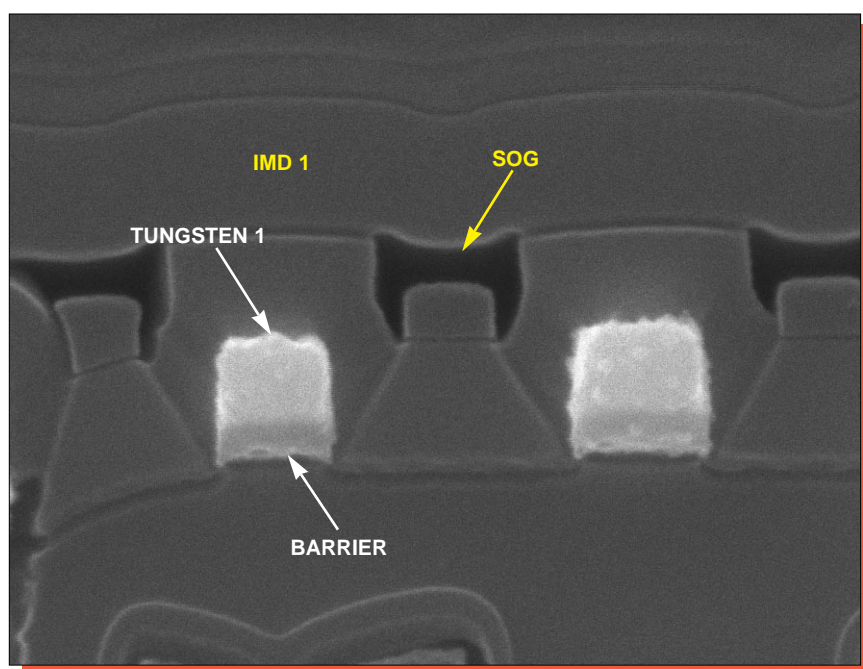


Mag. 35,000x

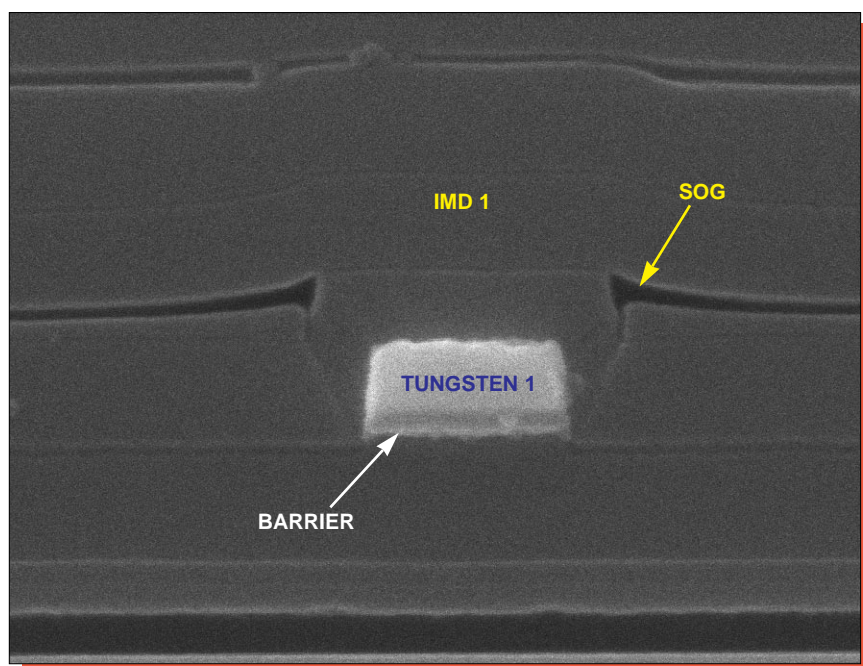


Mag. 35,000x

Figure 17. Additional SEM section views of metal 2-to-metal 1 vias.



Array, Mag. 52,000x



Periphery, Mag. 40,000x

Figure 18. SEM section views of metal 1 line profiles.

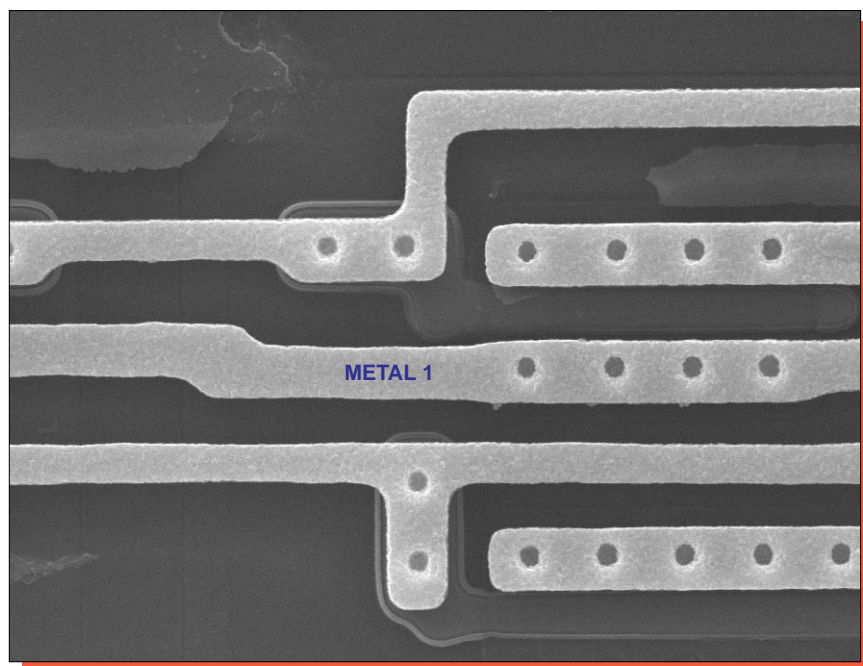
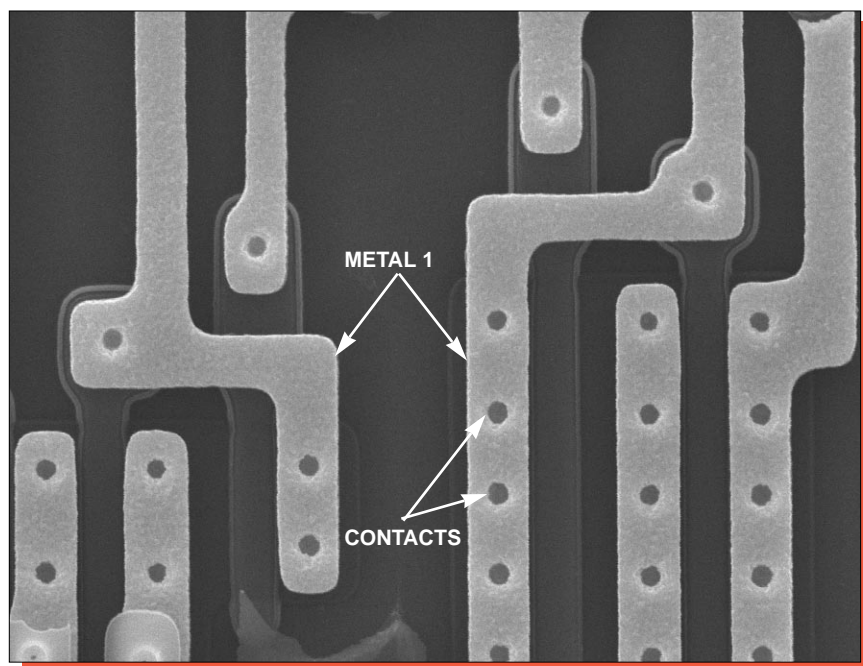
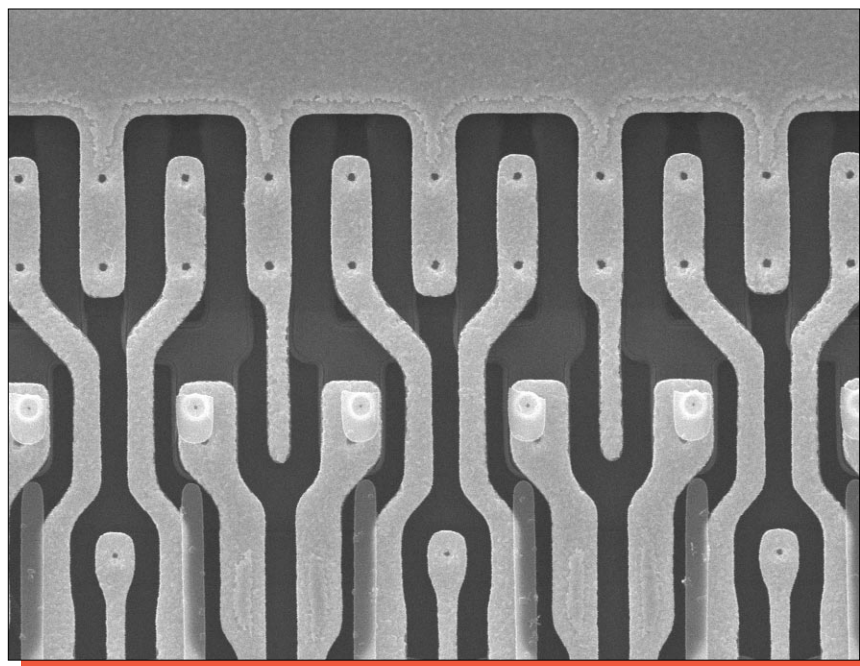
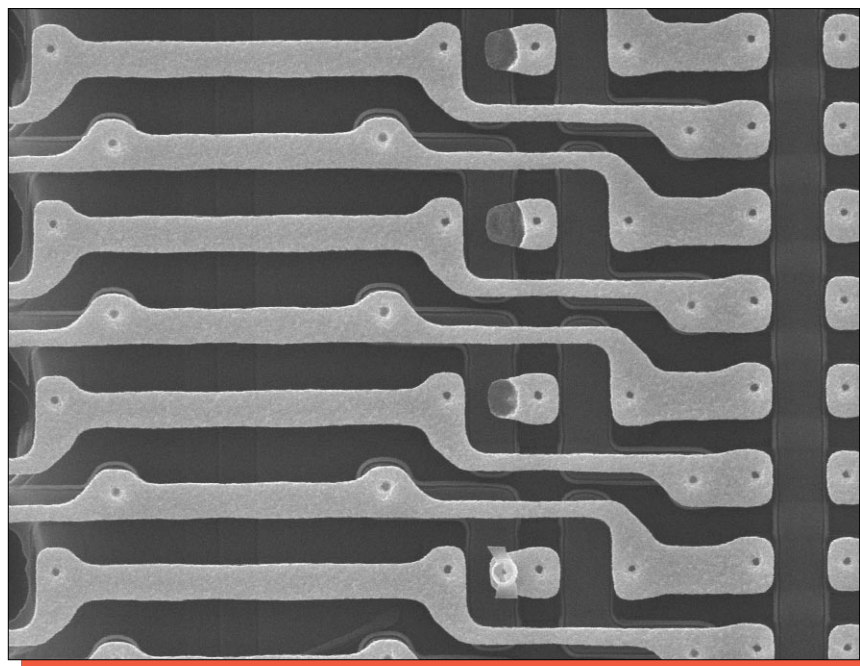


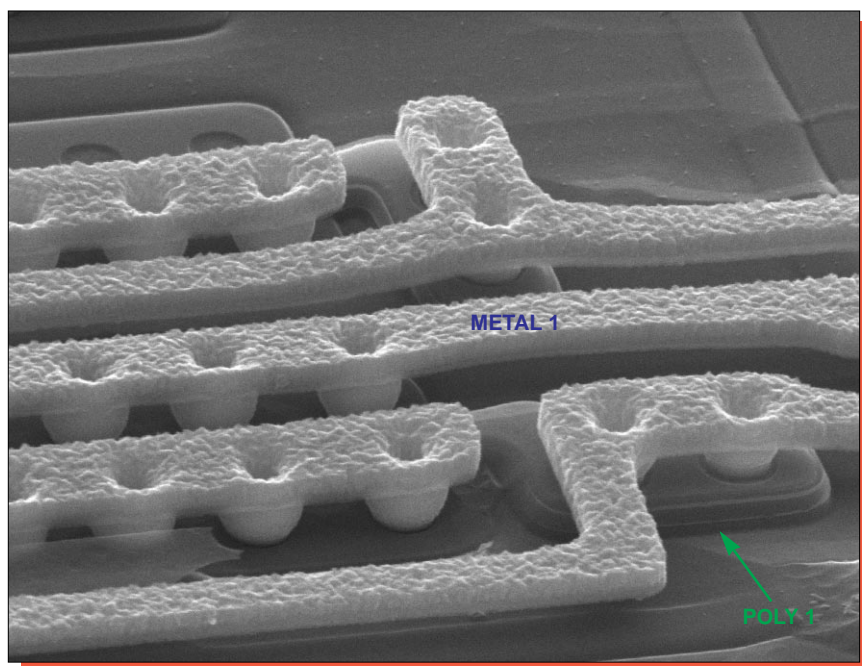
Figure 19. Topological SEM views of metal 1 patterning in the periphery. Mag. 8000x, 0°.



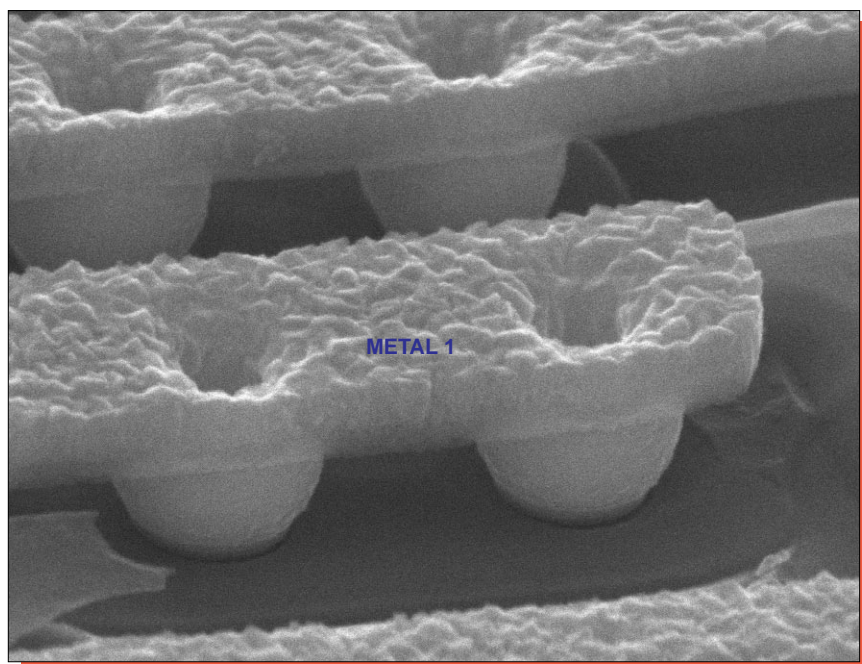
Row Decode



Column Decode

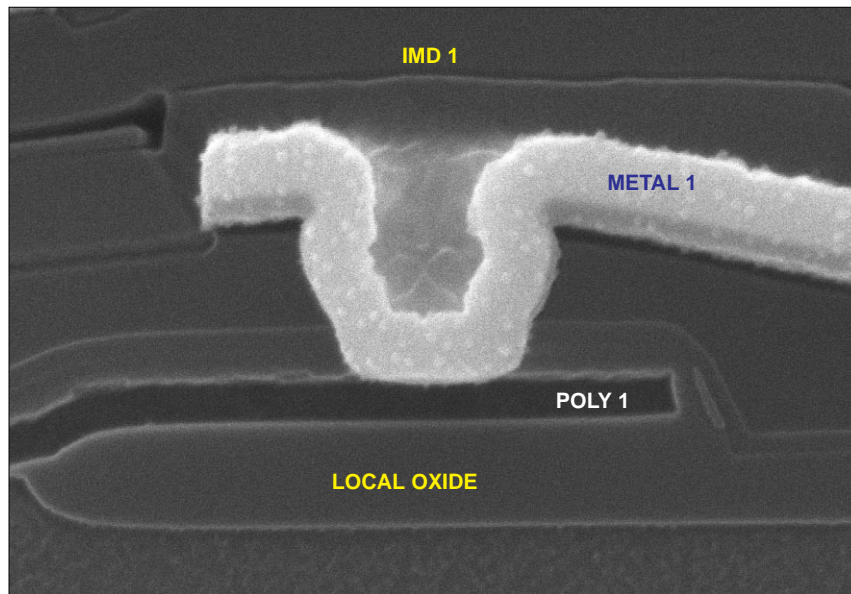


Mag. 14,000x

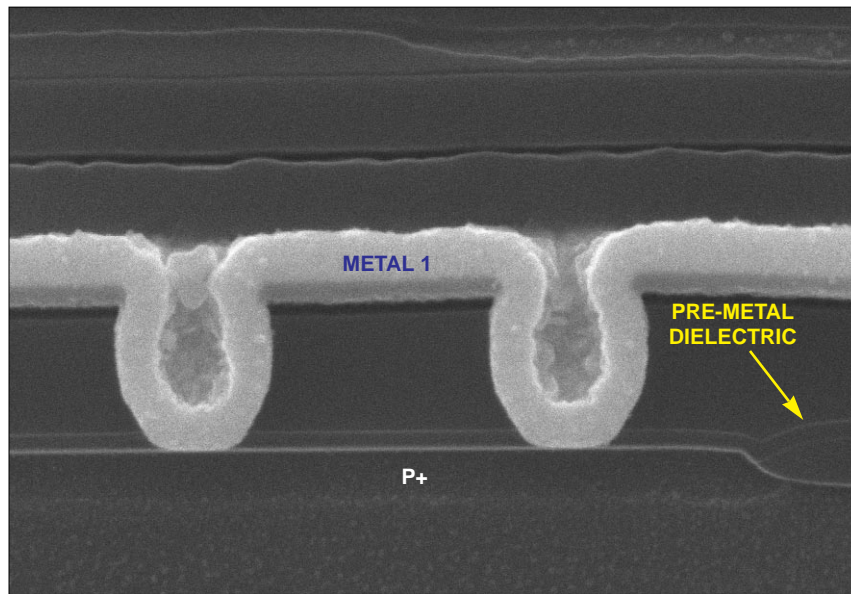


Mag. 35,000x

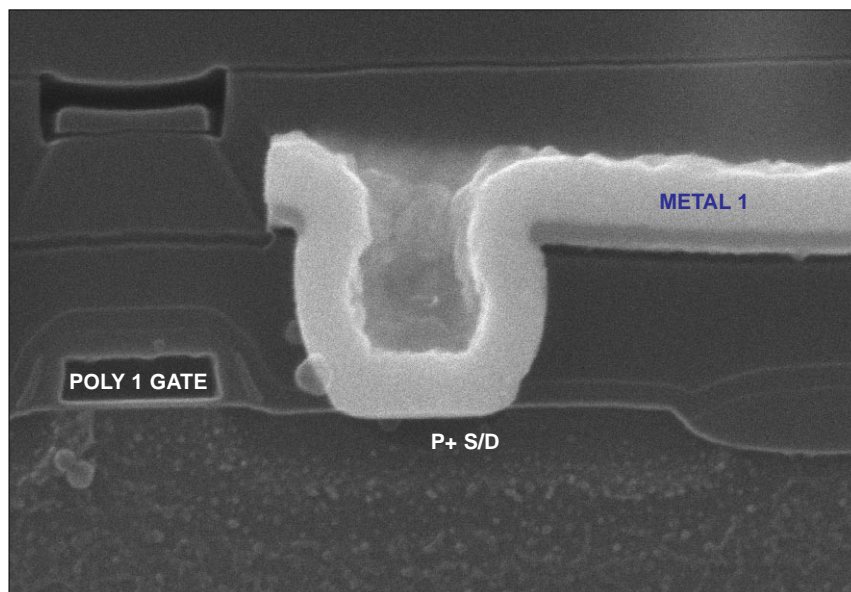
Figure 21. Perspective SEM views of metal 1 coverage. 60°.



metal 1-to-poly 1,
Mag. 40,000x

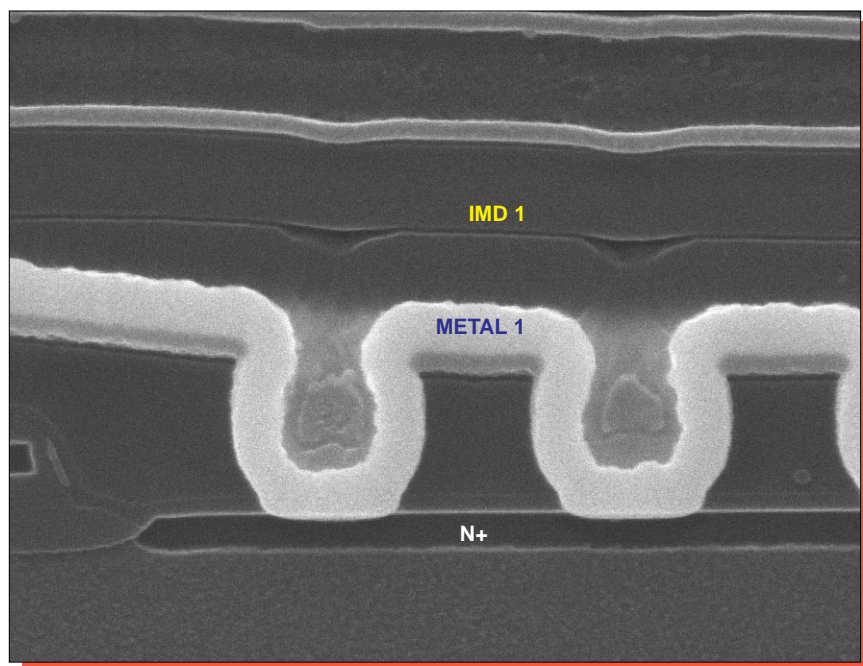


metal 1-to-P+,
Mag. 30,000x

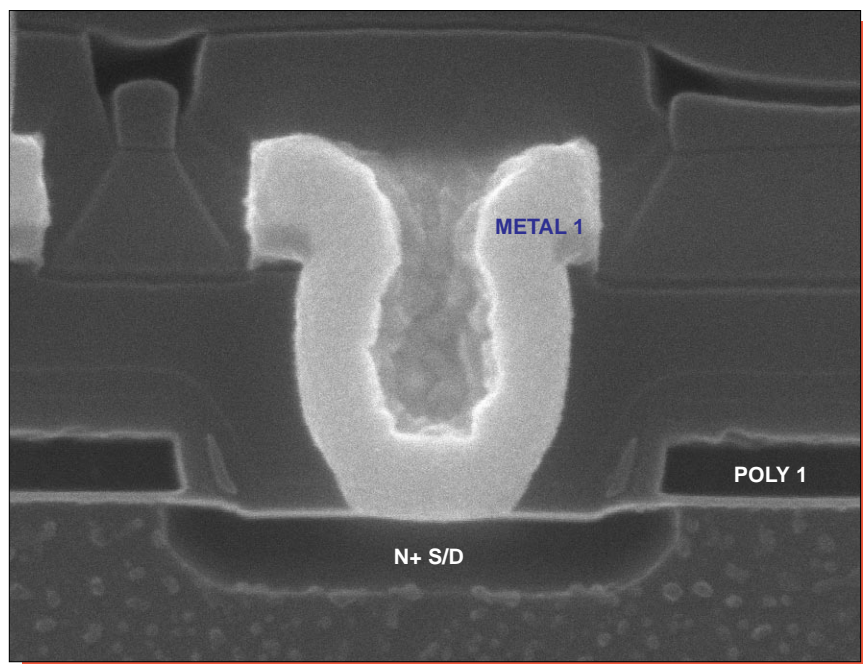


metal 1-to-P+,
Mag. 40,000x

Figure 22. SEM section views of metal 1 contacts.



Mag. 30,000x



Mag. 52,000x

Figure 23. SEM section views of metal 1-to-N+ diffusion contacts.

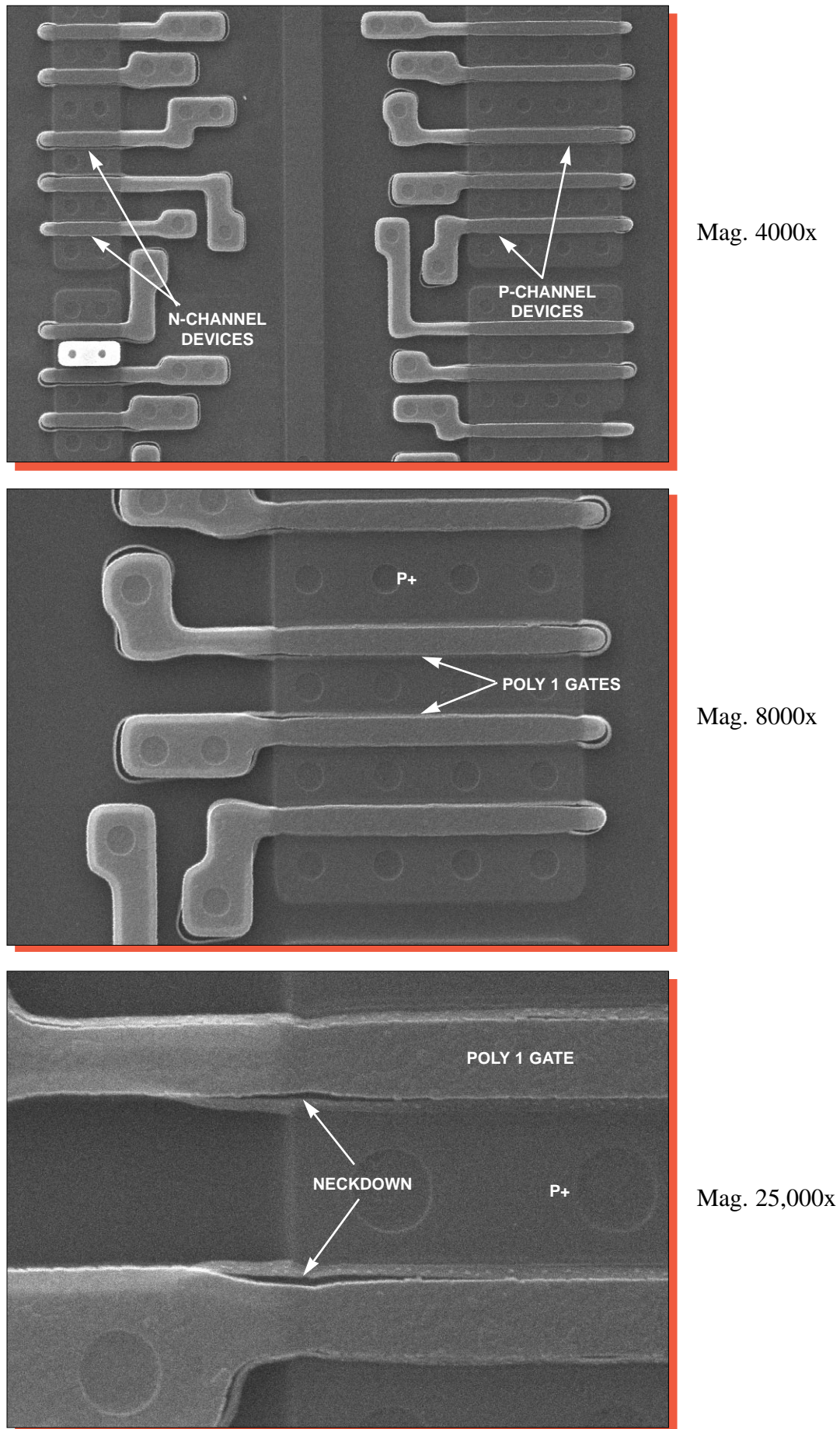
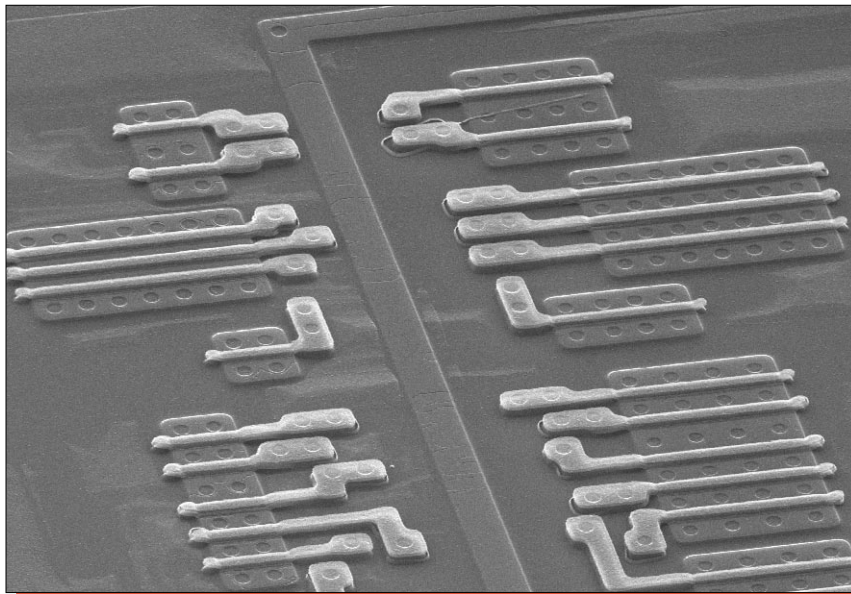
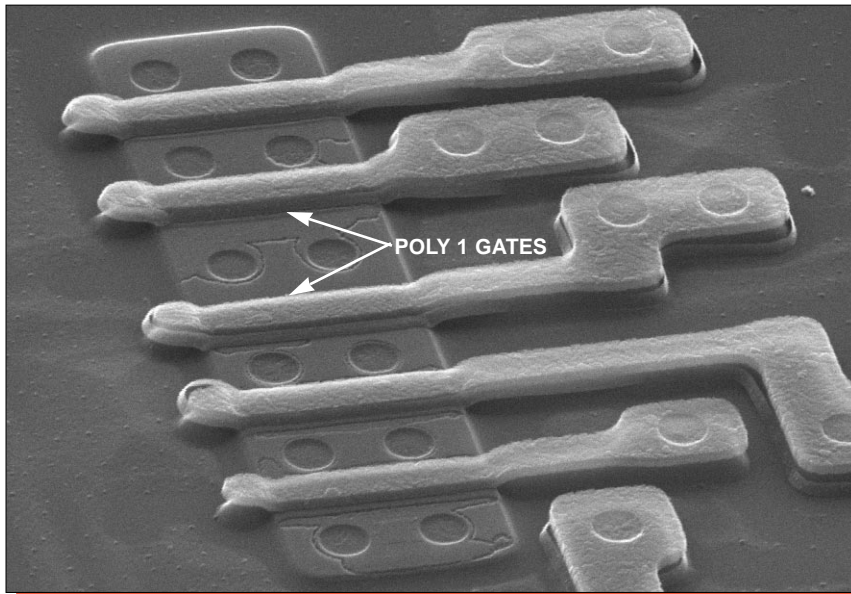


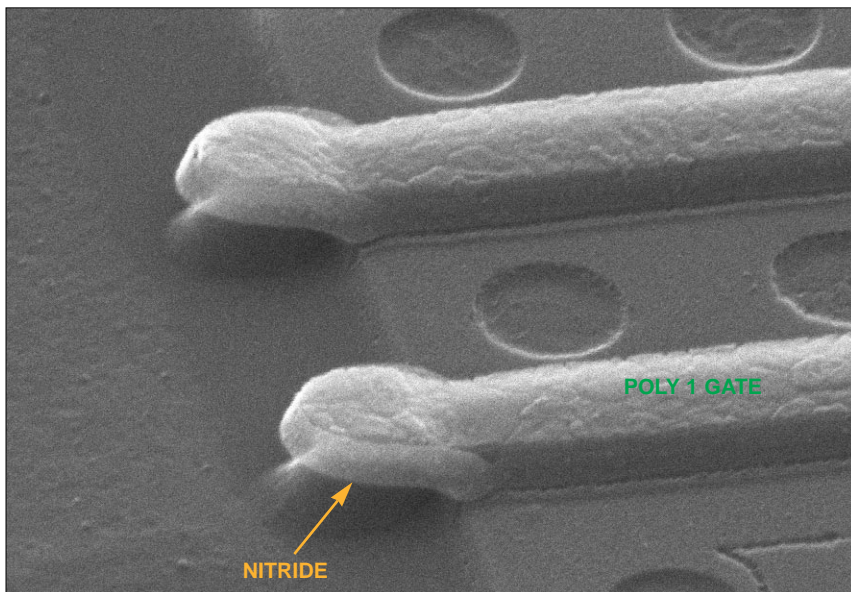
Figure 24. Topological SEM views of poly 1 patterning. 0°.



Mag. 3000x

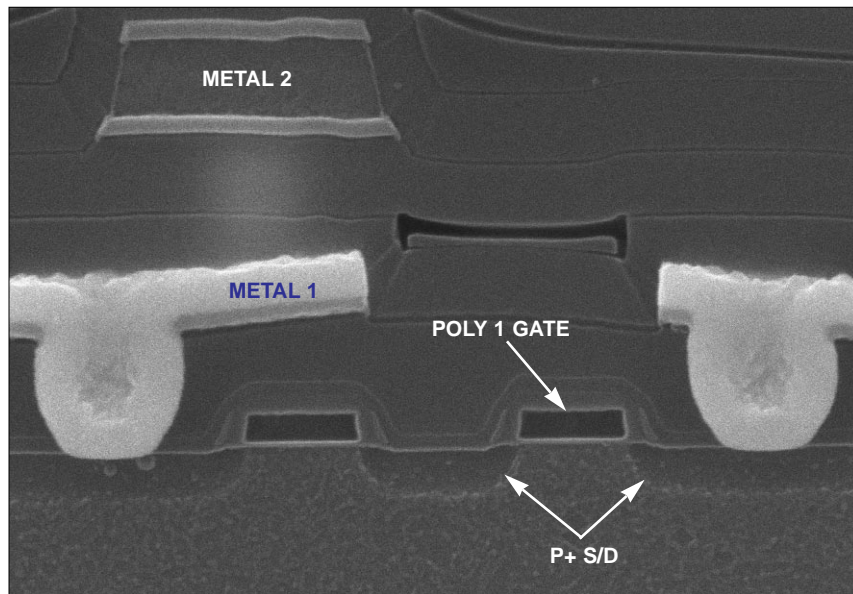


Mag. 10,000x

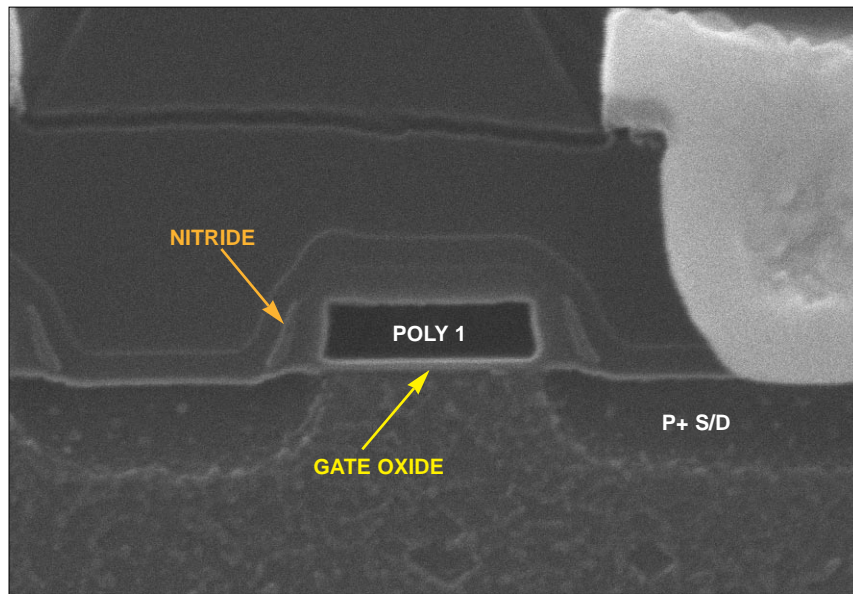


Mag. 30,000x

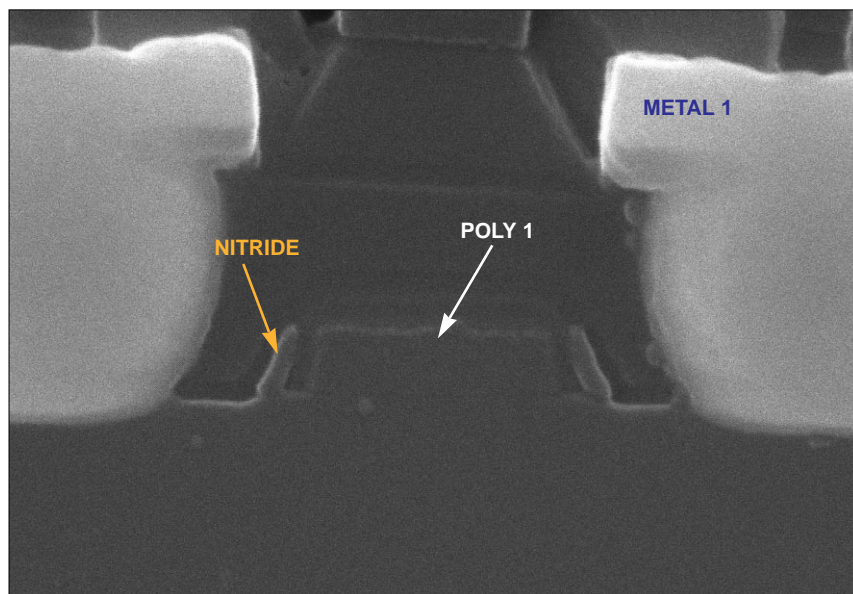
Figure 25. Perspective SEM views of poly 1 coverage. 60°.



Mag. 26,000x

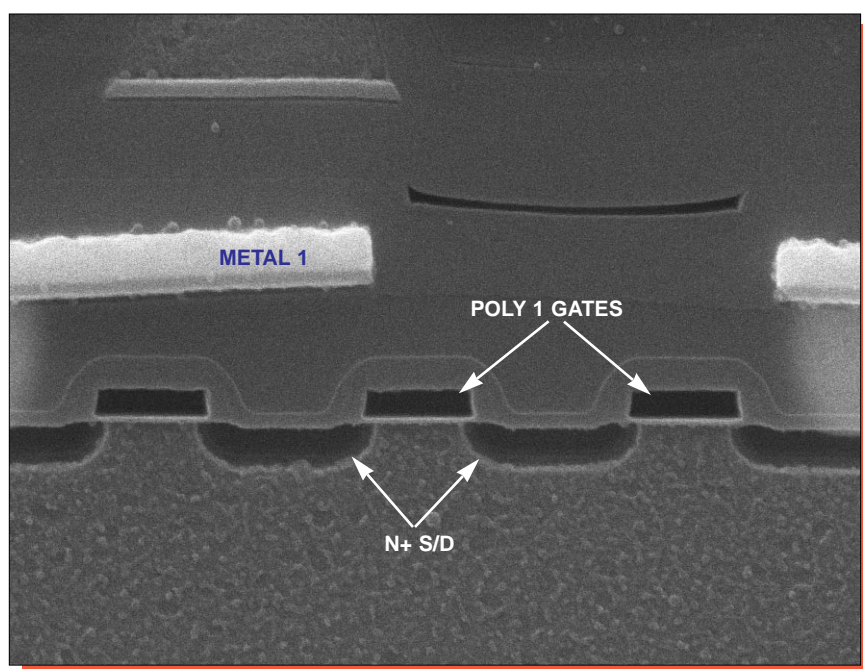


Mag. 52,000x

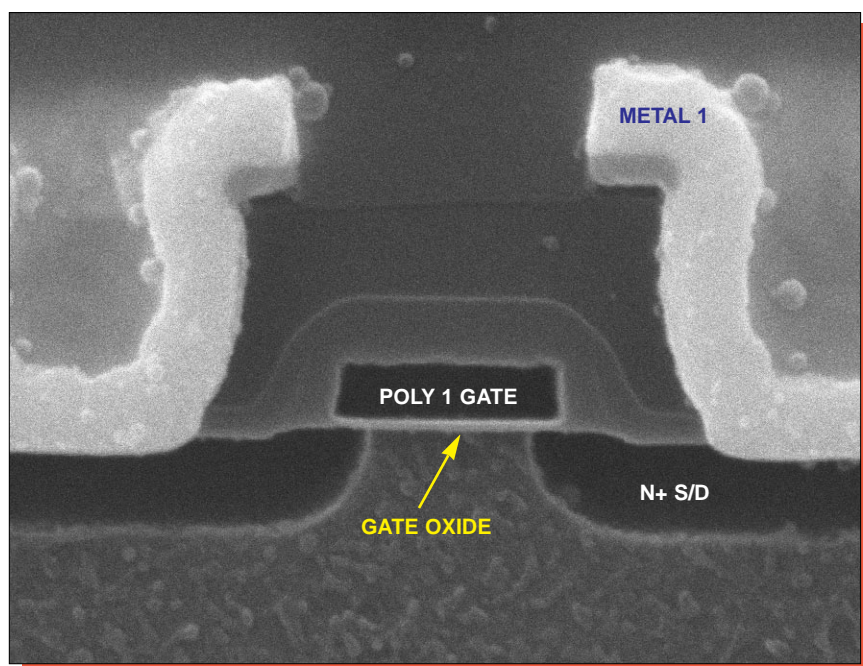


Mag. 52,000x

Figure 26. SEM section views of typical P-channel transistors.

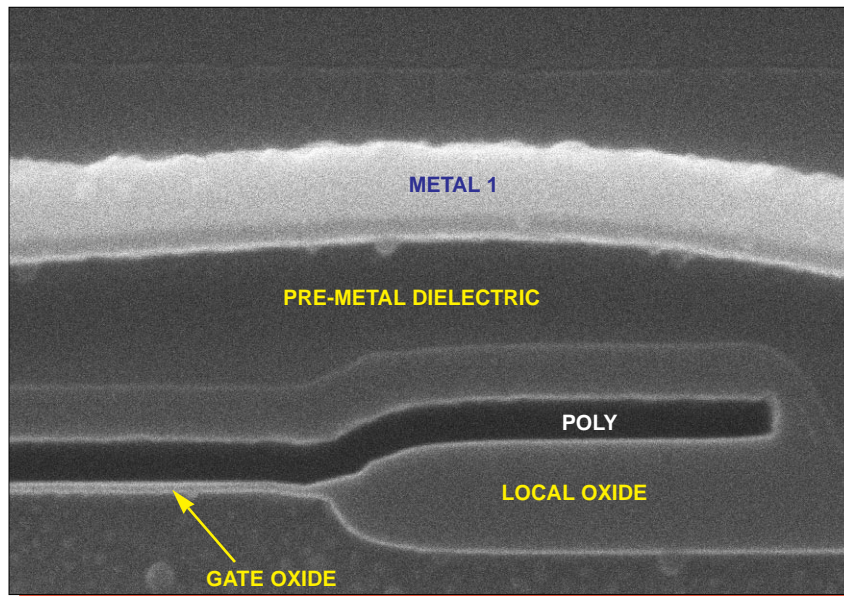


Mag. 26,000x

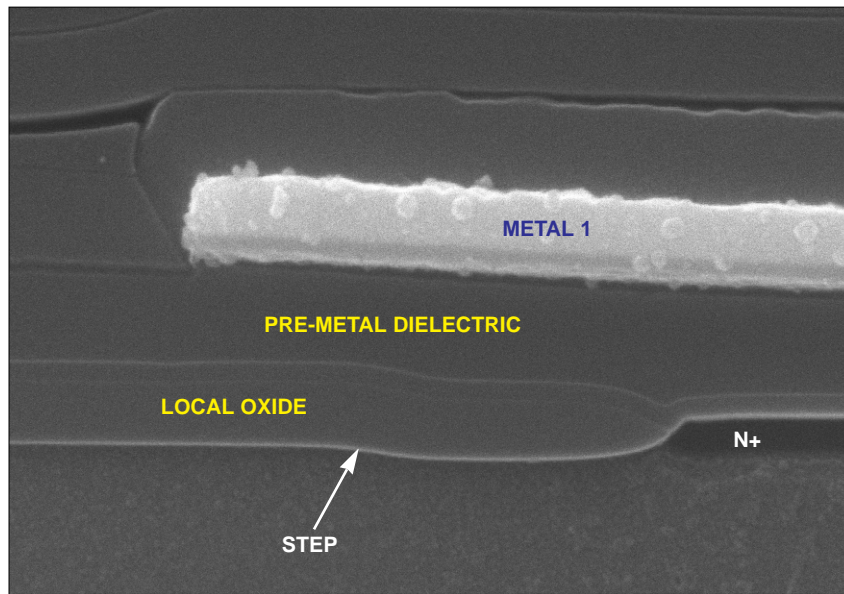


Mag. 52,000x

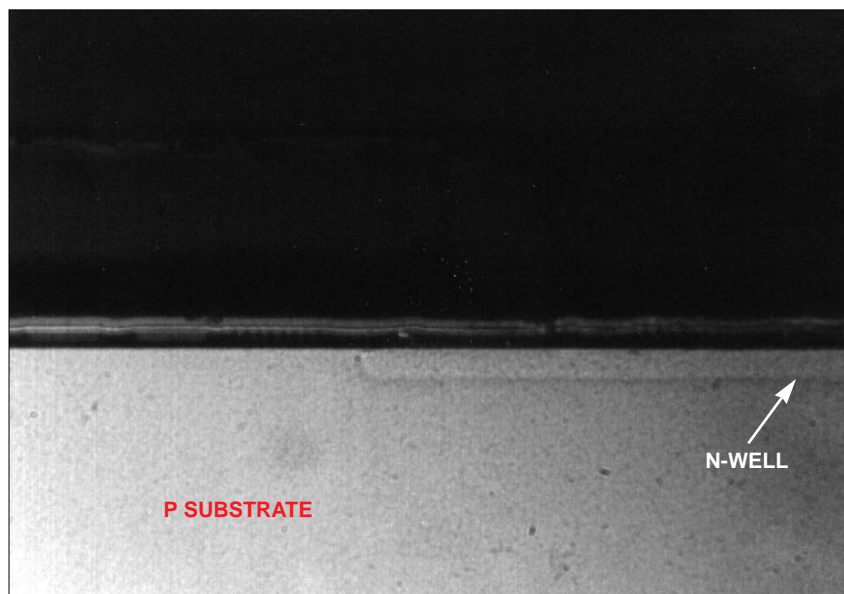
Figure 27. SEM section views of typical N-channel transistors.



Mag. 40,000x

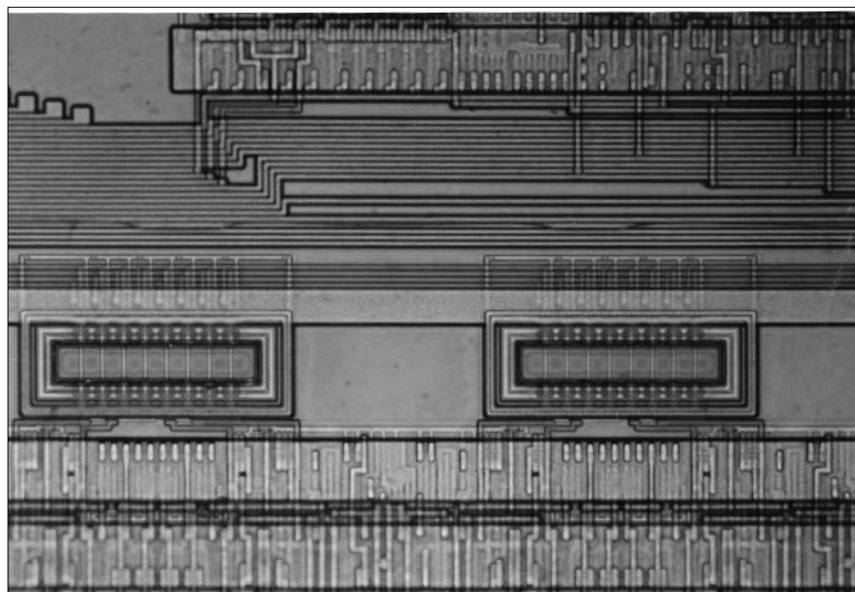


Mag. 35,000x

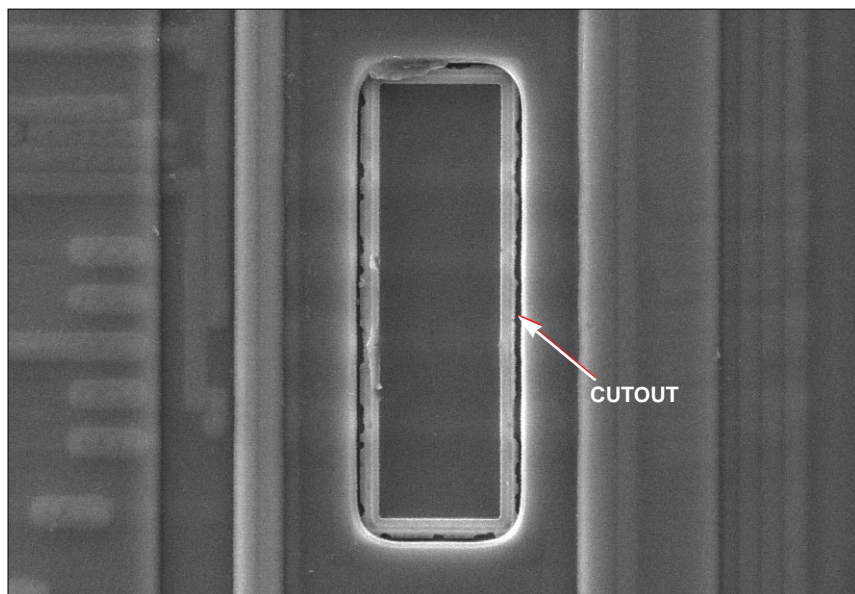


Mag. 800x

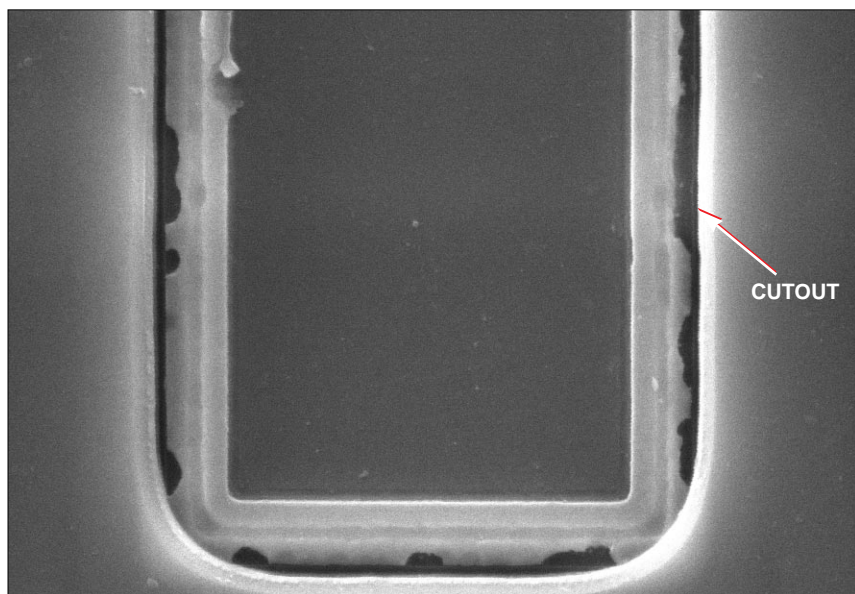
Figure 28. Optical and SEM section views of a birdsbeak and the well structure.



Mag. 400x

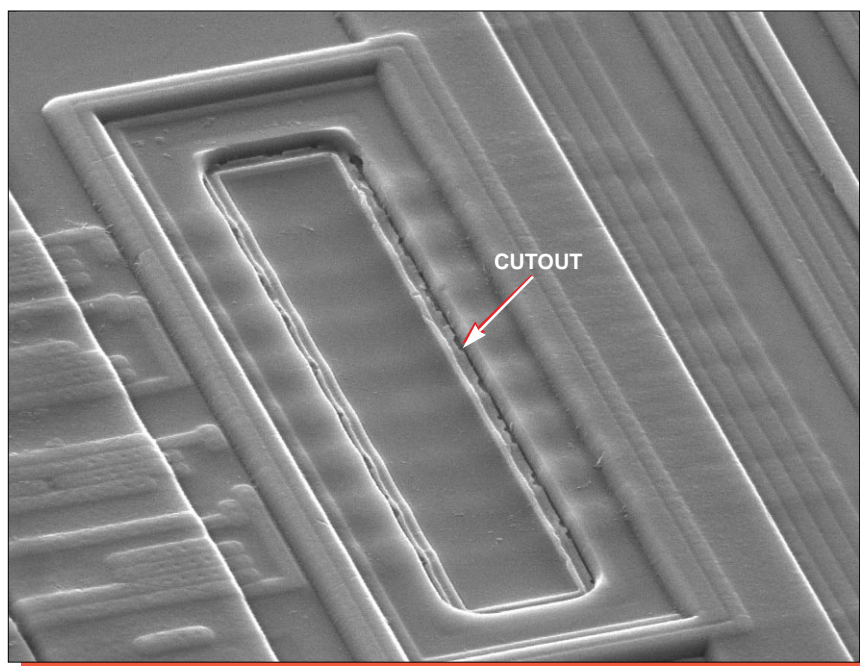


Mag. 1500x

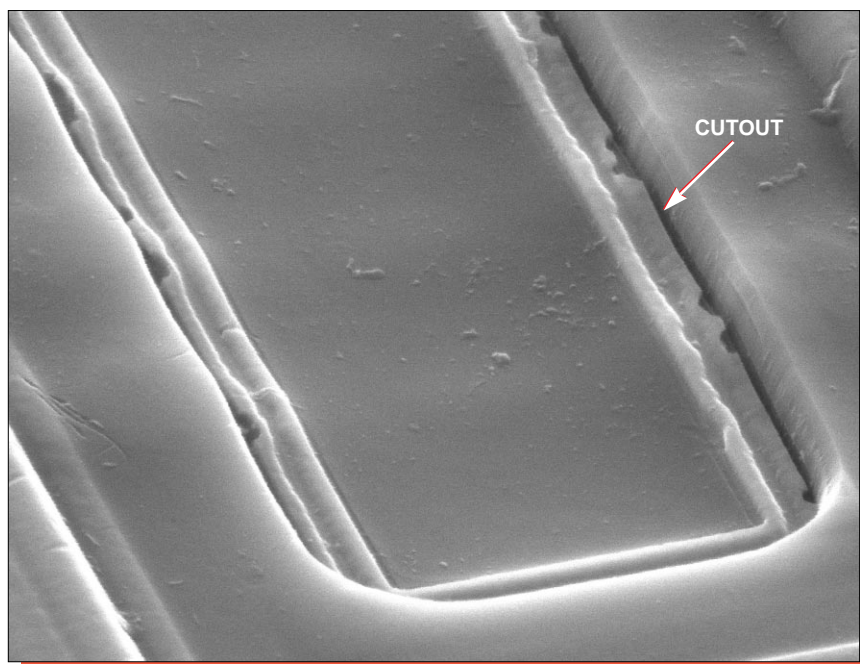


Mag. 5000x

Figure 30. Topological SEM views of poly 1 fuses. 0°.

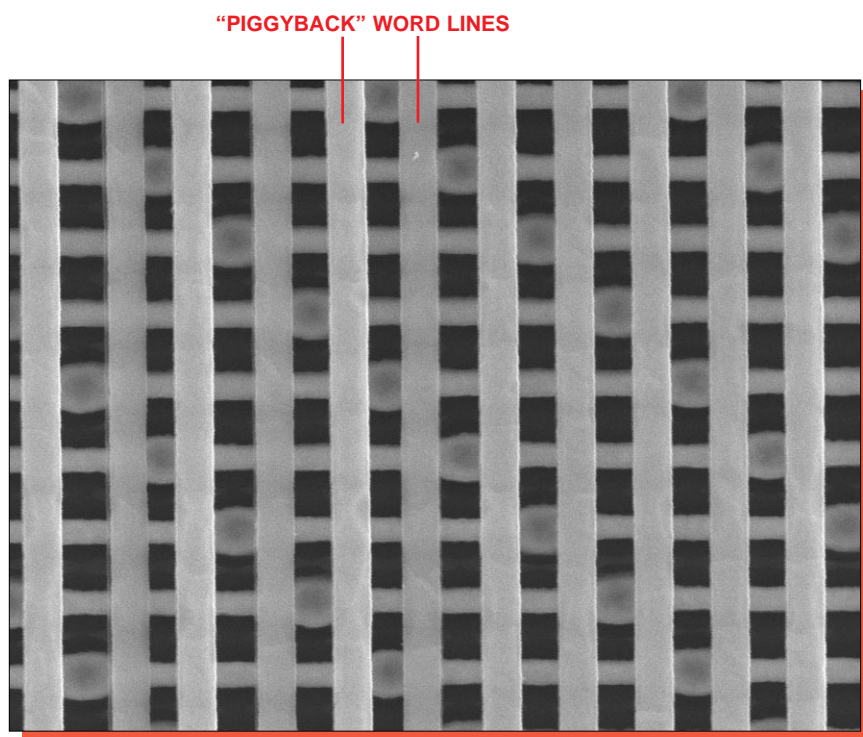


Mag. 1500x

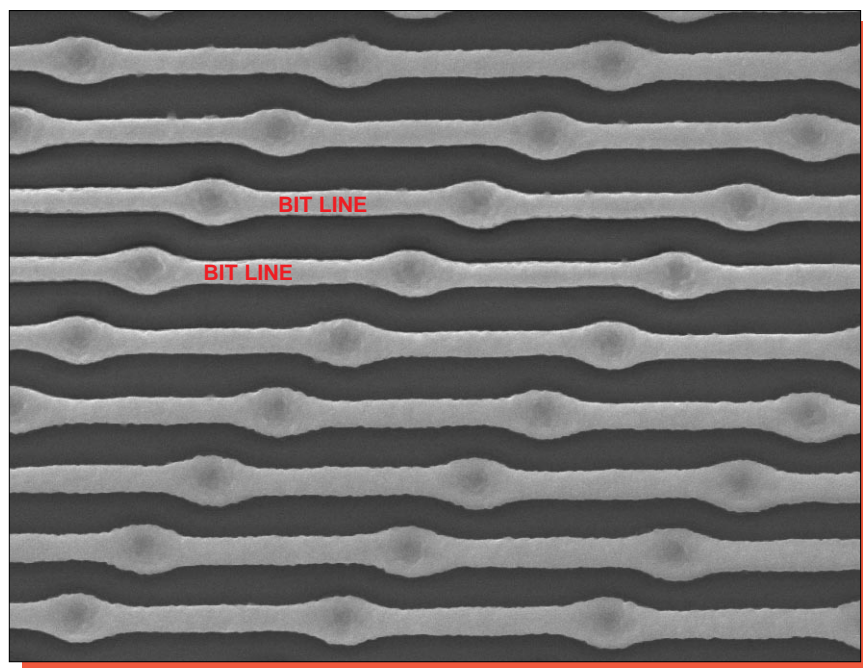


Mag. 5000x

Figure 31. Perspective SEM views of poly 1 fuses. 55°.

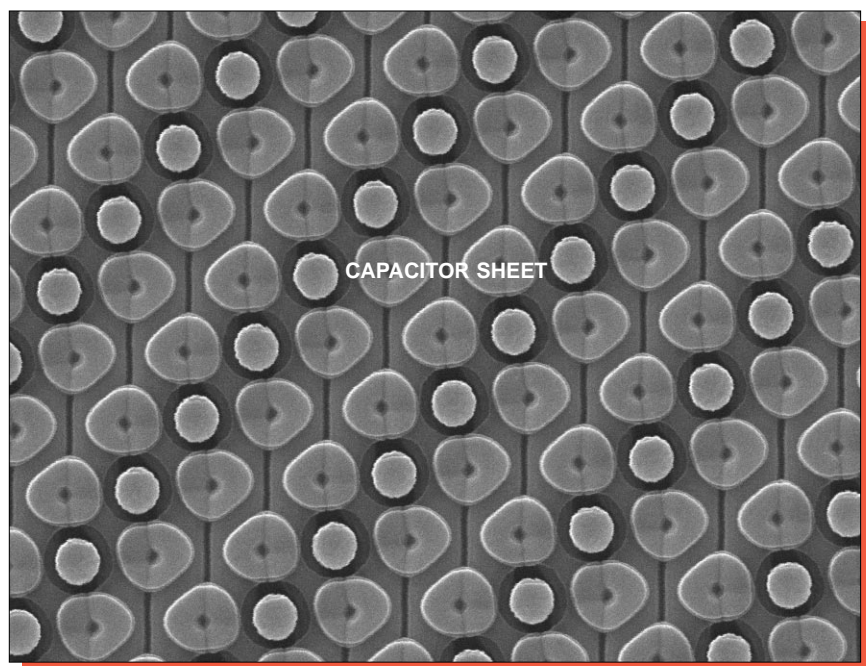


metal 2

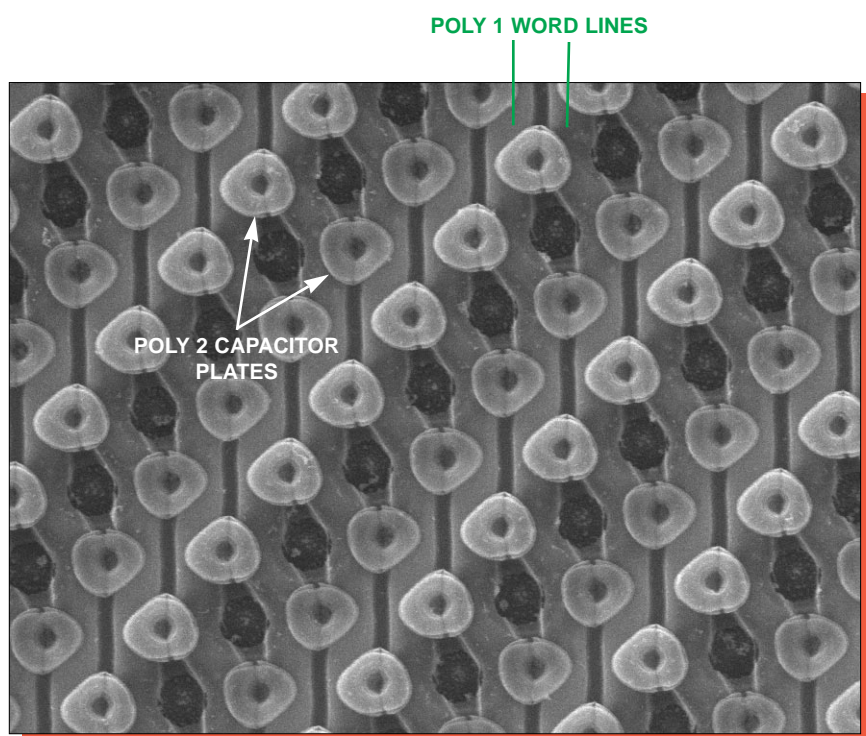


metal 1

Figure 32. Topological SEM views of the DRAM array. Mag. 10,000x, 0°.



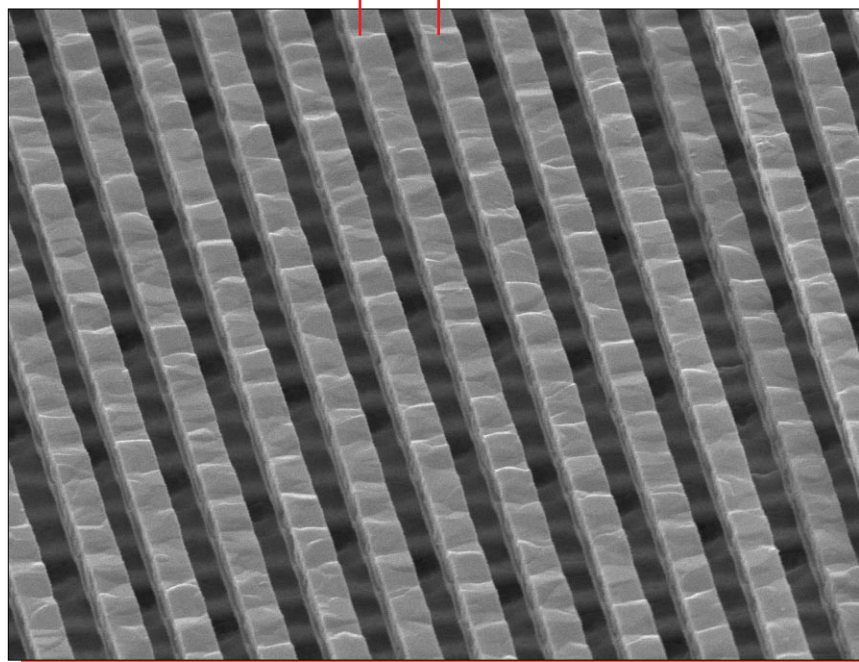
poly 3



poly 1 and 2

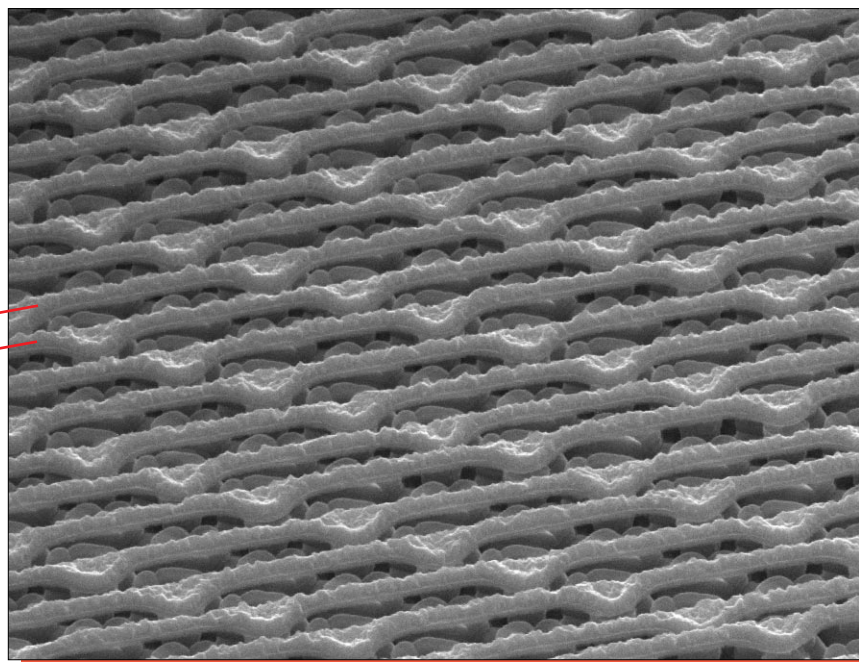
Figure 32a. Topological SEM views of the DRAM array. Mag. 10,000x, 0°.

"PIGGYBACK" WORD LINES



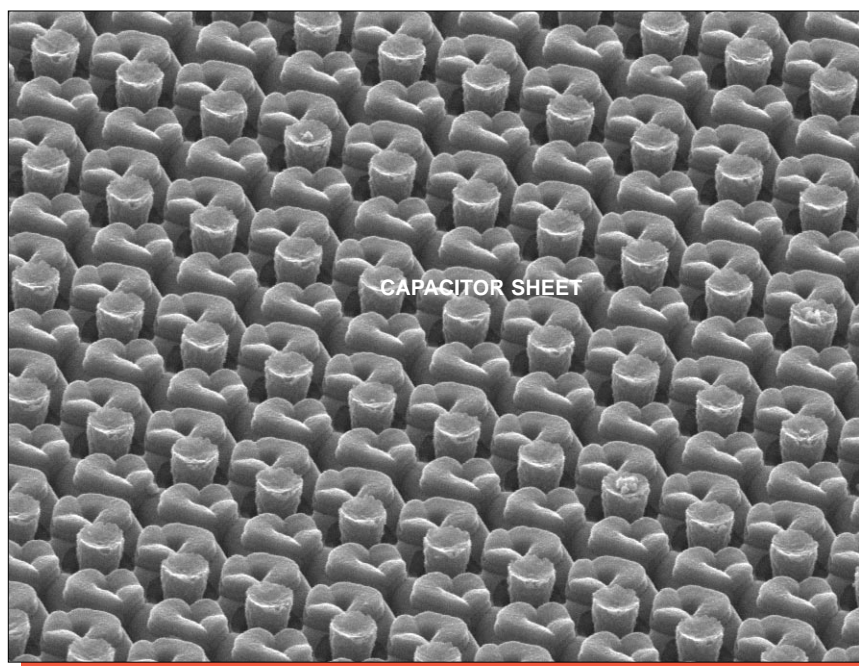
metal 2

BIT
LINES

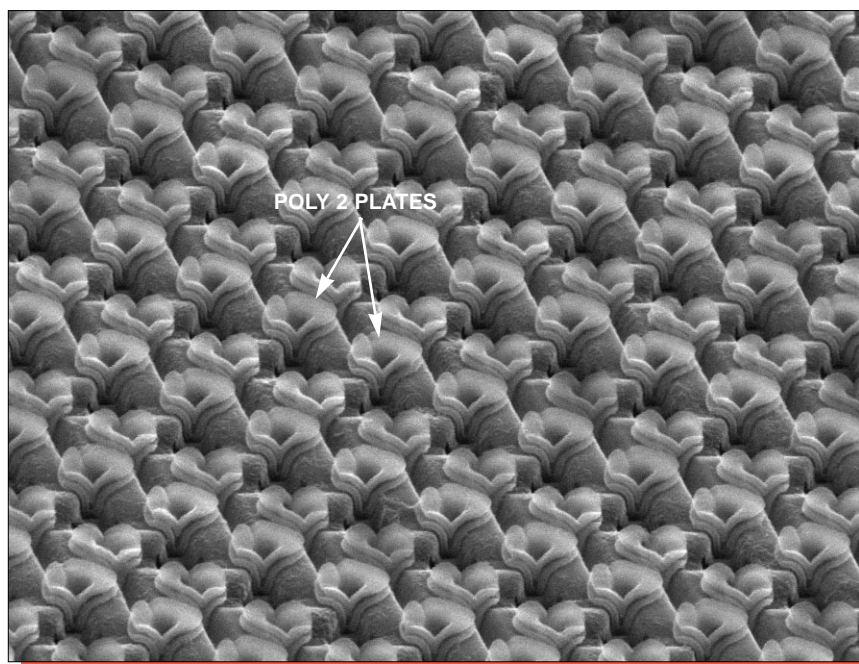


metal 1

Figure 33. Perspective SEM views of the cell array. Mag. 10,000x, 60°.

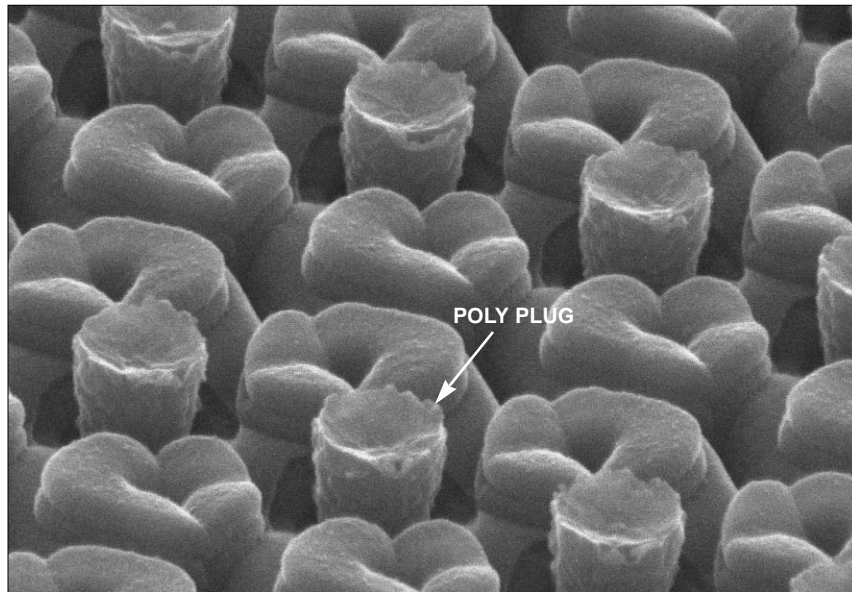


poly 3

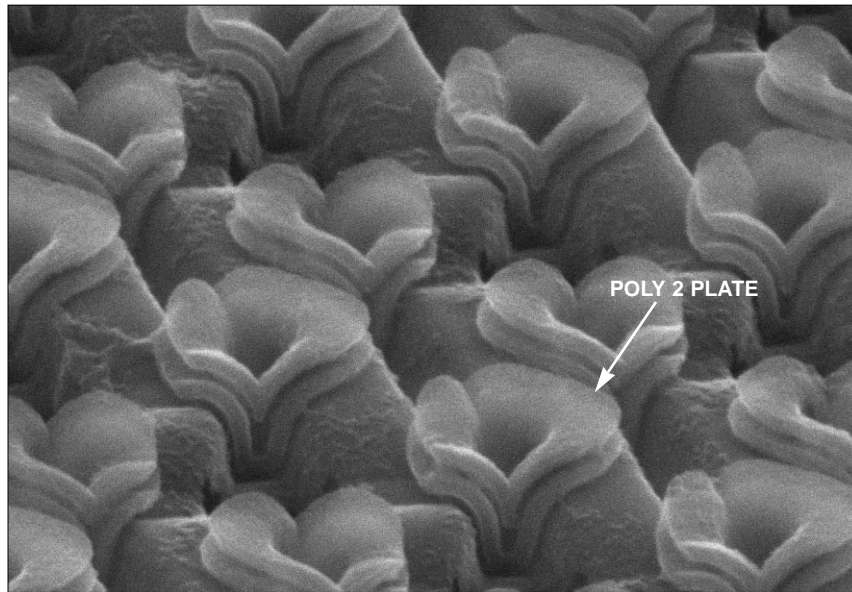


poly 1 and 2

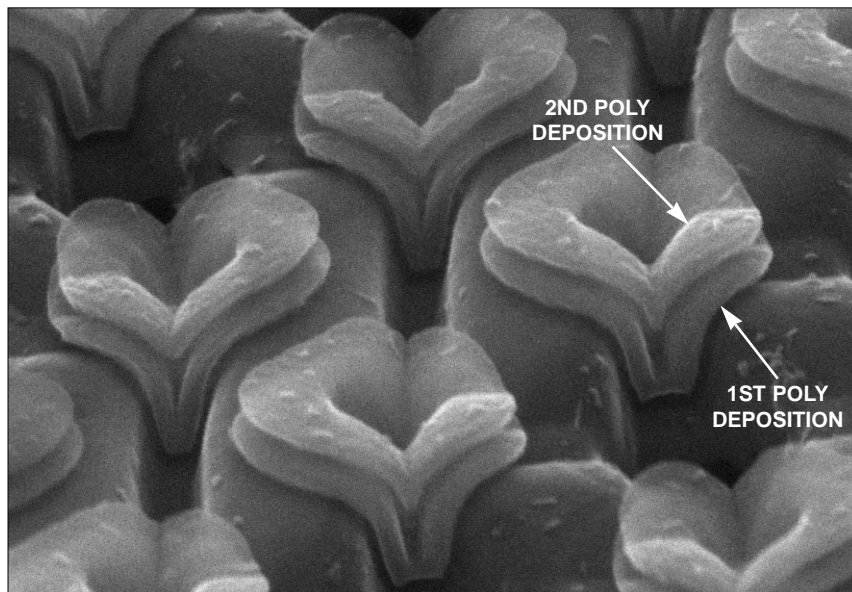
Figure 33a. Perspective SEM views of the cell array. Mag. 10,000x, 60°.



Mag. 30,000x

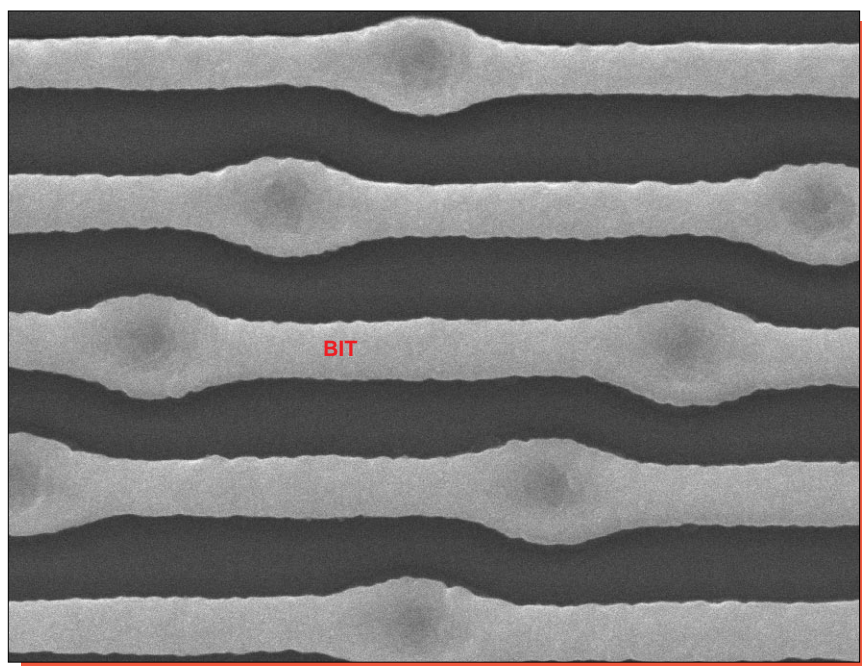


Mag. 30,000x

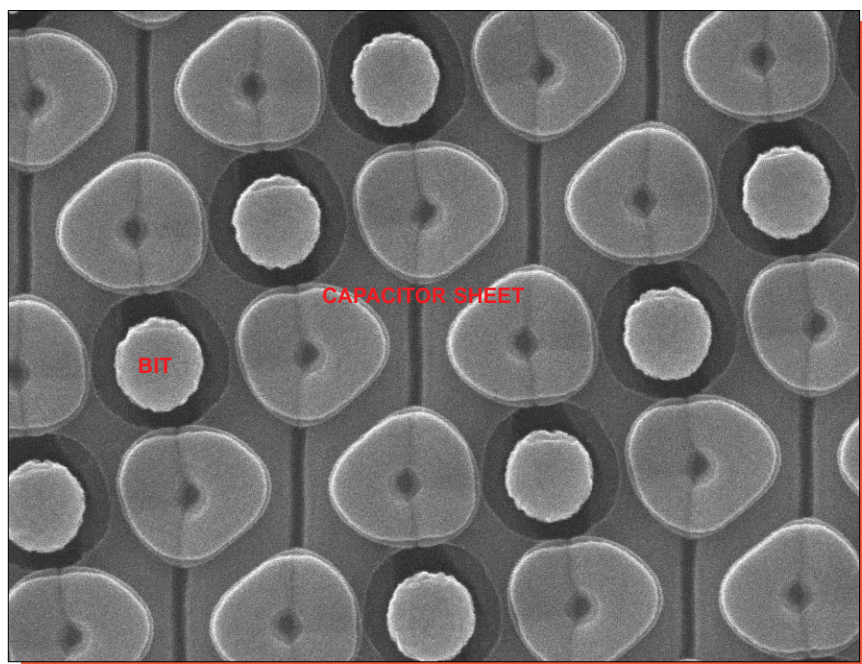


Mag. 40,000x

Figure 34. Perspective SEM details of DRAM cells. 60°.

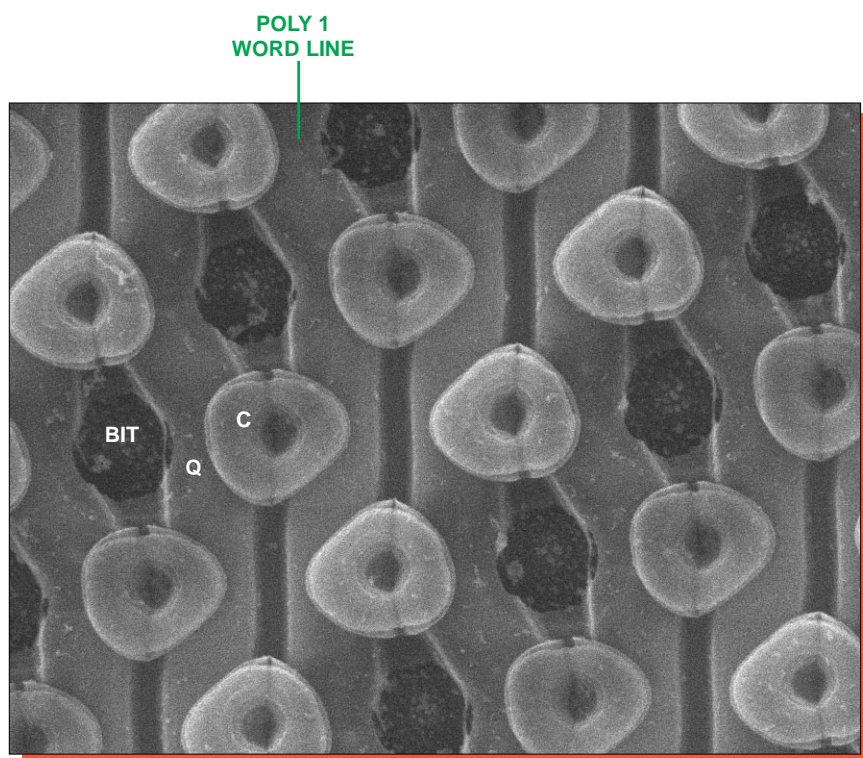


metal 1



poly 3

Figure 35. Topological SEM details of memory cells. Mag. 20,000x, 0°.



poly 1 and 2

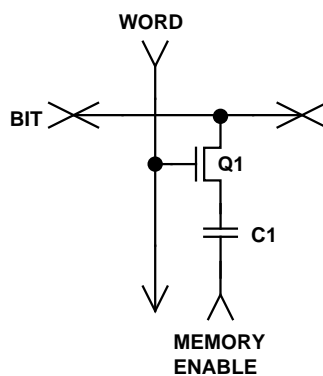
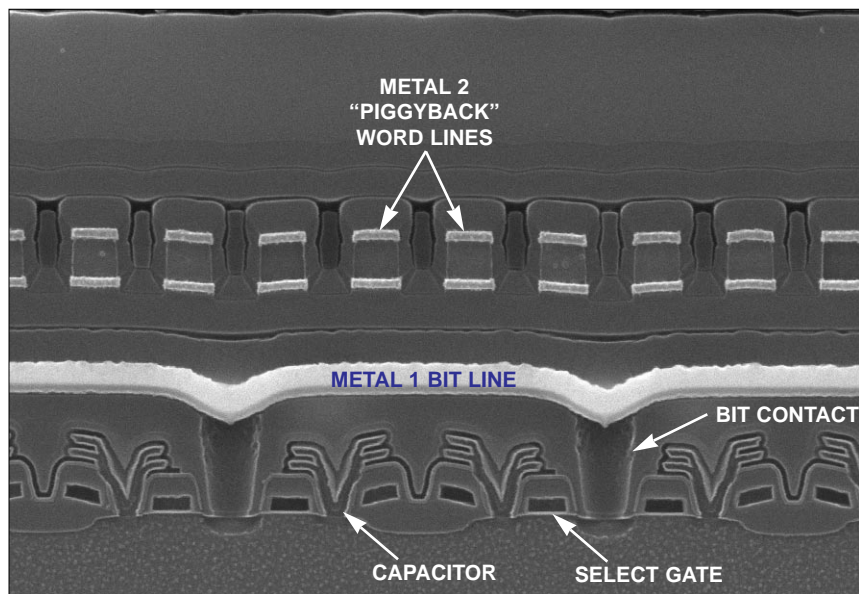
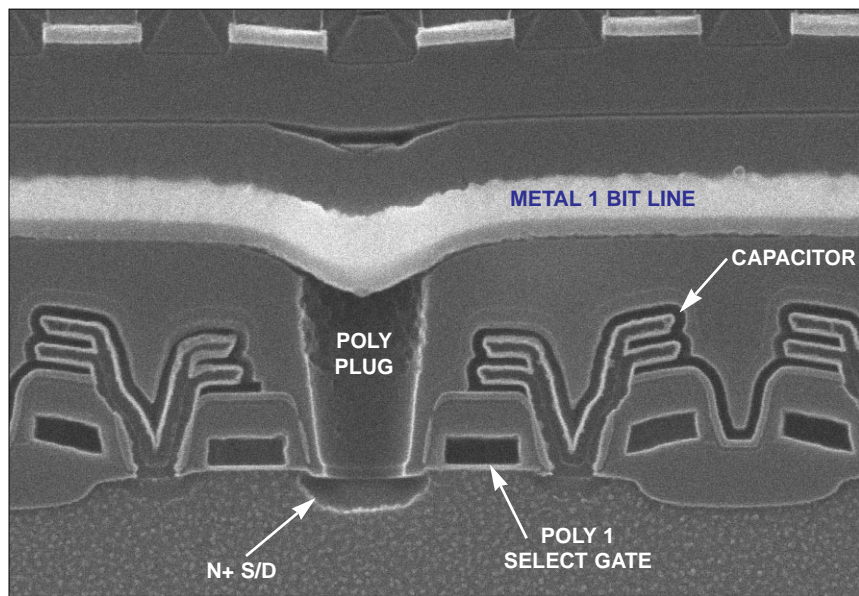


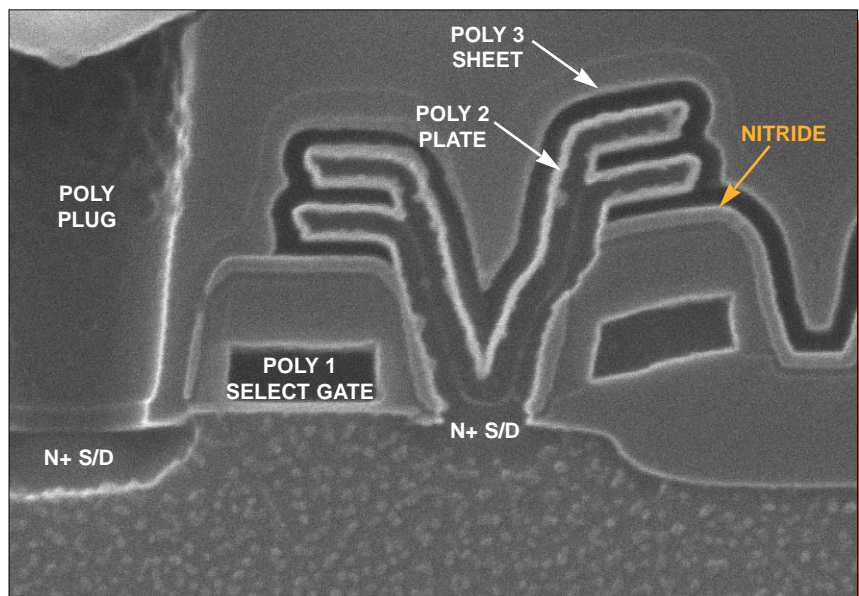
Figure 35a. Topological SEM details of memory cells with the cell schematic.
Mag. 20,000x, 0°.



Mag. 13,000x

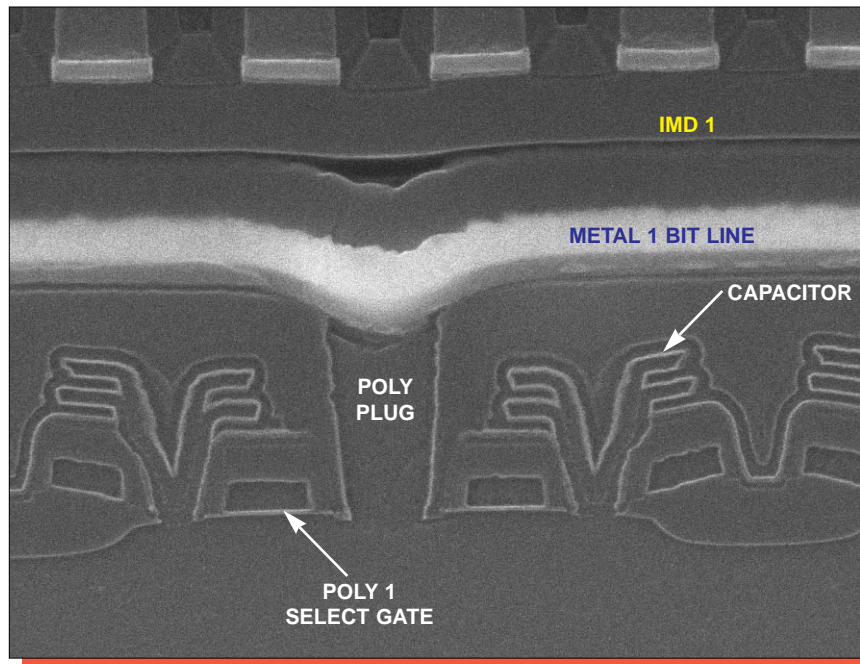


Mag. 26,000x

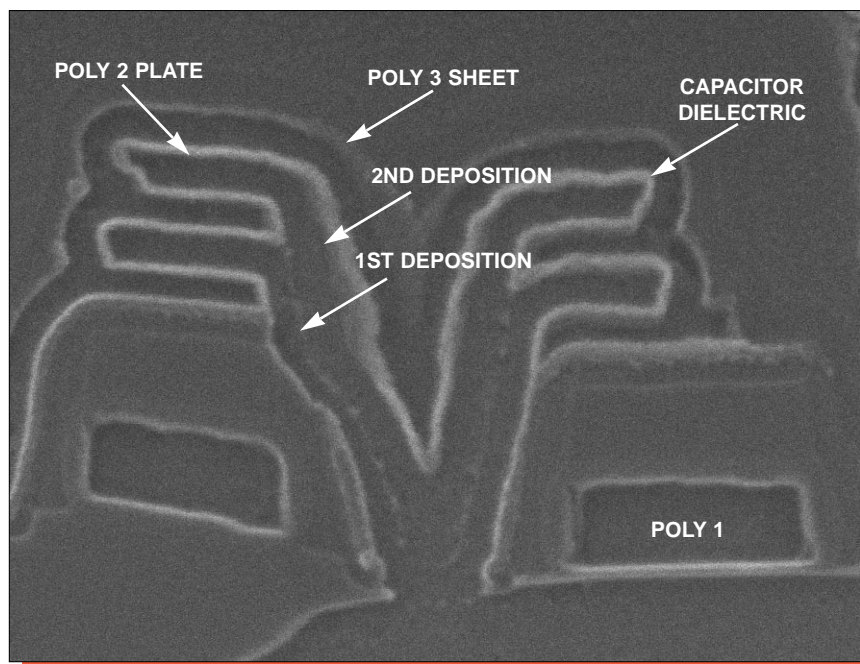


Mag. 52,000x

Figure 36. SEM section views of DRAM cells (parallel to bit lines).

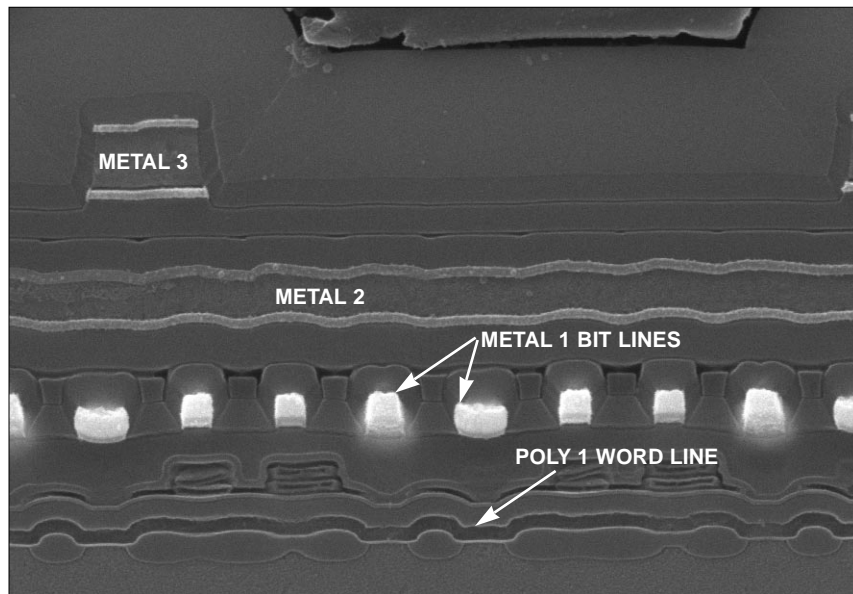


Mag. 26,000x

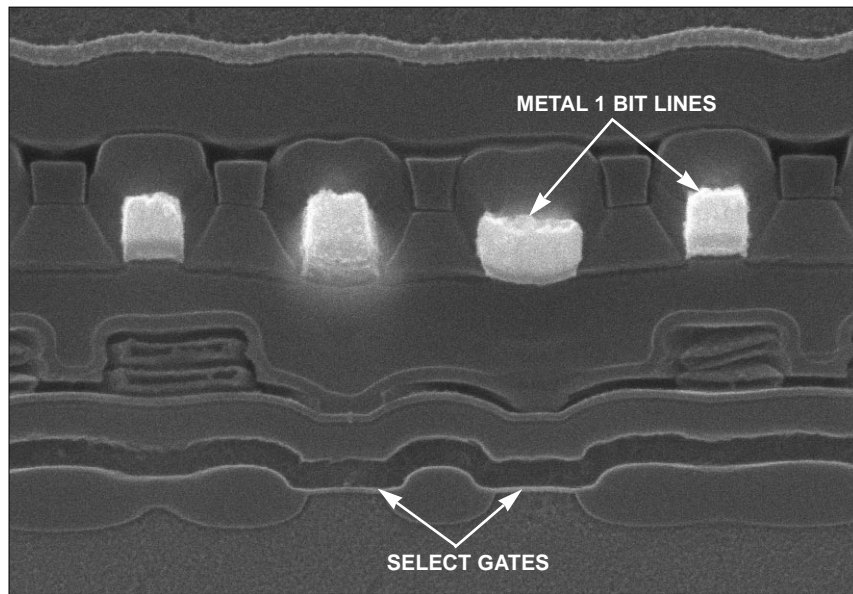


Mag. 73,500x

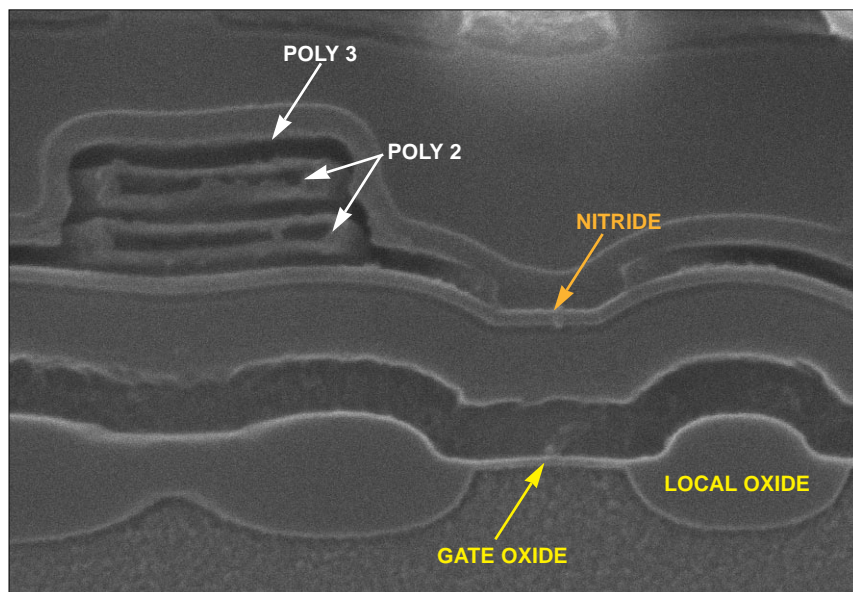
Figure 37. Plasma-etched section views of DRAM cells (parallel to bit lines).



Mag. 13,000x

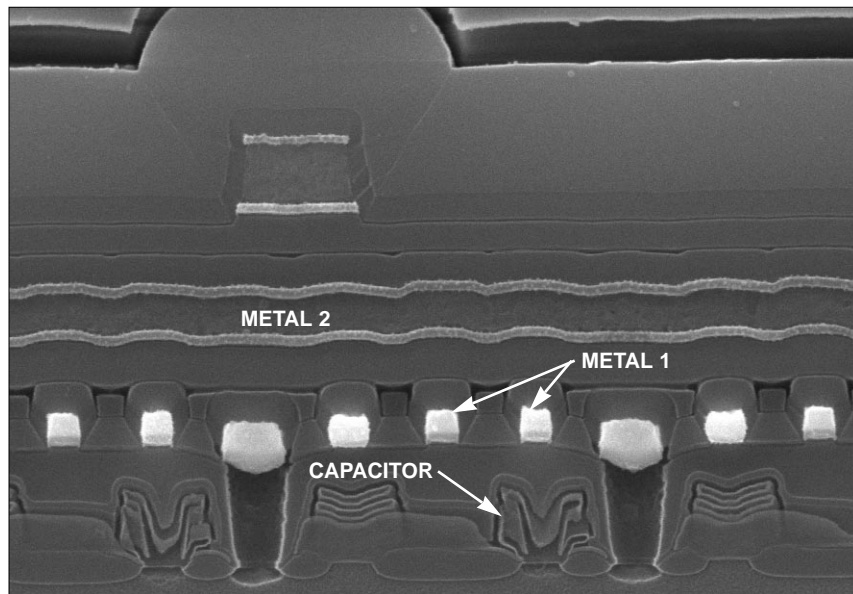


Mag. 26,000x

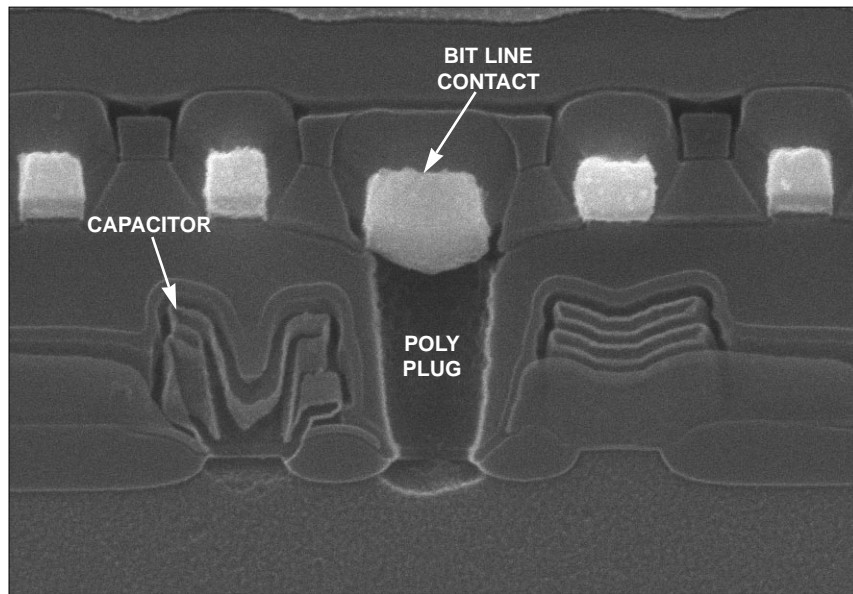


Mag. 52,000x

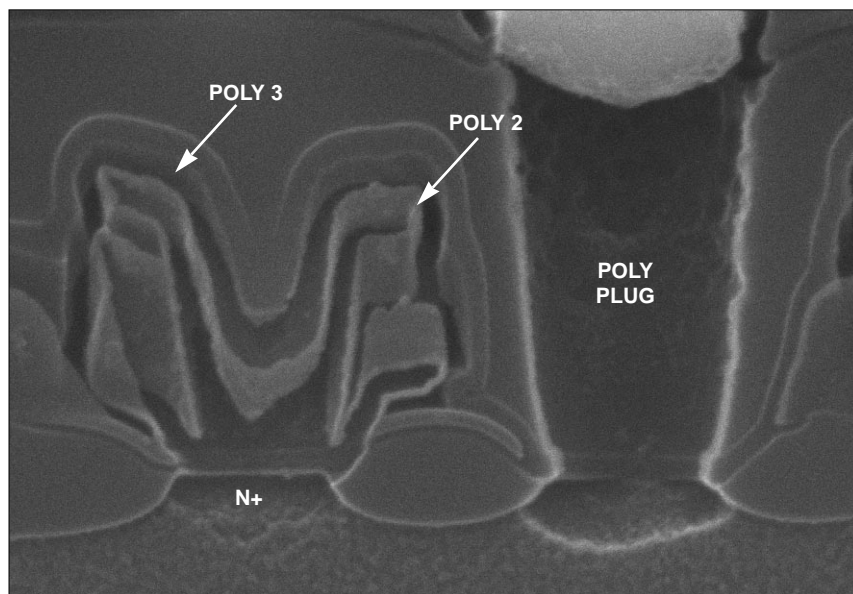
Figure 38. SEM section views of DRAM cells (parallel to word line).



Mag. 13,000x



Mag. 26,000x



Mag. 52,000x

Figure 39. SEM section views of DRAM cells (parallel to word lines).

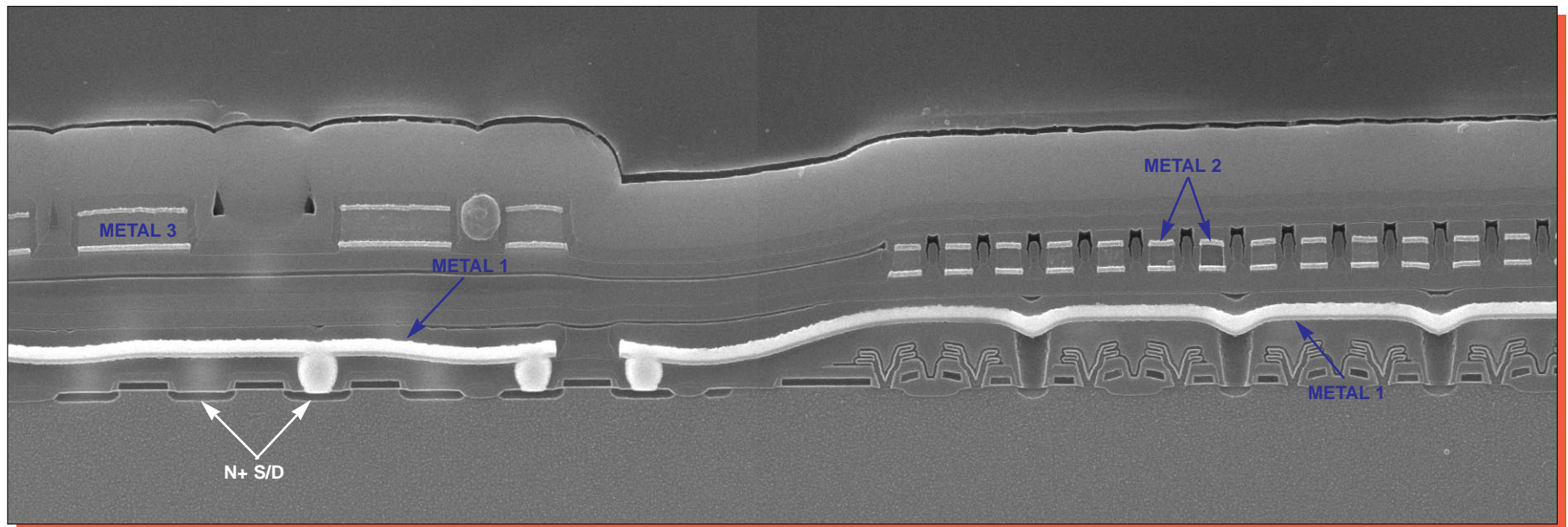


Figure 40. SEM section view of the cell array transition. Mag. 8000x.

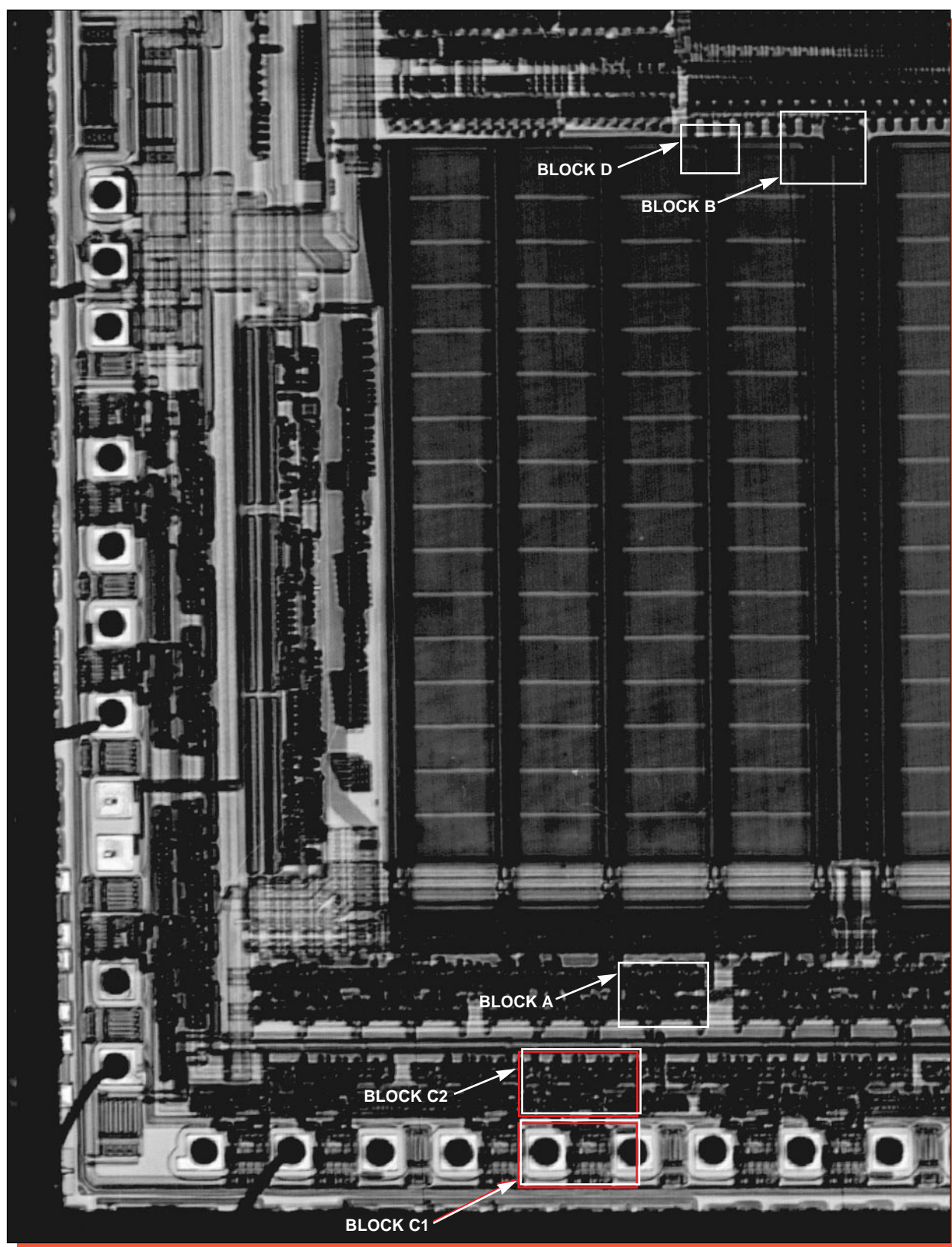


Figure 41. Portion of the die illustrating location of circuit blocks. Mag. 60x.

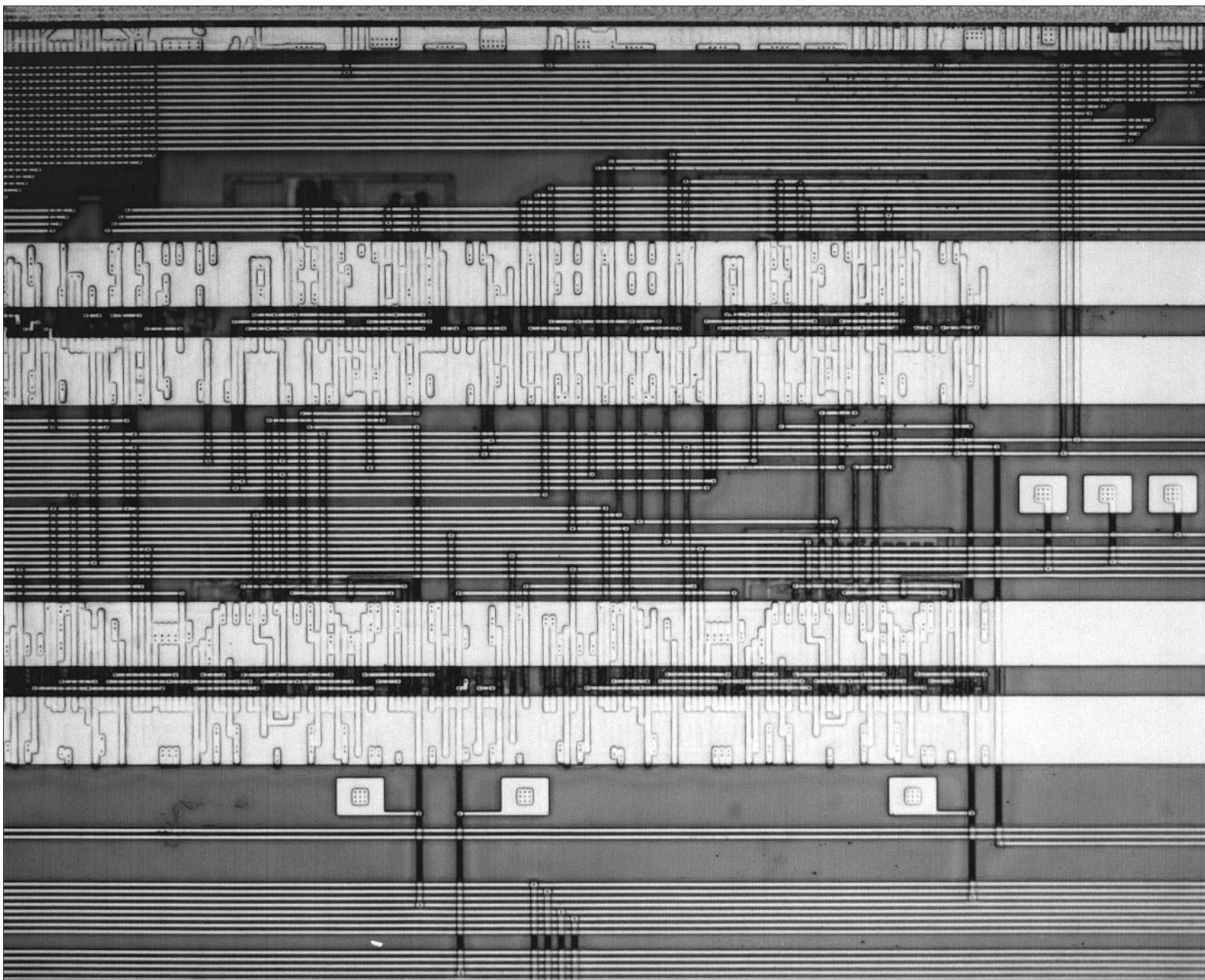


Figure 42. Optical view of Circuit Block A (metal 3). Mag. 640x.

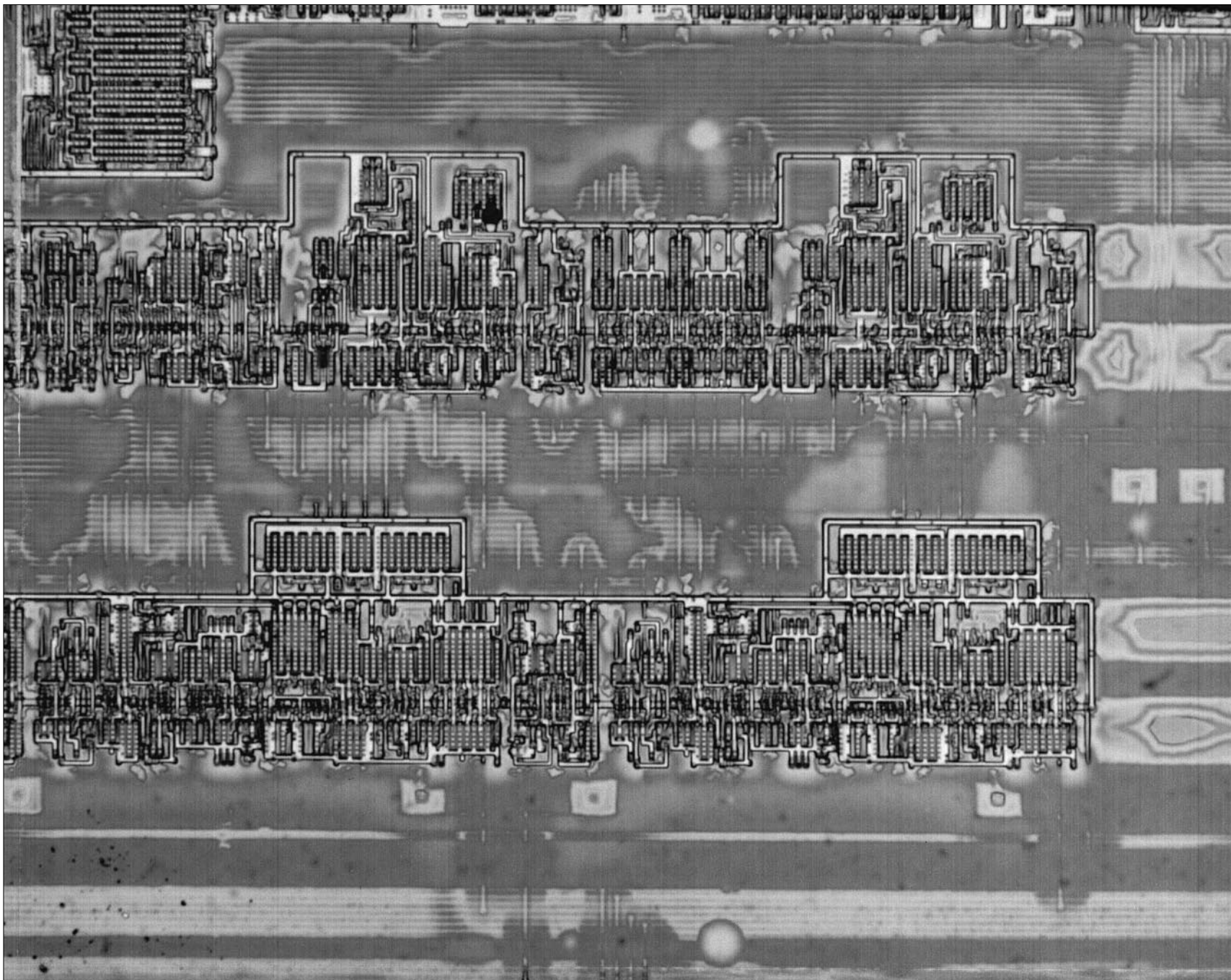


Figure 42a. Optical view of Circuit Block A (metal 1). Mag. 640x.

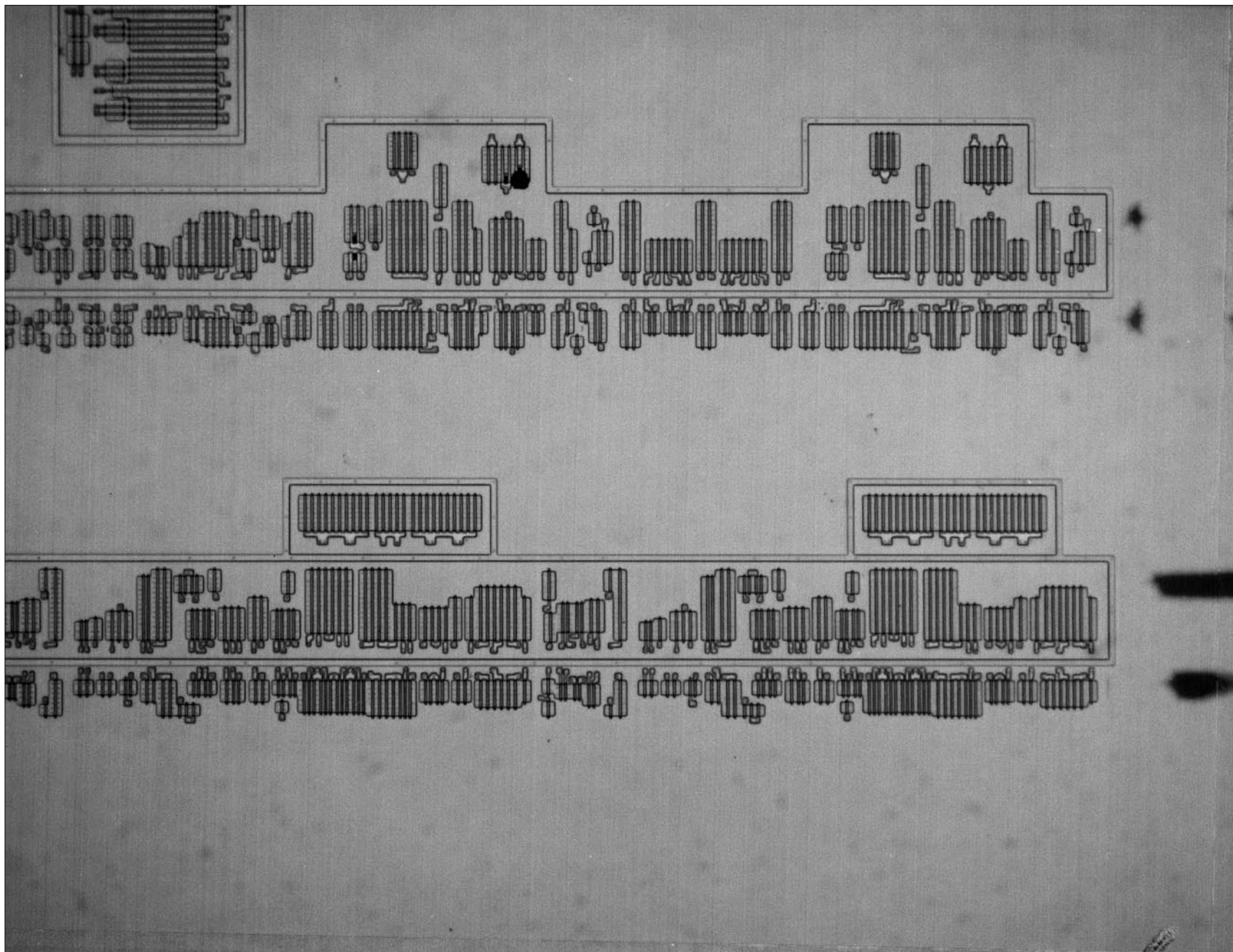


Figure 42b. Optical view of Circuit Block A (unlayered). Mag. 640x.

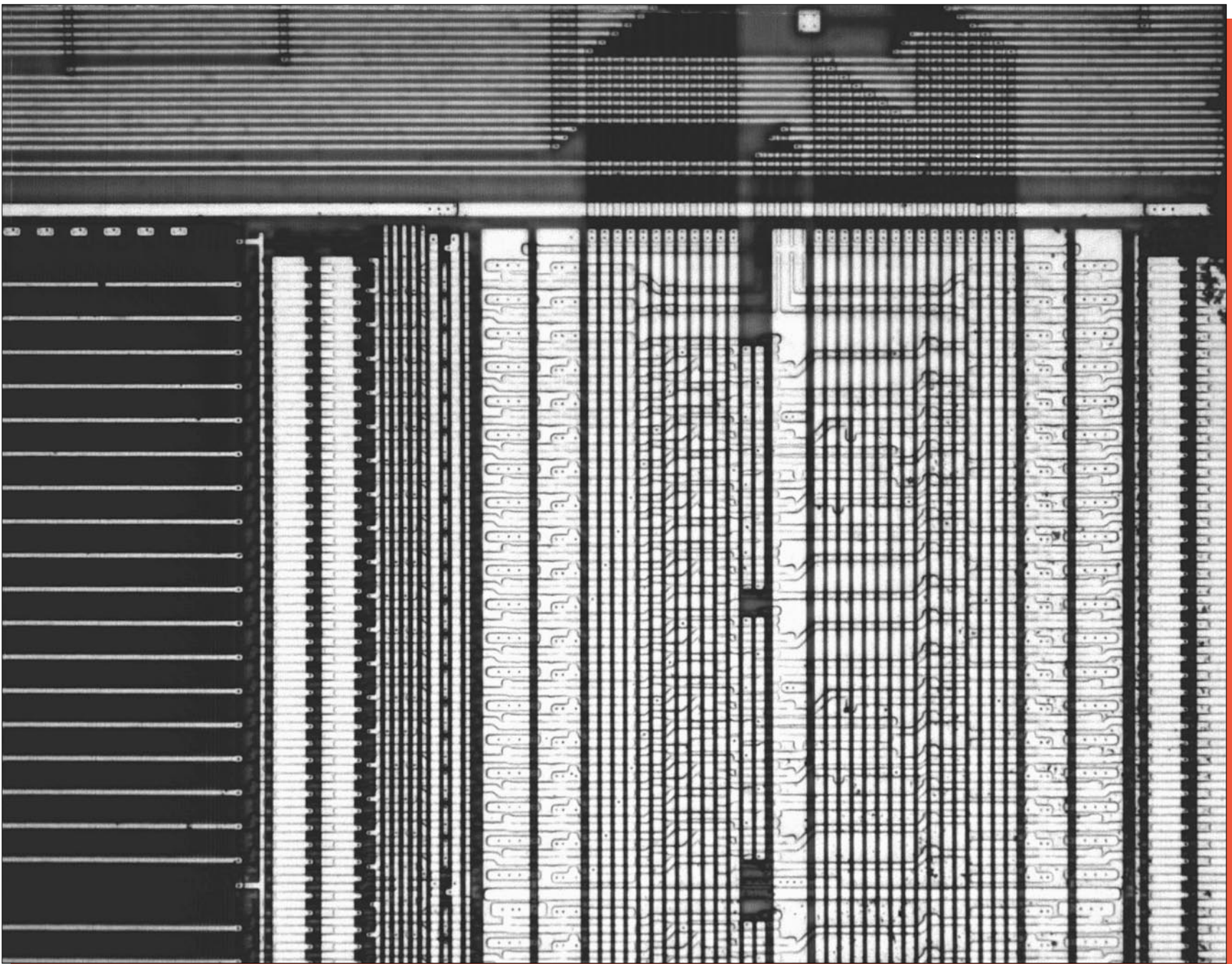


Figure 43. Optical view of Circuit Block B (metal 3). Mag. 800x.

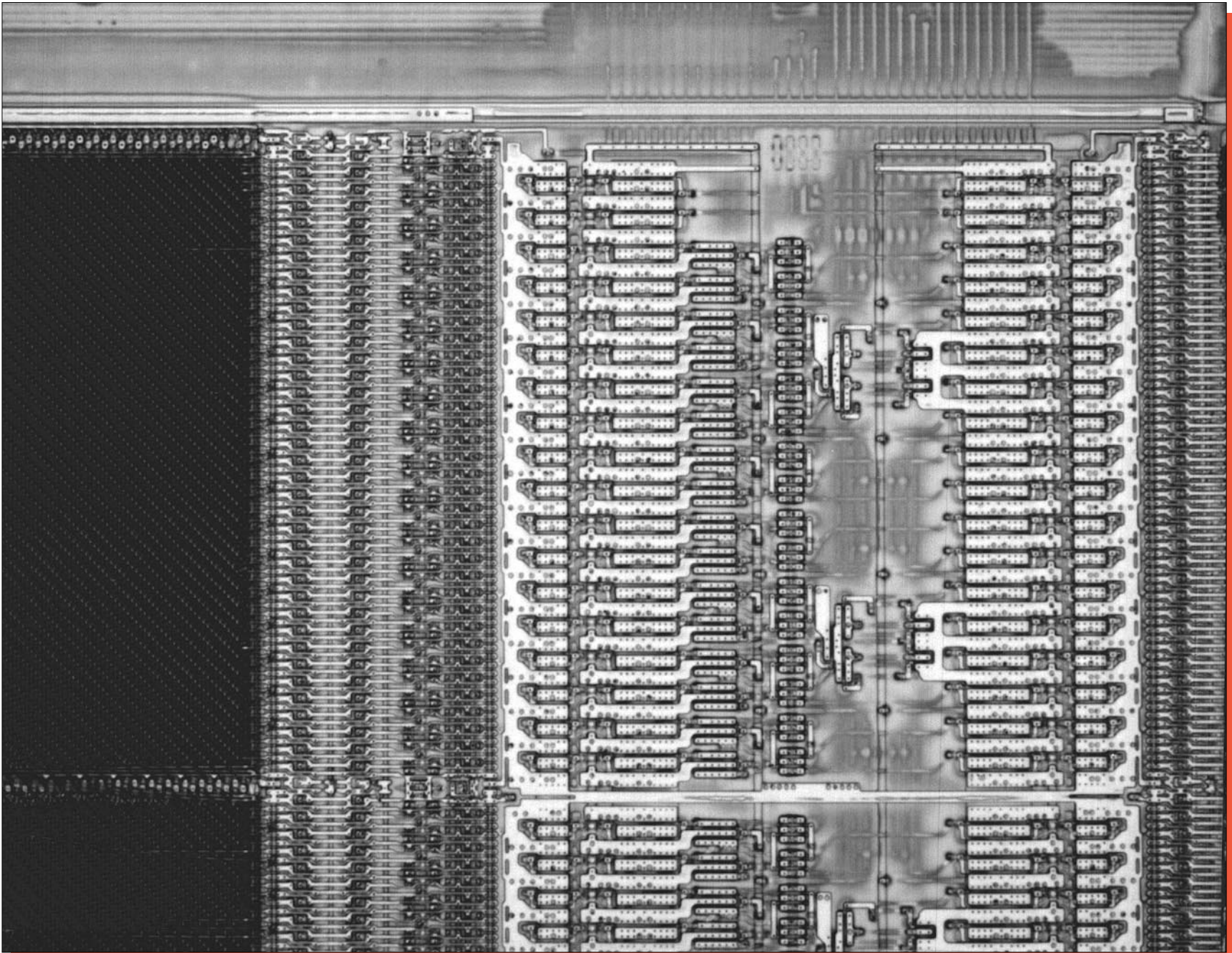


Figure 43a. Optical view of Circuit Block B (metal 1). Mag. 800x.

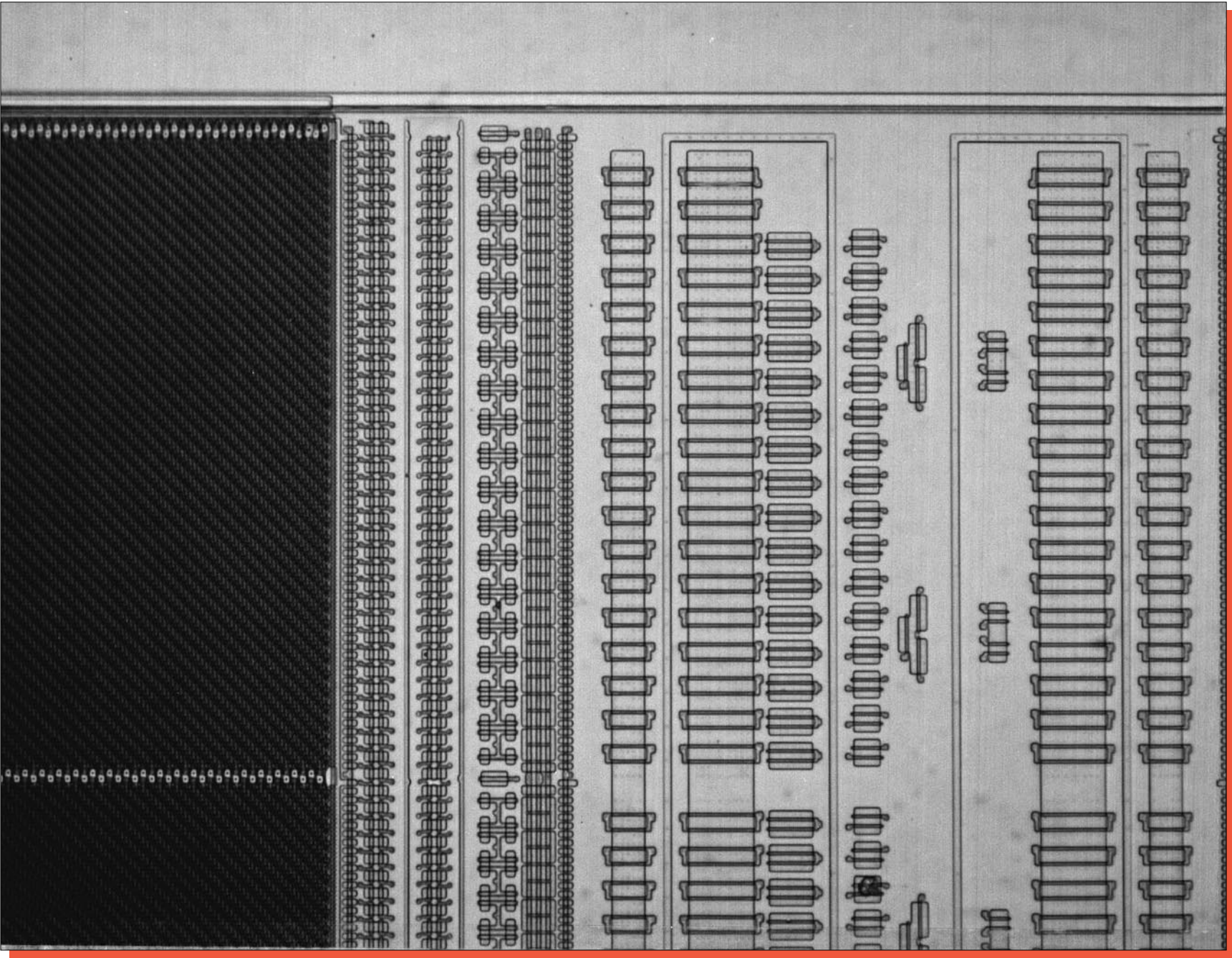


Figure 43b. Optical view of Circuit Block B (unlayered). Mag. 800x.

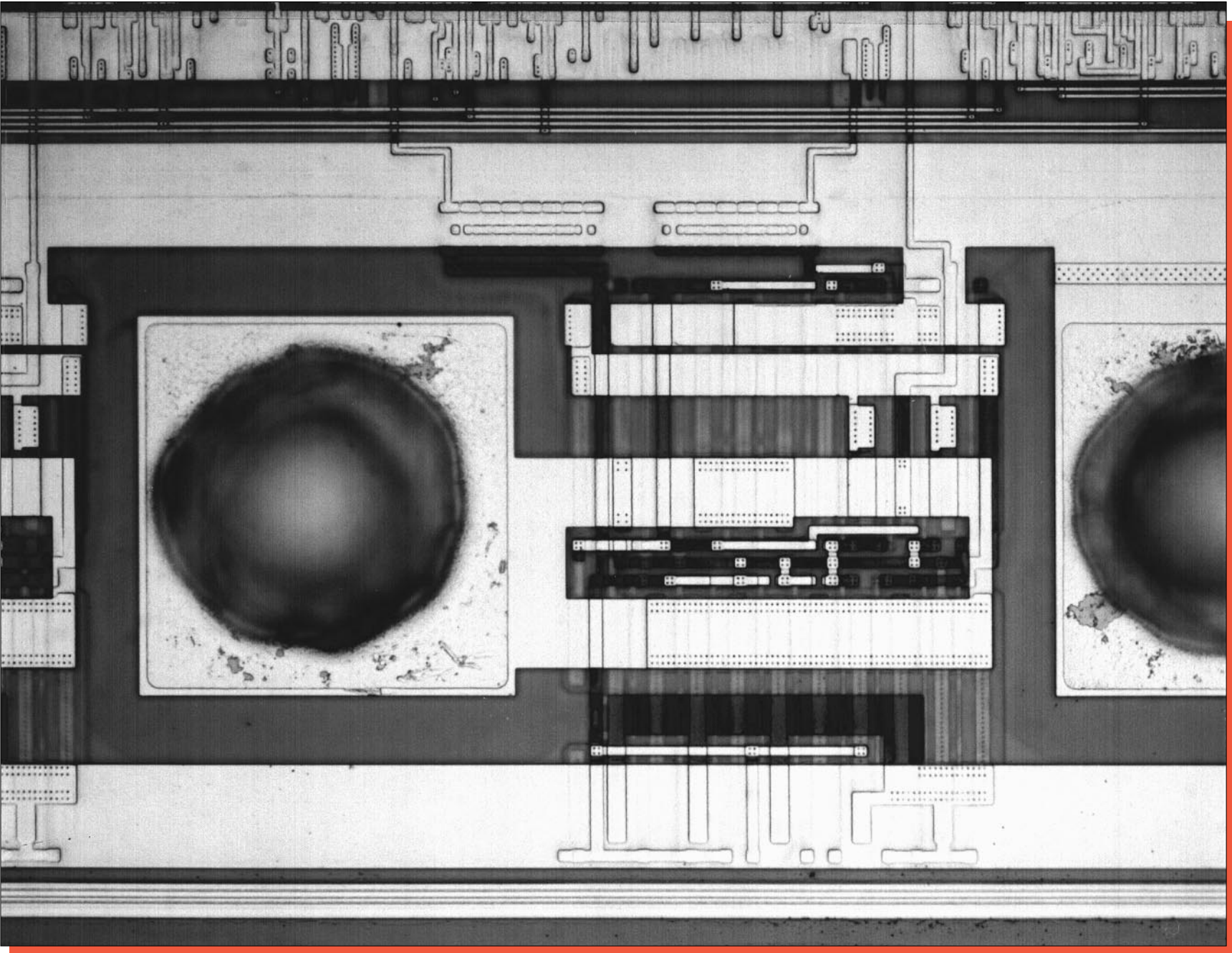


Figure 44. Optical view of Circuit Block C1 (metal 3). Mag. 640x.

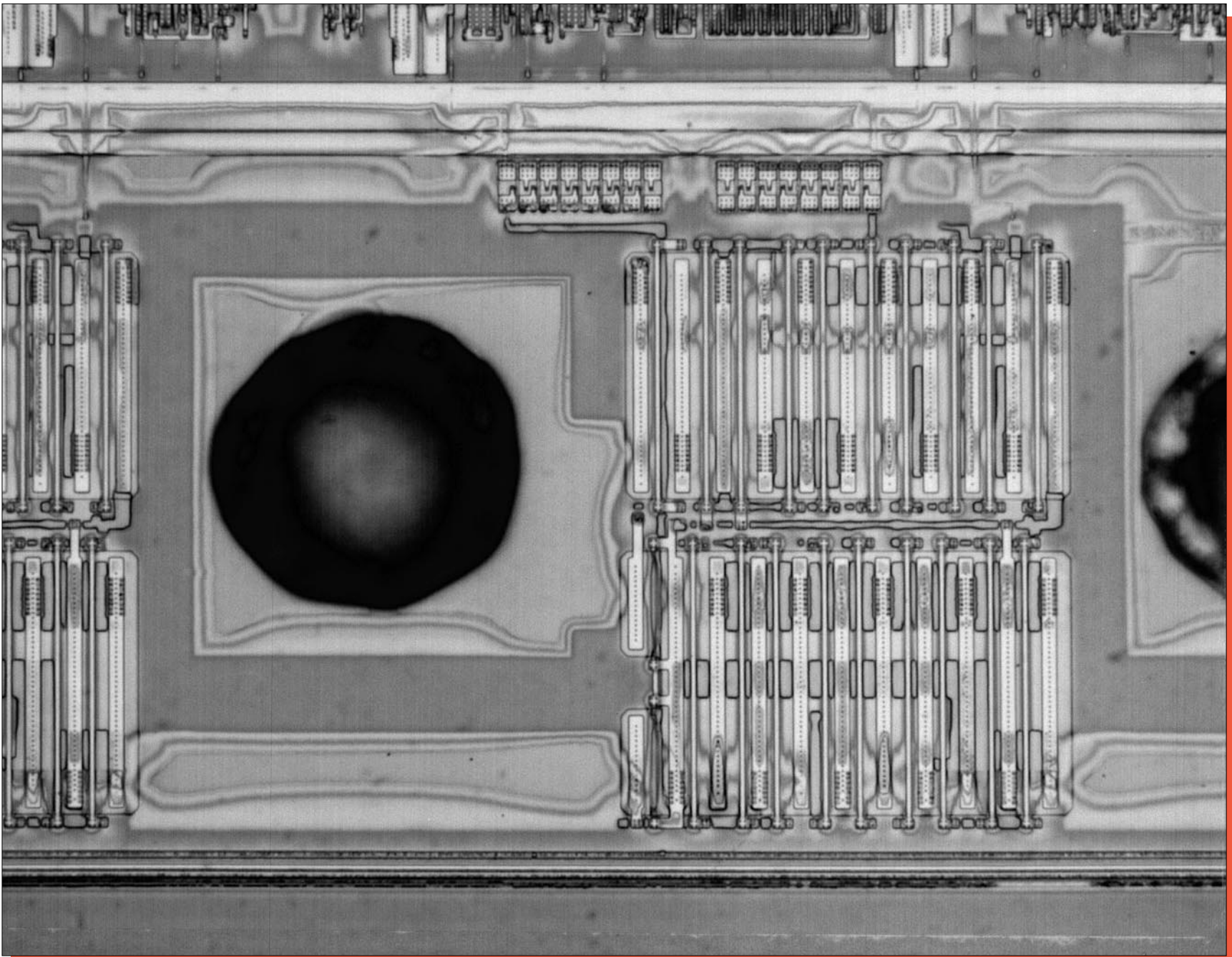


Figure 44a. Optical view of Circuit Block C1 (metal 1). Mag. 640x.

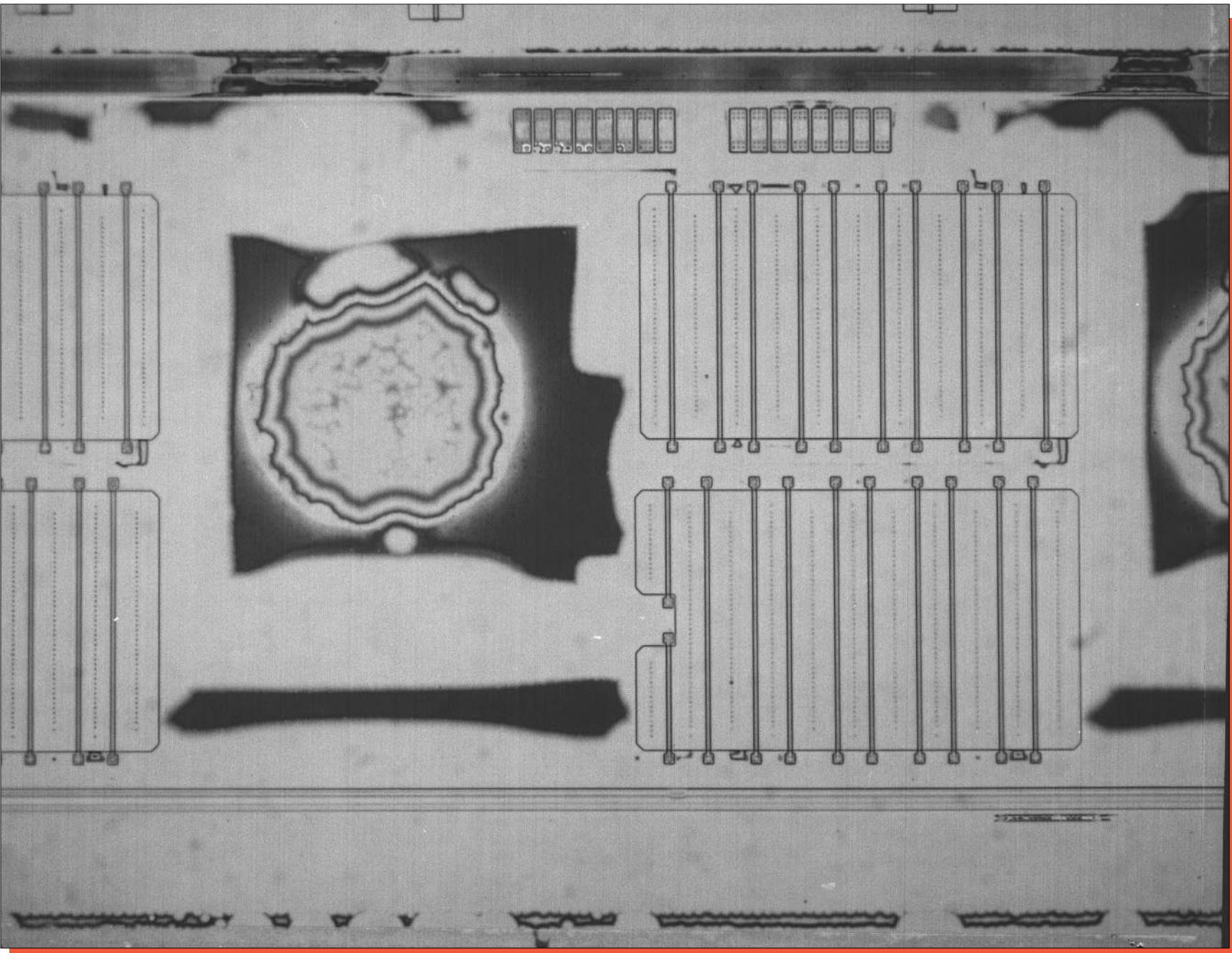


Figure 44b. Optical view of Circuit Block C1 (unlayered). Mag. 640x.

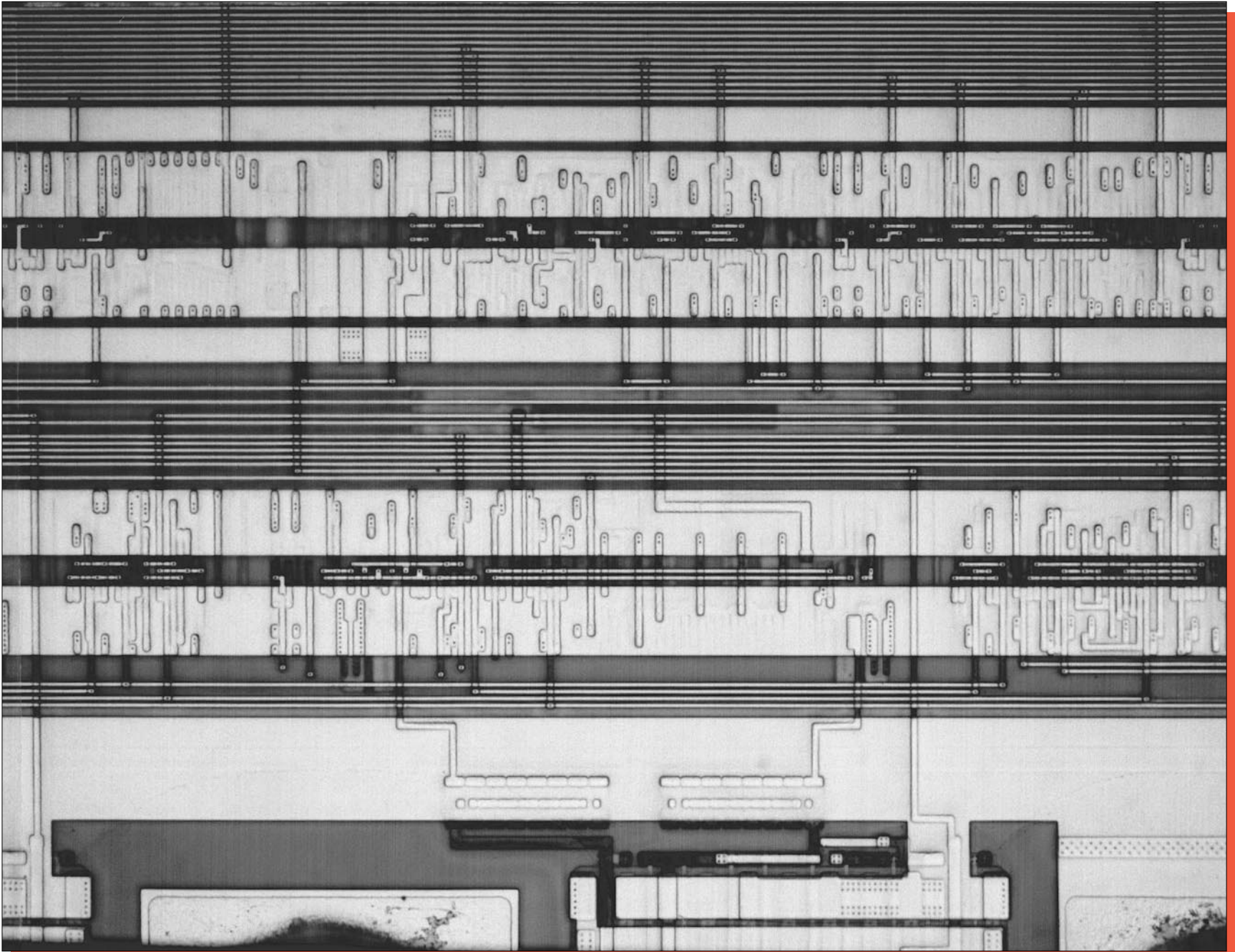


Figure 45. Optical view of Circuit Block C2 (metal 3). Mag. 640x.

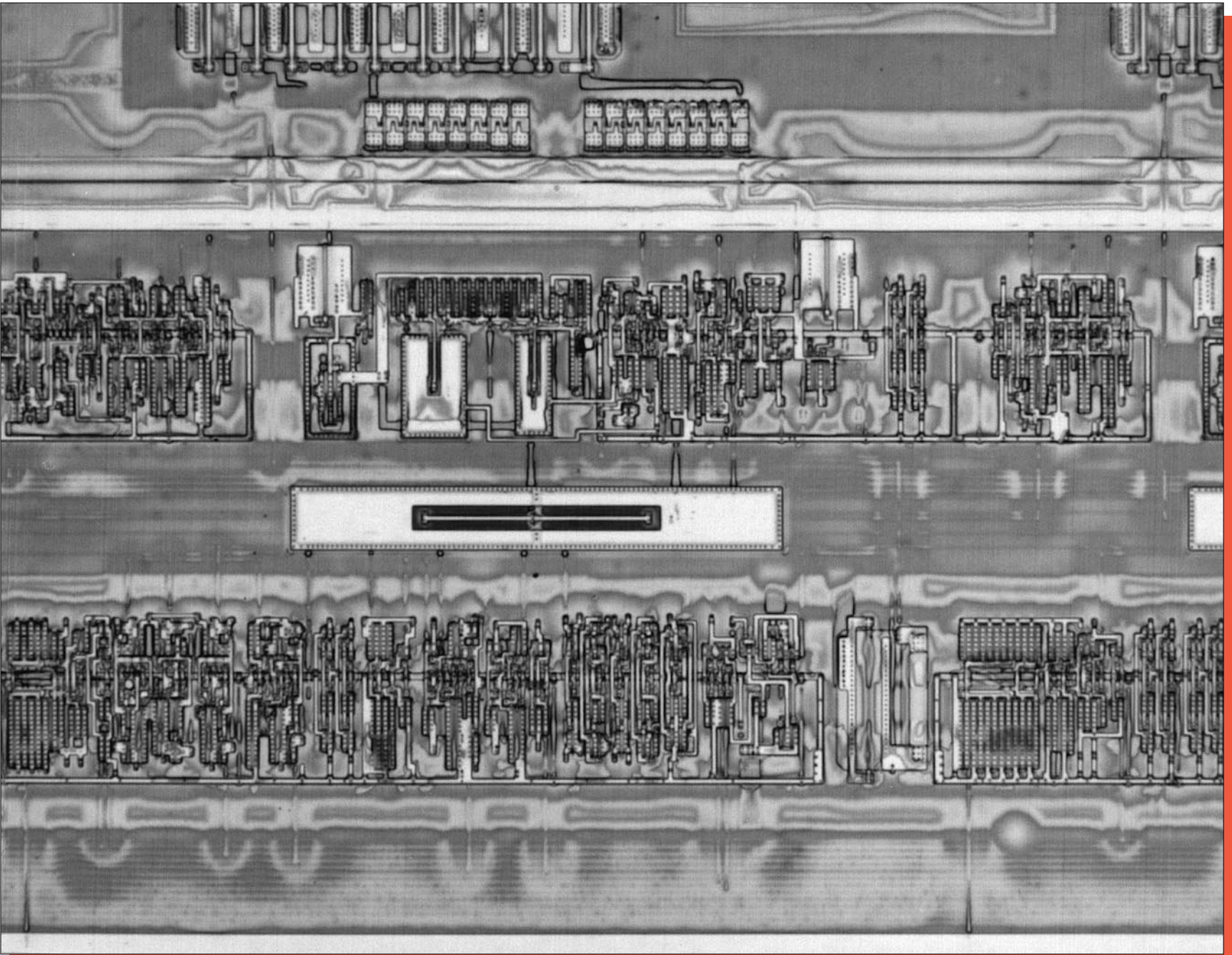


Figure 45a. Optical view of Circuit Block C2 (metal 1). Mag. 640x.

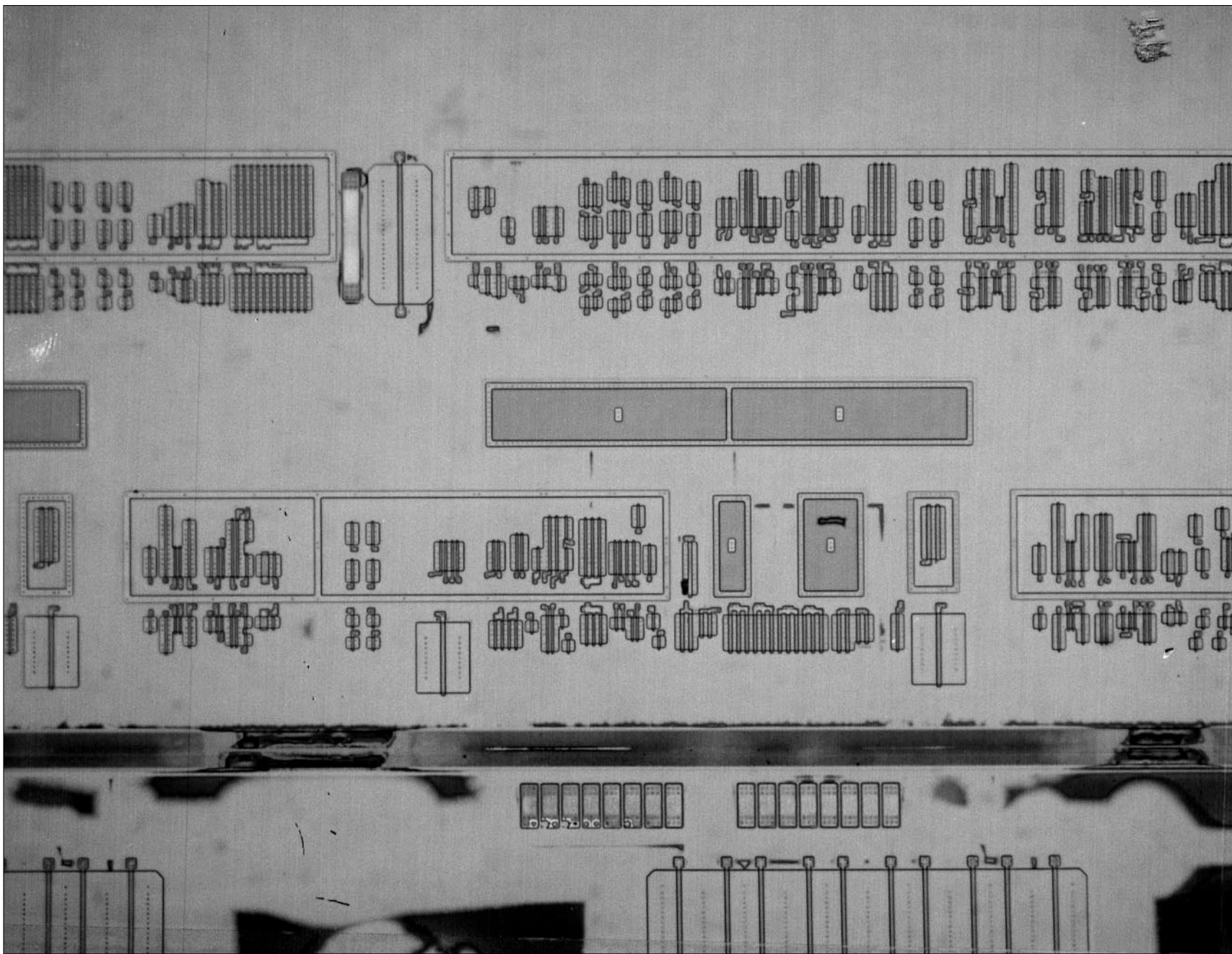


Figure 45b. Optical view of Circuit Block C2 (unlayered). Mag. 640x.

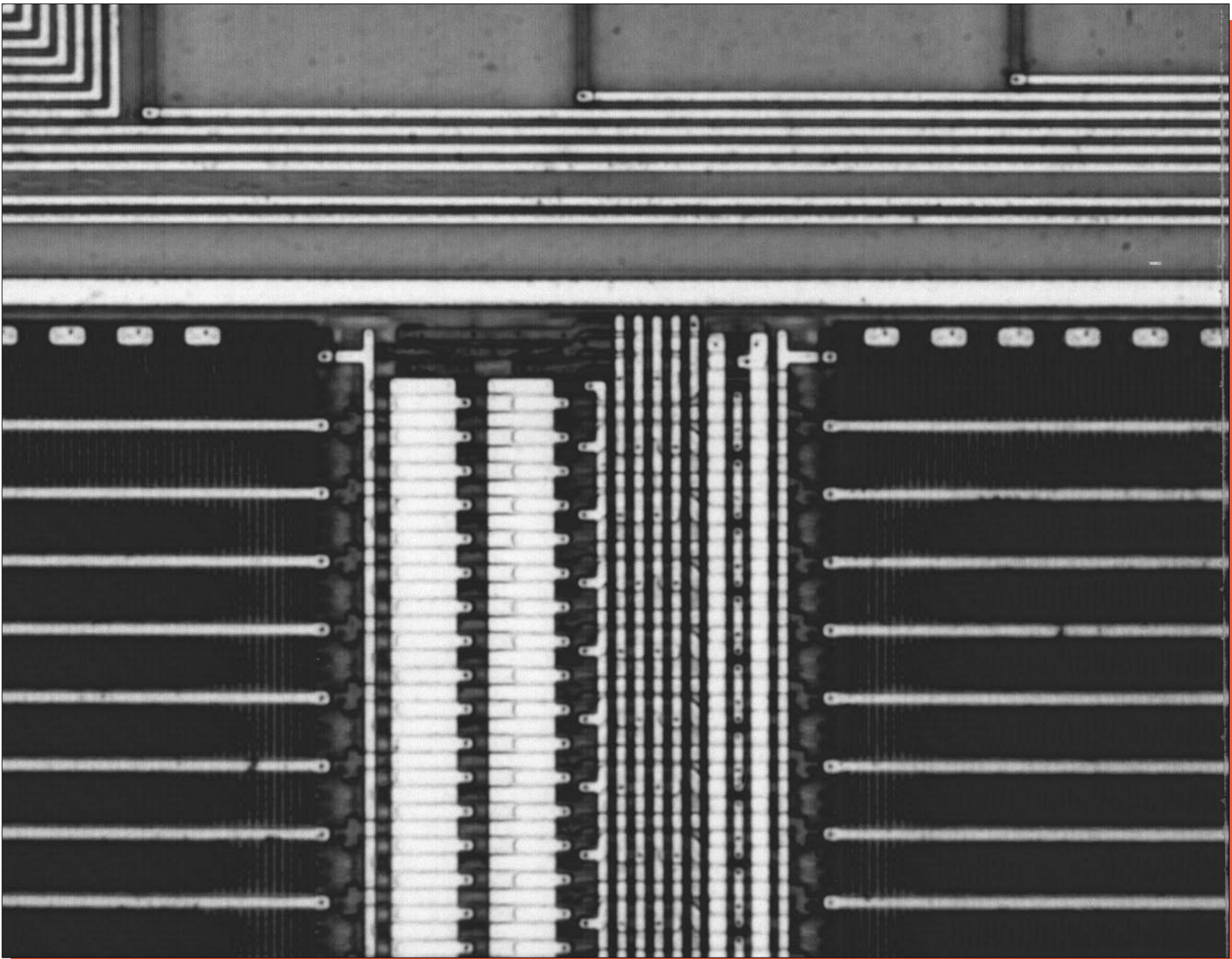


Figure 46. Optical view of Circuit Block D (metal 3). Mag. 1600x.

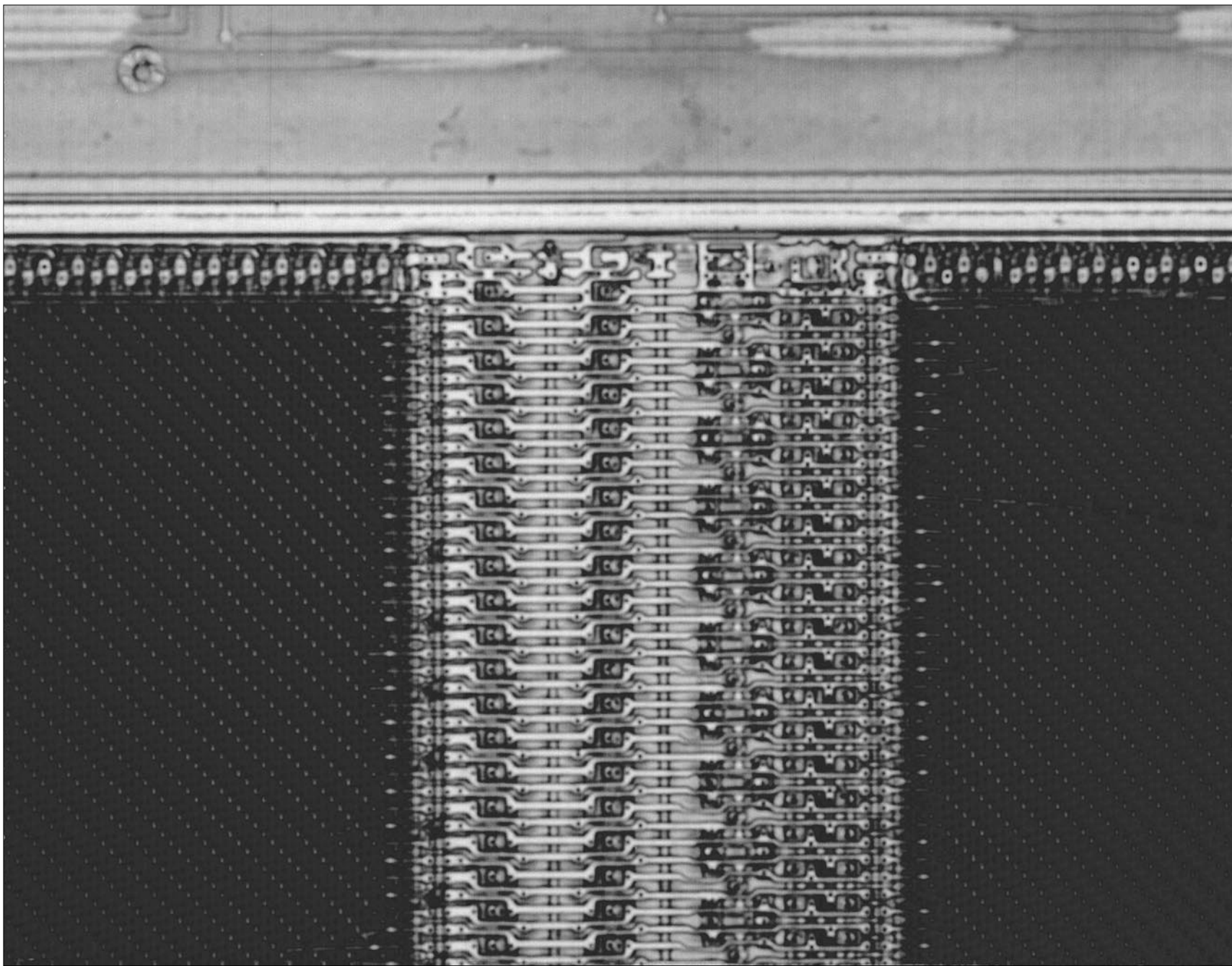


Figure 46a. Optical view of Circuit Block D (metal 1). Mag. 1600x.

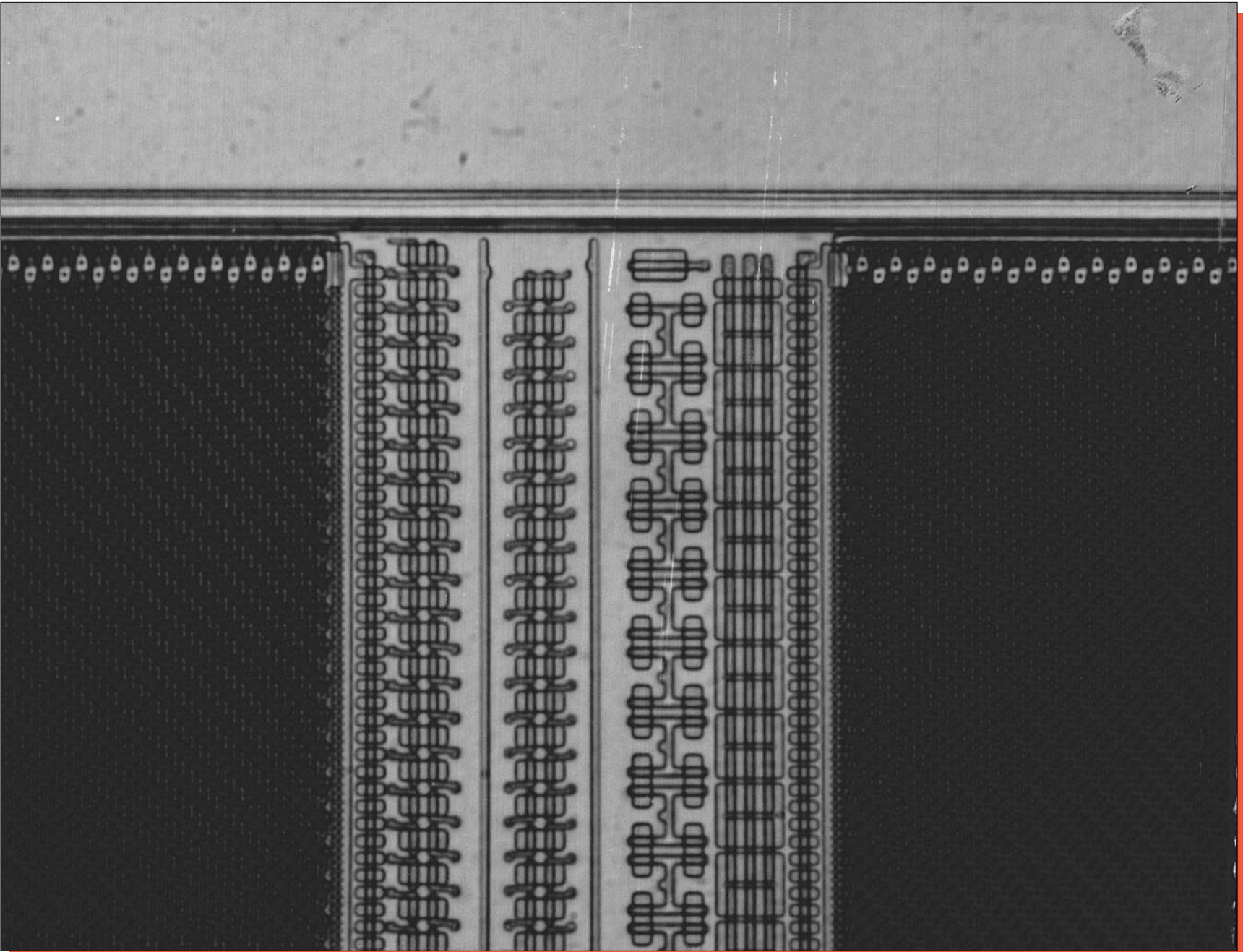


Figure 46b. Optical view of Circuit Block D (unlayered). Mag. 1600x.