Construction Analysis

Fujitsu MB81G8322-010
8Meg. SGRAM

Report Number: SCA 9702-528

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INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Fujitsu MB81G8322-010, 8 Meg SGRAM. One decapped device was received for the analysis. The date code was 9627.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 2 aluminum thinning up to 90 percent[2] at vias (Figure 10).
- Metal 1 aluminum thinning up to 95 percent[2] at contacts (Figure 14).

Special Features:

- Sub-micron gate lengths (0.6 micron P-channel and 0.45 N-channel).
- Stacked capacitor DRAM cell design.
- Four layers of poly in the cell array.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing multiple wells in a P substrate (no epi was used).

- Final passivation: A thick layer of nitride over a layer of glass.

- Metallization: Metal 2 consisted of aluminum with a very thin TiN cap and barrier defined by a dry-etch technique. Metal 1 consisted of aluminum with a titanium-nitride barrier. Standard vias and contacts were employed.

- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of two layers of glass.

- Pre-metal dielectric: A single layer of reflow glass over a densified oxide.

- Polysilicon: Four layers of polysilicon were employed. Poly 4 (sheet) and poly 3 formed the plates of the capacitors. Polycide 2 (poly 2 and tungsten silicide) was used to form the bit lines. These three layers are used exclusively in the cell array. Poly 1 formed all gates and word lines on the die.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Diffusions were not silicided. Sidewall spacers were not present.

- Wells: Multiple wells in a P substrate. N-wells were located under the P-channel devices and under the cell array. A shallow P-well was located within the N-well under the cell array. No step was noted in the local oxide at the edges of the well boundaries.

- Fuses: All Poly 1 redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were present.

TECHNOLOGY DESCRIPTION (continued)

- Memory cells: Stacked capacitor DRAM design. Metal 1 formed the “piggyback” word lines. Metal 2 was not used directly within the cells. Four layers of polysilicon were employed. Poly 4 (sheet) was used to form the common plate of the capacitors and was tied to memory enable. Poly 3 formed the individual plates of the capacitors. Polycide 2 was used to form the bit lines. Poly 1 provided the word lines/select gates.

ANALYSIS RESULTS

Die Process and Design: **Figures 1 - 41b**

Questionable Items:[1]

- Metal 2 aluminum thinning up to 90 percent[2] at vias (Figure 10).
- Metal 1 aluminum thinning up to 95 percent[2] at contacts (Figure 14).

Special Features:

- Sub-micron gate lengths (0.6 micron P-channel and 0.45 N-channel).
- Stacked capacitor DRAM cell design.
- Four layers of poly in the cell array.

General Items:

- Fabrication process: Selective oxidation CMOS process employing multiple wells in a P substrate (no epi was used). No problems were found in this process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

<u>ANALYSIS RESULTS</u> (continued)

- Final passivation: A thick layer of nitride over a layer of glass. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.

- Metallization: Metal 2 consisted of aluminum with a very thin TiN cap and barrier defined by a dry-etch technique. Metal 1 consisted of aluminum with a titanium-nitride barrier. Standard vias and contacts were employed.

- Metal patterning: Both metal layers were defined by a dry-etch of good quality.

- Metal defects: None. No notching of voiding of the metal layers was found. No silicon nodules were found following removal of the aluminum.

- Metal step coverage: Metal 2 aluminum thinned up to 90 percent at vias. It was reduced to 85 percent with the addition of the cap and barrier. Metal 1 aluminum thinned up to 95 percent at contacts. This thinning was reduced to 85 percent with the addition of the barrier. MIL-STD-883D allows up to 70 percent metal thinning for contacts of this size.

- Vias and contacts: Via and contact cuts appeared to be defined by a dry etch. No over-etching or other contact problems were found.

- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of two layers of glass. No problems were found with these layers.

- Pre-metal dielectric: A single layer of reflow glass (BPSG) over a densified oxide in peripheral circuit areas and in the memory array. No problems were found in these layers.

- Polysilicon: Four layers of polysilicon were employed. Poly 4 (sheet) and poly 3 were used to form the plates of the capacitors. Polycide 2 (poly 2 and tungsten silicide) was used to form the bit lines. These three layers were used exclusively in the cell array. Poly 1 formed all gates and word lines on the die. Definition was good at all layers and no problems were noted.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. No step was present in the local oxide at the well boundaries.

- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. No sign of sidewall spacer use visible but they must have been used and removed. No problems were found in any of these areas.

- Wells: Multiple wells in a P substrate. N-wells were located under the P-channel devices and under the cell array. A shallow P-well was located within the N-well under the cell array. No step was noted in the local oxide at the edge of the well boundaries. No problems were noted.

- Fuses: All Poly 1 redundancy fuses had passivation and oxide cutouts over them. Some laser blown fuses were noted.

- Memory cells: Stacked capacitor over bit line DRAM design. Metal 1 formed the "piggyback" word lines. Metal 2 was not used directly within the cells. Four layers of polysilicon were employed. Poly 4 (sheet) was used to form the common plate of the capacitors and was tied to memory enable. Poly 3 formed the individual plate of the capacitors. Polycide 2 was used to form the bit lines. Poly 1 provided the word lines/select gates. Definition was good and no problems were noted. Cell pitch was 1.3 x 2.2 microns (2.9 microns^2).

PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection

SEM inspection of passivation

Passivation integrity test

Delayer to metal 2 and inspect

Aluminum removal (metal 2)

Delayer to metal 1 and inspect

Delayer to poly/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

*****Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Contact registration	G

*****_Metal 2 thinning of up to 90 percent and metal 1 thinning of up to 95 percent._

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIAL ANALYSIS

Overlay passivation:	A thick layer of nitride over a layer of glass.
Metallization 2:	Aluminum with a very thin titanium-nitride (TiN) cap and barrier.
Interlevel dielectric:	Two layers of silicon-dioxide.
Metallization 1:	Aluminum with a titanium-nitride (TiN) barrier.
Pre-metal dielectric:	A single layer of reflow glass over a densified oxide.
Polcide:	Tungsten-silicide.

HORIZONTAL DIMENSIONS

Die size:	4.8 x 15 mm (190 x 595 mils)
Die area:	73 mm^2 (113,050 $mils^2$)
Min pad size:	0.11 x 0.11 mm (4.5 x 4.5 mils)
Min pad window:	0.1 x 0.1 mm (4.1 x 4.1 mils)
Min pad space:	0.03 mm (1.2 mils)
Min metal 2 width:	0.85 micron
Min metal 2 space:	1.0 micron
Min metal 2 pitch:	1.85 micron
Min via:	0.8 micron
Min metal 1 width:	1.2 micron
Min metal 1 space:	0.5 micron
Min metal 1 pitch:	1.7 micron
Min contact:	0.65 micron
Min poly 3 space:	0.35 micron
Min poly 2 width:	0.35 micron
Min poly 2 space:	0.6 micron
Min poly 1 width - (cell):	0.35 micron
Min poly 1 width - (periphery):	0.4 micron
Min poly 1 space:	0.55 micron
Min gate length* - (N-channel):	0.4 micron
- (P-channel):	0.6 micron
Cell area:	2.9 $microns^2$
Cell size:	1.3 x 2.2 microns

*****_Physical gate length._

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (20 mils)

Layers

Passivation 2:	0.5 micron
Passivation 1:	0.15 micron
Metal 2 - aluminum:	0.8 micron
Interlevel dielectric 1 - glass 2:	0.65 micron
- glass 1:	0.11 micron
Metal 1 - aluminum:	0.35 micron
- barrier:	0.15 micron
Reflow glass:	0.06-0.4 micron
Poly 4 (sheet):	0.05 micron (approximate)
Poly 3:	0.1 micron (approximate)
Poly 2:	0.15 micron
Poly 1:	0.15 micron
Local oxide:	0.35 micron
N+ S/D diffusion:	0.2 micron
P+ S/D diffusion:	0.25 micron
N-well:	3.2 microns
P-well:	1.0 micron

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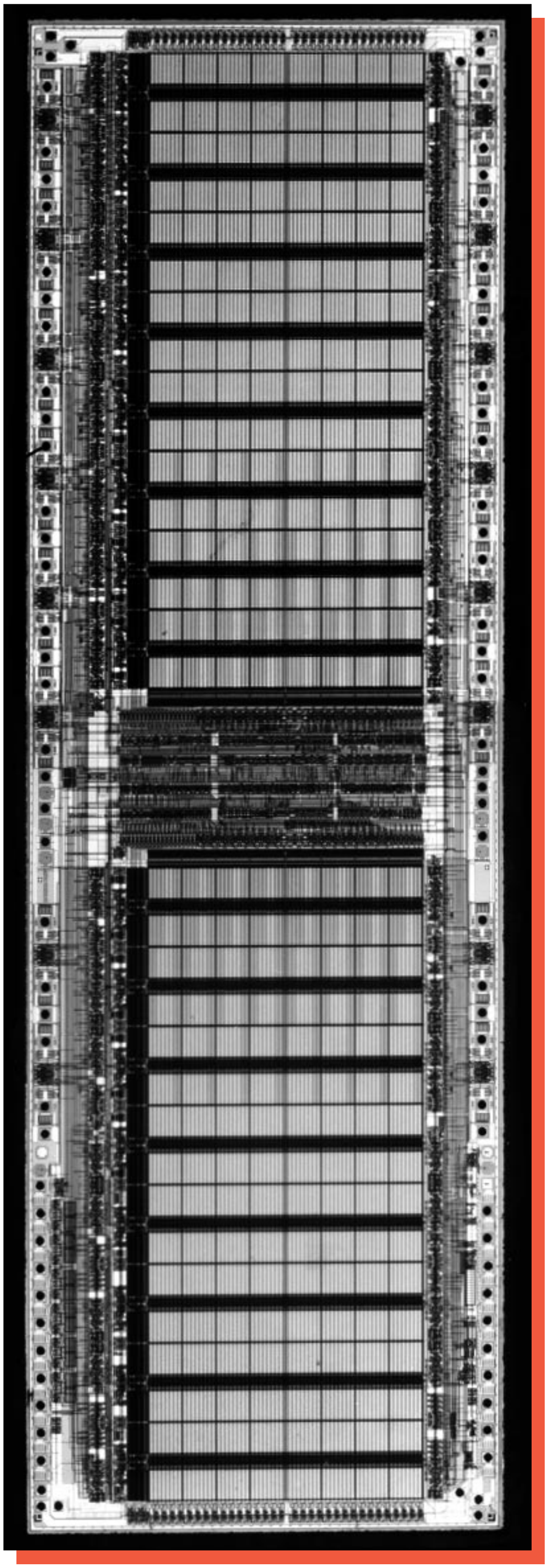
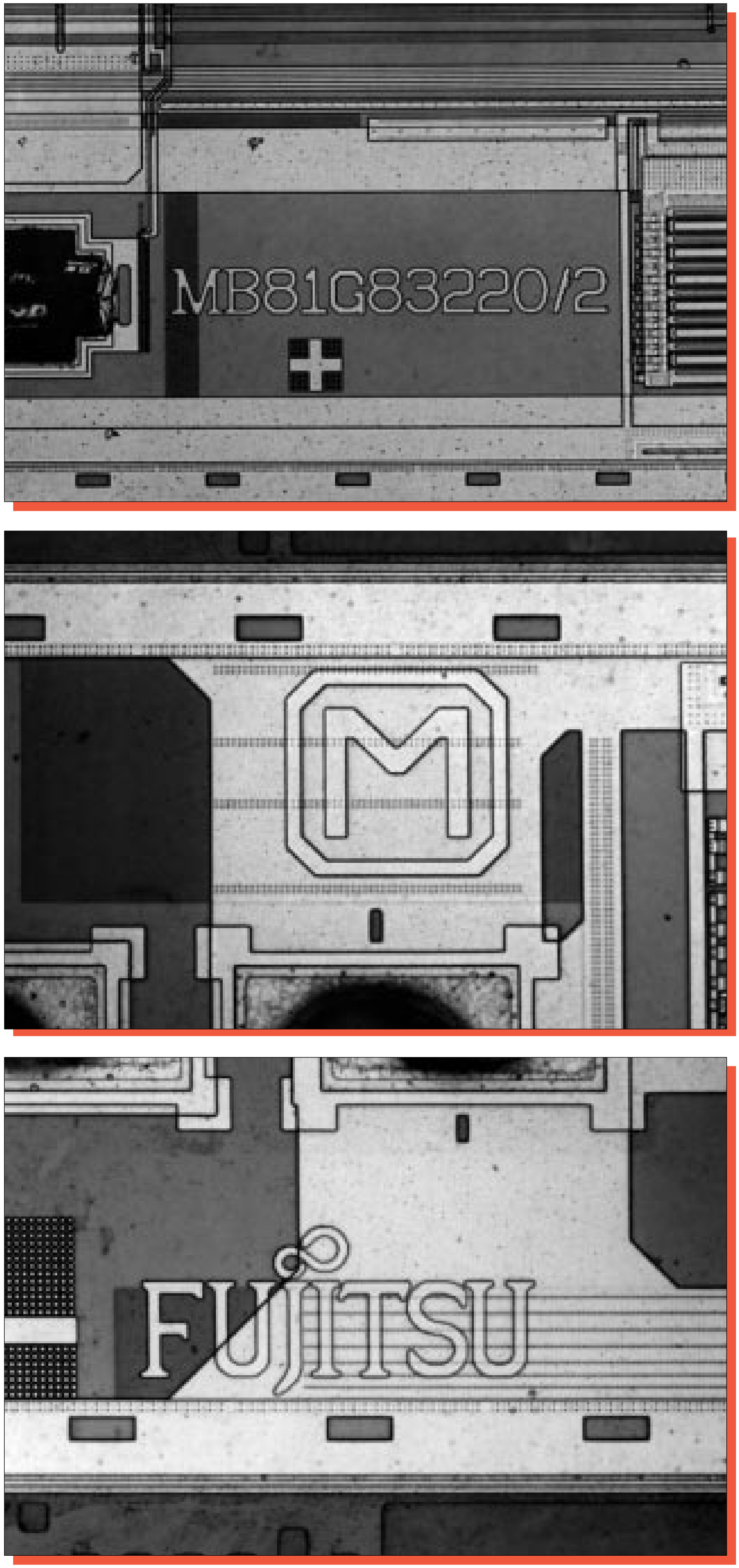


Figure 1. Whole die photograph of the Fujitsu MB81G8322-010 8M SRAM. Mag. 13x.



Mag. 200x

Mag. 400x

Mag. 400x

Figure 2. Optical views of the die markings from the surface.

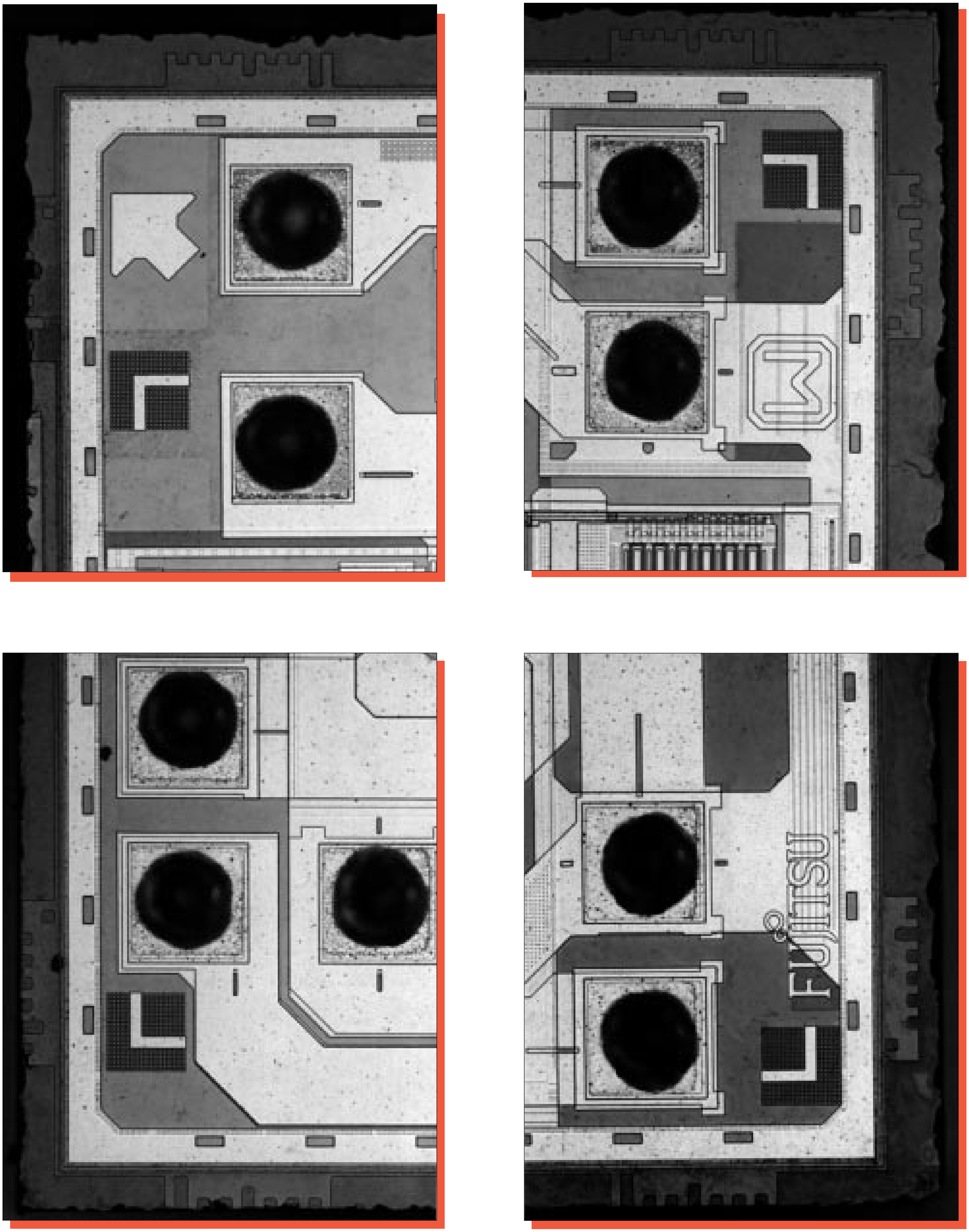
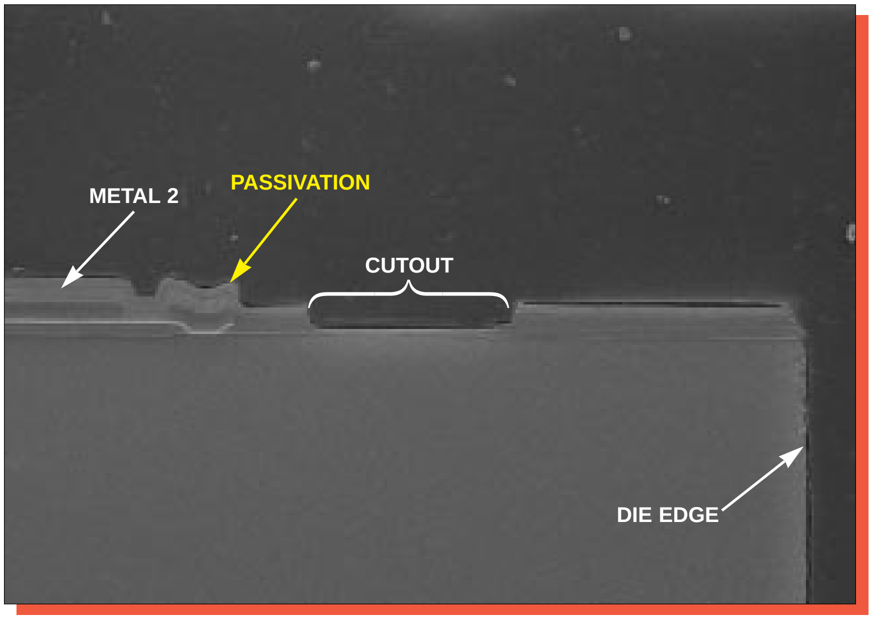
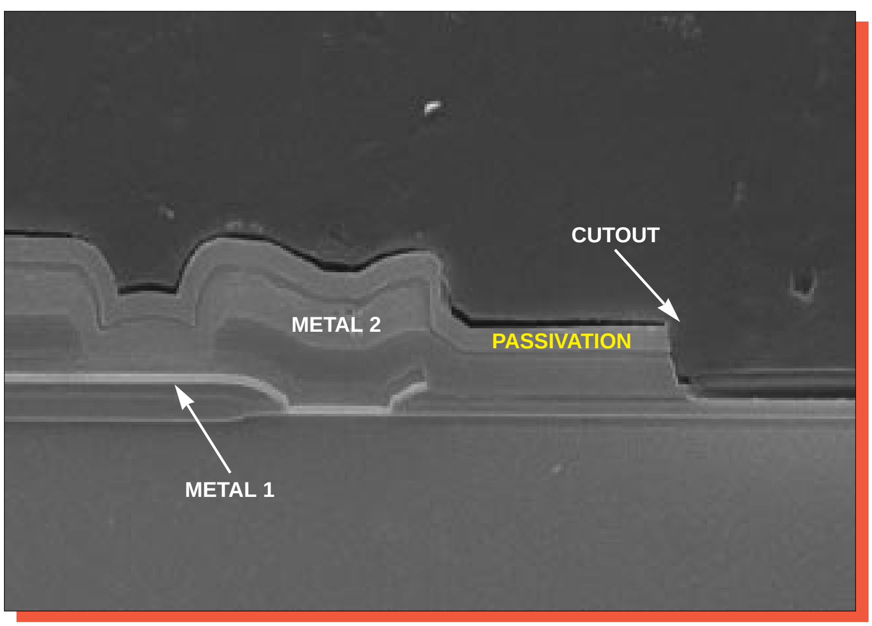


Figure 3. Optical views of the die corners on the Fujitsu MB81G8322-010. Mag. 200x.

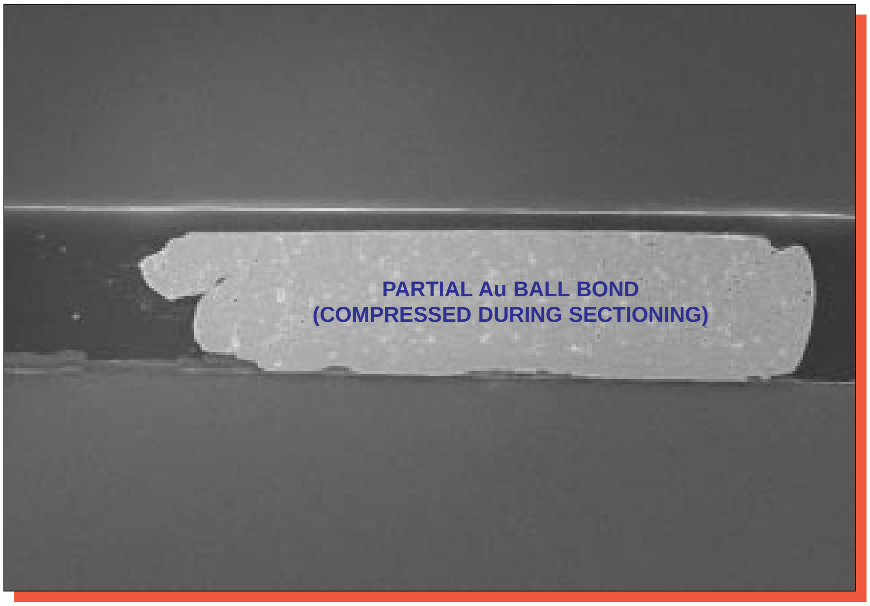


Mag. 2000x

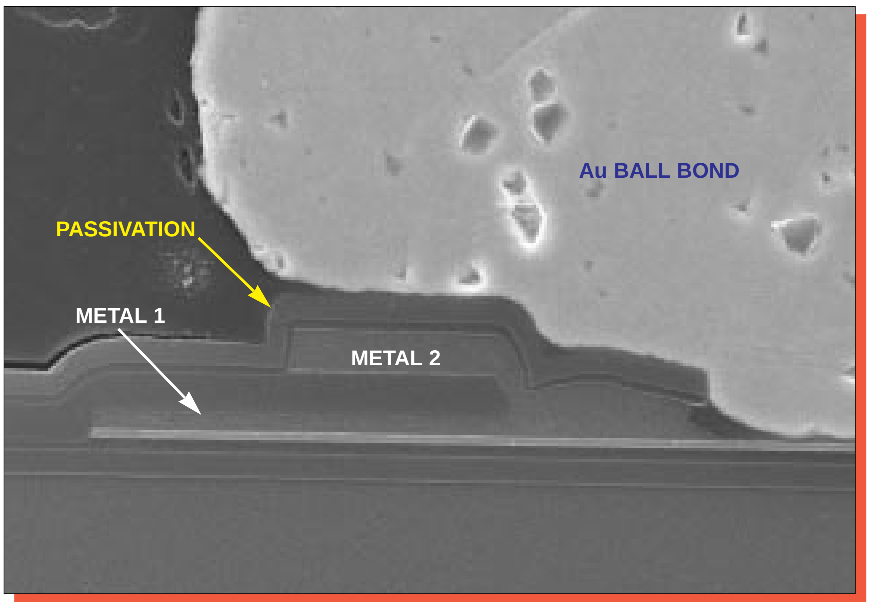


Mag. 7000x

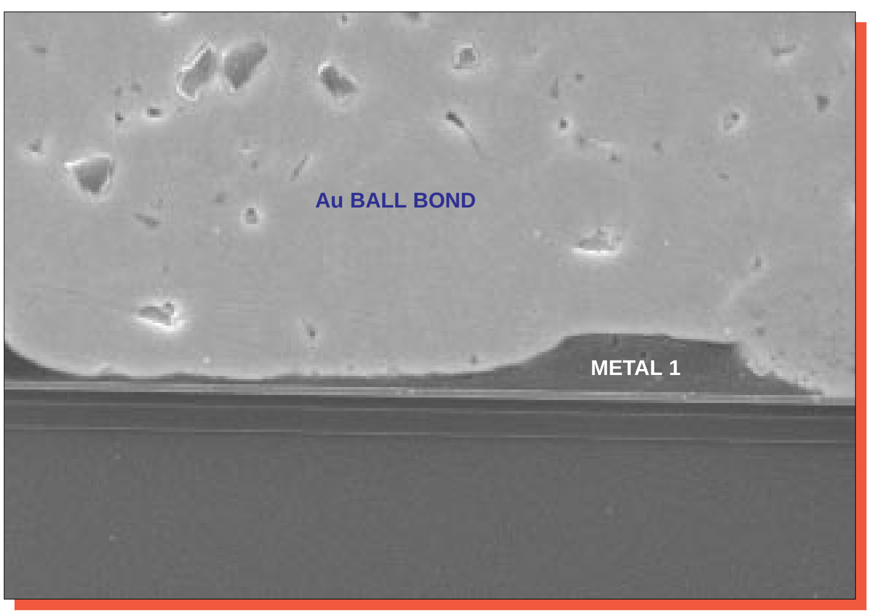
Figure 4. SEM section views of the edge seal.



Mag. 810x

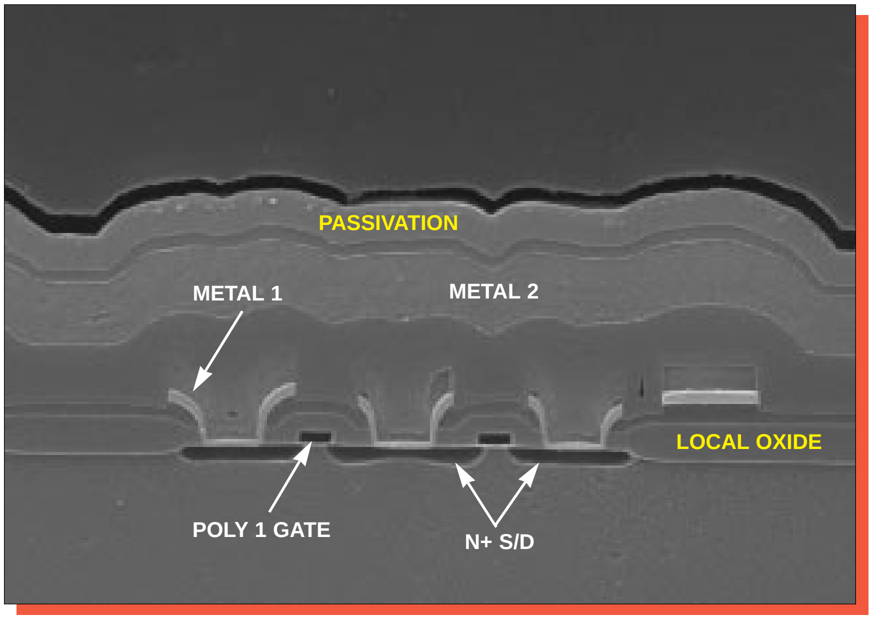


Mag. 6500x



Mag. 6500x

Figure 5. SEM section views of the bond pad structure.



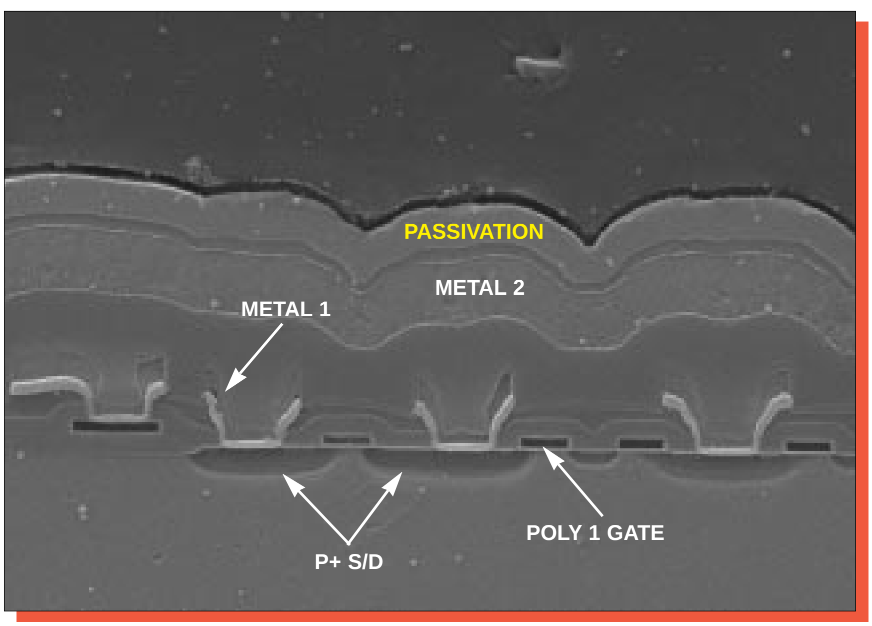
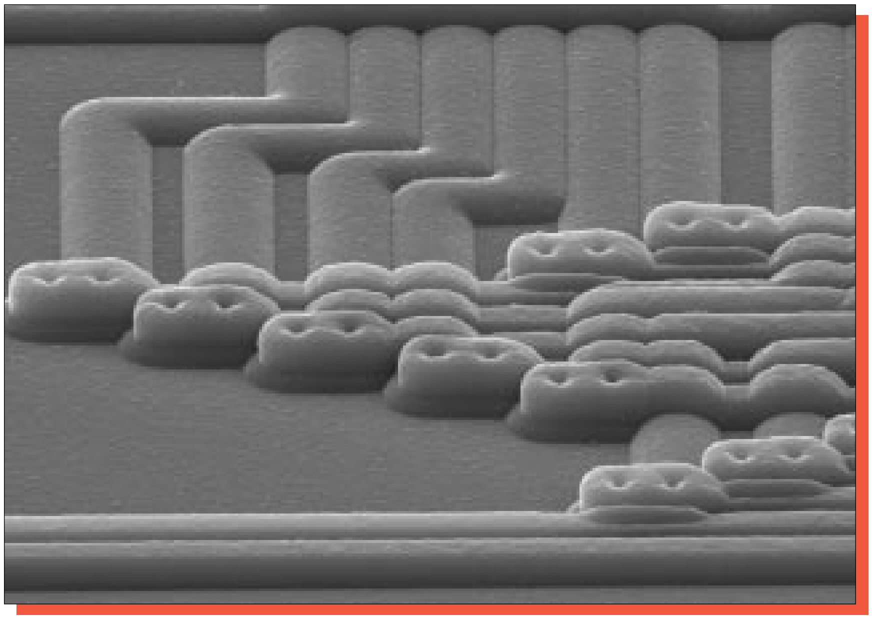
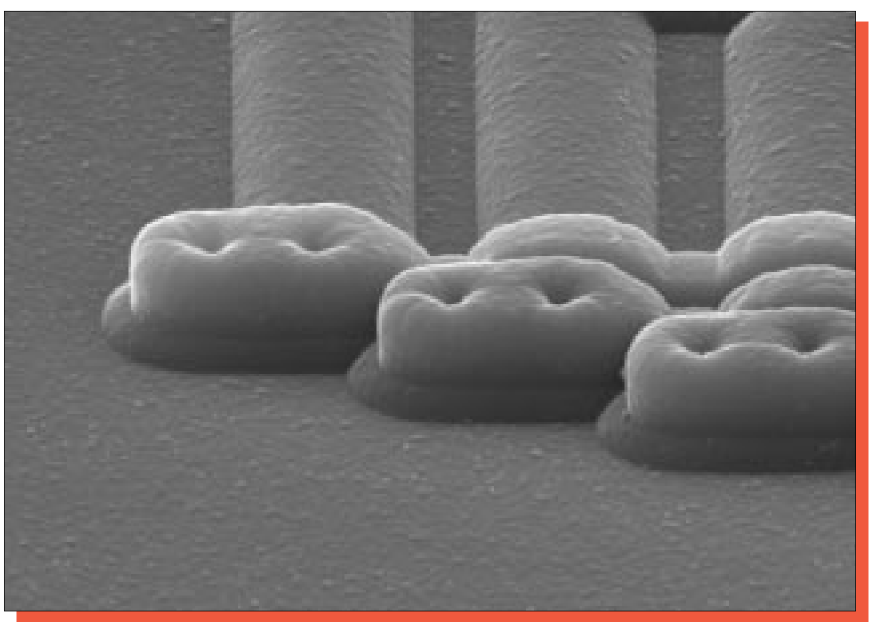


Figure 6. SEM section views of general construction. Silicon etch, Mag. 10,000x.

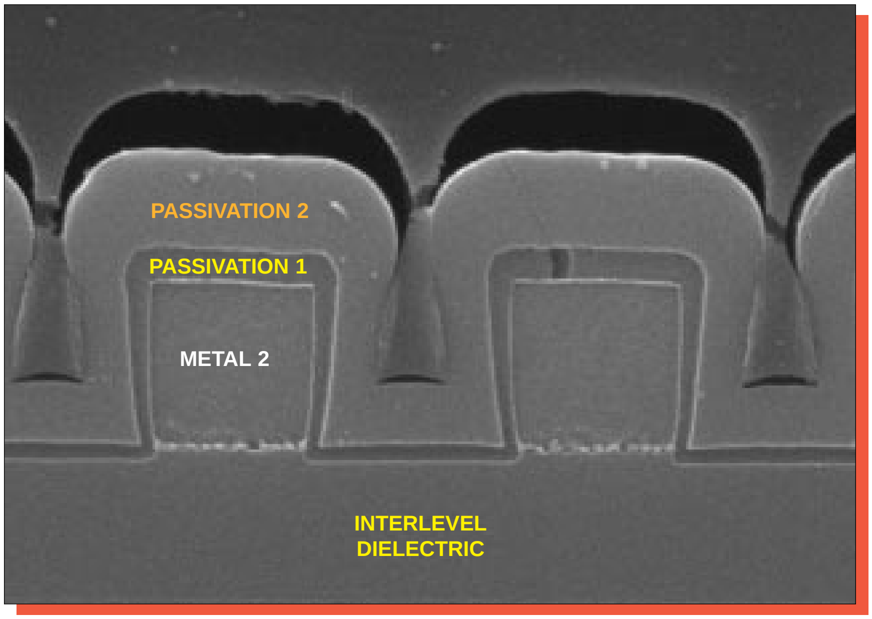


Mag. 4000x

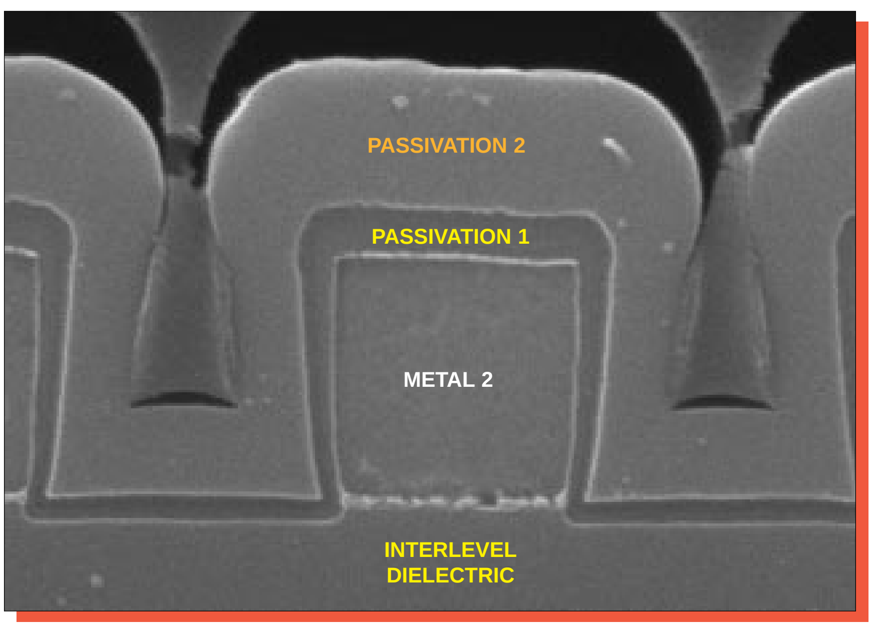


Mag. 8000x

Figure 7. SEM views of overlay passivation coverage. 60°.

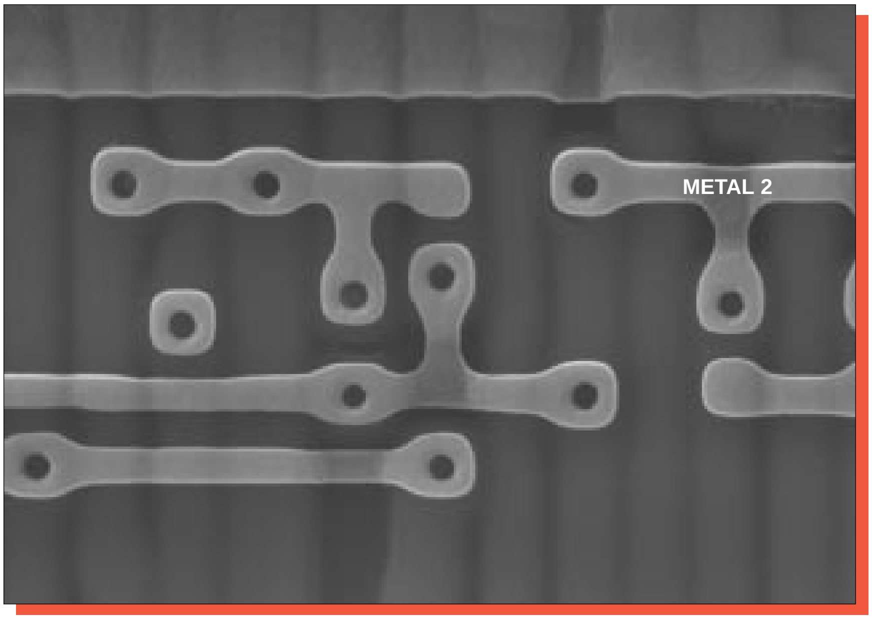


Mag. 26,000x

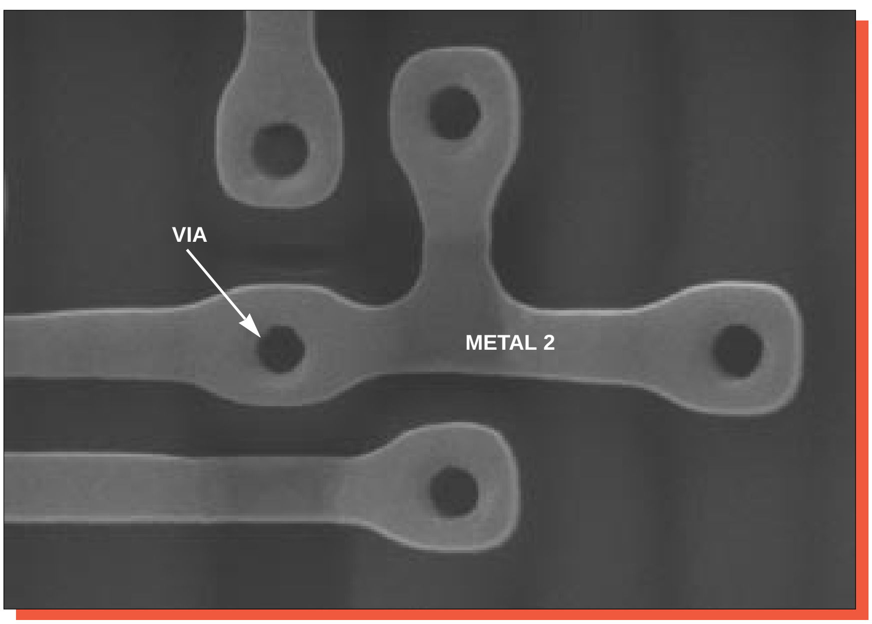


Mag. 40,000x

Figure 8. SEM section views of metal 2 line profiles.

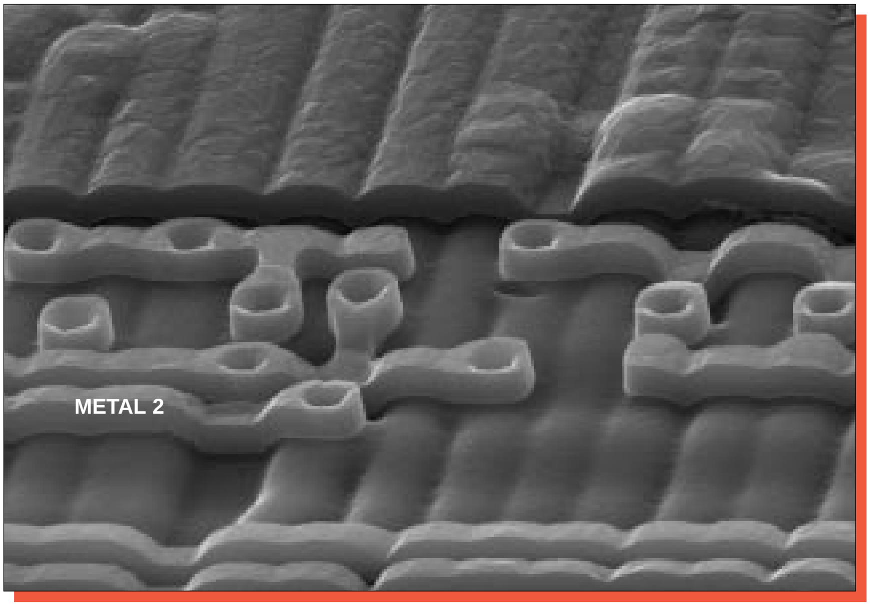


Mag. 5000x

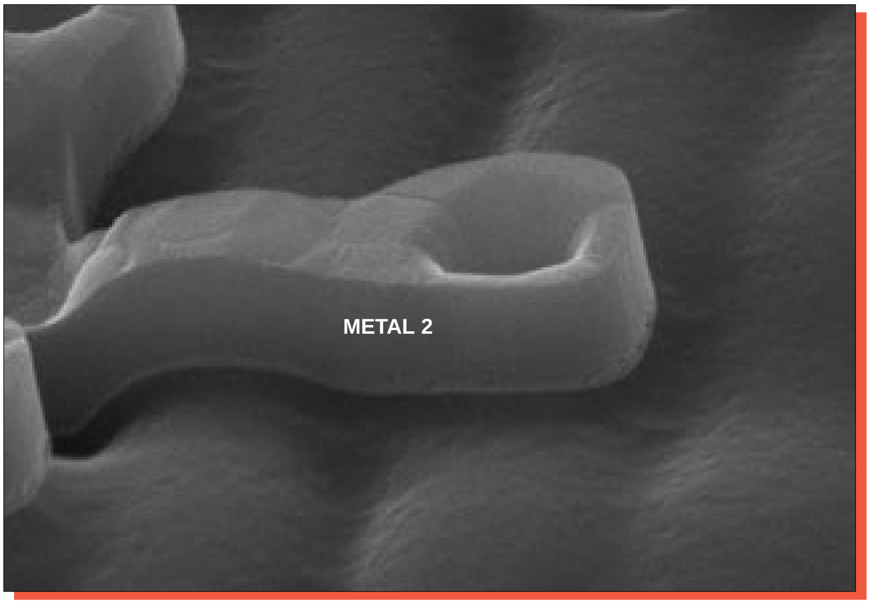


Mag. 10,000x

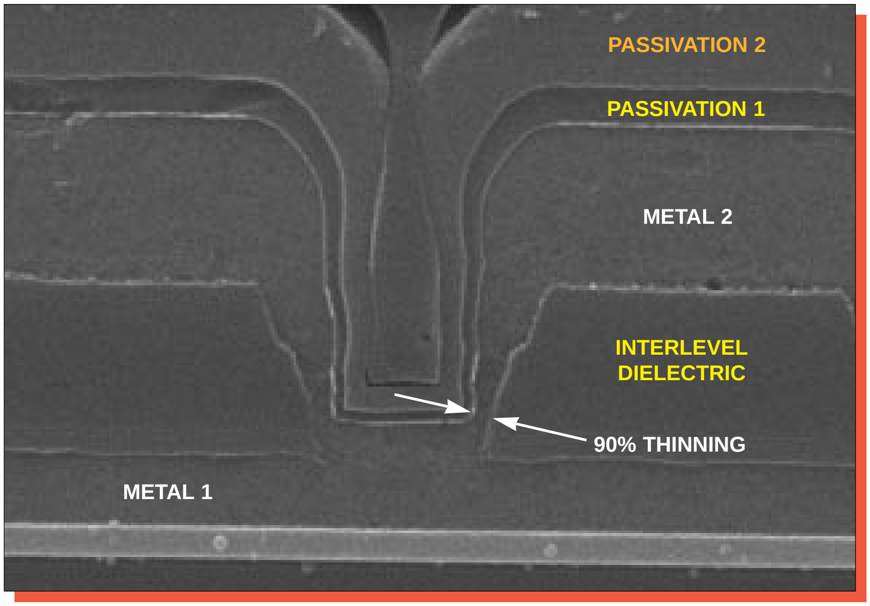
Figure 9. Topological SEM views of metal 2 patterning. 0°.



Mag. 5500x, 60°

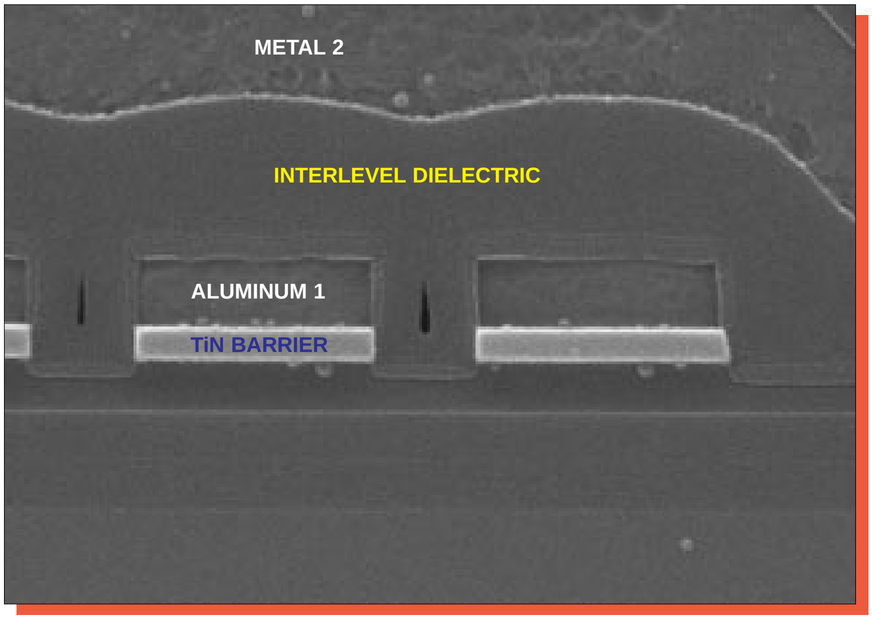


Mag. 20,000x, 60°

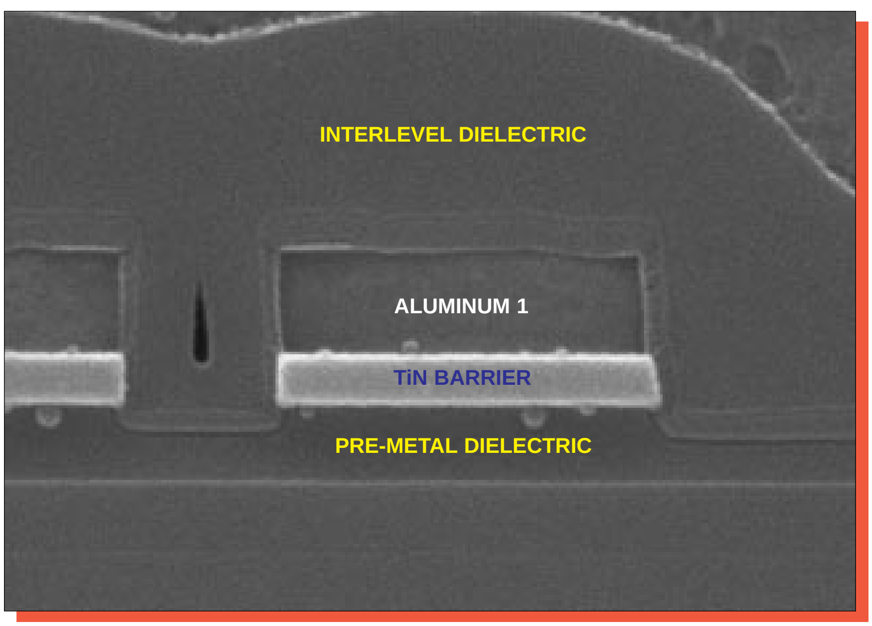


Mag. 26,000x

Figure 10. SEM views of metal 2 coverage and via.

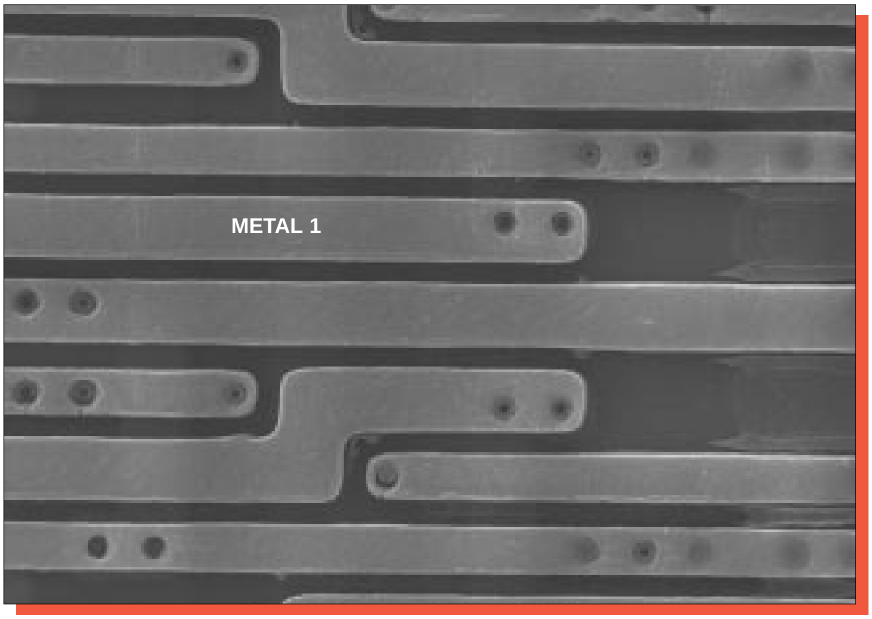


Mag. 26,000x

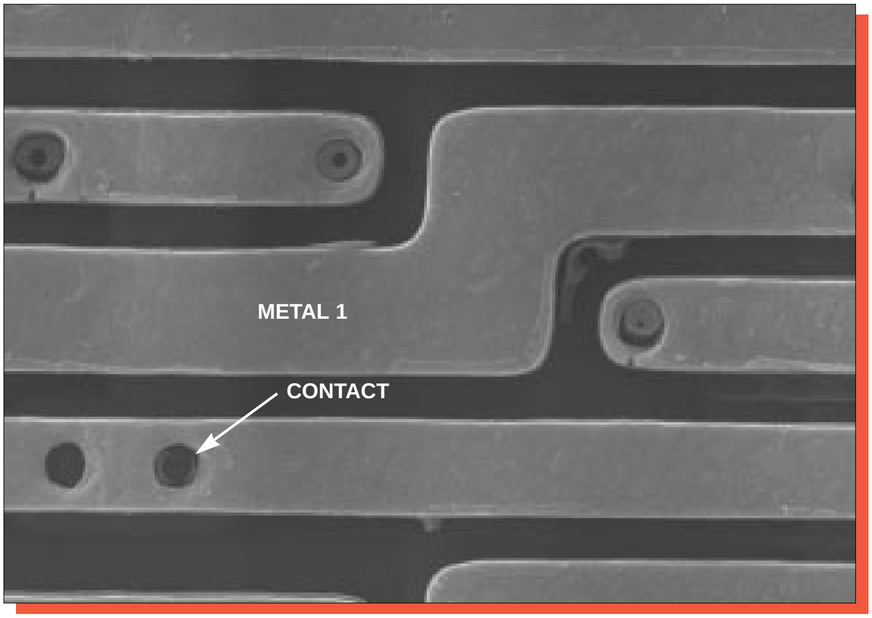


Mag. 40,000x

Figure 11. SEM section views of metal 1 line profiles.

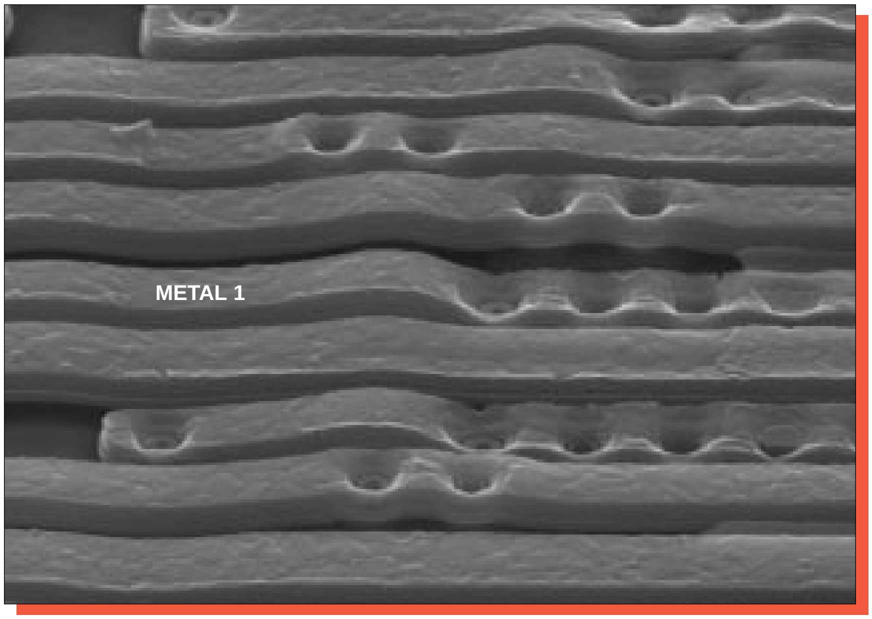


Mag. 5200x

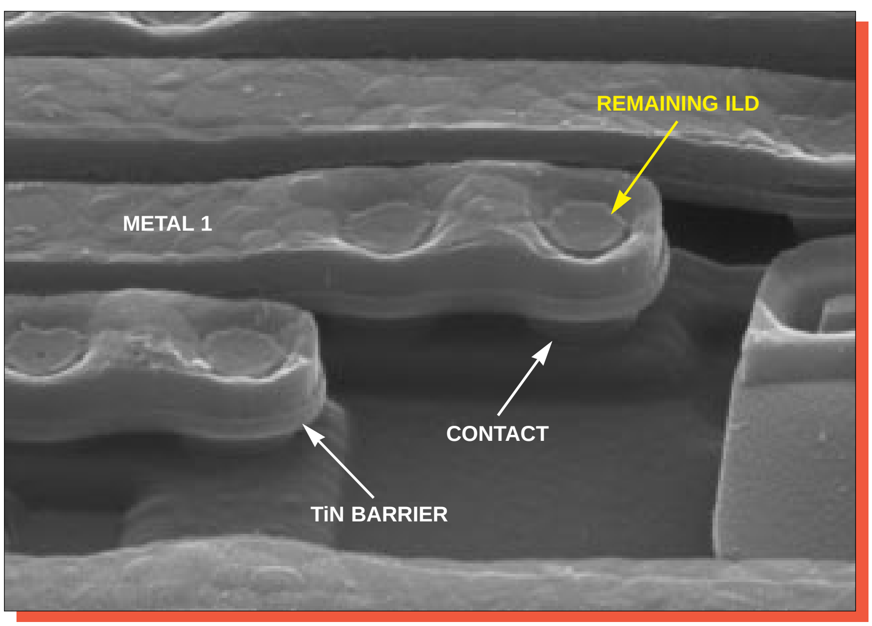


Mag. 10,000x

Figure 12. Topological SEM views of metal 1 patterning. 0°.

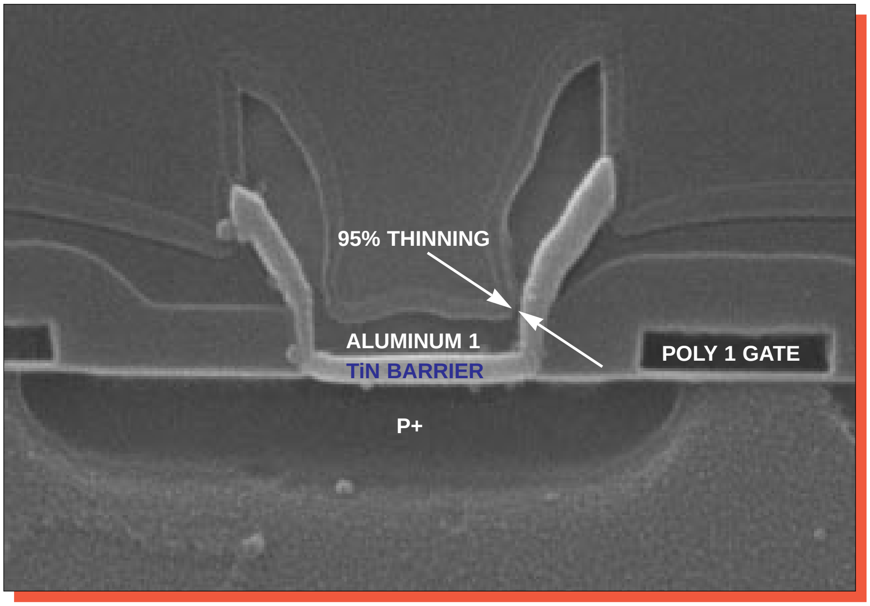


Mag. 8800x

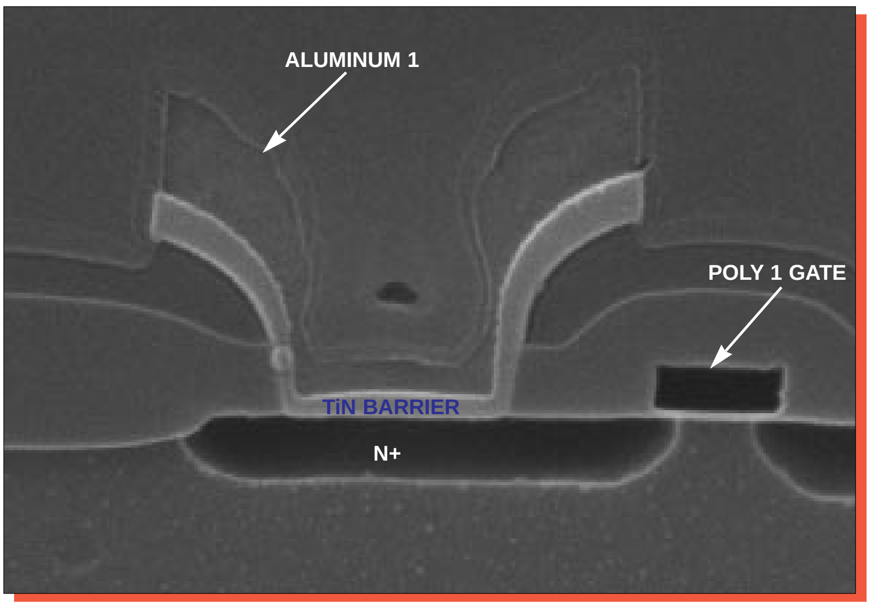


Mag. 17,000x

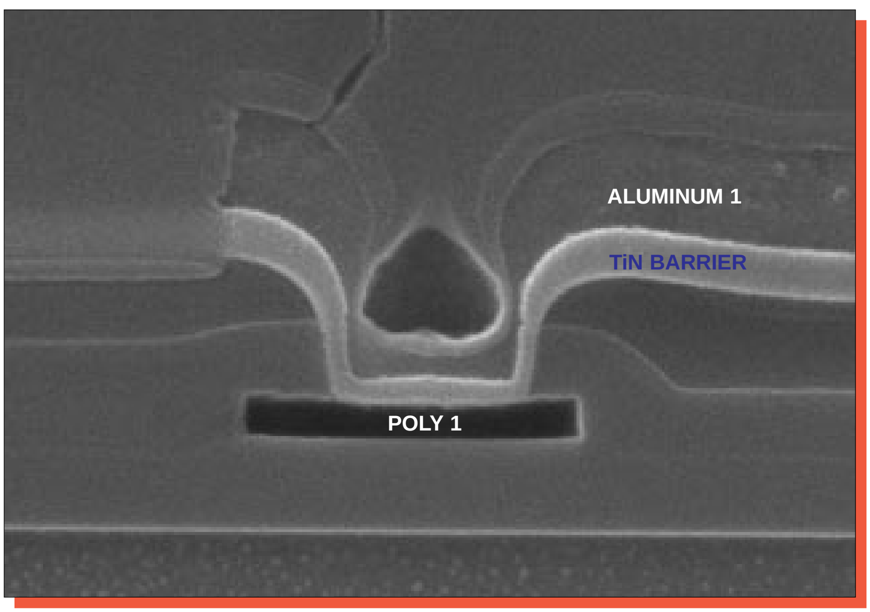
Figure 13. Perspective SEM views of metal 1 coverage. 60°.



metal 1-to-P+

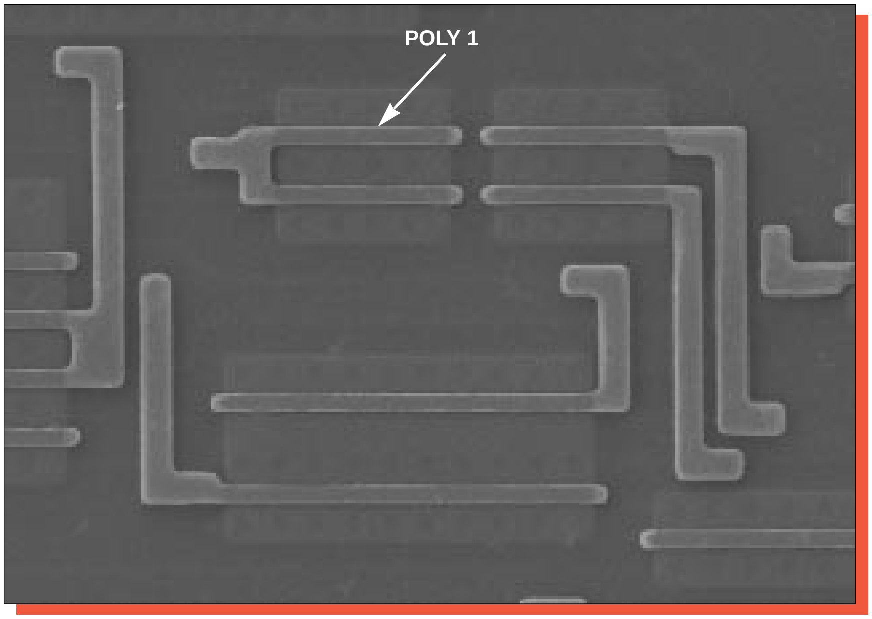


metal 1-to-N+

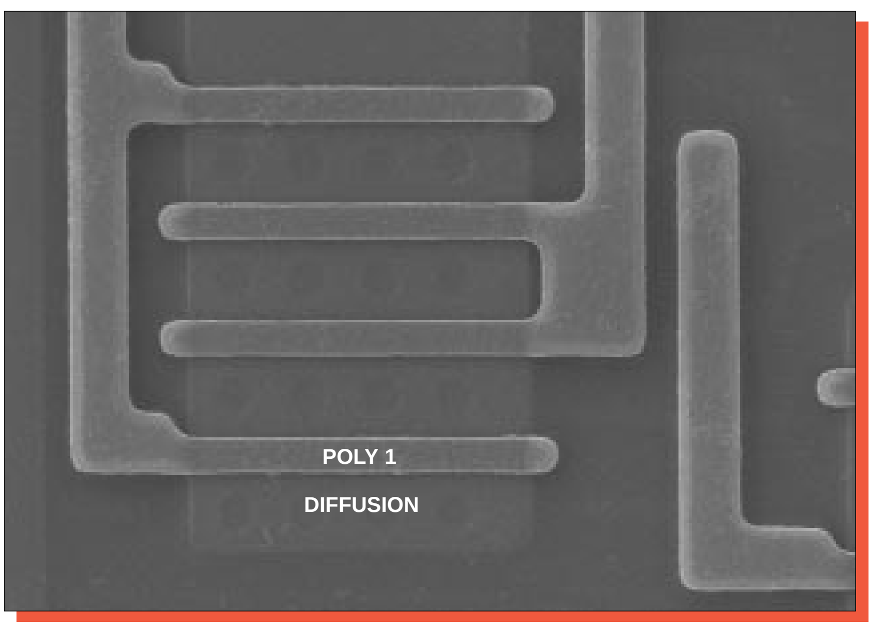


metal 1-to-poly 1

Figure 14. SEM section views ot typical metal 1 contacts. Mag. 40,000x.

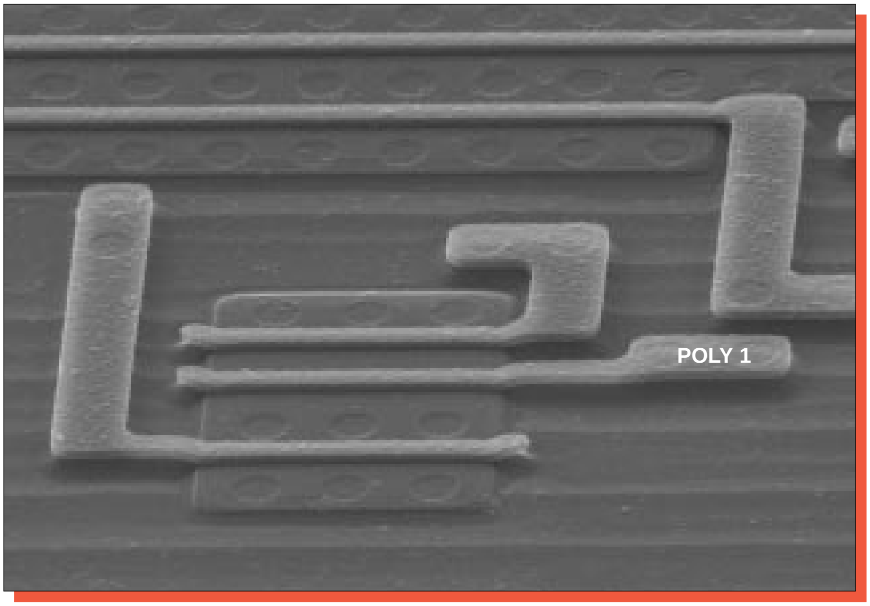


Mag. 3200x

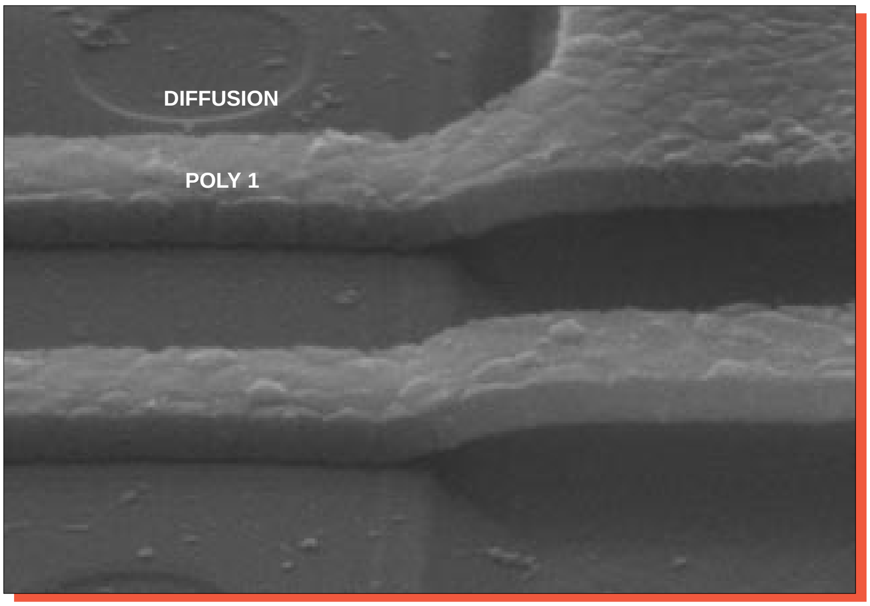


Mag. 6500x

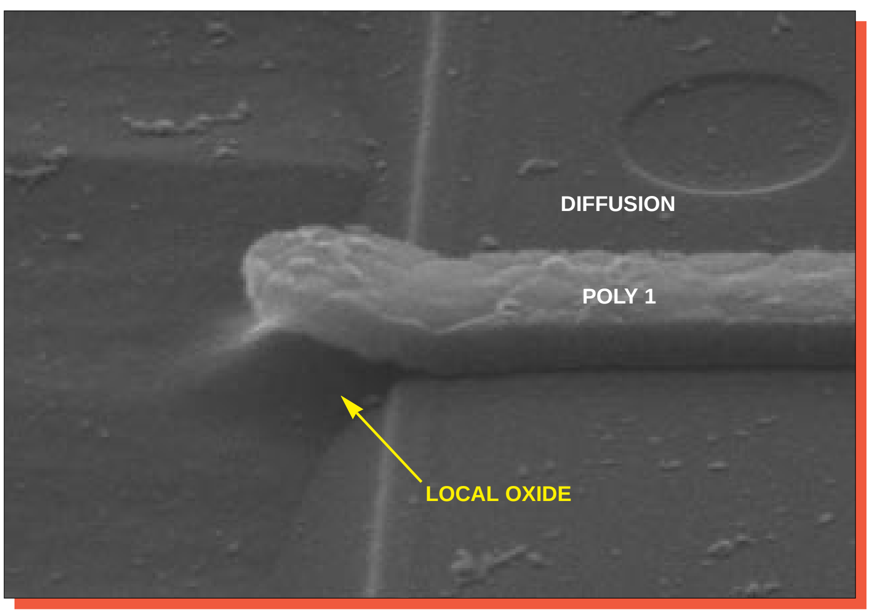
Figure 15. Topological SEM views of poly 1 patterning. 0°.



Mag. 8000x

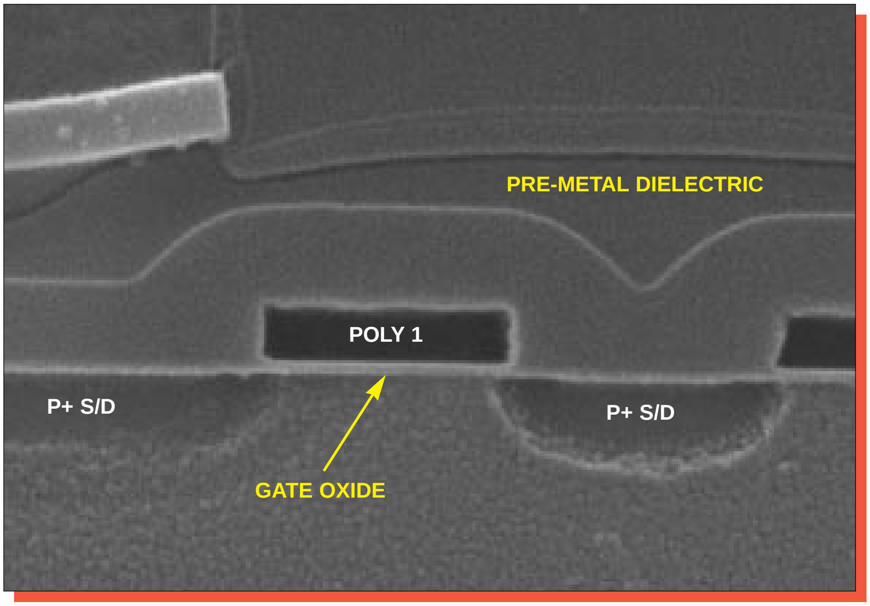


Mag. 40,000x

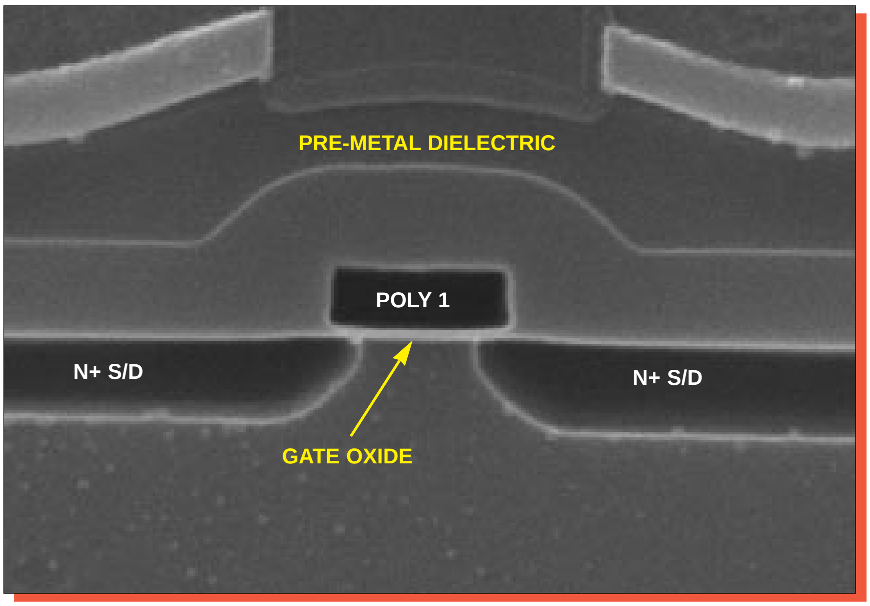


Mag. 40,000x

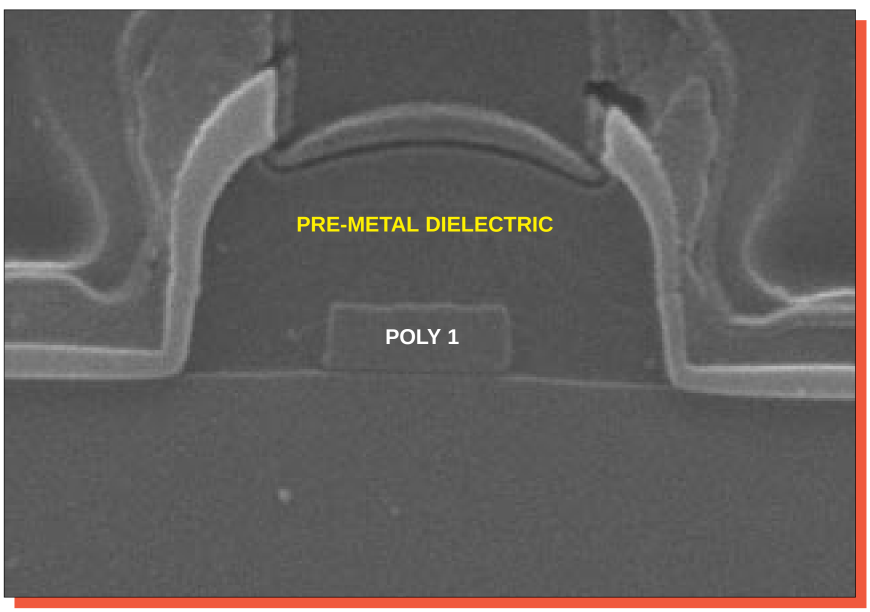
Figure 16. Perspective SEM views of poly 1 coverage. 60°.



P-channel, silicon etch



N-channel, silicon etch



glass etch

Figure 17. SEM section views of typical transistors. Mag. 52,000x.

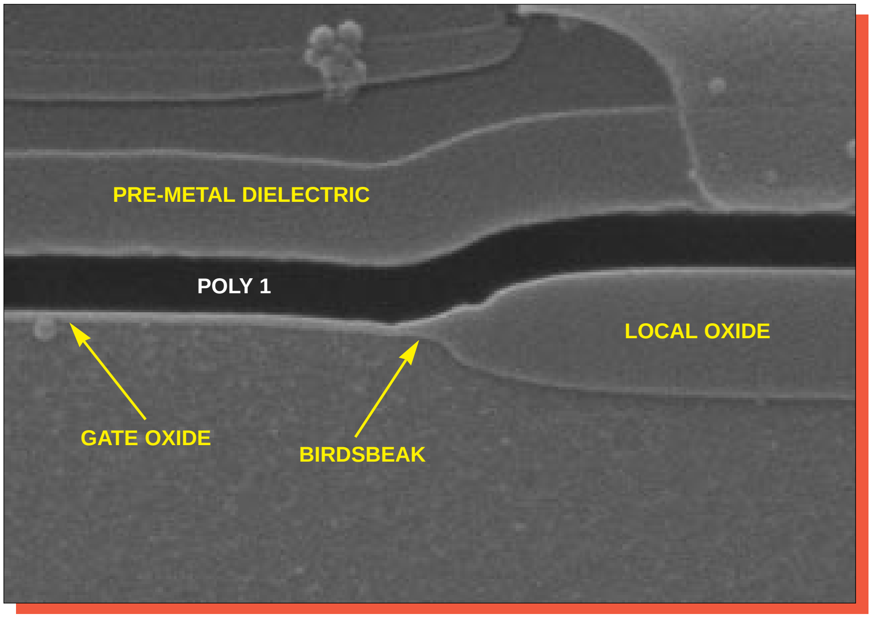


Figure 18. SEM section view of a local oxide birdsbeak. Mag. 52,000x.

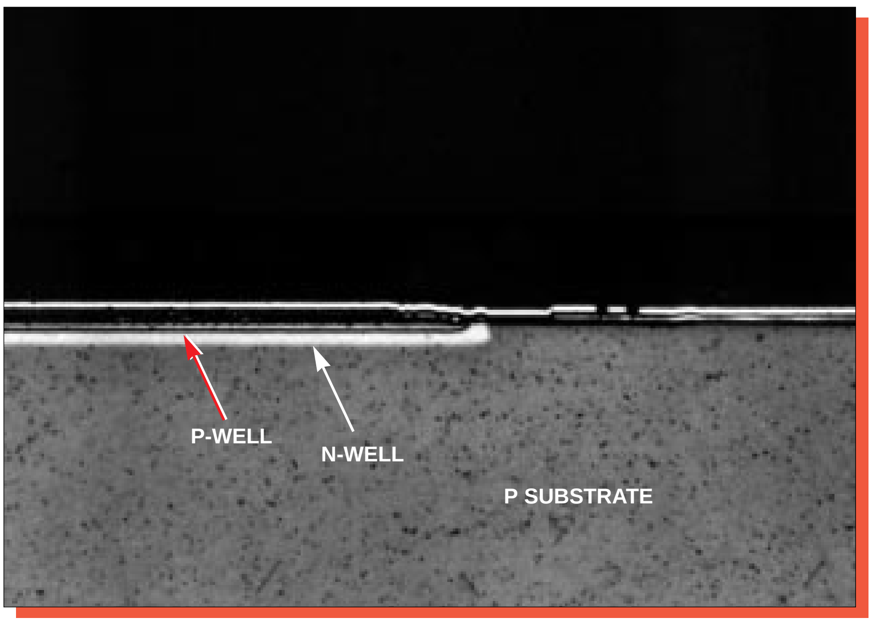
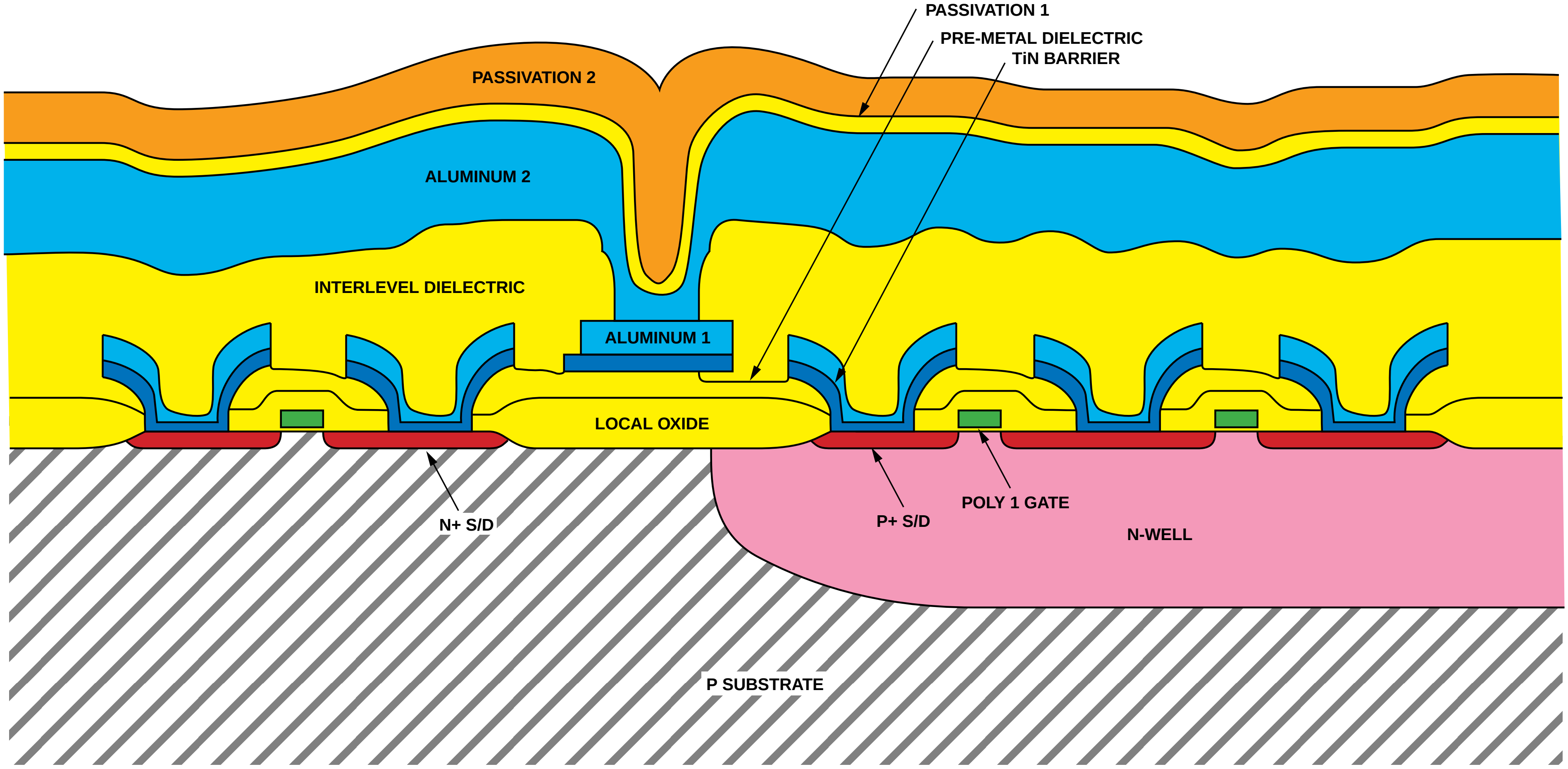


Figure 19. Optical view of the well structure. Mag. 800x.

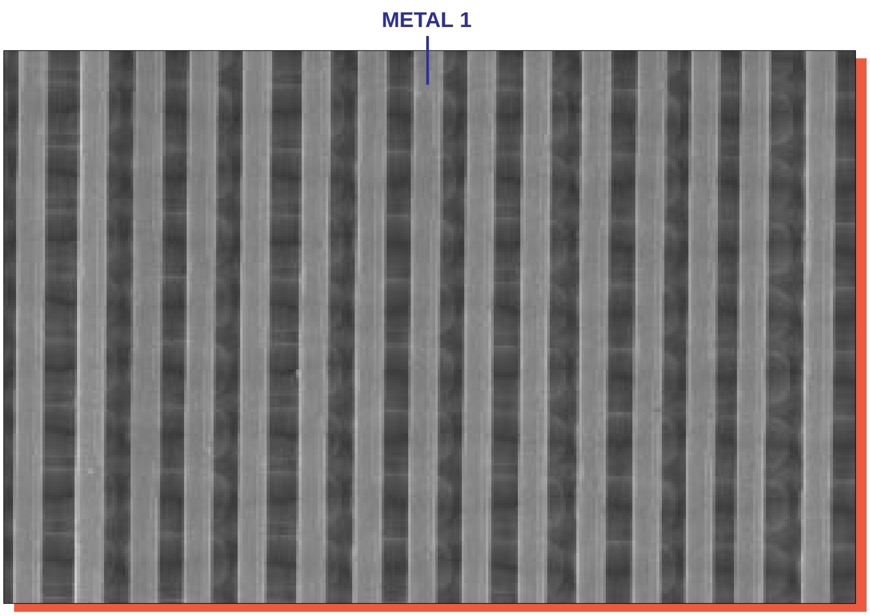


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

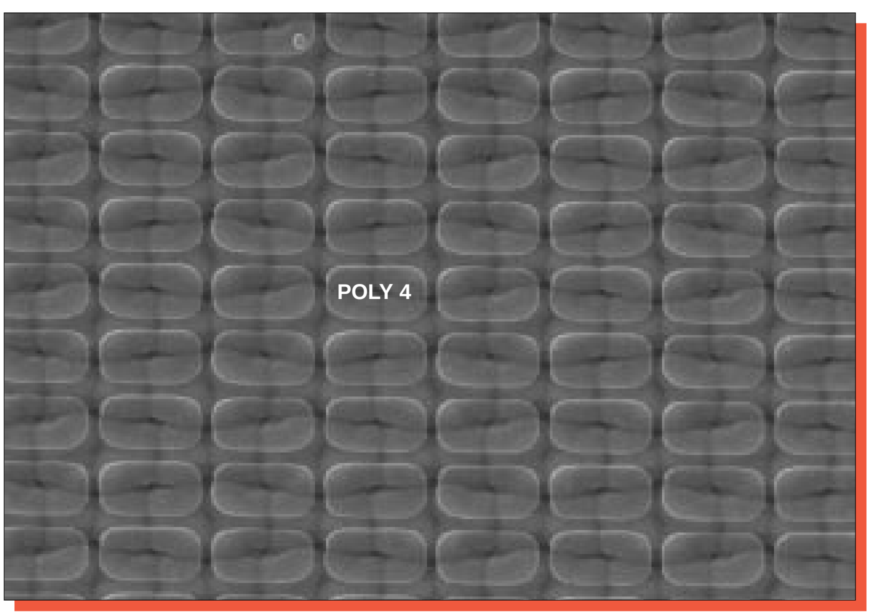
Red = Diffusion, and Gray = Substrate

Figure 20. Color cross section drawing illustrating device structure.

metal 2

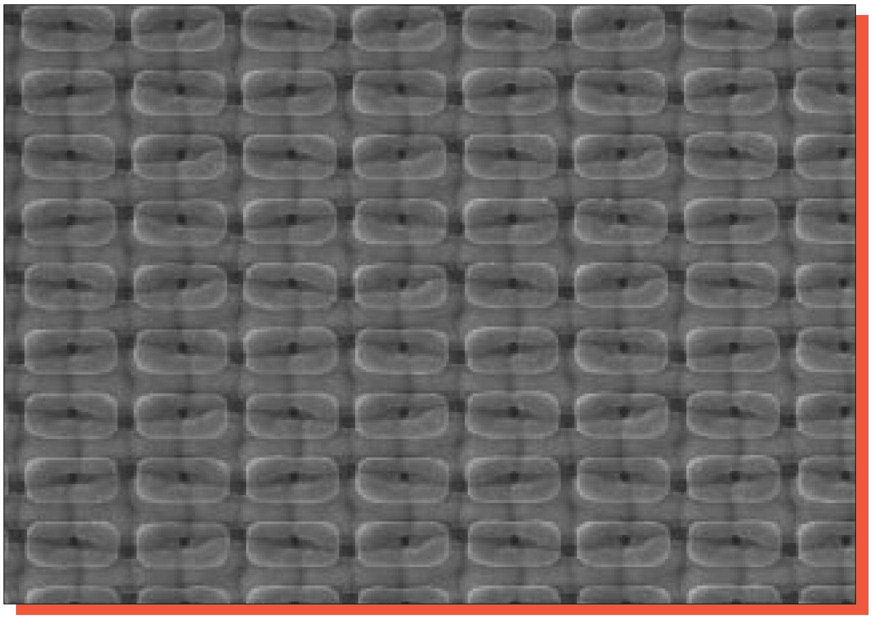


metal 1

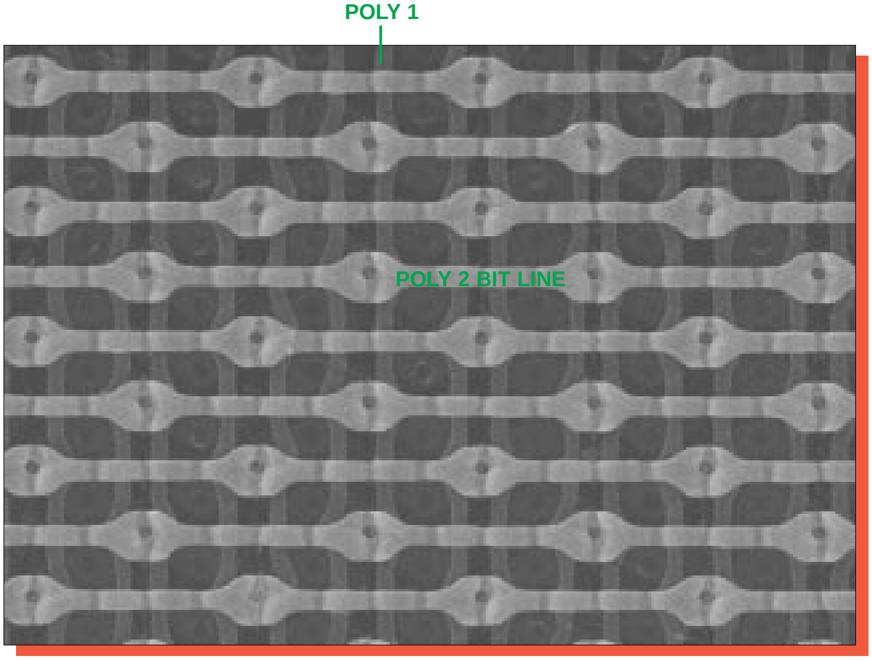


poly 4 sheet

Figure 21. Topological SEM views of the DRAM cell array. Mag. 6500x. 0°.

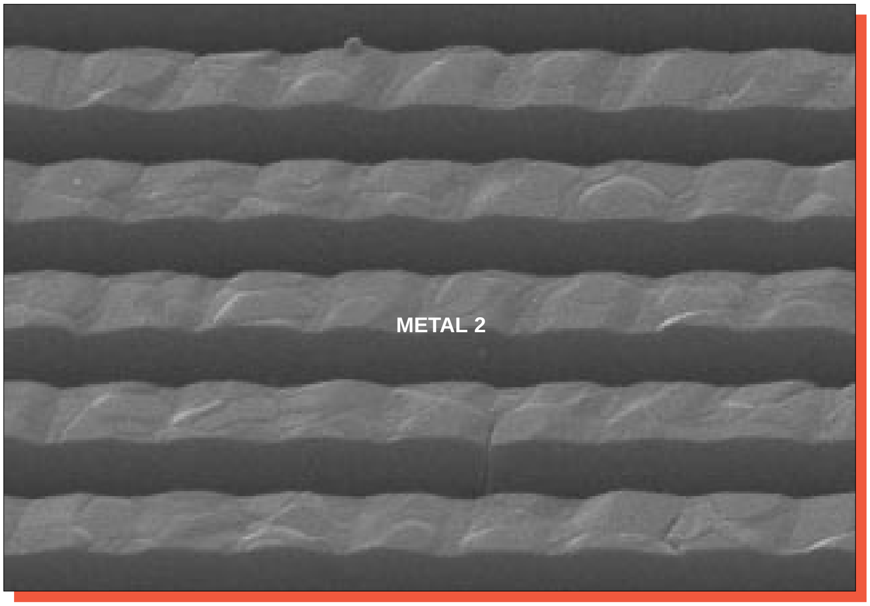


poly 3 capacitors

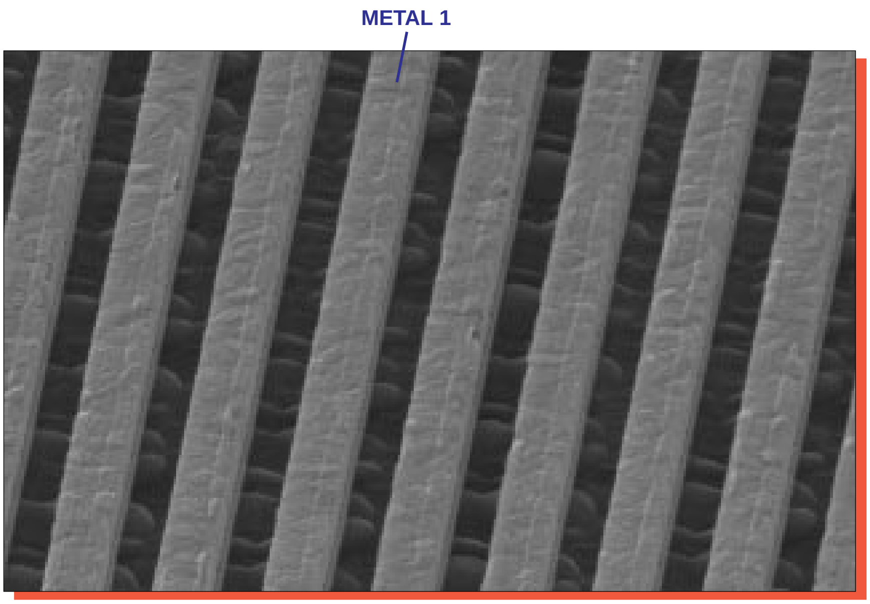


poly 2 and 1

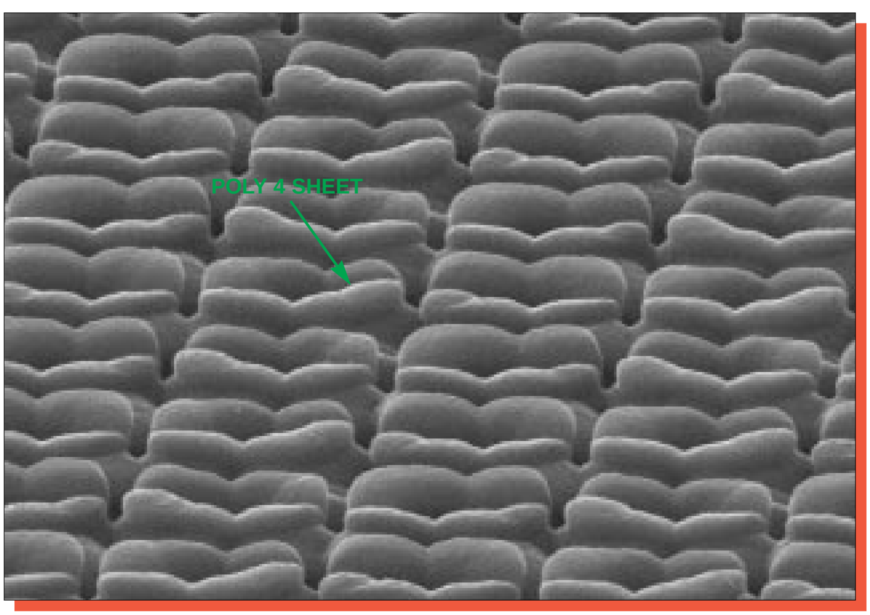
Figure 22. Topological SEM views of the DRAM cell array. Mag. 6500x, 0°.



metal 2

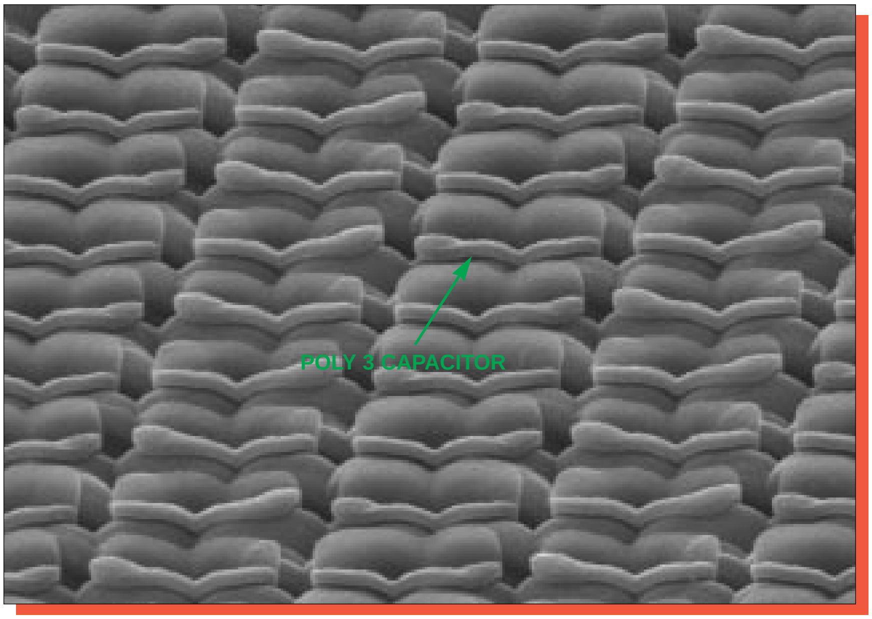


metal 1

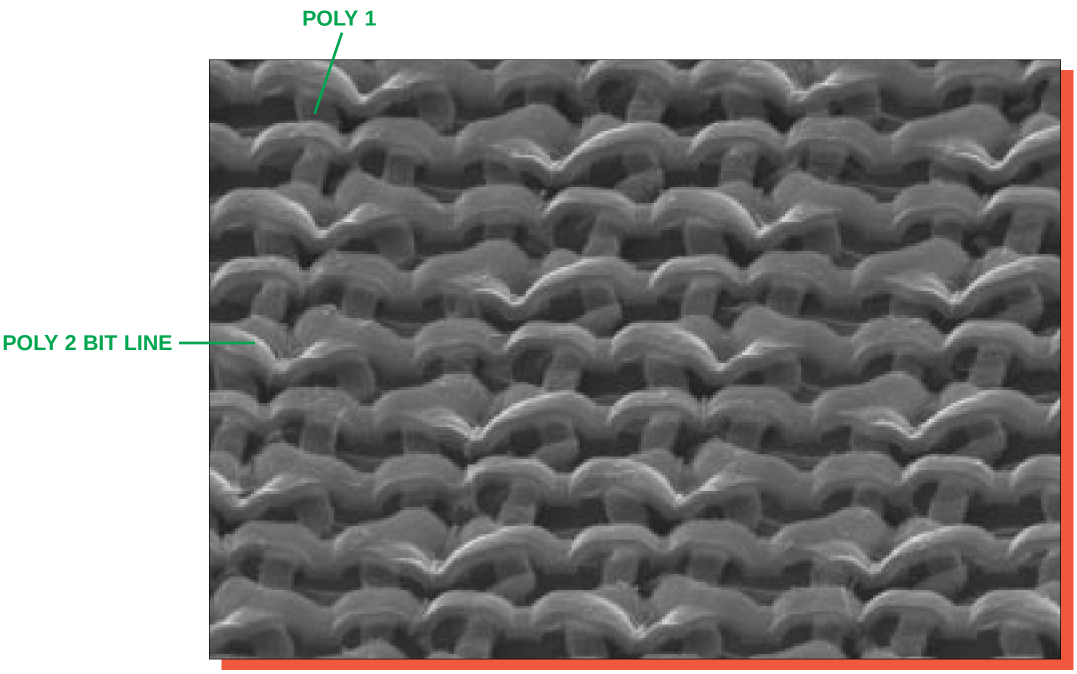


poly 4 sheet

Figure 23. Perspective SEM views of the DRAM cell array. Mag. 13,000x. 60°.

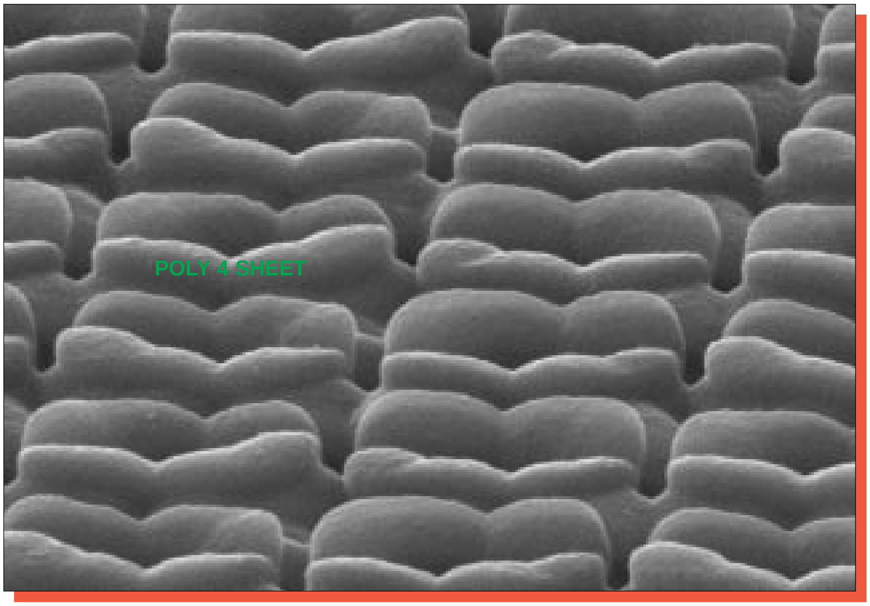


poly 3

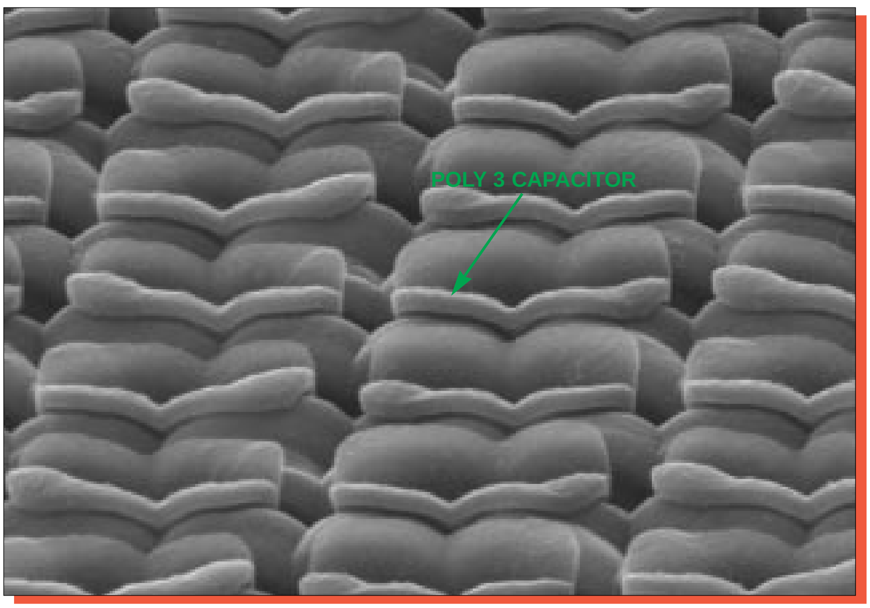


poly 2 and 1

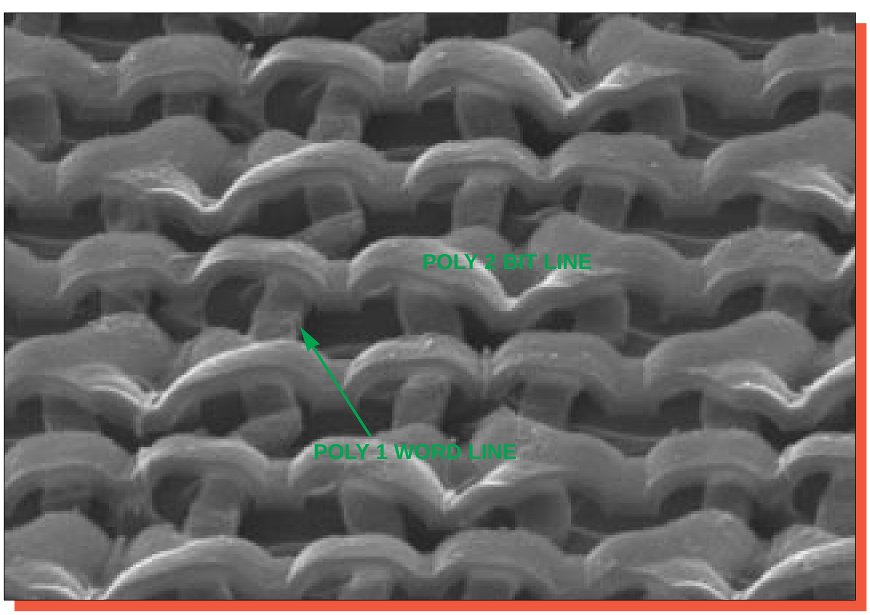
Figure 24. Perspective SEM views of the DRAM cell array. Mag. 13,000x, 60°.



poly 4 sheet

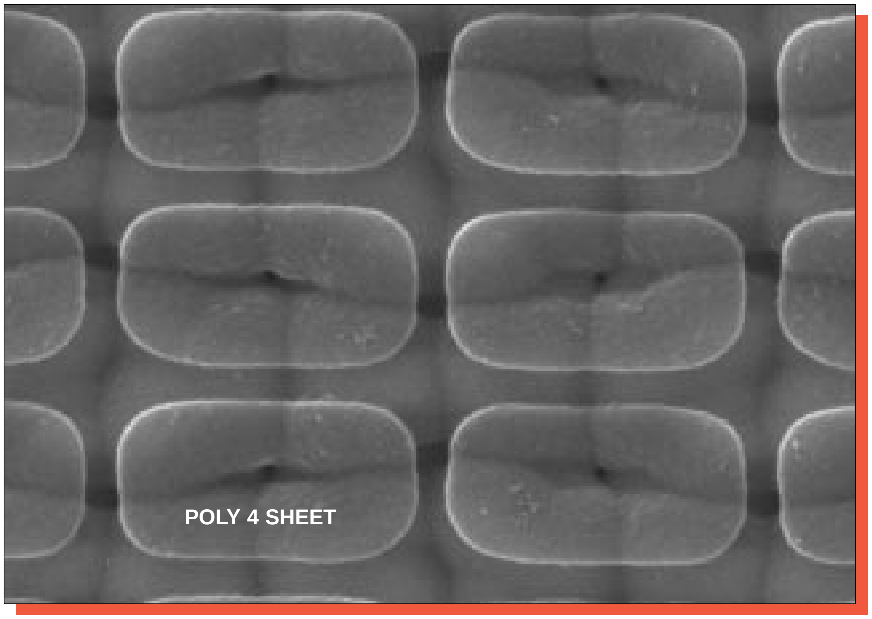


poly 3

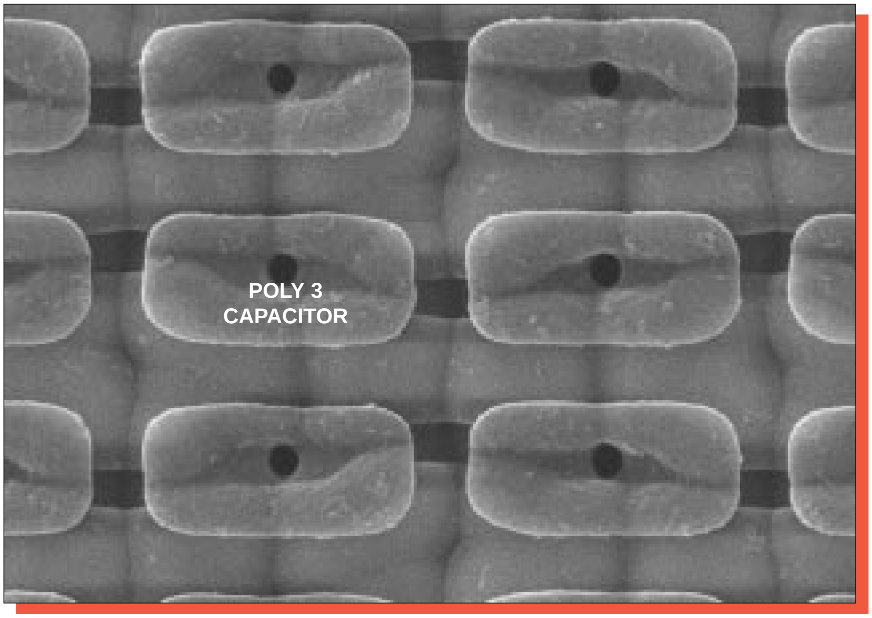


poly 2 and 1

Figure 25. Detailed SEM views of the DRAM cell array. Mag. 20,000x.

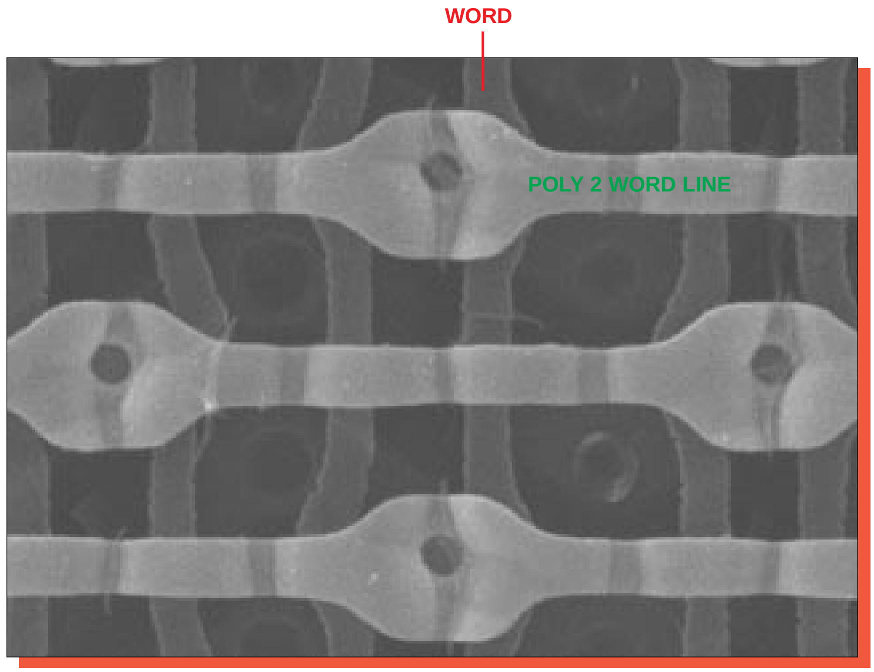


poly 4 sheet



poly 3

Figure 26. Detailed topological SEM views of the DRAM cell array. Mag. 20,000x, 0.



Mag. 20,000x

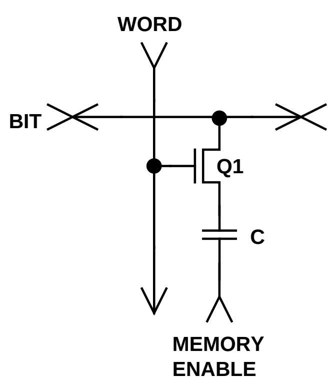
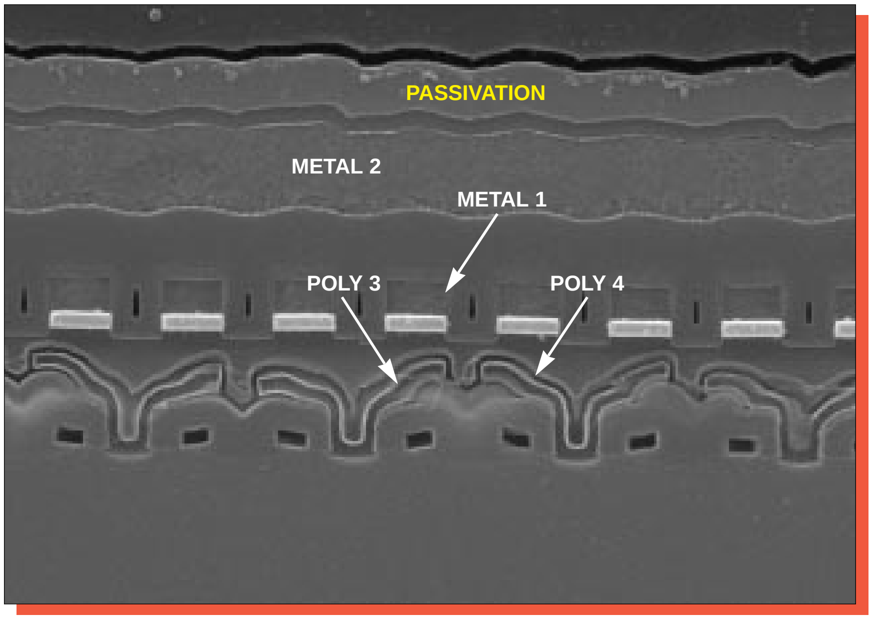
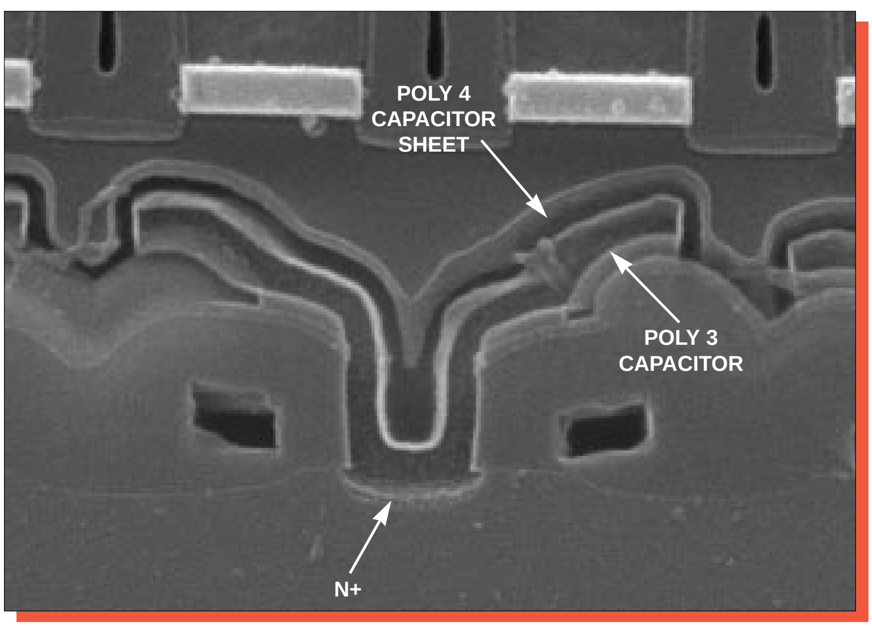


Figure 27. Detailed topological SEM views and schematic of the DRAM cell.

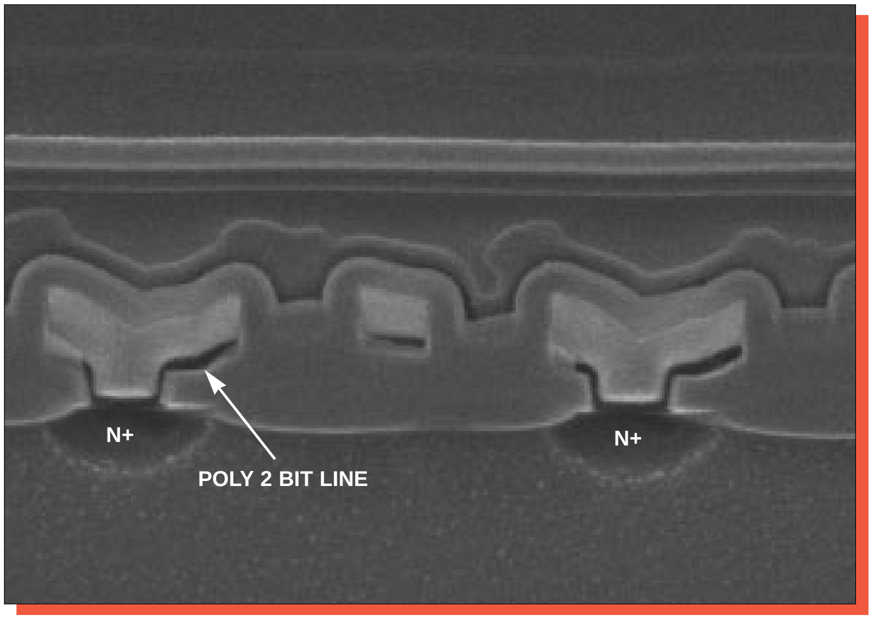


Mag. 13,000x

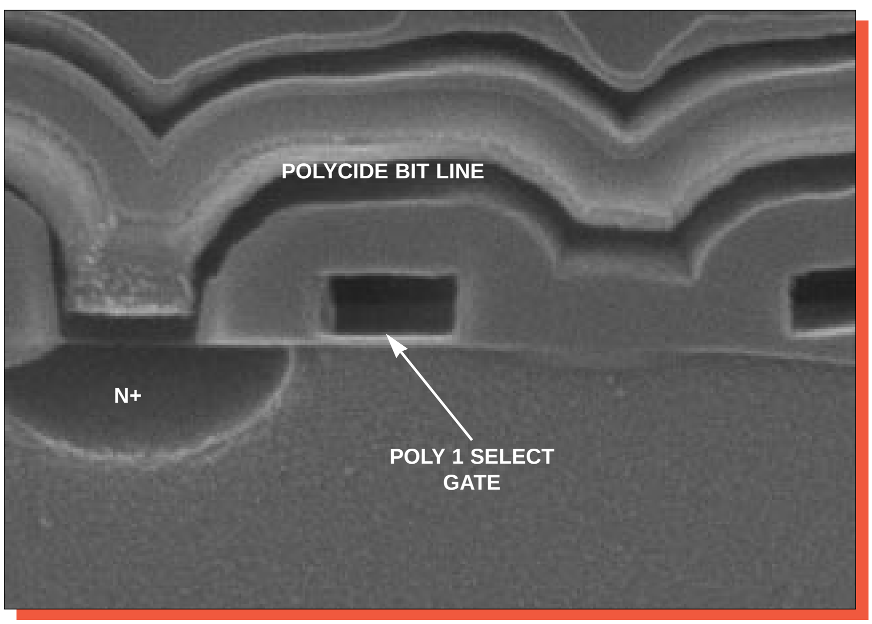


Mag. 40,000x

Figure 28. SEM section views of the DRAM cell array (parallel to bit line).

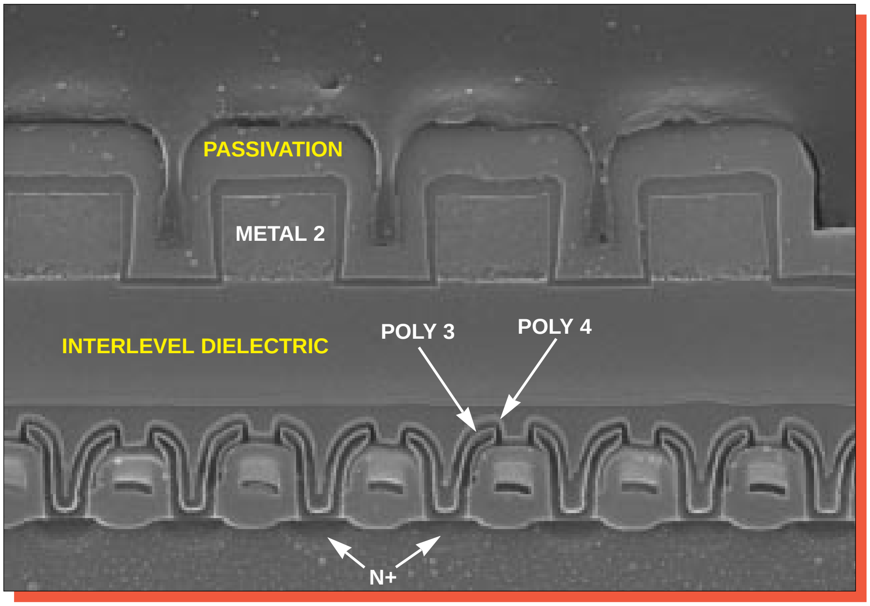


perpendicular to bitline, Mag. 26,000x

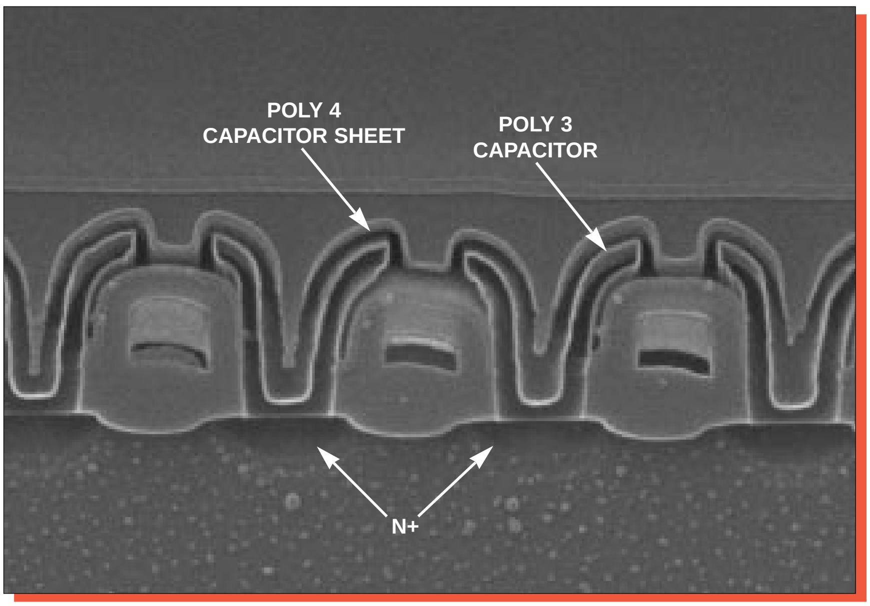


parallel to bitline, Mag. 52,000x

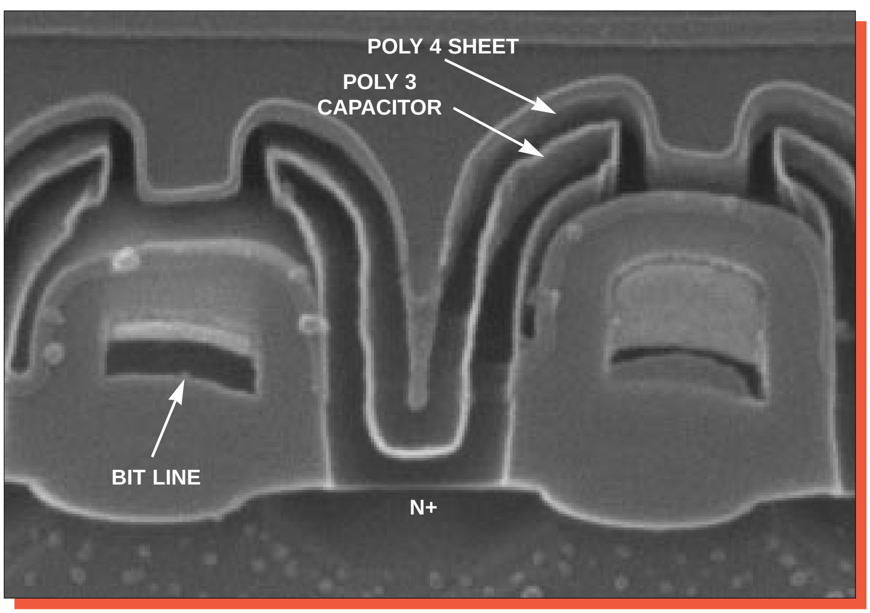
Figure 29. SEM section views of the bit line contact.



Mag. 13,000x

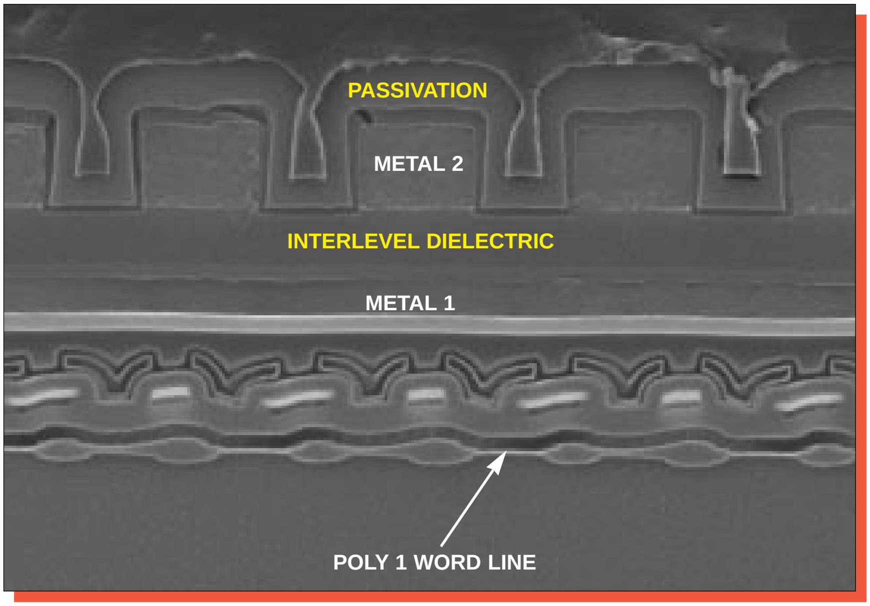


Mag. 26,000x

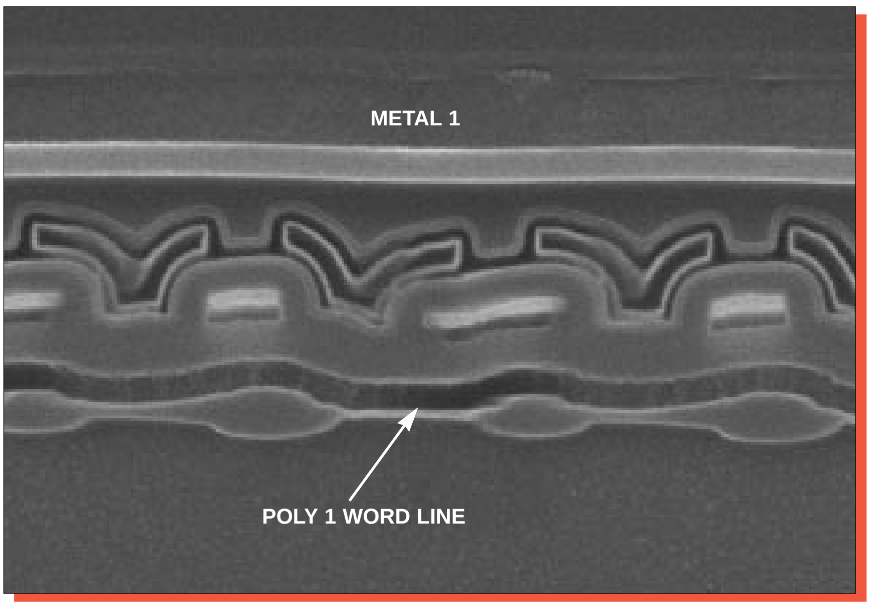


Mag. 52,000x

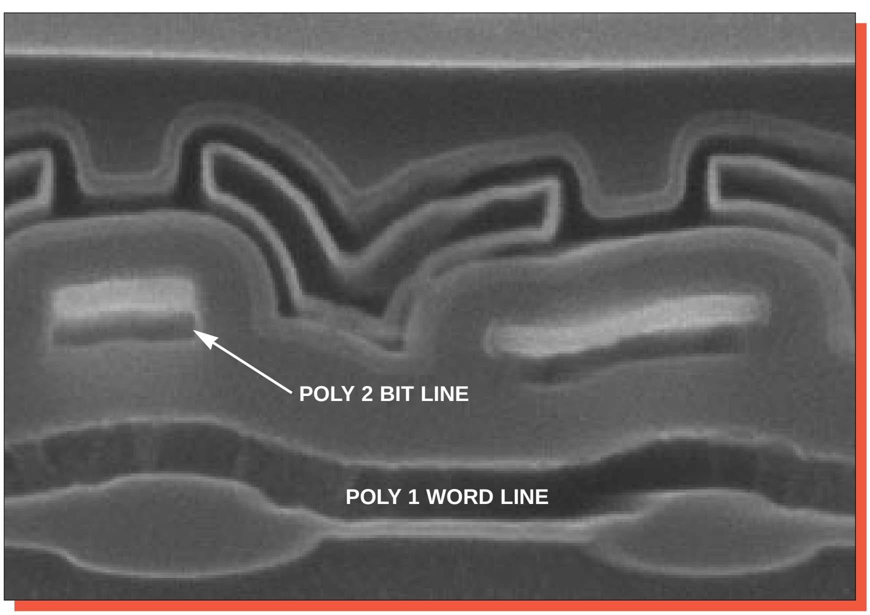
Figure 30. SEM section views of the DRAM cell array (perpendicular to bitline).



Mag. 13,000x

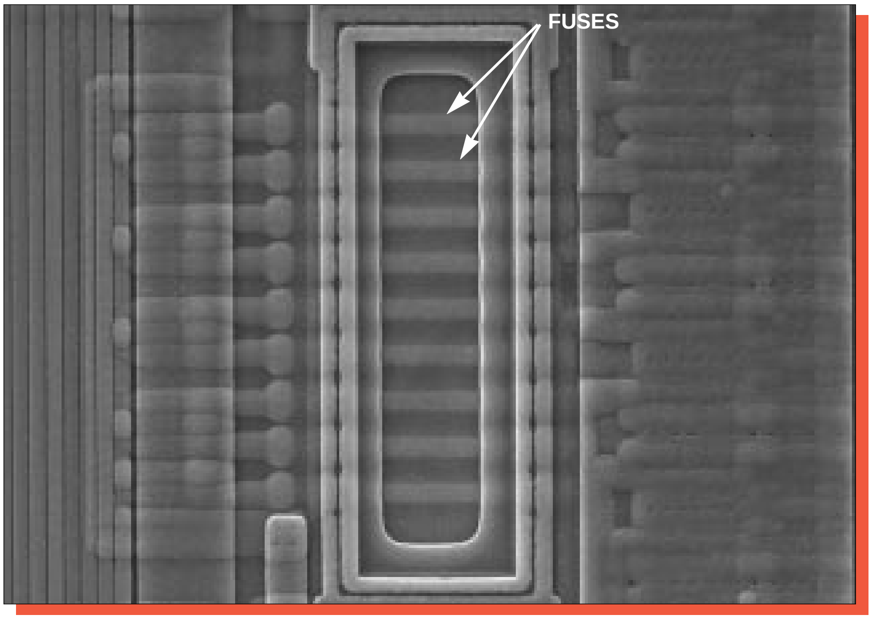


Mag. 26,000x

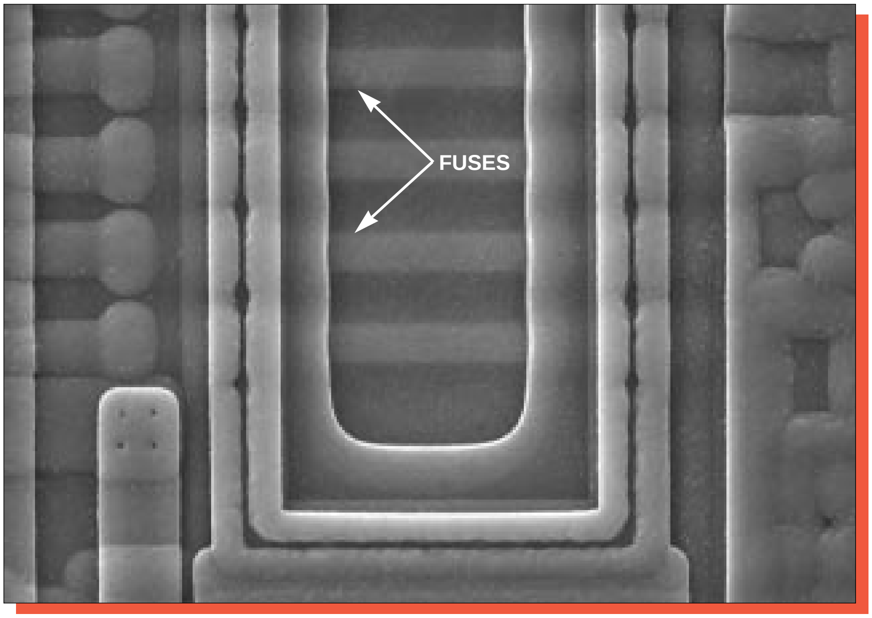


Mag. 52,000x

Figure 31. SEM section views of the DRAM cell array (perpendicular to bitline).

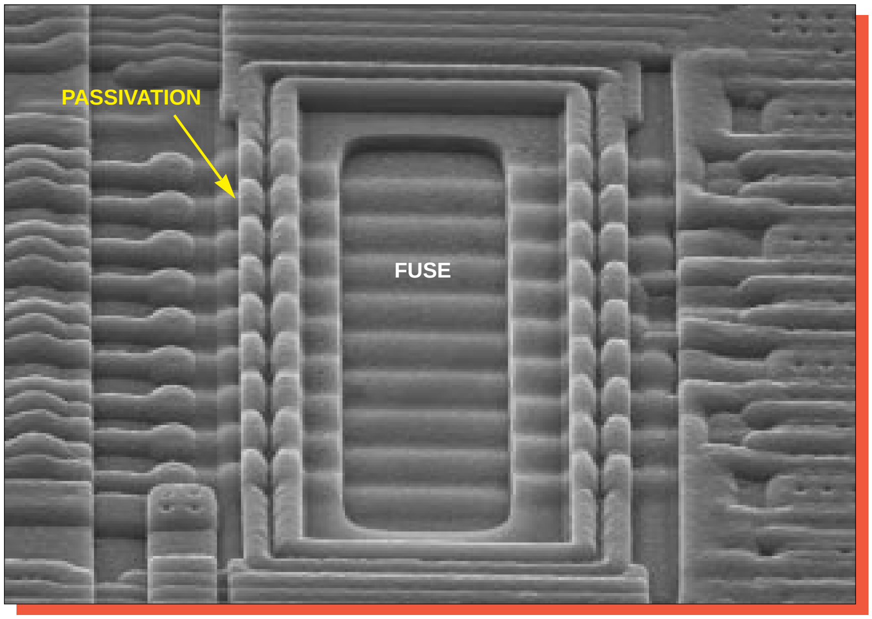


Mag. 1300x

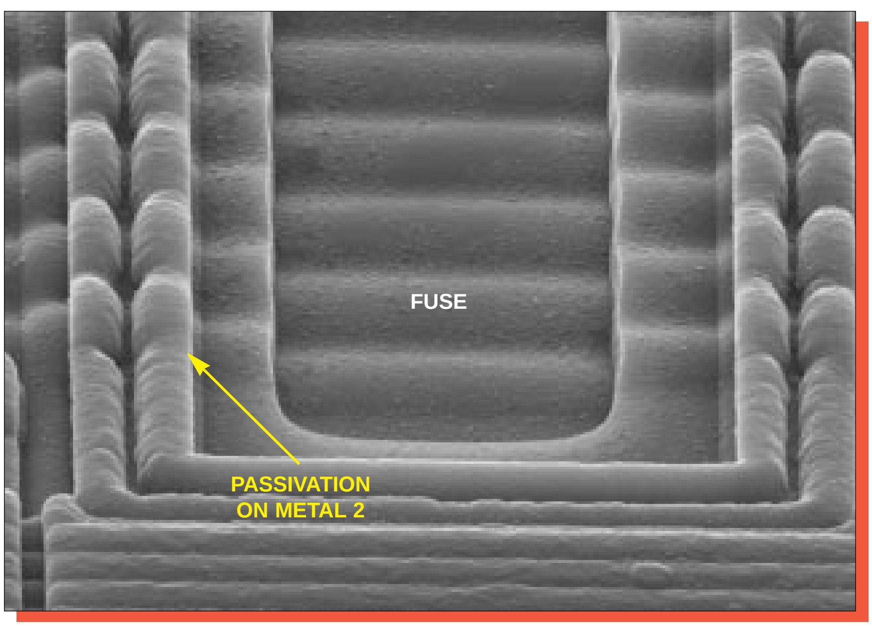


Mag. 2600x

Figure 32. Topological SEM views of typical fuses. 0°.

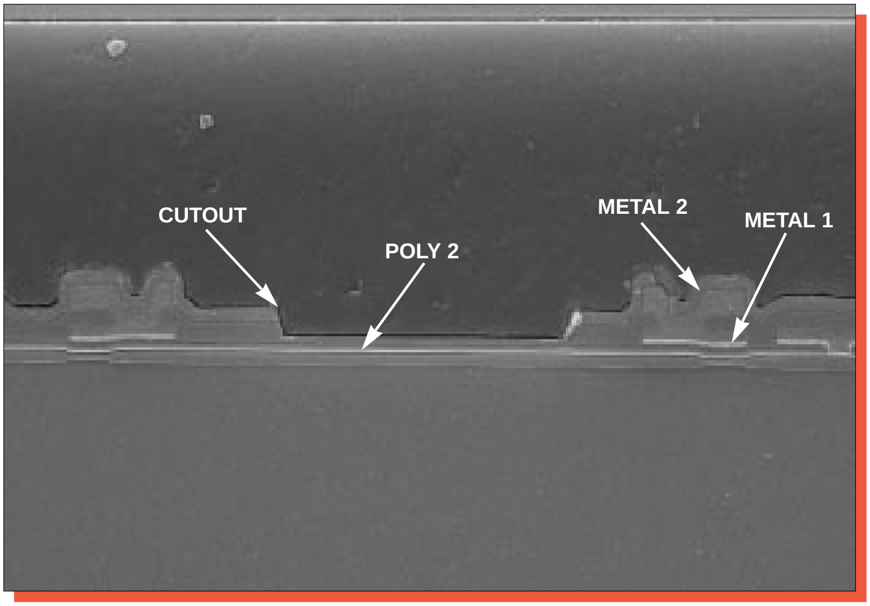


Mag. 2100x

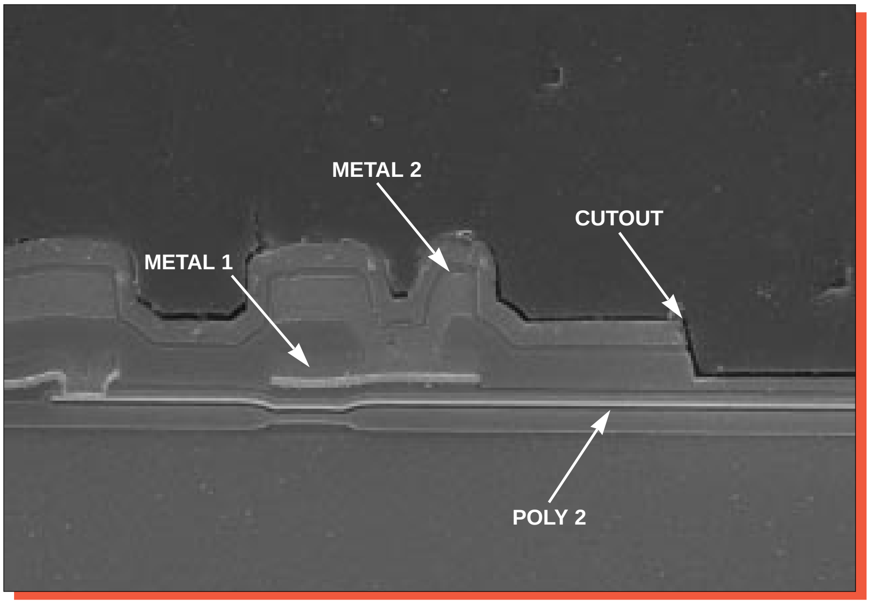


Mag. 4200x

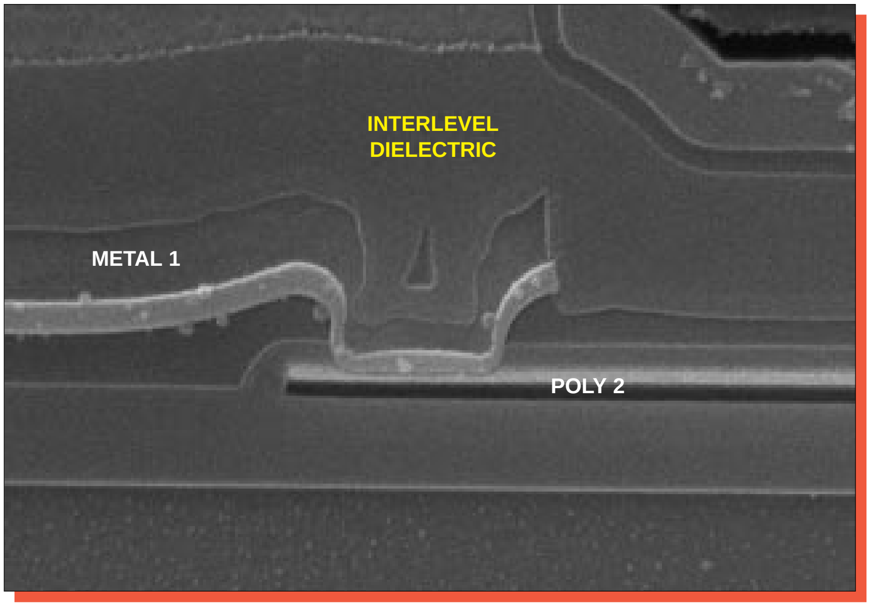
Figure 33. Perspective SEM views of typical fuses, 60°.



Mag. 3200x

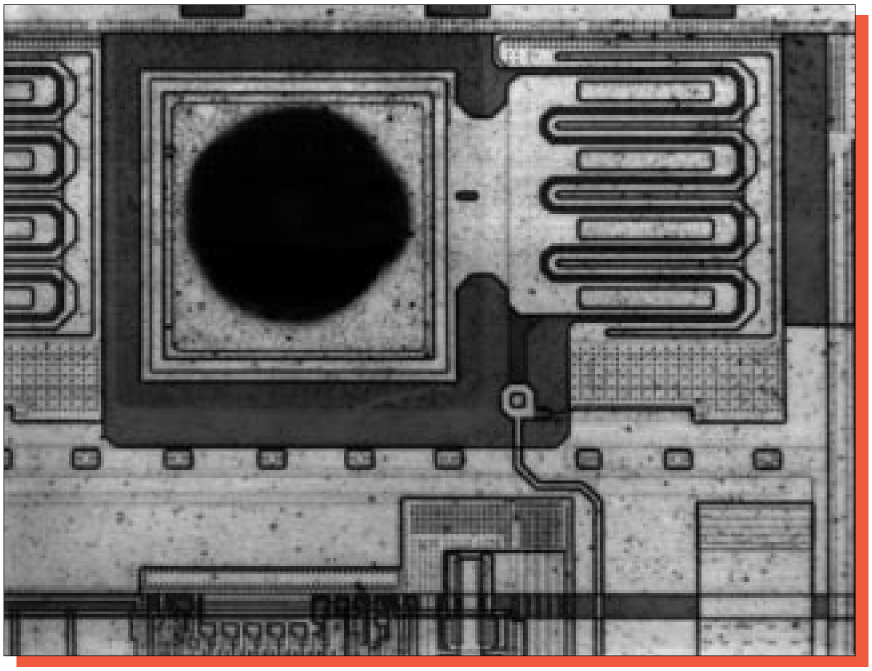


Mag. 6500x

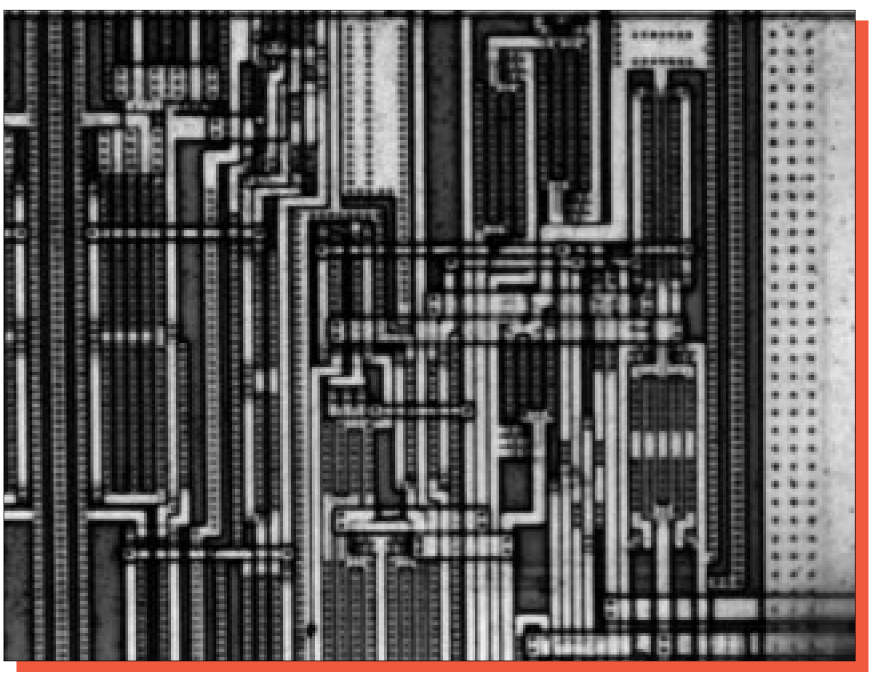


Mag. 26,000x

Figure 34. SEM section views of a typical fuse.



Mag. 320x



Mag. 800x

Figure 35. Optical views of I/O structure and general circuitry.

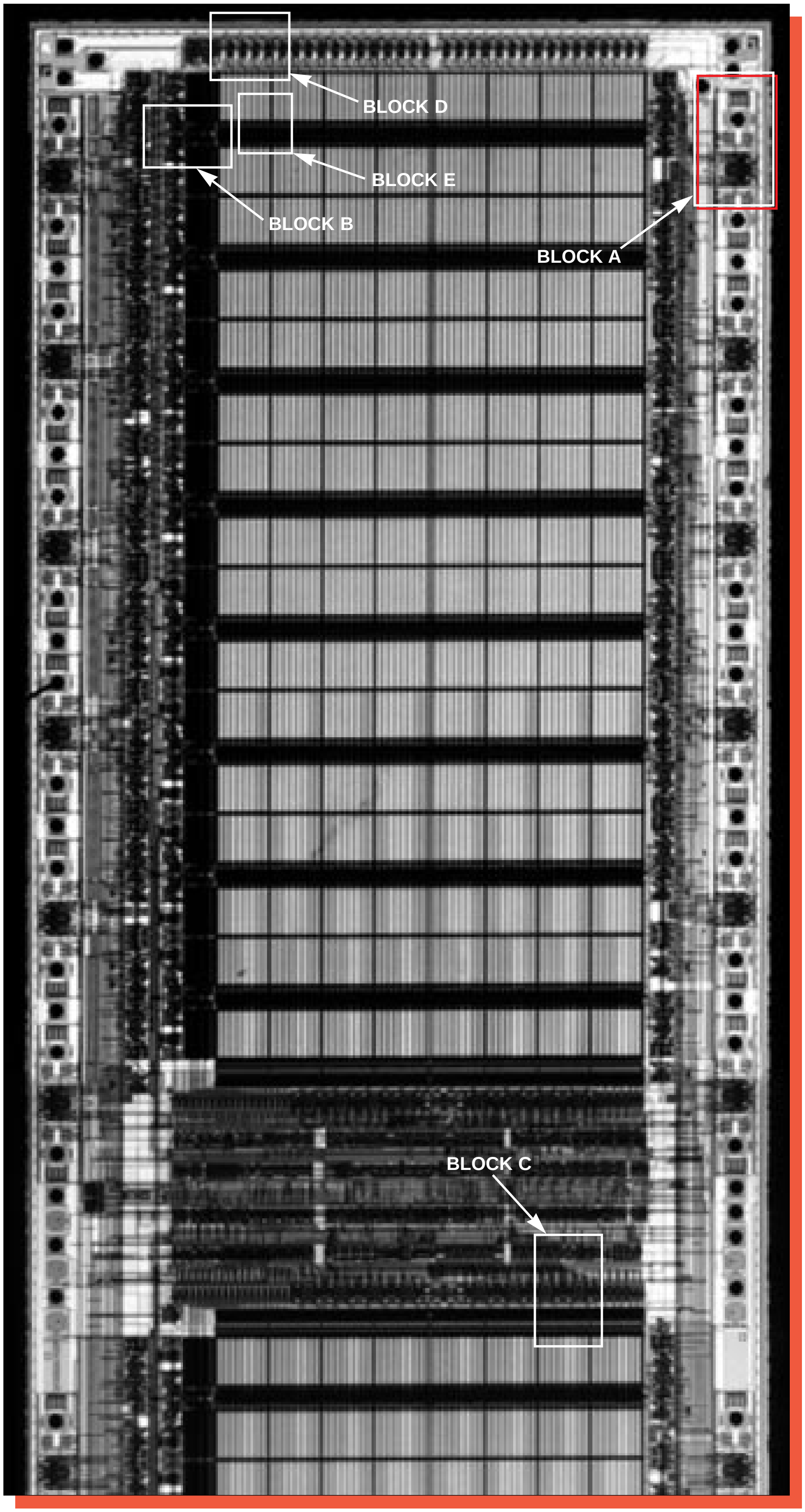


Figure 36. Portion of whole die illustrating locations of optical photographs. Mag. 21x.

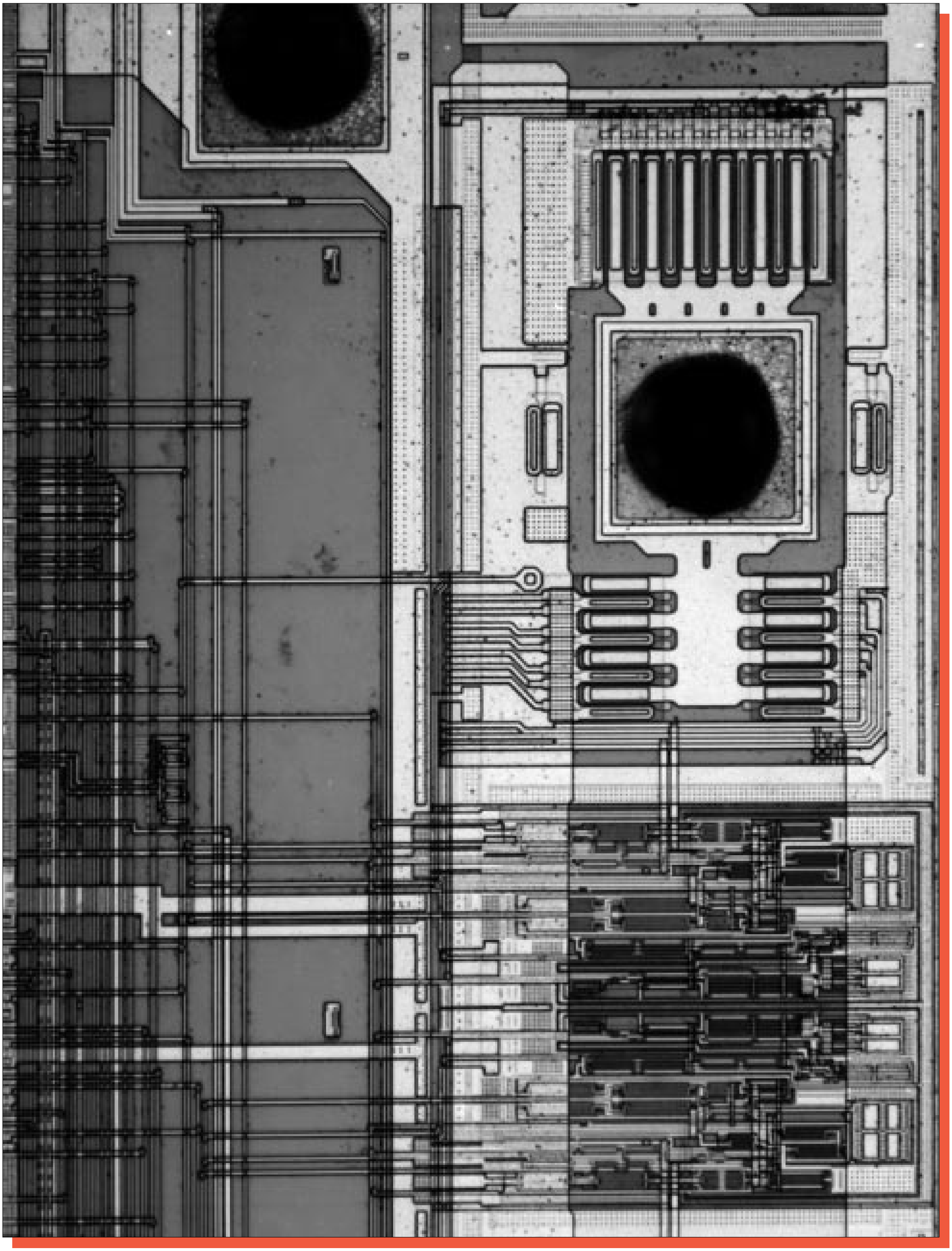


Figure 37. Optical view of Circuit Block A. Intact, Mag. 320x.

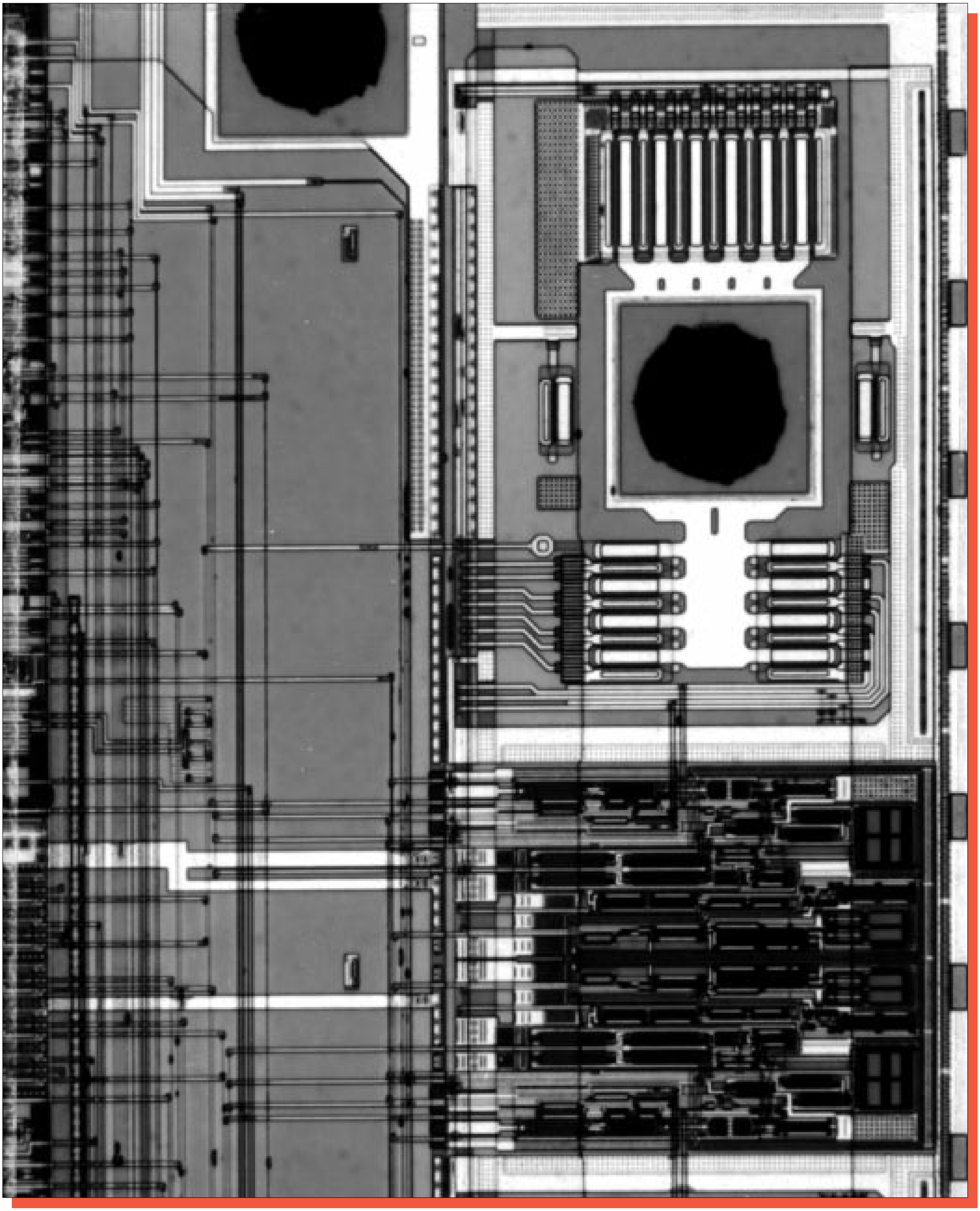


Figure 37a. Optical view of Circuit Block A. Metal 1, Mag. 320x.

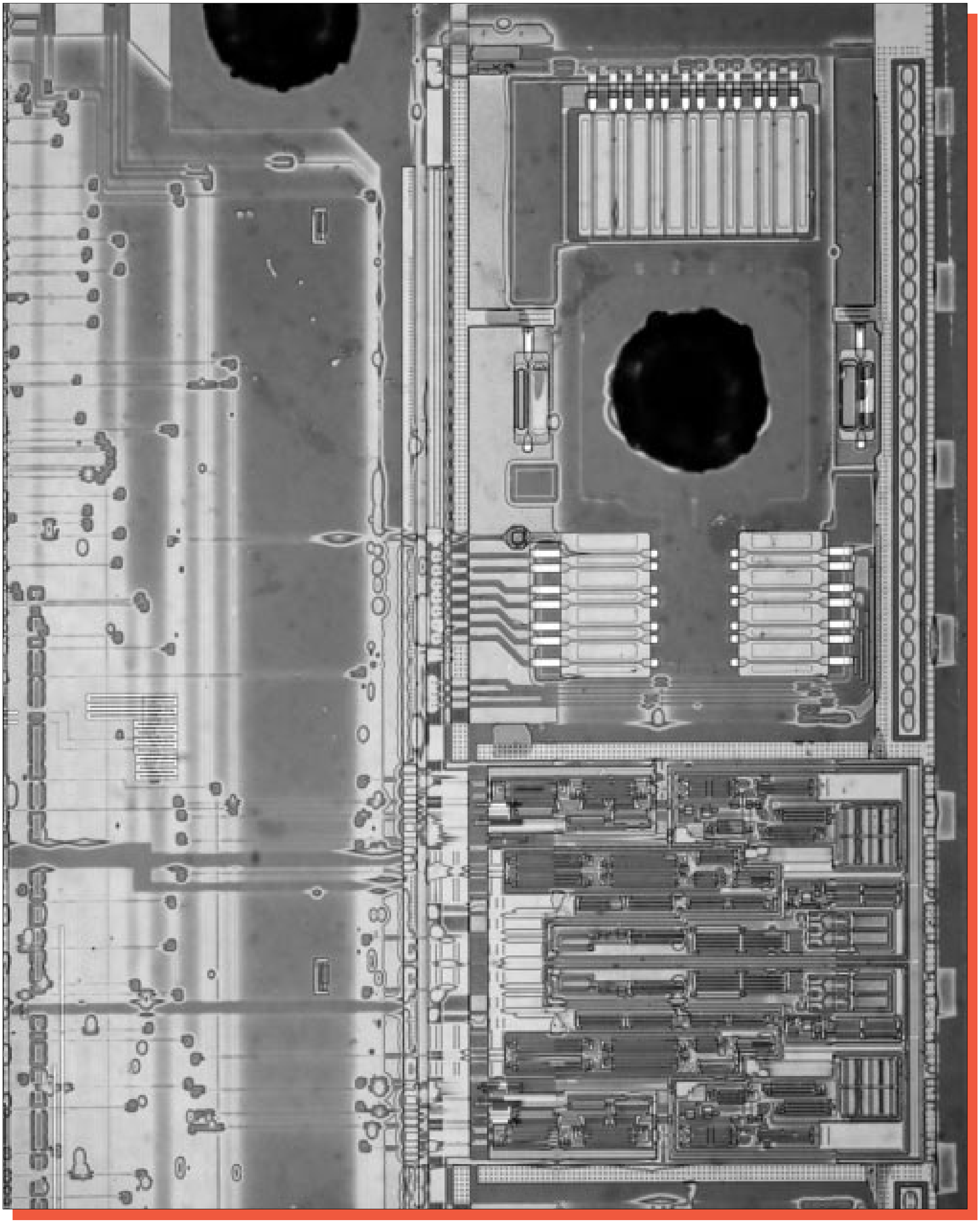


Figure 37b. Optical view of Circuit Block A. Unlayered, Mag. 320x.

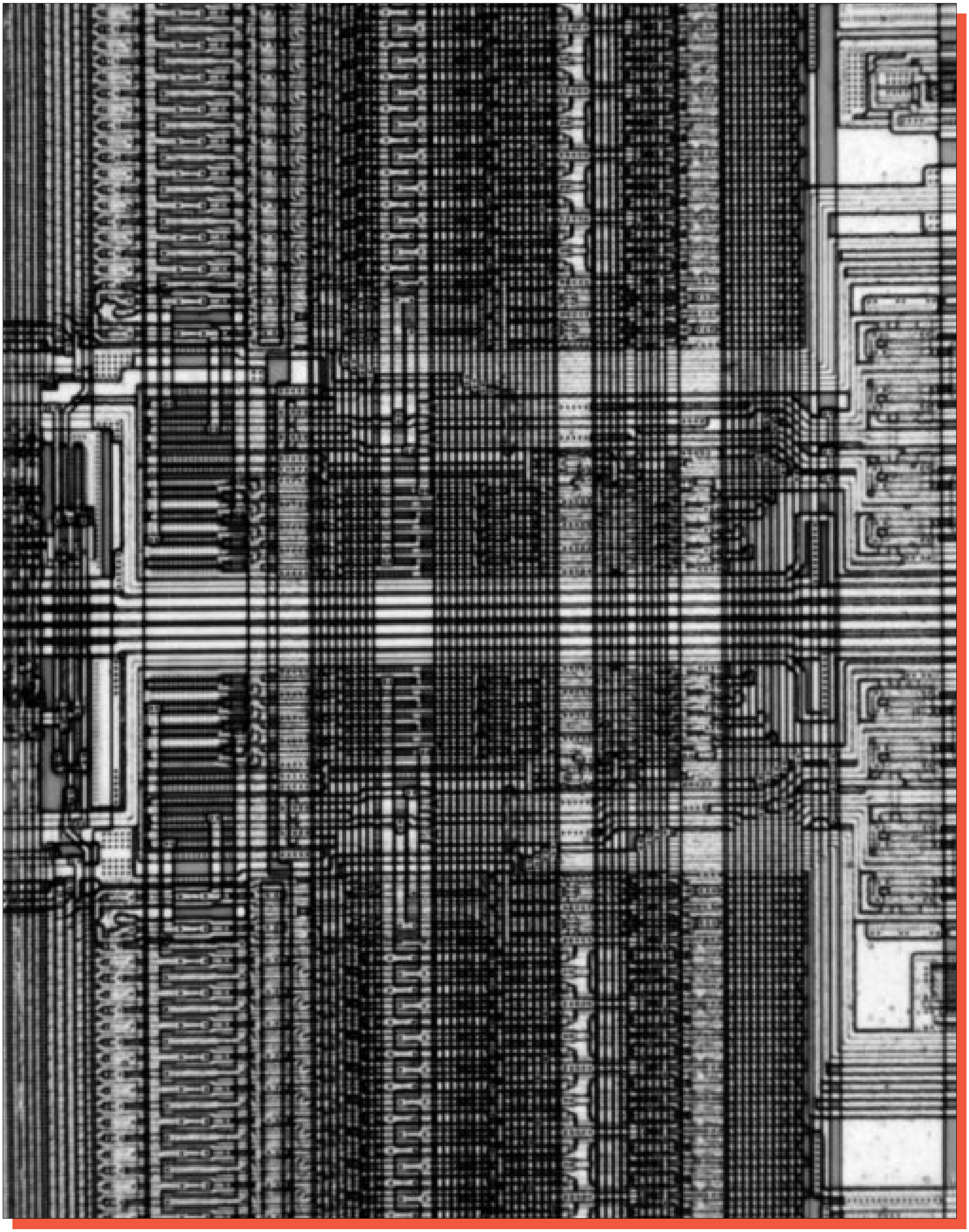


Figure 38. Optical view of Circuit Block B. Intact, Mag. 640x.

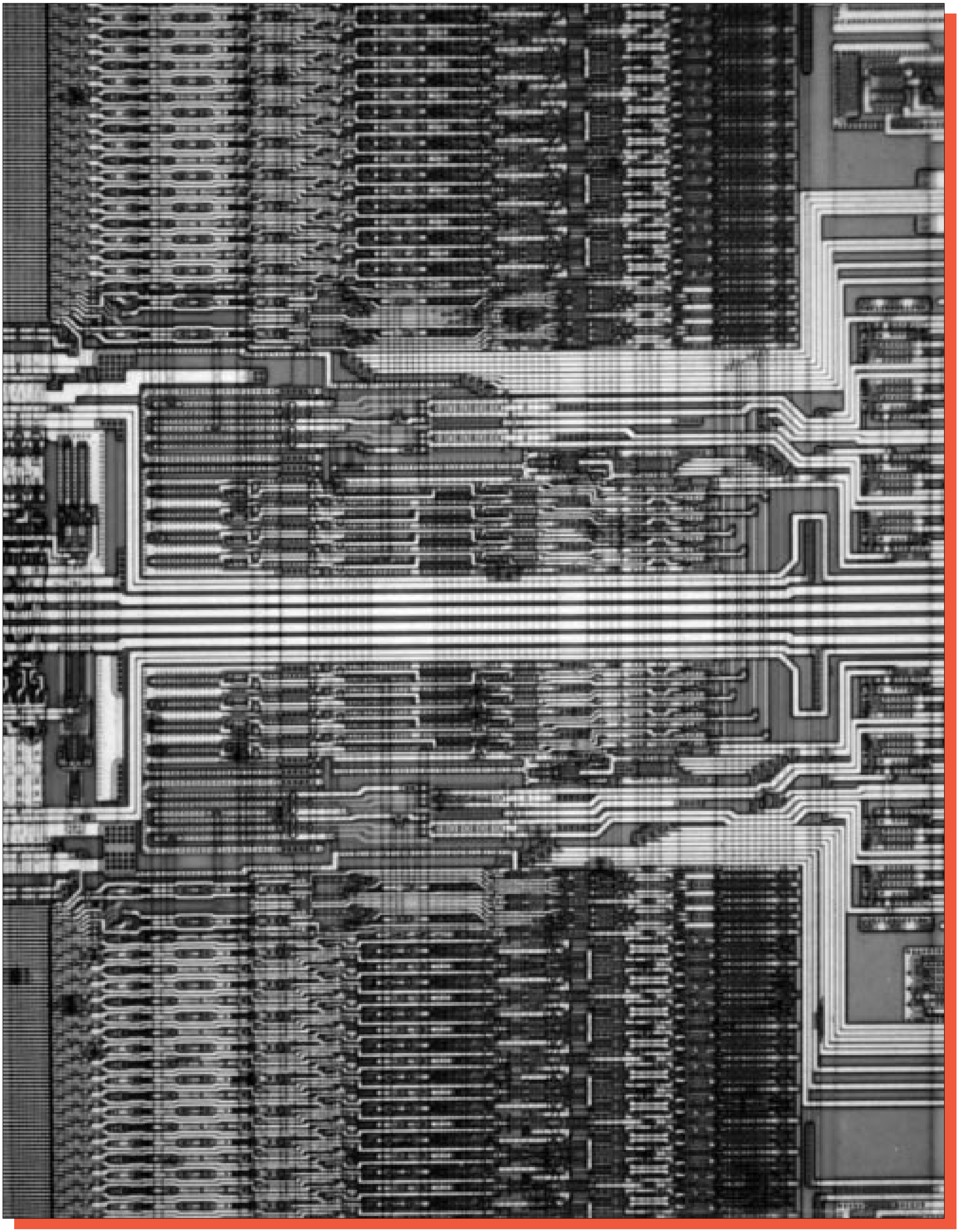


Figure 38a. Optical view of Circuit Block B. Metal 1, Mag. 640x.

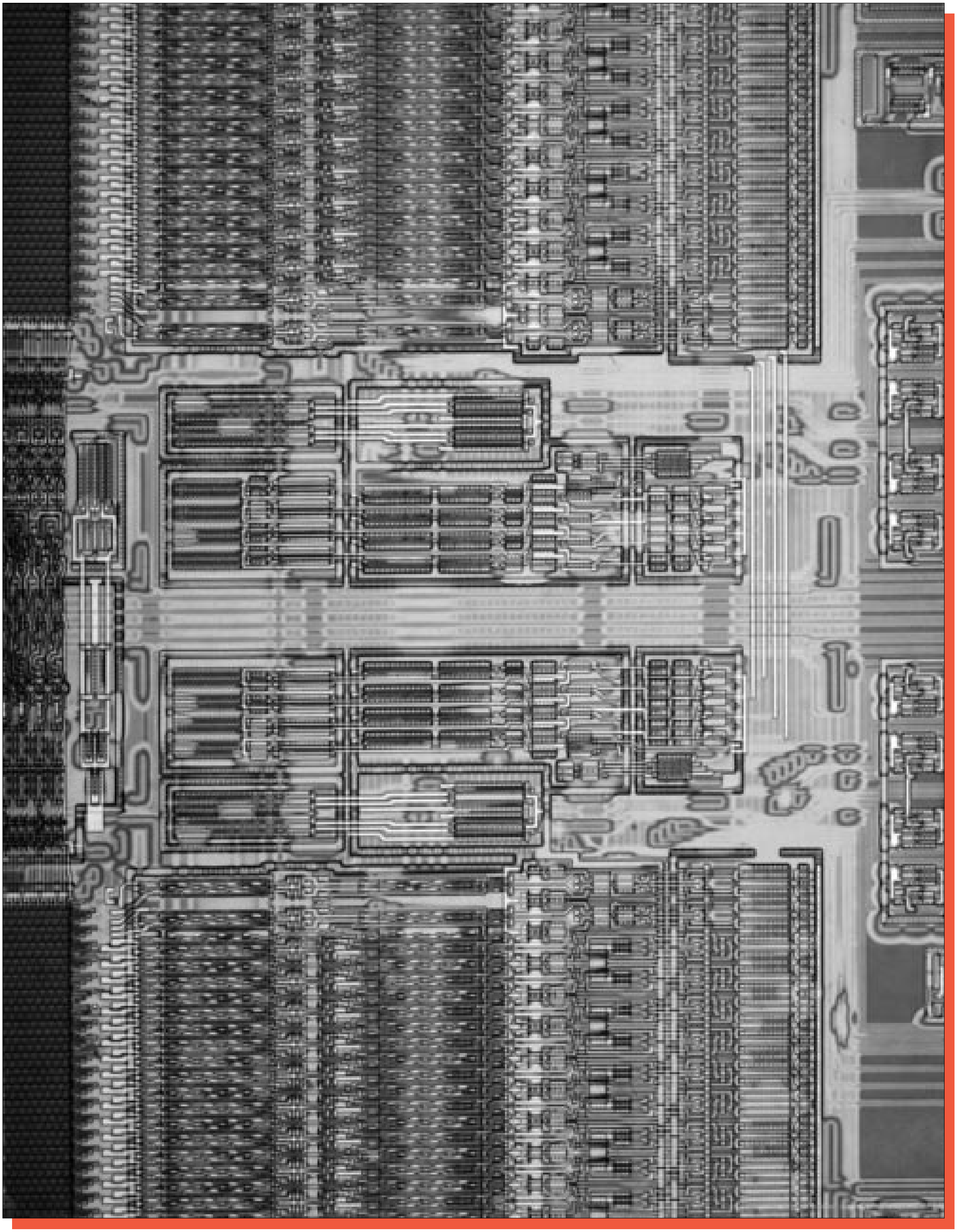


Figure 38b. Optical view of Circuit Block B. Unlayered, Mag. 640x.

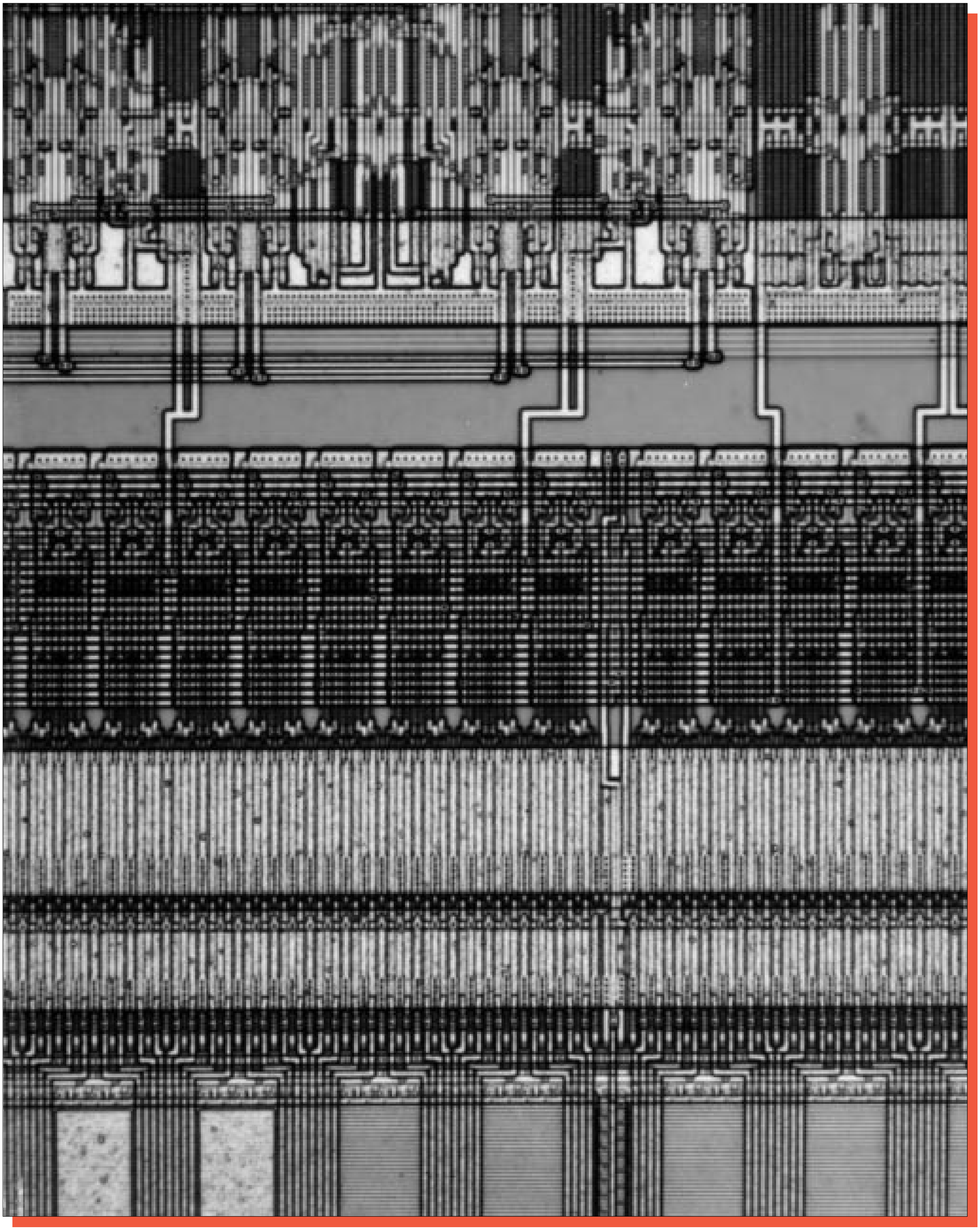


Figure 39. Optical view of Circuit Block C. Intact, Mag. 640x.

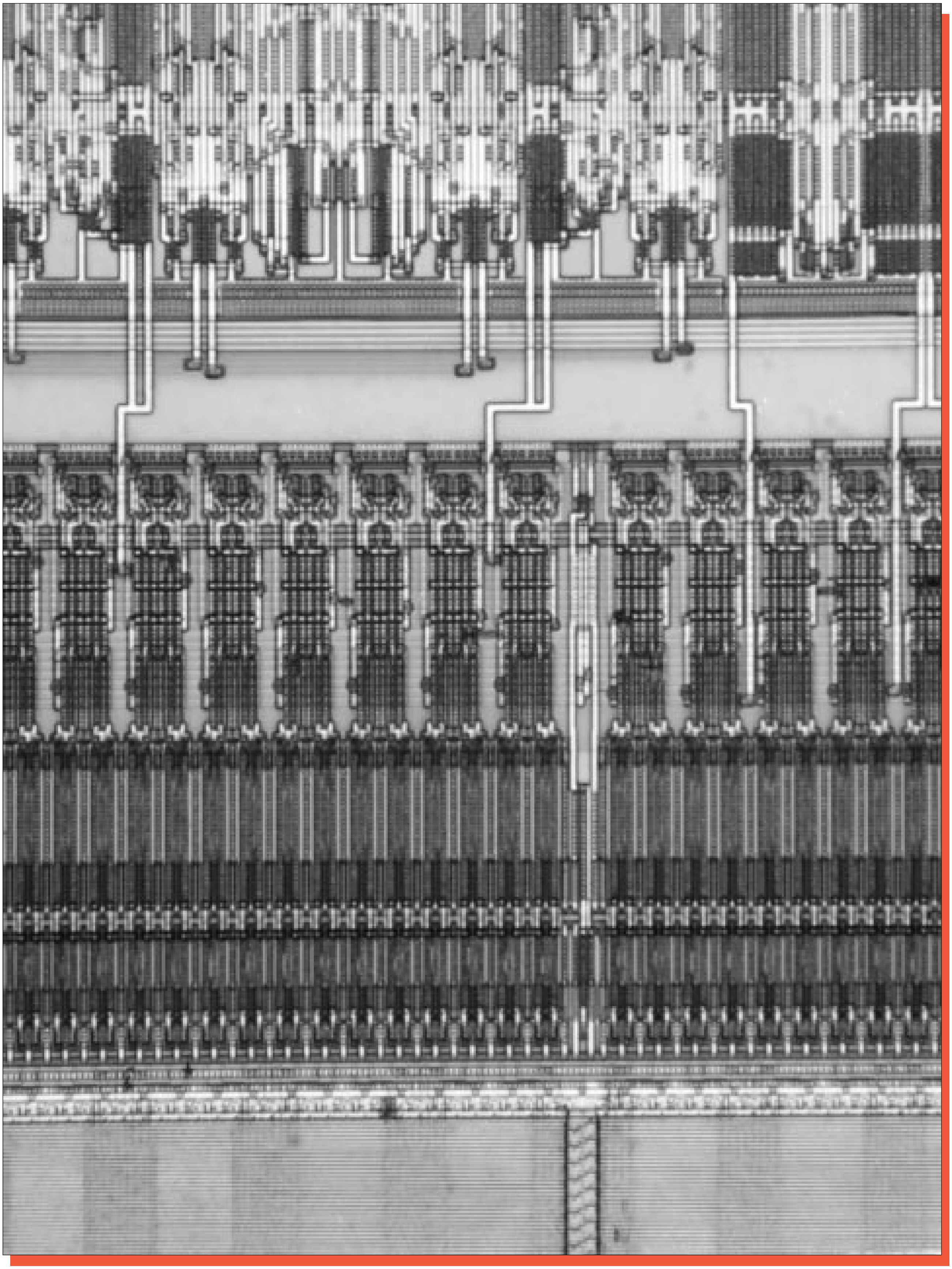


Figure 39a. Optical view of Circuit Block C. Metal 1, Mag. 640x.

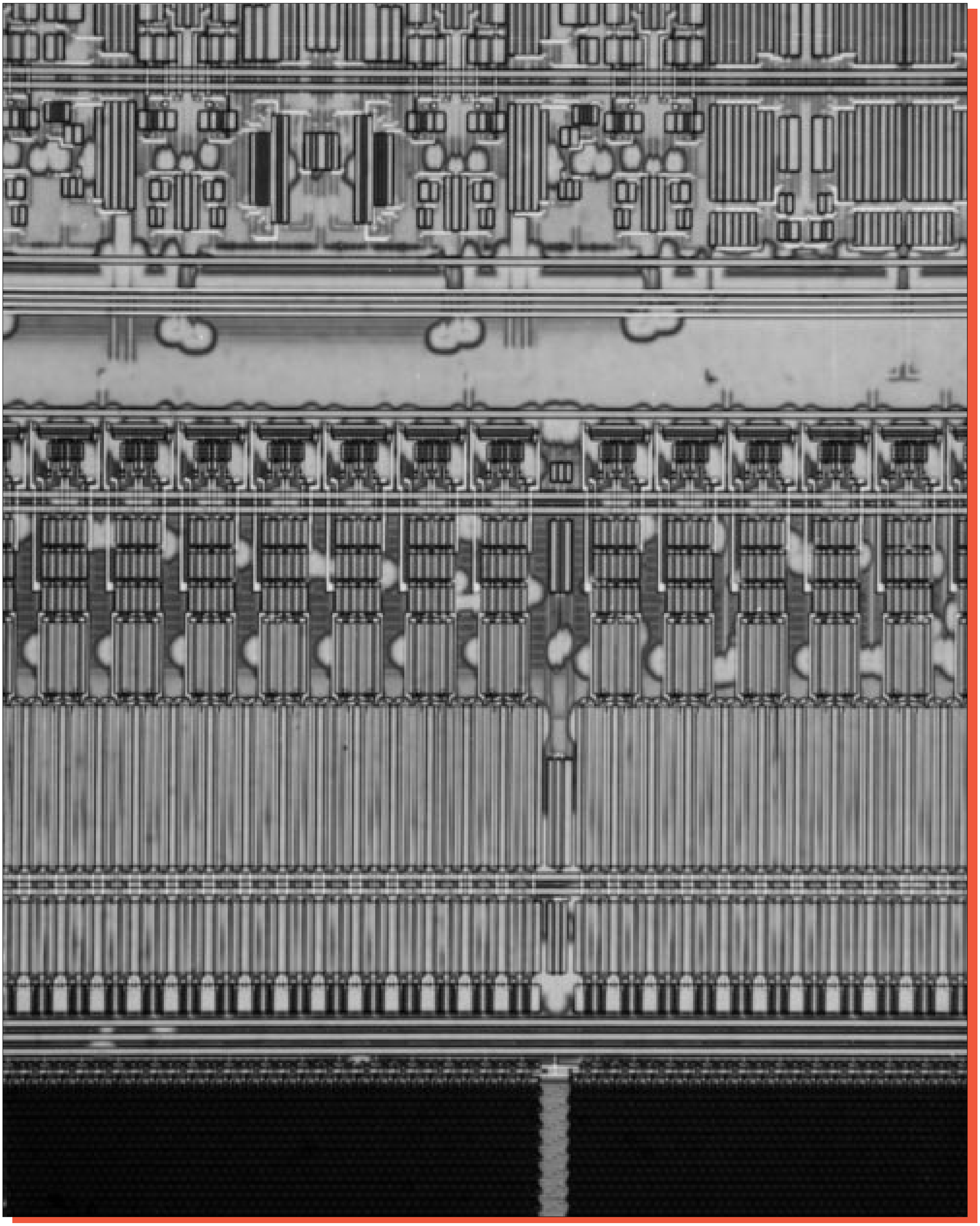


Figure 39b. Optical view of Circuit Block C. Unlayered, Mag. 640x.

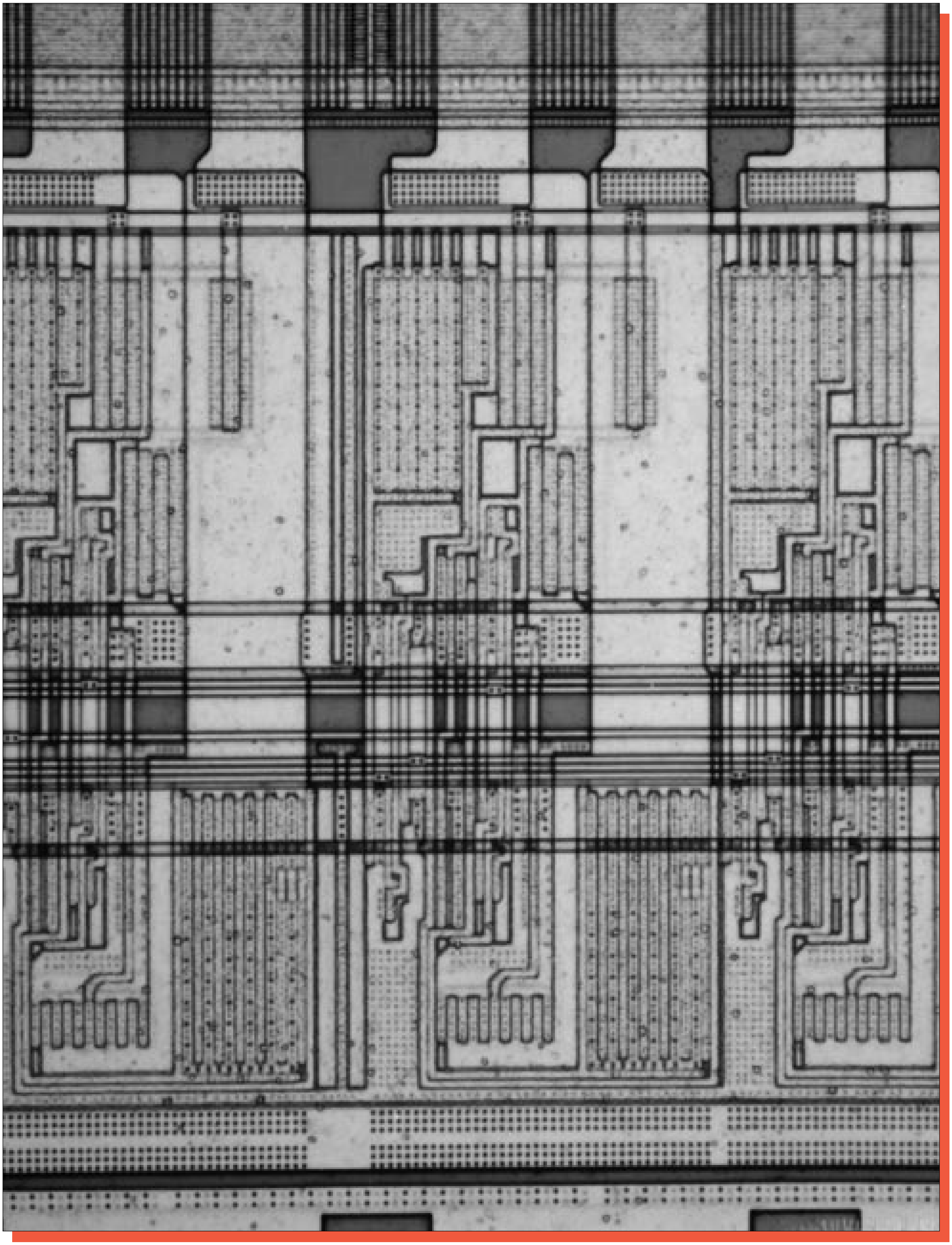


Figure 40. Optical view of Circuit Block D. Intact, Mag. 800x.

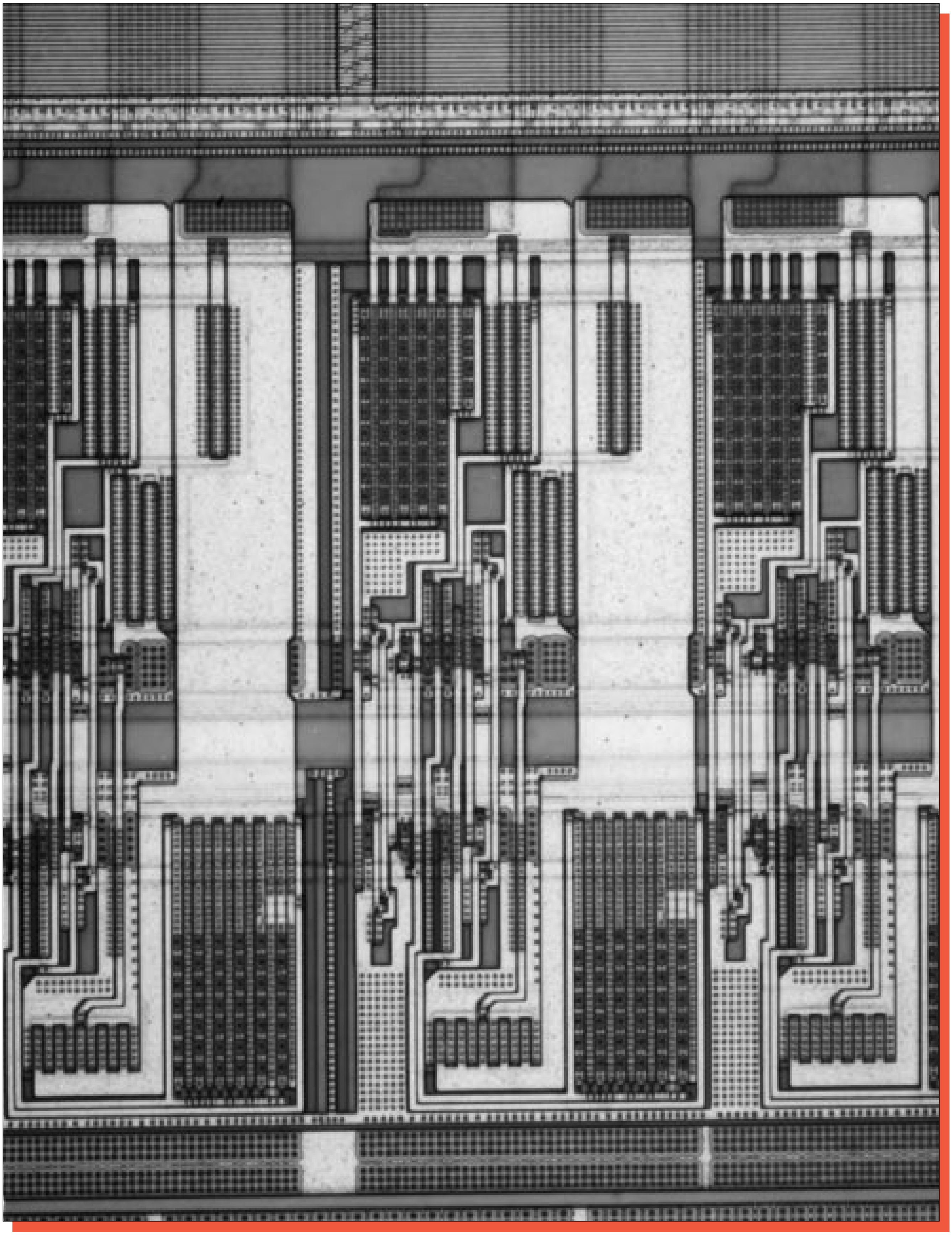


Figure 40a. Optical view of Circuit Block D. Metal 1, Mag. 800x.

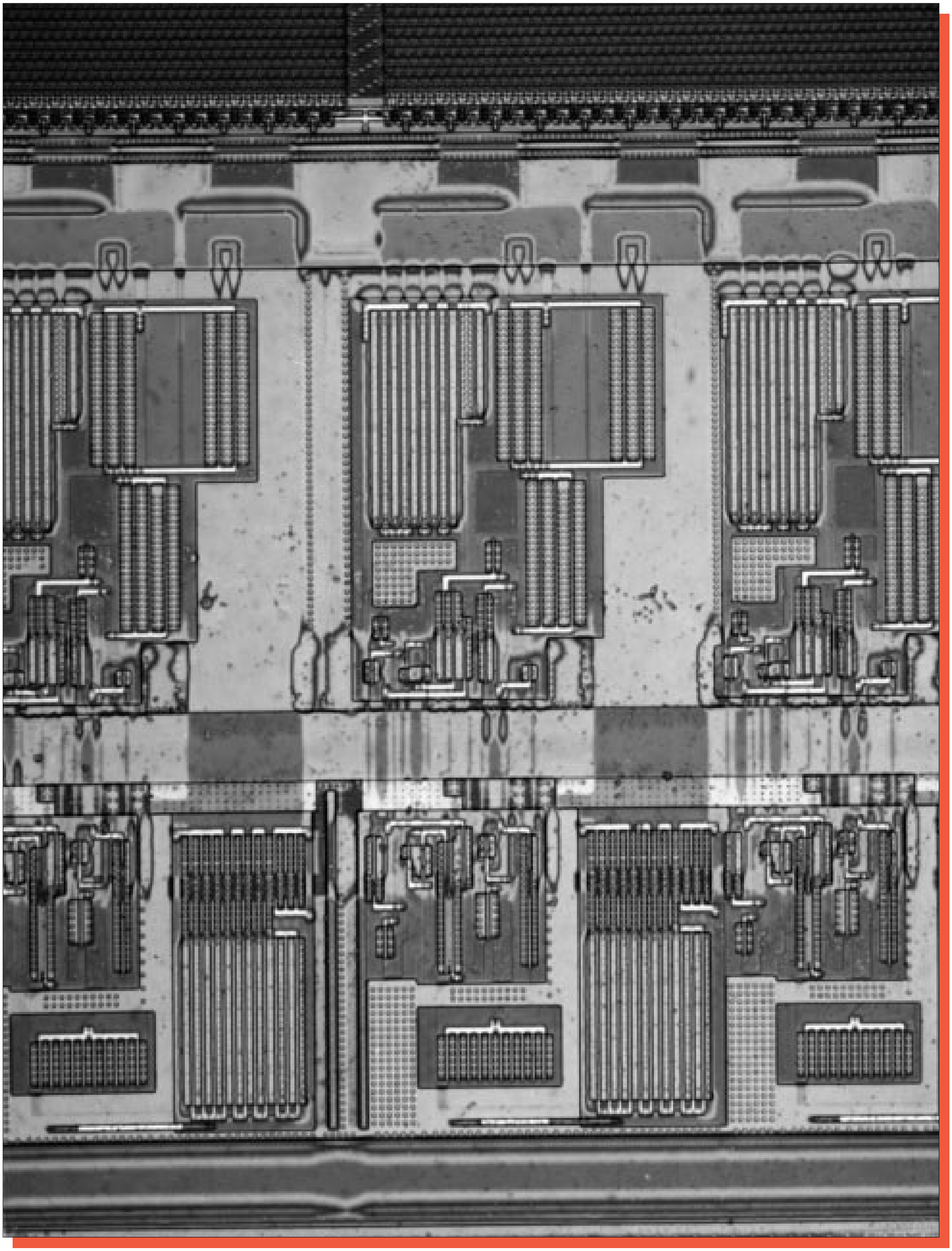


Figure 40b. Optical view of Circuit Block D. Unlayered, Mag. 800x.

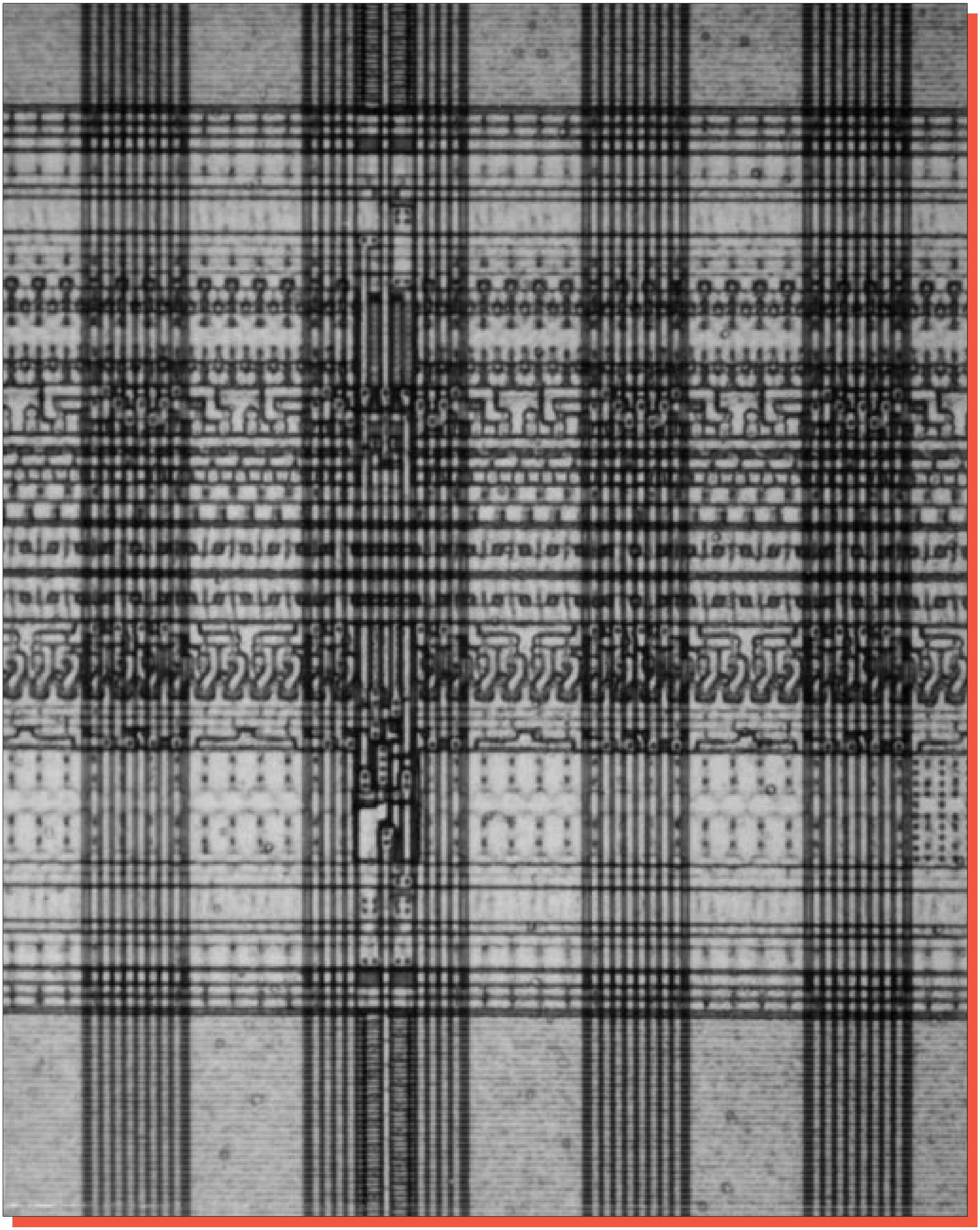


Figure 41. Optical view of Circuit Block E. Intact, Mag. 1000x.

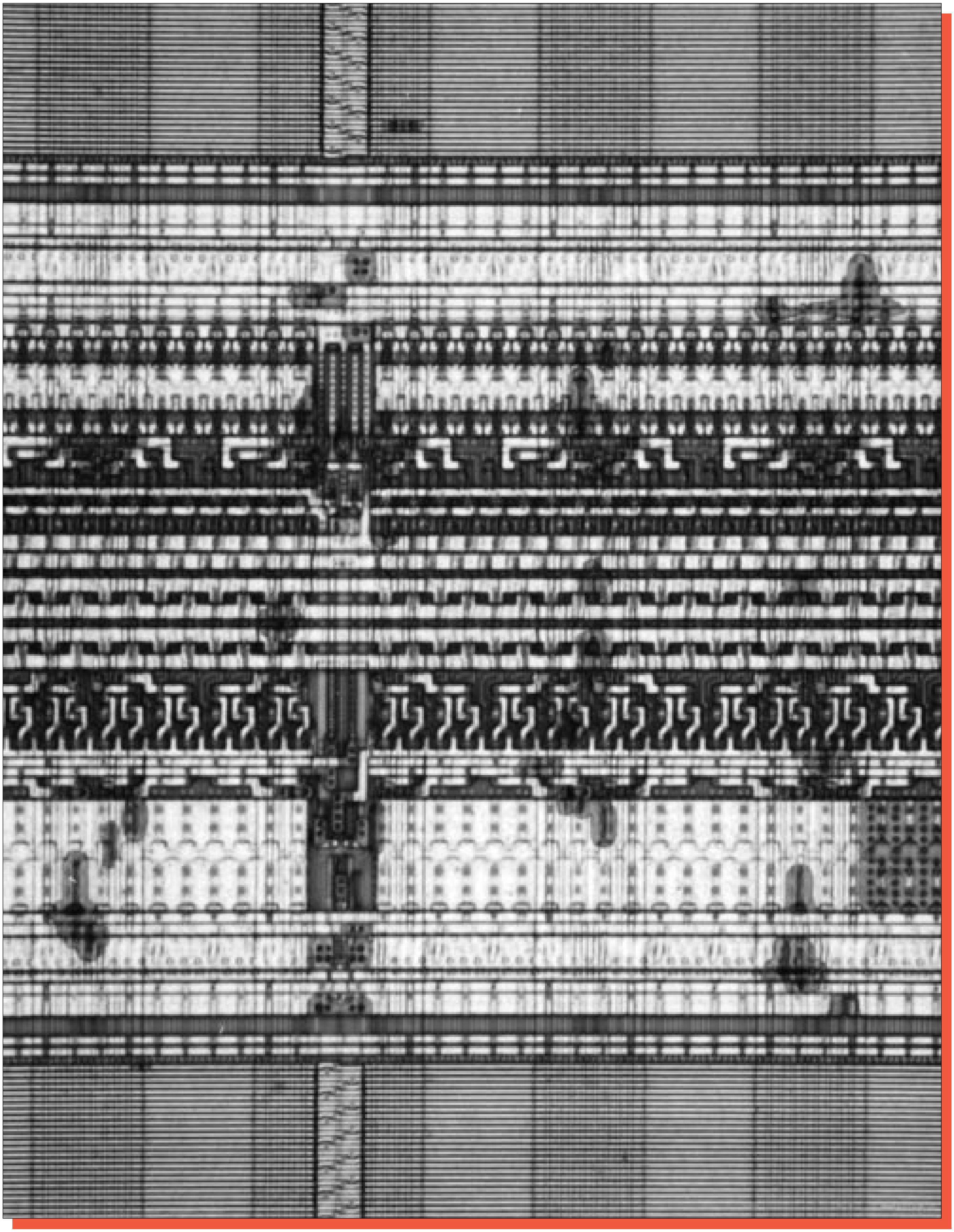


Figure 41a. Optical view of Circuit Block E. Metal 1, Mag. 1000x.

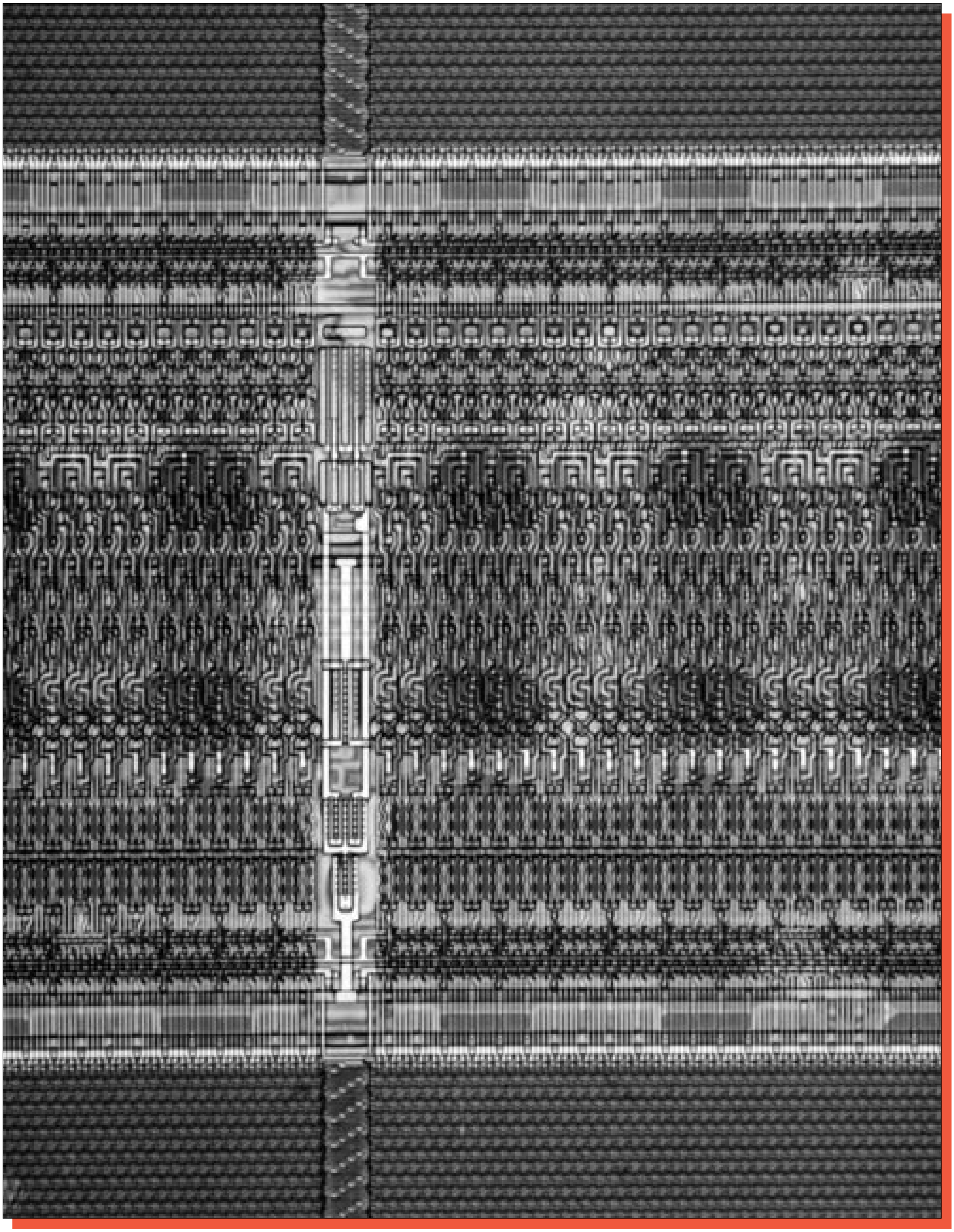


Figure 41b. Optical view of Circuit Block E. Unlayered, Mag. 1000x.