Construction Analysis

AMD MACH5 256 PLD

Report Number: SCA 9702-527

INTEGRATED CIRCUIT ENGINEERING

15022 N. 75th Street
Scottsdale, AZ 85270-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: http://www.ice-corp.com/ice

INDEX TO TEXT

INTRODUCTION

This report describes a construction analysis of the AMD MACH5 256 macrocell device. One decapsulated device was supplied for the analysis.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 2 aluminum thinning up to 85 percent[2] at some via edges (Figure 11). With the addition of the barrier metal overall metal thinning was 80 percent.

Special Features:

- Sixteen blocks of EEPROM memory arrays were employed on the device.

- Titanium silicide present over all diffusions (salicide process).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Die Process and Design

- Fabrication process: Device was fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was present.

- Die coat: No die coat was present.

- Final passivation: Consisted of three layers. A layer of nitride over a layer of spin-on-glass (SOG) to aid in planarization, over the first layer of silicon-dioxide.

- Metallization: Two levels of metal defined by dry-etch techniques. Both metal layers consisted of aluminum. Metal 2 did not use a cap, but did employ a titanium barrier. Metal 1 employed a titanium-nitride cap and barrier on a titanium adhesion layer. Metal 2 employed standard vias. Metal 1 contacts were formed with tungsten plugs.

- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of two layers of glass with a spin-on glass (SOG) between to aid in planarization. The SOG and first layer of glass had been subjected to an etchback.

- Pre-metal dielectric: A single layer of BPSG (borophosphosilicate glass) over a layered deposited glass over densified oxides. The layered glass had been planarized by RIE back etching.

- Polysilicon: A single layer of polycide (no silicide) was used to form all gates on the die, the word lines and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Definition of the poly was by a dry etch.

TECHNOLOGY DESCRIPTION (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used and were left in place. A layer of sintered titanium was present over all diffusions (salicide process).

- Local oxide (LOCOS) isolation was used. No step was noted in the oxide at the edge of the well boundaries.

- Wells: Twin-wells in a P substrate. The P-well could not be delineated in cross section but its presence is assumed from the N-well edge profiles. No epi was used.

- The memory cell consisted of a three transistor, one tunnel oxide device, single capacitor, EEPROM design. Metal 1 was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor and the tunnel-oxide device. A tunnel oxide "window" was present under the program gate.

- Redundancy fuses were not present.

ANALYSIS RESULTS

Die Process and Design: **Figures 5 - 42**

Questionable Items:[1]

- Metal 2 aluminum thinning up to 85 percent[2] at some via edges (Figure 11). With the addition of the barrier metal, overall metal thinning was 80 percent.

Special Features:

- Sixteen blocks of EEPROM memory arrays were employed on the device.

- Titanium silicide present on all diffusions.

General Items:

- Fabrication process: The device was fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was present. No significant problems were found in the basic process.

- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Final passivation: Consisted of three layers, a layer of nitride over a layer of spin-on-glass (SOG) for planarization over the first layer of silicon-dioxide. Passivation integrity tests indicated defect-free passivation. Edge seal was also good leaving no exposed metal.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS (continued)

- Metallization: Two levels of metal defined by dry-etch techniques. Both metal layers consisted of aluminum. Metal 2 did not use a cap, but did employ a titanium barrier. Metal 1 employed a titanium-nitride cap and barrier on a titanium adhesion layer. Metal 2 employed standard vias. Metal 1 contacts were formed with tungsten plugs. Beveled and slotted metal lines were present at each die corner. Metal 1 employed large contact arrays.

- Metal patterning: Both metals were defined by a dry etch of normal quality. No problems were found.

- Metal defects: No notching or voiding was found. No silicon nodules were found following the removal of the aluminum layers.

- Metal step coverage: Metal 2 aluminum thinned up to 85 percent at some vias (Figure 11). With the addition of the barrier metal, overall metal thinning was 80 percent. MIL-STD-883D allows up to 70 percent metal thinning for vias of this size. No thinning of metal 1 was present due to the use of tungsten plugs.

- Vias and plugs: Vias were defined by a two step process while contacts were defined by a single dry-etch. No significant over-etching was found. Voids were noted in the center of tungsten plugs but no problems are foreseen (Figures 15, 17 and 17a).

- Intermetal dielectric: Intermetal dielectric (between M2 and M1) consisted of two layers of glass with a spin-on glass (SOG) between to aid in planarization. The SOG and first layer of glass had been subjected to etchbacks. No problems were found in this area.

- Pre-metal dielectric: A single layer of BPSG (borophosphosilicate glass) over multi-layer deposited glass over densified oxides. The multi-layered glass had been subjected to a substantial RIE (?) planarizing etch. No problems were found.

ANALYSIS RESULTS (continued)

- Polysilicon: A single layer of polycide (Ti silicide) was used to form all gates on the die, the word lines and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Long and patterned poly interconnect lines are used (Figure 20a) as well as special patterned gates and capacitors (Figure 21a). Definition of the poly was by a dry etch. No problems were found.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. No step was noted in the local oxide at the well boundaries.

- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used on all gates and were left in place. There was a faint indication of a light implant under the capacitor regions in the EEPROM array. A layer of titanium was present over all diffusions (salicide process). No problems were found in any of these areas.

- Wells: Twin-wells used in a P substrate (no epi). Definition of the N-wells was normal and the edge profiles indicated P-wells were also present although they could not be delineated in cross section.

- Memory cells: The memory cell consisted of a three transistor, single capacitor, and tunnel oxide device EEPROM design. Metal 1 was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor and the program device which employed an oval tunnel-oxide window. No problems were apparent in the cell arrays.

PROCEDURE

The device was subjected to the following analysis procedures:

Optical inspection

Passivation integrity test

Passivation removal and inspect metal 2

Aluminum 2 removal and inspect barrier

Delayer to metal 1 and inspect

Aluminum 1 removal and inspect barrier

Delayer and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Dicing method	Sawn (full depth)
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Contact registration	G

**85 percent aluminum 2 thinning at vias.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MATERIALS

Passivation:	Nitride over SOG over a layer of silicon-dioxide.
Metal 2 - body:	Aluminum
- barrier:	Titanium
Metal 1 - cap:	Titanium-nitride
- body:	Aluminum
- barrier:	Titanium-nitride
- adhesion layer:	Titanium
Pre-metal dielectric:	Borophosphosilicate glass (BPSG) over a layered deposited glass over densified oxides.
Salicide:	Titanium-silicide

HORIZONTAL DIMENSIONS

Die size:	8.5 x 8.7 mm (338 x 344 mils)
Die area:	73.9 mm^2 (116,272 $mils^2$)
Min metal 2 width:	1.4 micron
Min metal 2 space:	1.1 micron
Min metal 2 pitch:	2.5 microns
Min via size:	1.1 micron
Min via space:	1.6 micron
Min metal 1 width:	1.25 micron
Min metal 1 space:	0.9 micron
Min metal 1 pitch:	2.15 microns
Min contact size:	0.85 micron
Min contact space:	0.8 micron
Min poly width:	0.7 micron
Min poly space:	0.95 micron
Min contact to gate poly space:	0.35 micron
Min gate length* - (N-channel):	0.8 micron
- (P-channel):	0.9 micron
Tunnel oxide window:	1 x 2 microns (oval)

**Physical gate length.*

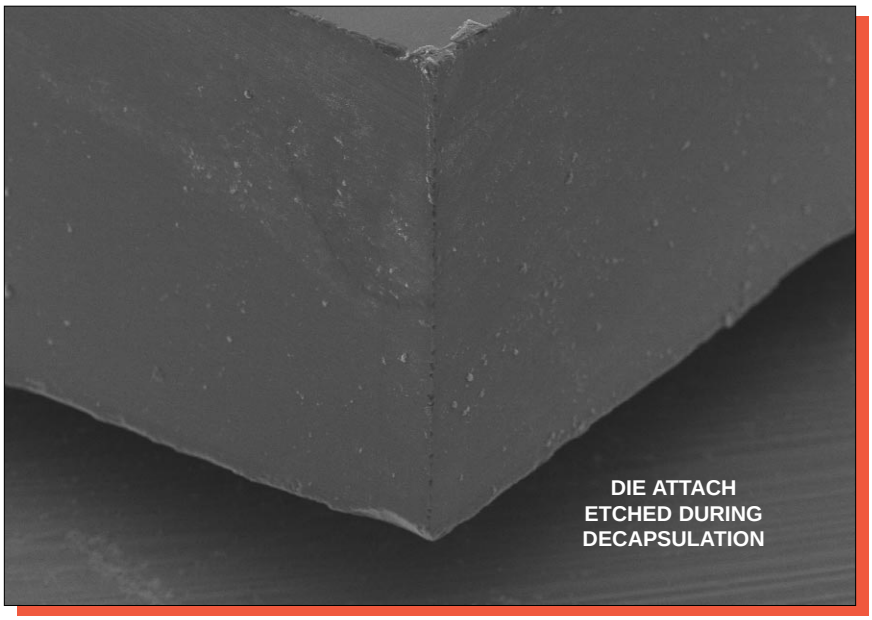
VERTICAL DIMENSIONS

Die thickness:	0.5 mm (20 mils)

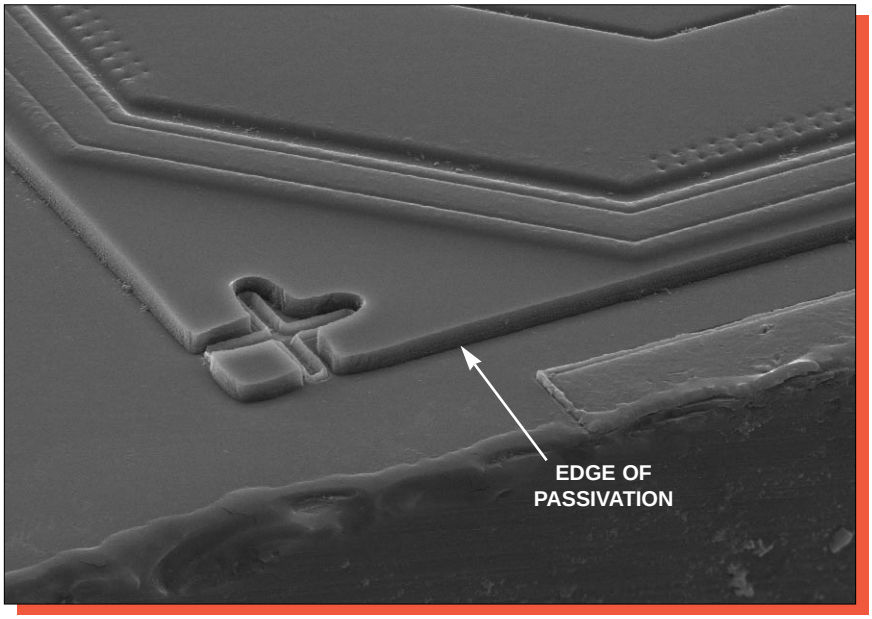
Layers

Passivation 3:	1.45 micron
Passivation 2:	0.16 micron (average)
Passivation 1:	0.3 micron
Metal 2 - aluminum:	1.0 micron
- barrier:	0.15 micron
Intermetal dielectric:	0.95 micron (average)
Metal 1 - cap:	0.07 micron (approx.)
- aluminum:	0.35 micron
- barrier:	0.09 micron
Pre-metal glass - BPSG:	0.5 micron
- multi-layered glass:	0.5 micron
Poly:	0.3 micron
Local oxide:	0.55 micron
N+ S/D diffusion:	0.35 micron
P+ S/D diffusion:	0.4 micron
Implant under cell capacitors:	0.4 micron
N-well:	3.0 microns
P-well:	Could not delineate

INDEX TO FIGURES



Mag. 150x



Mag. 1000x

Figure 1. Perspective SEM views of die corner and edge seal. 60°.

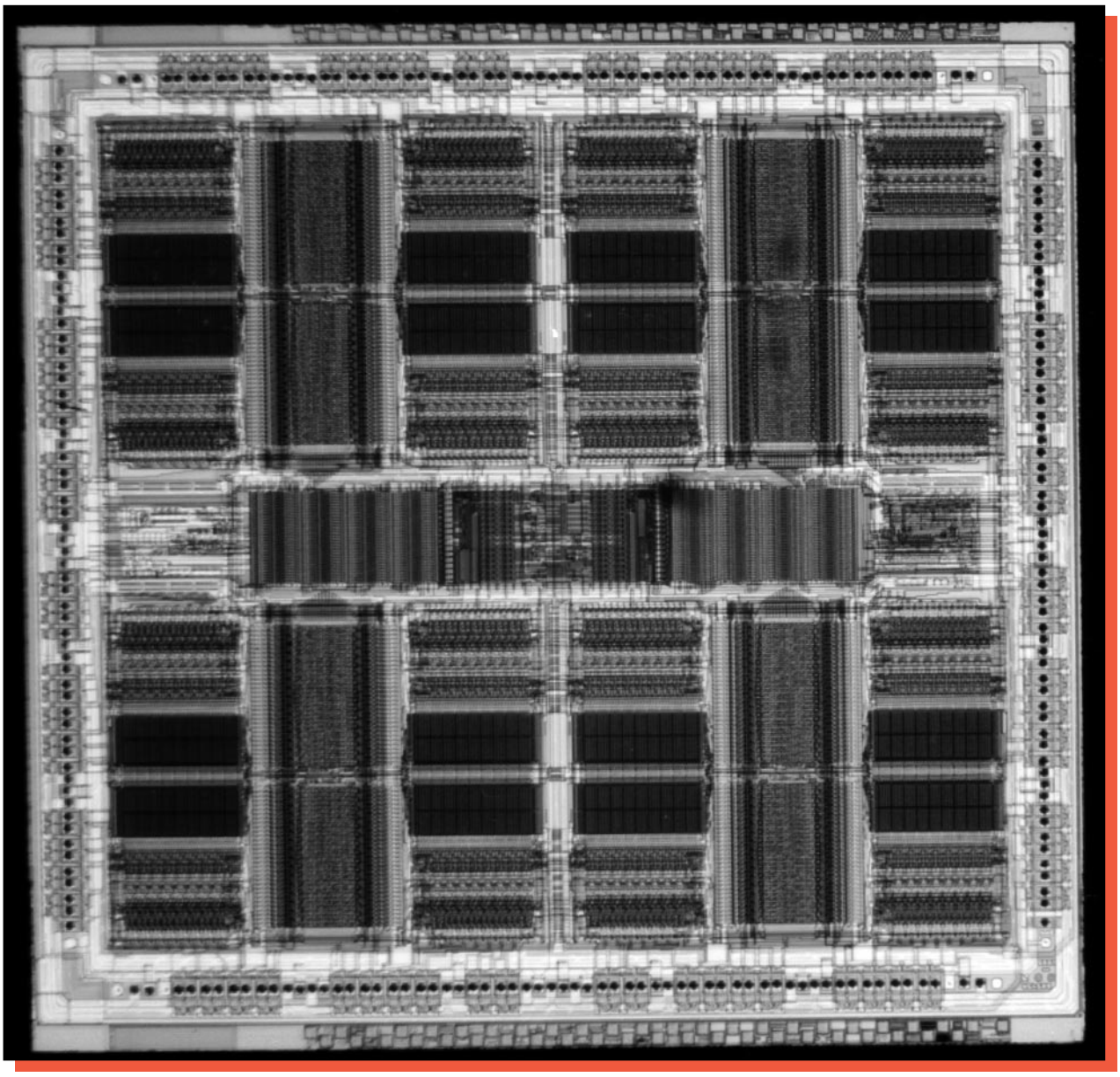


Figure 2. Whole die photograph of the AMD MACH5 256. Mag. 18x.

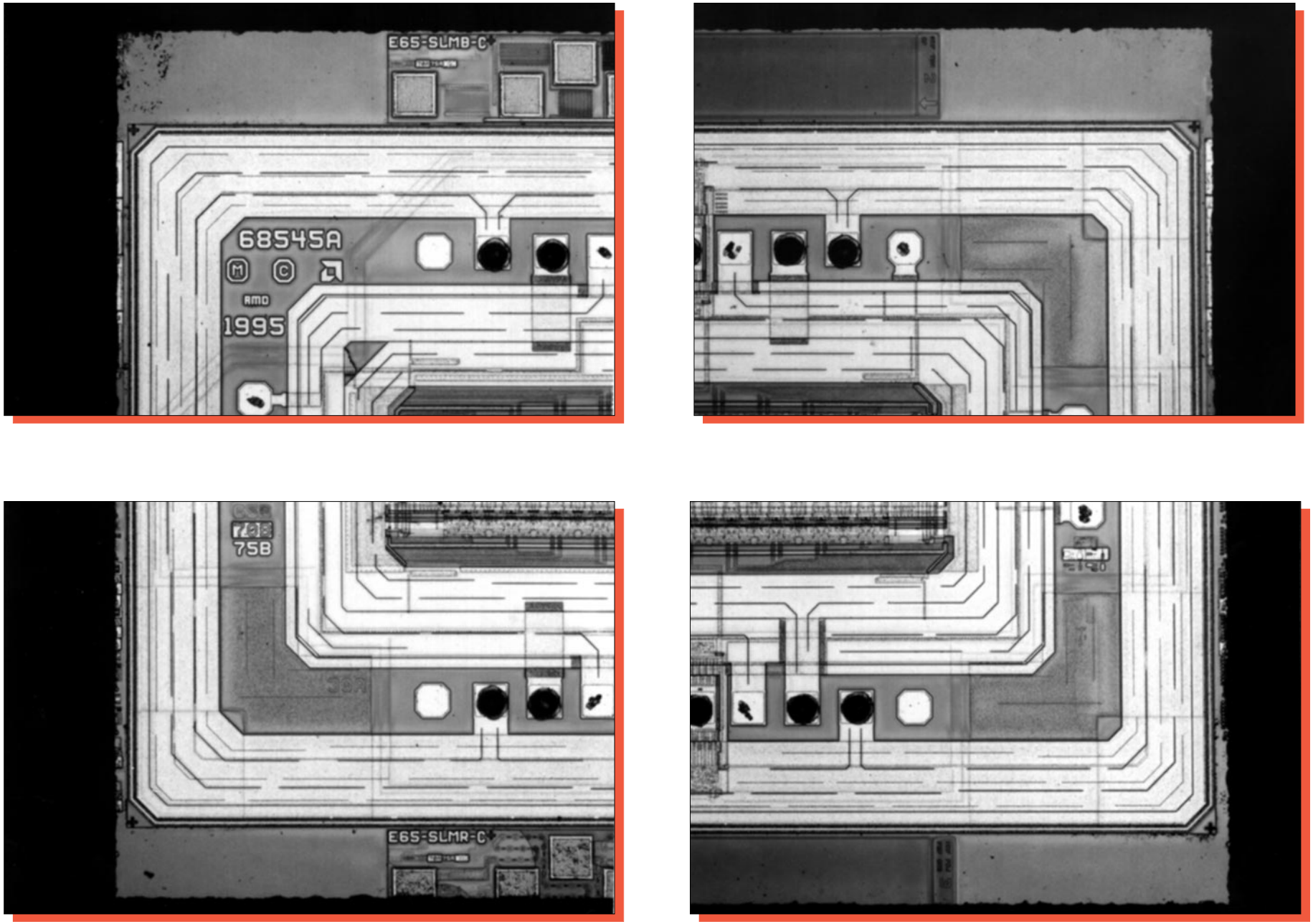


Figure 3. Optical views of the die corners on the AMD MACH5 256 die. Mag. 80x.

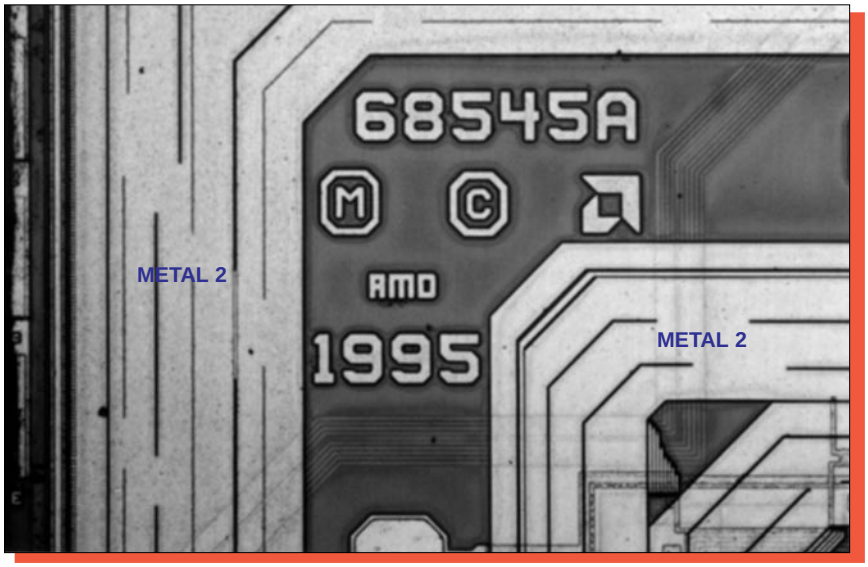
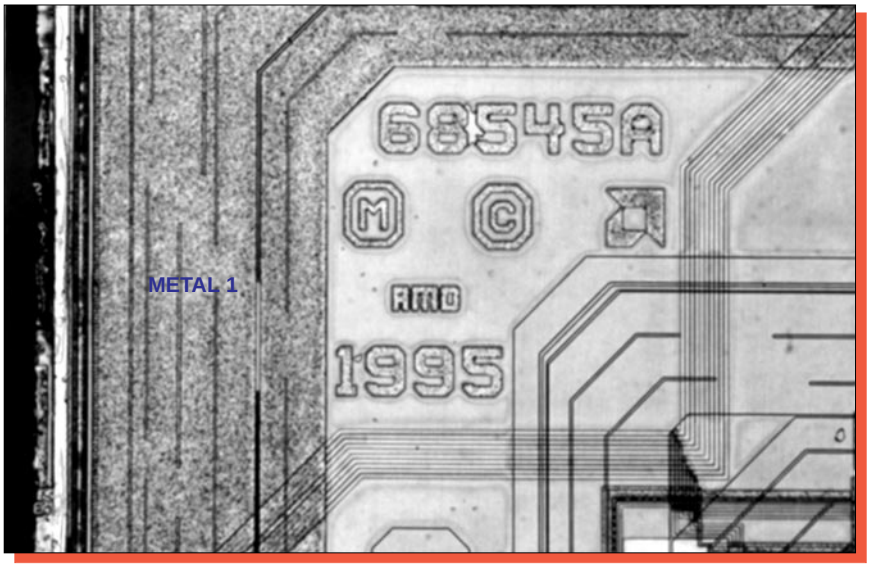
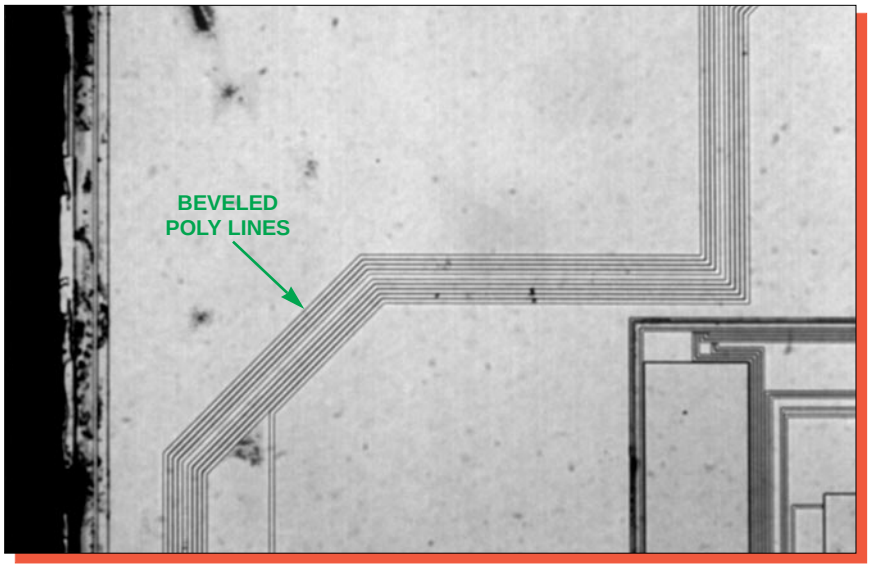


Figure 4. Die markings from the surface of the die. Intact, Mag. 160x.

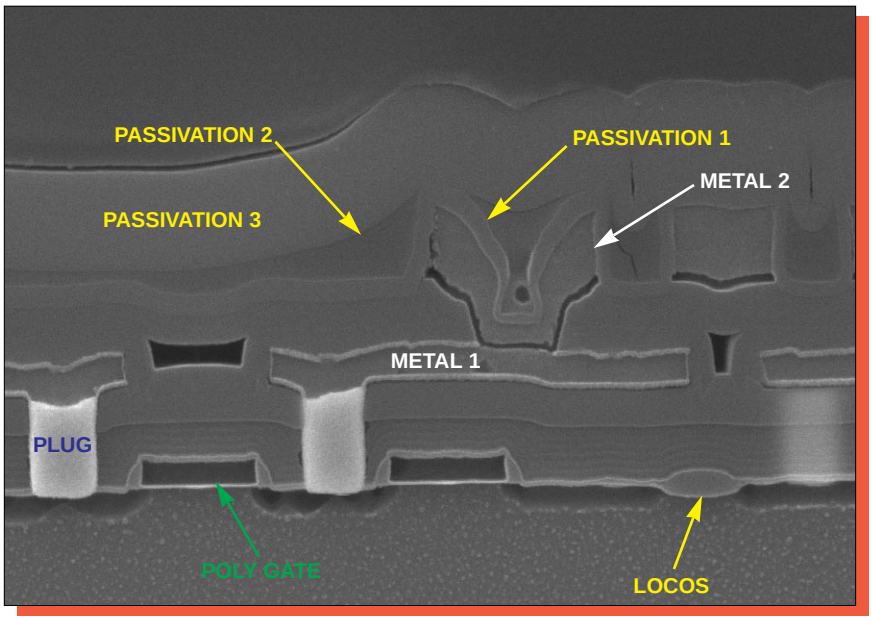


metal 1

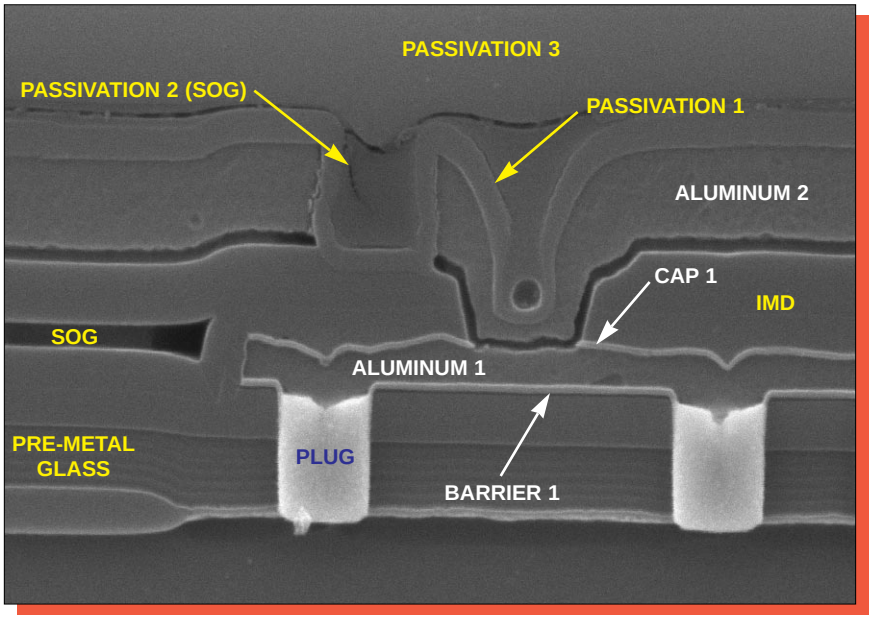


unlayered

Figure 5. Metal patterning along die corner. Mag. 160x.

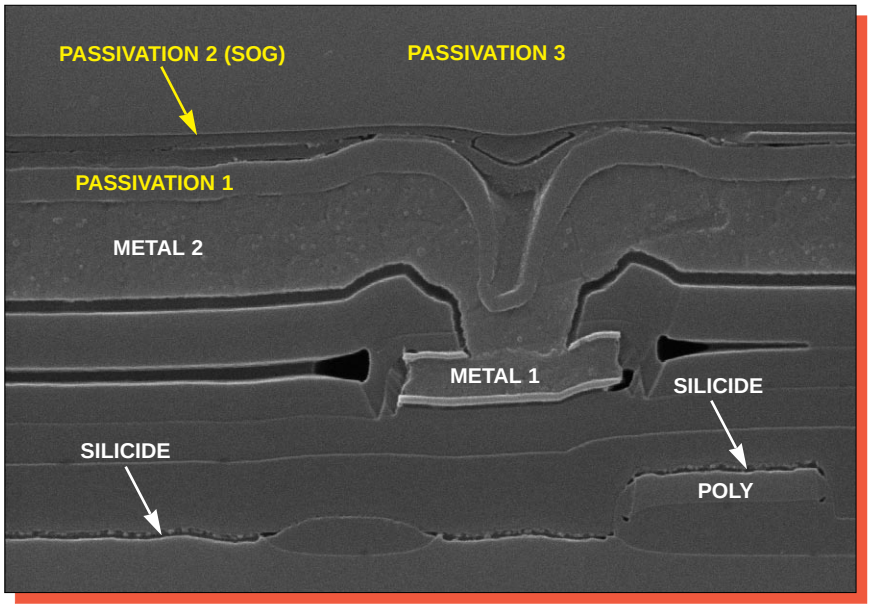


Mag. 10,000x



Mag. 13,000x

Figure 6. SEM section views of general structure. Silicon-etch.



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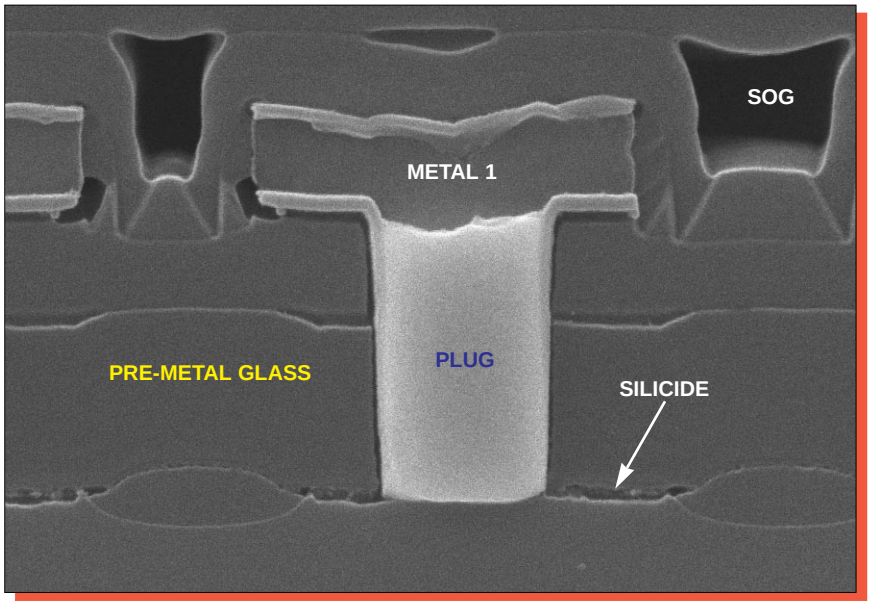
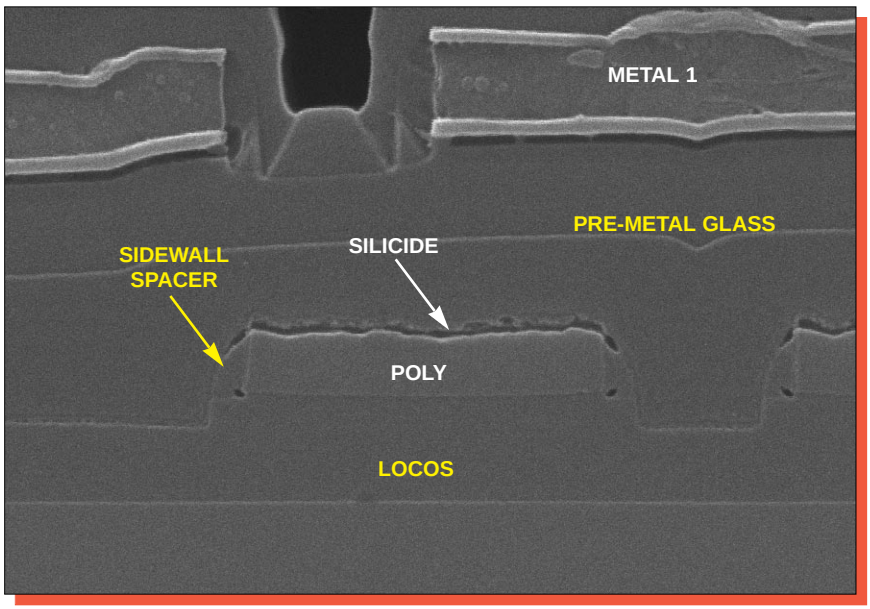
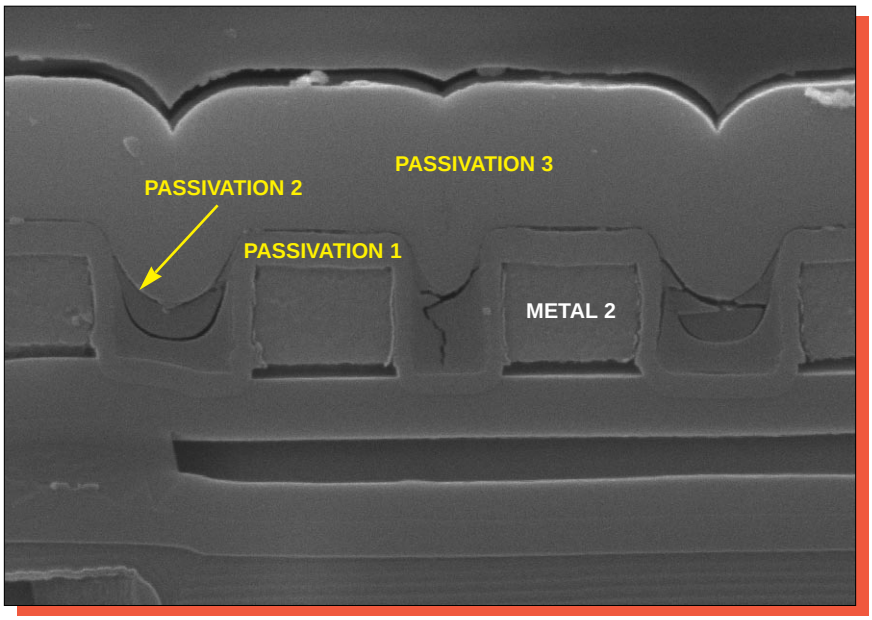


Mag. 26,000x



Mag.26,000x

Figure 6a. SEM section views of general construction. Glass-etch.



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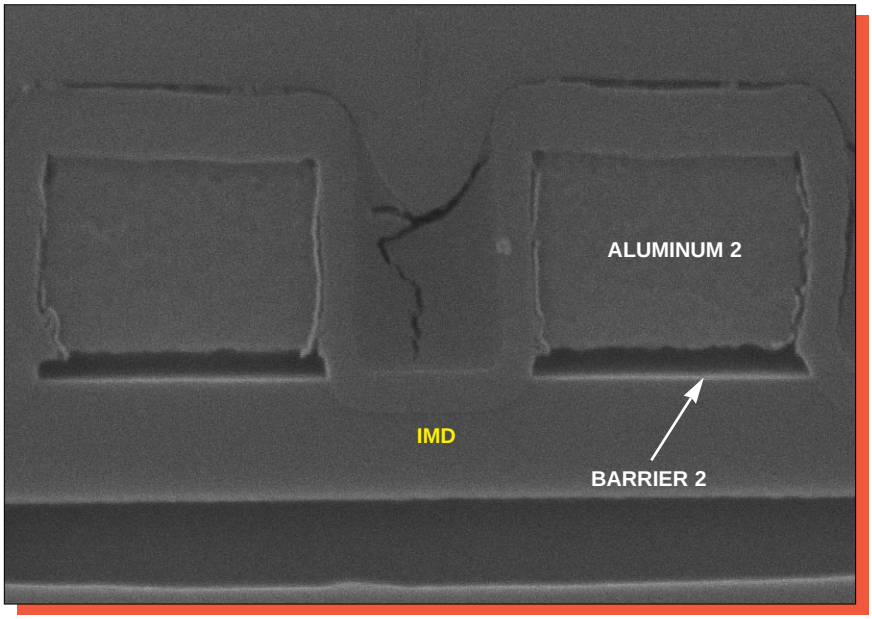
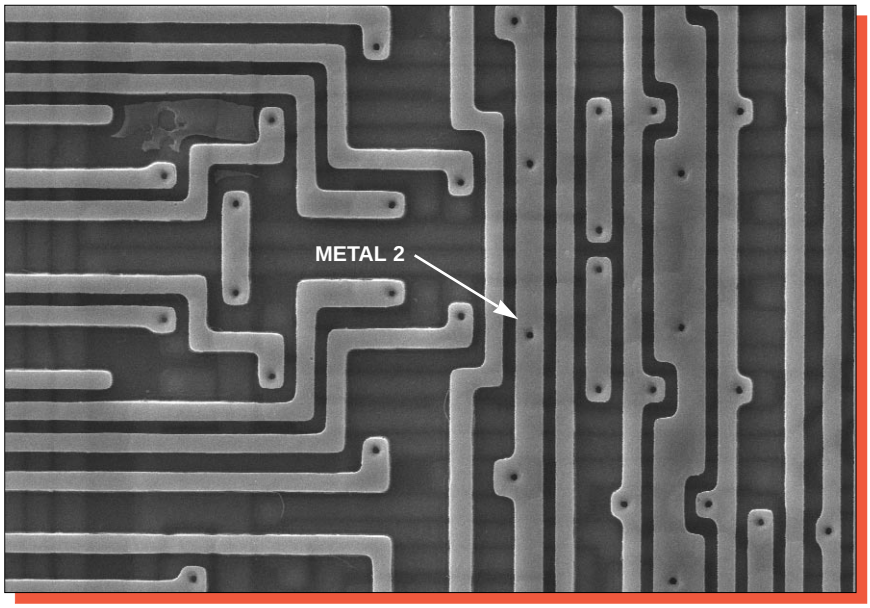
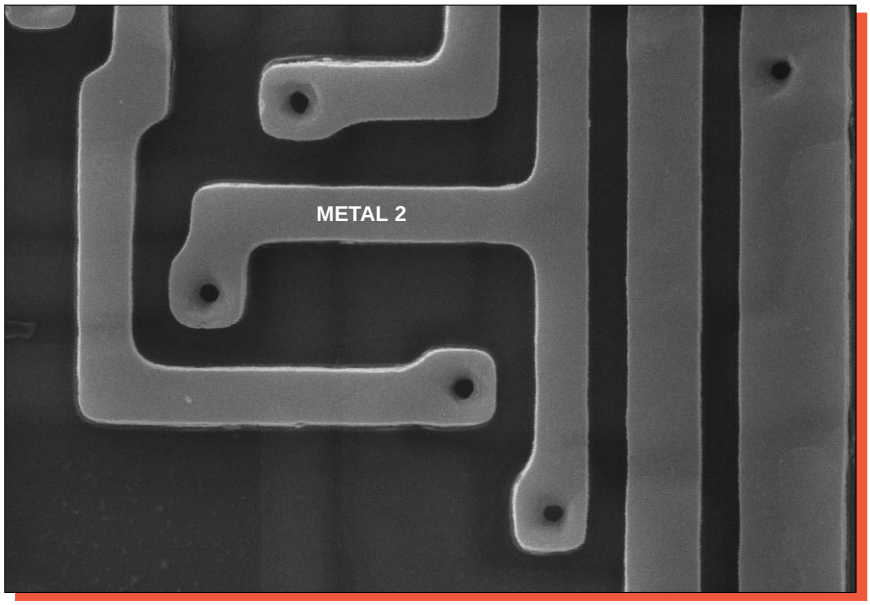


Mag. 26,000x

Figure 7. SEM section views of metal 2 line profiles.



Mag. 1600x



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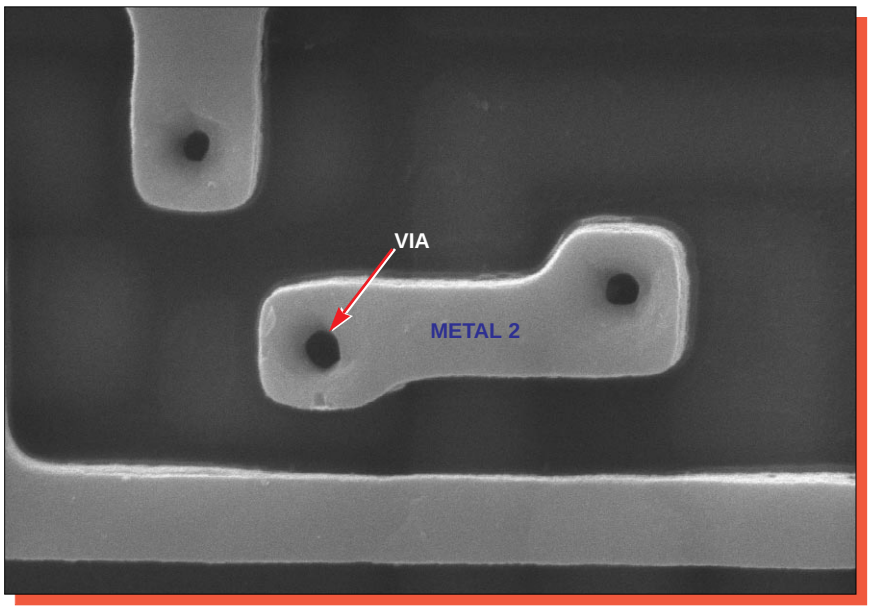
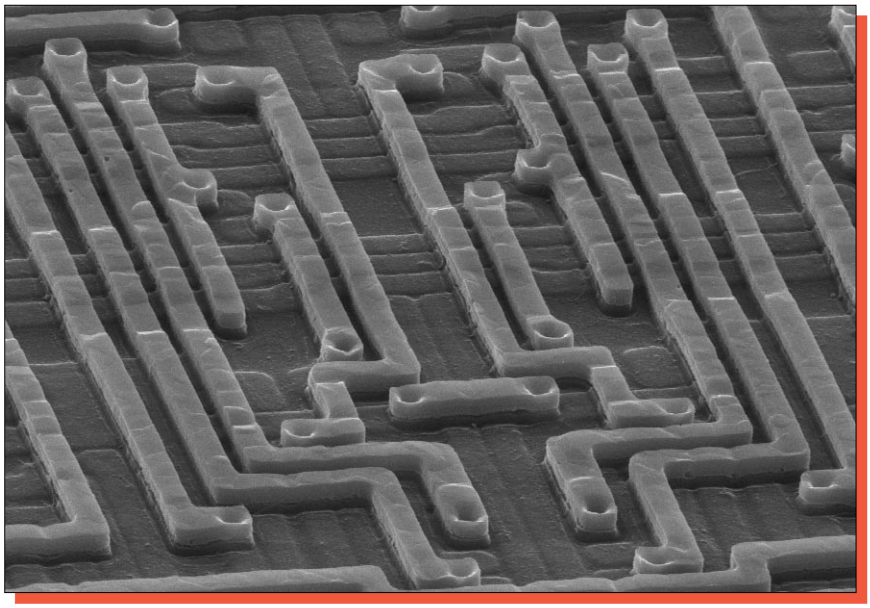
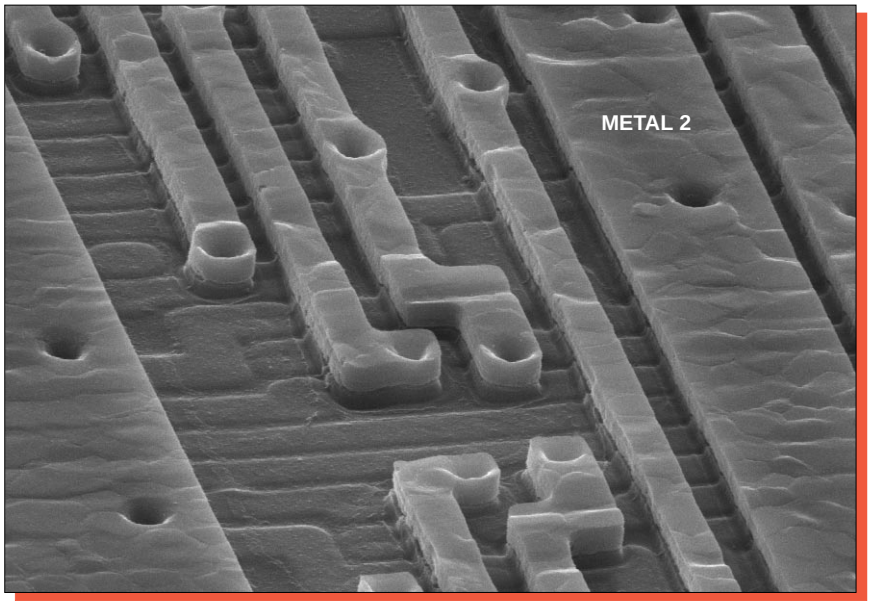


Mag. 8000x

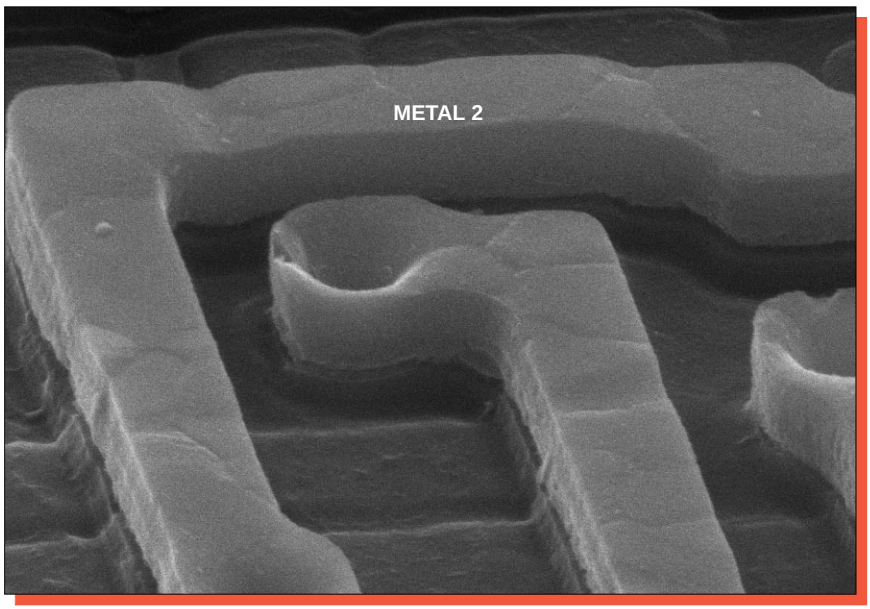
Figure 8. Topological SEM views of metal 2 patterning. 0°.



Mag. 2500x

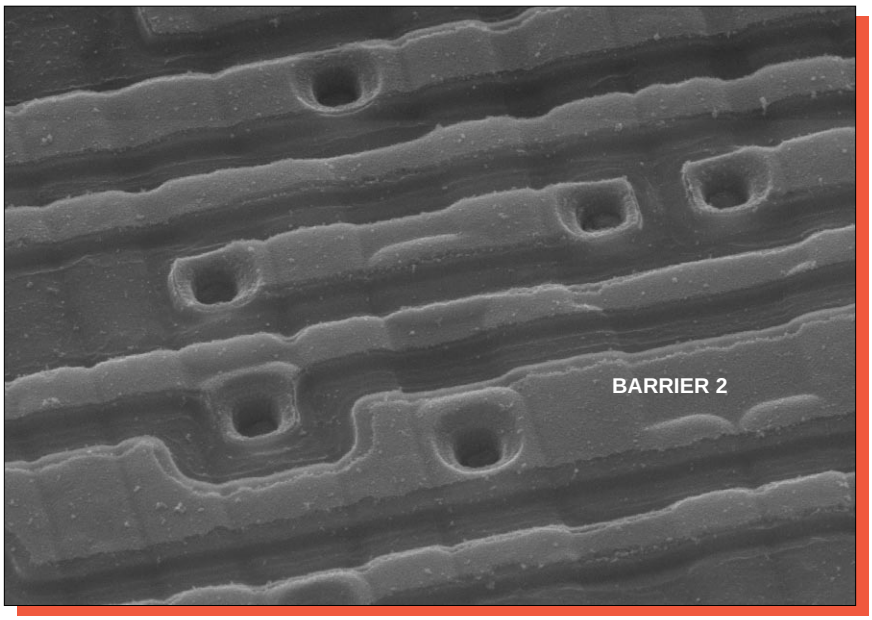


Mag. 4000x

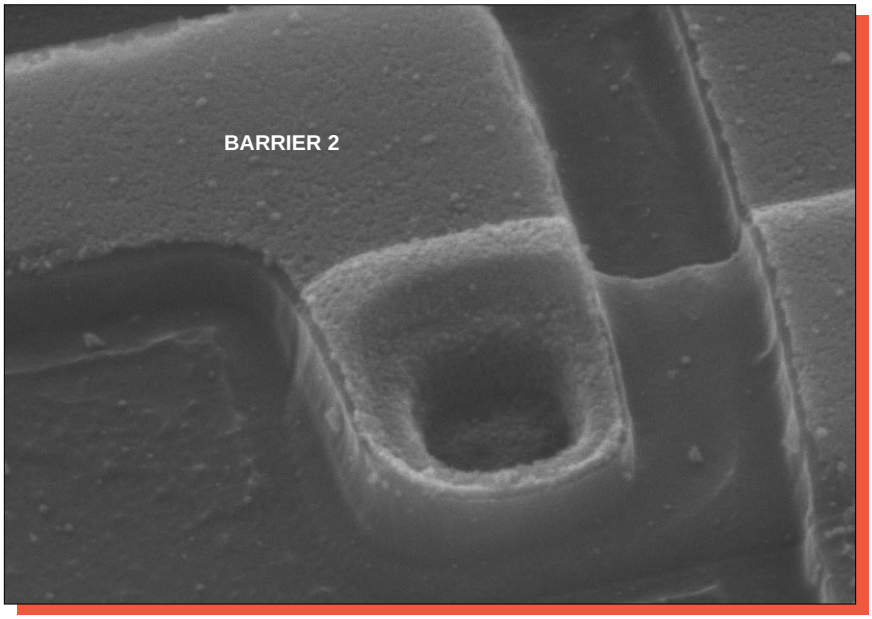


Mag. 12,000x

Figure 9. Perspective SEM views of metal 2 coverage. 60°.

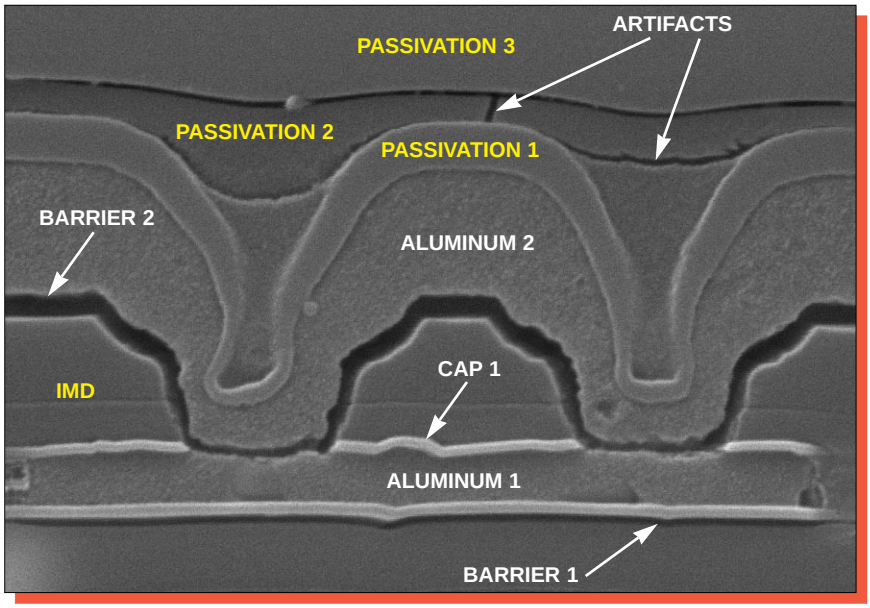


Mag. 6000x

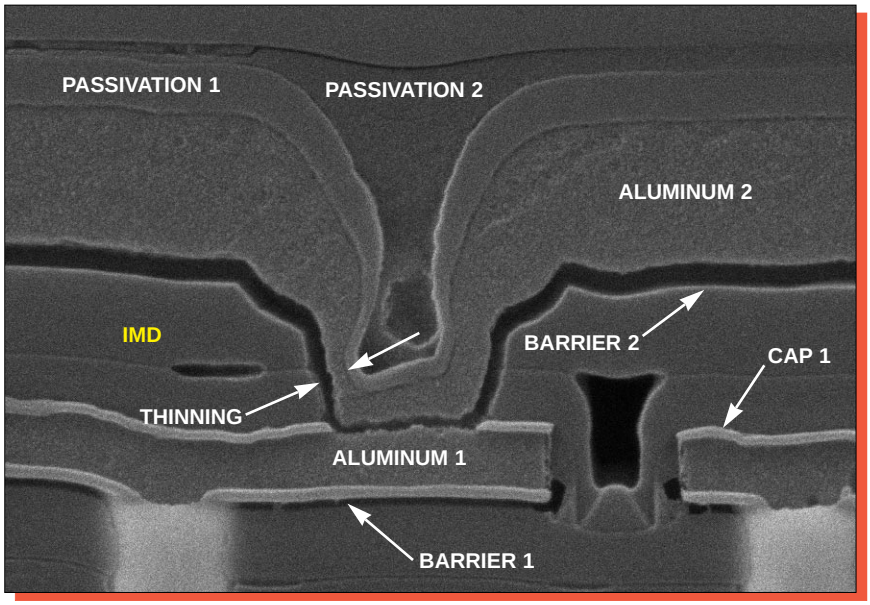


Mag. 20,000x

Figure 10. Perspective SEM views of metal 2 barrier. 45°.



Mag. 20,000x



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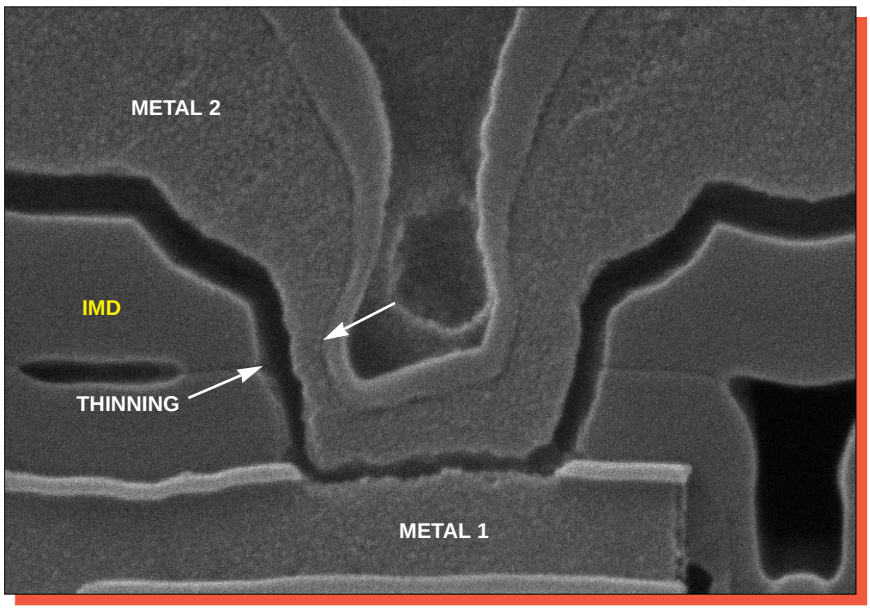


Mag. 35,000x

Figure 11. SEM section views of metal 2-to-metal 1 vias.

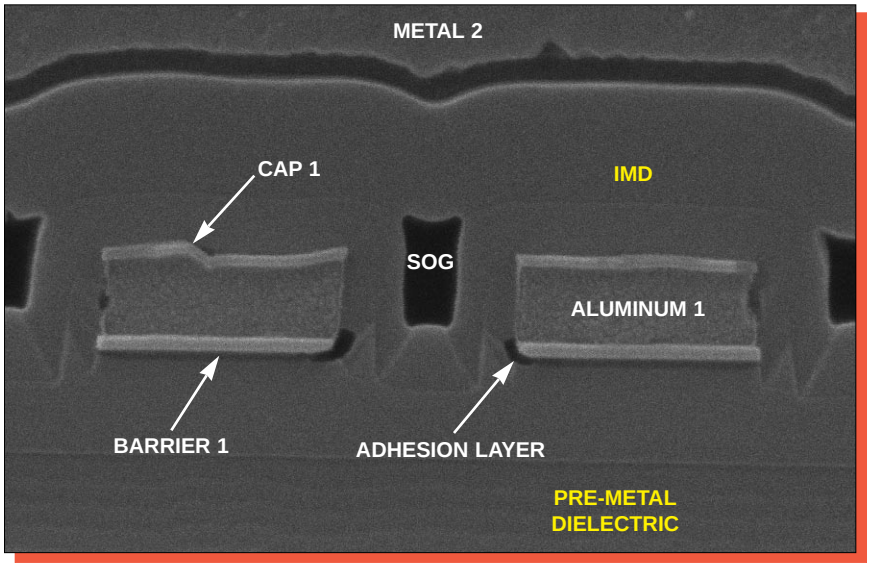
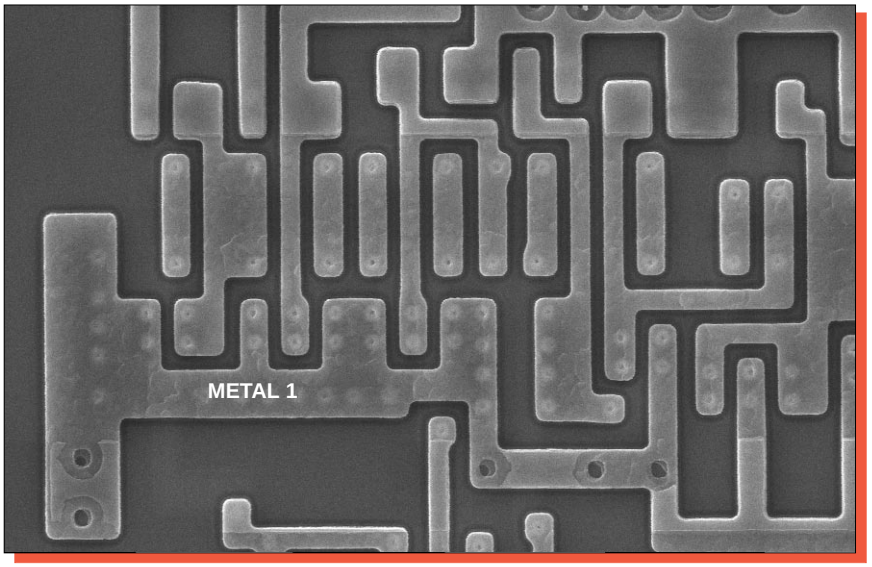
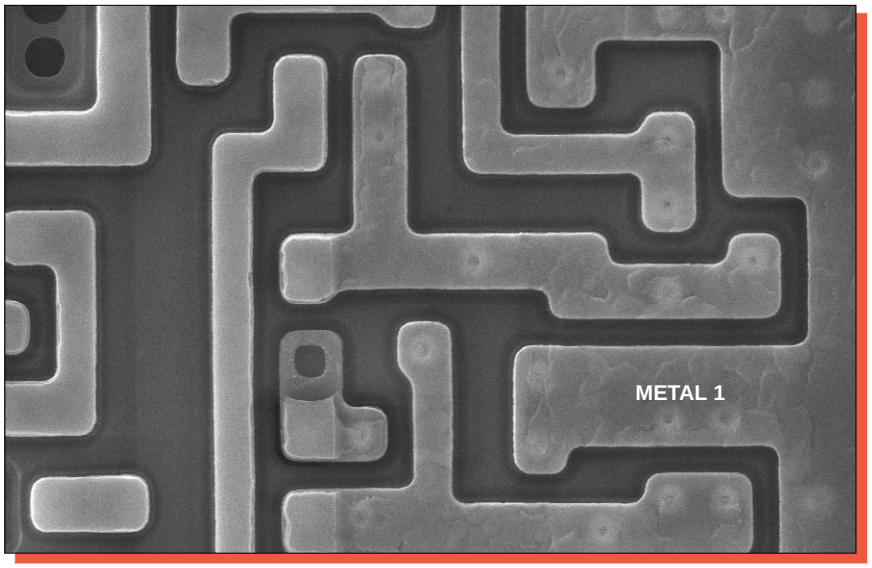


Figure 12. SEM section views of metal 1 line profiles. Mag. 26,000x.

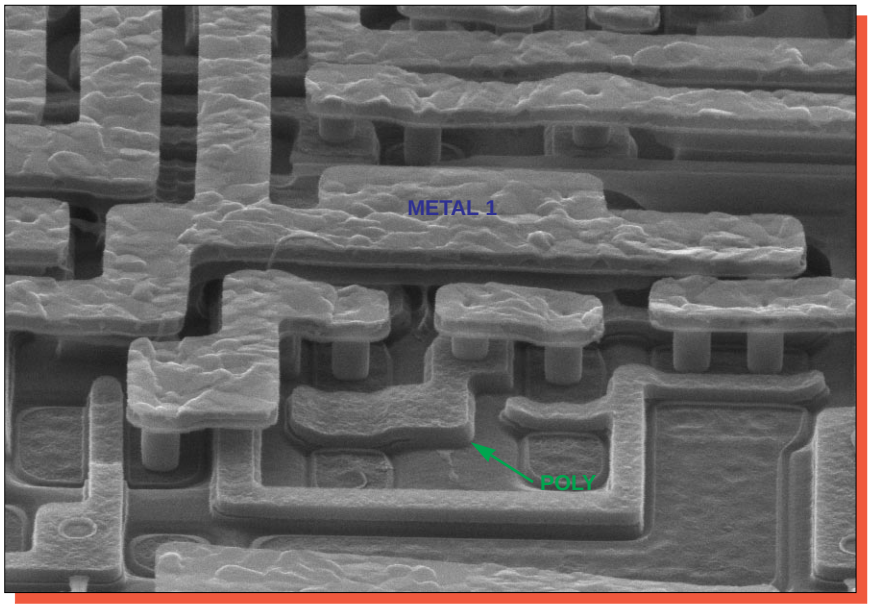


Mag. 2000x

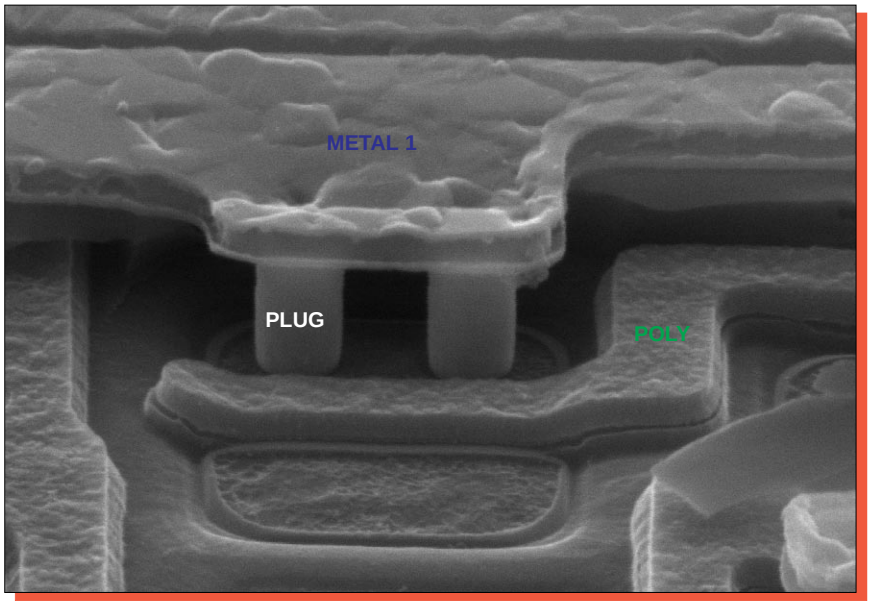


Mag. 4000x

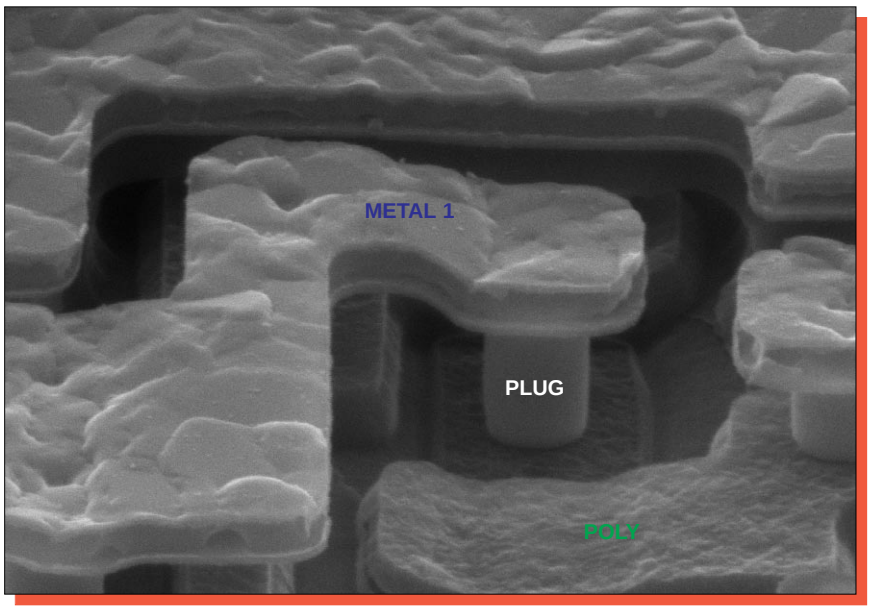
Figure 13. Topological SEM views of metal 1 patterning. 0°.



Mag. 6000x

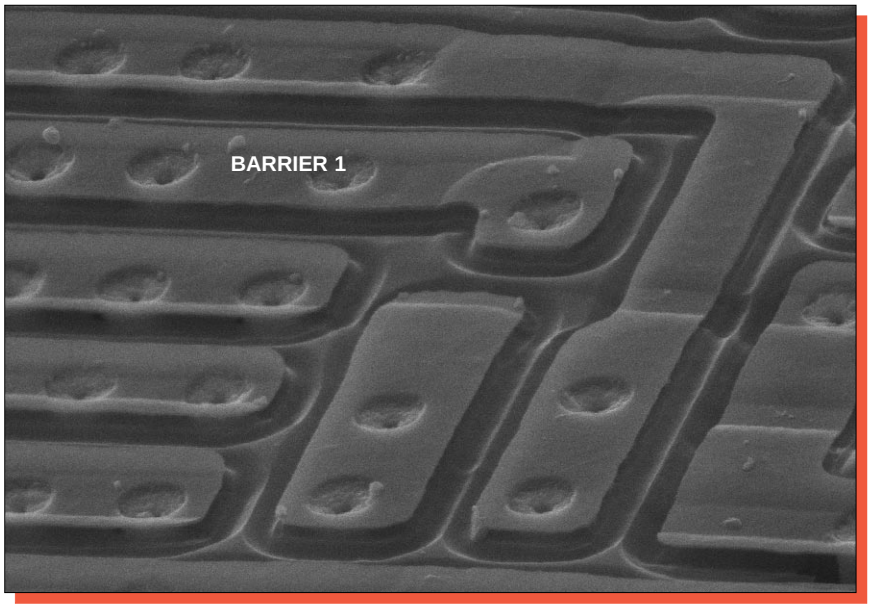


Mag. 13,000x

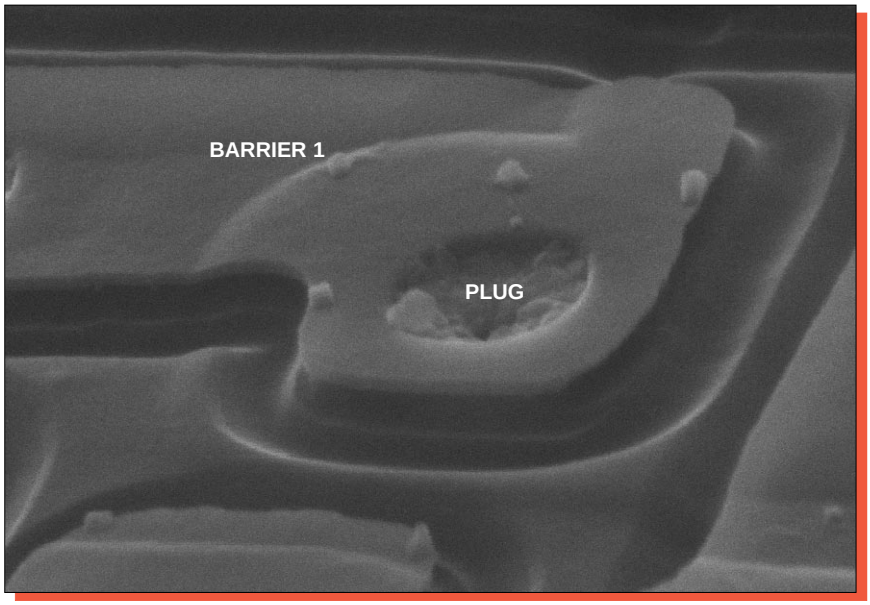


Mag. 16,000x

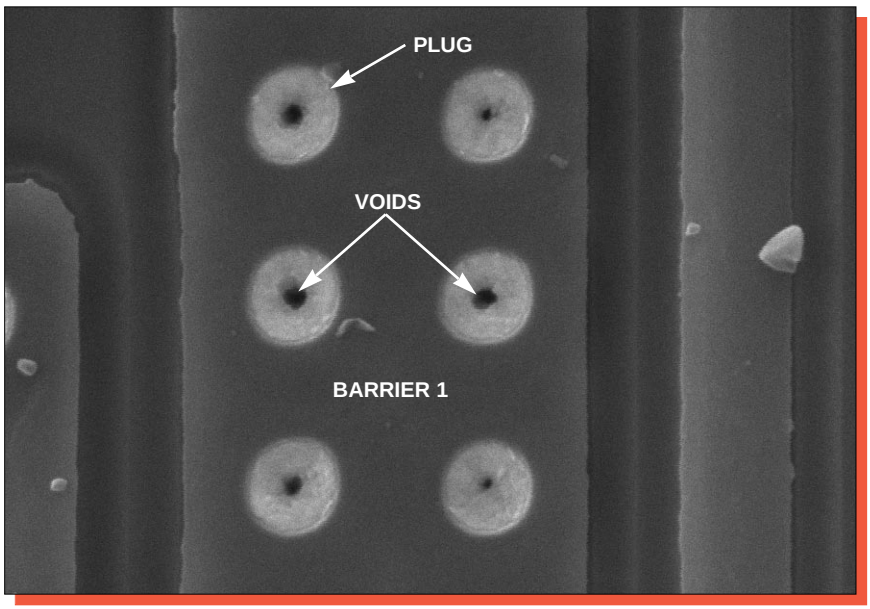
Figure 14. Perspective SEM views of metal 1 coverage. 60°.



Mag. 10,000x, 60°



Mag. 27,000x, 60°



Mag. 13,000x, 0°

Figure 15. Topological SEM views of metal 1 barrier.

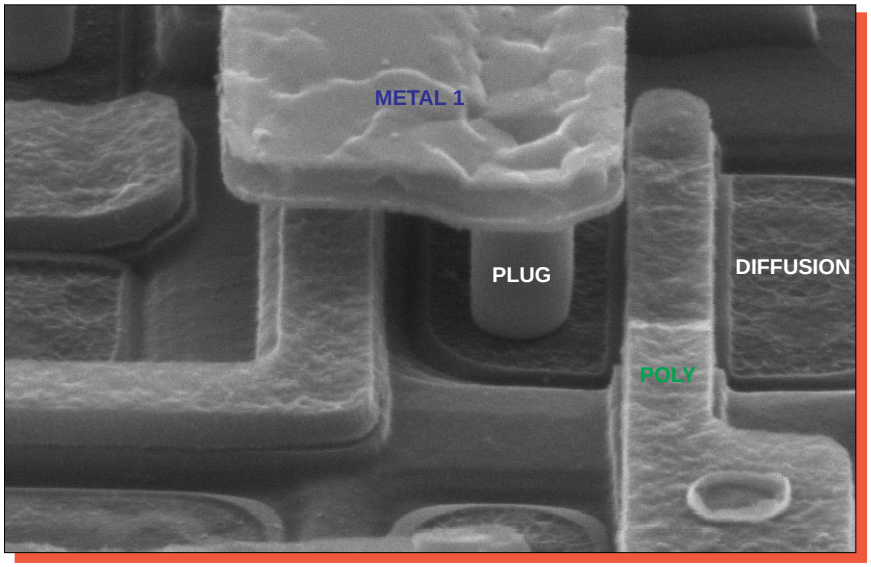
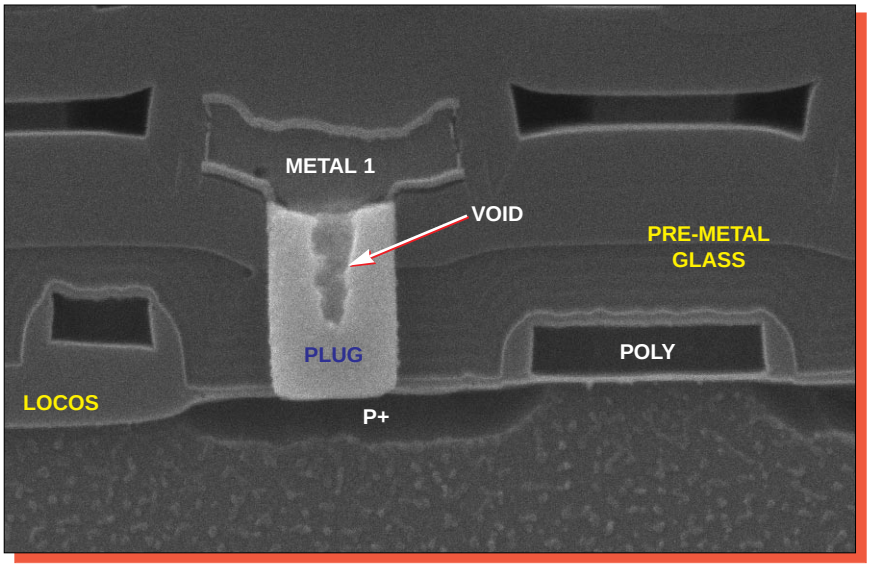
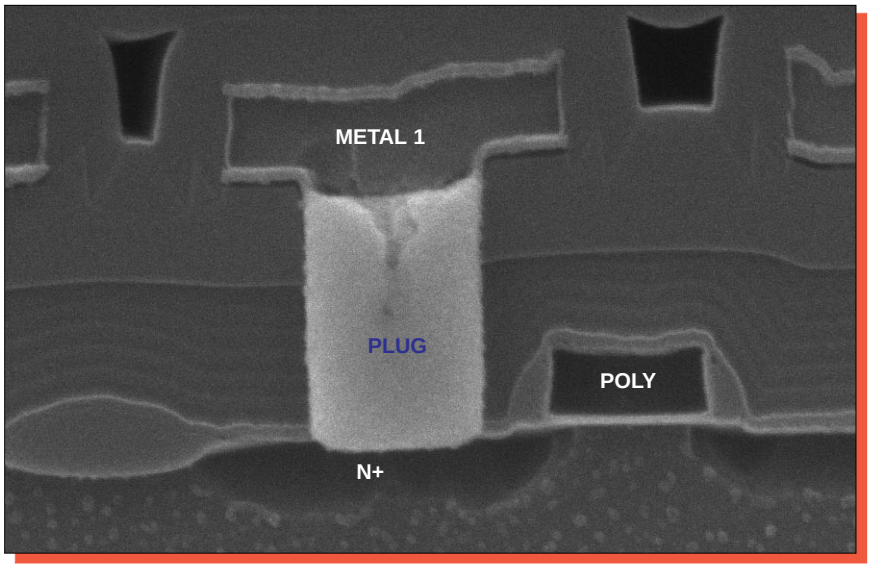


Figure 16. Perspective SEM view of metal 1-to-diffusion contact. Mag. 15,000x, 60°.

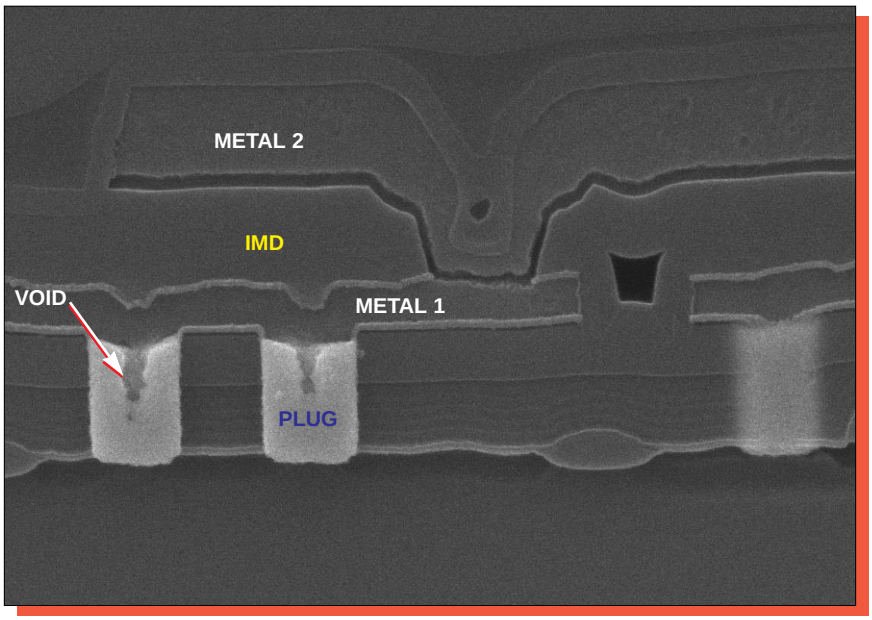


metal 1-to-P+,
Mag. 20,000x

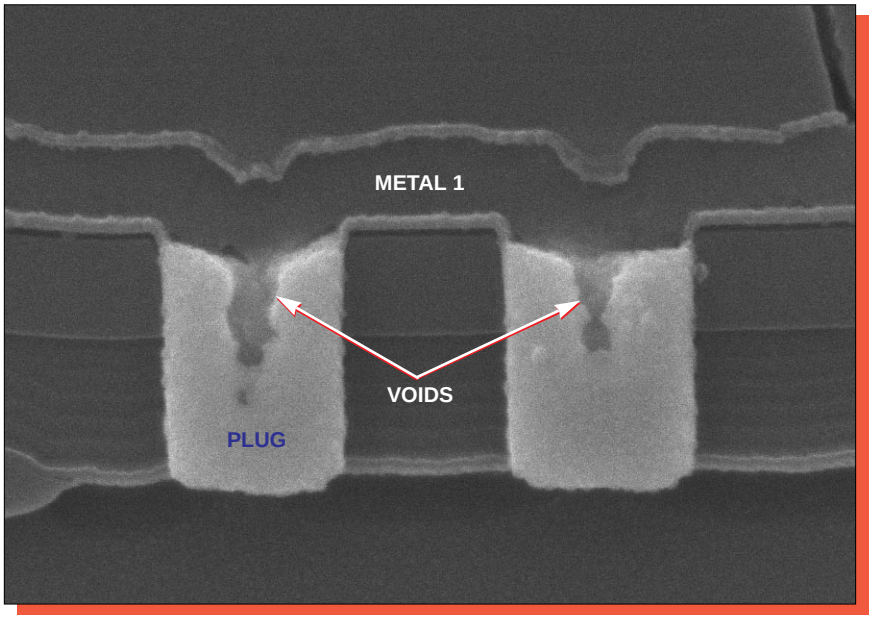


metal 1-to-N+,
Mag. 26,000x

Figure 17. SEM section views of metal-to-diffusion contacts.

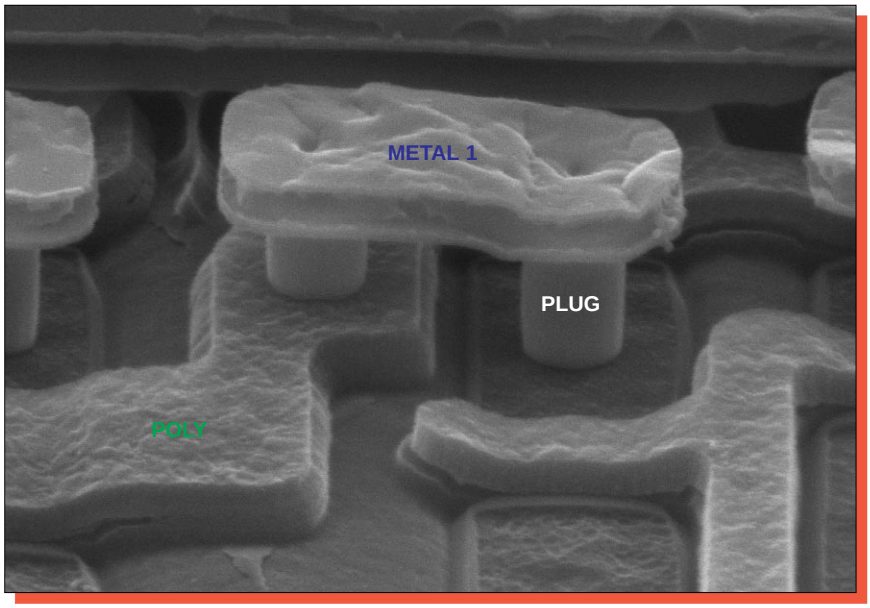


Mag. 13,000x

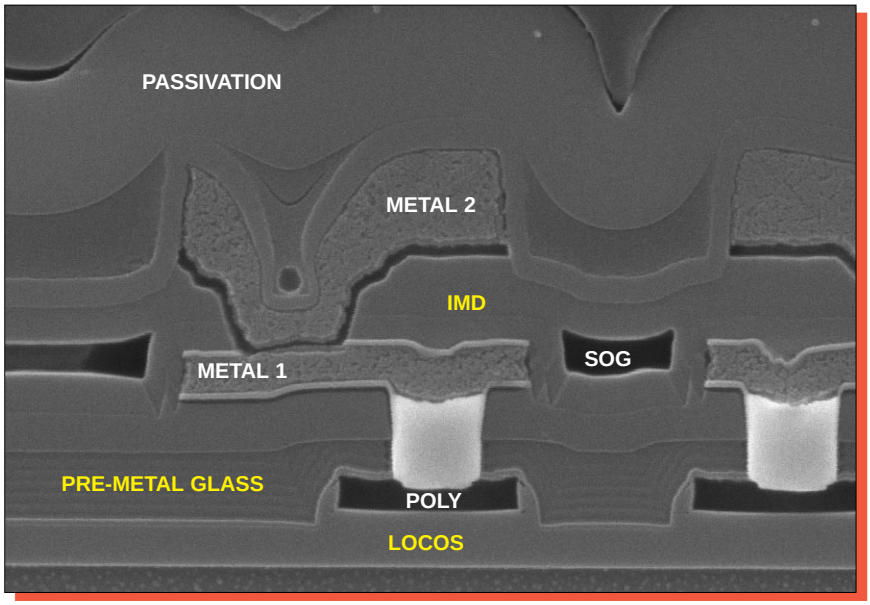


Mag. 26,000x

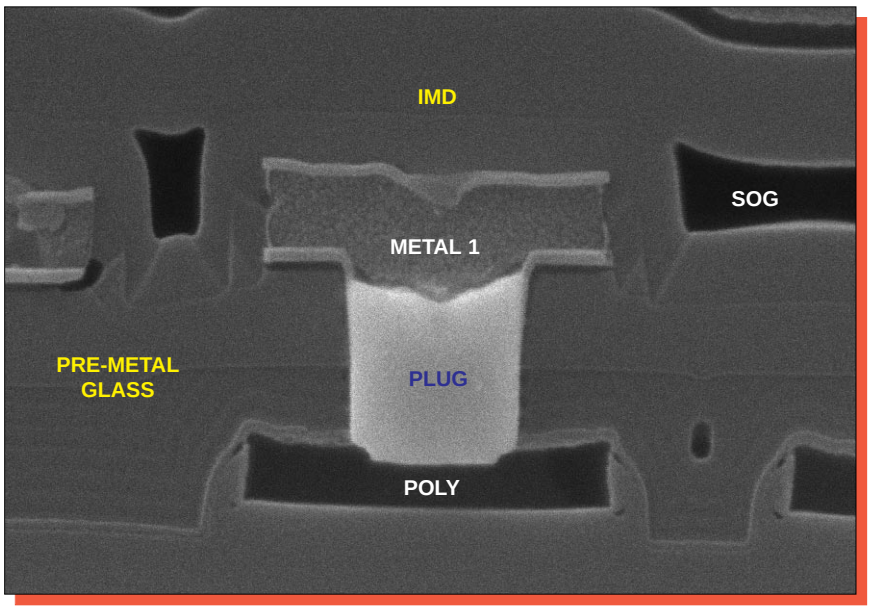
Figure 17a. SEM section views illustrating the voids in the metal 1 plugs.



Mag. 16,000x, 60°

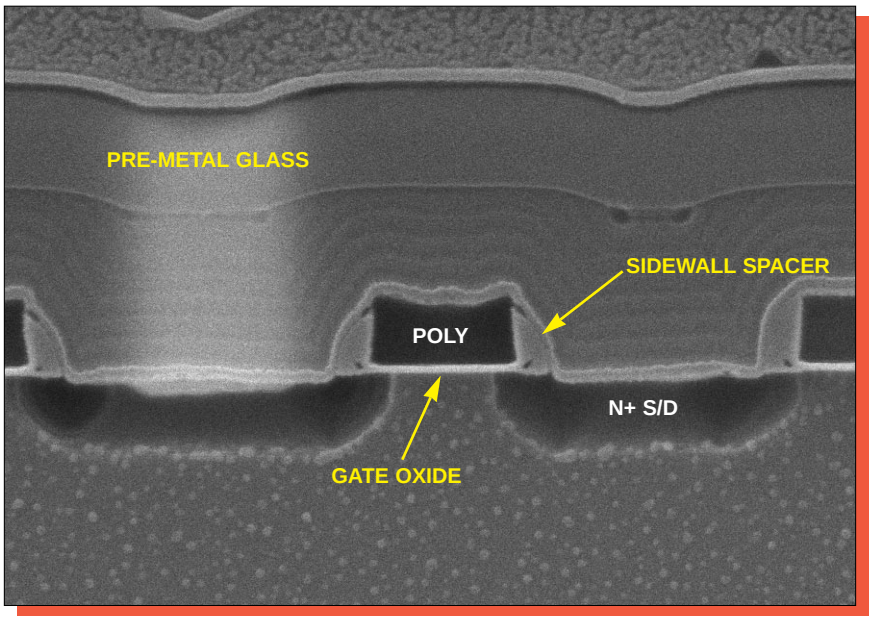


Mag. 13,000x

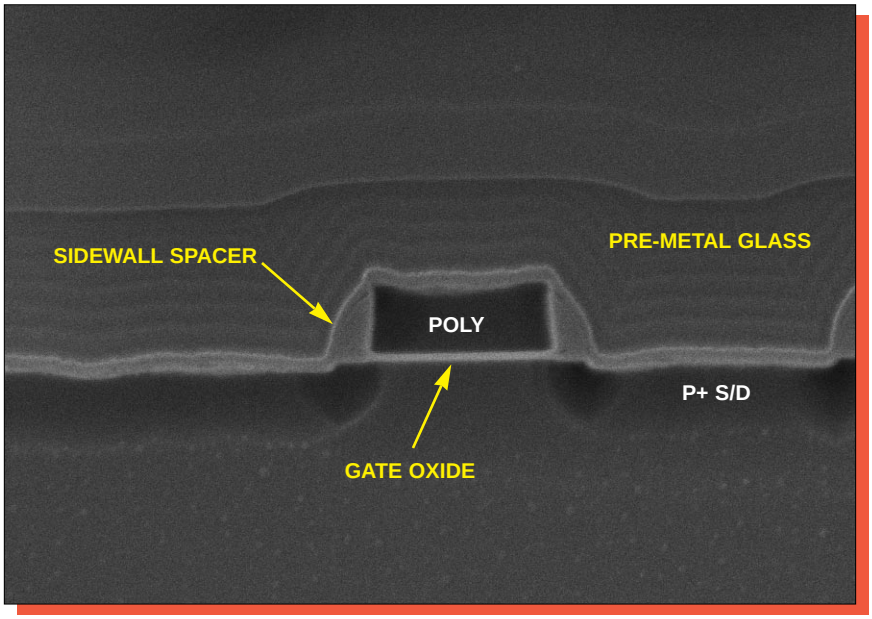


Mag. 26,000x

Figure 18. Topological and SEM section views of metal 1-to-poly contacts.

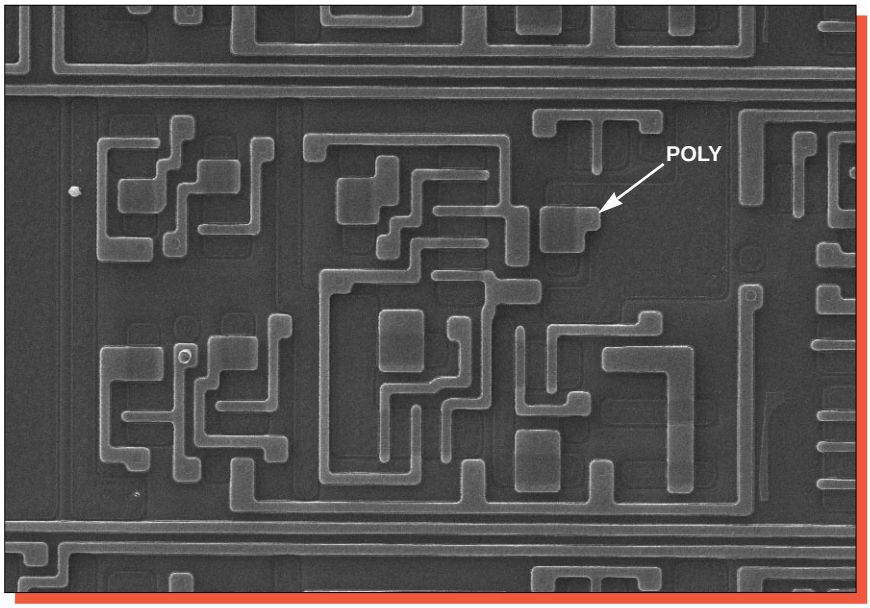


N-channel

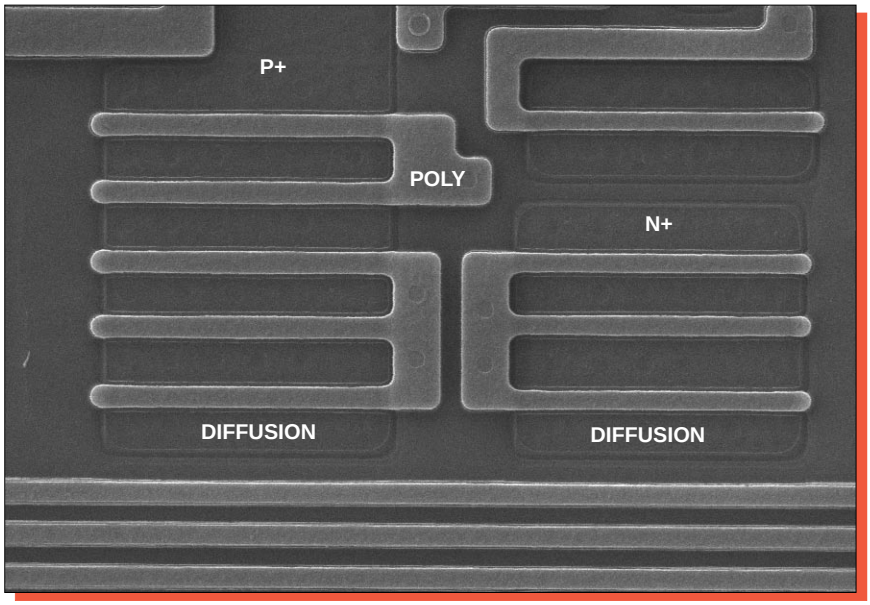


P-channel

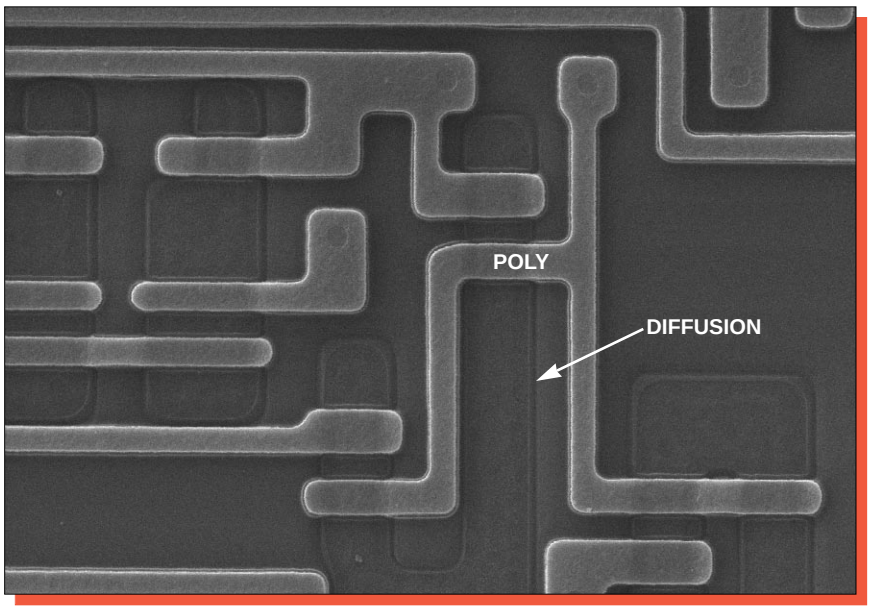
Figure 19. SEM section views of typical transistors. Mag. 26,000x.



Mag. 1600x

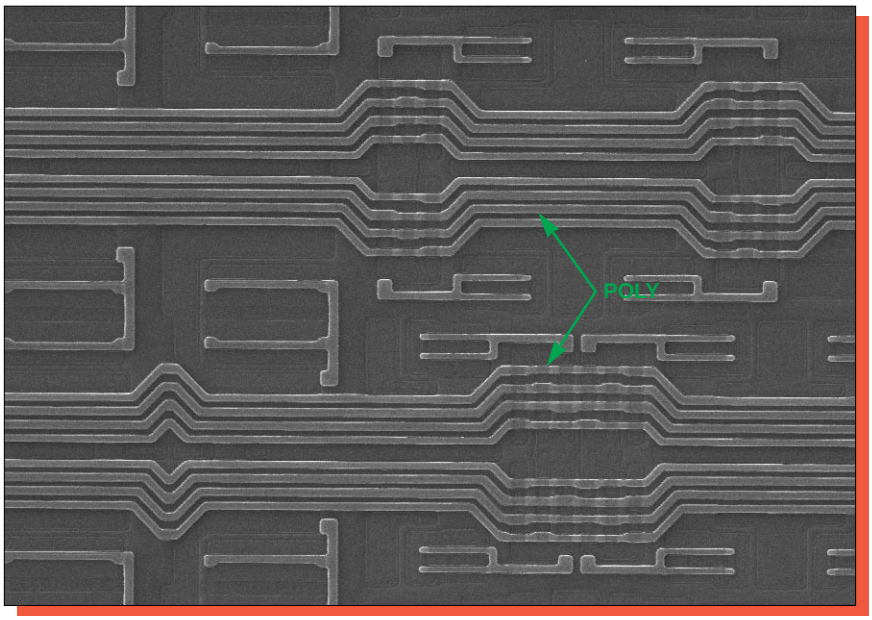


Mag. 3000x

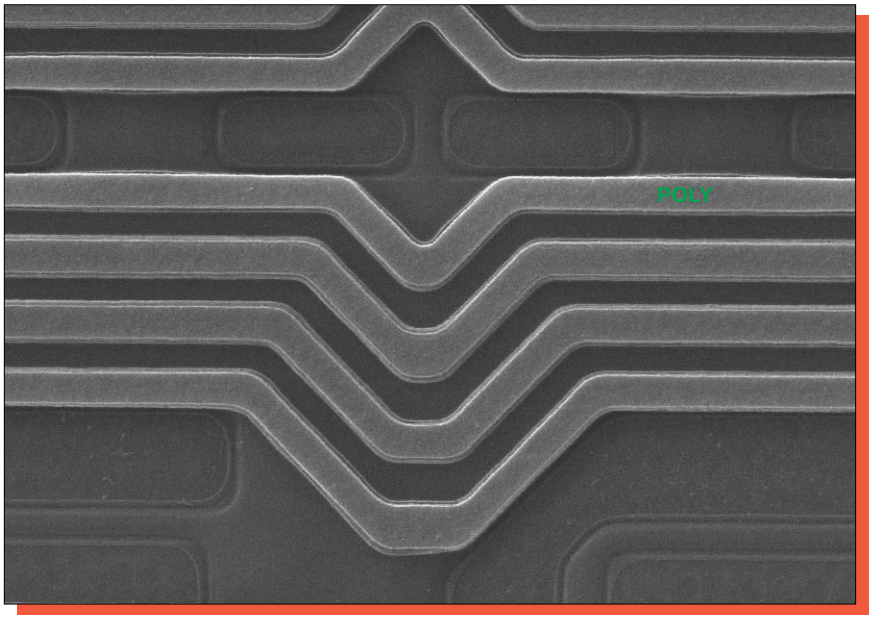


Mag. 4000x

Figure 20. Topological SEM views of poly patterning. 0°.

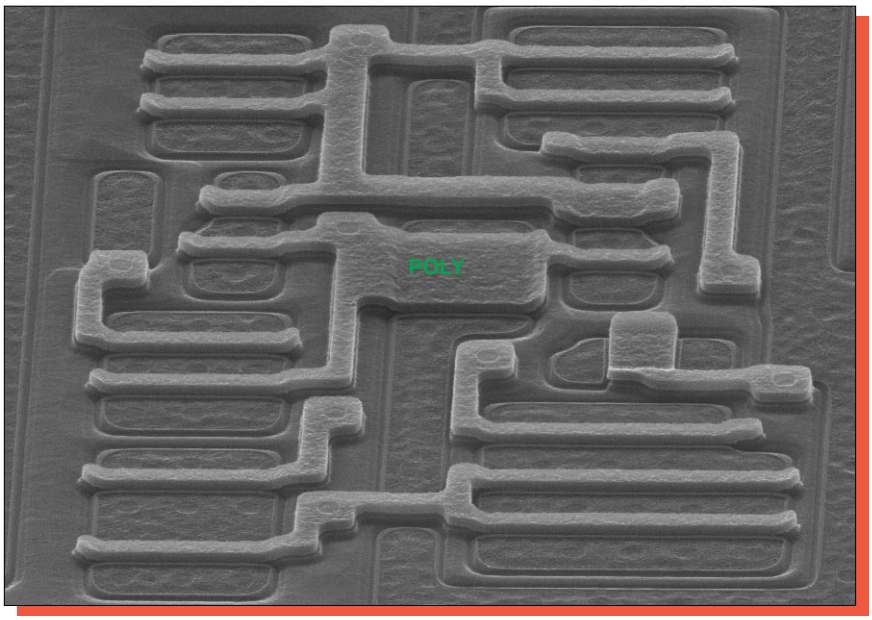


Mag. 1000x

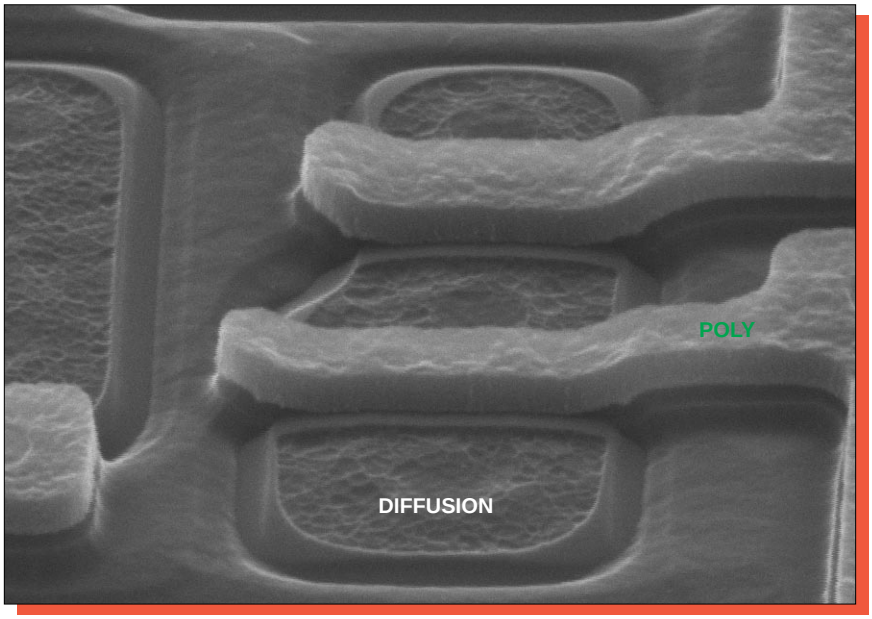


Mag. 5000x

Figure 20a. Additional topological SEM views of poly patterning. 0°.

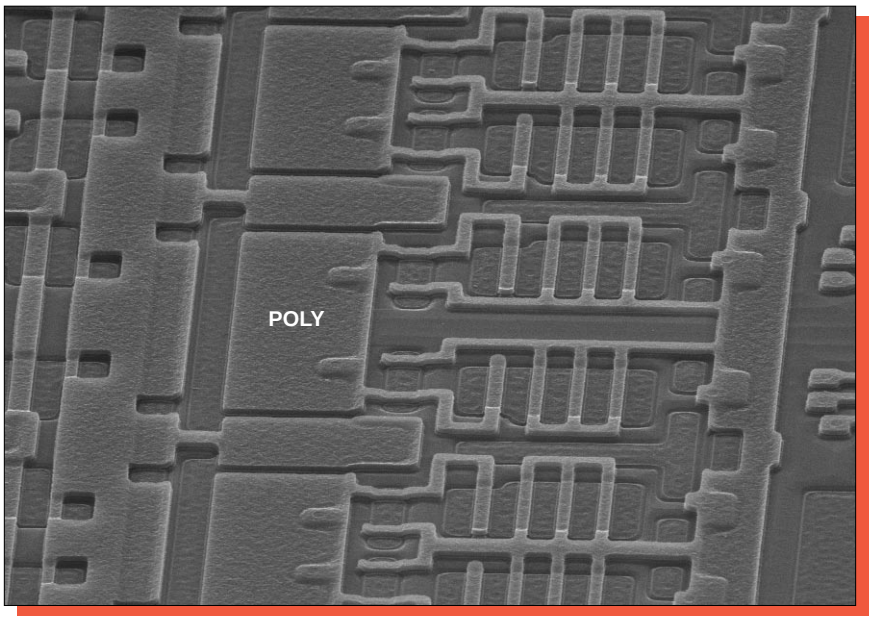


Mag. 4000x

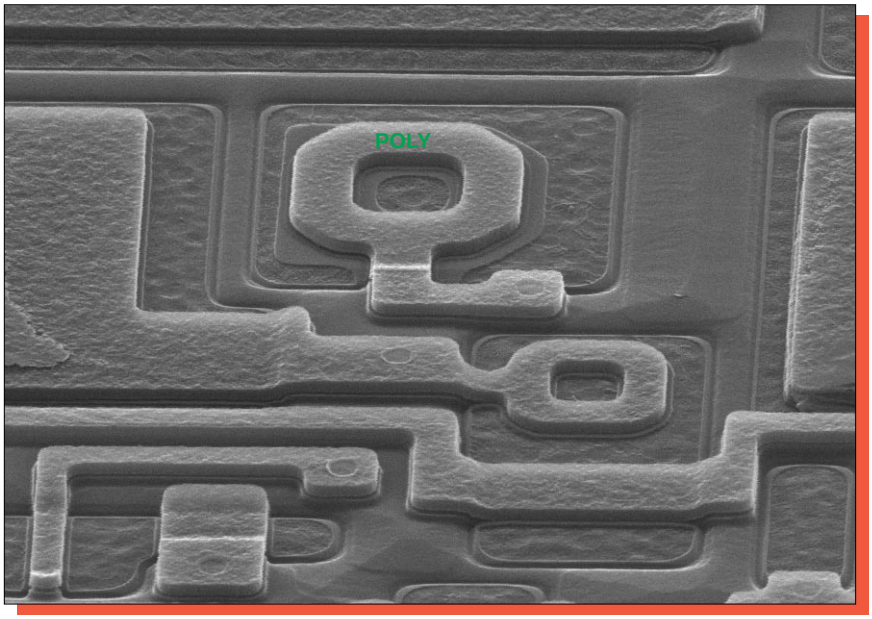


Mag. 16,000x

Figure 21. Perspective SEM views of poly patterns. 60°.



Mag. 2000x



Mag. 5000x

Figure 21a. Additional SEM views of poly coverage. 60°.

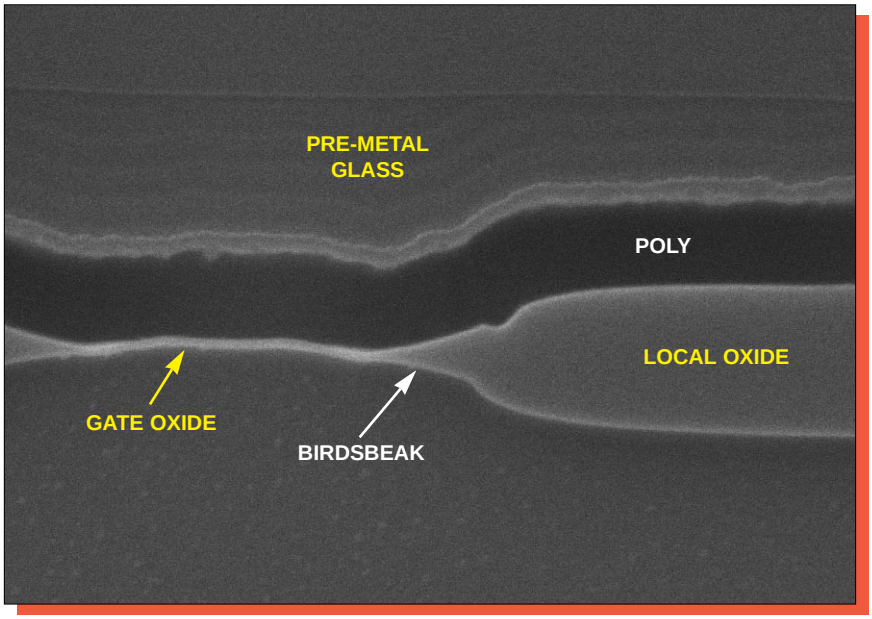


Figure 22. SEM section view of a local oxide birdsbeak. Mag. 35,000x.

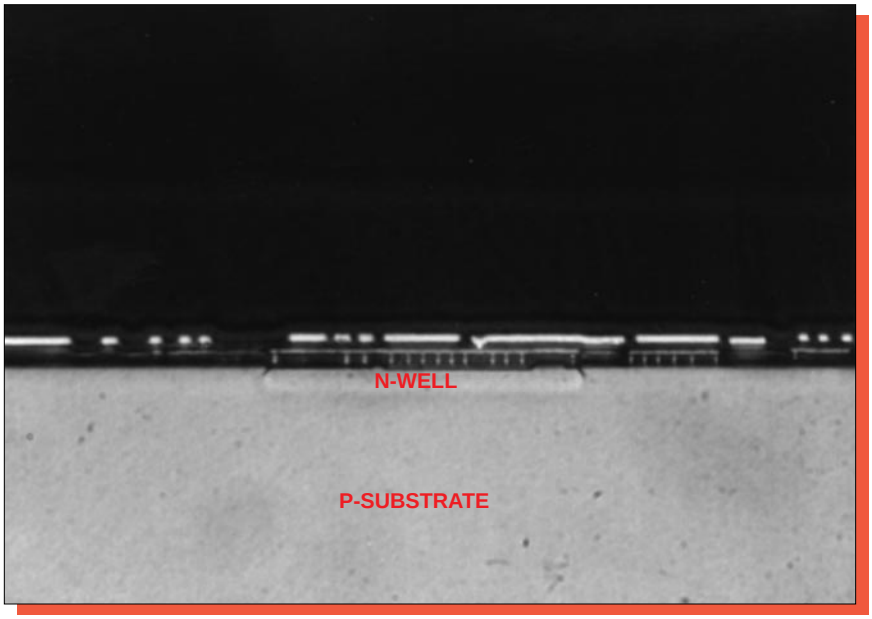
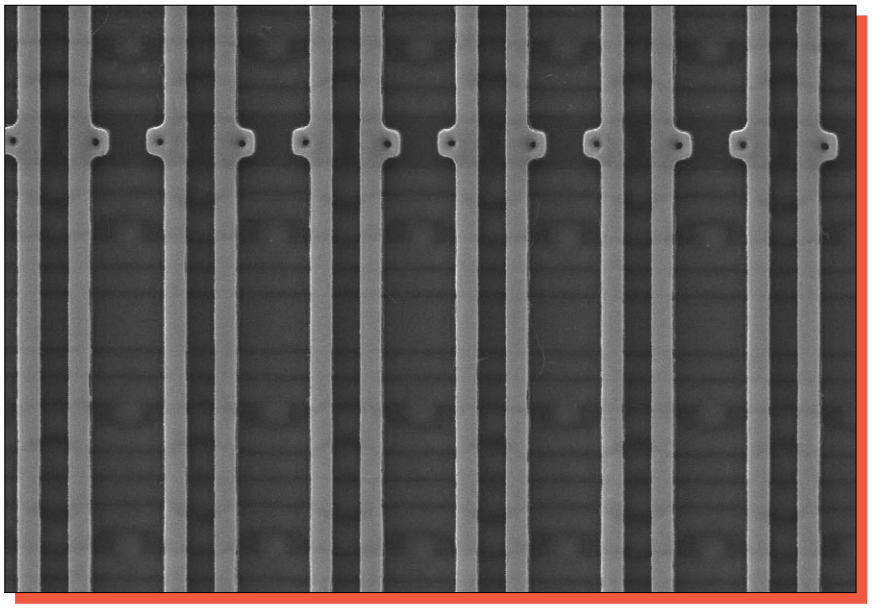
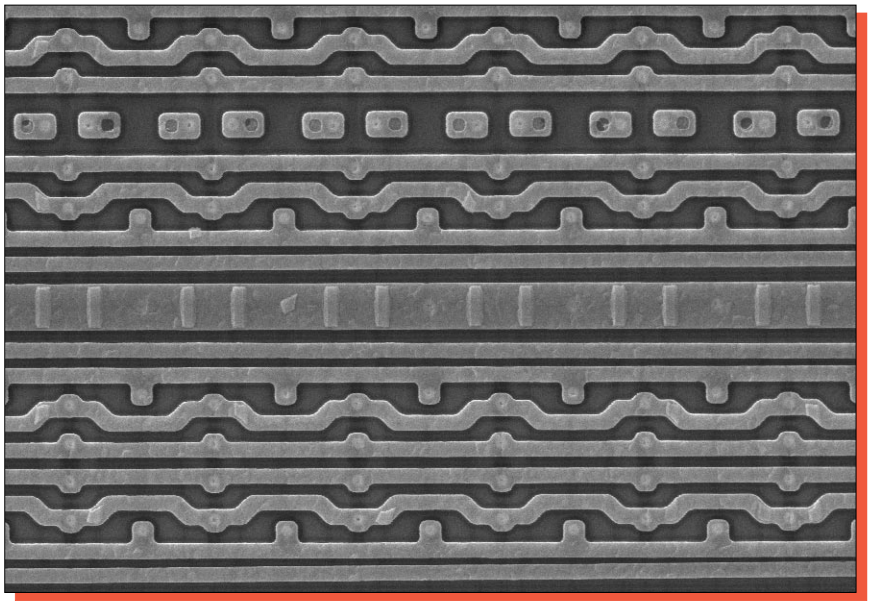


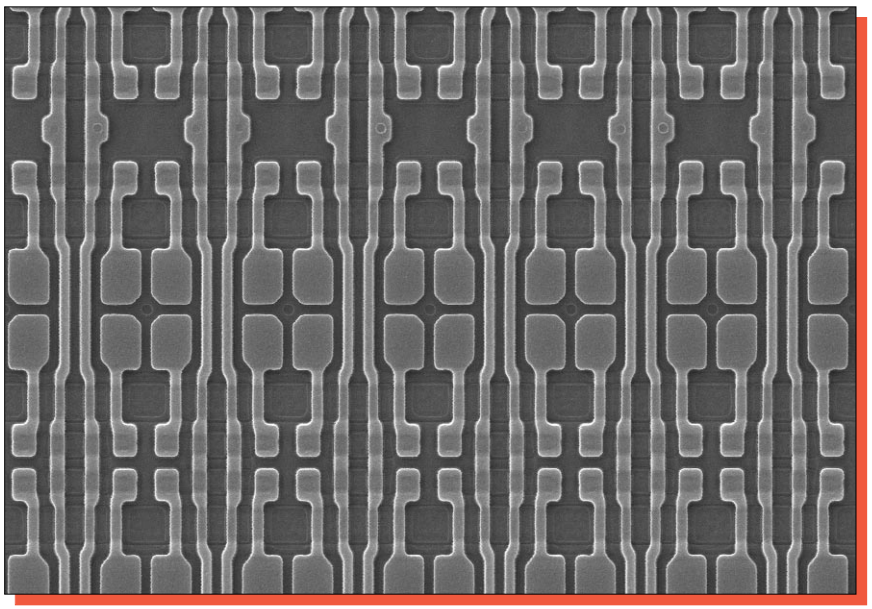
Figure 23. Optical view of the well structure. Mag. 1000x.



metal 2

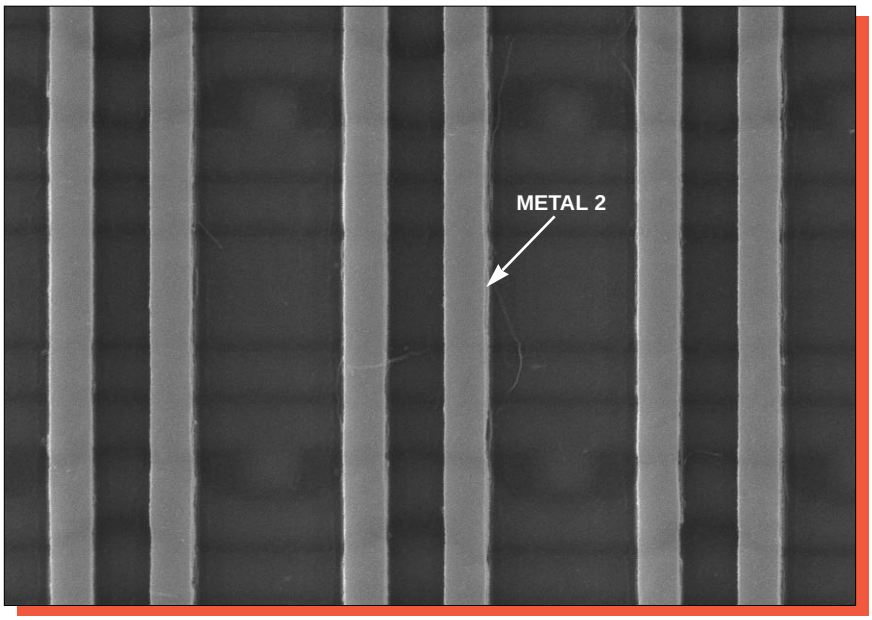


metal 1

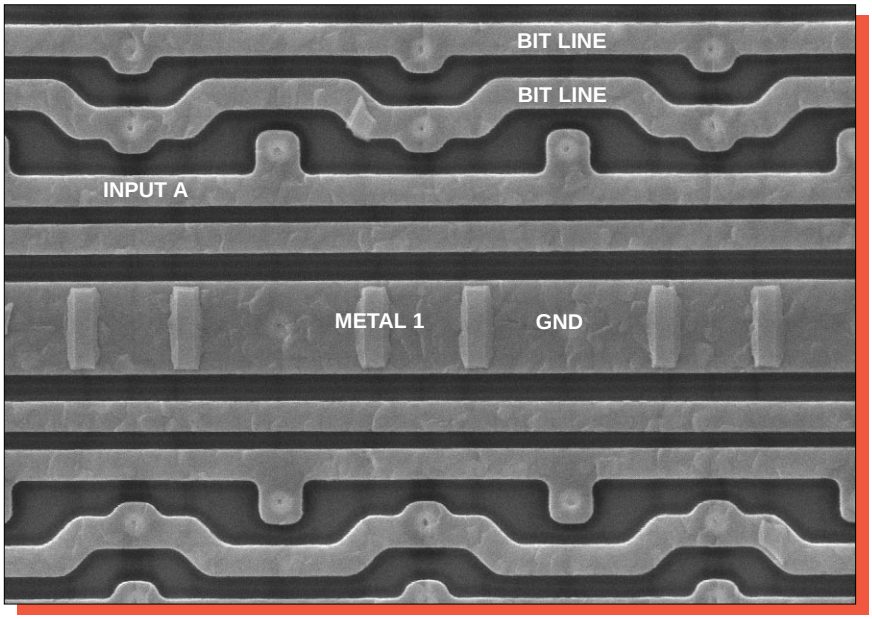


delayered

Figure 24. Topological SEM views of an EEPROM cell array. Mag. 1600x, 0°.

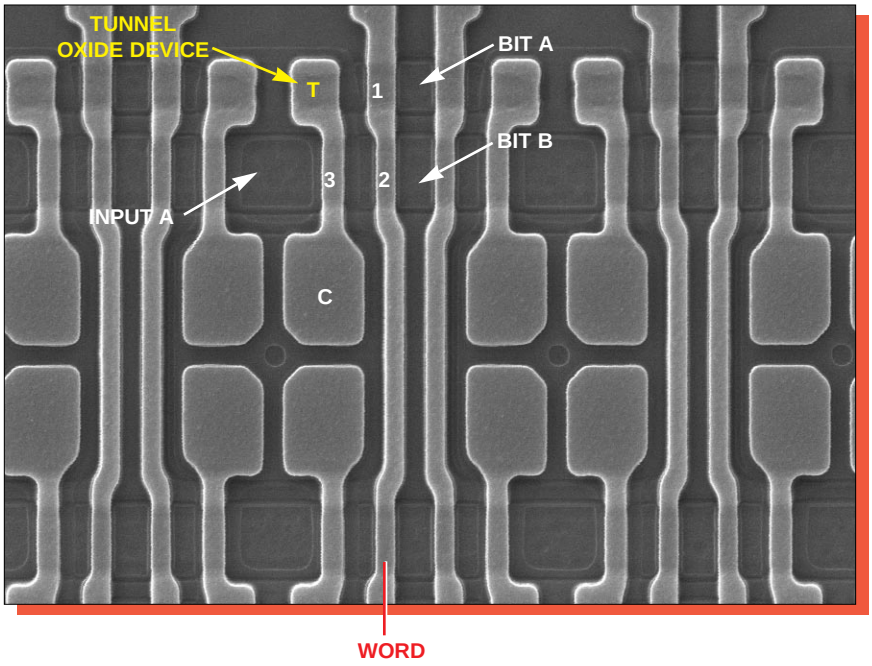


metal 2



metal 1

Figure 25. Detailed SEM views of EEPROM cells. Mag. 3300x, 0°.



unlayered to poly

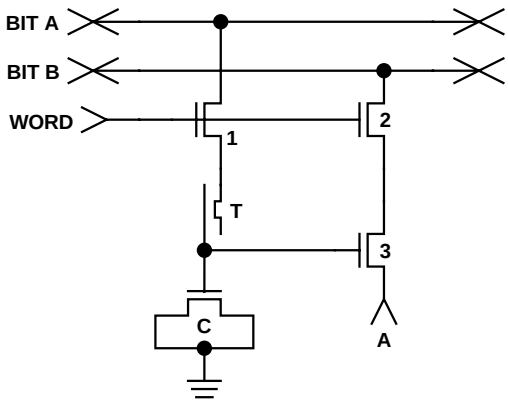
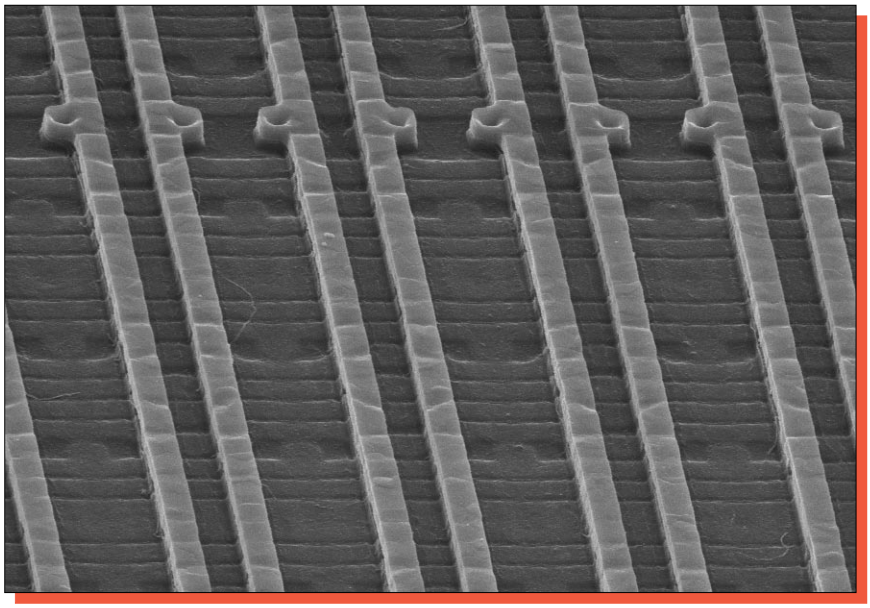
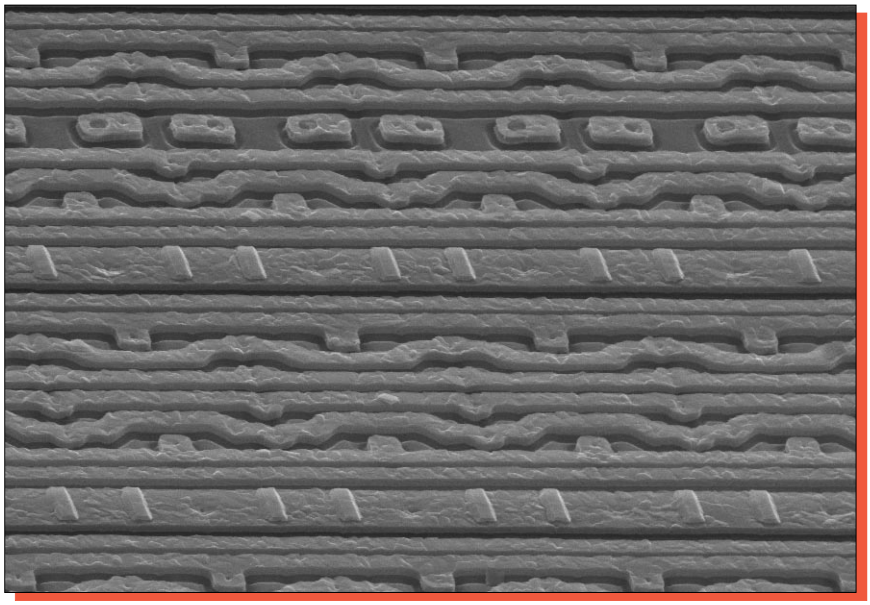


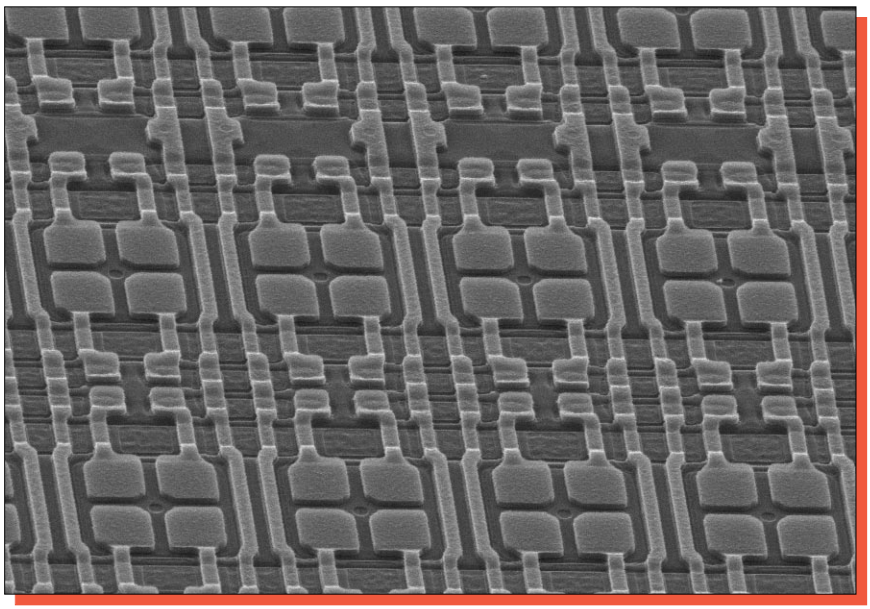
Figure 26. SEM view and schematic of EEPROM cells. Mag. 3300x, 0°.



metal 2



metal 1



unlayered

Figure 27. Perspective SEM views of EEPROM cell array. Mag. 2400x, 60°.

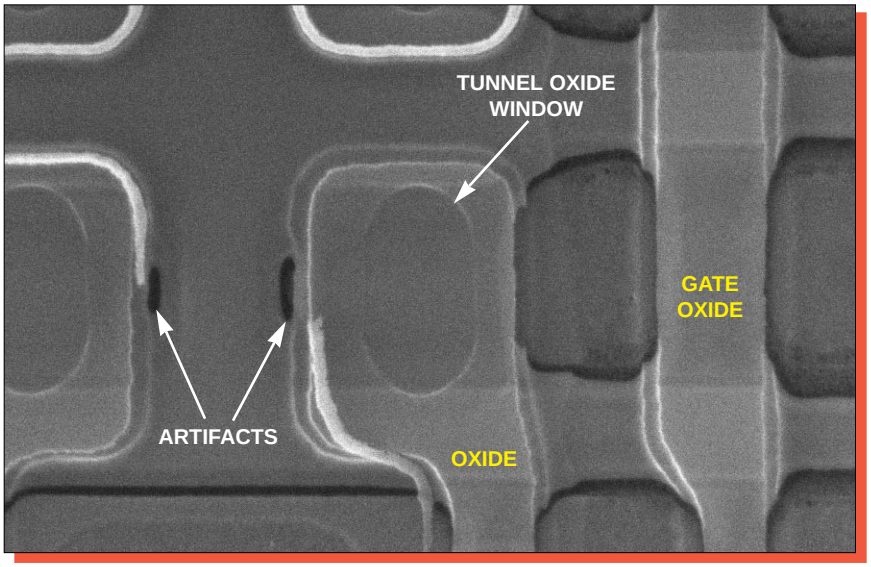


Figure 28. Topological SEM view of an tunnel oxide window.
Mag. 13,500x, 0°.

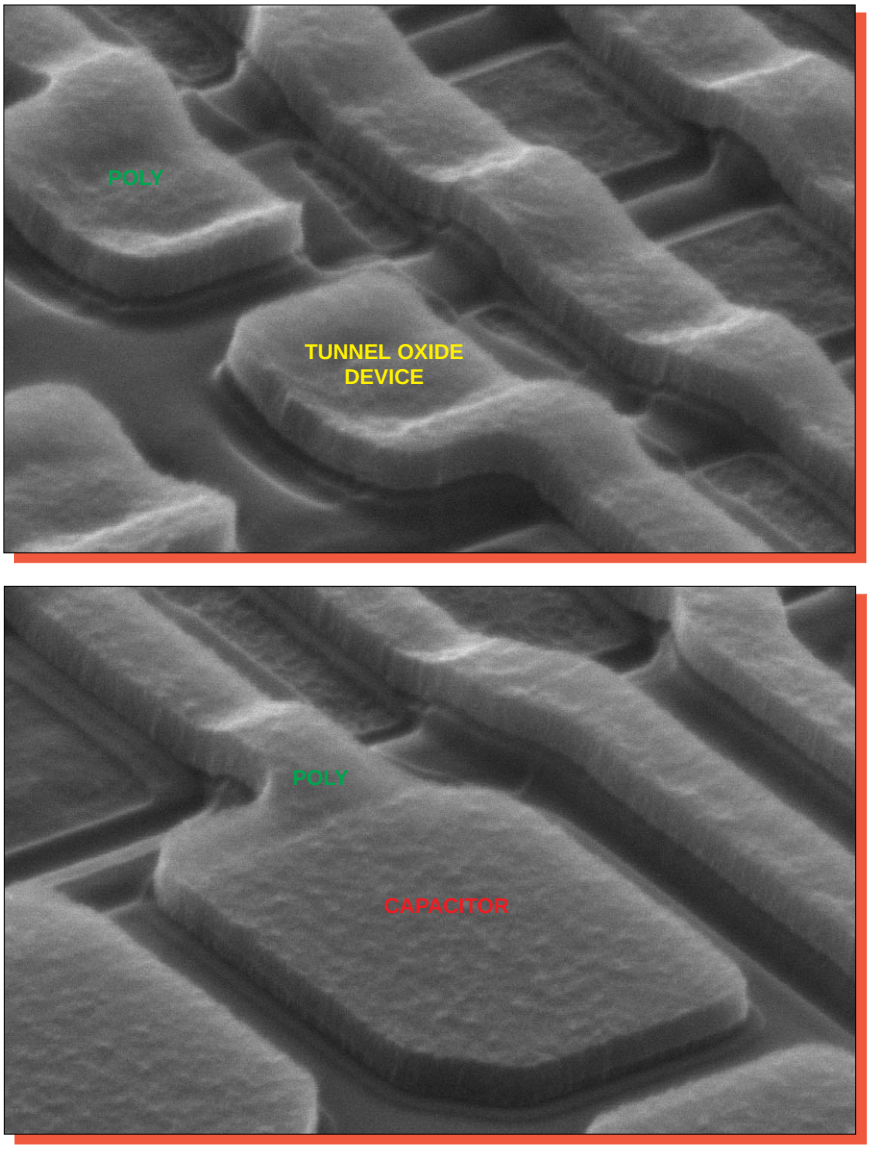
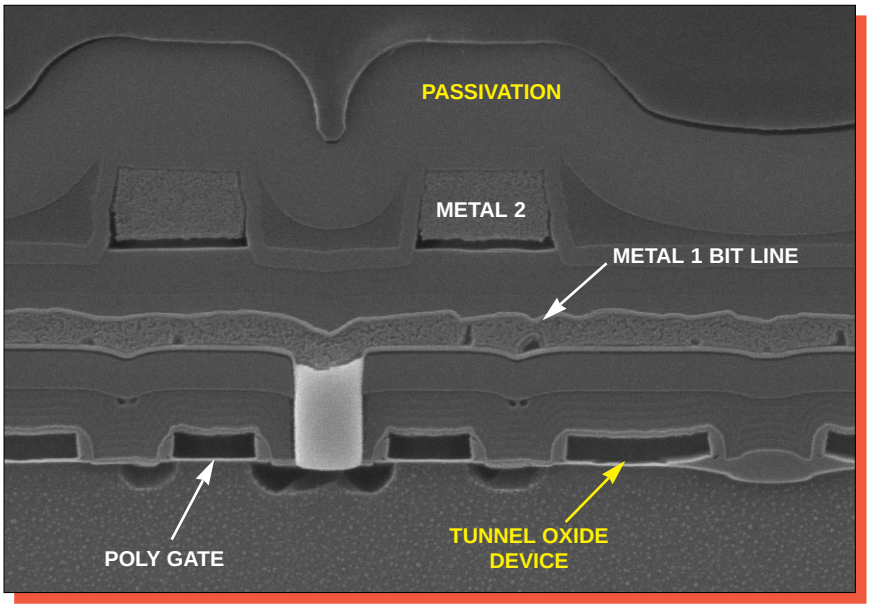
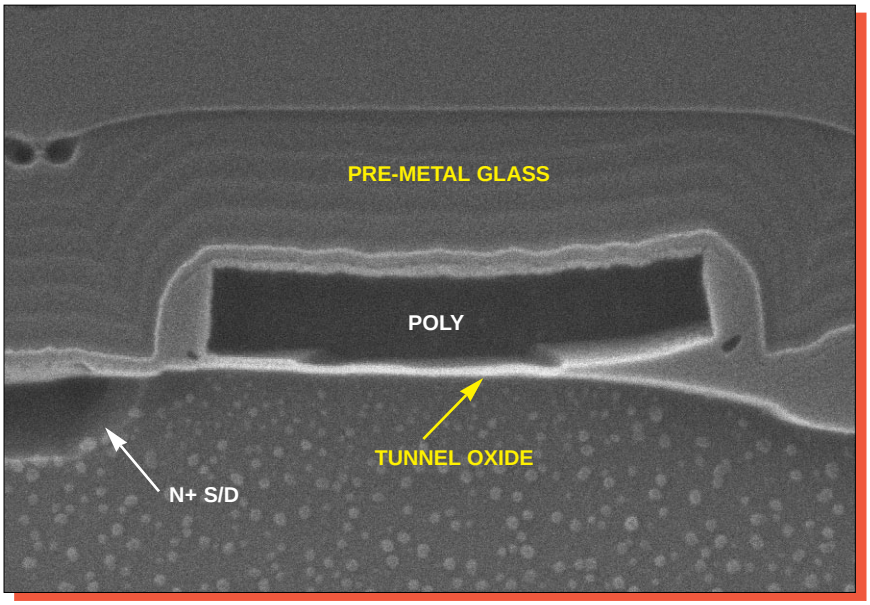


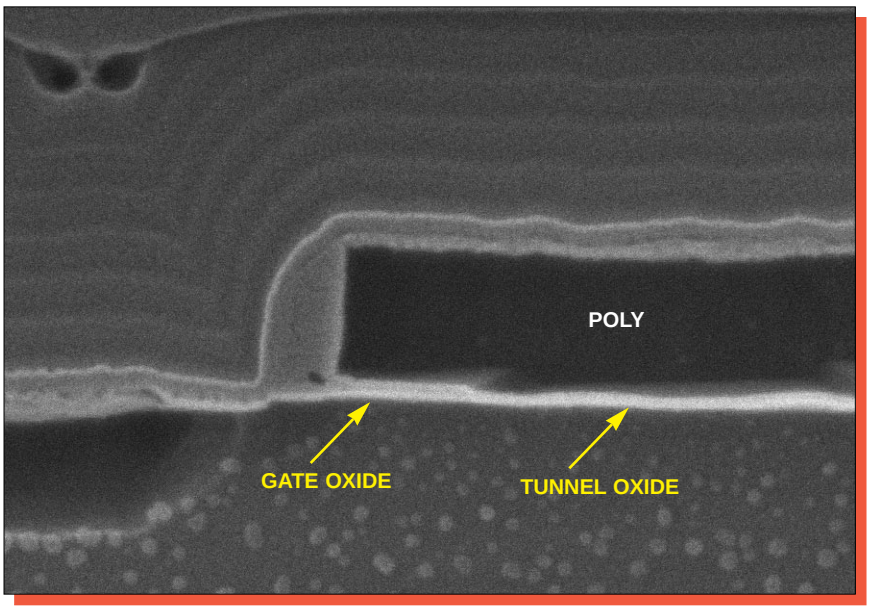
Figure 29. Detailed SEM views of an EEPROM cell. Mag. 16,000x, 60°.



Mag. 10,000x

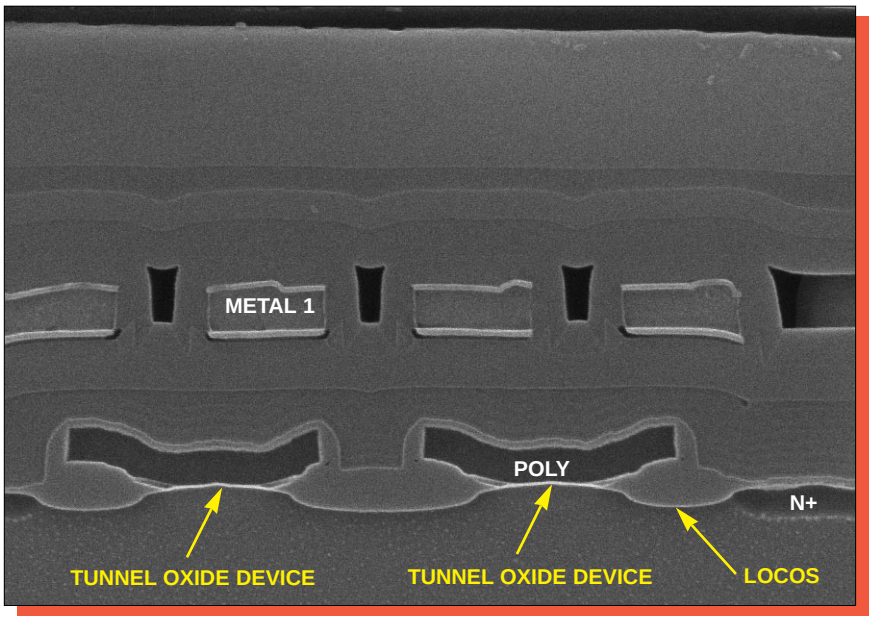


Mag. 35,000x

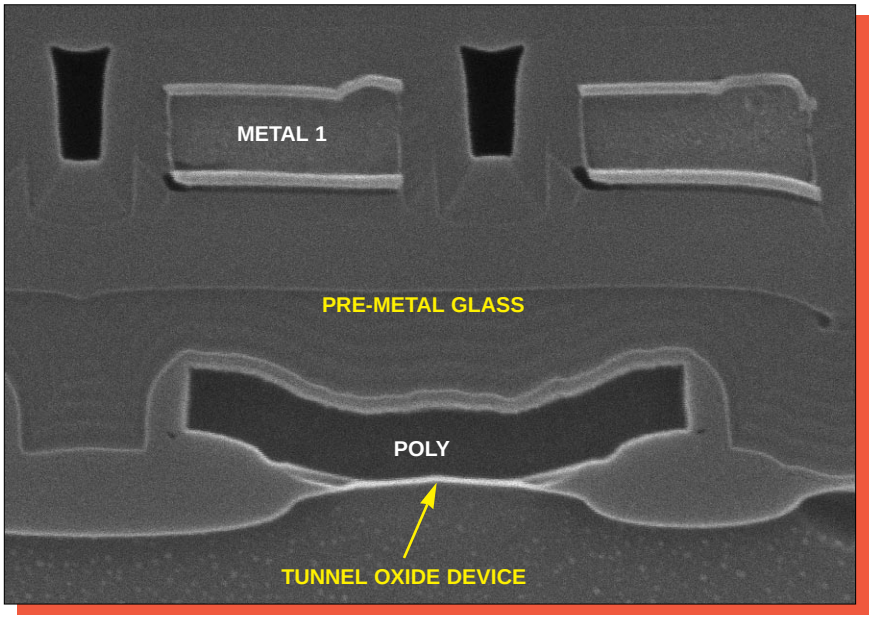


Mag. 52,000x

Figure 30. SEM section views of an EEPROM cell (X-direction).

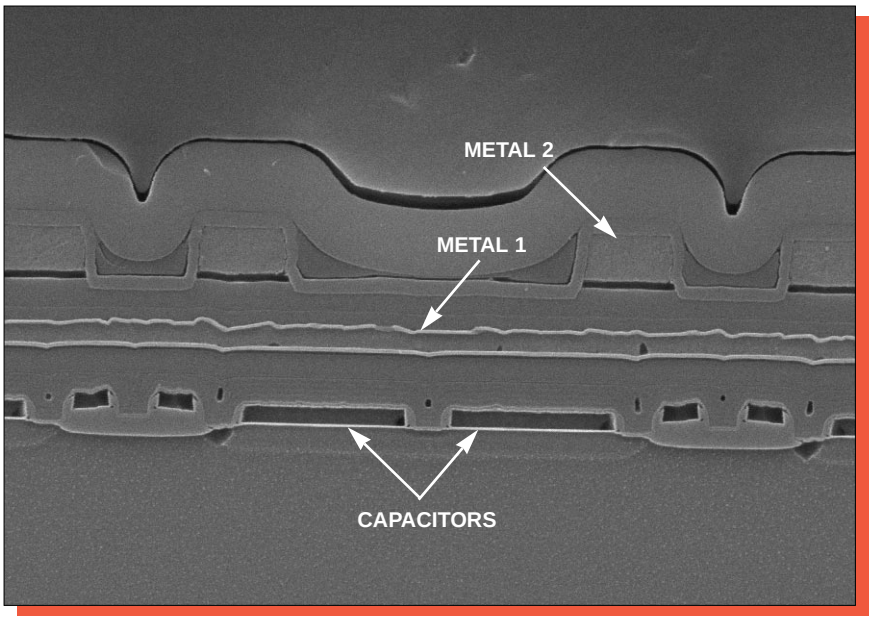


Mag. 13,000x

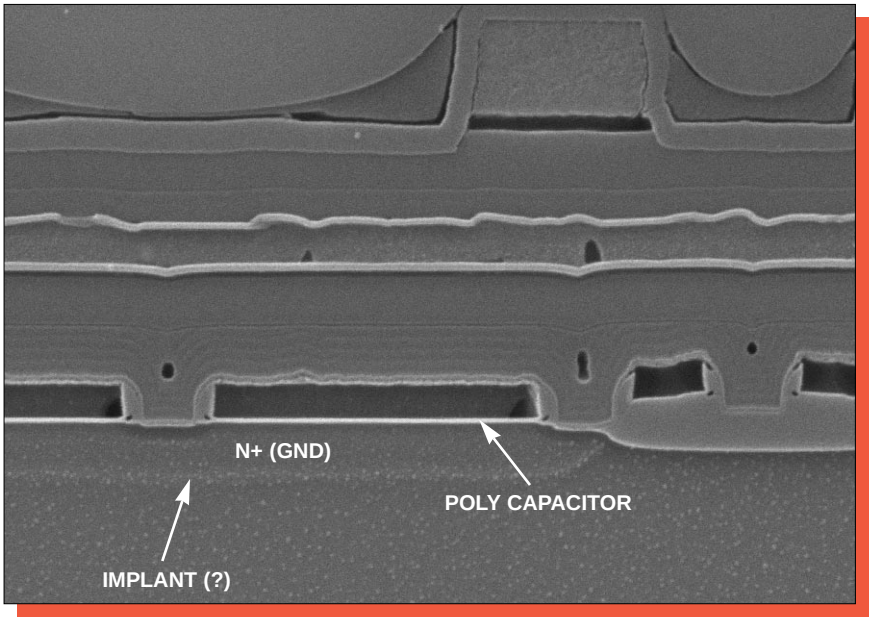


Mag. 26,000x

Figure 31. SEM section views of an EEPROM cell (Y-direction).

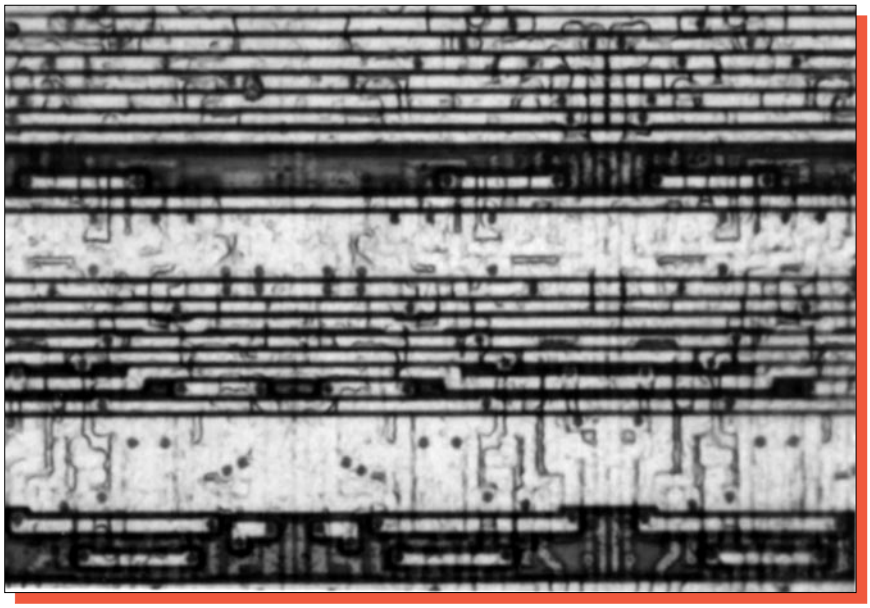


Mag. 6500x

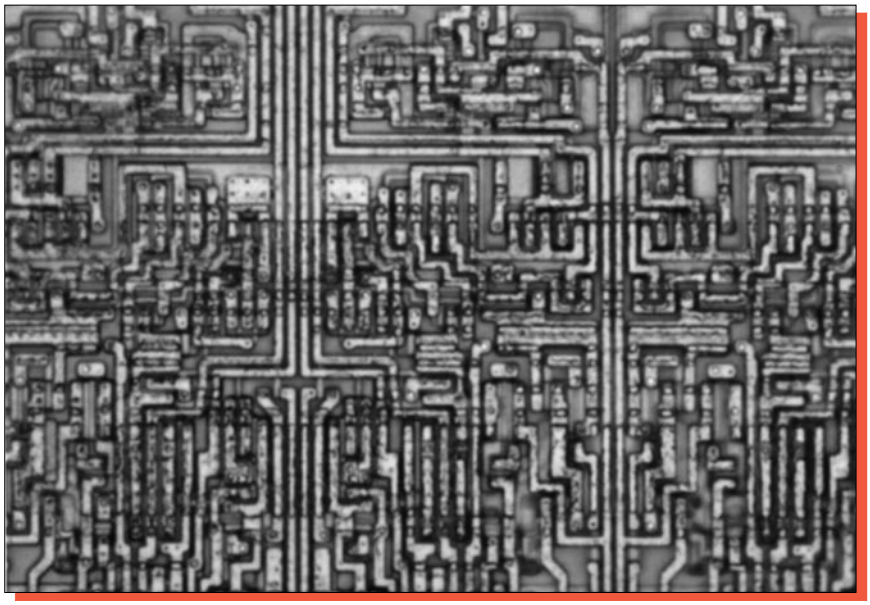


Mag. 13,000x

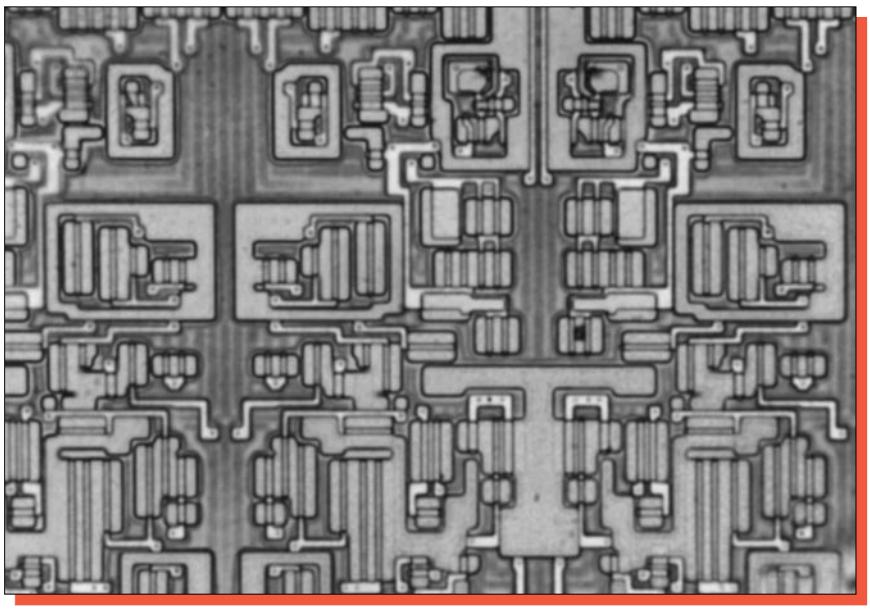
Figure 32. SEM section views of the EEPROM through the capacitor region (X-direction).



metal 2

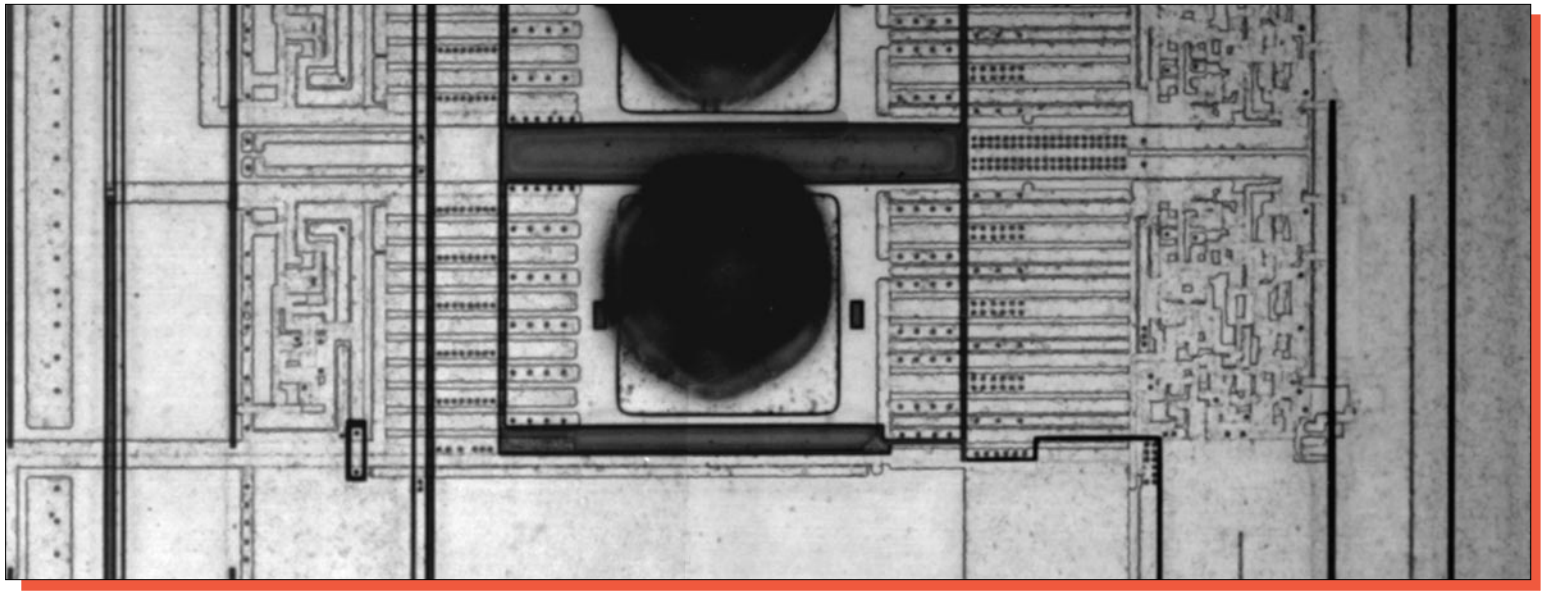


metal 1

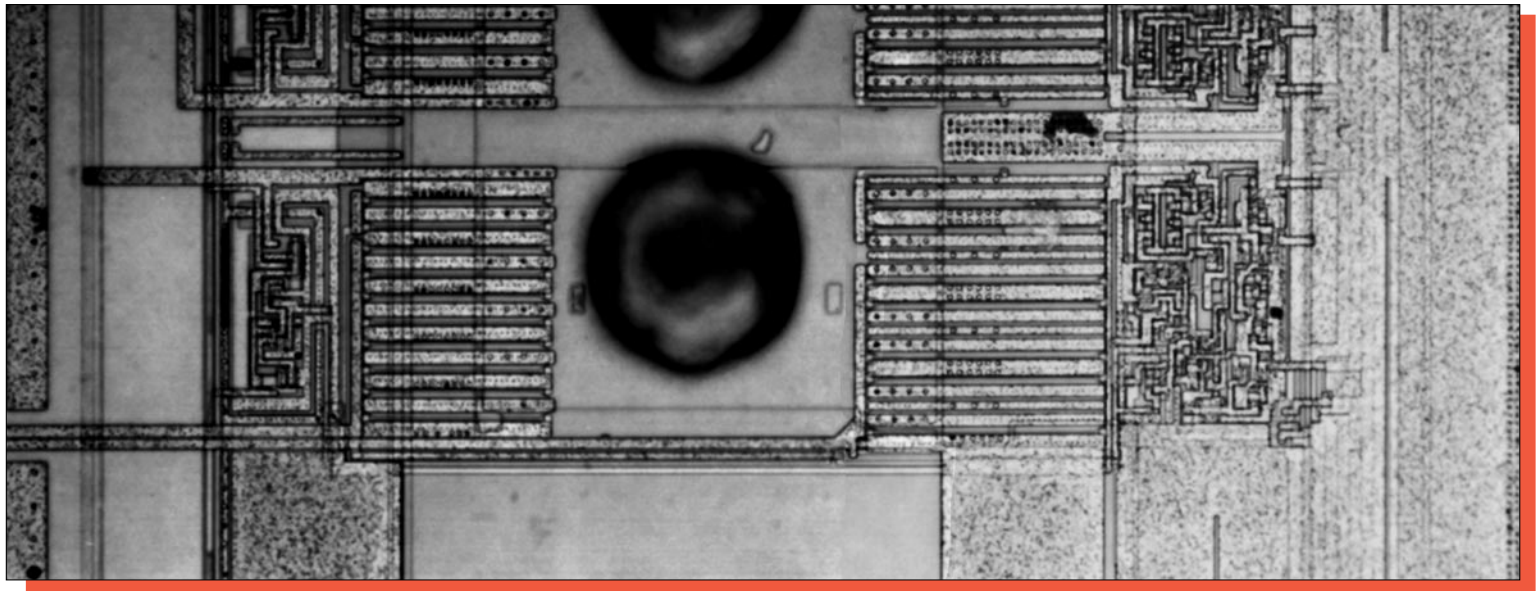


delayered

Figure 33. Optical views of general device circuitry. Mag. 800x.



metal 2



metal 1

Figure 34. Optical views of typical input protection. Mag. 400x.

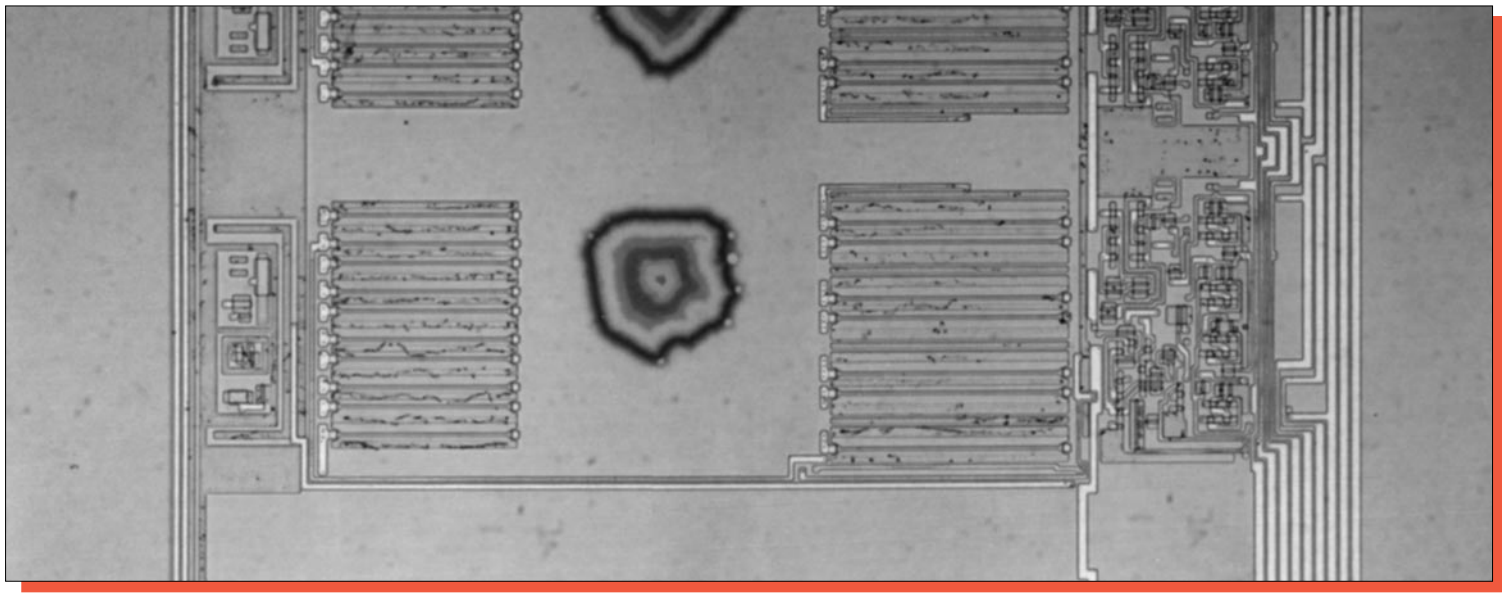
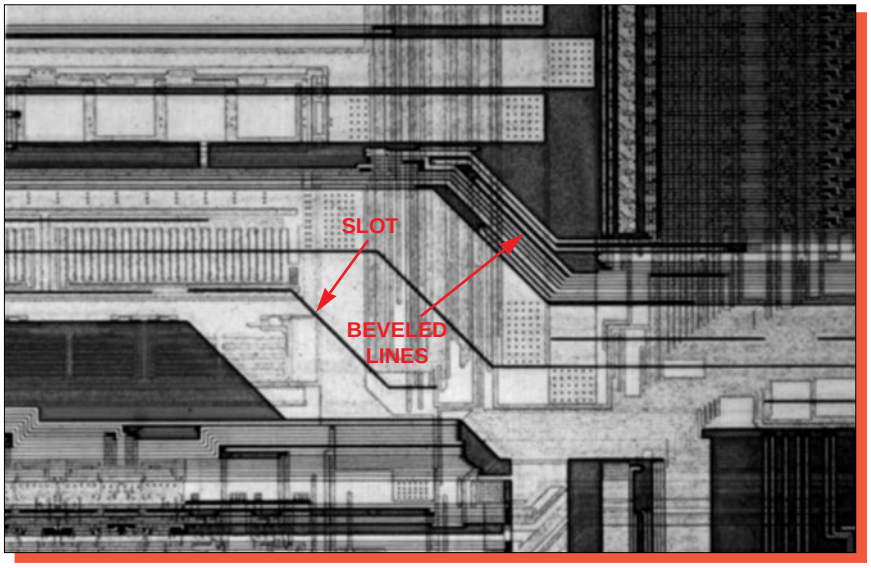
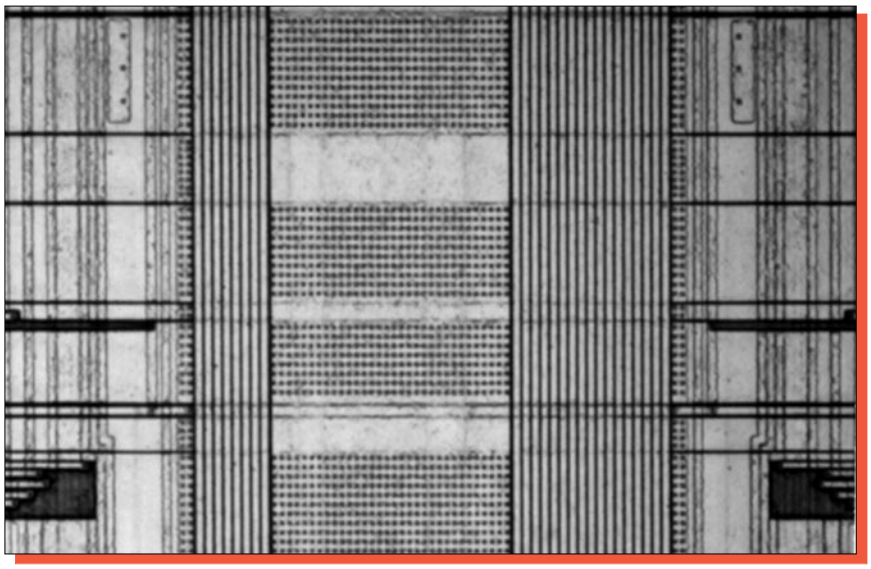


Figure 34a. Optical view of typical input protection (delayered). Mag. 400x.



intact,
Mag. 160x



intact,
Mag. 400x

Figure 35. Optical views of metal design features.

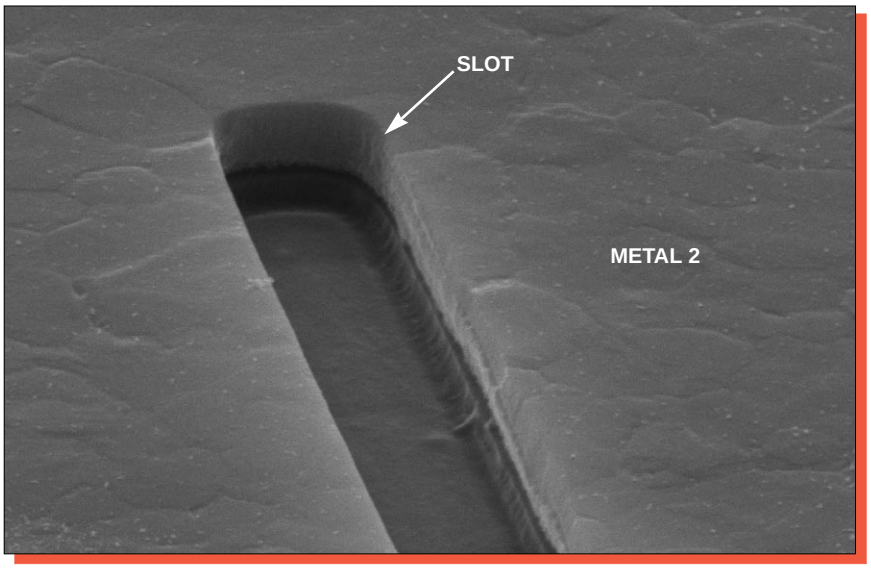


Figure 36. Perspective SEM view of slot cut-out. Mag. 10,000x, 60°.