

Construction Analysis

Dallas Semiconductor DS80C320 Microcontroller

Report Number: SCA 9702-525



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INTRODUCTION

This report describes a construction analysis of the Dallas Semiconductor DS80C320 Microcontroller. Five devices packaged in 44-pin Plastic Leaded Chip Carriers (PLCCs) were received for the analysis. Devices were date coded 9638.

MAJOR FINDINGS

Questionable Items:¹

- Metal thinned up to 85 percent² at some contact edges (Figure 17). No cap or barrier metals were used and this amount of thinning of metal that is only of 0.45 microns nominal thickness should be discussed with the manufacturer.

Special Features:

- An SRAM array and a MROM array were employed on the device.
- Somewhat unusual CMOS process having no reflow glass (uses SOG), and relatively deep S/D diffusions and active loads.
- Large polycide interconnect areas.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 44-pin plastic leaded (PLCC) chip carriers.
- The die was mounted to the paddle using a silver epoxy die attach.
- Die separation was by sawing.
- Wirebonding was by the thermosonic ball bond method using 1.1 mil O.D. gold wire.
- Lead-locking provisions (anchors and holes) at all pins.

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of a layer of nitride over a thick layer of silicon-dioxide.
- Metallization consisted of a single layer of dry-etched metal. The metal layer consisted of aluminum and did not use a cap or barrier. Standard contacts were used (no plugs).
- Pre-metal dielectric consisted of a layer of phosphosilicate glass (PSG) over densified oxides and covered with a layer of SOG. The glass was not reflowed.

TECHNOLOGY DESCRIPTION (continued)

- A single layer of polycide was used (tungsten-silicide). It was used to form all gates on the die and the word lines in both memory arrays. It was also used as a layer of interconnect. Direct poly-to-diffusion (buried) contacts were not used. Definition of the poly was by a normal dry etch.
- Fairly deep implanted N⁺ and P⁺ diffusions formed the sources/drains of the CMOS transistors. Oxide sidewall spacers on the gates were left in place.
- Local oxide (LOCOS) isolation. A slight step was present in the oxide at the edge of the well boundaries indicating a twin-well process was used.
- SRAM array: A 6T SRAM cell design. Metal was used to form the bit lines. Poly was used to form the word/select lines, storage gates and pull-up devices. Long active P-channel loads were employed.
- MROM arrays: Metal formed the bit lines and poly formed the word lines. The array was programmed at the field oxide (diffusion) level (see Figures 29 and 30).
- Redundancy fuses were not present.

ANALYSIS RESULTS I

Package and Assembly:

Figures 1 - 9

Questionable Items:¹ None.

Special Features: None.

General Items:

- Devices were packaged in 44-pin plastic leaded (PLCC) chip carriers.
- Overall package quality: Good. No significant defects were noted on the external or internal portions of the package. No cracks or voids were noted in the plastic.
- Leadframe: The leadframe was constructed of copper. External tinning consisted of tin-lead (SnPb) while internal plating consisted of silver (Ag). No gaps were noted at lead exits.
- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present.
- Die attach: A silver epoxy of normal quality was used to attach the die to the header. No significant voids were noted in the die attach.
- Wirebonding was by the thermosonic ball bond method using 1.1 mil O.D. gold wire. Bonds were well formed and placement was good. Wirepull strengths were normal with no bond lifts (see page 10).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process:

Figures 10 - 32b

Questionable Items:¹ None.

Special Features:

- An SRAM array and a MROM array were employed on the device.
- Somewhat unusual CMOS process having no reflow glass (uses SOG), and relatively deep S/D diffusions and active loads.
- Large polycide interconnect areas.

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good as it extended into the scribe lane to seal the metallization.

¹*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

²*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metallization: A single layer of metal consisting of aluminum. No cap or barrier metals was used.
- Metal patterning: The metal layer was patterned by a dry etch of normal quality. All contacts were completely surrounded by aluminum.
- Metal defects: No voiding, notching, or neckdown was noted in the metal layer. No silicon nodules were noted following the removal of the aluminum layer.
- Metal step coverage: **Worst case aluminum thinning was 85 percent at contact edges.** MIL-STD allows up to 70 percent metal thinning for contacts of this size, but in this case the metal already seems to be unusually thin normally, and no cap or barriers are present. Typical aluminum thinning was 60 percent.
- Pre-metal dielectric: A layer of SOG over a layer of phosphosilicate glass over densified oxides was used under the metal. No reflow was performed. This is a somewhat unusual structure but no problems were found.
- Contact defects: None. No significant over-etching of the contacts was noted and no pitting or silicon mound growth was present.
- Polysilicon: A single layer of polycide (tungsten- silicide) was used to form all gates on the die and for interconnect (crossunders). Slots were noted within some of the large poly crossunders (Figures 32a and 32b). Direct poly-to-diffusion (buried) contacts were not used. Poly “links” are inactive and appear to have been a mask modification (Figure 21). Definition was by a dry etch of normal quality.
- Diffusions: Fairly deep implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. Oxide sidewall spacers were used at all gates and left in place. No silicide was present on the diffusions.

ANALYSIS RESULTS II (continued)

- Local oxide (LOCOS) isolation was used. No problems were noted. The slight step present in the oxide at the well boundary indicates a twin-well process was employed.
- SRAM array: Two blocks of SRAM memory were present. A 6T SRAM cell design was employed. Metal was used to form the bit lines. Poly was used to form the word/select lines, storage gate and pull-up devices. Cell pitch was relatively large 12.2 x 22.8 microns.
- MROM array: Two separated blocks of MROM arrays were present on the device. Metal formed the bit lines and poly formed the word lines. No problems of any sort were noted in the SRAM nor MROM arrays. Both arrays were programmed at the field oxide (diffusion) level (see Figures 29 and 30).
- Special items: ESD tests were performed on Sample 4 and revealed that all pins passed pulses of +4000V.
- Latch-up tests were performed on Sample 5 and revealed that no pin latched-up.

PROCEDURE

The devices were subjected to the following analysis procedures:

- External inspection
- ESD and Latch-up tests
- X-ray
- Package section
- Decapsulate
- Internal optical inspection
- SEM of passivation and assembly features
- Passivation integrity test
- Wirepull test
- Passivation removal
- SEM inspection of metal
- Metal removal
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal to Poor*

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver epoxy
Dicing method	Sawn
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	NP*
Contact coverage	G
Contact registration	G

*Metal thinning up to 85 percent on metal that is only 0.45 micron thick.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (TOP)

DALLAS
DS80C320
9638B3-QCG

(BOTTOM)

KOREA
478AA

WIREBOND STRENGTH

Wire material: 1.1 mil O.D. gold
Die pad material: aluminum

Sample # 1
of wires pulled: 15
Bond lifts: 0
Force to break - high: 17g
- low: 15g
- avg.: 15.8g
- std. dev.: 0.9

DIE MATERIAL ANALYSIS (EDX and WDX)

Overlay passivation:† A layer of nitride over a layer of silicon- dioxide.
Metallization: Aluminum (Al).
Pre-metal dielectric:† A phosphosilicate glass (PSG) containing 3.6 wt. % phosphorus. No boron was detected. Topped with a layer of SOG.
Polycide: Tungsten (W) silicide.

†WDX analysis.

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MROM MEMORY CELLS	Figures 29 - 30
INPUT PROTECTION CIRCUIT	Figure 31
GENERAL CIRCUIT LAYOUT	Figure 32
POLY DESIGN FEATURES	Figures 32a and 32b

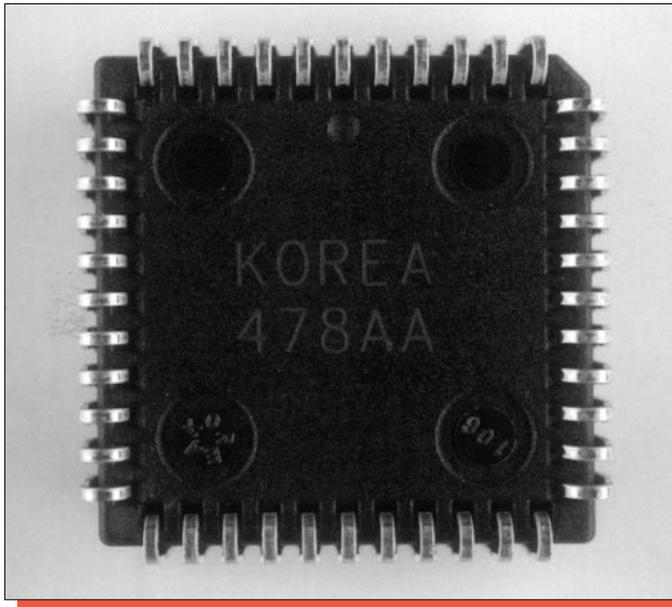
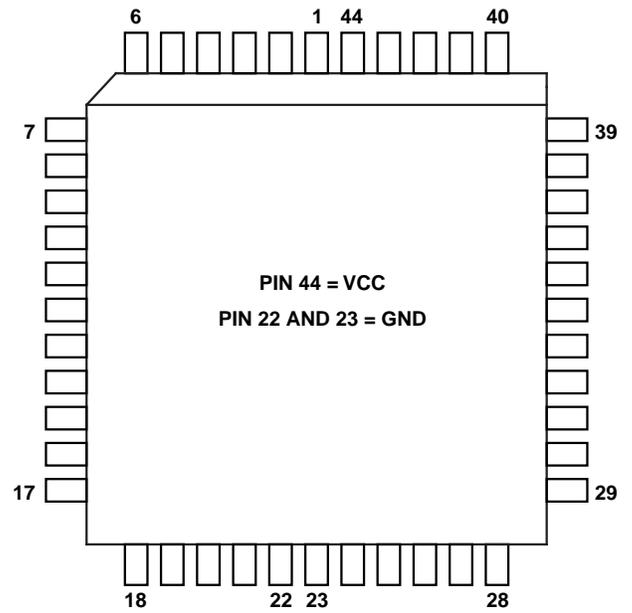
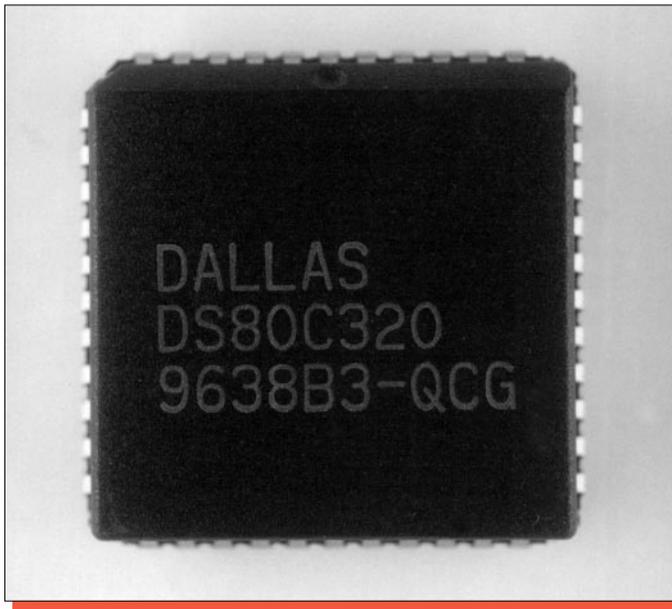
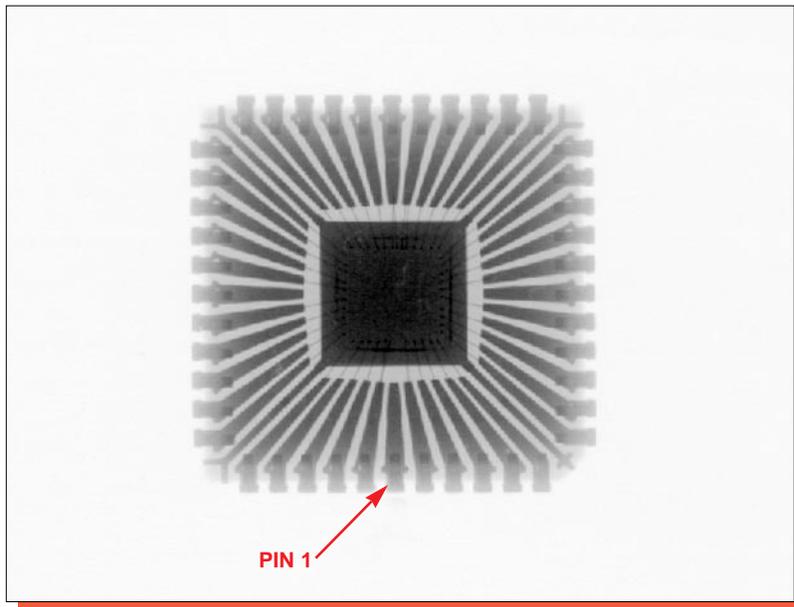
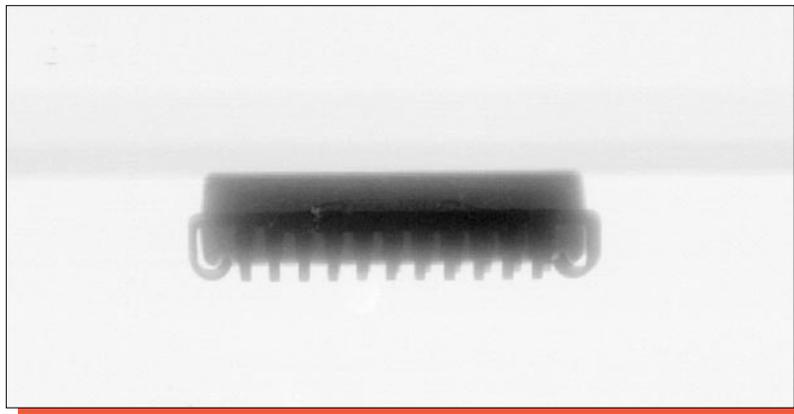


Figure 1. Package photographs and pinout of the Dallas Semiconductor DS80C320.
Mag. 3x.



top view



side view

Figure 2. X-ray views of the package. Mag. 3x.

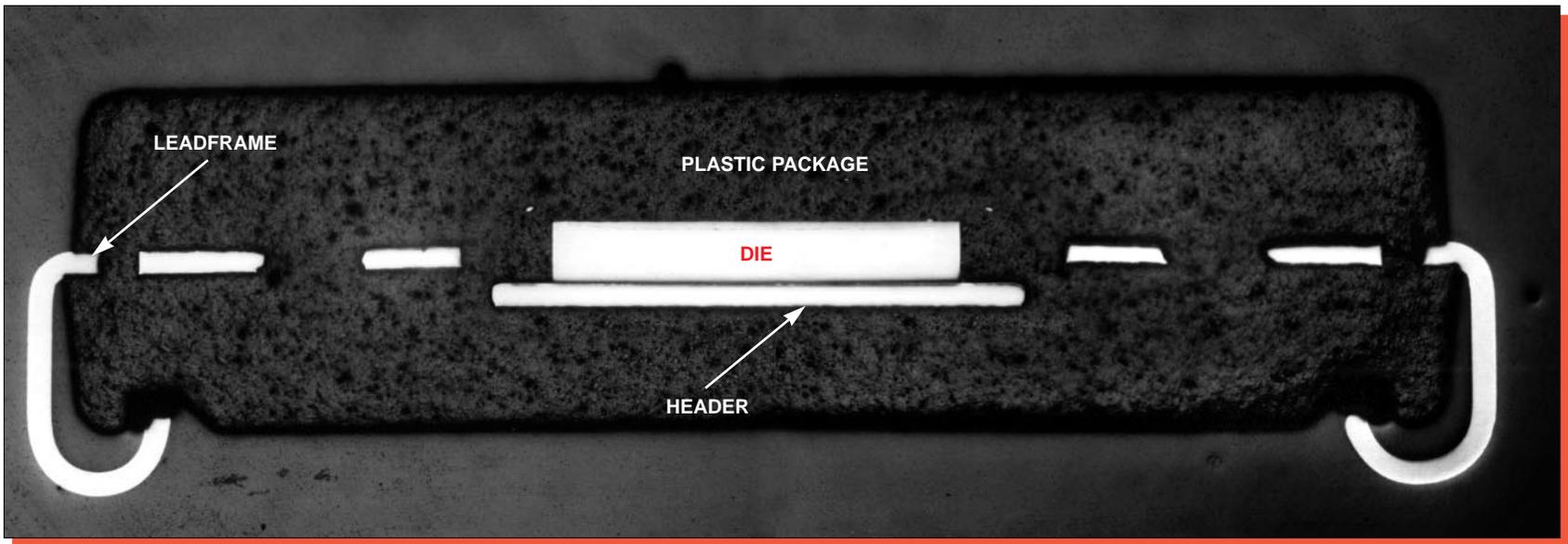
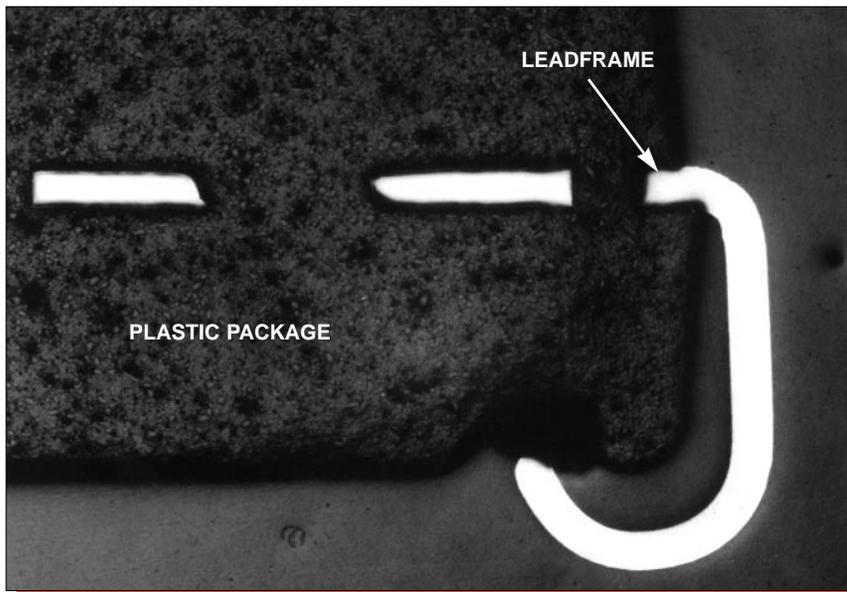


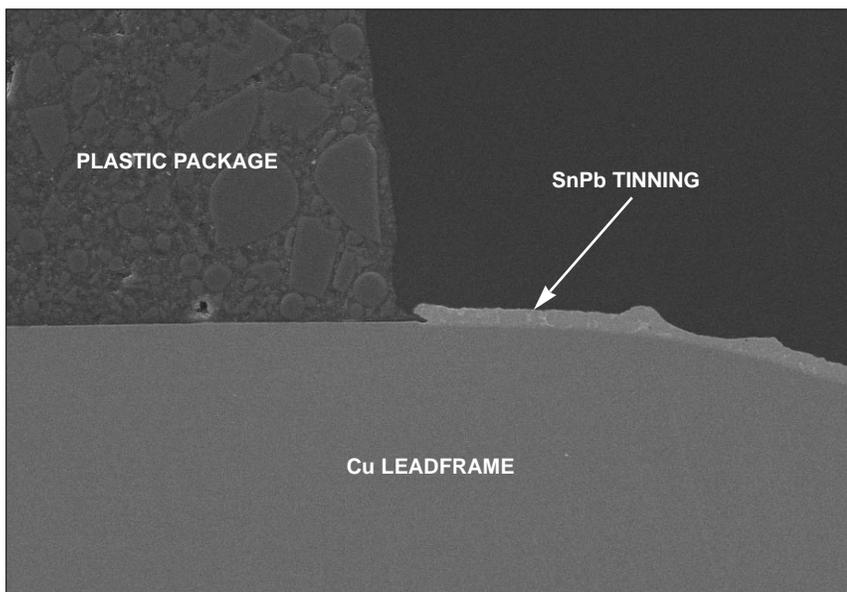
Figure 3. Package section views illustrating general package construction. Mag. 13x.



Mag. 20x

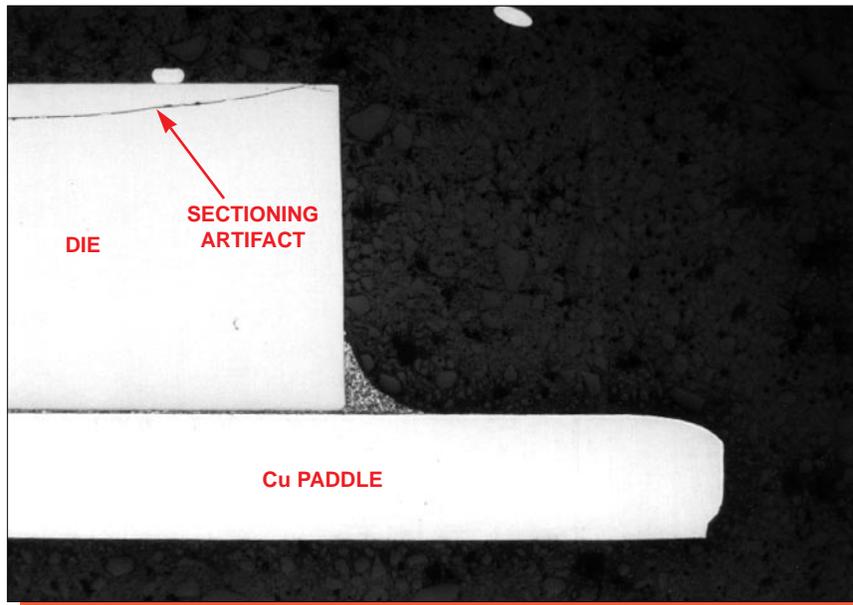


Mag. 100x

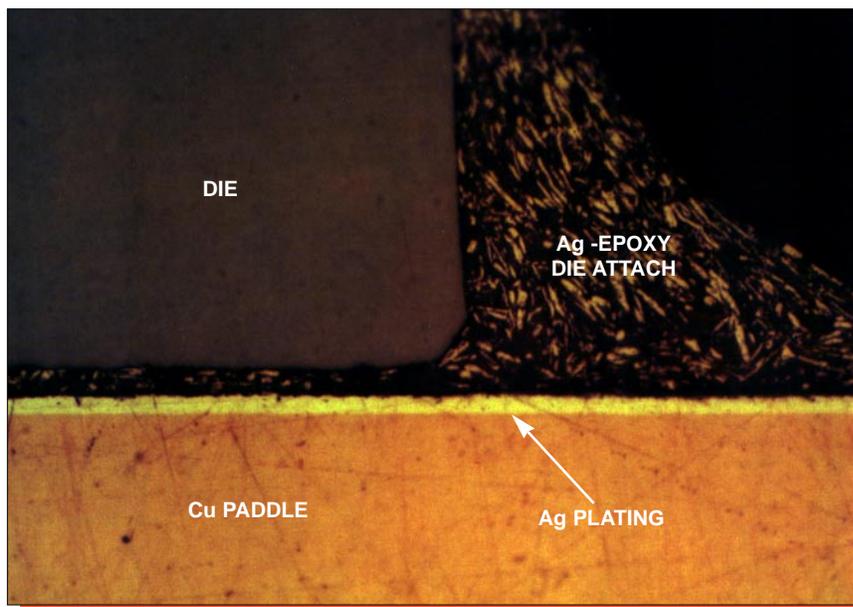


Mag. 300x

Figure 4. Optical and SEM views of lead forming and lead plating.

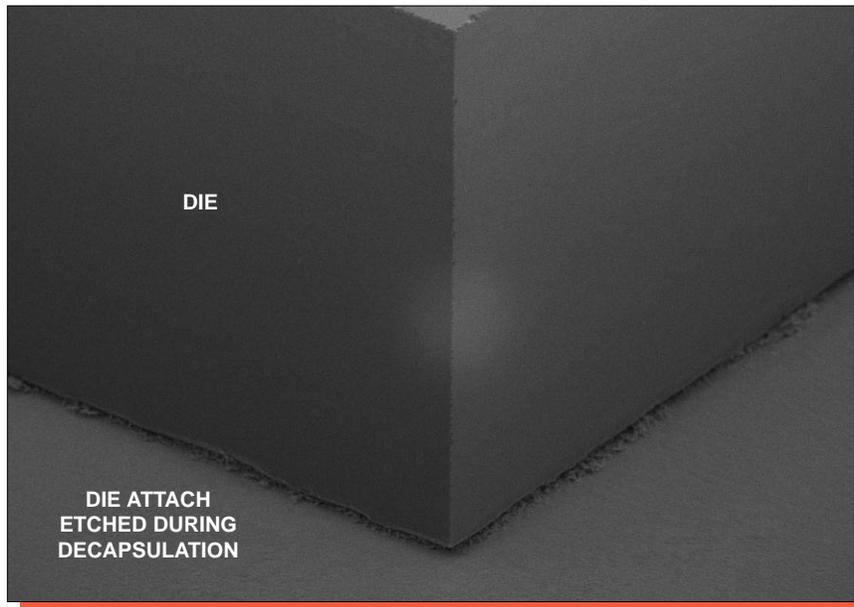


Mag. 65x

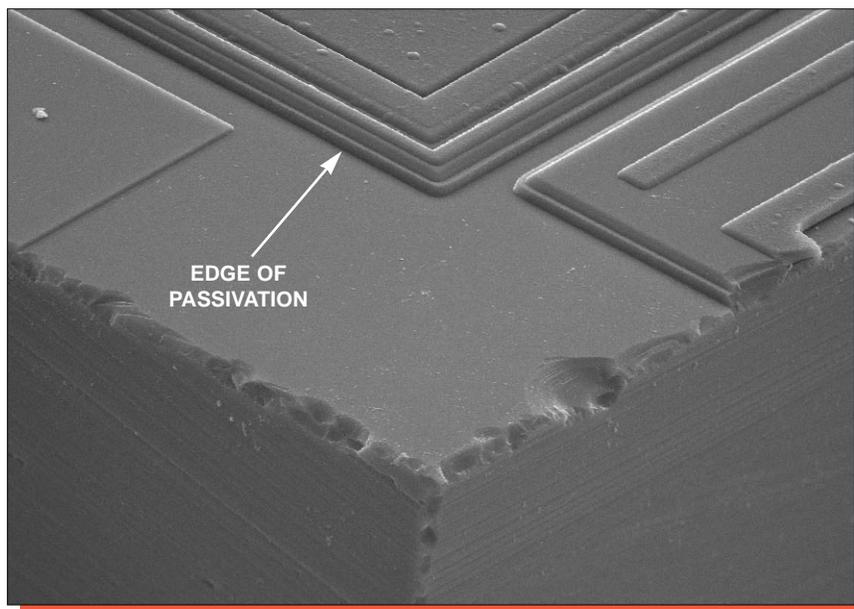


Mag. 500x

Figure 5. Optical package section views of die dicing and die attach.

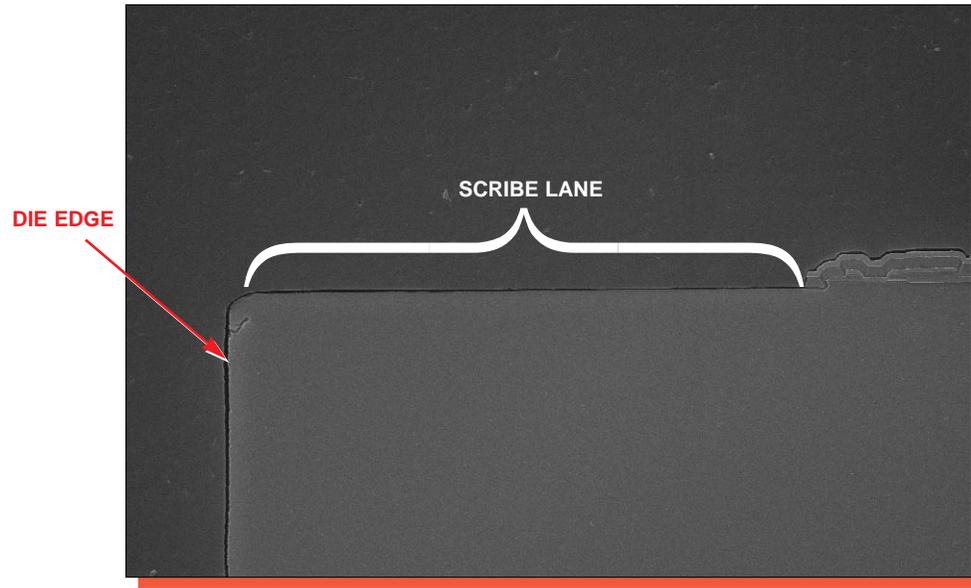


Mag. 120x

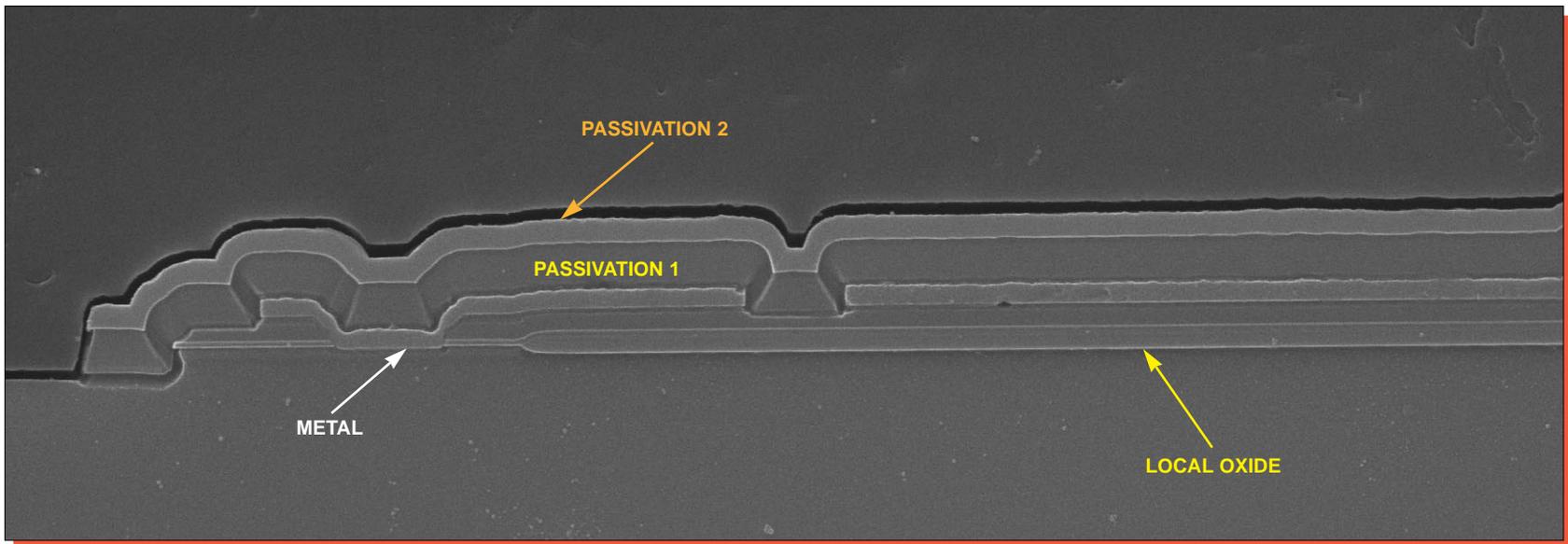


Mag. 1000x

Figure 6. SEM views of dicing and die edge seal. 60°.



Mag. 1400x



Mag. 6500x

Figure 7. SEM views of the edge seal.

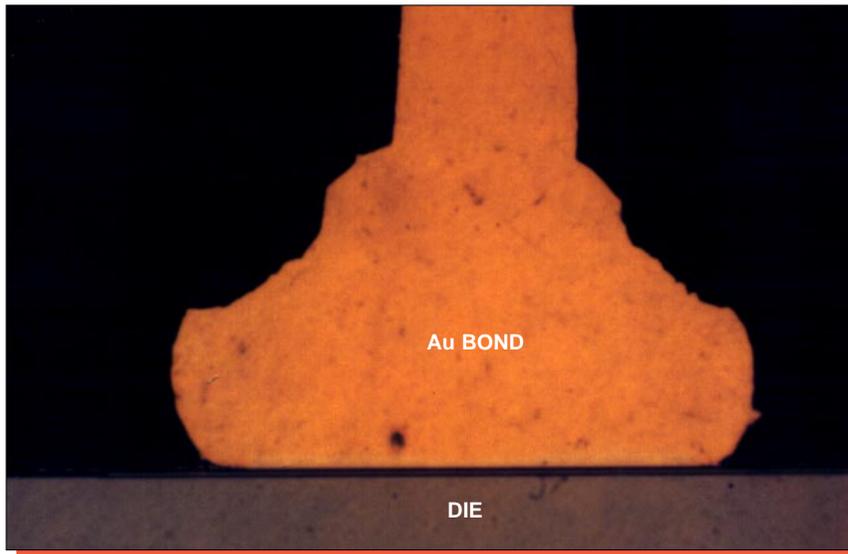
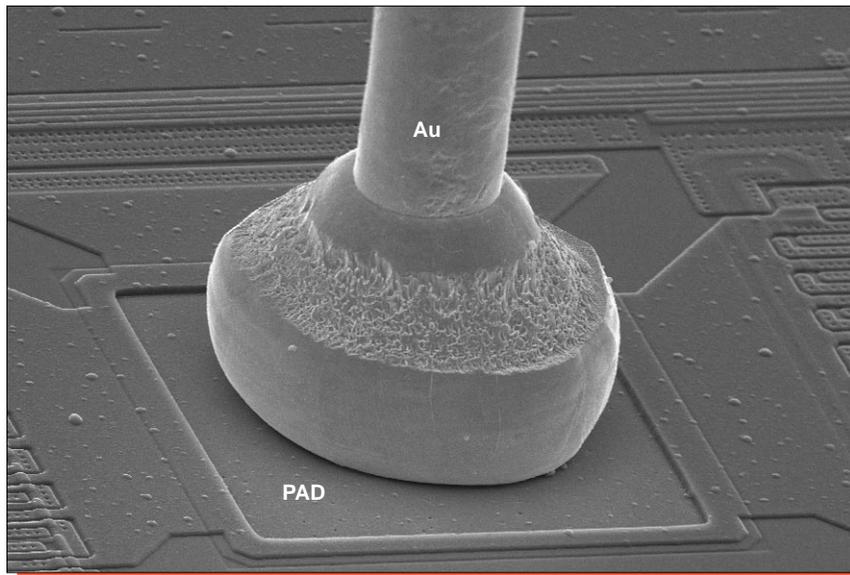
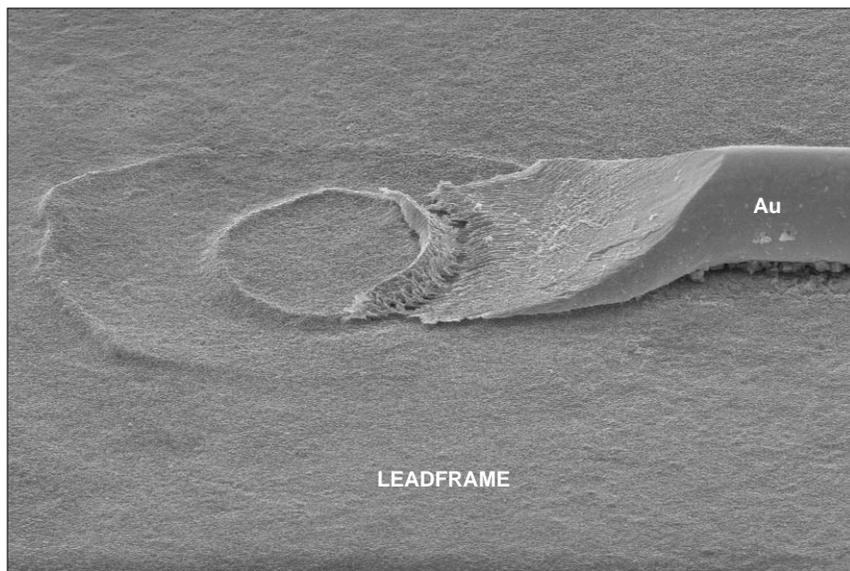


Figure 8. Optical section view of a typical ball bond. Mag. 800x.



Mag. 600x



Mag. 500x

Figure 9. SEM views of typical wirebonds. 60°.

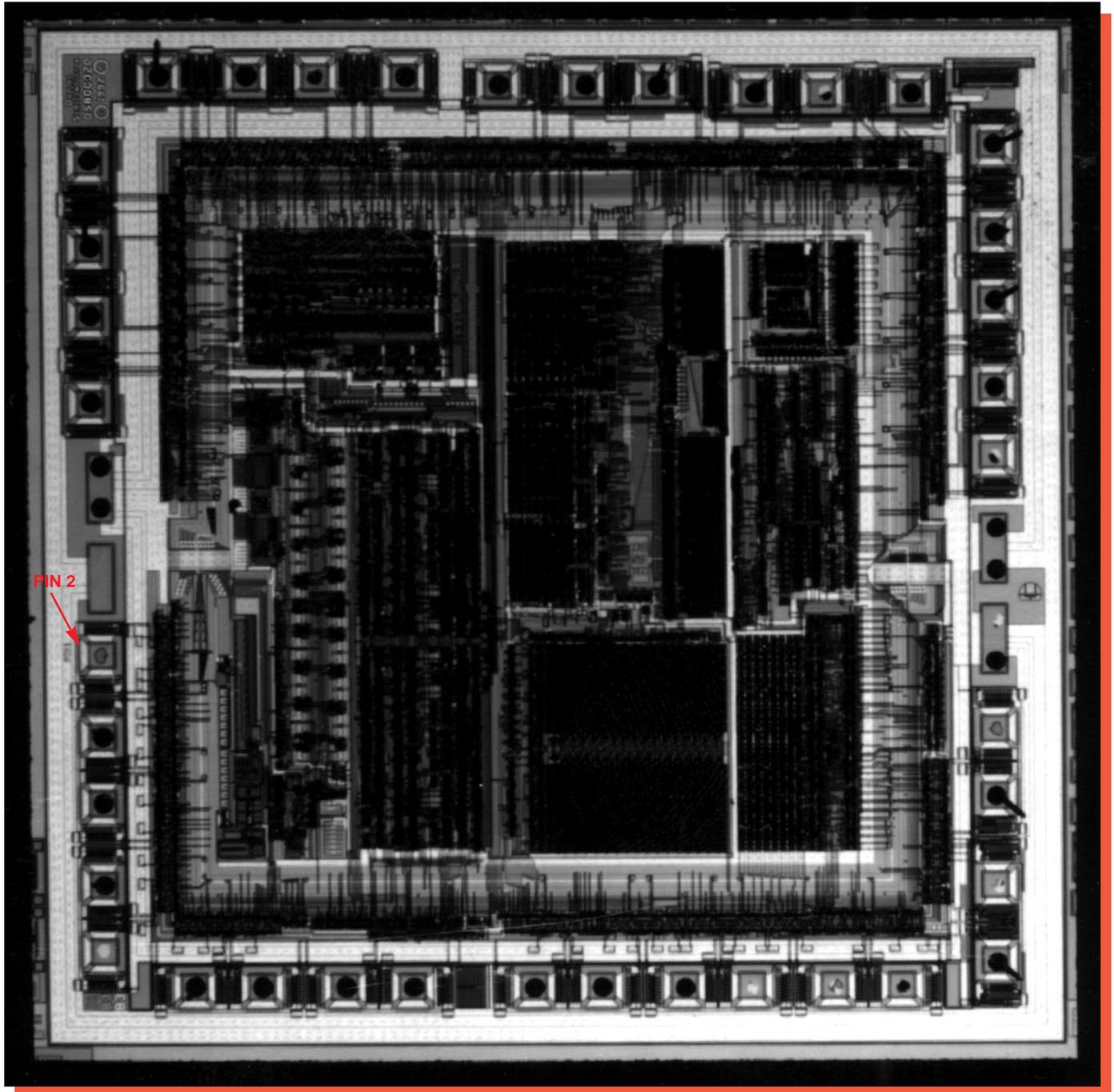
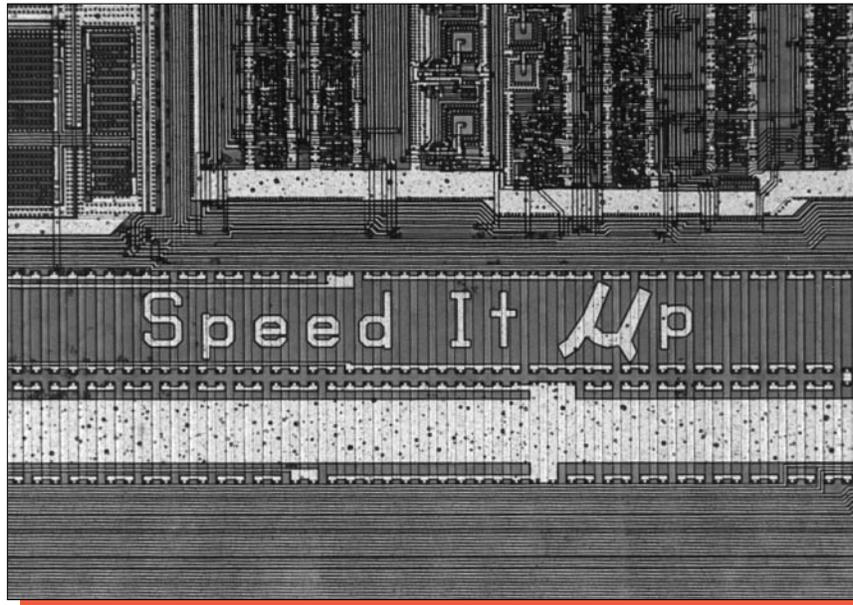


Figure 10. Whole die photograph of the Dallas Semiconductor DS80C320. Mag. 32x.

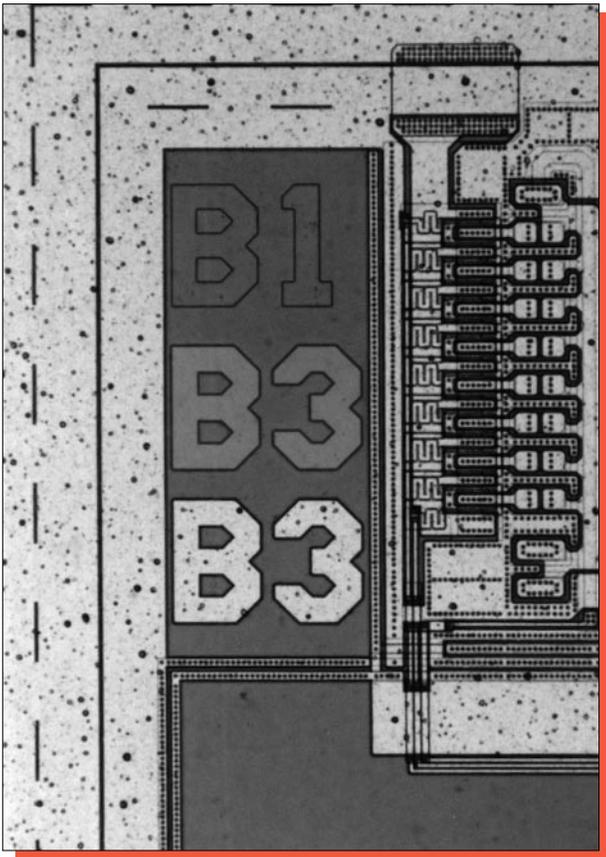


Mag. 200x

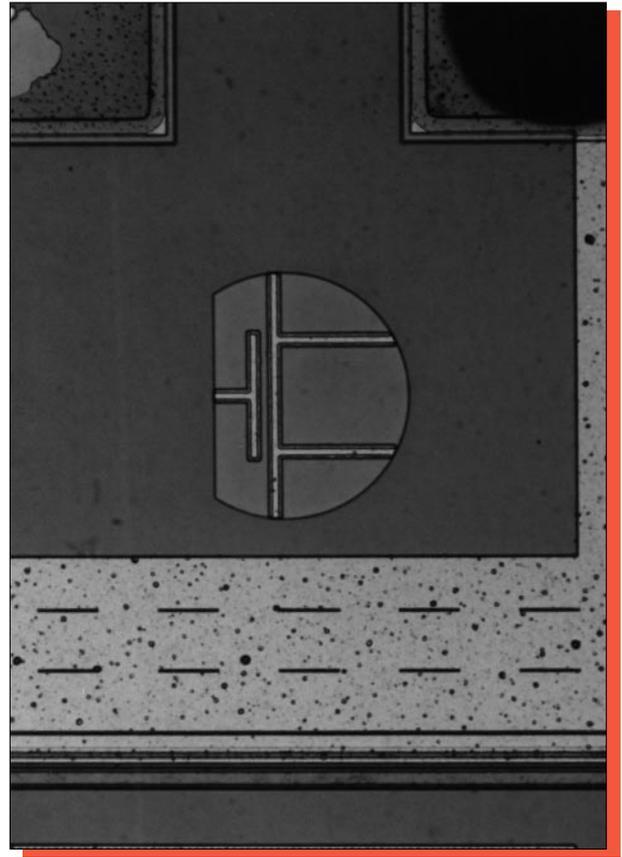


Mag. 320x

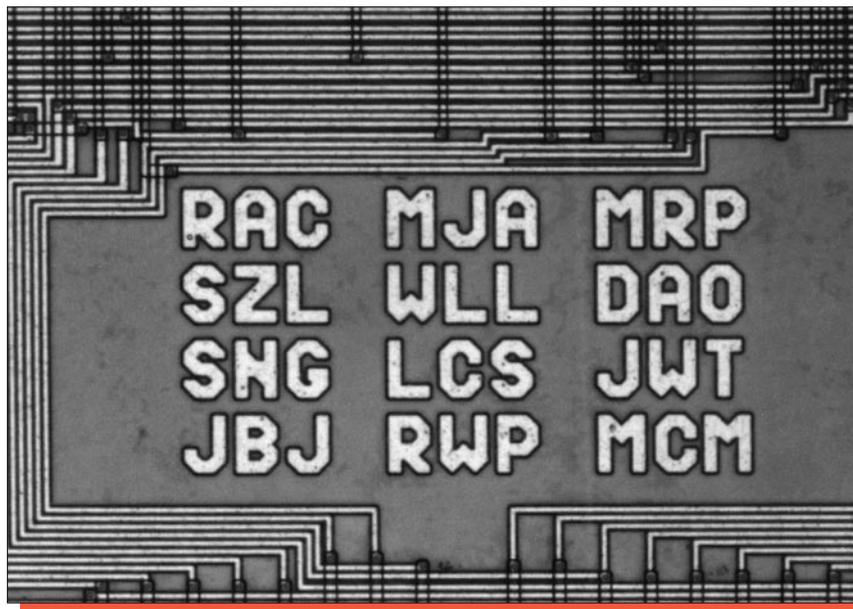
Figure 11. Identification markings from the die surface.



Mag. 320x

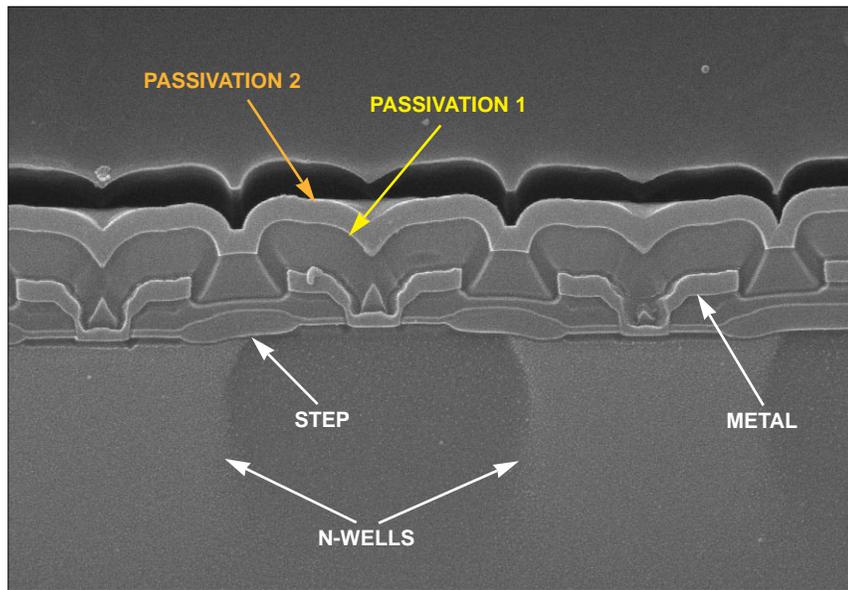


Mag. 320x

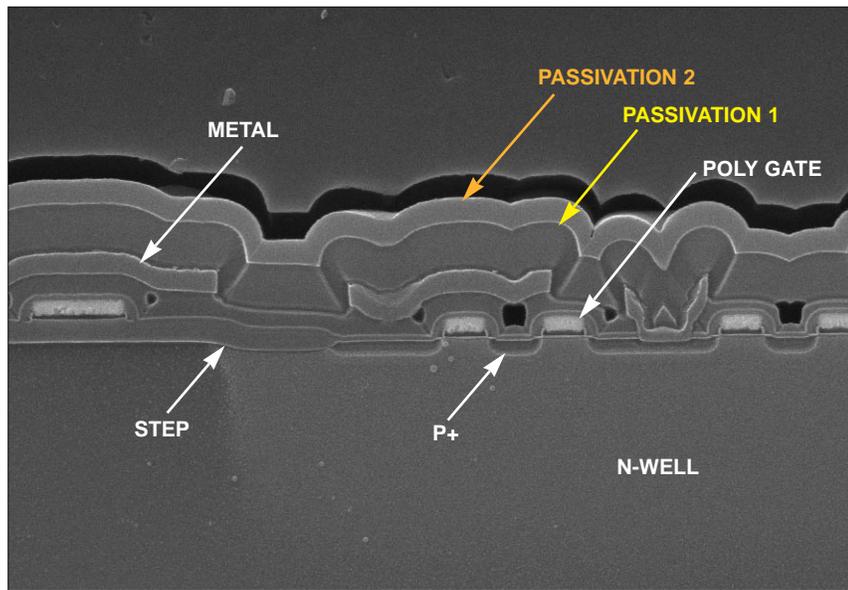


Mag. 500x

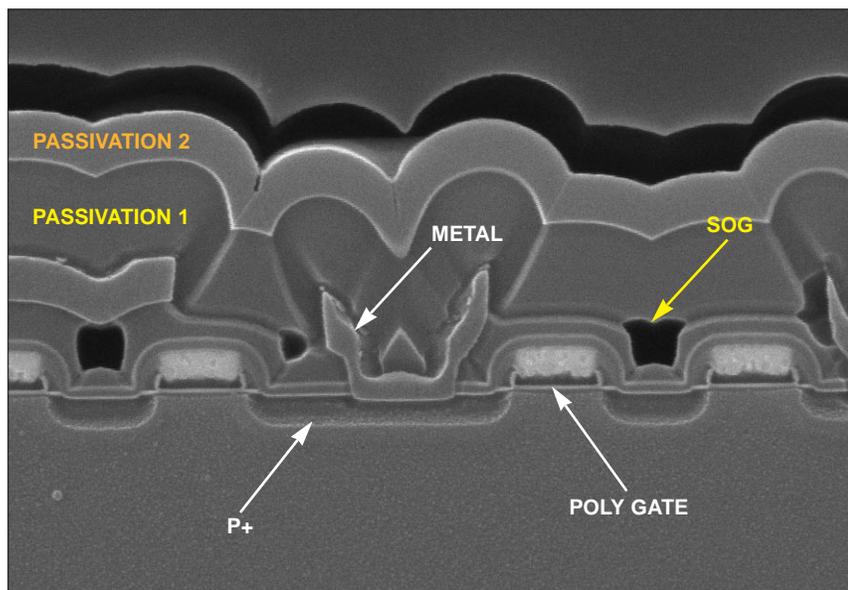
Figure 11a. Additional die markings from the surface.



Mag. 6500x

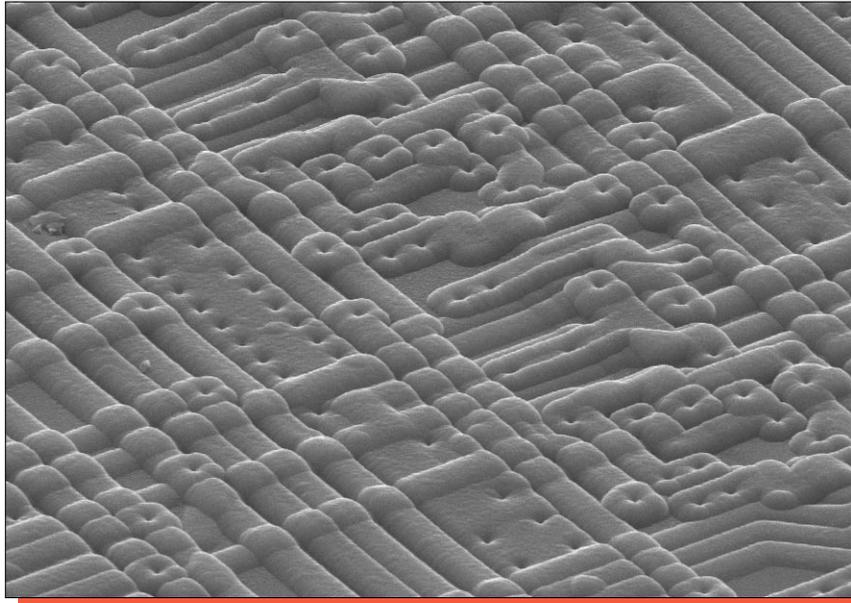


Mag. 6500x

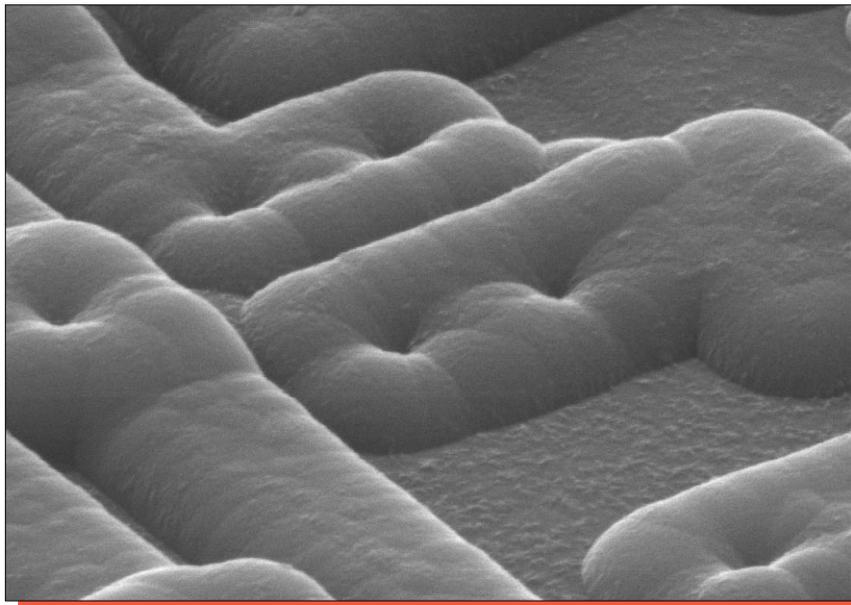


Mag. 13,000x

Figure 12. SEM section views illustrating general device structure.

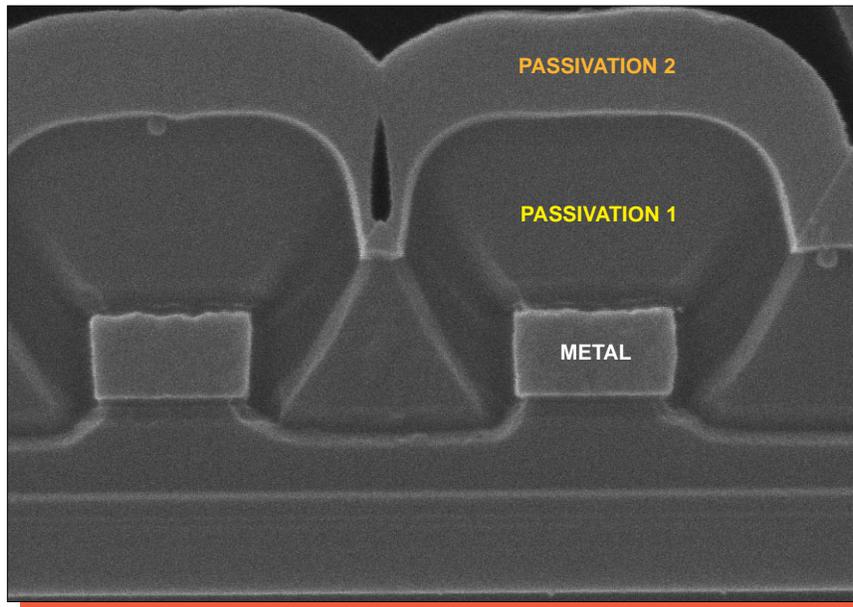


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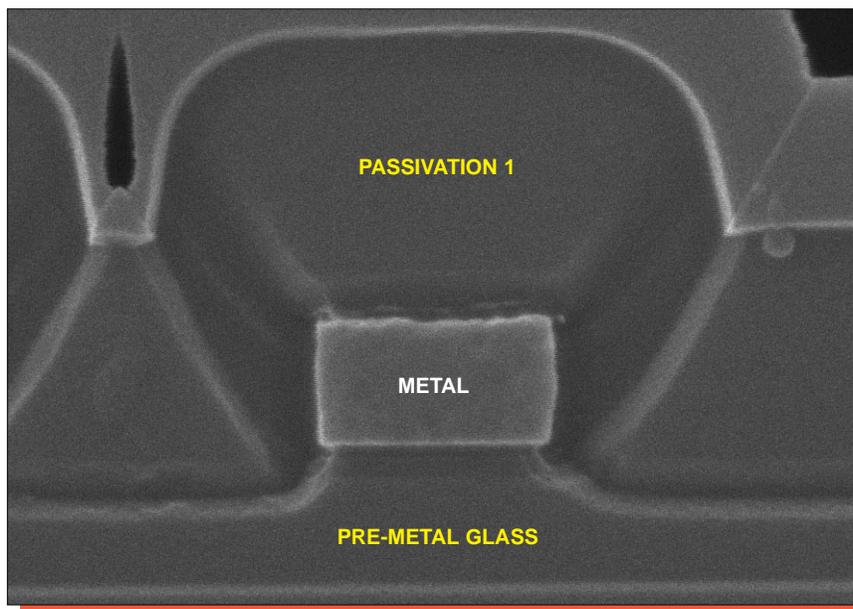


Mag. 12,000x

Figure 13. SEM views of overlay passivation coverage. 60°.

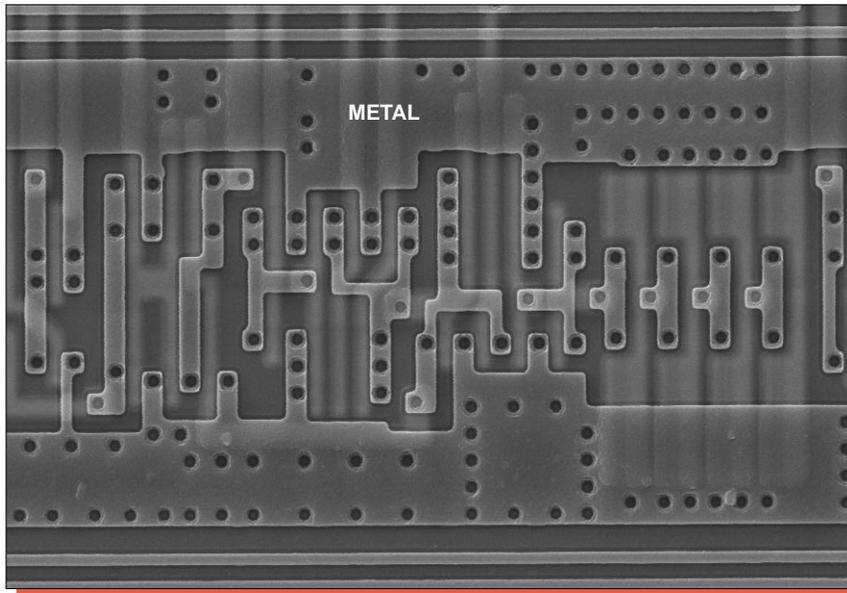


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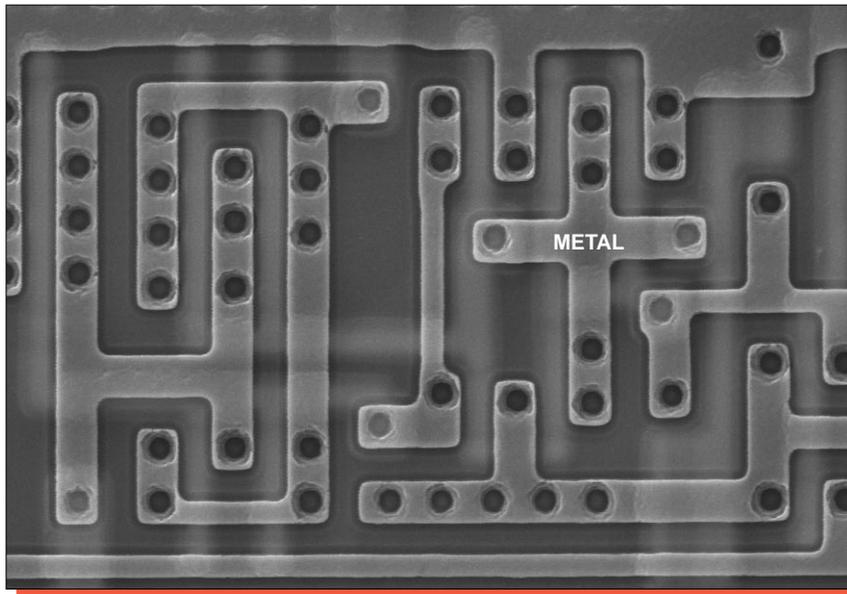


Mag. 40,000x

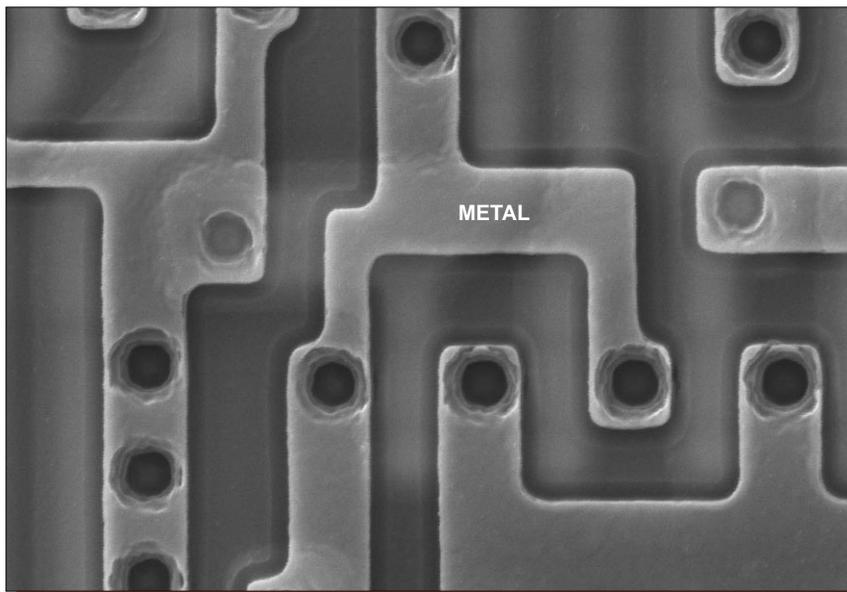
Figure 14. SEM section views of metal line profiles.



Mag. 1600x

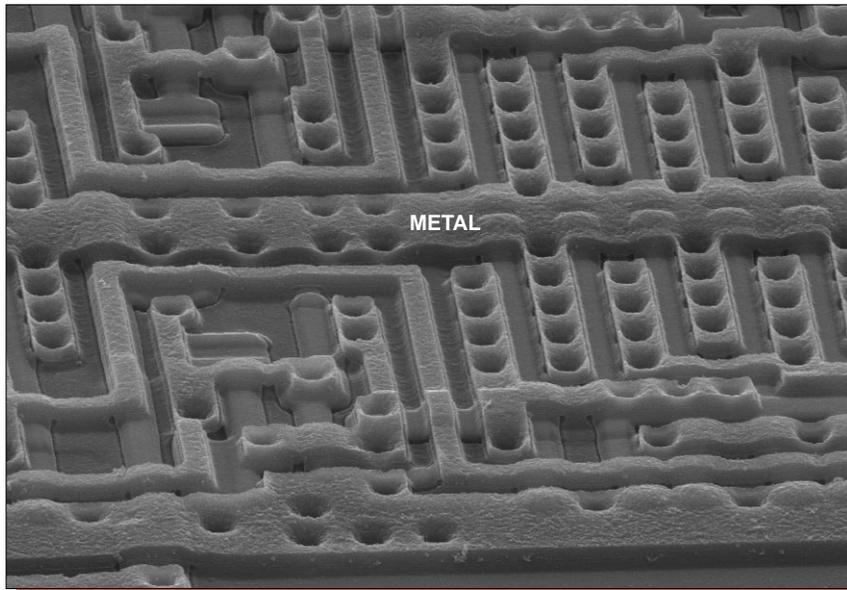


Mag. 3200x

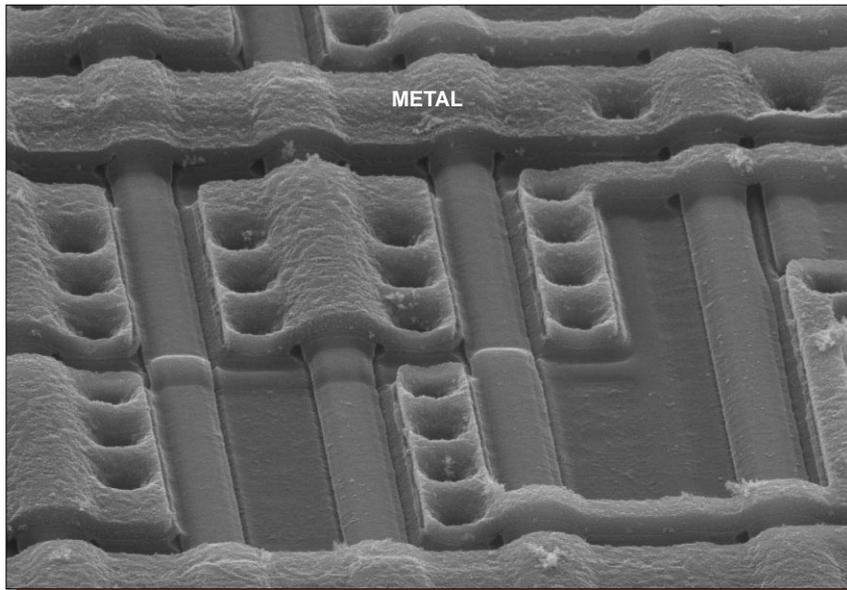


Mag. 6500x

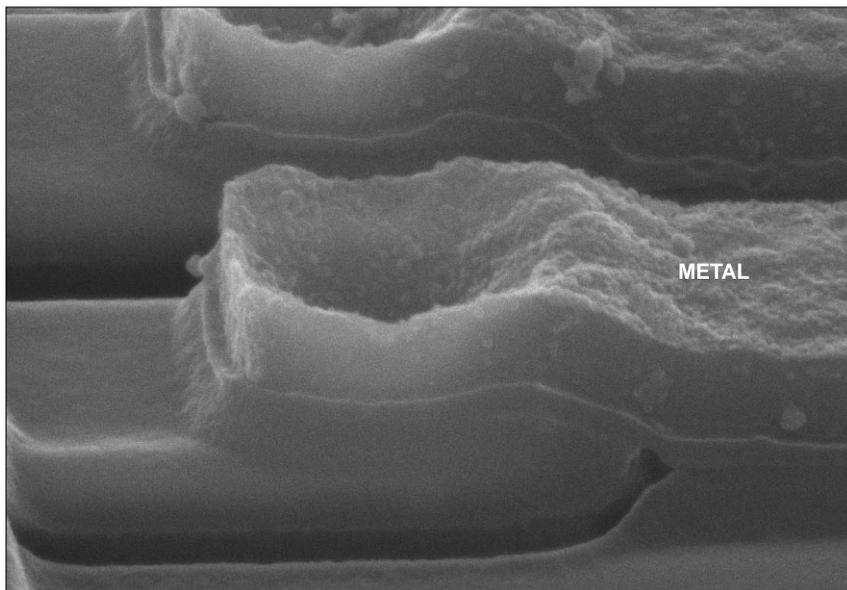
Figure 15. Topological SEM views illustrating metal patterning. 0°.



Mag. 3200x

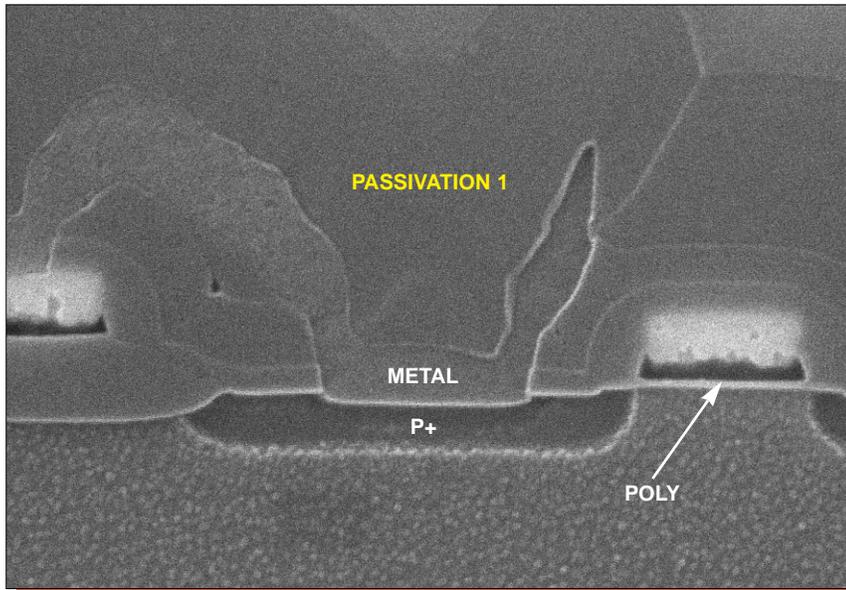


Mag. 5200x

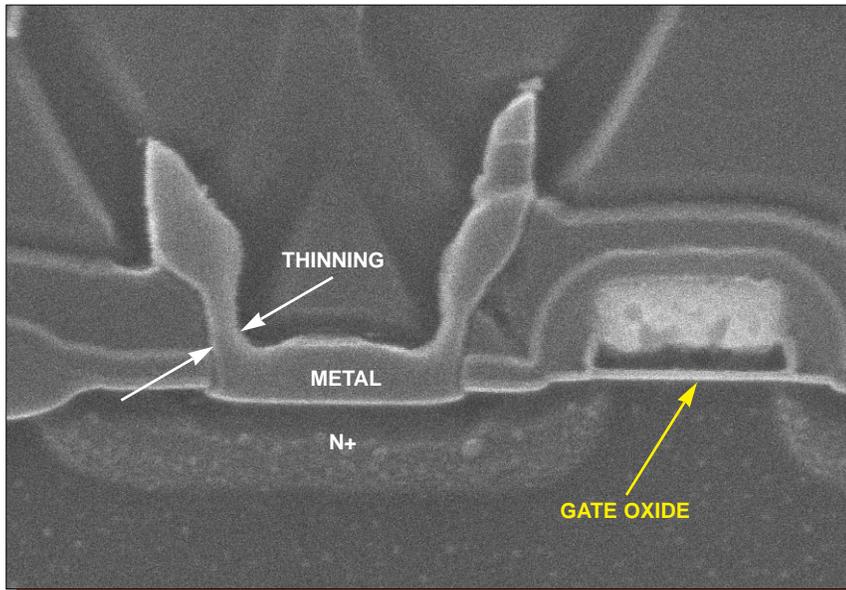


Mag. 26,000x

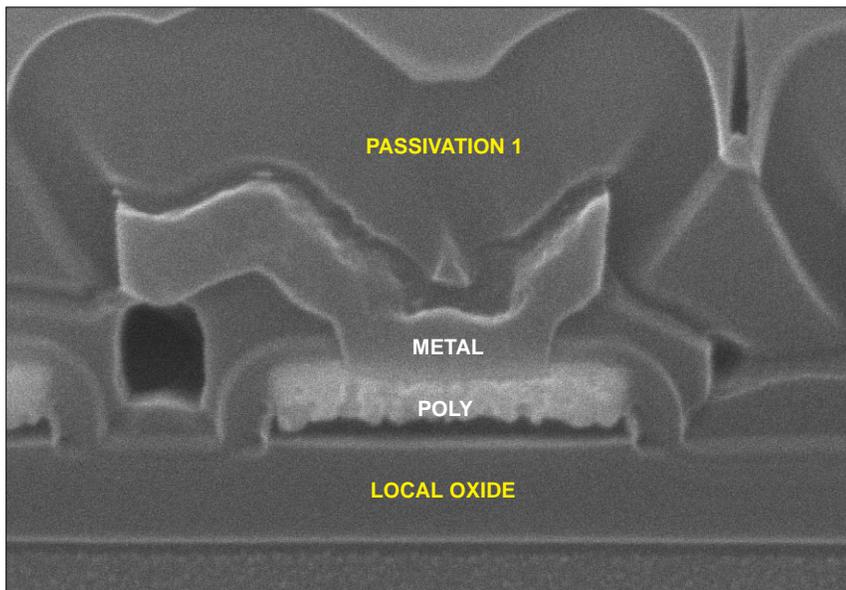
Figure 16. Perspective SEM views illustrating metal coverage. 60°.



metal-to-P+,
Mag. 28,000x

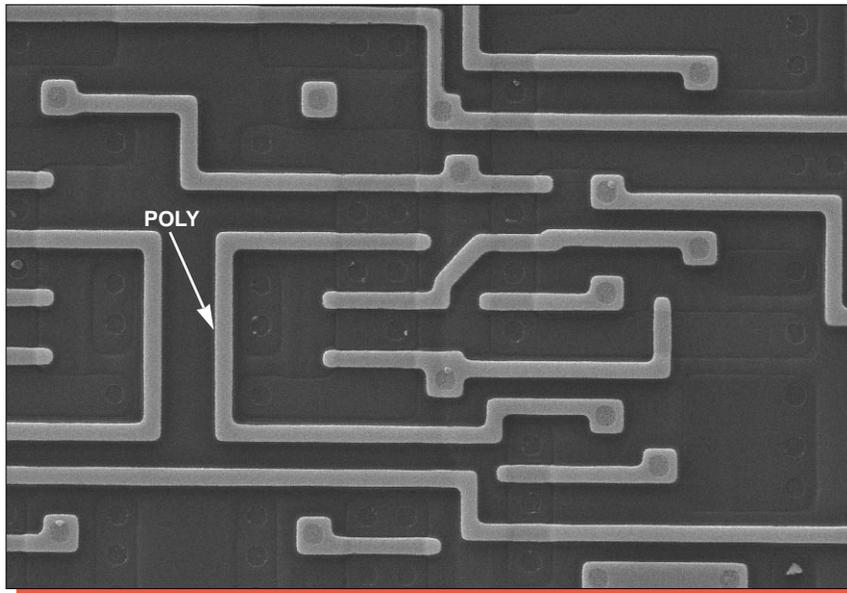


metal-to-N+,
Mag. 30,000x

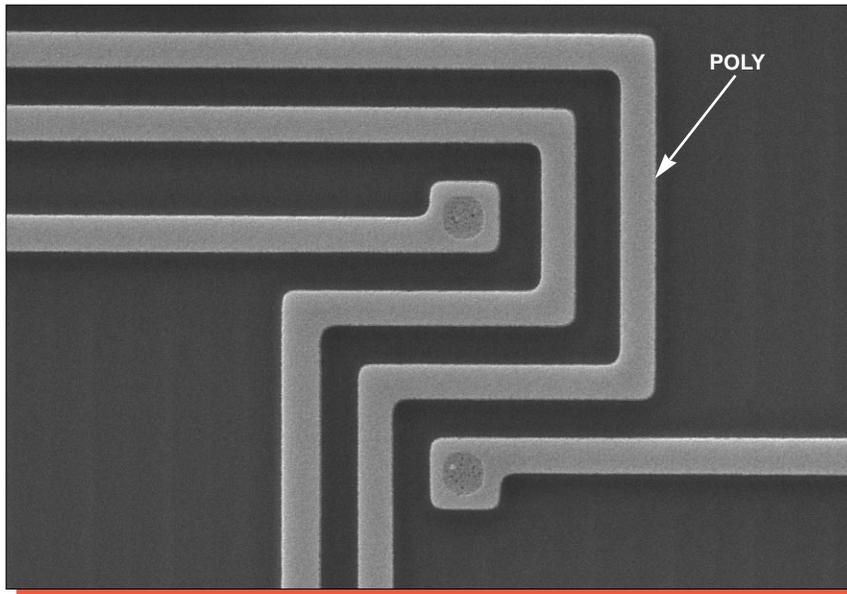


metal-to-poly,
Mag. 26,000x

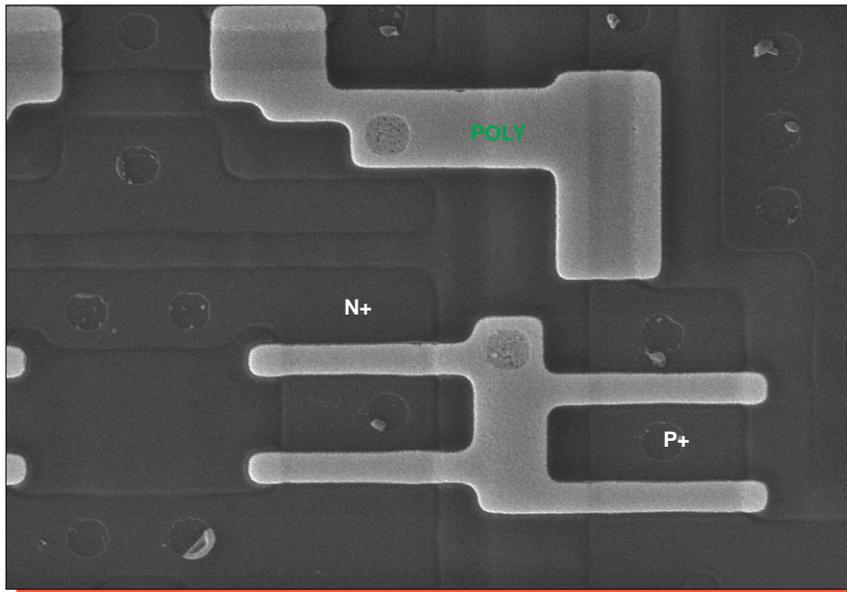
Figure 17. SEM section views of metal contacts.



Mag. 2500x

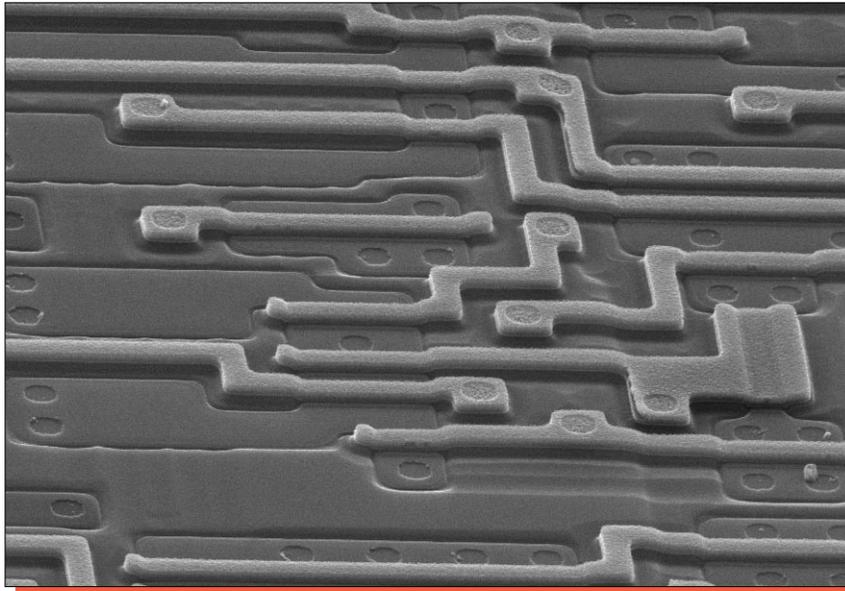


Mag. 5000x

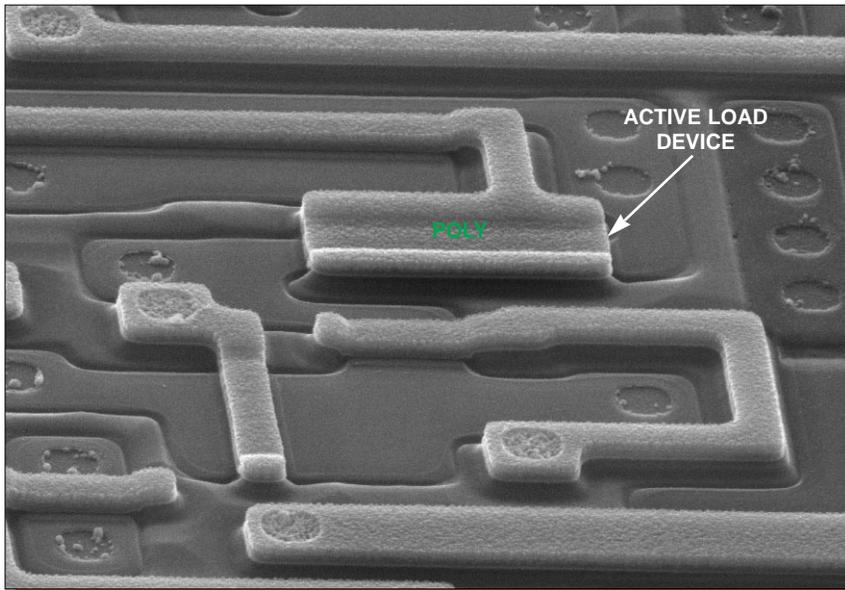


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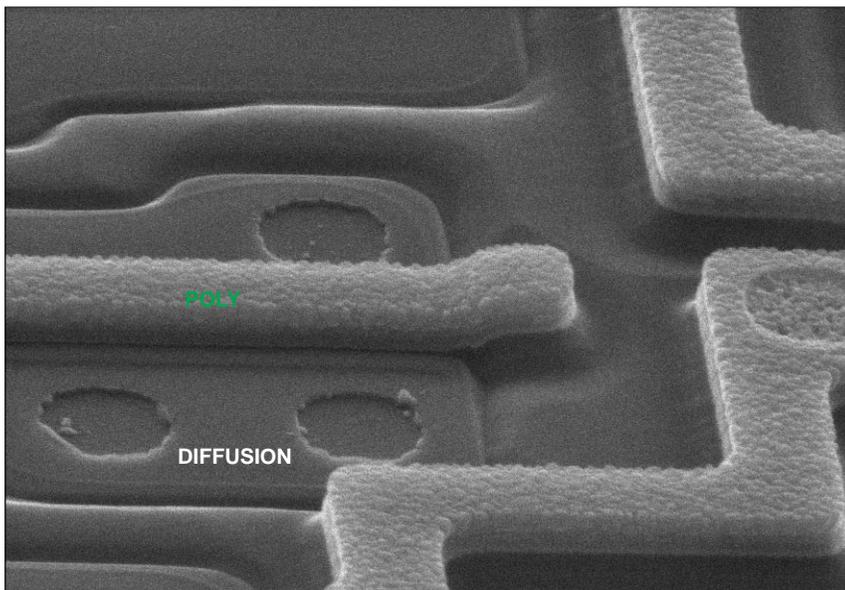
Figure 18. Topological SEM views illustrating poly patterning. 0°.



Mag. 4000x

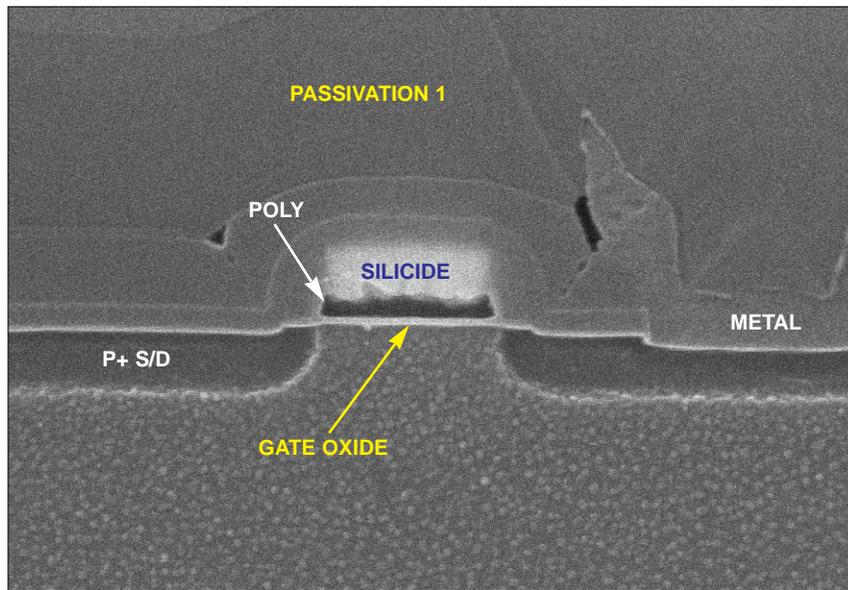


Mag. 7000x

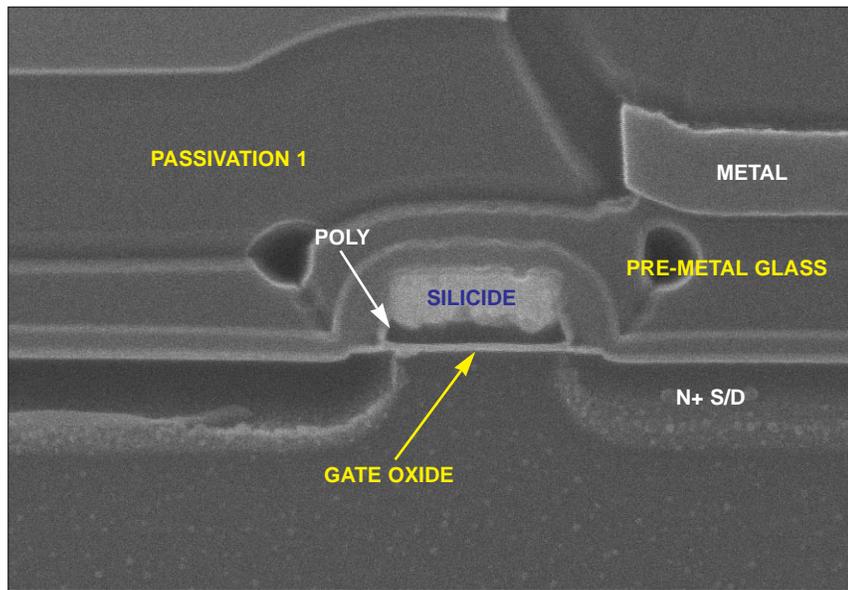


Mag. 17,000x

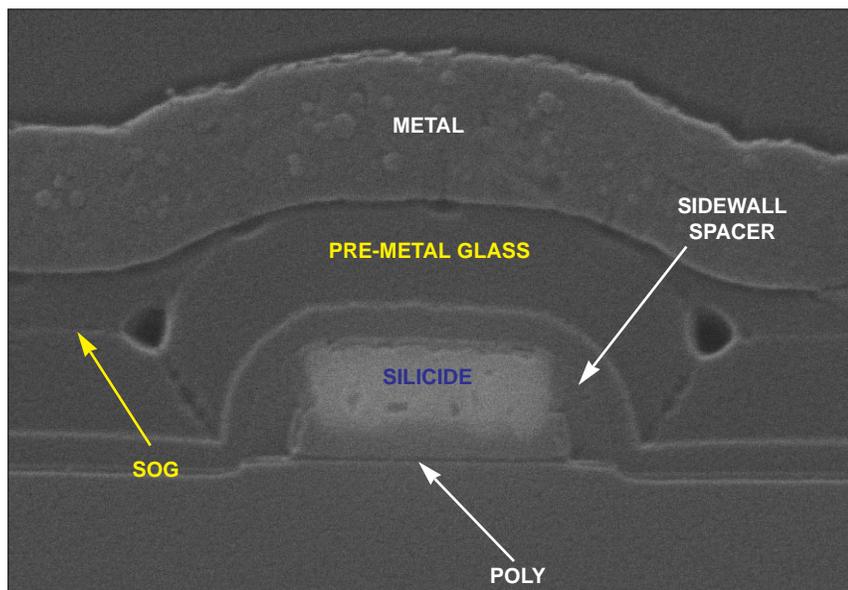
Figure 19. SEM views illustrating poly coverage. 60°.



P-channel,
Mag. 26,000x

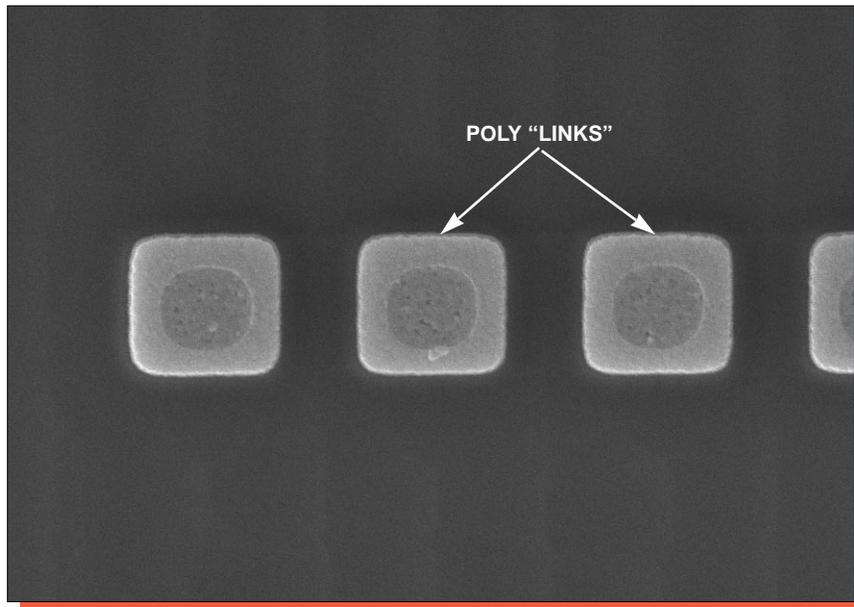


N-channel,
Mag. 26,000x

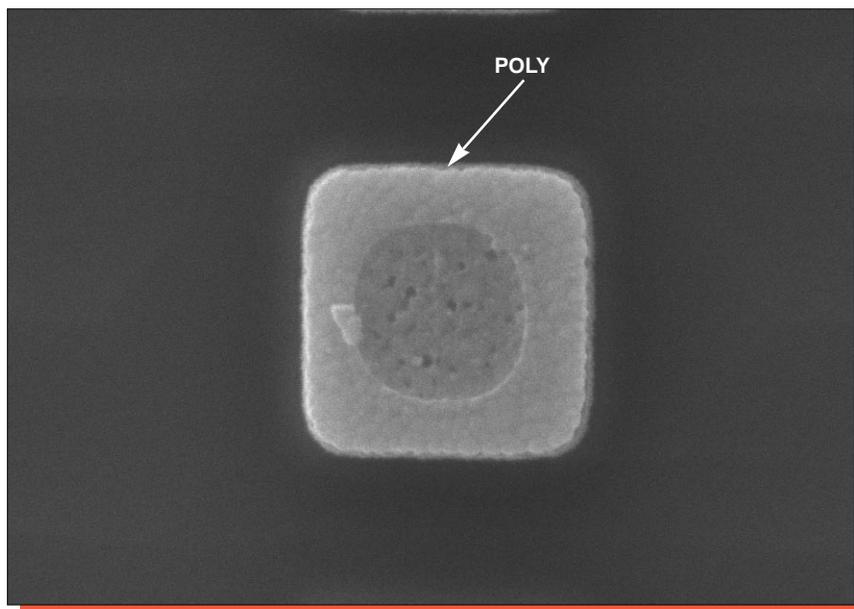


glass etch,
Mag. 40,000x

Figure 20. SEM section views illustrating typical gates.



Mag. 10,000x



Mag. 20,000x

Figure 21 Topological SEM views of poly "links". 0°.

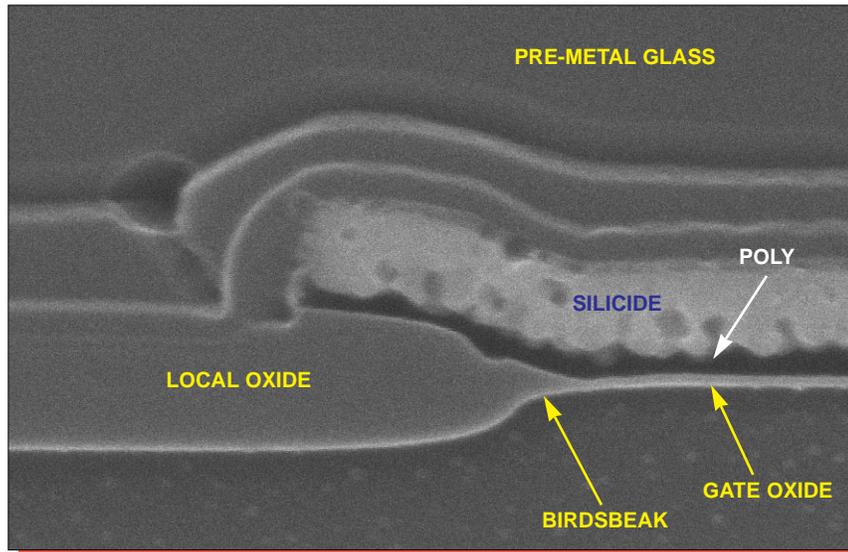
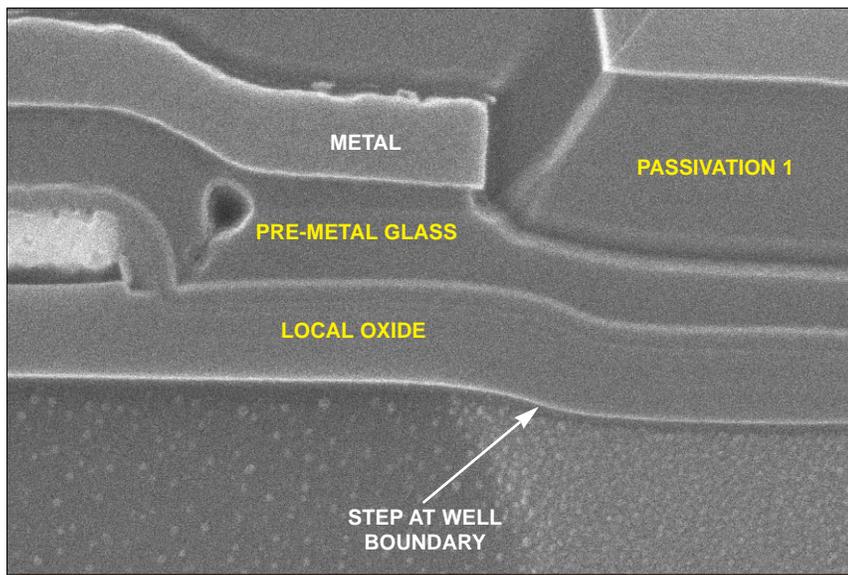
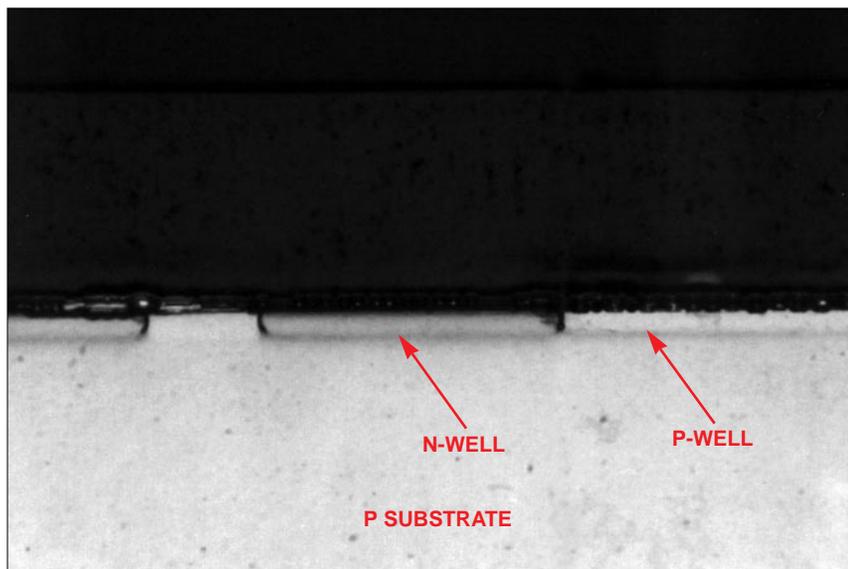


Figure 22. SEM section view of a local oxide birdsbeak. Mag. 40,000x.

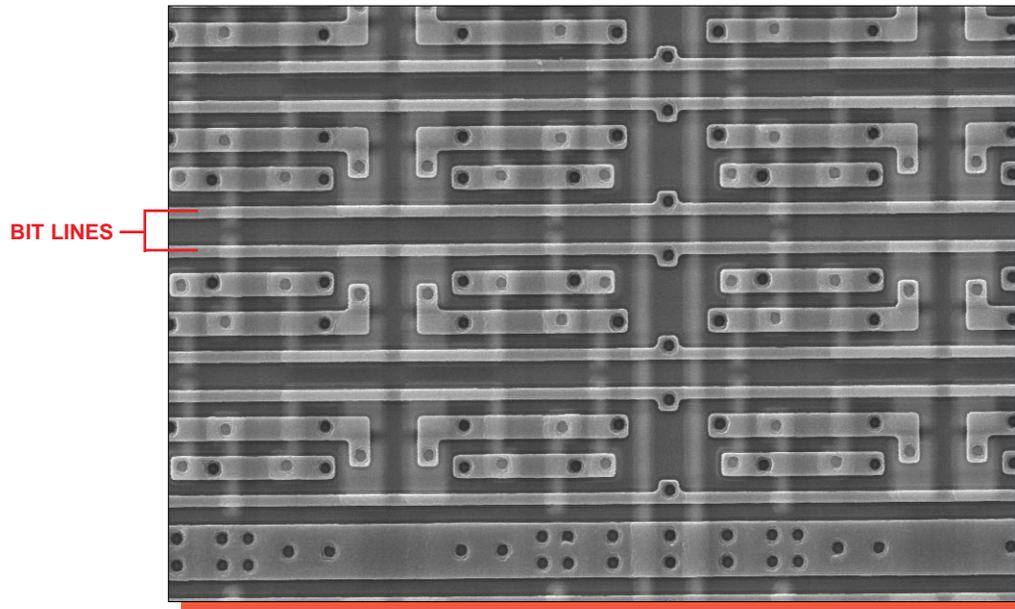


Mag. 26,000x

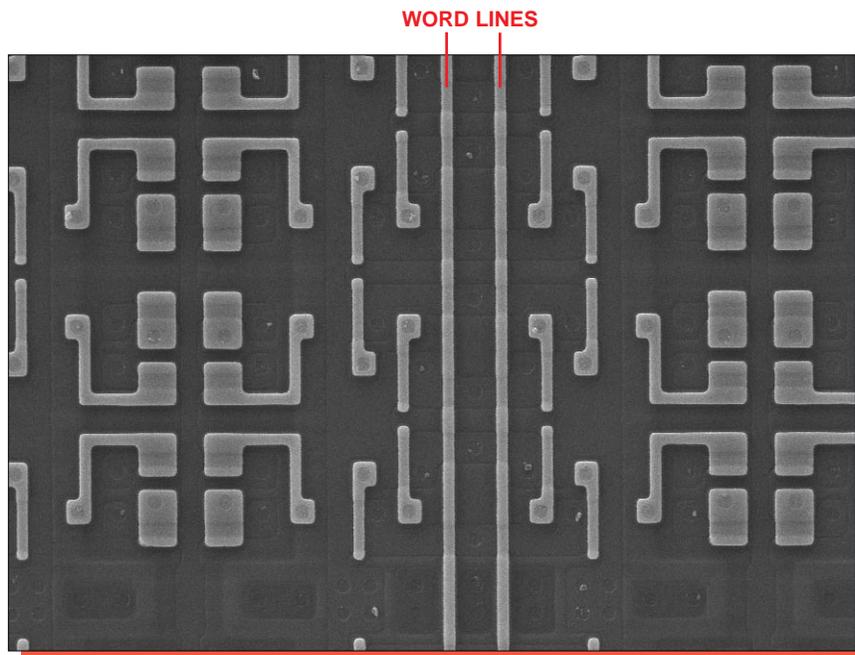


Mag. 800x

Figure 23. SEM and optical views illustrating the well structure.

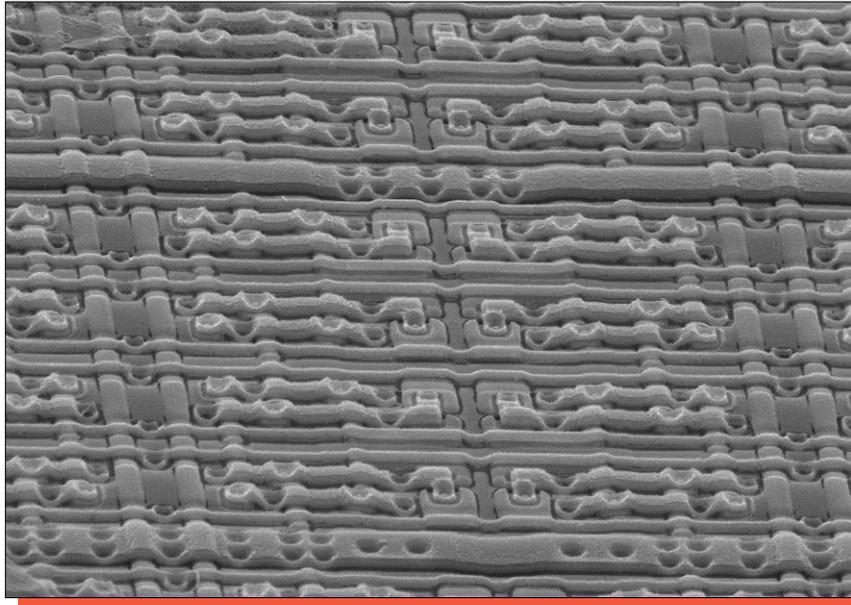


metal

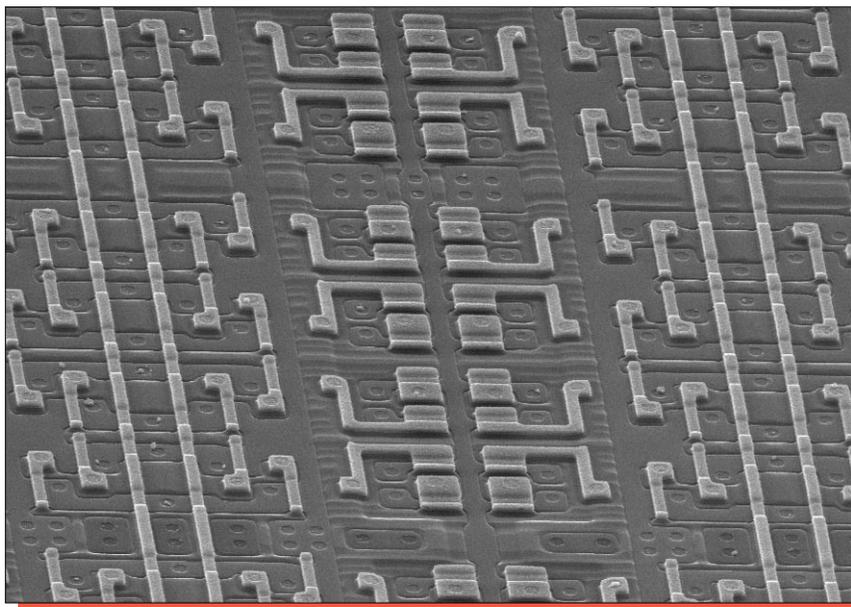


unlayered

Figure 25. Topological SEM views of the SRAM array. Mag. 1600x, 0°.

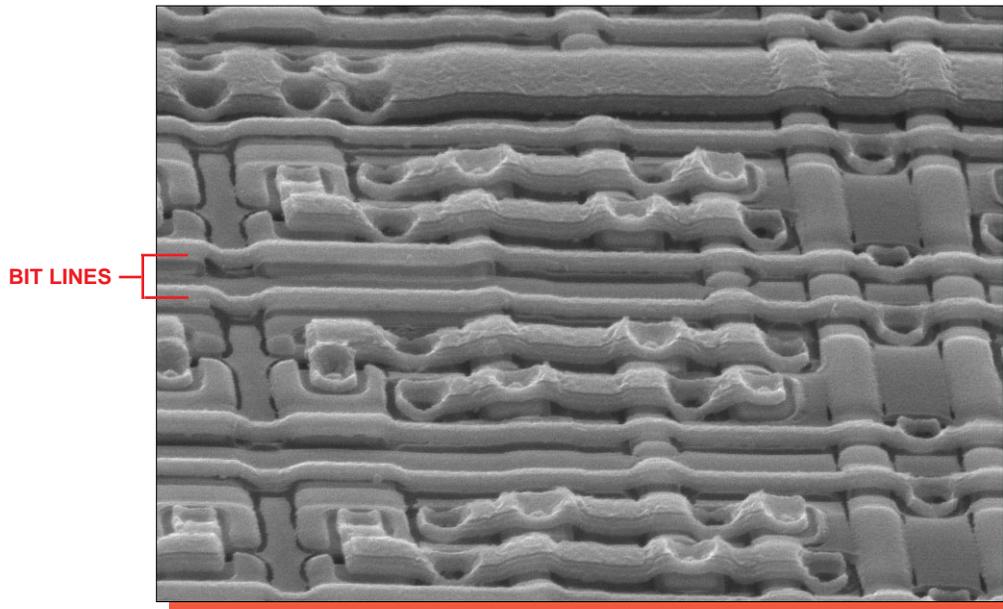


metal

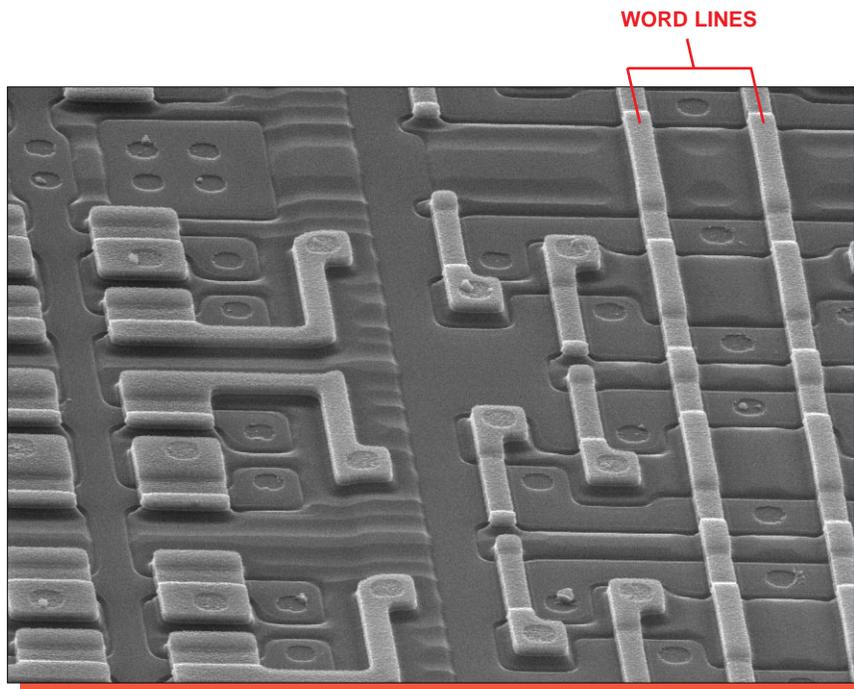


unlayered

Figure 26. Perspective SEM views of the SRAM array. Mag. 2000x, 60°.



metal



unlayered

Figure 27. Detailed SEM views of the SRAM array. Mag. 4000x, 60°.

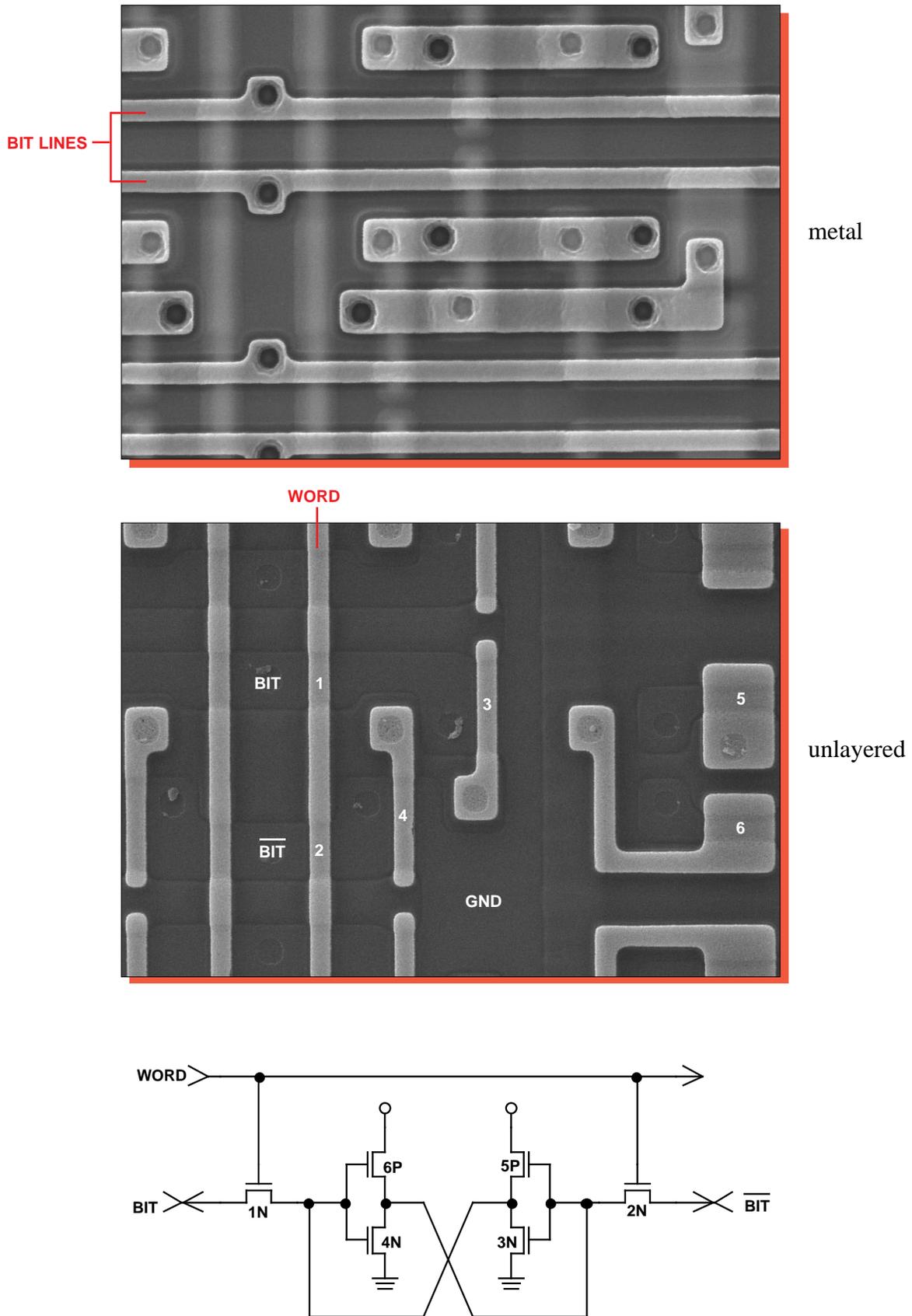
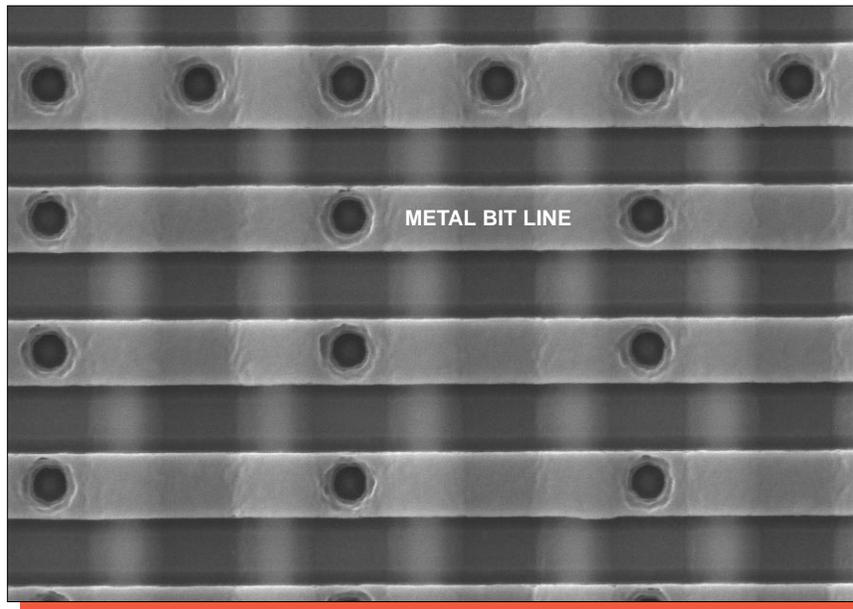
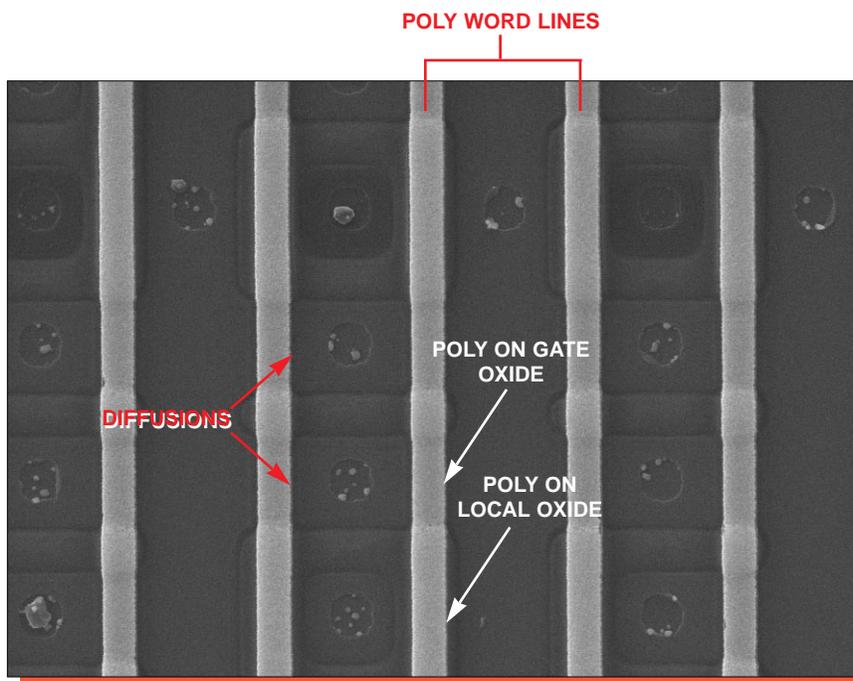


Figure 28. Topological SEM views of an SRAM cell along with the schematic.
Mag. 4000x, 0°.

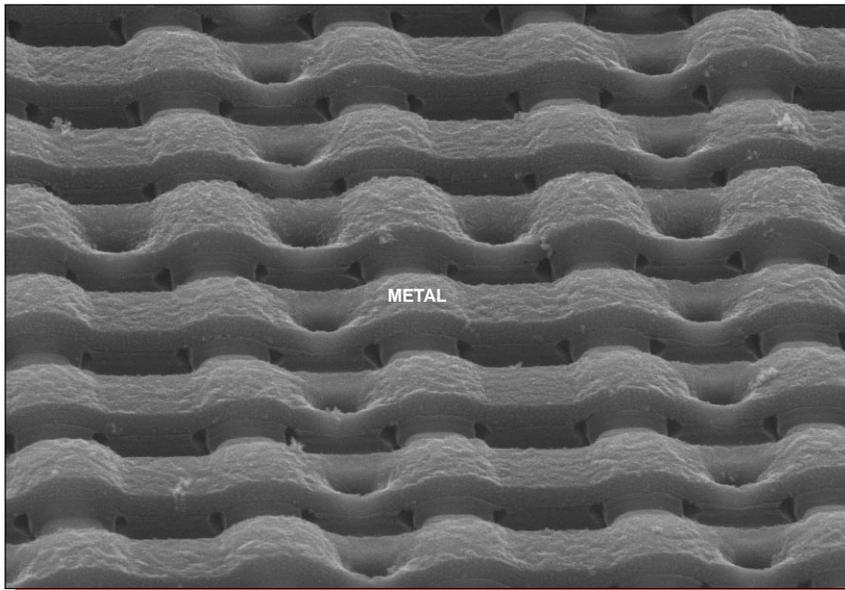


metal

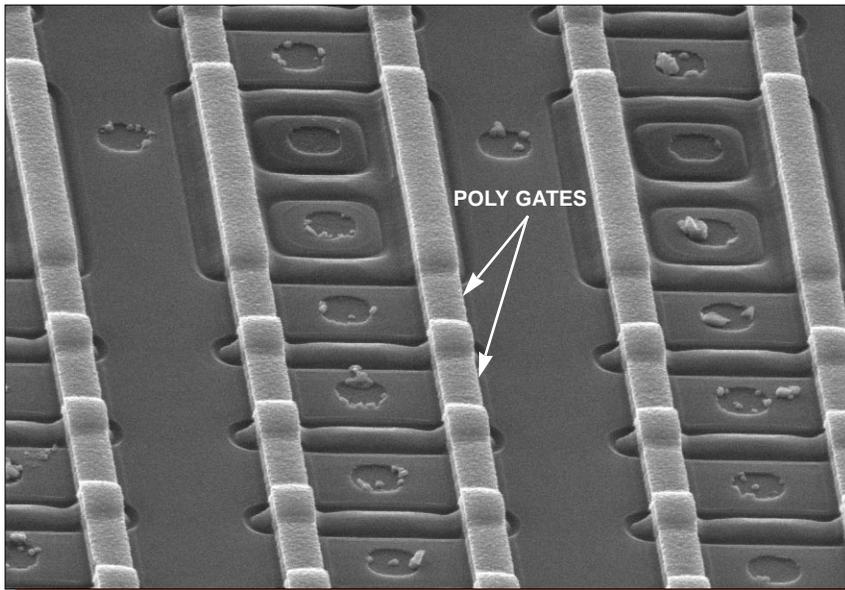


poly

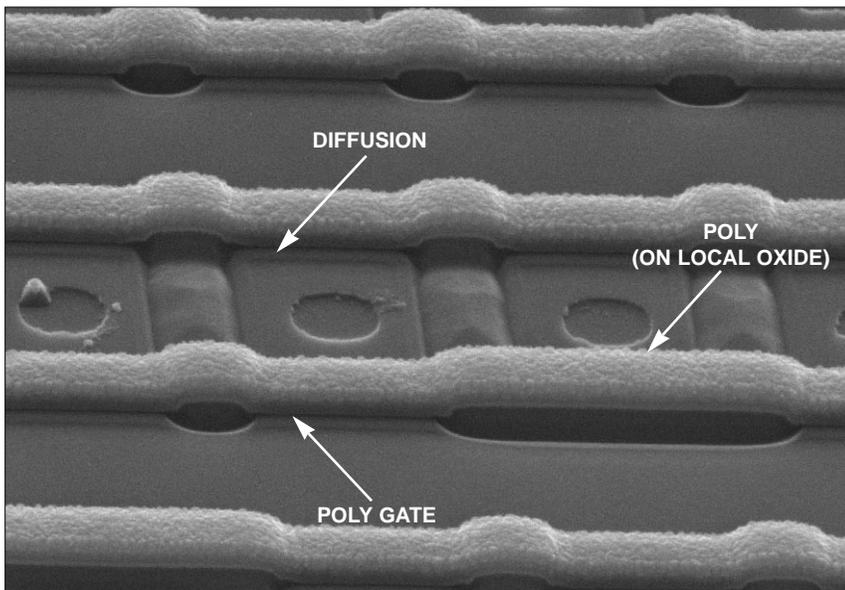
Figure 29. Topological SEM views of an MROM array on the DS80C320. Mag. 5000x, 0°.



metal,
Mag. 6000x

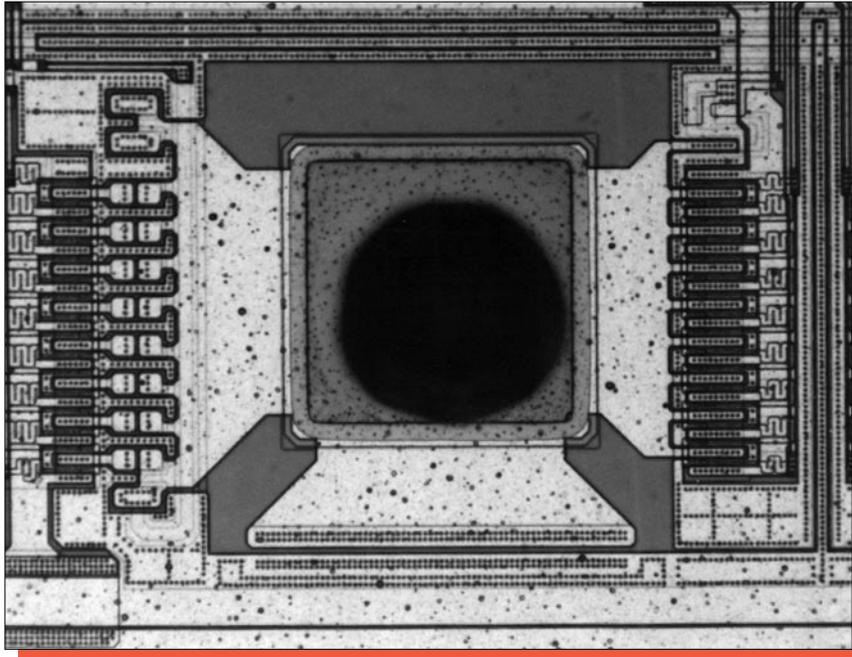


poly,
Mag. 6000x

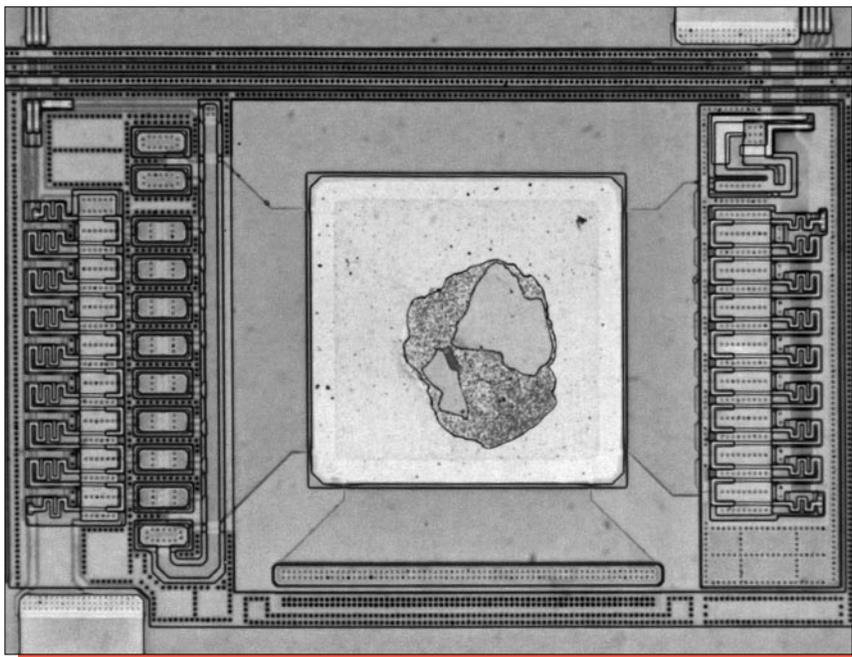


poly,
Mag. 10,000x

Figure 30. Perspective SEM views of the MROM array. Mag. 6000x, 60°.



metal



unlayered

Figure 31. Optical views of input protection. Mag. 320x.

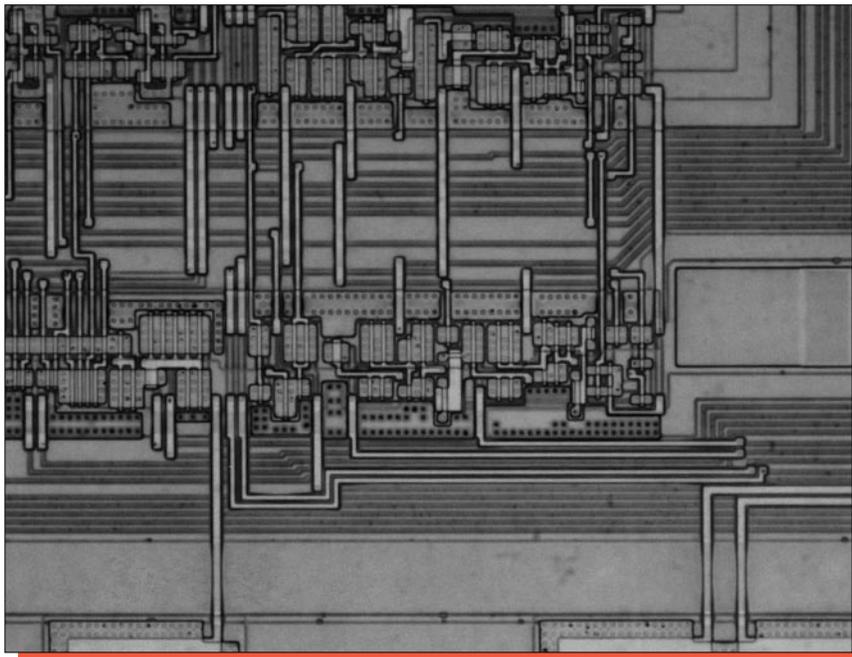
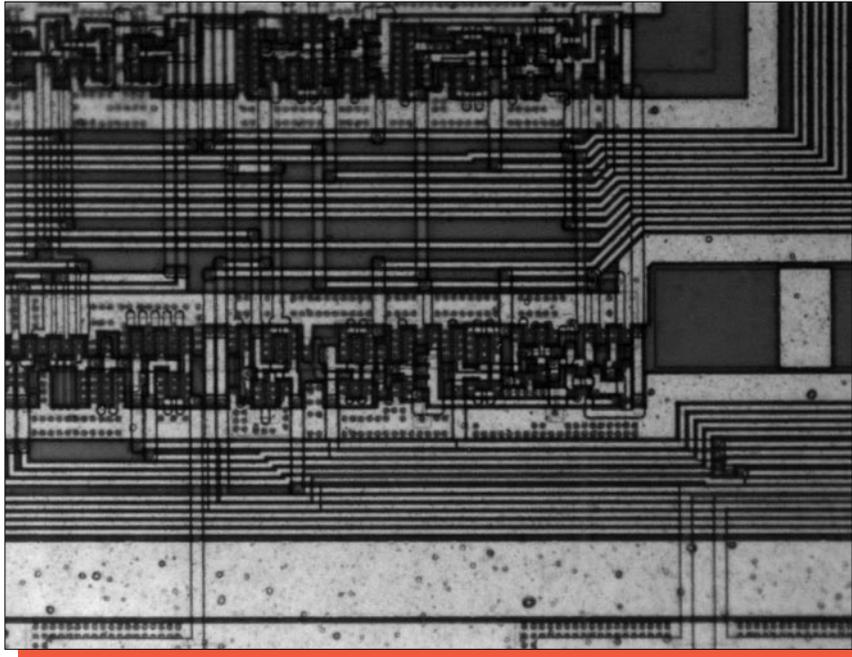
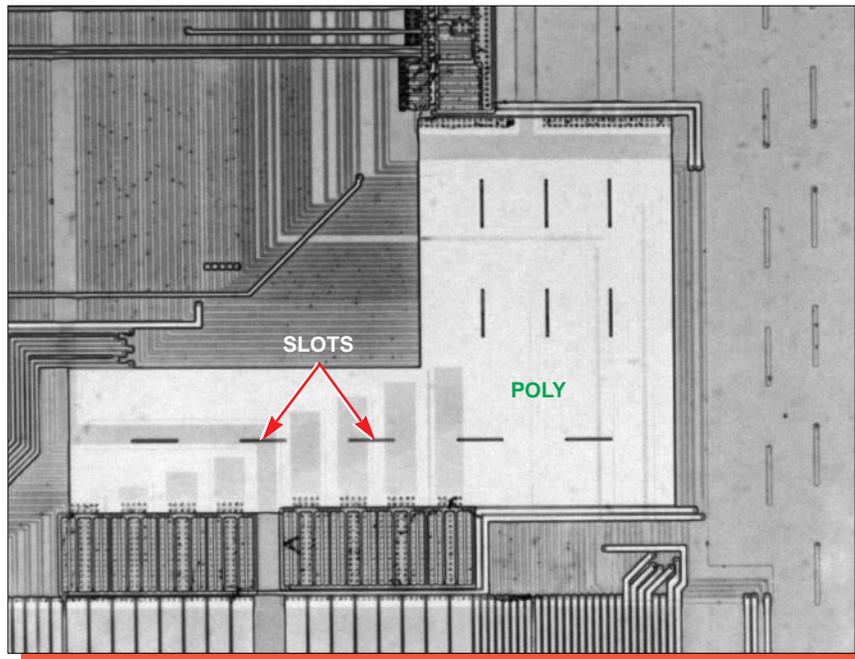
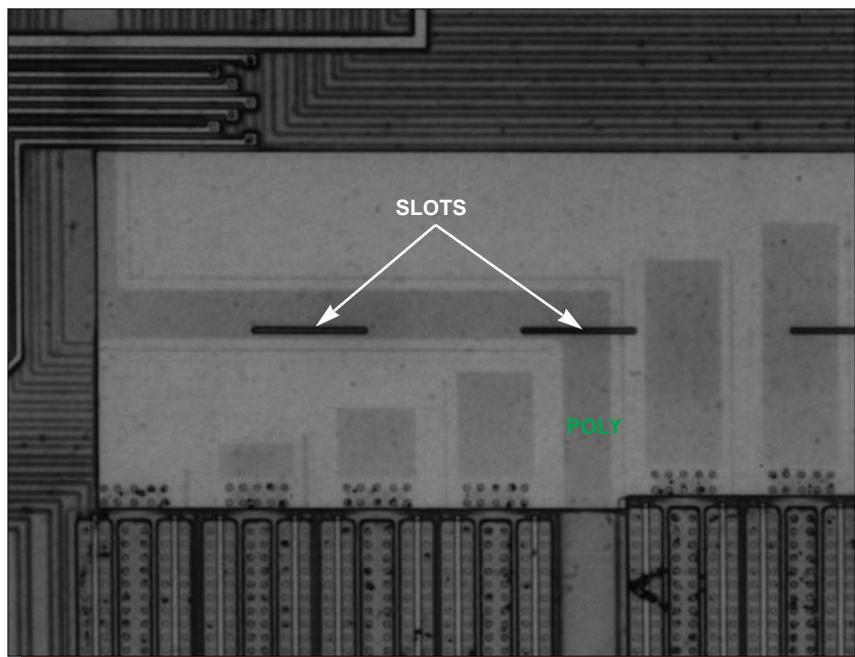


Figure 32. Optical views of typical circuit layout. Mag. 500x.

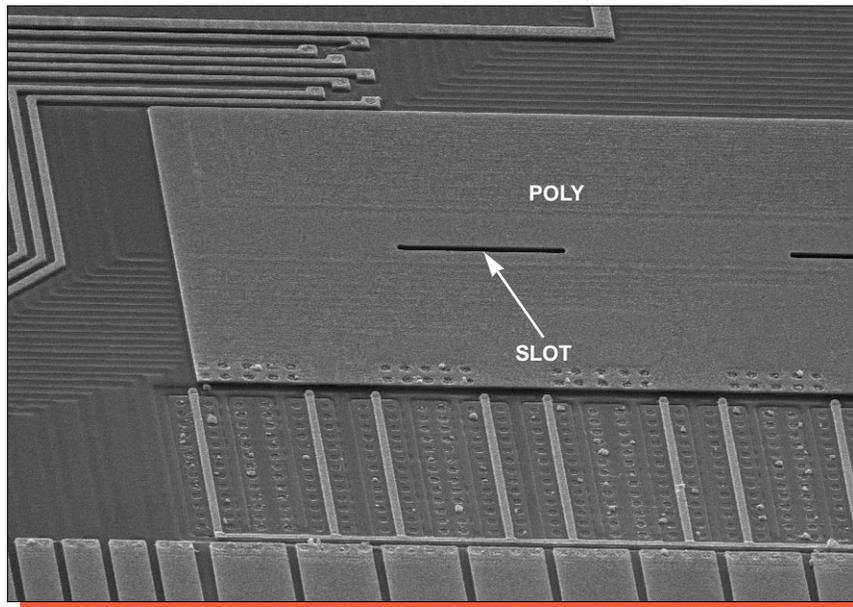


Mag. 320x

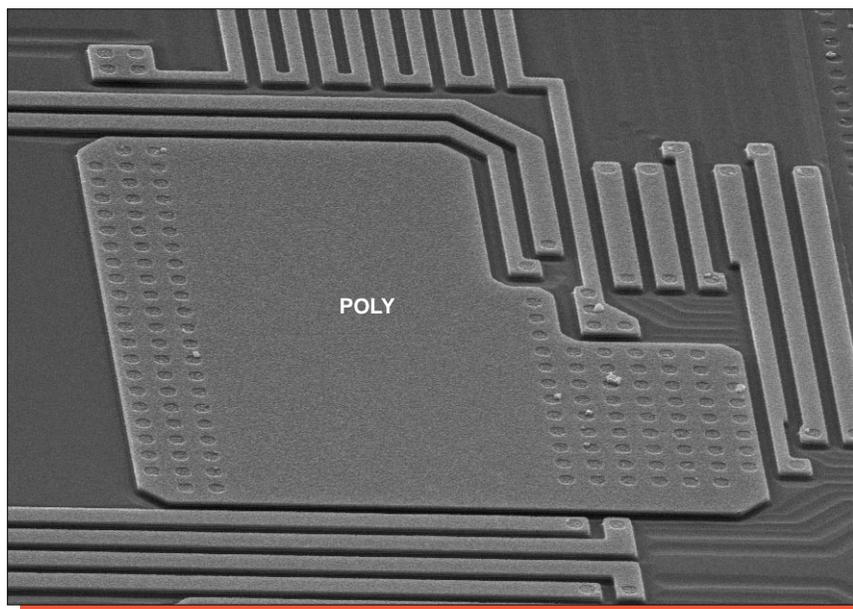


Mag. 800x

Figure 32a. Optical views of poly interconnect.



Mag. 1000x



Mag. 2000x

Figure 32b. Perspective SEM views of poly interconnect. 60°.