

Construction Analysis

Sony CXK5B16120J-12 1Mbit (64K x 16) BiCMOS SRAM

Report Number: SCA 9612-523



INTEGRATED CIRCUIT ENGINEERING

15022 N. 75th Street
Scottsdale, AZ 85260-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: <http://www.ice-corp.com/ice>

INDEX TO TEXT

<u>TITLE</u>	<u>PAGE</u>
INTRODUCTION	1
MAJOR FINDINGS	1
TECHNOLOGY DESCRIPTION	
Assembly	2
Die Process	2 - 4
ANALYSIS RESULTS I	
Assembly	5 - 6
ANALYSIS RESULTS II	
Die Process and Design	7 - 10
TABLES	
Procedure	11
Overall Quality Evaluation	12
Package Markings	13
Wirebond Strength	13
Package Material Analysis	13
Die Material Analysis	14
Horizontal Dimensions	15
Vertical Dimensions	16

INDEX TO FIGURES

PACKAGE AND ASSEMBLY	Figures 1 - 5
LAYOUT AND IDENTIFICATION	Figures 6 - 7
PHYSICAL DIE STRUCTURES	Figures 8 - 33
COLOR PROCESS DRAWING	Figure 26b
MEMORY CELL	Figures 27 - 33
FUSES	Figure 34
INPUT STRUCTURE AND GENERAL CIRCUIT LAYOUT	Figure 35

INTRODUCTION

This report describes a construction analysis of the Sony CXK5B16120J-12, 1 Mbit (64K x 16) BiCMOS SRAM. Four devices packaged in 44-pin SOJ packages date code 9604 were received for the analysis. Analysis of the assembly is included.

MAJOR FINDINGS

Questionable Items:¹

- Metal 1 (aluminum) thinned up to 100 percent² at contact edges (Figures 18 - 19a). Barrier (barely) maintained continuity.
- Cracks in the barrier at sidewalls of some contacts (Figure 19a).

Special Features:

- BiCMOS, twin-well process with apparent buried layer.
- Sub-micron gate lengths (0.5 micron).
- TFT pull-up devices in the SRAM cell array.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 44-pin plastic Small Outline J-lead (SOJ) packages for surface mount applications.
- The leadframe was constructed of copper and tinned externally with tin-lead (SnPb) solder. Leads appeared to be plated with tin (Sn) prior to tinning.
- Internal leadframe plating was by silver (Ag) over a gold (Au) flash.
- The header/paddle consisted of copper (Cu). It employed large oval-shaped slots for strength.
- The die was mounted to the header/paddle using a silver-filled epoxy die attach.
- A patterned polyimide die coat was employed.
- Die separation by sawn dicing (full depth).
- Wirebonding by the thermosonic ball bond method using 1.2 mil gold wire.
- Pins 22, 23 and 28 were not connected.

Die Process

- Fabrication process: Selective oxidation BiCMOS process employing twin-wells in a P substrate. Bipolar (NPN) devices were located in N-wells with an apparent buried layer.
- Final passivation: A single thick layer of nitride.

TECHNOLOGY DESCRIPTION (continued)

- Metallization: Two levels of metal defined by dry-etch techniques. Metal 2 consisted of aluminum with a titanium barrier while Metal 1 employed a titanium-nitride cap and barrier. Standard vias and contacts were employed (no plugs). Metal 1 elongated contacts were used at bipolar devices.
- Intermetal dielectric (IMD): Intermetal dielectric (between M2 and M1) consisted of four layers of glass. The second layer (SOG) had been subjected to an etchback to aid in planarization.
- Pre-metal glass: A single layer of BPSG (borophosphosilicate glass) over a deposited glass, another thin layer of CVD glass (probably BPSG) and various densified oxides.
- Polysilicon: Four layers of polysilicon were employed. Poly 4 and poly 3 (thin layers) were used exclusively in the SRAM cell array. They were used for the TFT pull-up devices (PD1 and PD2). Poly 4 also distributed Vcc and poly 3 was also used for cell interconnect. Poly 2 and poly 1 employed a tungsten silicide. Poly 2 was used for bit line interconnections and also distributed GND in the SRAM cell array. Poly 2 was also used in the periphery and decode as interconnect. Poly 1 was used to form all gates on the die including the select and storage gates in the array and for redundancy fuses. A separate poly was used to form the emitter dopant source at bipolar NPN devices.
- Diffusions: Implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place.
- Bipolar devices: Poly was used as the dopant source for the emitters at bipolar NPN devices. A separate P+ diffusion was used for the base of NPN transistors. Deep N+ diffusions were used at collectors which were contacted by metal 1. All bipolar NPN devices were located in N-wells and appeared to have buried layers.

TECHNOLOGY DESCRIPTION (continued)

- Local oxide (LOCOS) isolation. A step was present in the oxide at the edge of the well indicating a twin-well process was used.
- Wells: Twin-wells in a P substrate.
- Fuses: Redundancy fuses (poly 1) were present on this device. Some laser blown fuses were noted. Overlay passivation and oxide cutouts were made over the fuses.
- Memory cells: The memory cells consisted of a 4T SRAM cell design with TFT pullups. Metal 1 formed the bit lines via poly 2 links. Poly 4 was used to form the body of the pull-up devices with poly 3 as the gates. The TFTs are identified as PD1 and PD2. Poly 4 distributed Vcc and poly 3 was also used for cell interconnect. Poly 2 distributed GND. Poly 1 formed all gates and word lines.
- Buried contacts: Direct poly-to-diffusion contacts were employed in the SRAM cell. Poly layers 1 and 3 contacted diffusion. No problems were found in these areas.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 5

Questionable Items:¹ None.

Special Features:

- Oval shaped slots in the header/paddle.

General Items:

- The devices were encapsulated in a 44-pin plastic Small Outline J-Lead (SOJ) packages.
- Overall package quality: Good. No significant defects were found on the external or internal portions of the packages. No voids or cracks were noted in the plastic. External pins were well formed and tinning of the leads was complete. No gaps were noted at lead exits.
- Leadframe: Copper (Cu) leadframe externally tinned with tin-lead (SnPb) solder and plated with tin (Sn) prior to tinning. The leadframe was internally spot-plated with silver (Ag) over a gold (Au) flash. No problems were found. Leadframe design provided a good match for die pad layout.
- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. All bond pull strengths were normal and no bond lifts occurred (see page 13).
- Die attach: A silver-filled epoxy of normal quality was used to attach the die to the header/paddle. No problems were found.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS I (continued)

- Die coat: A patterned, uniform thickness polyimide die coat was used. No problems were found.
- Die dicing: Die separation was by sawing (full depth) and showed normal quality workmanship. No large chips or cracks were present at the die surface.

ANALYSIS RESULTS II

Die Process and Design:

Figures 6 - 35

Questionable Items:¹

- Metal 1 aluminum thinned up to 100 percent² at contact edges (Figures 18 - 19a). The barrier (barely) maintained continuity.
- Cracks in the barrier at sidewalls of some contacts (Figure 19a).

Special Features:

- BiCMOS, twin-well process.
- Sub-micron gate lengths (0.5 micron).
- Thin-film pull-up devices in the SRAM cell array.

General Items:

- Fabrication process: Selective oxidation BiCMOS process employing twin-wells in a P substrate. Bipolar (NPN) devices were located in the N-wells with buried layers. No significant problems were found in the process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

²Seriousness depends on design margins.

ANALYSIS RESULTS II (continued)

- Final passivation: A single thick layer of nitride. Passivation appeared to have been etched at the edge seal, however; passivation integrity tests indicated defect free passivation in the periphery as well as at the edge seal.
- Metallization: Two levels of metal defined by dry-etch techniques. Metal 2 consisted of aluminum with a titanium barrier while metal 1 employed a titanium-nitride cap and barrier. Standard vias and contacts were employed (no plugs). Metal 1 elongated contacts were used with bipolar devices.
- Metal patterning: Metal layers were defined by a dry etch of good quality. Metal 2 lines were widened around vias. All vias and contacts were completely surrounded by metal.
- Metal defects: No notching or voiding of the metal layers was found. No significant silicon nodules were found following aluminum removal.
- Metal step coverage: Typical metal 2 thinning at via steps was 40 percent (including the barrier). Metal 1 aluminum thinned up to 100 percent at some contact edges and the barrier only barely maintained continuity. In addition, cracks were present in the barrier layer at some contact edges. This is a cause for real concern. Typical metal 1 thinning was 60 percent including cap and barrier.
- Vias and contacts: Via and contact cuts appeared to have been dry-etched. No significant over-etching was found at contacts.
- Intermetal dielectric (IMD): Intermetal dielectric (between M2 and M1) consisted of four layers of glass. The second layer (SOG) had been subjected to an etchback to aid in planarization. No problems were found with these layers.
- Pre-metal glass: A layer of reflow glass (BPSG) over an undoped glass, over another thin layer of reflow glass and various grown oxides. Reflow was prior to contact cuts. No problems were found except that the multilayer structure appears to contribute significantly to the barrier cracking noticed.

ANALYSIS RESULTS II (continued)

- Polysilicon: Four layers of polysilicon were employed. Poly 4 and poly 3 were used exclusively in the SRAM cell array. Poly 2 which employed a tungsten-silicide was used as a metal substitute for interconnect. Poly 1 was used to form all gates on the die, including the select and storage gates in the array, and for redundancy fuses. A separate poly appeared to be used to form the emitter dopant source at bipolar NPN devices. Definition of the poly layers was by a dry etch of good quality.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries indicating a twin-well process was employed.
- Diffusions: Implanted N⁺ and P⁺ diffusions were used for sources and drains. An LDD process was used employing oxide sidewall spacers. The spacers were left in place. No problems were found in any of these areas.
- Bipolar devices: Poly provided the connections and was used as the dopant source for the emitters at bipolar NPN devices. A separate P⁺ diffusion was used for the bases. Deep N⁺ diffusions were used at collectors which were contacted by metal 1. All bipolar NPN devices were located in N-wells with buried layers. No problems were found in any of these areas.
- Wells: Twin-wells were used in a P substrate. As mentioned, a step was noted in the local oxide indicating a twin-well process was employed.
- Buried contacts: Interpoly/buried contacts were used in the cell array only.
- Fuses: All poly 1 redundancy fuses had overlay passivation and oxide cutouts over them. Some laser blown fuses were present.
- Memory cells: The memory cells consisted of a standard 4T SRAM cell design with TFT pullups. Metal 1 formed the bit lines via poly 2 links. Selectively-doped poly 4

ANALYSIS RESULTS II (continued)

was used to form the body of the pull-up devices and distribute Vcc. Poly 3 was used for cell interconnect and provided the gates for the TFTs. Poly 2 formed the bit line connections and distributed GND. Poly 1 formed all gates and word lines.

- Latch-up: Latch-up tests were performed on Sample 5 per JEDEC Standard No. 17. Pins were tested from -200mA to +200mA and revealed that no pin latched up on the sample (see appendix).
- ESD sensitivity: ESD tests were performed on Sample 6 and revealed that no significant leakage occurred prior to + 4000V; however, pin 1 failed at -4000V and pin 4 failed at +4000V.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

ESD and latch-up tests

X-ray

Package section and material analysis

Decapsulate

Internal optical inspection

SEM inspection of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal and inspect metal 2

Delayer to metal 1 and inspect

Aluminum removal (metal 1), inspect barrier

Delayer to poly/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Poor

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	N
Dicing quality	N
Die attach method	Silver-filled epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	P*
Metal registration	N
Contact coverage	G
Contact registration	G

**100 percent metal 1 aluminum thinning and cracks in the barrier.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

SONY JAPAN
CXX5B16120J-12
604D24E Z

BOTTOM

NONE

WIREBOND STRENGTH

Wire material: 1.2 mil diameter gold
Die pad material: aluminum
Material at package lands: silver

Sample # 1

of wires pulled: 24
Bond lifts: 0
Force to break - high: 17 g
- low: 12 g
- avg.: 14.2 g
- std. dev.: 1.3

PACKAGE MATERIAL ANALYSIS

Leadframe: Copper (Cu)
External pin plating: Tin-lead (SnPb) solder over tin (Sn) flash
Internal plating: Silver (Ag) over a gold (Au) flash
Die attach: Silver-filled epoxy

DIE MATERIAL ANALYSIS

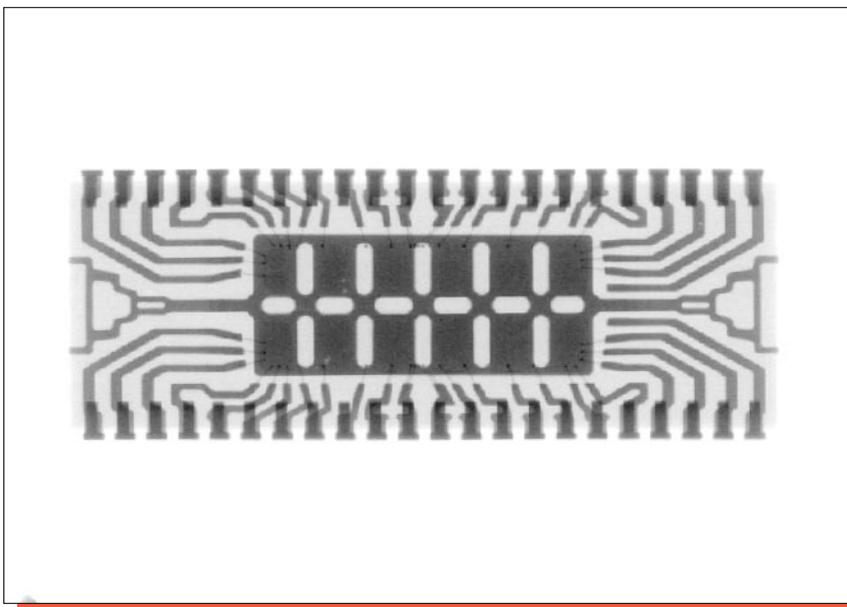
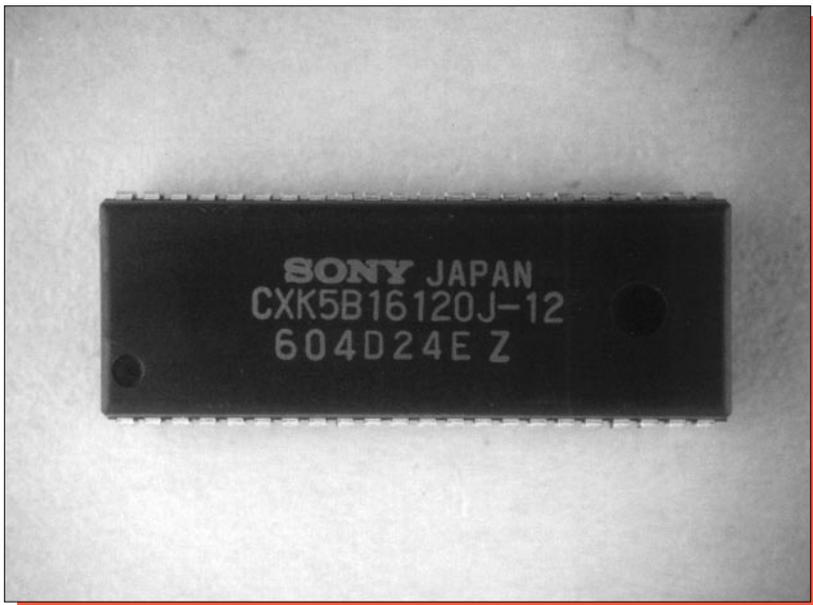
Overlay passivation:	Single thick layer of nitride.
Metallization 2:	Aluminum with a titanium barrier.
Intermetal dielectric (M2 to M1):	Four layers of glass including an SOG.
Metallization 1:	Aluminum with a titanium-nitride cap and barrier.
Intermediate glass:	BPSG containing 3.1 wt. percent boron and 6.7 wt. percent phosphorus over undoped glass over a thin layer of reflow glass (BPSG) over densified oxides.
Silicide:	Tungsten-silicide on polysilicon 1 and 2.

VERTICAL DIMENSIONS

Die thickness: 0.3 mm (13.5 mils)

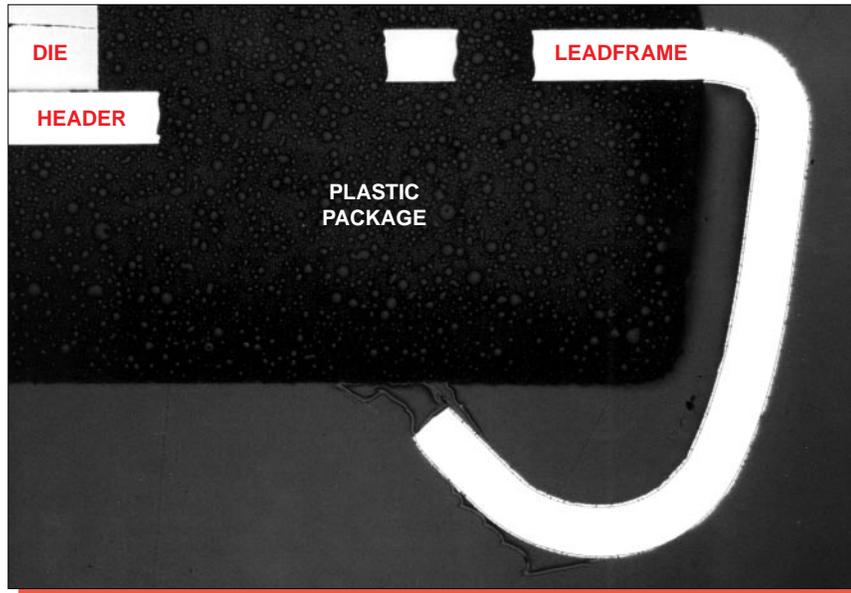
Layers

Passivation:	0.9 micron
Metal 2 - aluminum:	0.9 micron
- barrier:	0.2 micron
Intermetal dielectric (IMD):	0.5 - 0.7 micron
Metal 1 - cap:	0.04 micron (approximate)
- aluminum:	0.3 micron
- barrier:	0.1 micron
Pre-metal glass:	0.45 micron (average)
Poly 4:	0.03 micron
Poly 3:	0.04 micron
Poly 2 - silicide:	0.05 micron
- poly 2:	0.04 micron
Poly 1 - silicide:	0.06 micron
- poly 1:	0.1 micron
Local oxide (under poly 1):	0.25 micron
N+ S/D diffusion:	0.15 micron
Deep N+ diffusion (collector):	0.5 micron
P+ S/D diffusion:	0.2 micron
P+ (base):	0.3 micron
N+ (emitter):	0.15 micron
N- well/N+ buried layer:	2.2 microns
P- well:	could not delineate

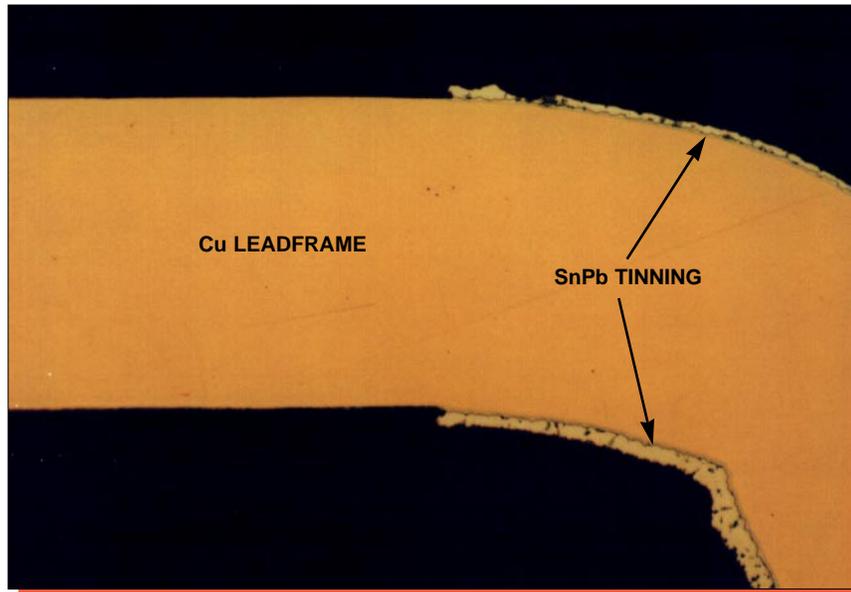


A4	1	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	\overline{OE}
A0	5	40	\overline{UB}
\overline{CE}	6	39	\overline{LB}
I/O1	7	38	I/O16
I/O2	8	37	I/O15
I/O3	9	36	I/O14
I/O4	10	35	I/O13
V _{CC}	11	34	GND
GND	12	33	V _{CC}
I/O5	13	32	I/O12
I/O6	14	31	I/O11
I/O7	15	30	I/O10
I/O8	16	29	I/O9
\overline{WE}	17	28	N.C.
A15	18	27	A8
A14	19	26	A9
A13	20	25	A10
A12	21	24	A11
N.C.	22	23	N.C.

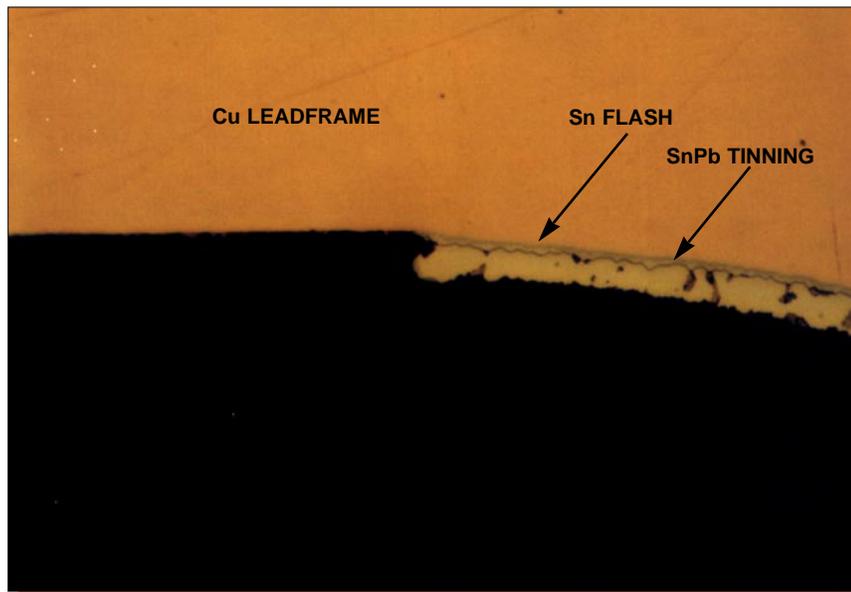
Figure 1. Package photograph, x-ray, and pinout of the Sony CXK5B16120J-12 1Mbit BiCMOS SRAM. Mag. 3x.



Mag. 30x

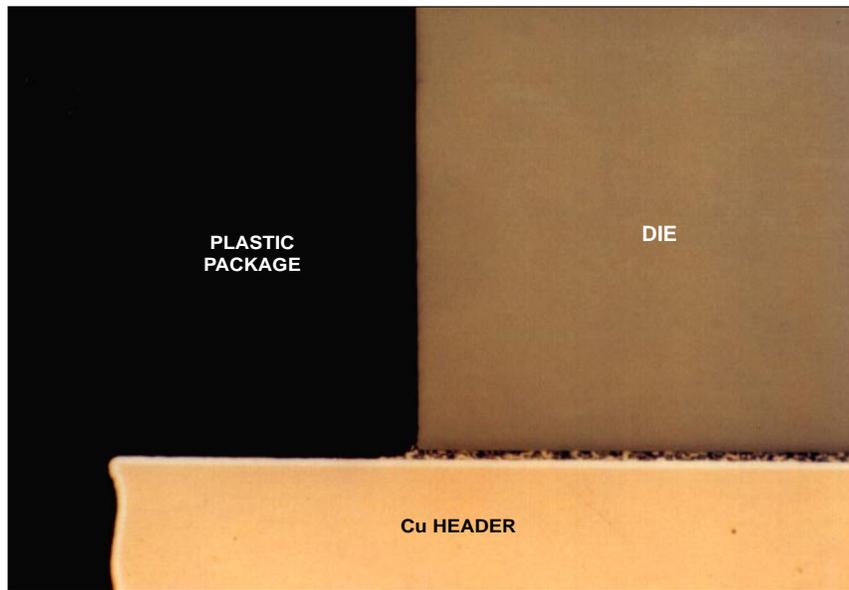


Mag. 200x

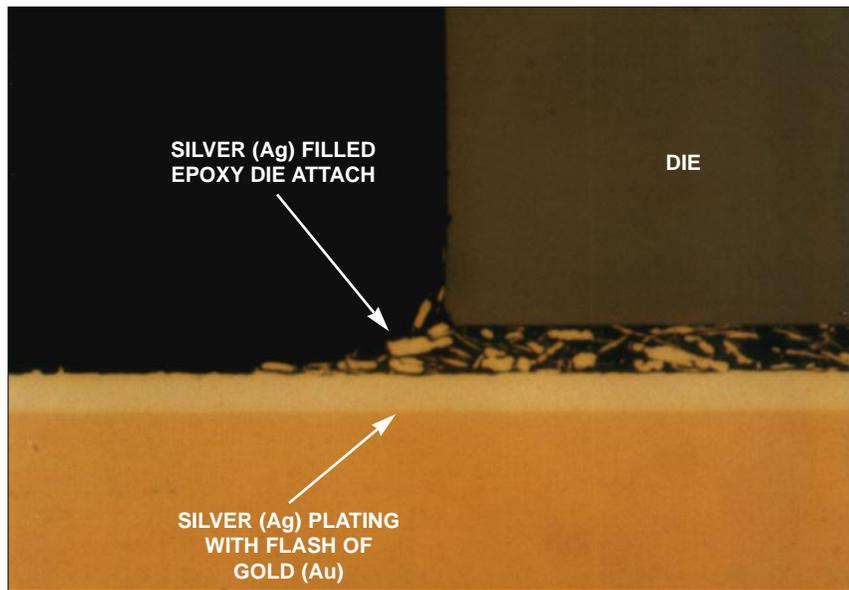


Mag. 500x

Figure 2. Package section views of the leadframe and leadframe exit.



Mag. 160x

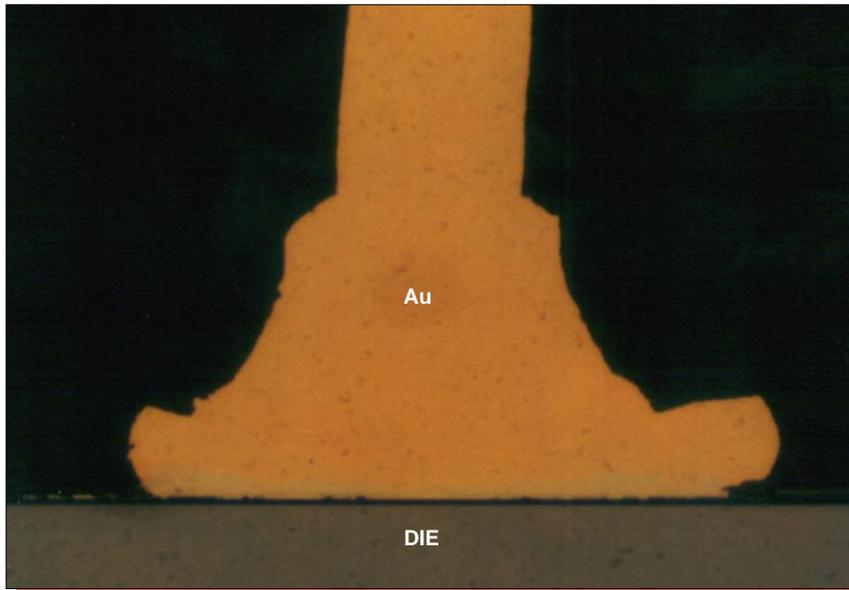


Mag. 800x

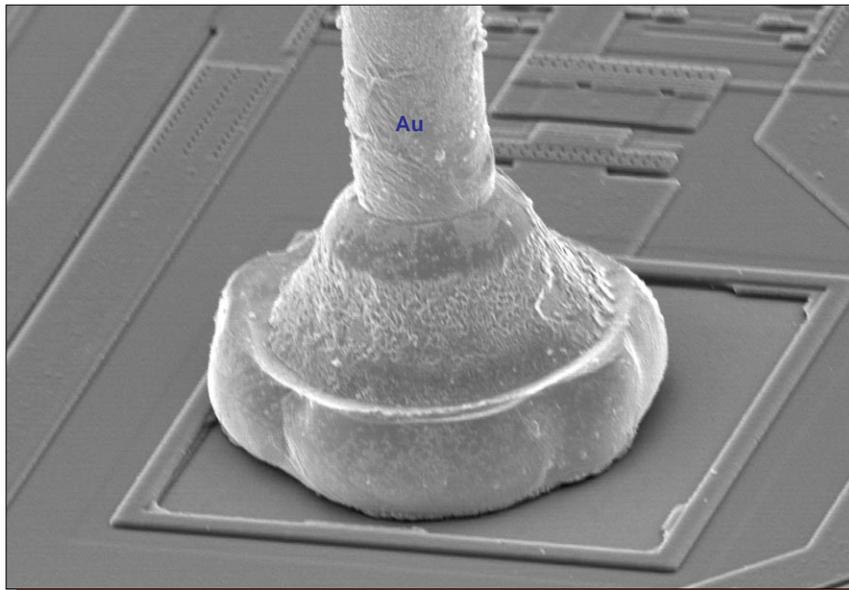


Mag. 800x

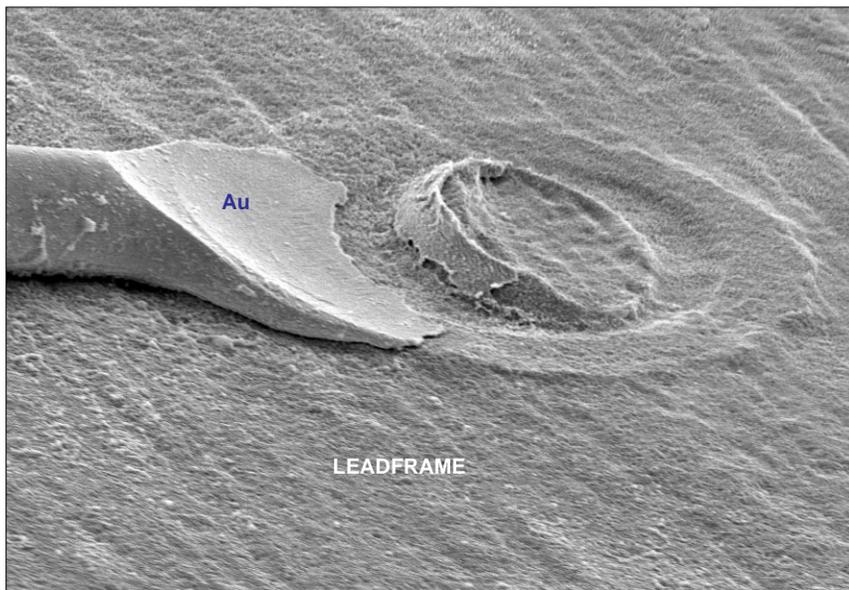
Figure 3. Package section views illustrating dicing, die attach, and die coat.



Mag. 800x

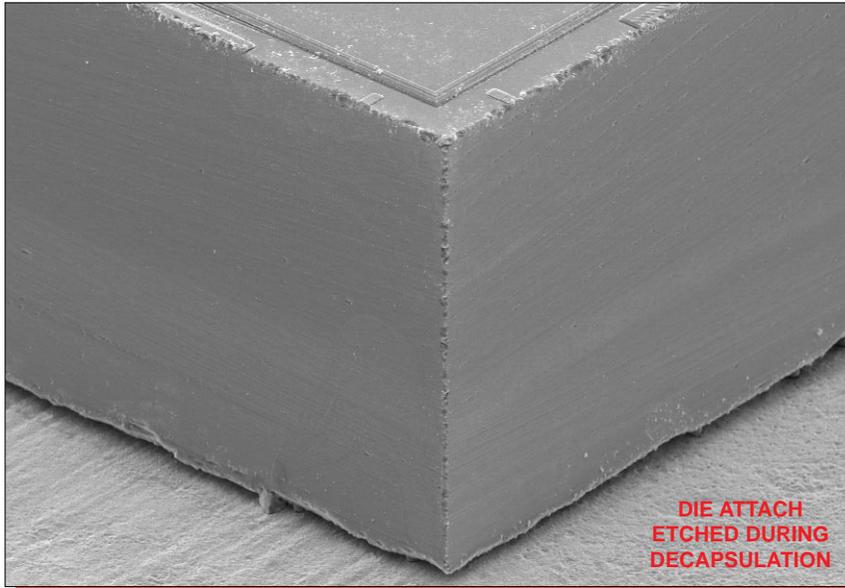


Mag. 600x, 60°

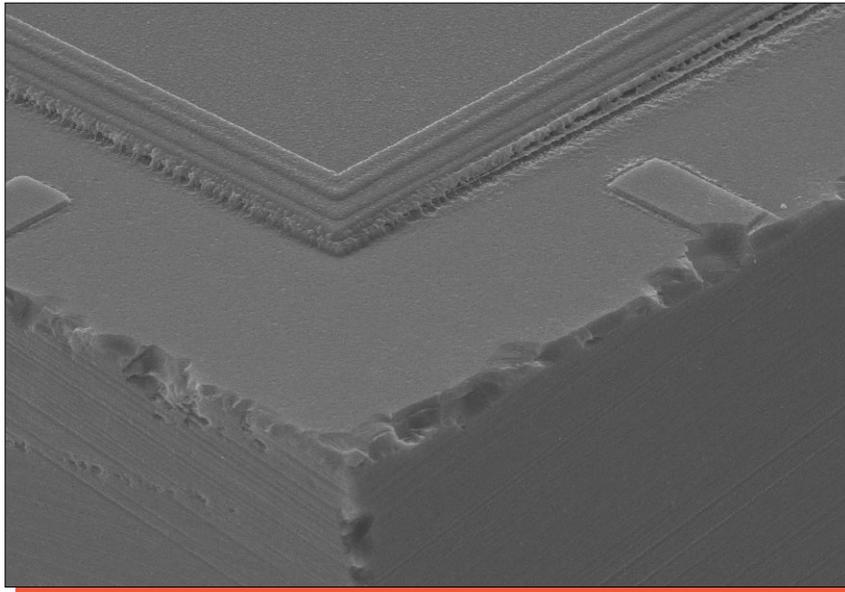


Mag. 500x, 60°

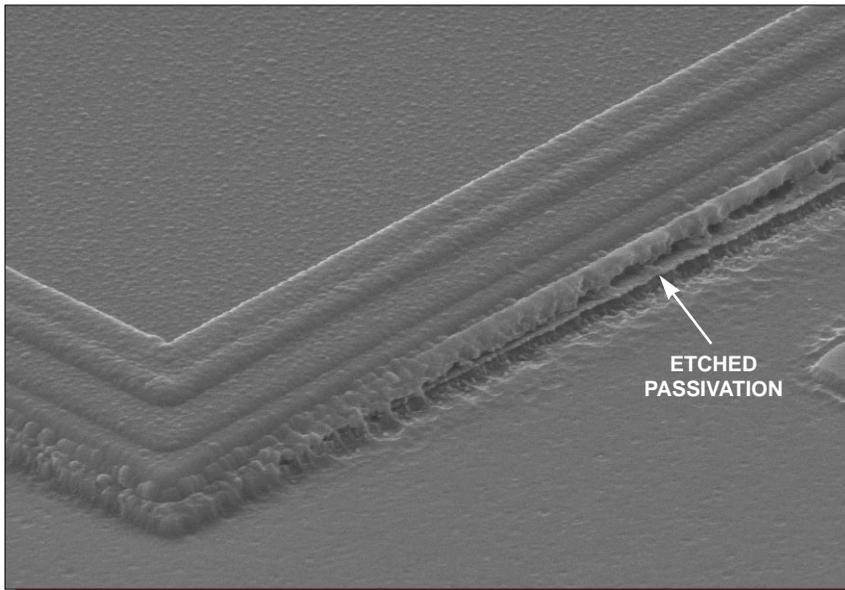
Figure 4. Optical and SEM views of typical wirebonds.



Mag. 160x



Mag. 1000x



Mag. 2500x

Figure 5. SEM views of a die corner and edge seal. 60°.

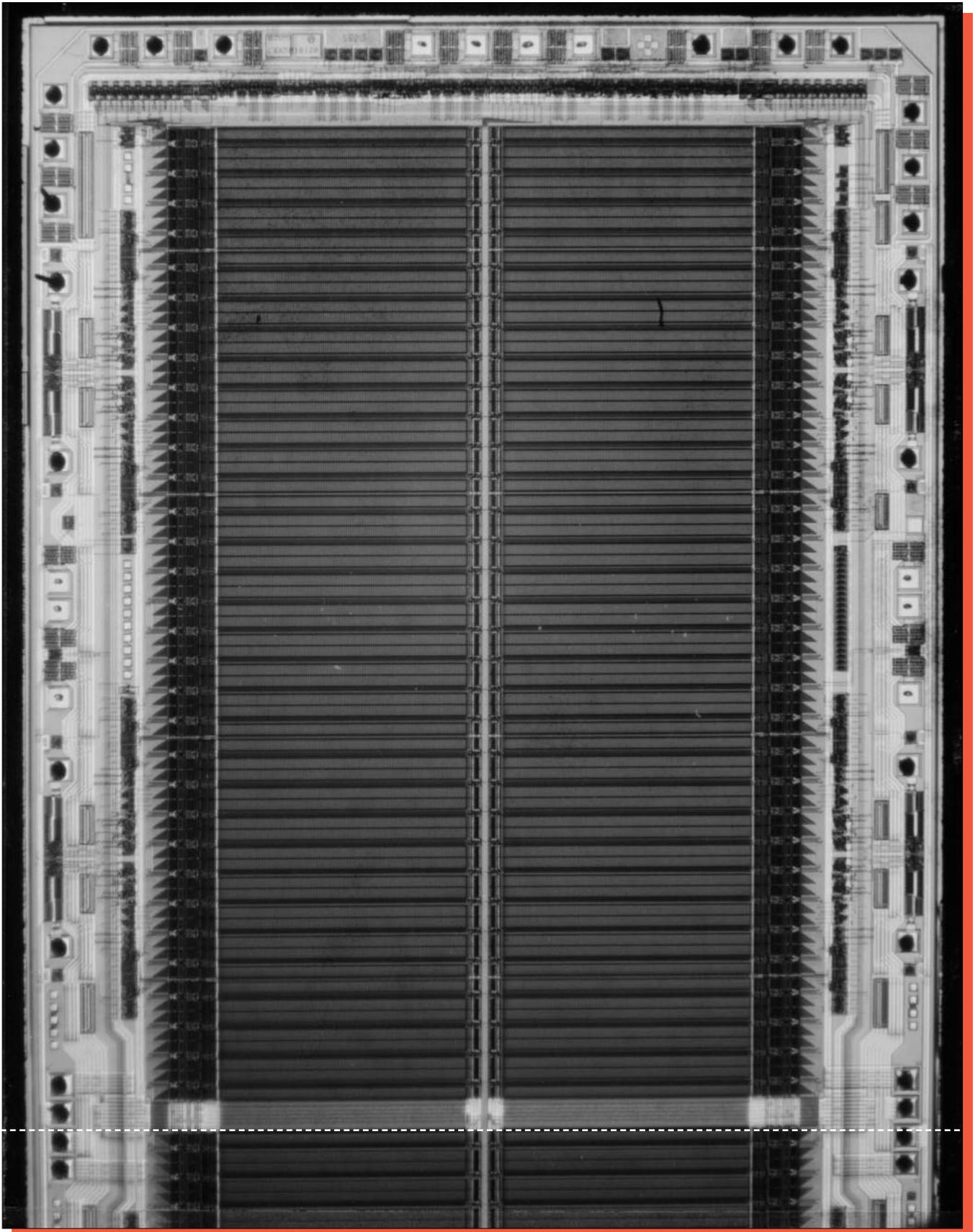


Figure 6. Portion of the Sony CXK5B16120J-12 die. Mag. 32x.

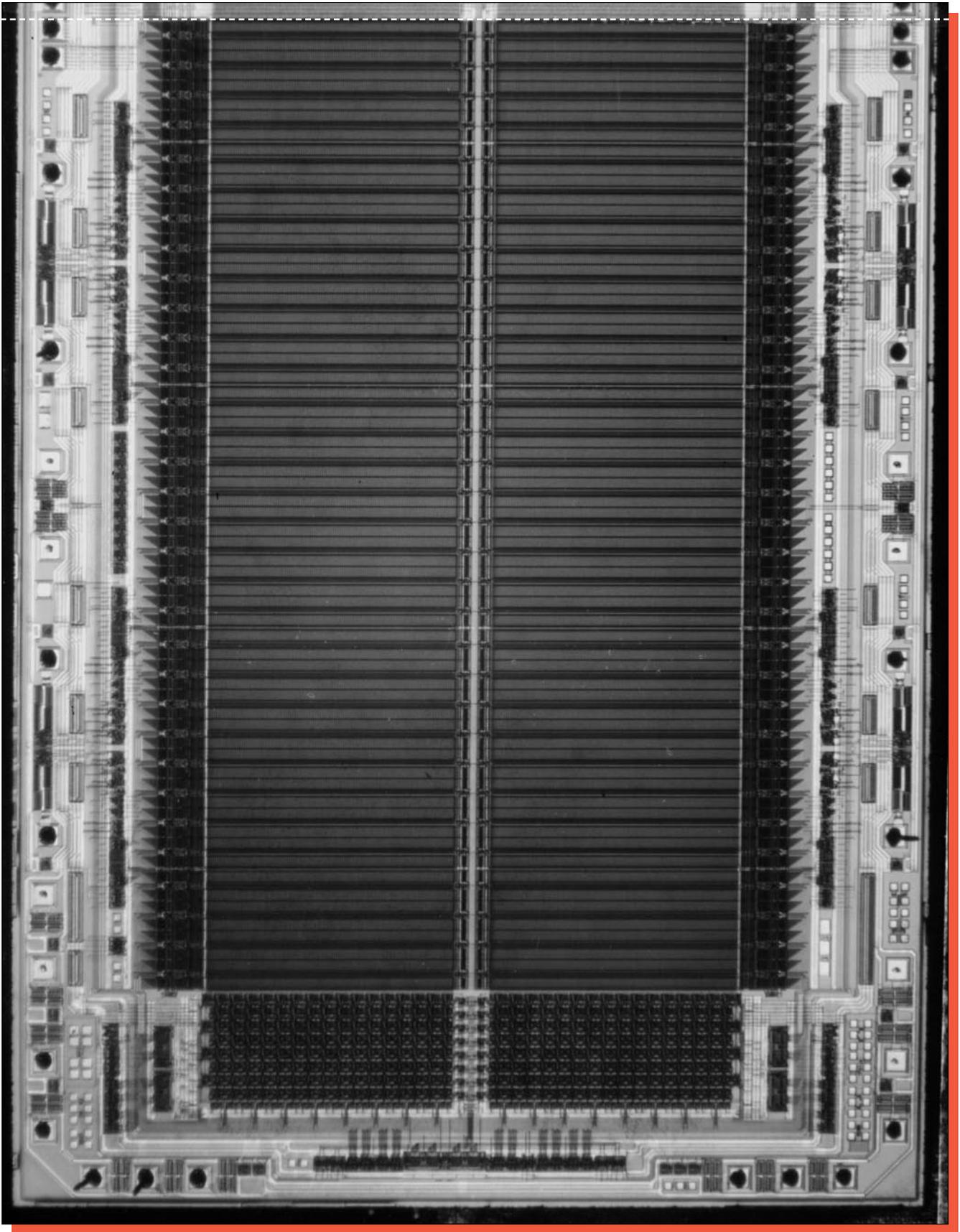


Figure 6a. Remaining portion of the Sony CXK5B16120J-12 die. Mag. 32x.

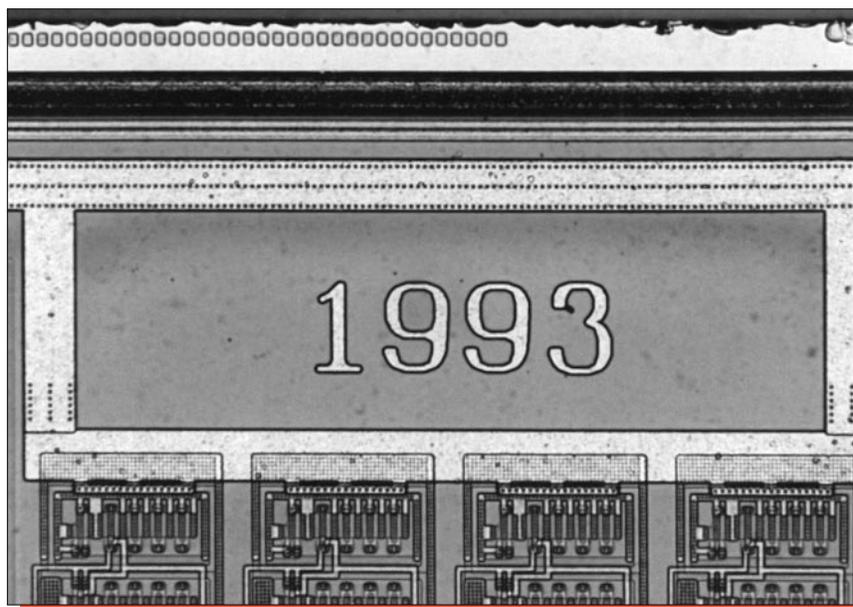
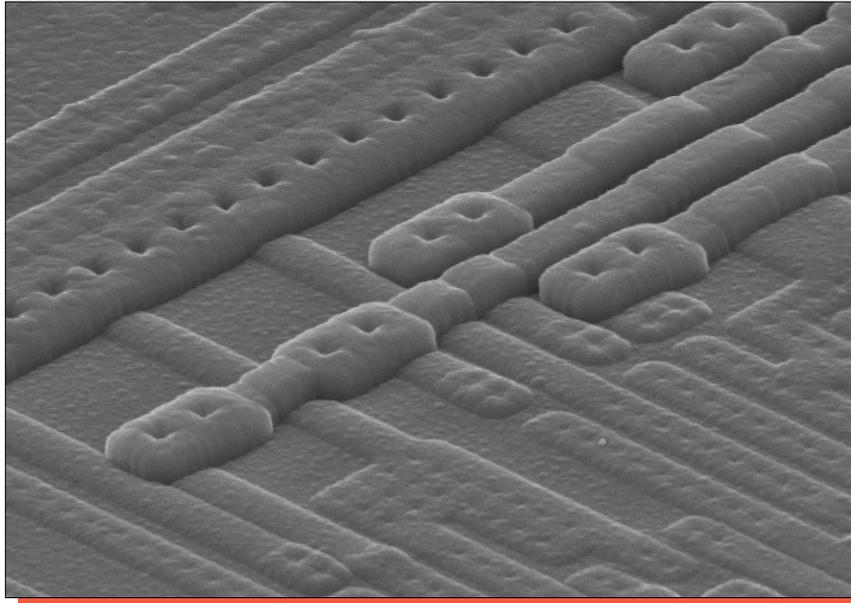
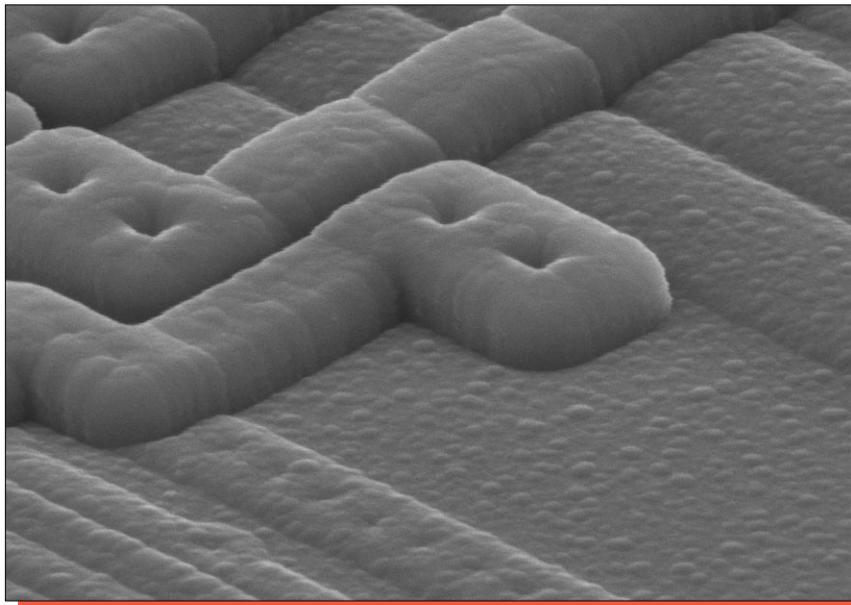


Figure 7. Die identification markings on the surface. Mag. 320x.

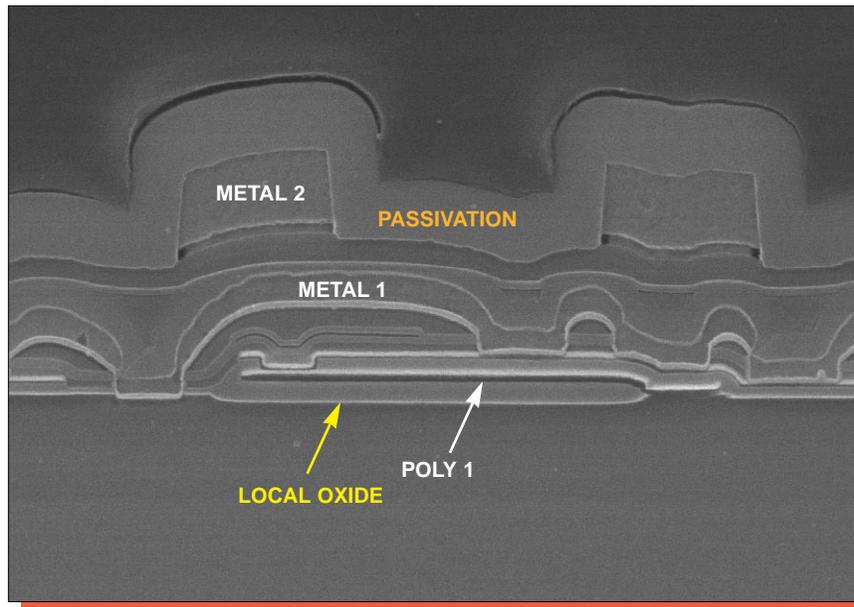


Mag. 3000x

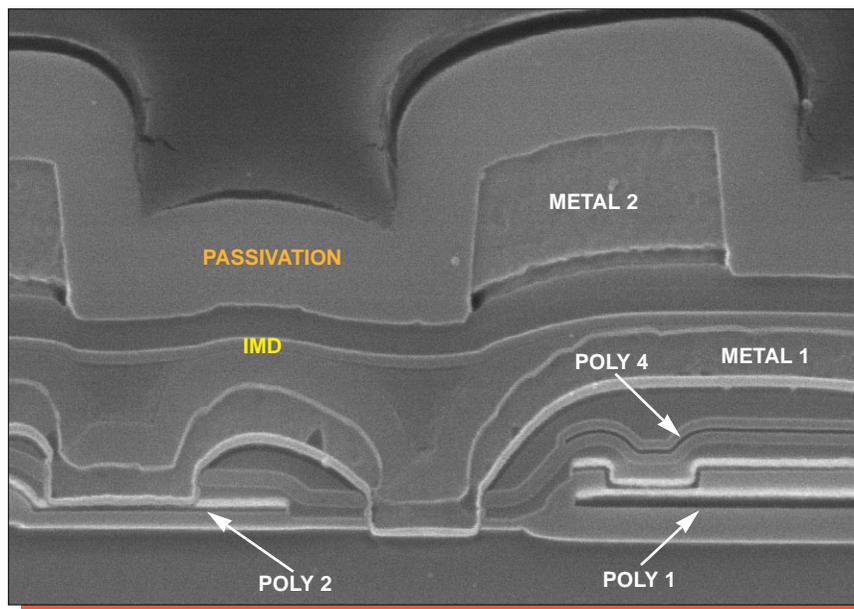


Mag. 6500x

Figure 8. SEM views illustrating passivation coverage. 60°.

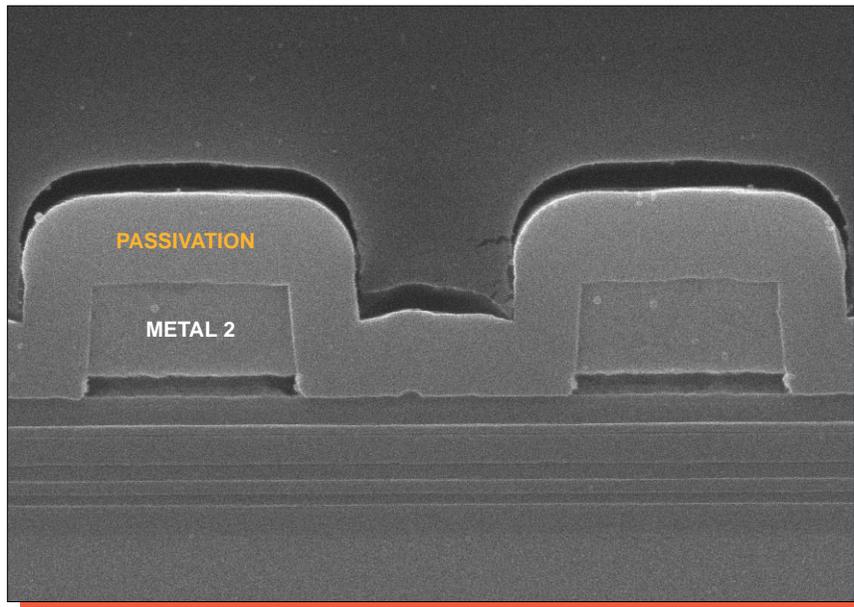


Mag. 10,000x

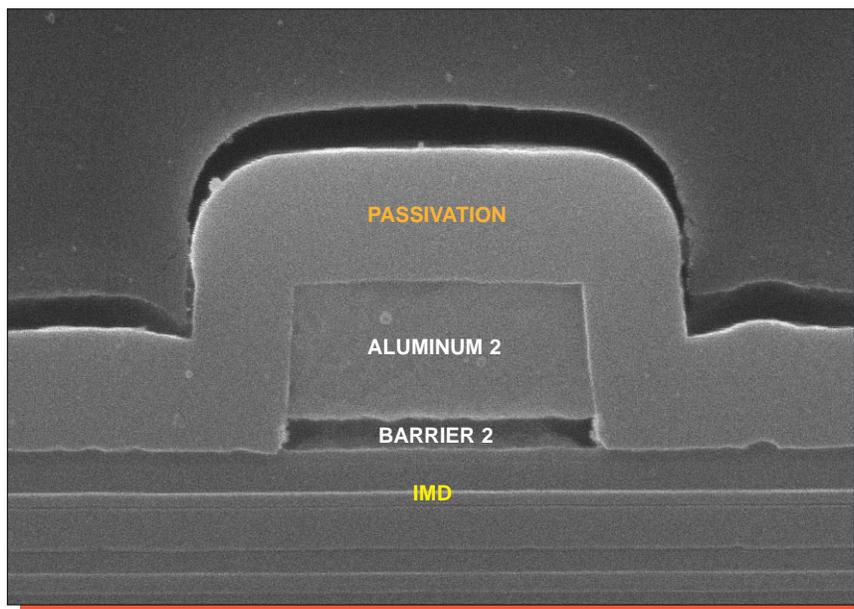


Mag. 16,000x

Figure 9. SEM section views illustrating general construction.

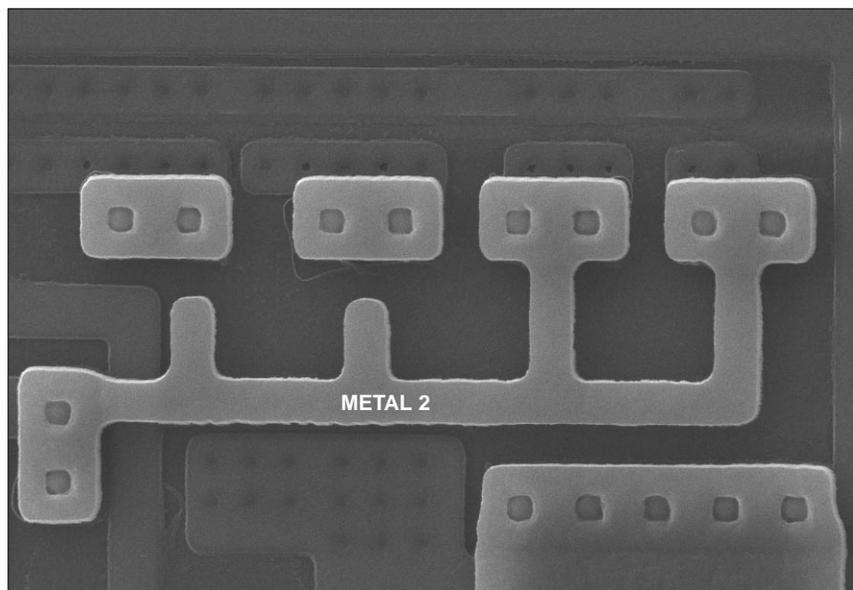


Mag. 13,000x

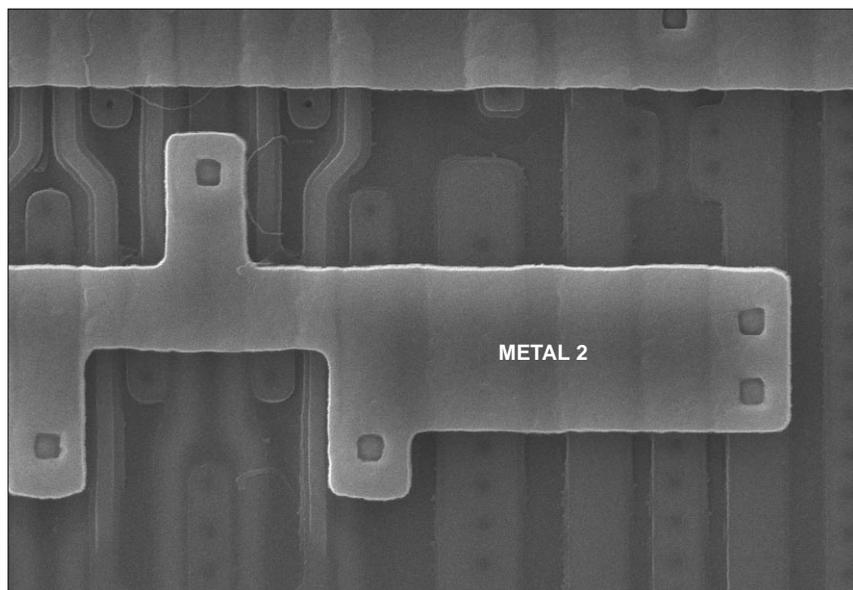


Mag. 20,000x

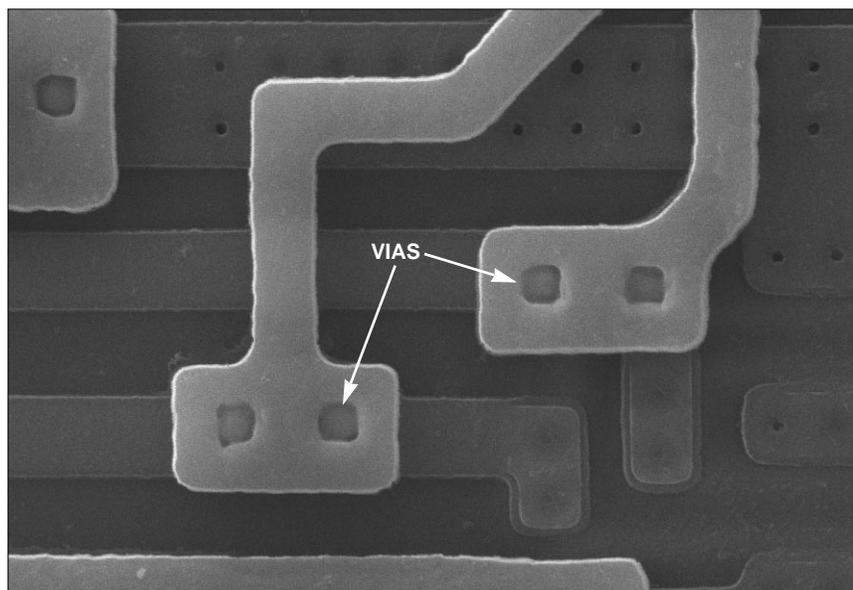
Figure 10. SEM section views of metal 2 line profiles.



Mag. 3300x

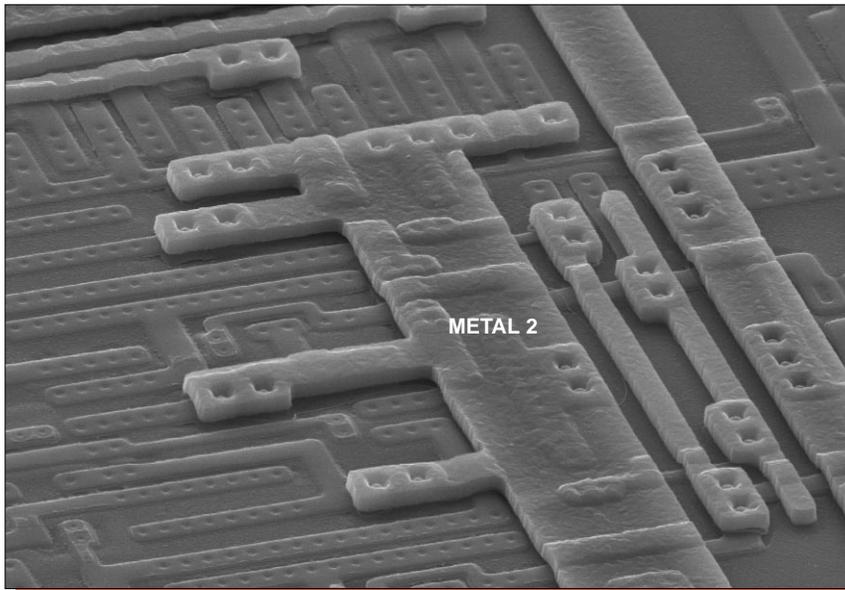


Mag. 3300x

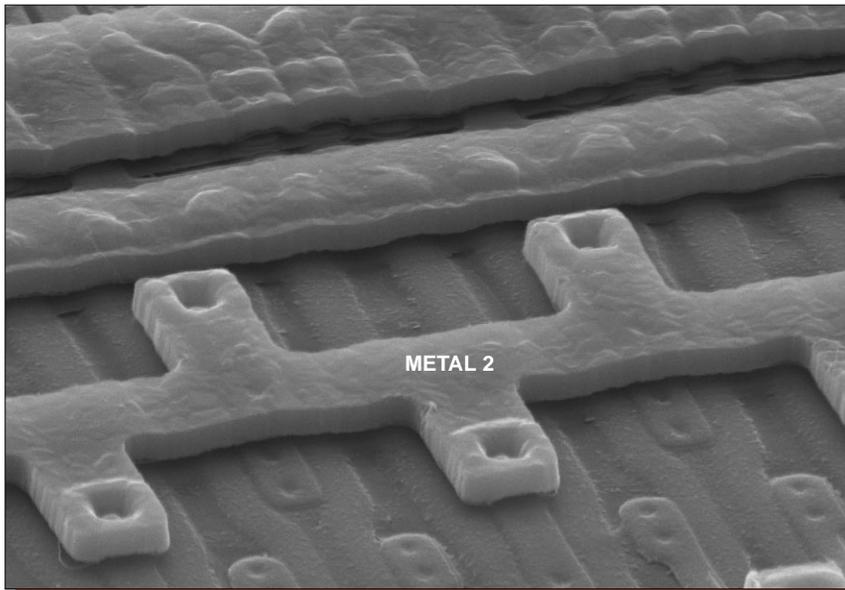


Mag. 5000x

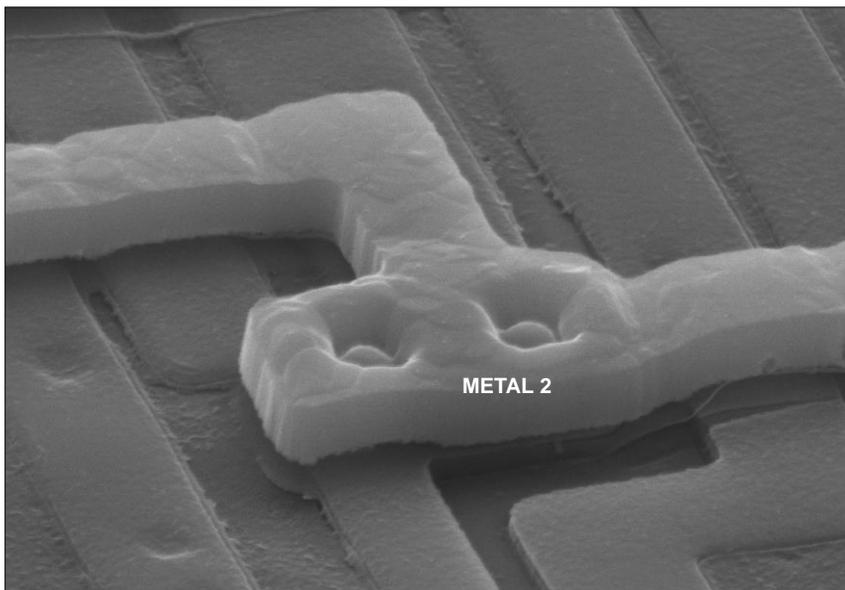
Figure 11. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 1500x

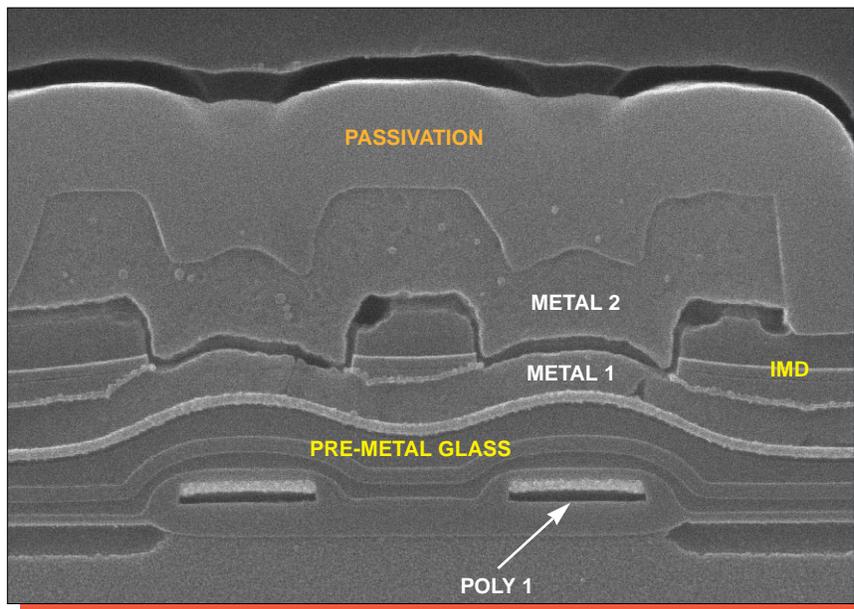


Mag. 3000x

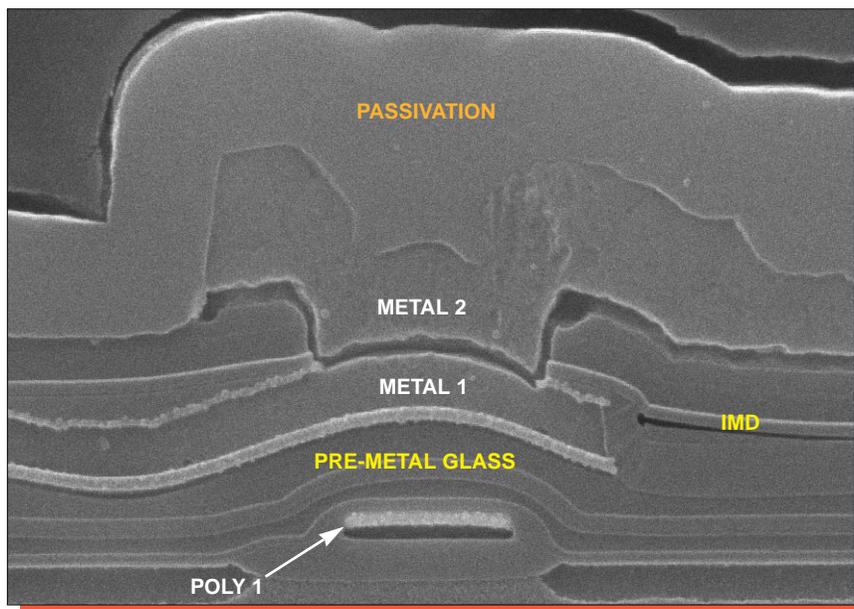


Mag. 6000x

Figure 12. Perspective SEM views illustrating metal 2 coverage. 60°.

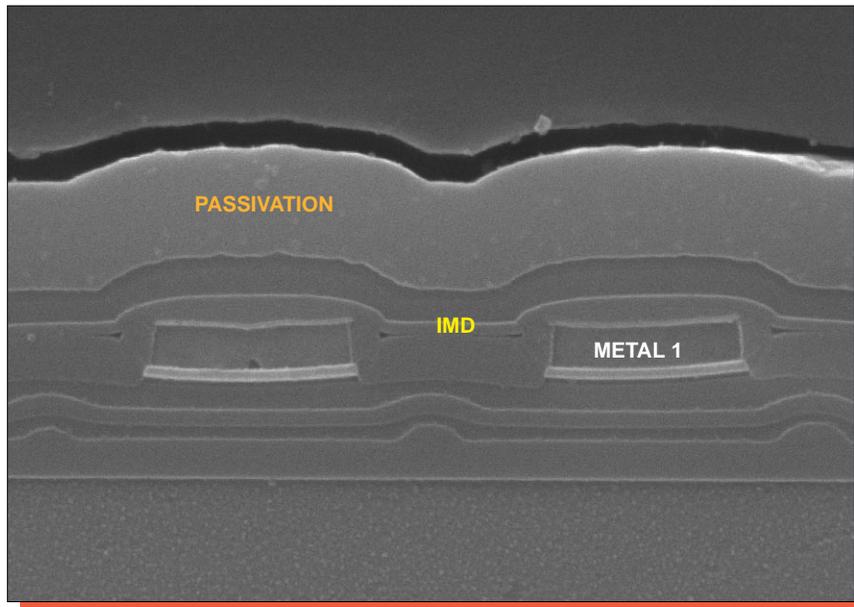


Mag. 16,000x

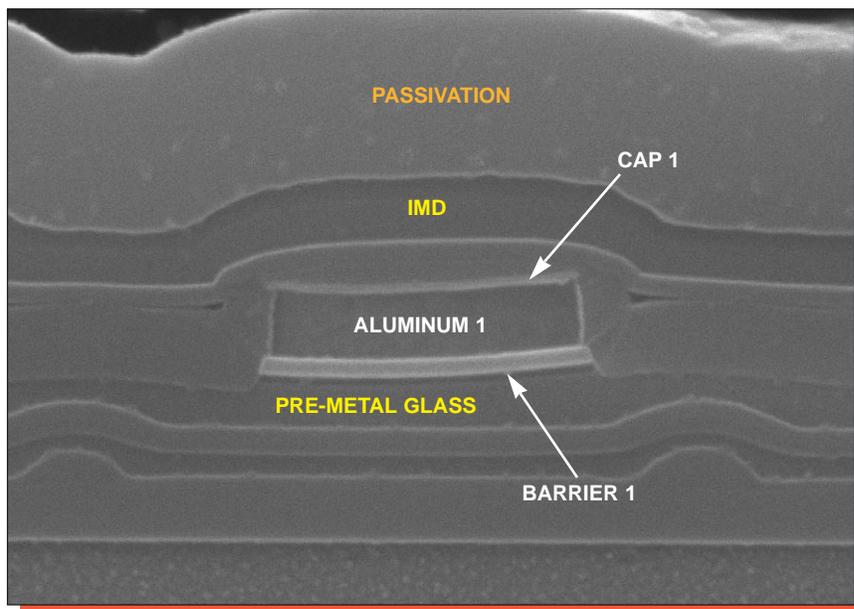


Mag. 20,000x

Figure 13. SEM section views of metal 2 vias.

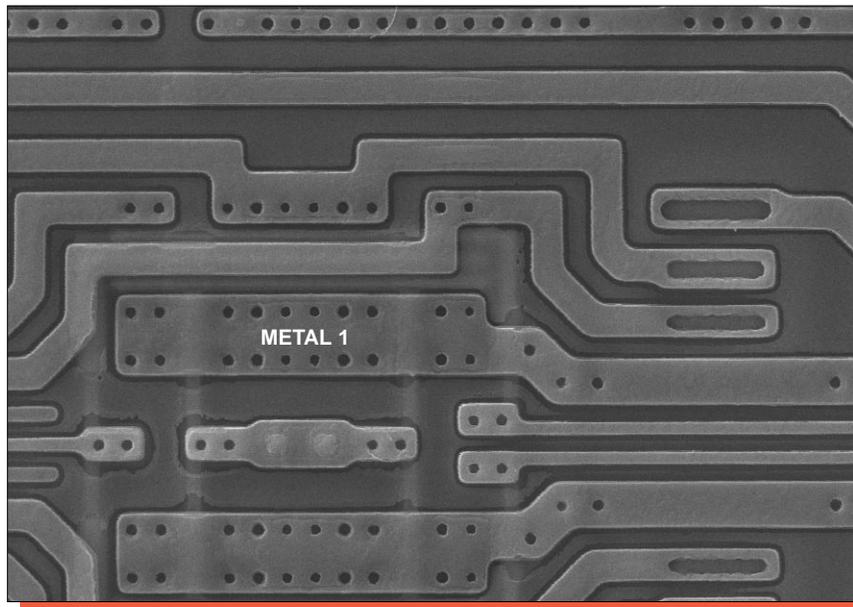


Mag. 16,000x

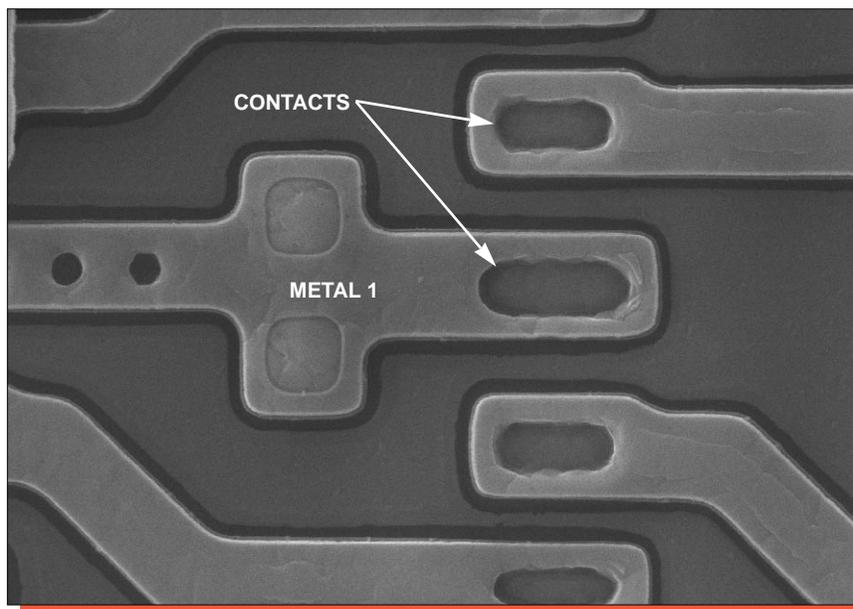


Mag. 26,000x

Figure 14. SEM section views of metal 1 line profiles.

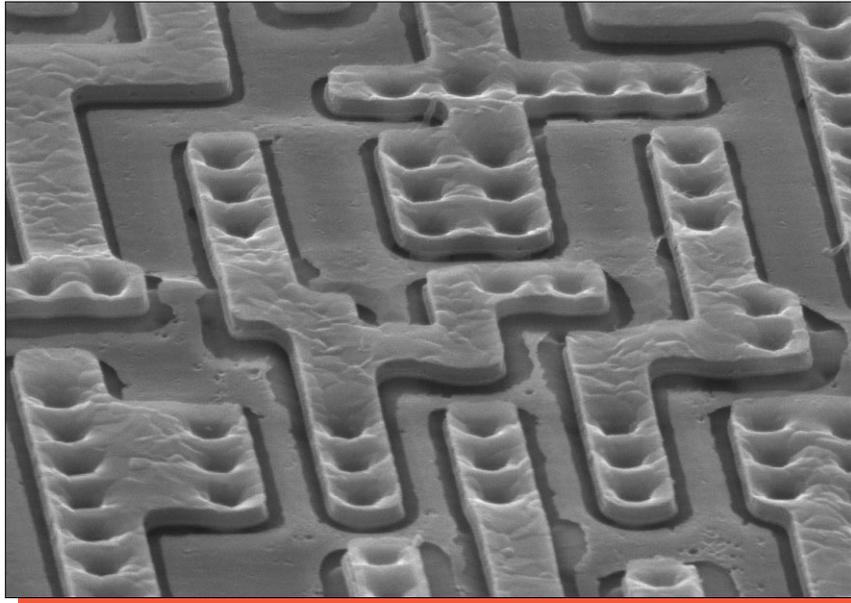


Mag. 2500x

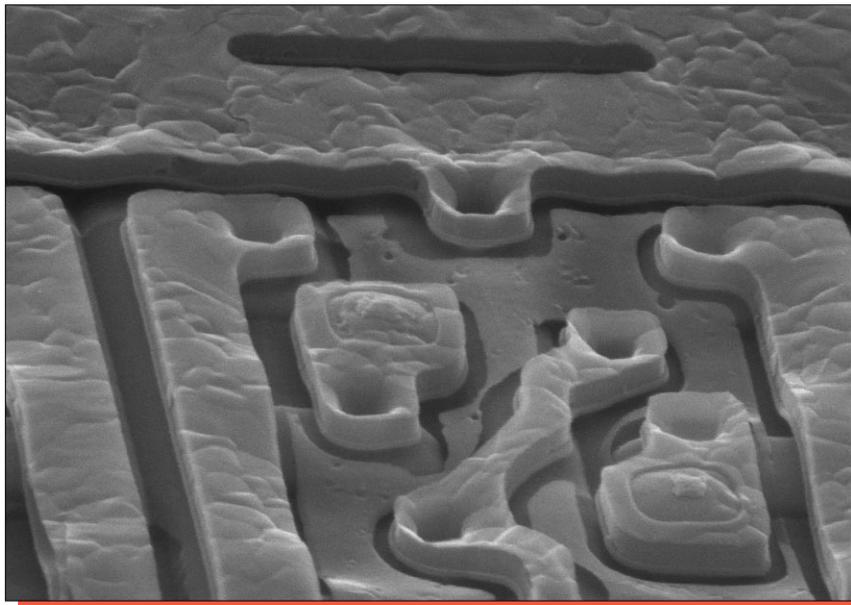


Mag. 6500x

Figure 15. Topological SEM views illustrating metal 1 patterning. 0°.



Mag. 5000x



Mag. 10,000x

Figure 16. Perspective SEM views of metal 1 coverage. 60°.

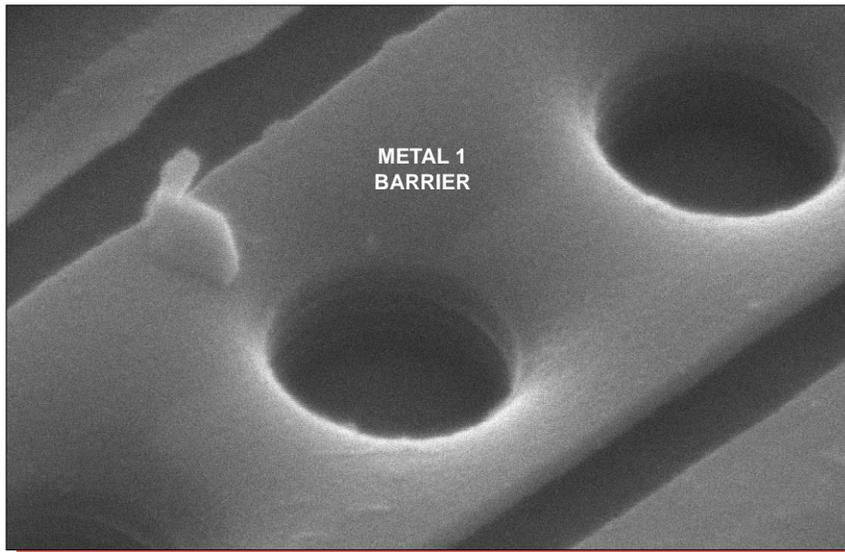
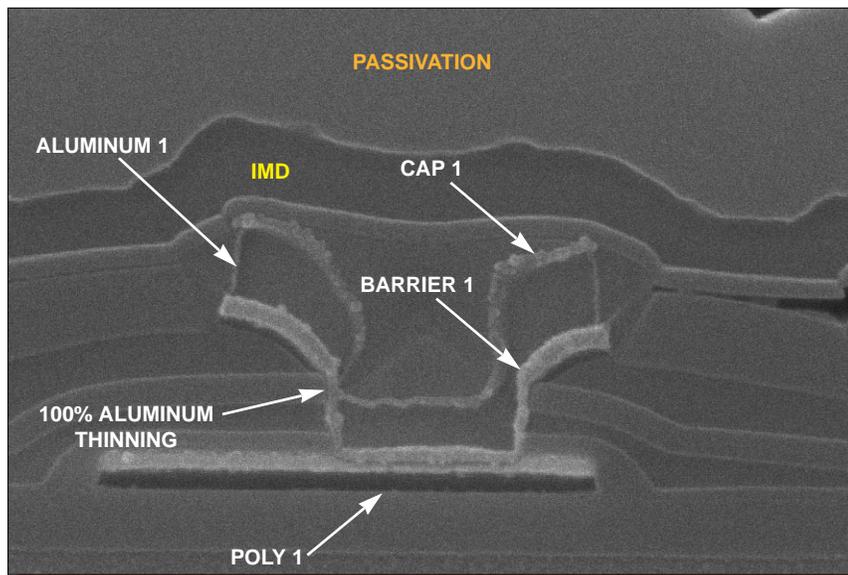
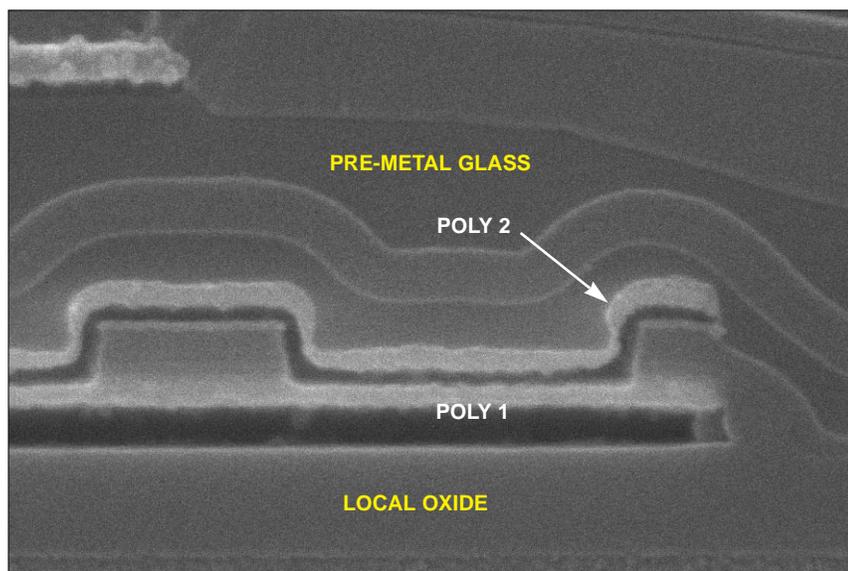


Figure 17. SEM view of metal 1 barrier, Mag. 40,000x, 45°.

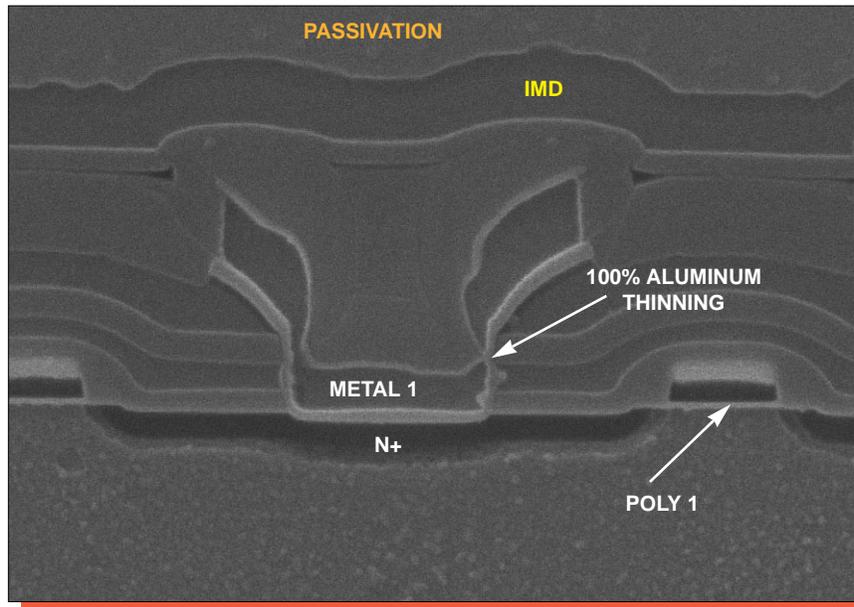


metal 1-to-poly 1,
Mag. 30,000x

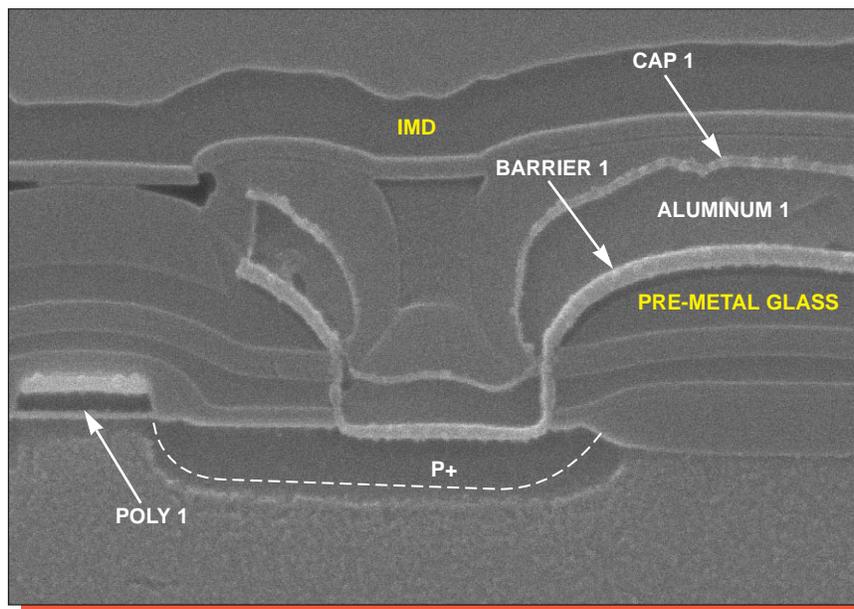


poly 2-to-poly 1,
Mag. 52,000x

Figure 18. SEM section views of typical contacts to poly 1.

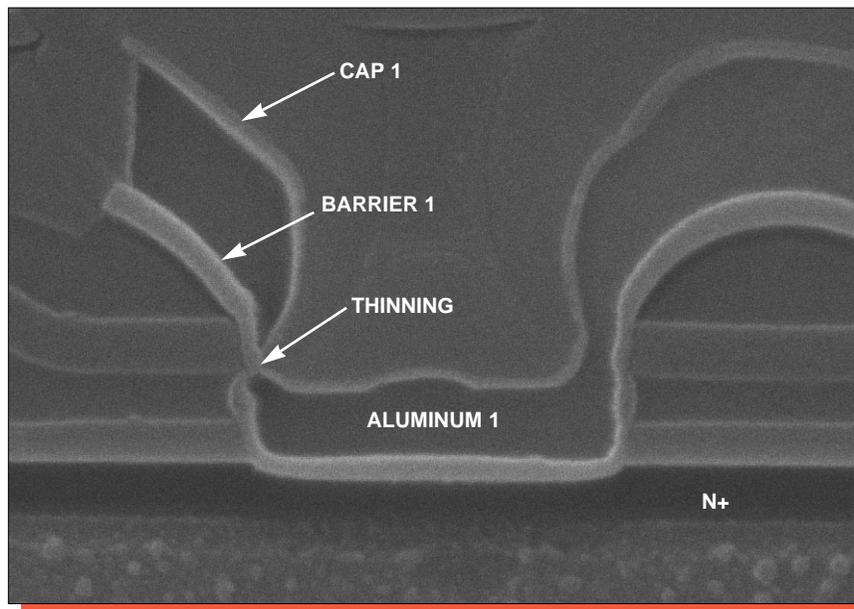


metal 1-to-N+

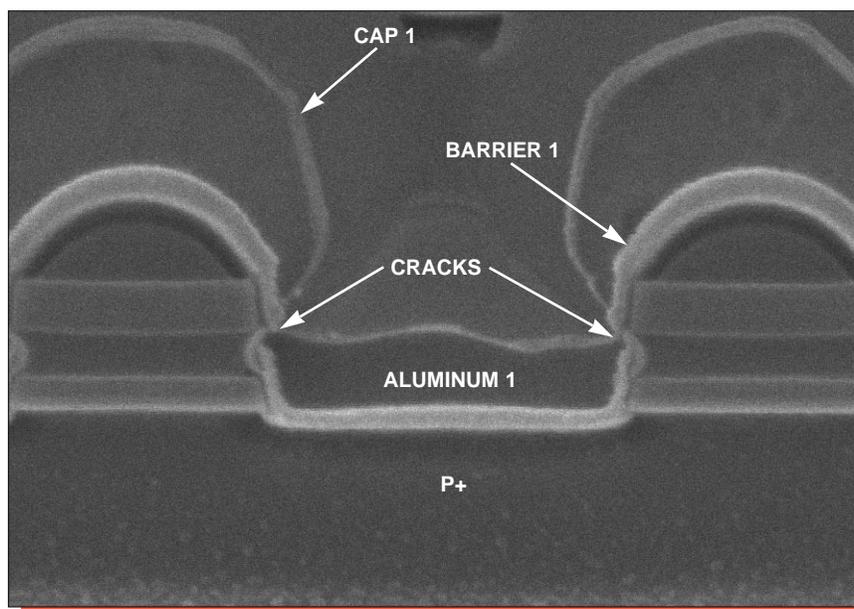


metal 1-to-P+

Figure 19. SEM section views of typical contacts to diffusion. Mag. 30,000x.

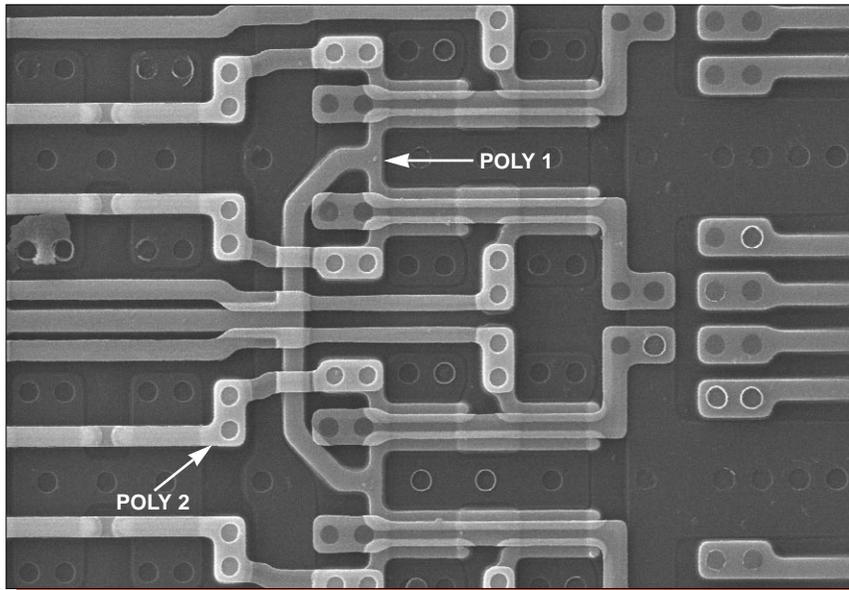


metal 1-to-N+

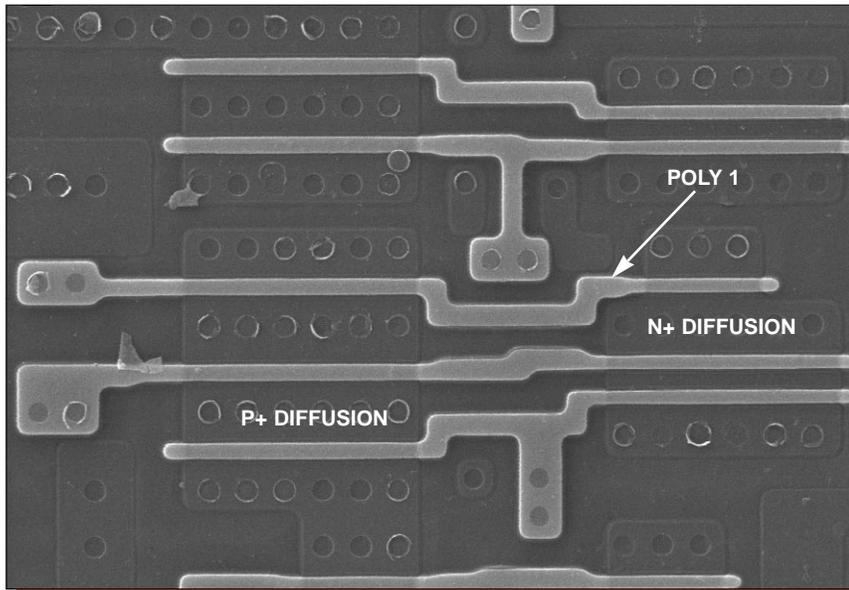


metal 1-to-P+

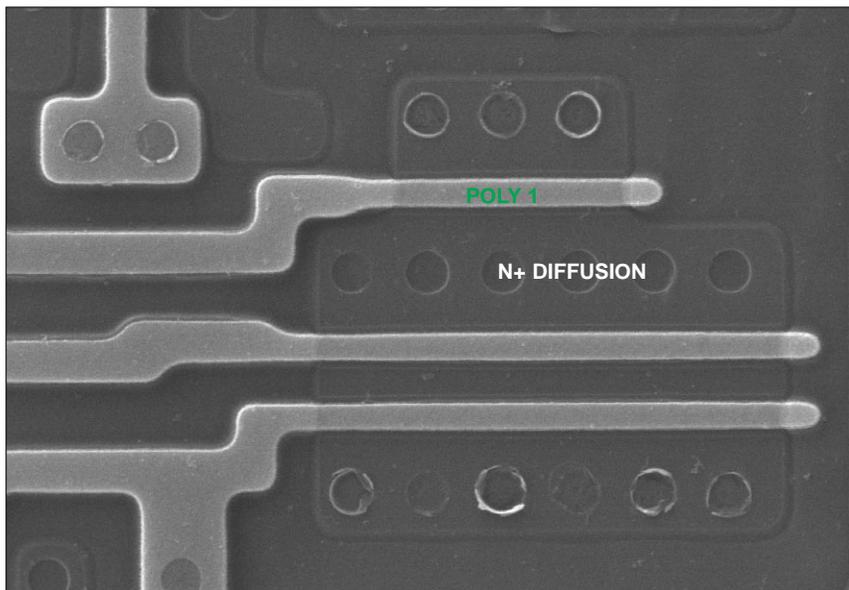
Figure 19a. SEM section views illustrating metal 1 thinning. Mag. 52,000x.



Mag. 3300x

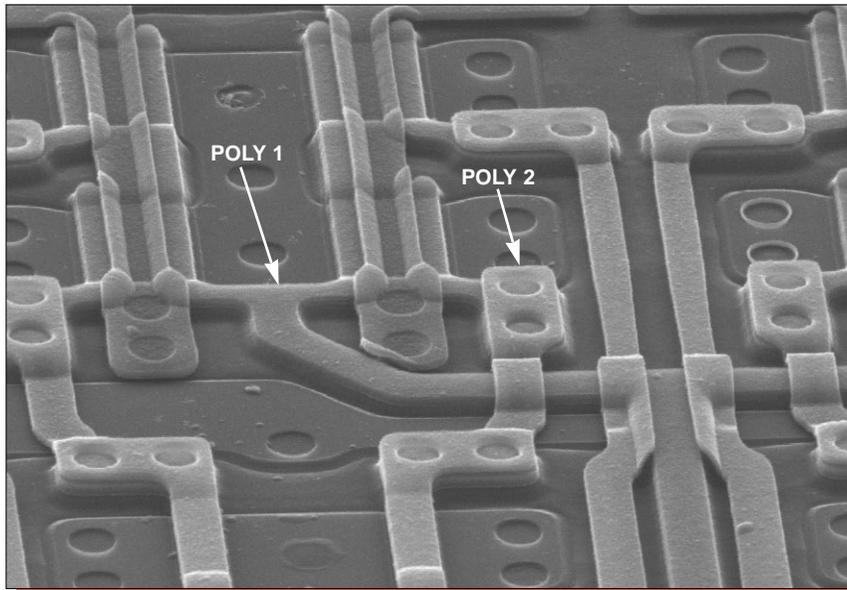


Mag. 3300x

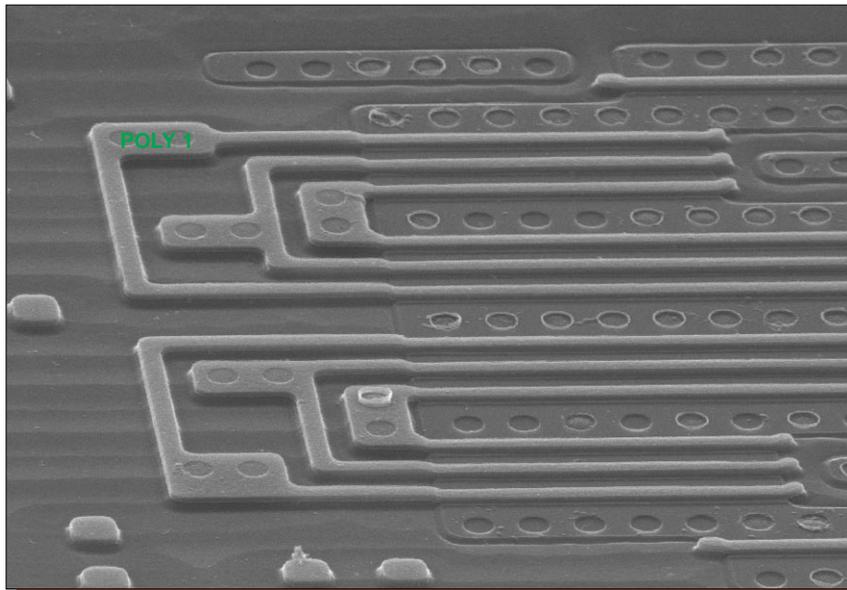


Mag. 6500x

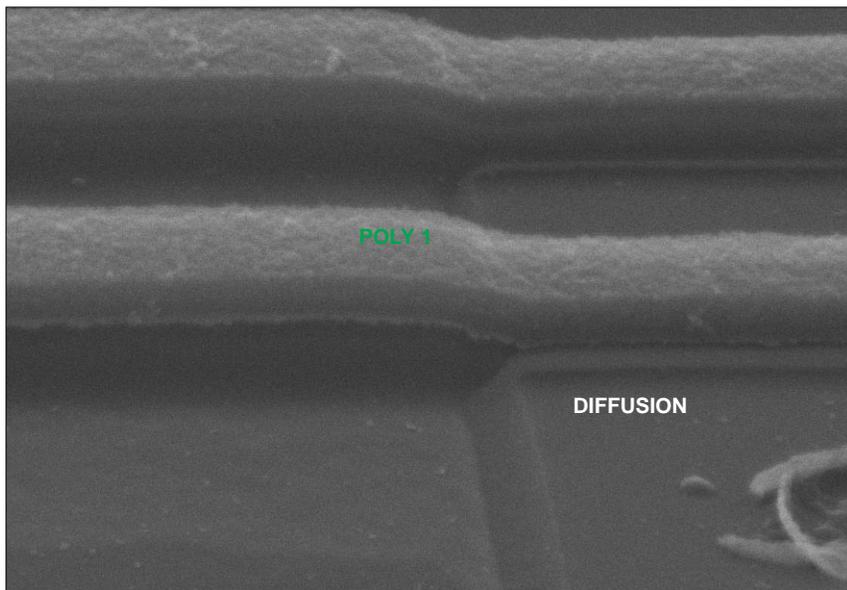
Figure 20. Topological SEM views illustrating poly 2 and poly 1 patterning. 0°.



Mag. 8000x

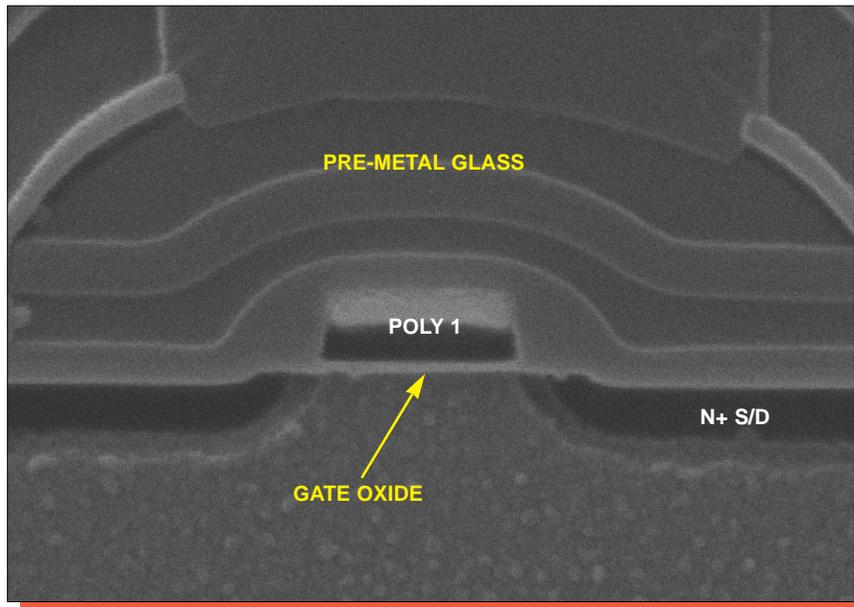


Mag. 5000x

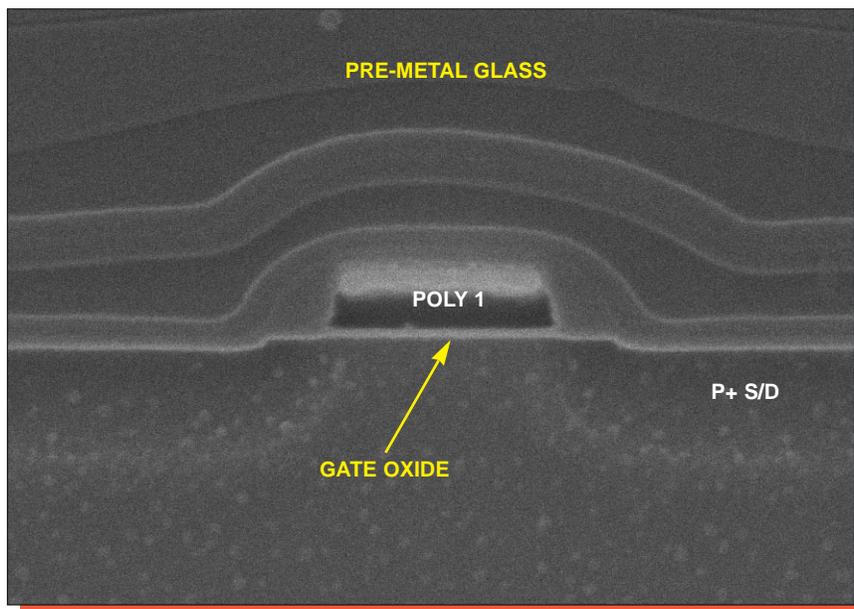


Mag. 40,000x

Figure 21. Perspective SEM views illustrating poly 2 and poly 1 coverage. 60°.

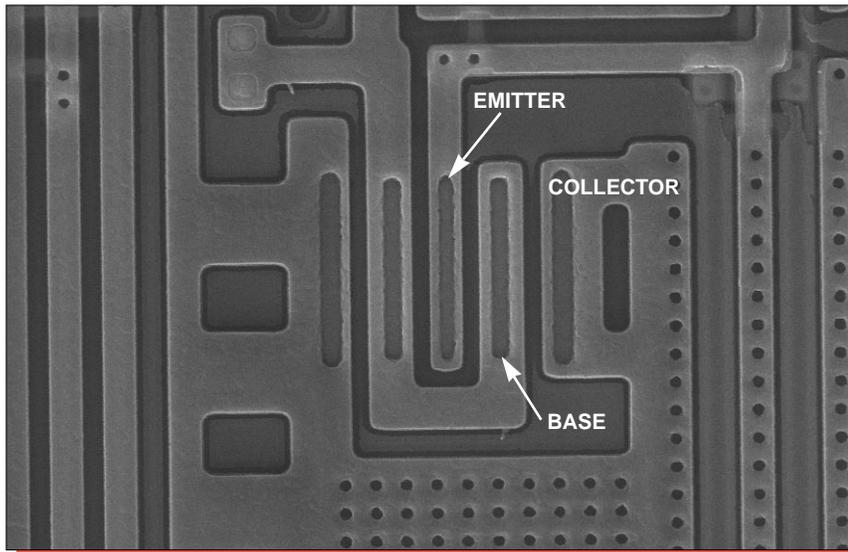


N-channel

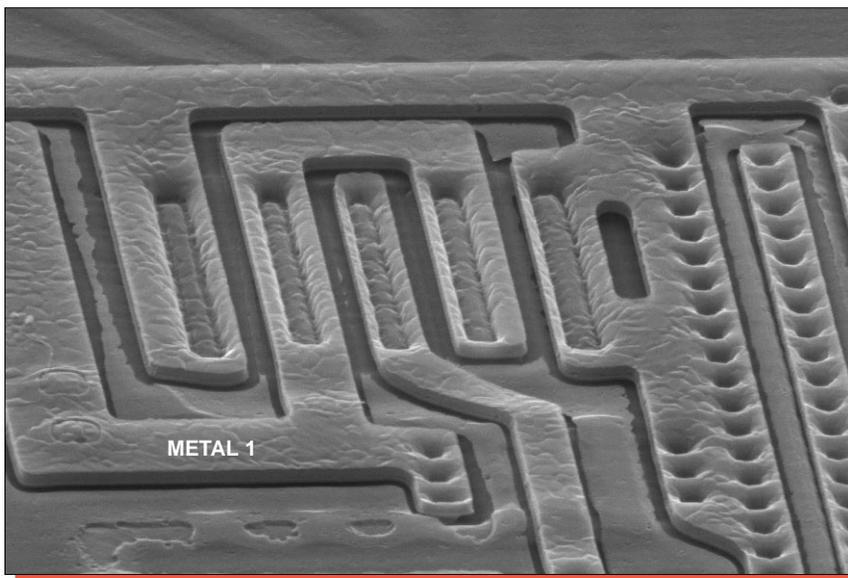


P-channel

Figure 22. SEM section views of typical transistors. Mag. 52,000x.



Mag. 2500x, 0°



Mag. 3000x, 60°

Figure 23. Topological and perspective SEM views of a bipolar device.

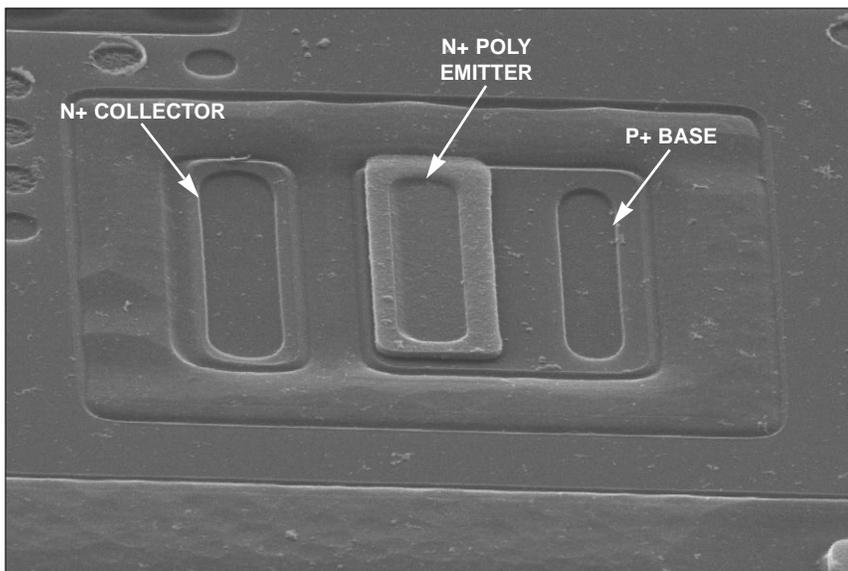
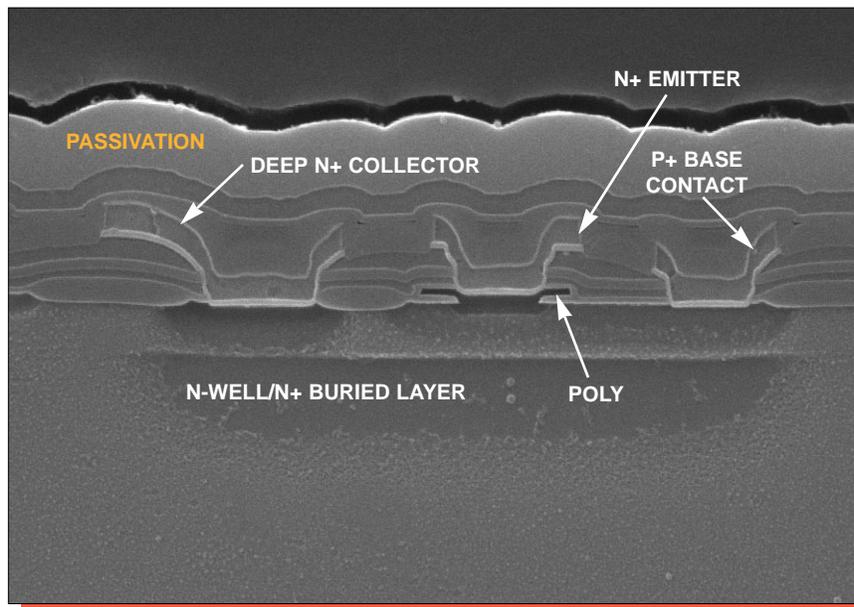
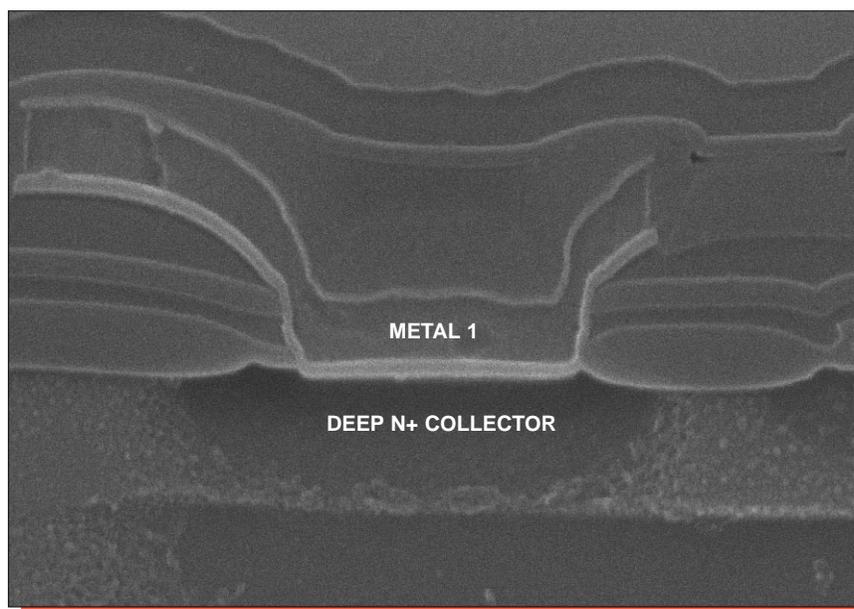


Figure 23a. Perspective SEM view of a bipolar device. Unlayered, Mag. 8000x, 60°.

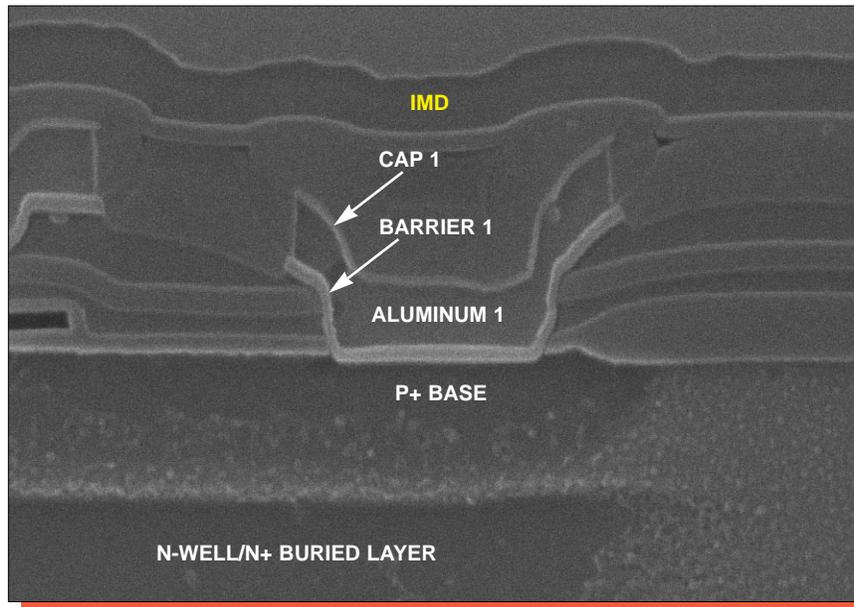


Mag. 10,000x

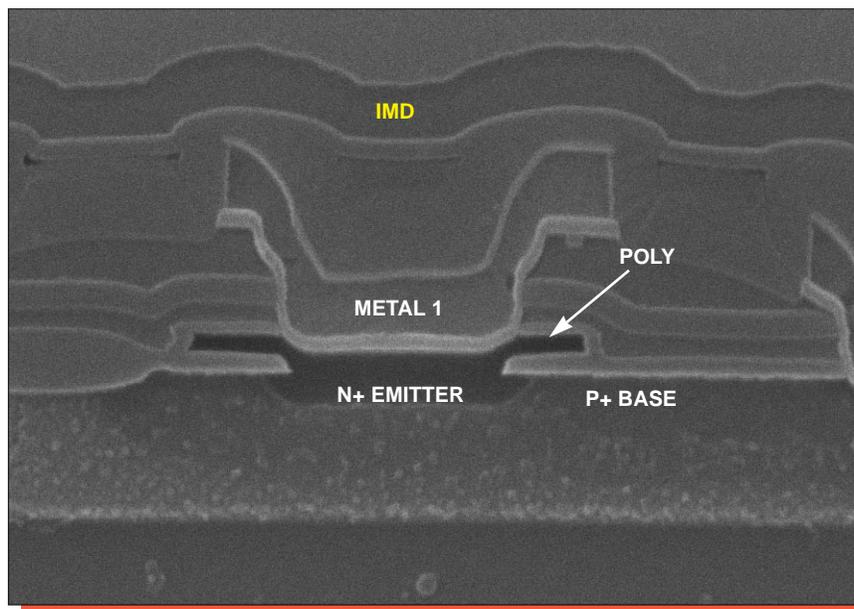


N+ collector, Mag. 26,000x

Figure 24. SEM section views of a NPN bipolar device.



P+ base



N+ emitter

Figure 25. SEM section views of a NPN bipolar device. Mag. 26,000x.

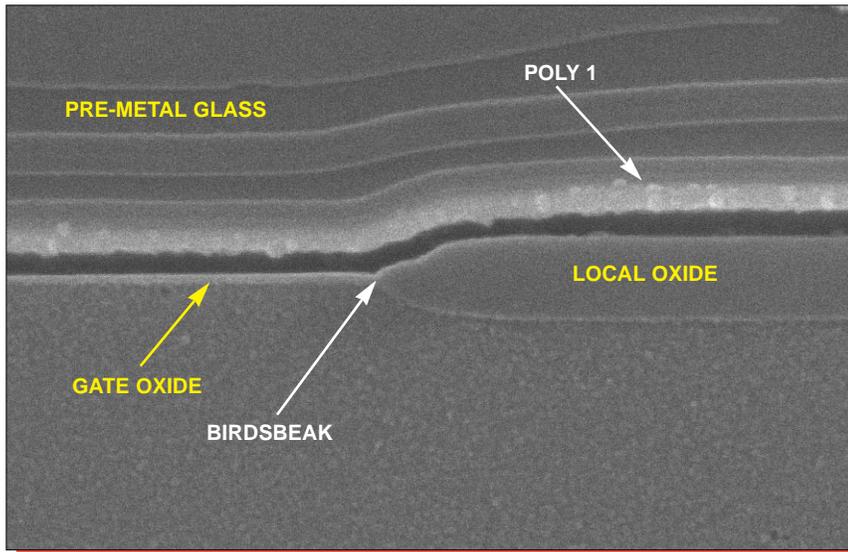
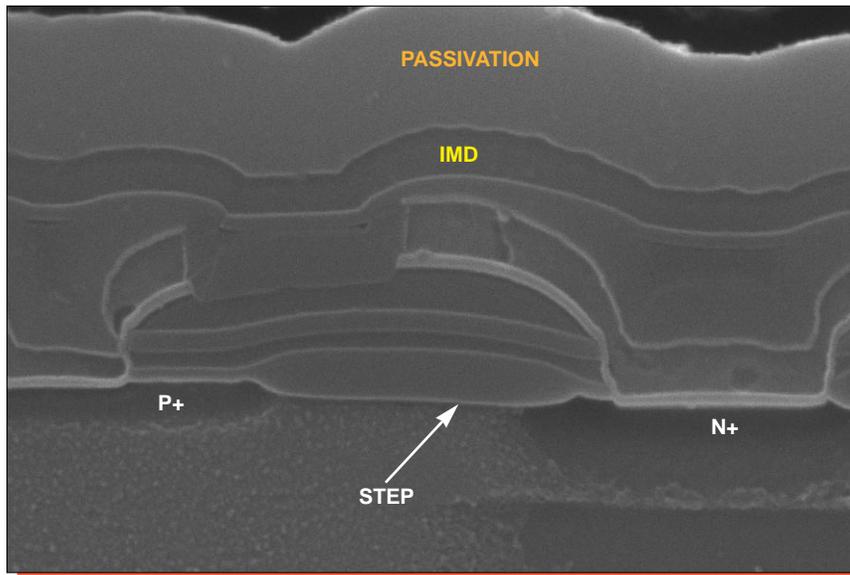
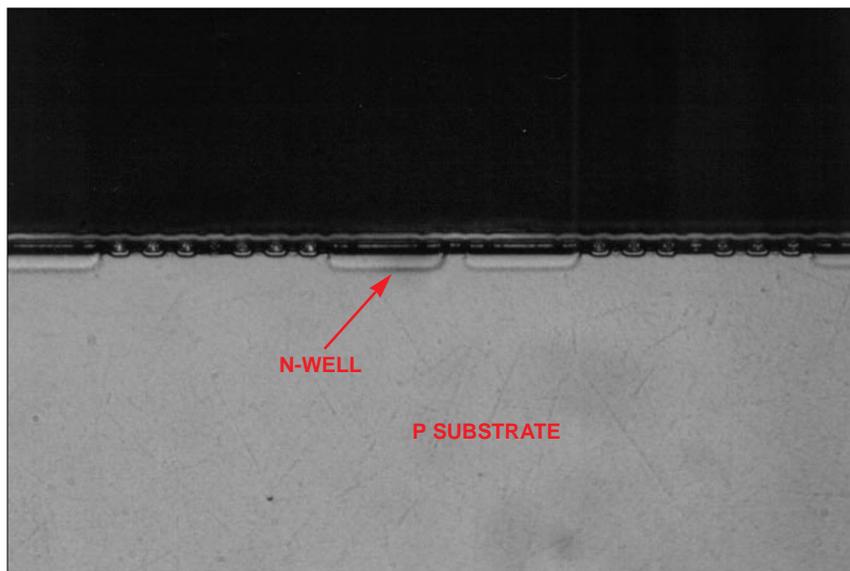


Figure 26. SEM section view of a local oxide birdsbeak. Mag. 40,000x.

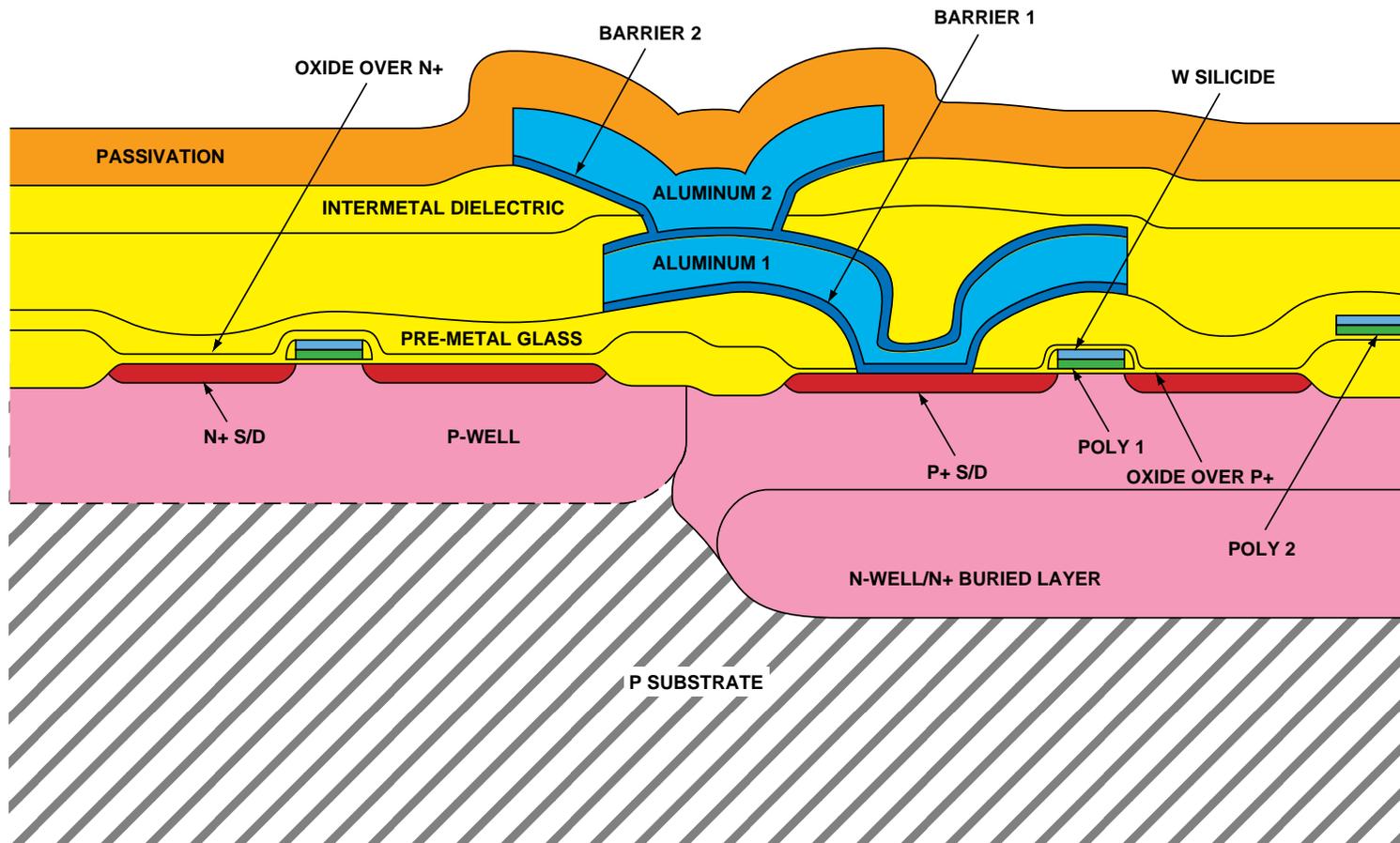


Mag. 20,000x



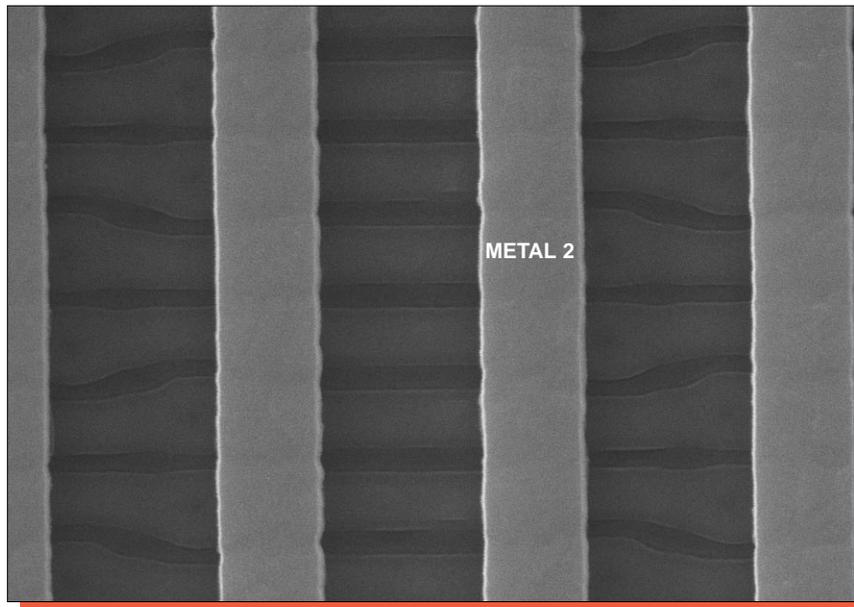
Mag. 1000x

Figure 26a. SEM and optical views of the well structure.

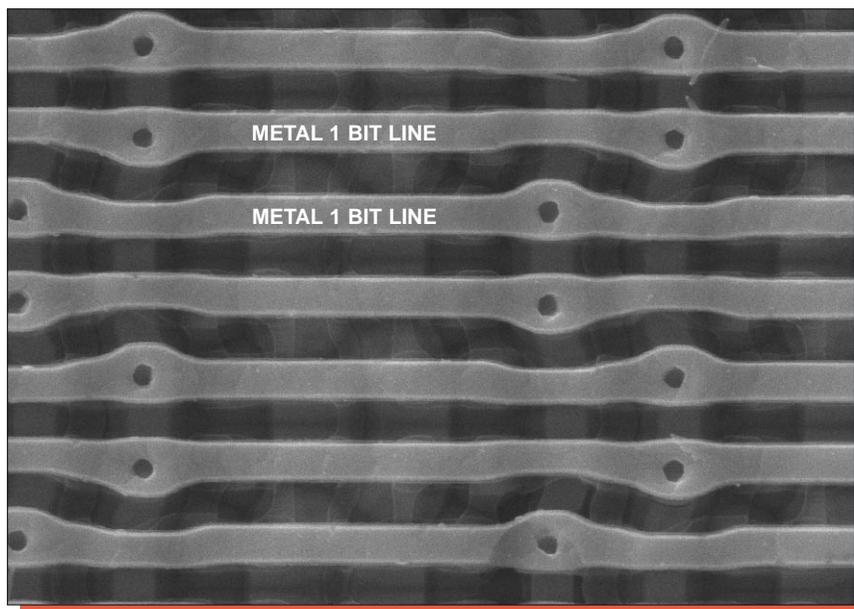


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
 Red = Diffusion, and Gray = Substrate

Figure 26b. Color cross section drawing illustrating device structure.

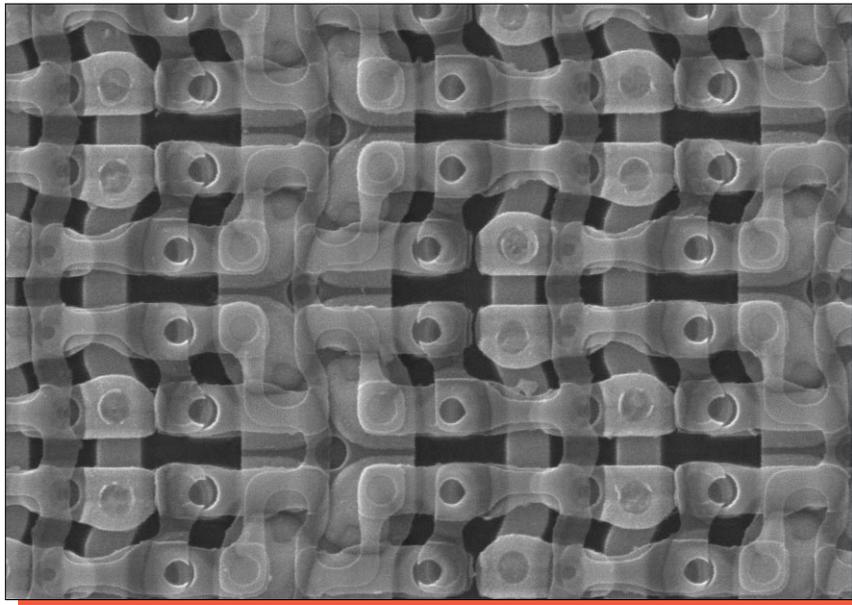


metal 2

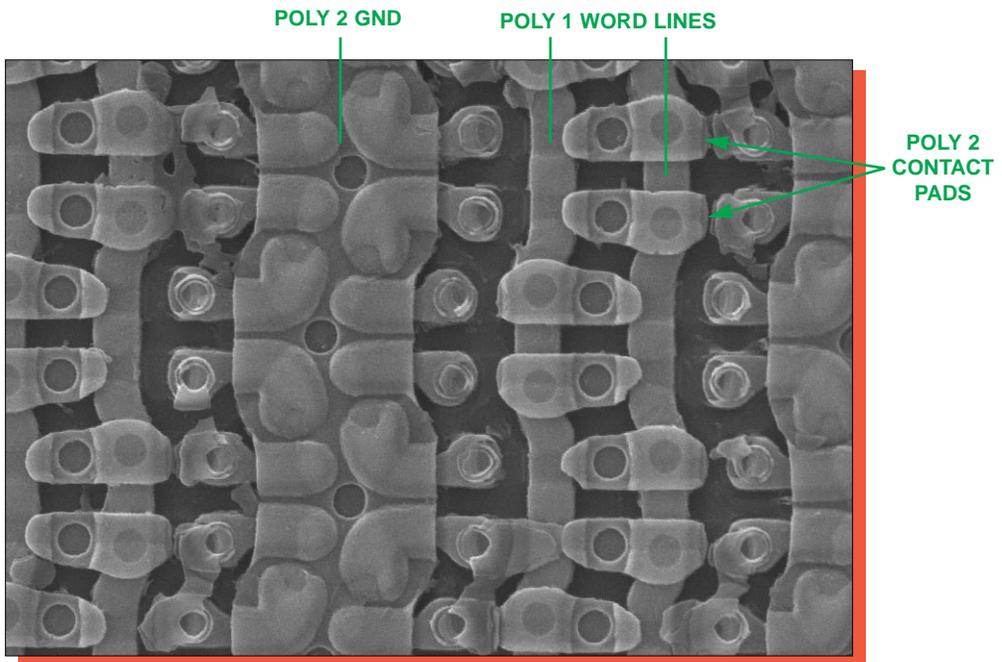


metal 1

Figure 27. Topological SEM views of the SRAM cell array. Mag. 6500x, 0°.

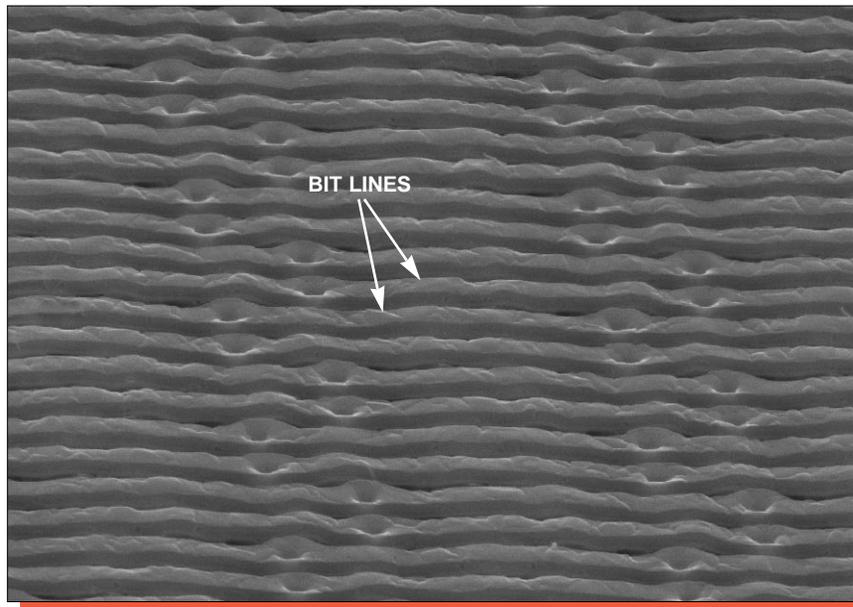


poly 1-poly 4

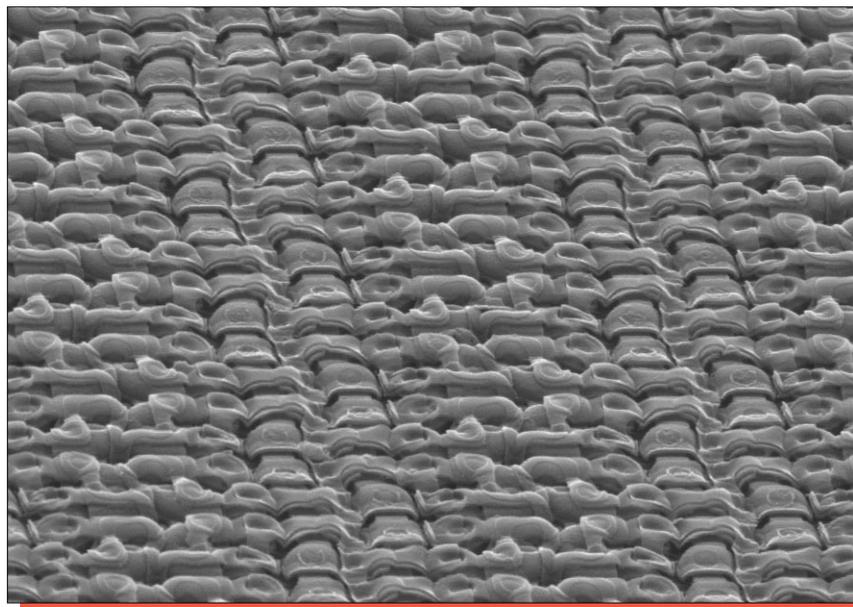


poly 1 and poly 2

Figure 27a. Topological SEM views of the SRAM cell array. Mag. 6500x.

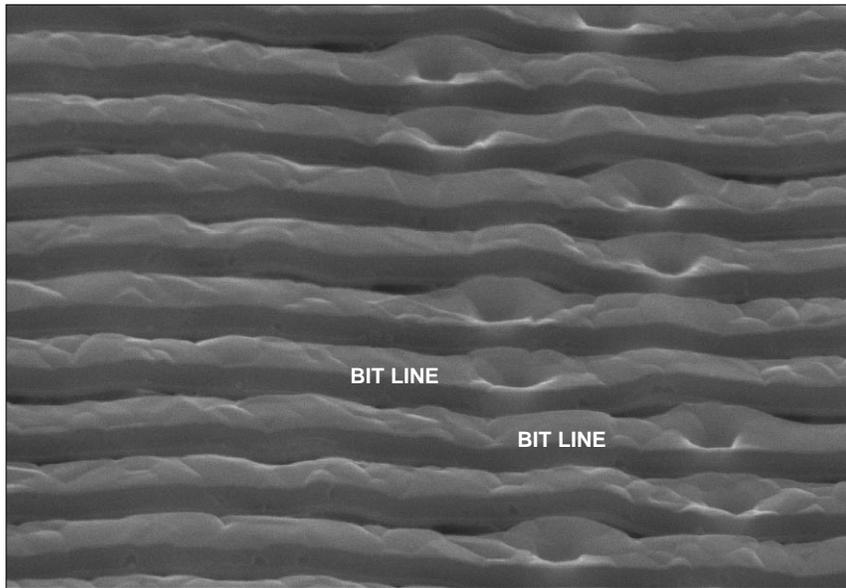


metal 1

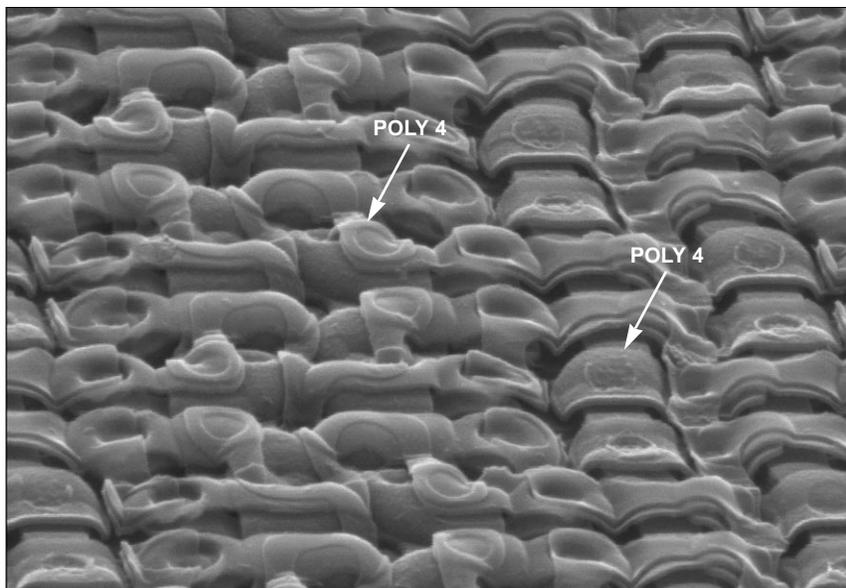


unlayered

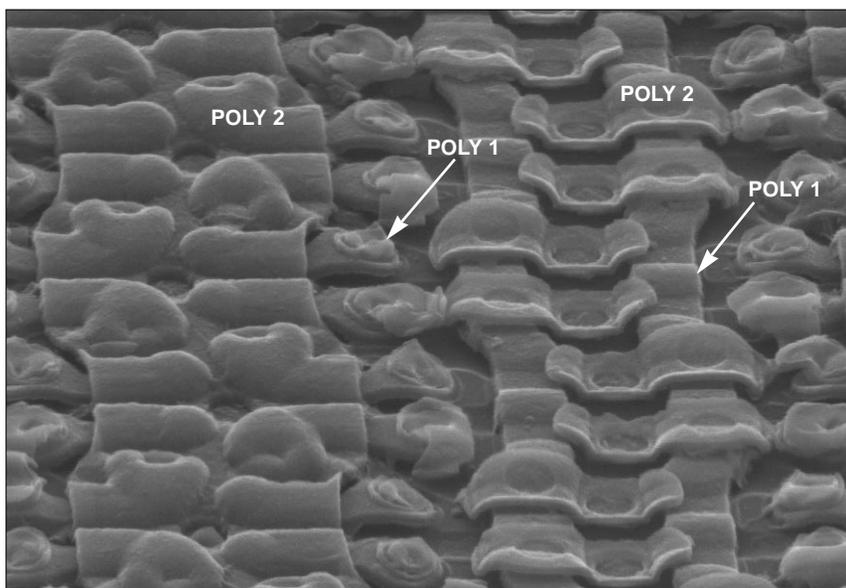
Figure 28. Perspective SEM views of the SRAM cell array. Mag. 5000x, 60°.



metal 1

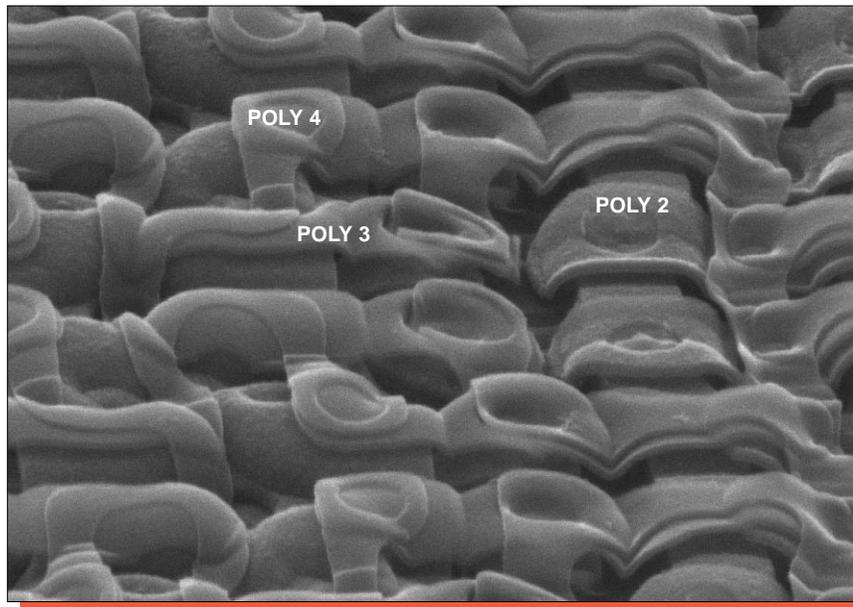


poly 3 and poly 4

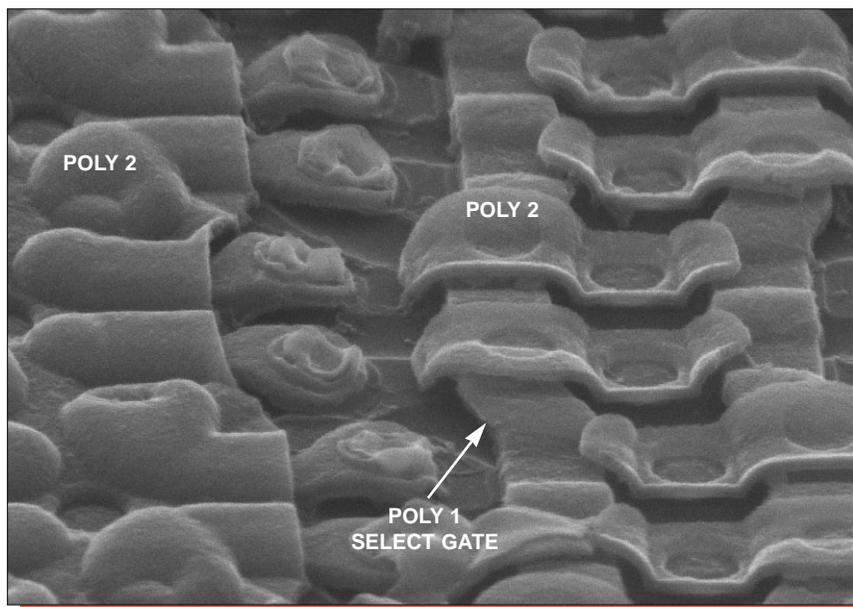


poly 1 and poly 2

Figure 28a. Additional perspective SEM views of the SRAM cell array.
Mag. 10,000x, 60°.

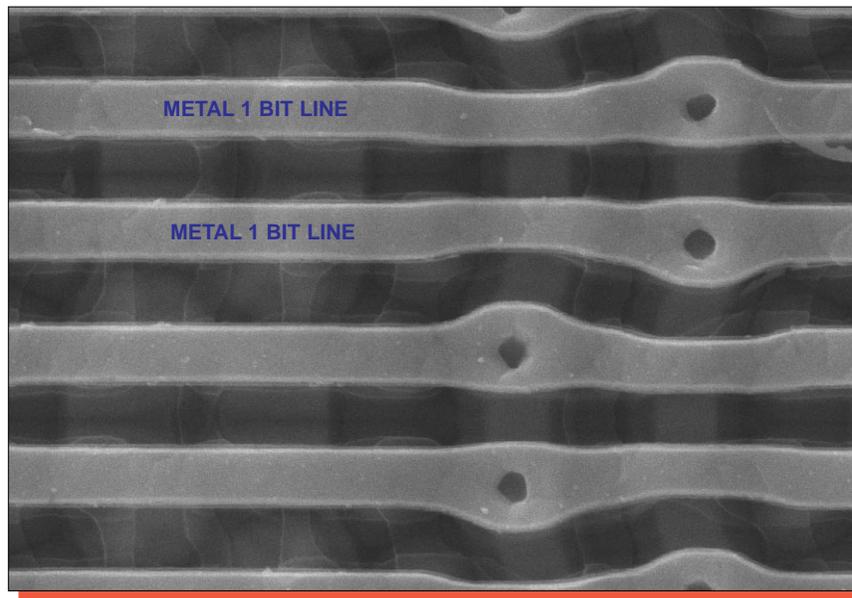


poly 3 and 4

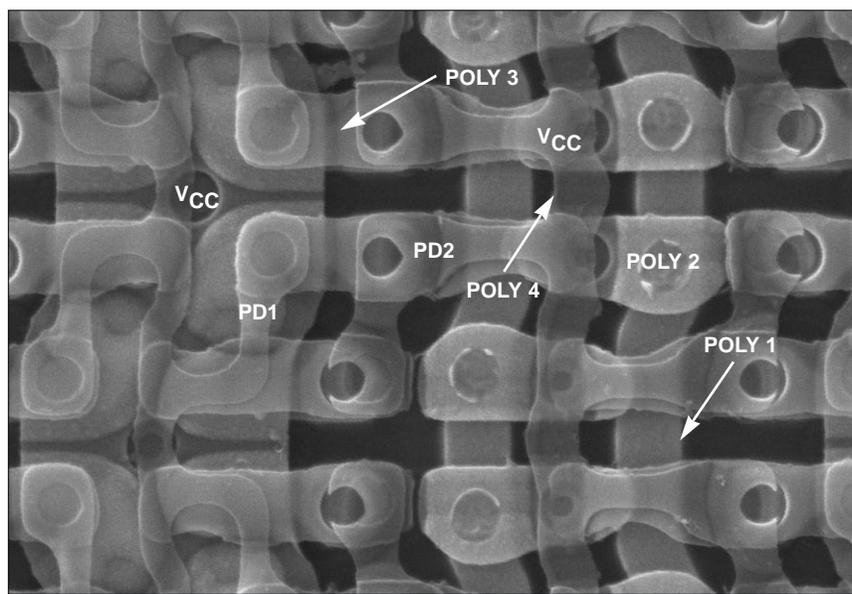


poly 1 and 2

Figure 29. Detailed perspective SEM views of the SRAM cell. Mag. 16,000x, 60°.

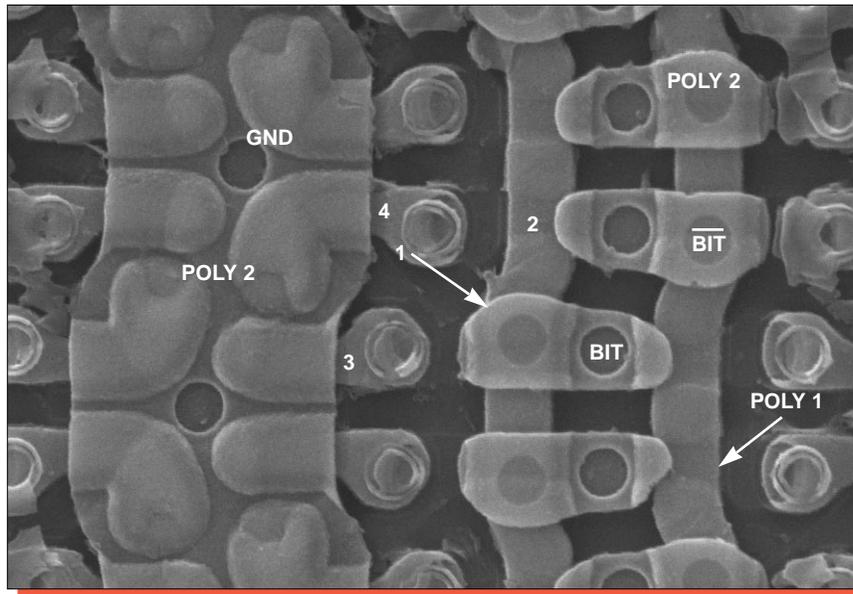


metal 1



poly 1 - poly 4

Figure 30. Detailed topological SEM views of the SRAM cell array. Mag. 10,000x, 0°.



poly 1 and poly 2

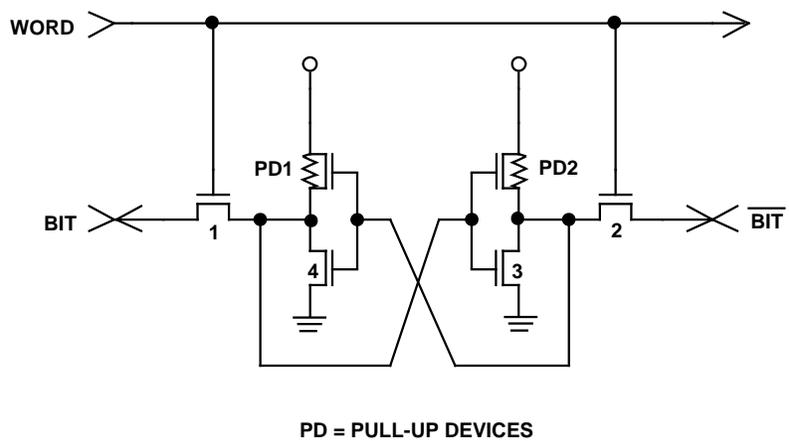
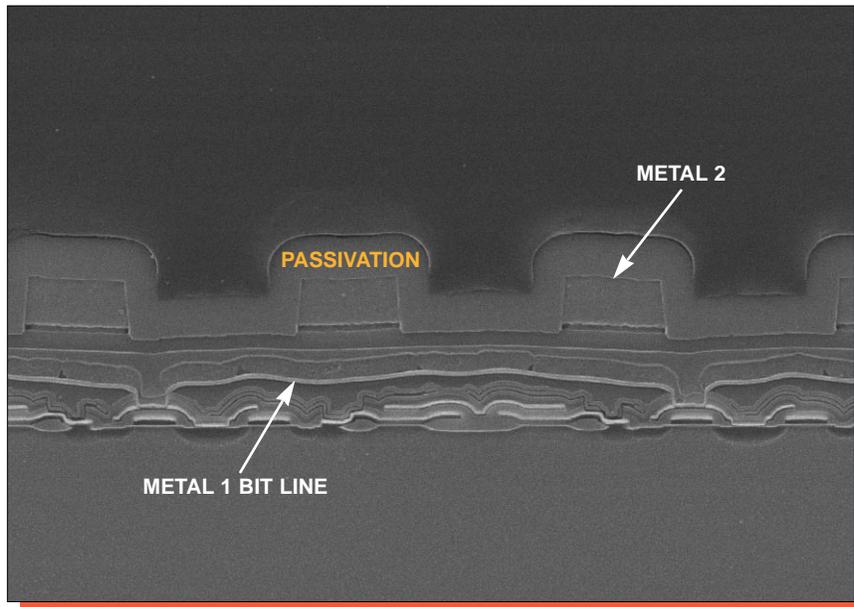
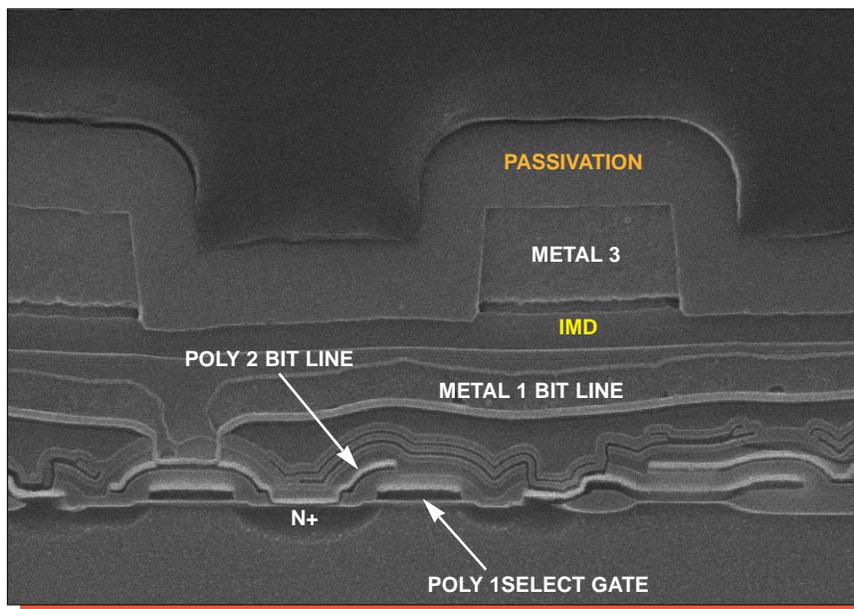


Figure 30a. Detailed topological SEM view and schematic of the SRAM cell.
Mag. 10,000x, 0°.

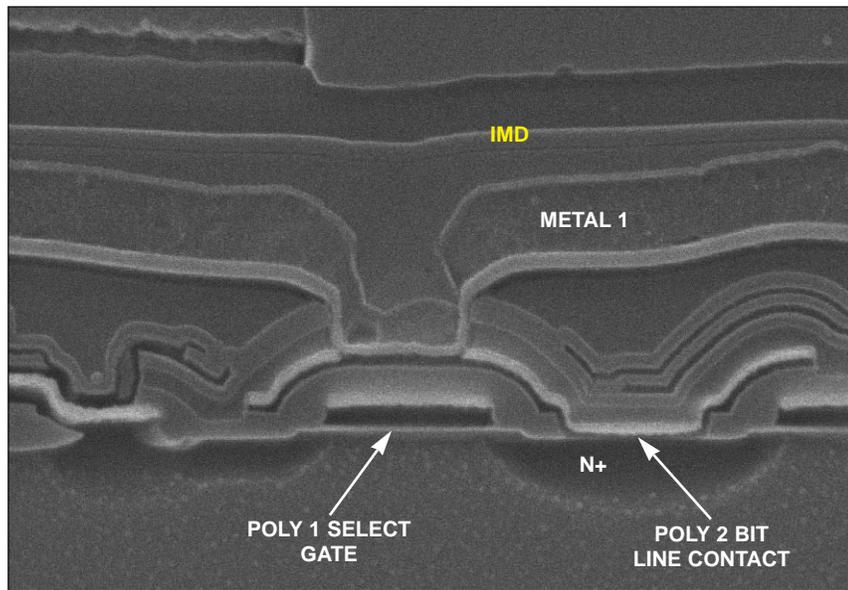


Mag. 6500x

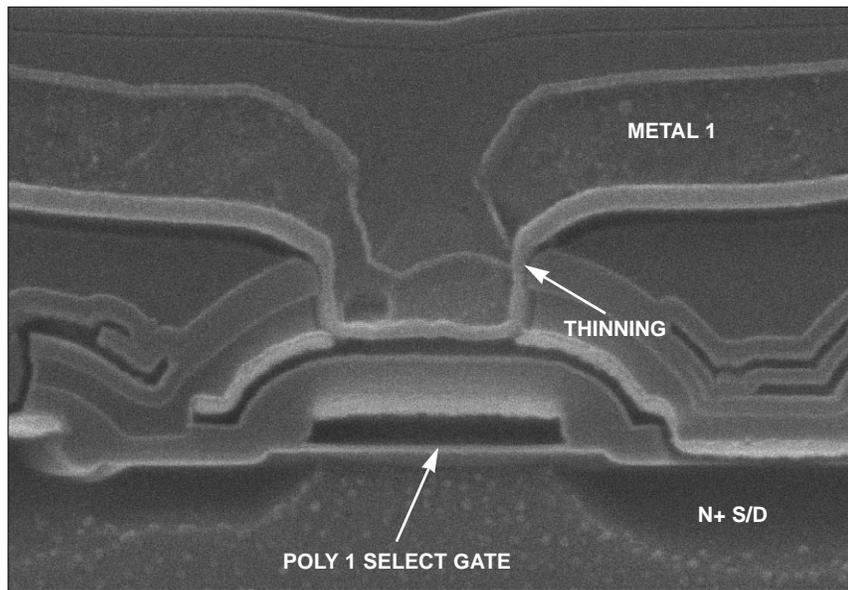


Mag. 13,000x

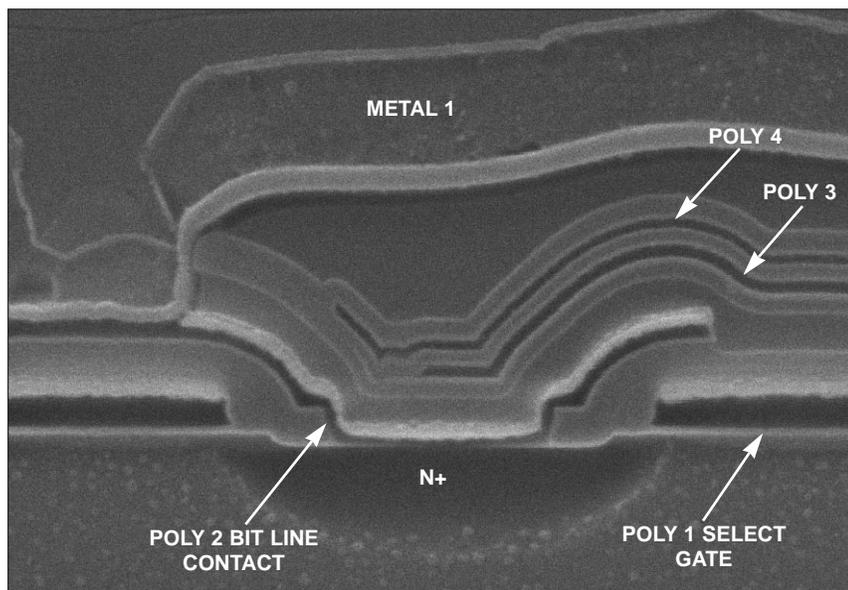
Figure 31. SEM section views of the SRAM cell array.



Mag. 26,000x

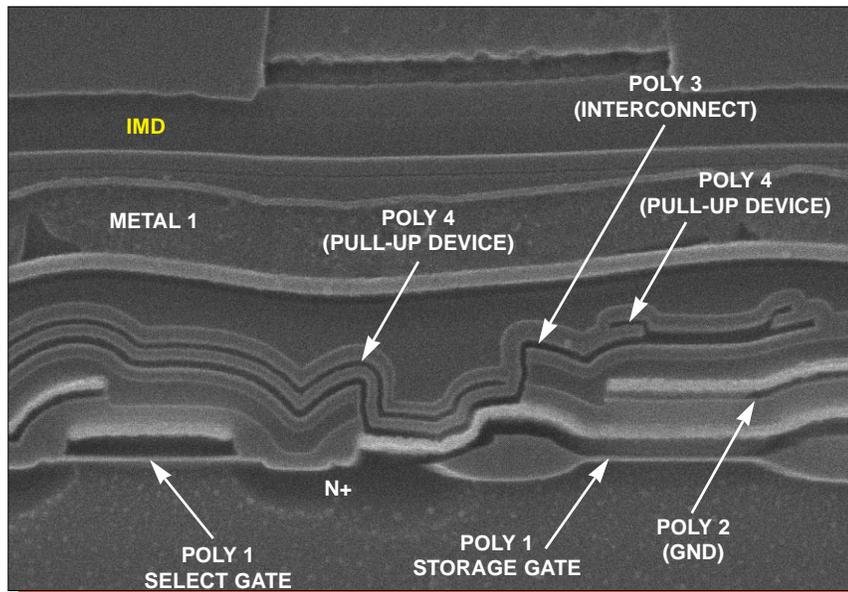


Mag. 40,000x

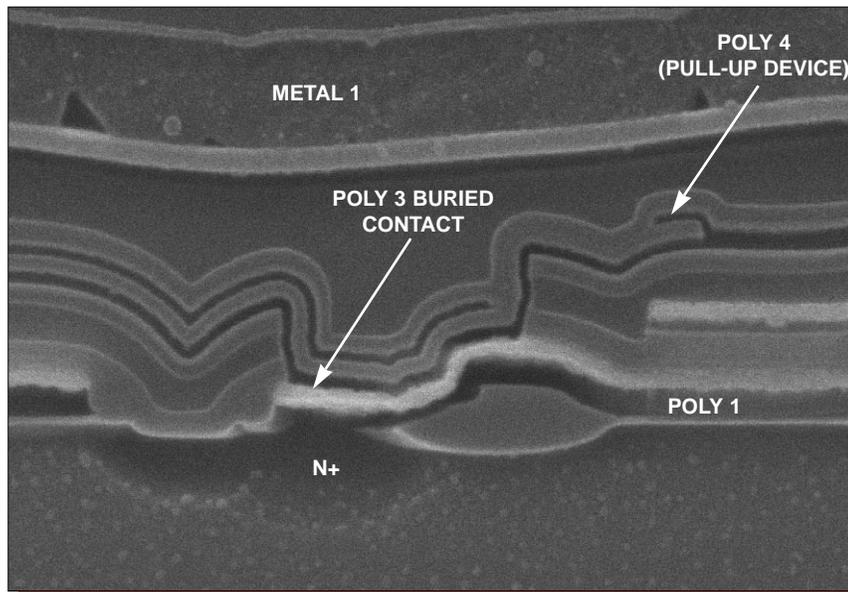


Mag. 40,000x

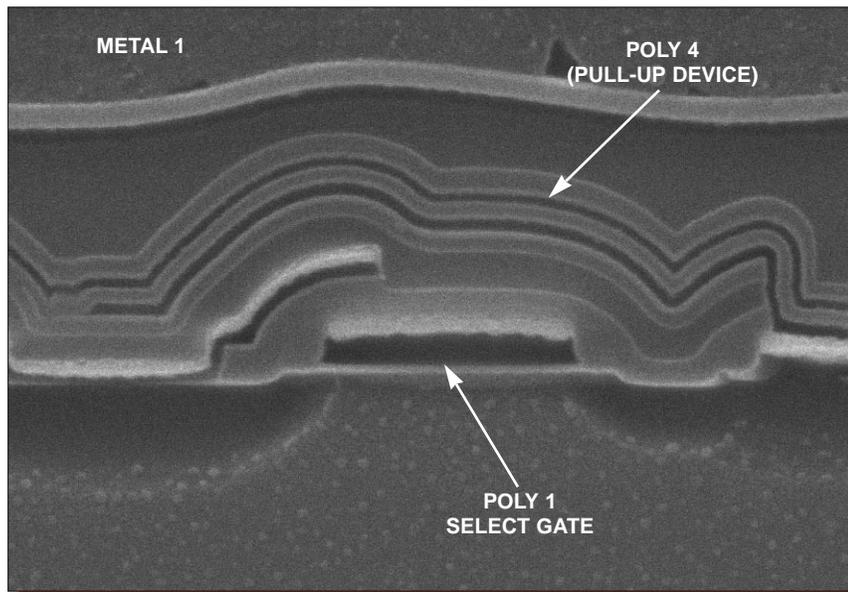
Figure 32. SEM section views of the SRAM bit line structure.



Mag. 26,000x



Mag. 40,000x



Mag. 40,000x

Figure 33. SEM section views of the SRAM cell.

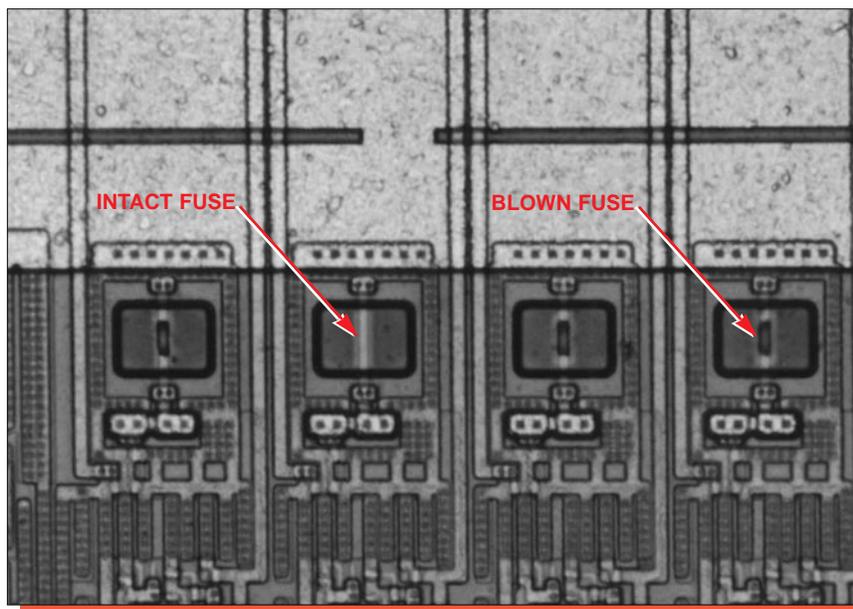
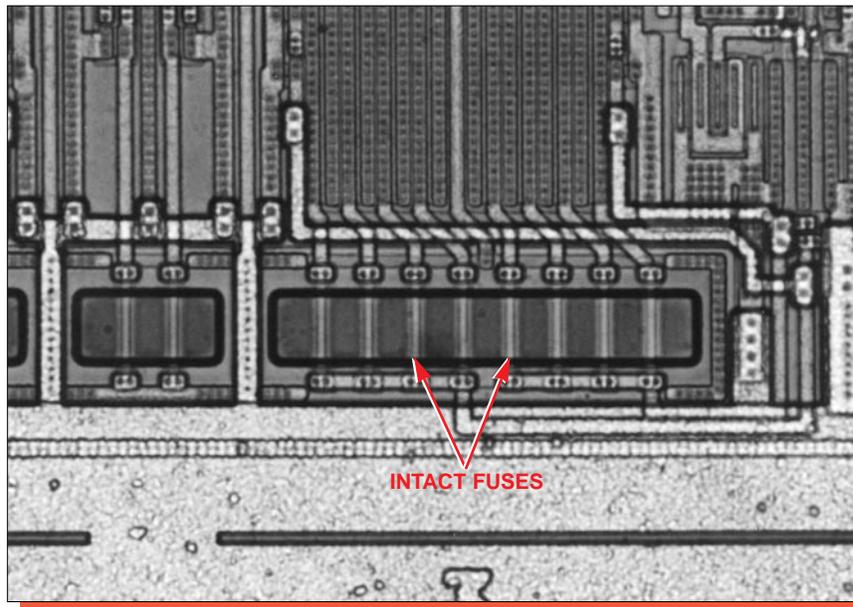
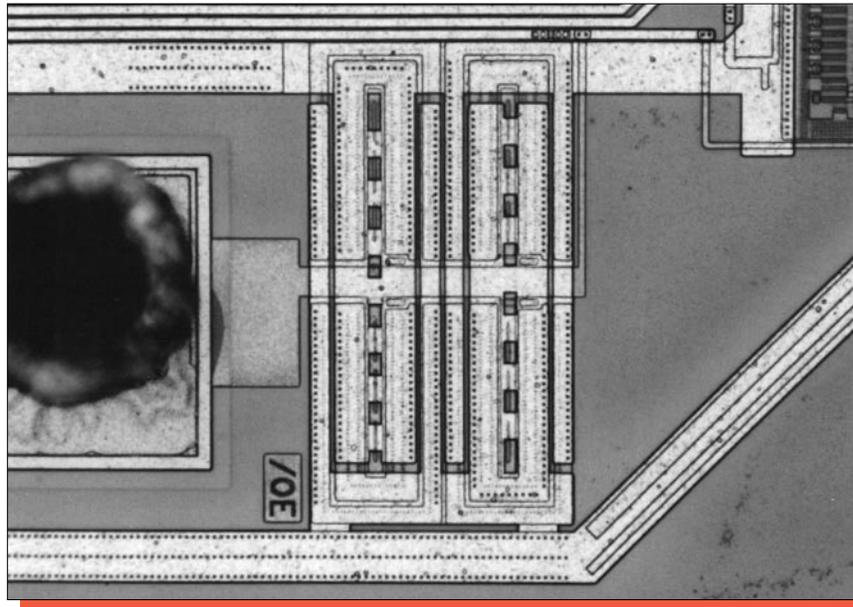
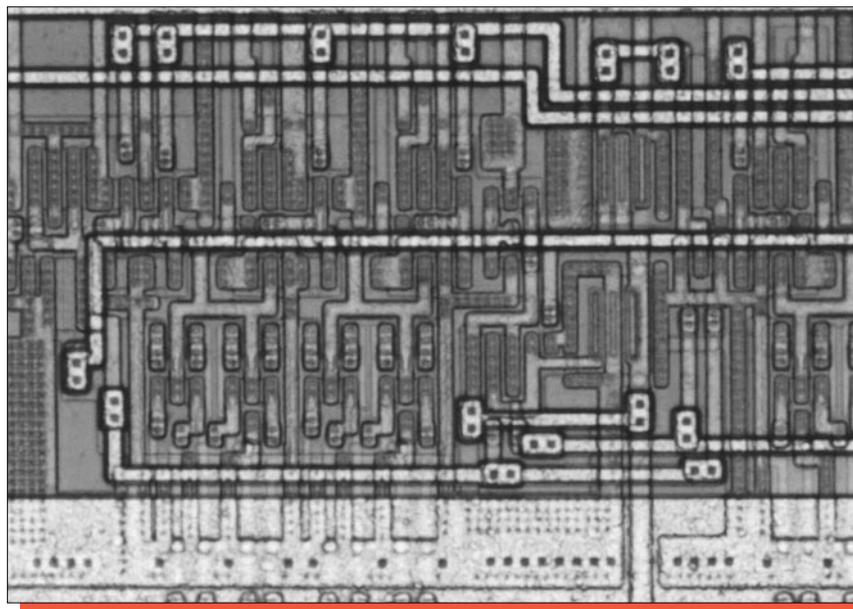


Figure 34. Optical views of typical fuses. Mag. 800x.



Mag. 320x



Mag. 800x

Figure 35. Optical views of typical input structure and general circuitry.