Construction Analysis

Lattice ispLSI1032E CPLD

Report Number: SCA 9612-522

INTEGRATED CIRCUIT ENGINEERING

15022 N. 75th Street
Scottsdale, AZ 85260-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: http://www.ice-corp.com/ice

INDEX TO TEXT

INTRODUCTION

This report describes a construction analysis of the new 6000 gate, 128 Macrocell Lattice ISPLSI1032E CPLD. One decapsulated device was received for the analysis. It was date coded 9628.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Twin-well CMOS process in a P substrate (no epi).
- Sub-micron gate lengths (0.55 micron N- and 0.65 micron P-channel).
- Standard contacts and vias (no plugs).
- Single poly EEPROM cells using tunnel-oxide windows.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- Device was packaged in a Plastic Leaded Chip Carrier (PLCC) for surface mount applications.

- The leadframe was constructed of copper and plated externally with tin-lead solder and internally with silver.

- Die separation was by sawing (full depth). Silver-filled epoxy was used to attach the die to the paddle.

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

- No die coat was present.

- Passivation consisted of a layer of nitride over a layer of glass.

- Metallization consisted of two layers of metal. Both metal layers consisted of aluminum with titanium-nitride caps and barriers. Standard contacts and vias were used at both levels (no plugs).

- Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing glass (probably SOG) layer in between.

- Pre-metal dielectric consisted of a layer of reflow glass (probably BPSG) over various densified oxides. The glass was reflowed prior to contact cuts only.

TECHNOLOGY DESCRIPTION (continued)

- A single layer of polycide (tungsten silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A step was present at the edge of the well indicating a twin-well process was used.

- Three different variations of EPROM cells were present on the die. Programming is achieved through an ultra-thin tunnel oxide window.

- Redundancy fuses were not present.

ANALYSIS RESULTS I

Package and Assembly: **Figures 1 - 4**

Questionable Items:[1] None.

General Items:

- Devices were packaged in a Plastic Leaded Chip Carrier (PLCC) for surface mount applications.

- Overall package quality: Good. No significant defects were noted in the external or internal portions of the package. No cracks or voids were noted in the package.

- Leadframe: The leadframe was apparently constructed of copper (Cu) and plated externally with tin-lead (Sn-Pb) solder and internally plated with silver (Ag). No voids or cracks were noted at lead exits.

- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present. A silver-filled epoxy was used to attach the die to the header.

- Wirebonding: Thermosonic ball bond method using gold wire. No problems are foreseen.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

Die Process: **Figures 5 - 33**

Questionable Items:[1] None.

Special Features:

- Twin-well CMOS process in a P substrate (no epi).
- Sub-micron gate lengths (0.55 micron N- and 0.65 micron P-channel).
- Standard contacts and vias (no plugs).
- Three variations of EPROM cells on die.

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: A layer of nitride over a layer of glass. Overlay integrity test indicated defect-free passivation. Edge seal was good.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metallization: Two layers of metal. Both consisted of aluminum with titanium-nitride caps and barriers. Standard contacts and vias were used at all levels (no plugs were used).

- Metal patterning: Both metal layers were patterned by a dry etch of normal quality.

- Metal defects: No voiding, notching, or neckdown was noted in either of the metal layers. All contacts and vias were completely surrounded by metal. No silicon nodules were noted following the removal of either metal layer.

- Metal step coverage: Metal 2 aluminum thinning did not exceed 55 percent. Metal 1 aluminum thinning did not exceed 45 percent. The addition of the cap and barrier metals further reduced the thinning of both the metal layers.

- Interlevel dielectric consisted of two layers of silicon-dioxide with a planarizing glass (SOG) layer between. No problems were found in any of these layers.

- Pre-metal dielectric: A layer of reflow glass (probably BPSG) over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Via and contact cuts were defined by a two step process. No over-etching of the contacts or vias was noted.

- A single layer of polycide (poly and tungsten silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by dry-etch of normal quality.

<u>ANALYSIS RESULTS II</u> (continued)

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No problems were found.

- Local oxide (LOCOS) isolation was used. The step present at the well boundary indicates a twin-well process was employed.

- Three variations of EPROM cells were present on the die. Programming is achieved through ultra-thin tunnel oxide windows. No problems were discovered.

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

Internal optical inspection

SEM of passivation

Passivation integrity test

Passivation removal

Delayer to metal 2 and inspect

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity	N
Package markings	N/A
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	N
Metal registration	N
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

DIE MARKINGS

LATTICE (LOGO)
1994 PLSI
1032-02
LOW

DIE MATERIAL ANALYSIS

Overlay passivation:	A layer of nitride over a layer of glass.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Polycide:	Polysilicon with tungsten (W) silicide.

HORIZONTAL DIMENSIONS

Die size:	6.5 x 6.8 mm (258 x 269 mils)
Die area:	44.2 mm^2 (69,402 $mils^2$)
Min metal 2 width:	1.4 micron
Min metal 2 space:	1.2 micron
Min metal 2 pitch:	2.6 microns
Min via size:	1.1 micron
Min metal 1 width:	0.85 micron
Min metal 1 space:	1.3 micron
Min metal 1 pitch:	2.15 microns
Min contact size:	1.2 micron
Min poly width:	0.55 micron
Min poly space:	1.1 micron
Min contact to gate poly space:	0.6 micron
Min gate length* - (N-channel):	0.55 micron
- (P-channel):	0.65 micron
Tunnel oxide window:	1.3 micron (dia.)

*****_Physical gate length_

VERTICAL DIMENSIONS

Die thickness: 0.5 mm (19.5 mils)

Layers:

Passivation 2:	0.5 micron
Passivation 1:	0.25 micron
Metal 2 - cap:	0.08 micron (approximate)
- aluminum:	0.85 micron
- barrier:	0.15 micron
Interlevel dielectric - glass 2:	0.15 micron
- glass 1:	0.3 - 0.45 micron
Metal 1 - cap:	0.1 micron
- aluminum:	0.75 micron
- barrier:	0.2 micron
Pre-metal dielectric:	0.15 - 0.35 micron
Oxide on poly:	0.12 micron
Poly - silicide:	0.15 micron
- poly:	0.15 micron
Local oxide:	0.45 micron
N+ S/D:	0.15 micron
P + S/D:	0.2 micron
N-well:	5.5 microns (approximate)
P-well:	Could not delineate

INDEX TO FIGURES

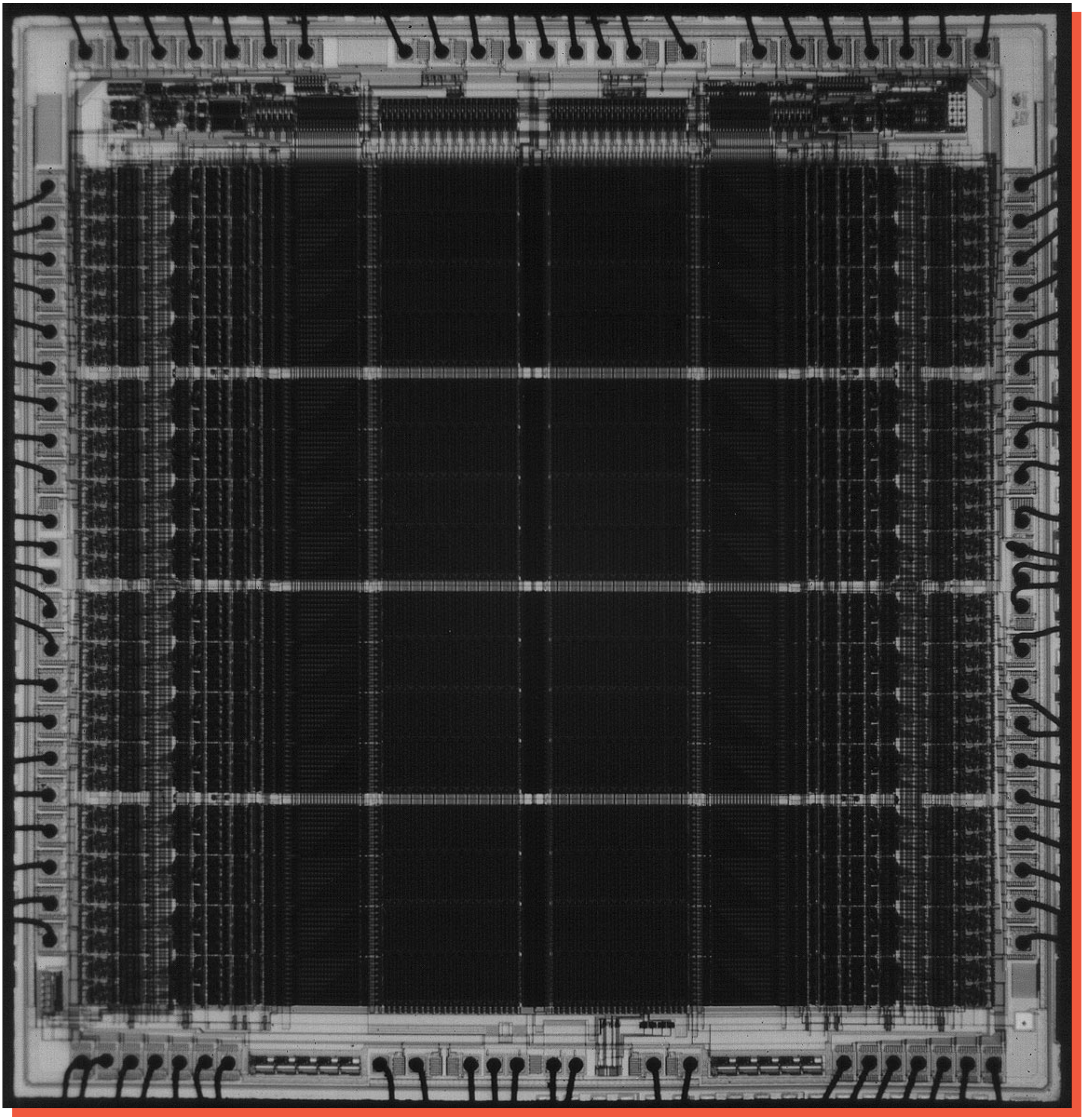
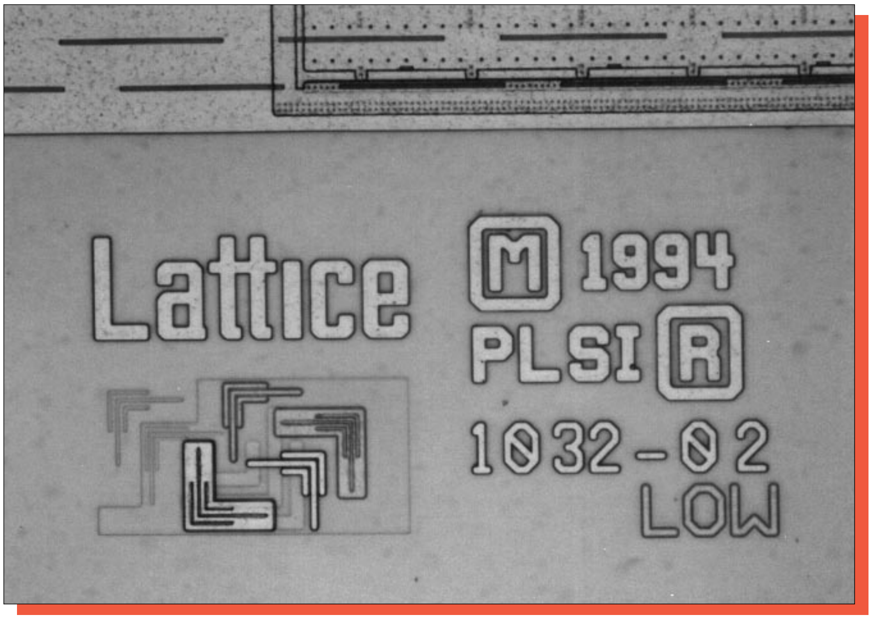


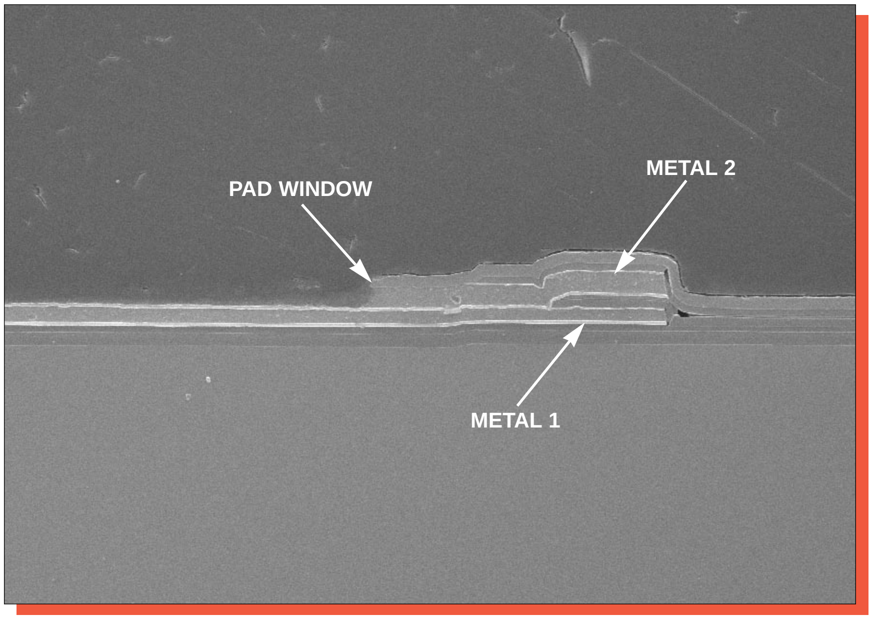
Figure 1. Whole die photograph of the Lattice ispLSI1032E CPLD. Mag. 29x.



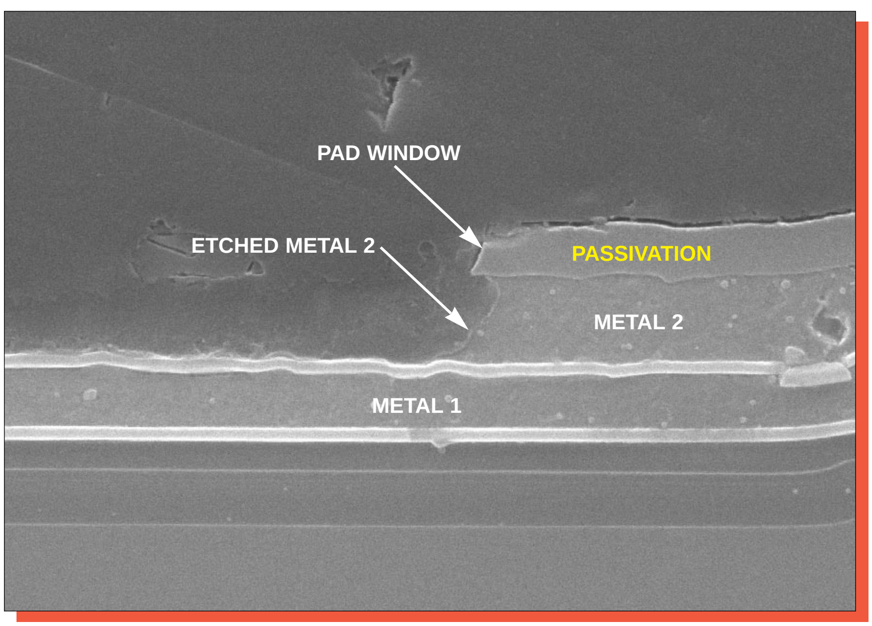
Mag. 400x

Mag. 800x

Figure 2. Markings from the die surface.

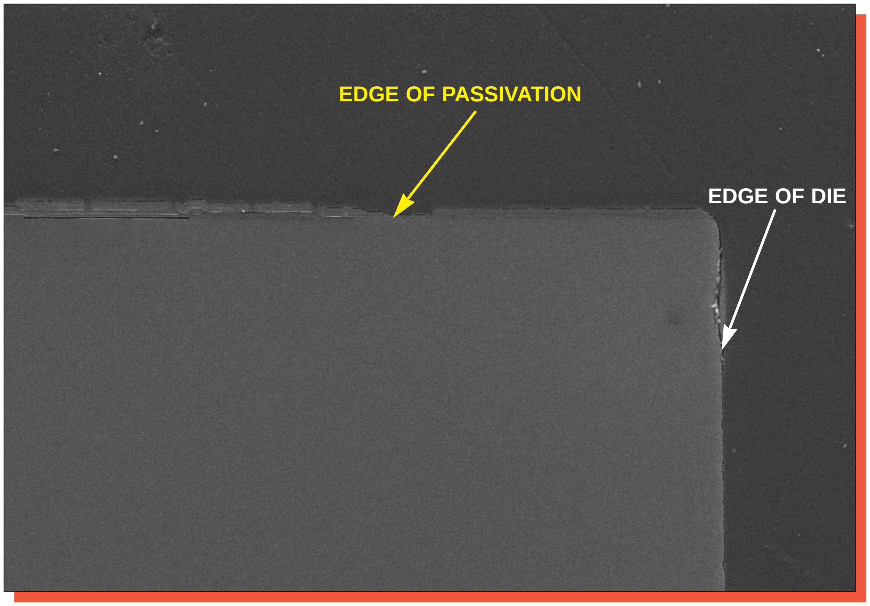


Mag. 3100x

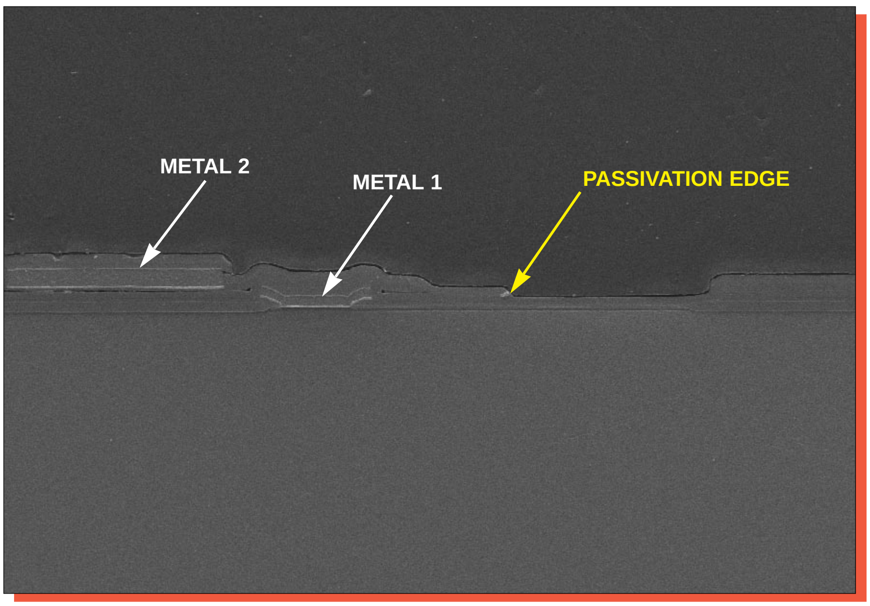


Mag. 13,000x

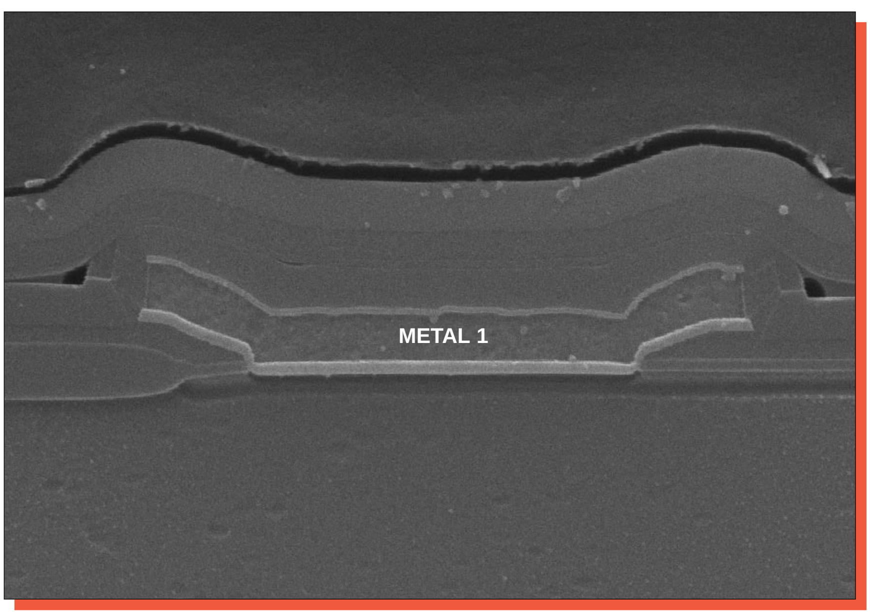
Figure 3. SEM section views of the bond pad structure.



Mag. 6200x

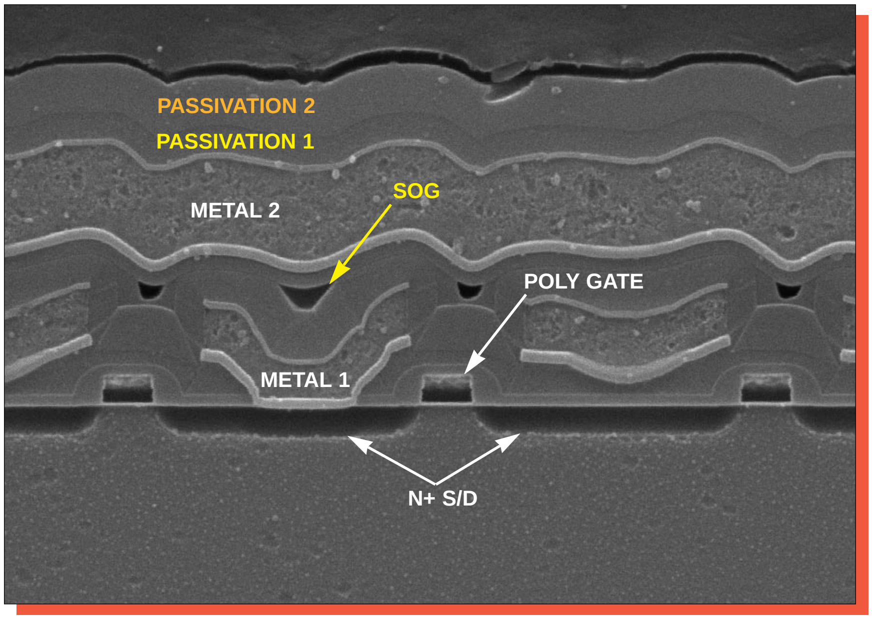


Mag. 2500x

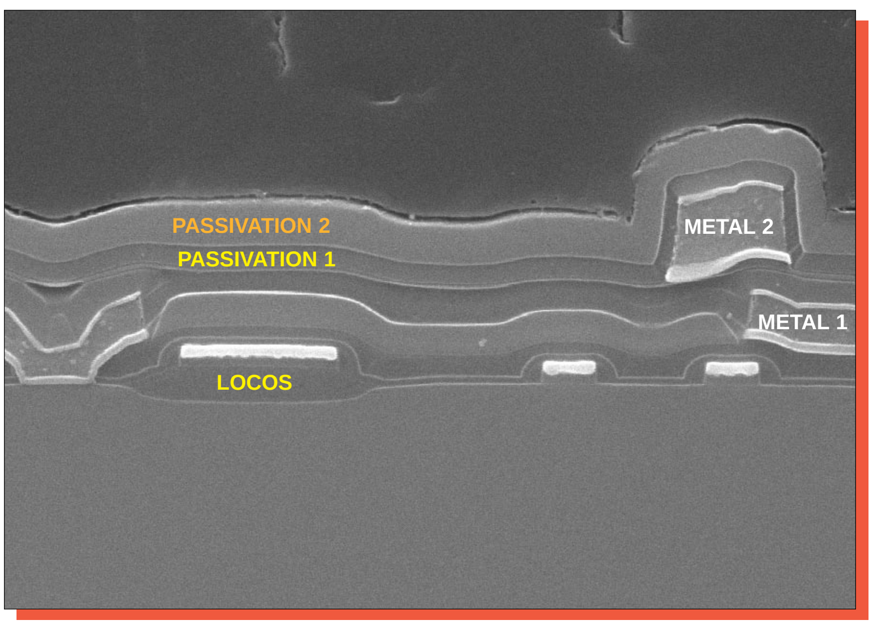


Mag. 13,000x

Figure 4. SEM section views of the edge seal.

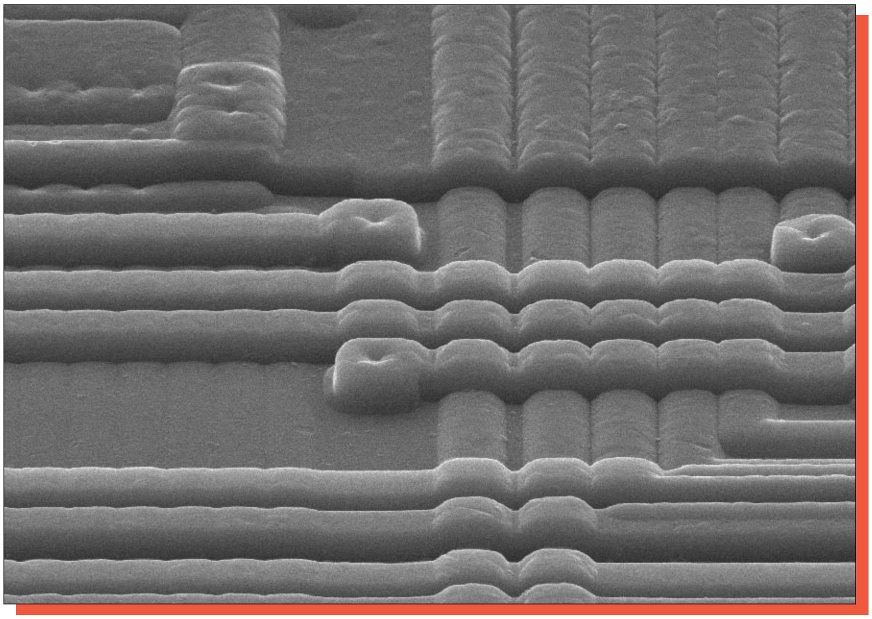


silicon etch, Mag. 13,000x

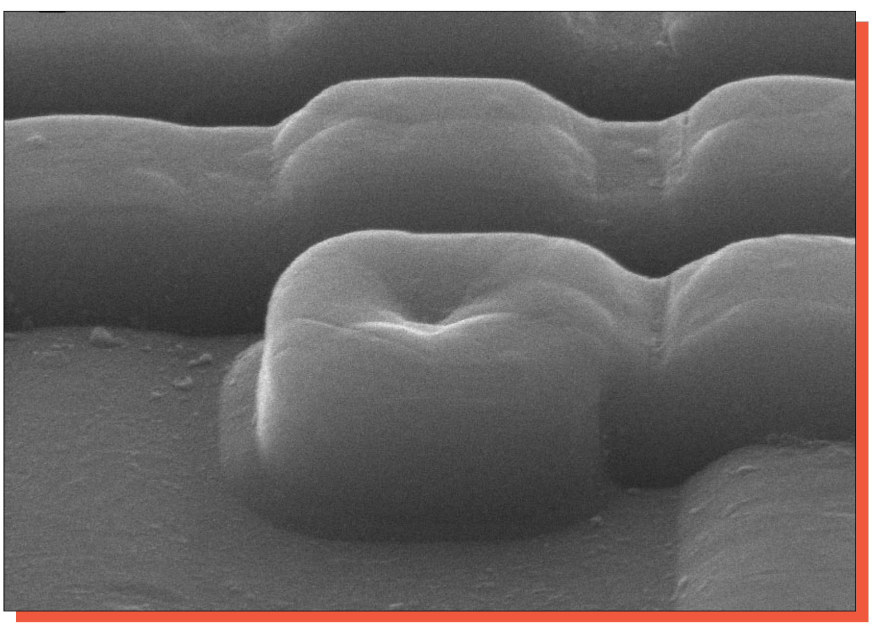


glass etch, Mag. 10,000x

Figure 5. SEM section views of general device construction.

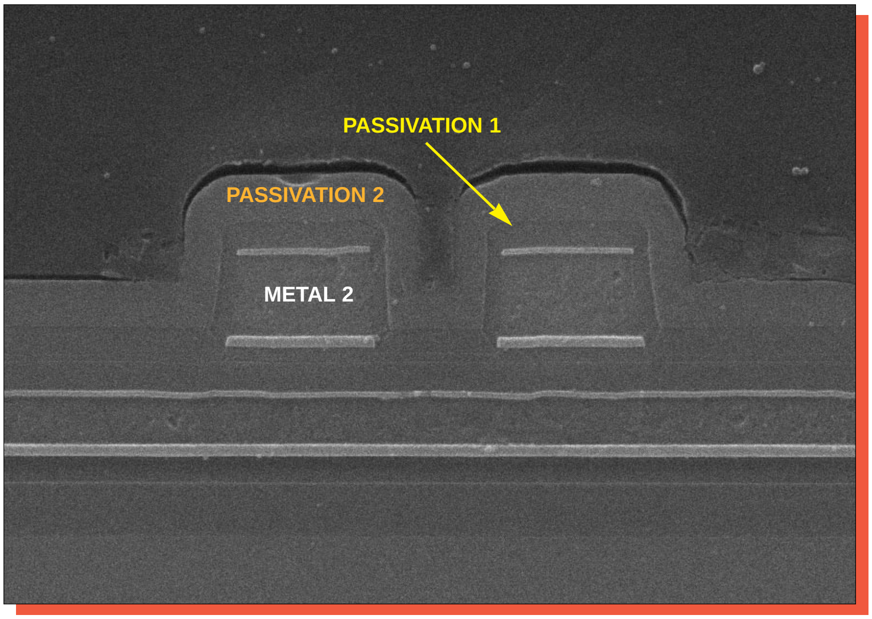


Mag. 3400x

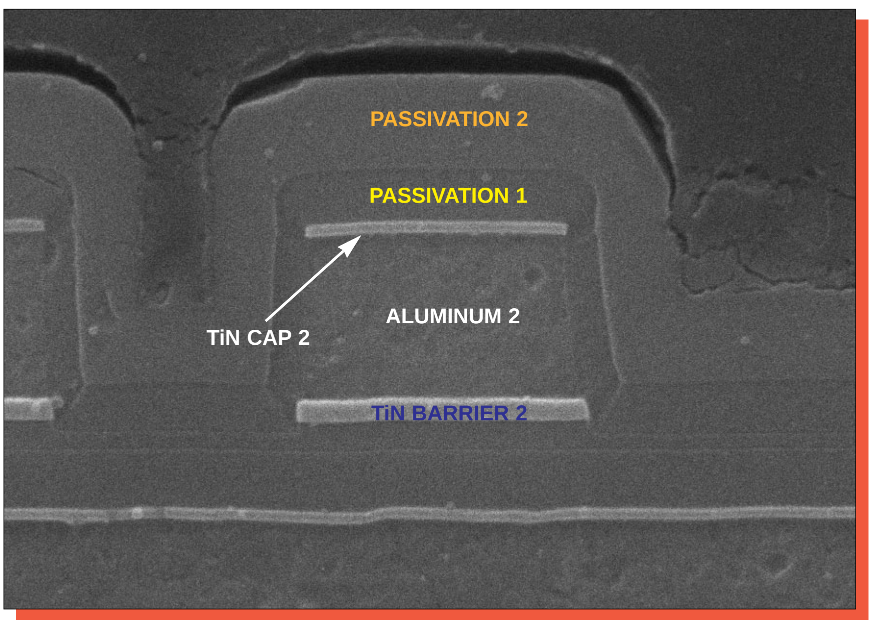


Mag. 13,500x

Figure 6. Perspective SEM views illustrating passivation coverage. 60°.

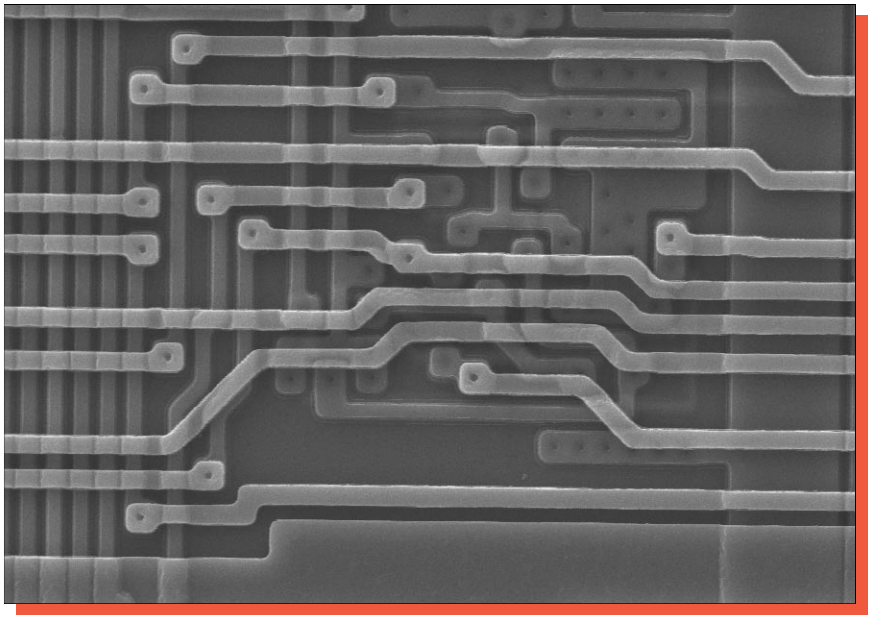


Mag. 13,000x

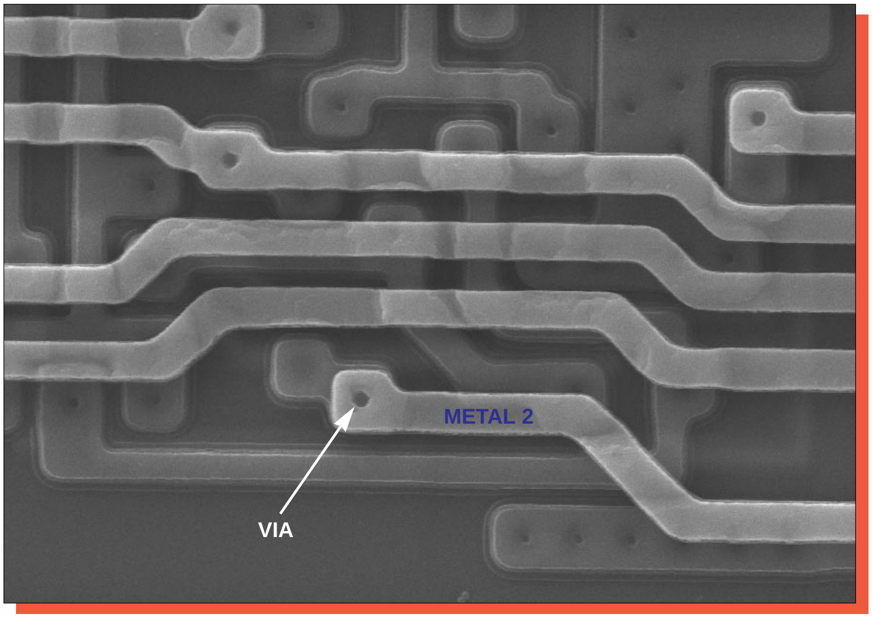


Mag. 26,000x

Figure 7. SEM section views of metal 2 line profiles.

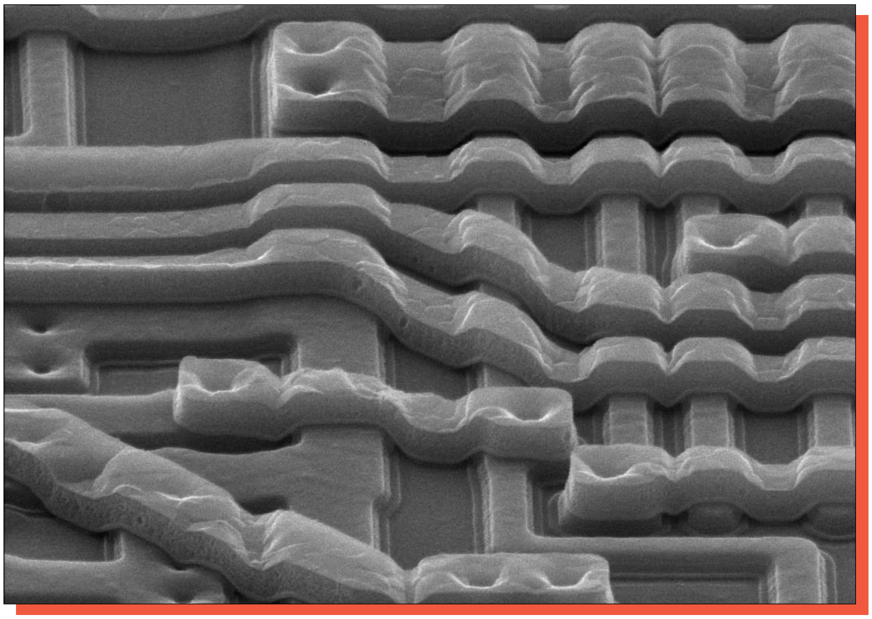


Mag. 1600x

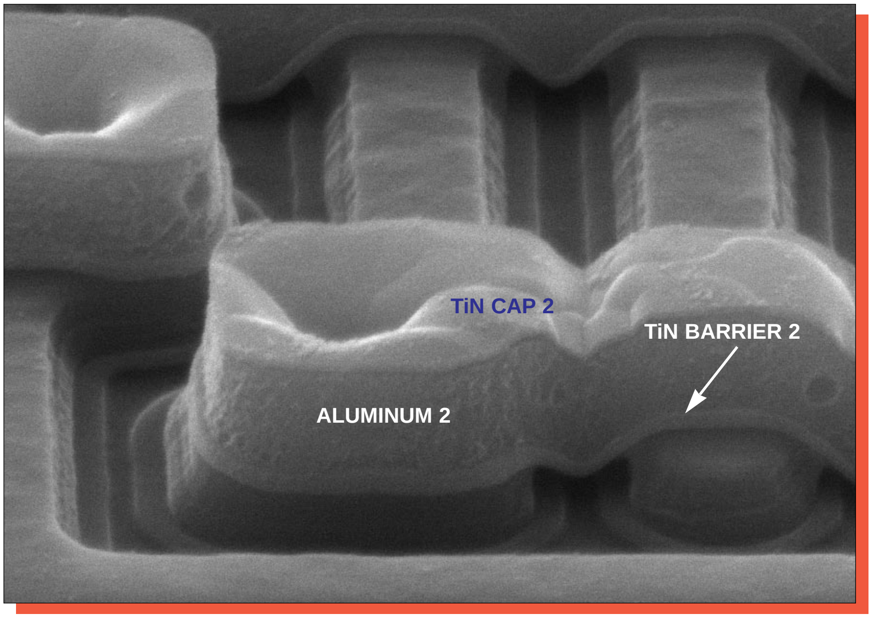


Mag. 3200x

Figure 8. Topological SEM views of metal 2 patterning. 0°.

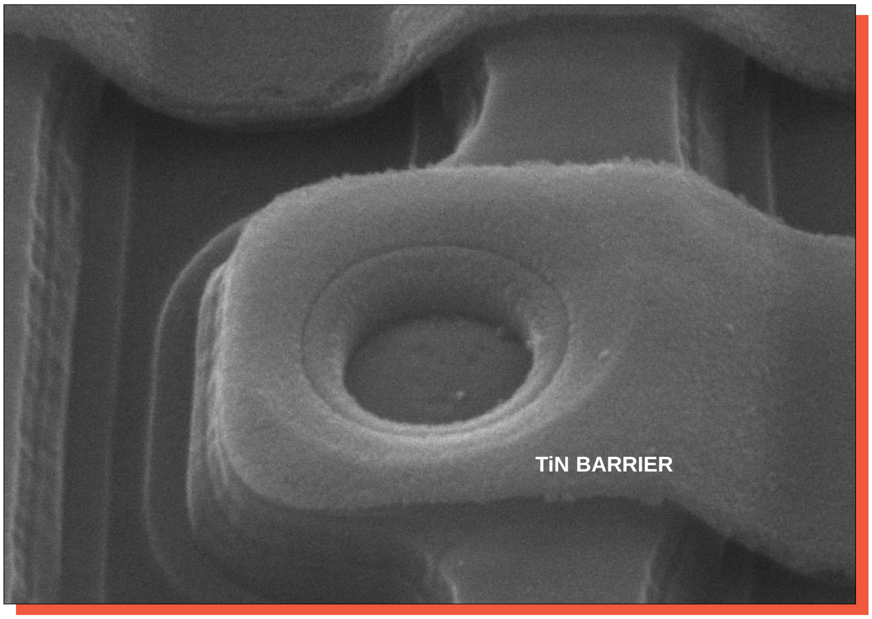


Mag. 4000x

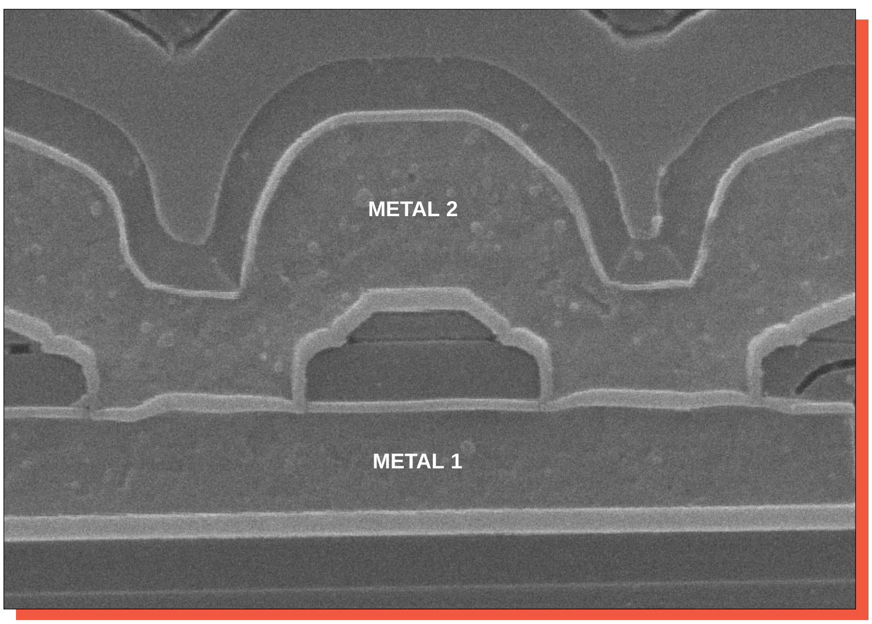


Mag. 15,000x

Figure 9. SEM views illustrating metal 2 coverage. 60°.

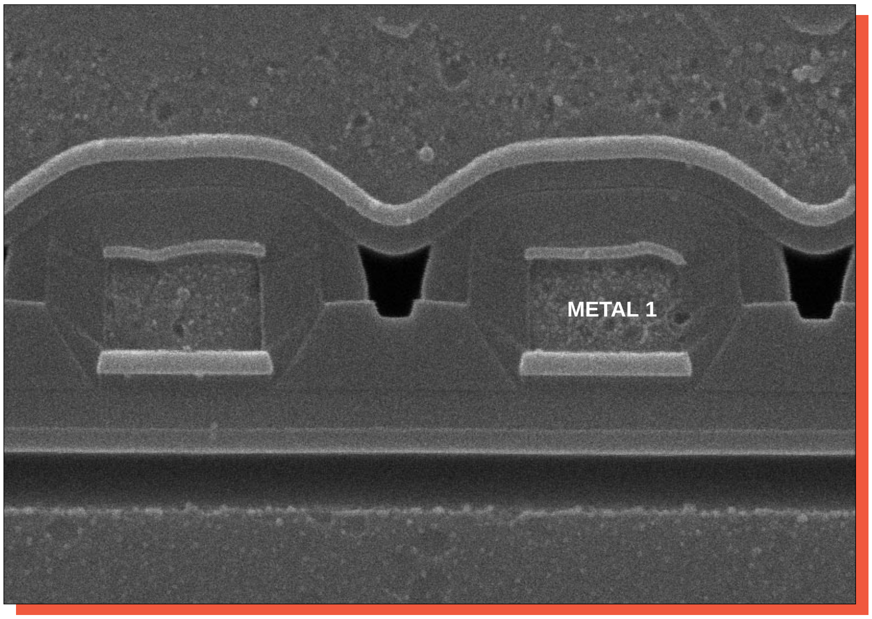


Mag. 24,000x, 45°

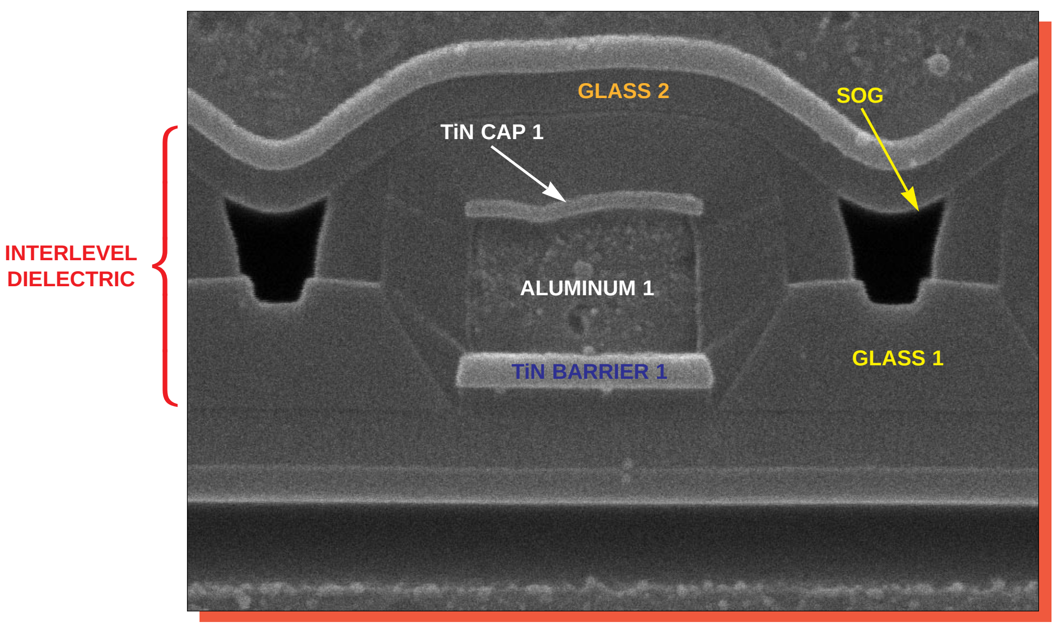


Mag. 26,000x

Figure 10. SEM views of metal 2-to-metal 1 vias.

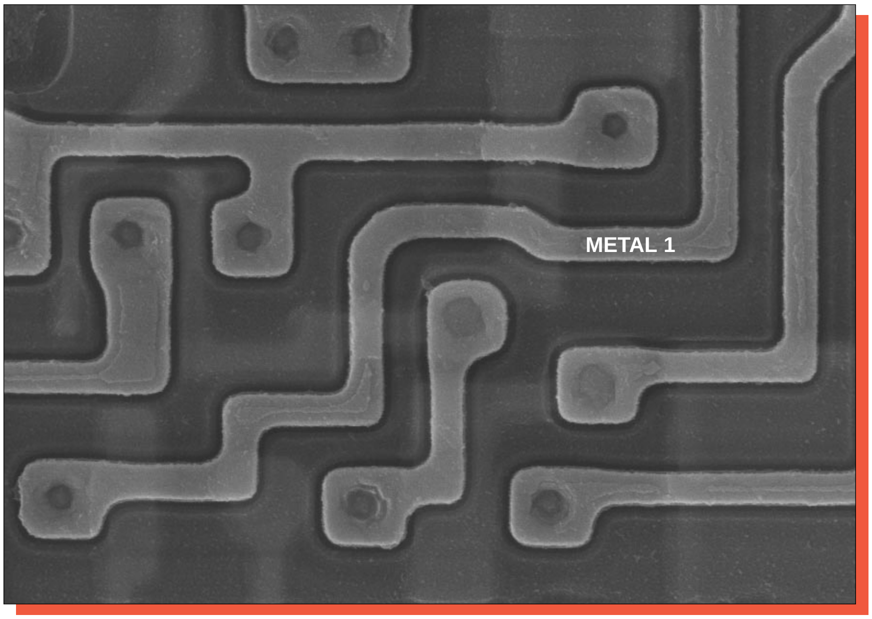


Mag. 26,000x



Mag. 40,000x

Figure 11. SEM section views of metal 1 line profiles.



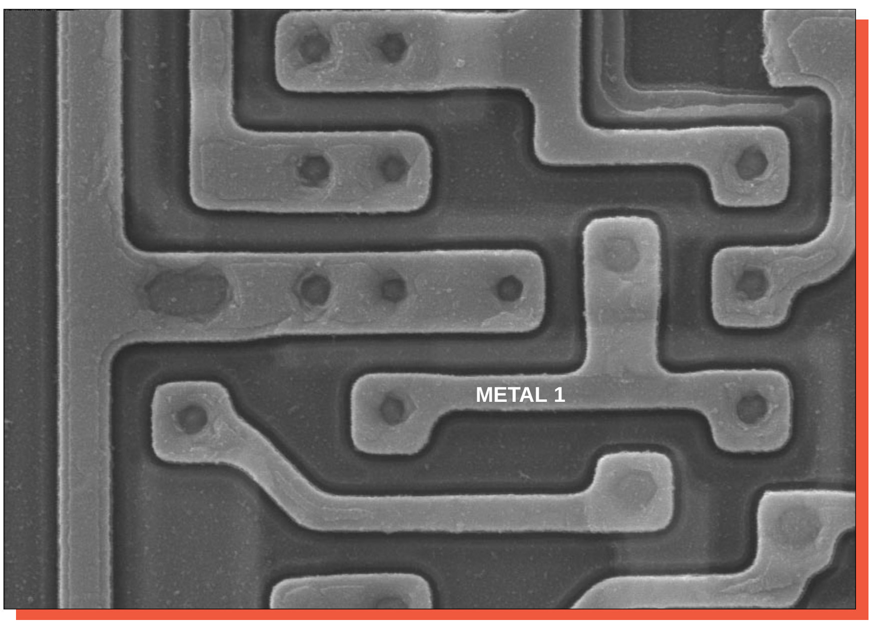
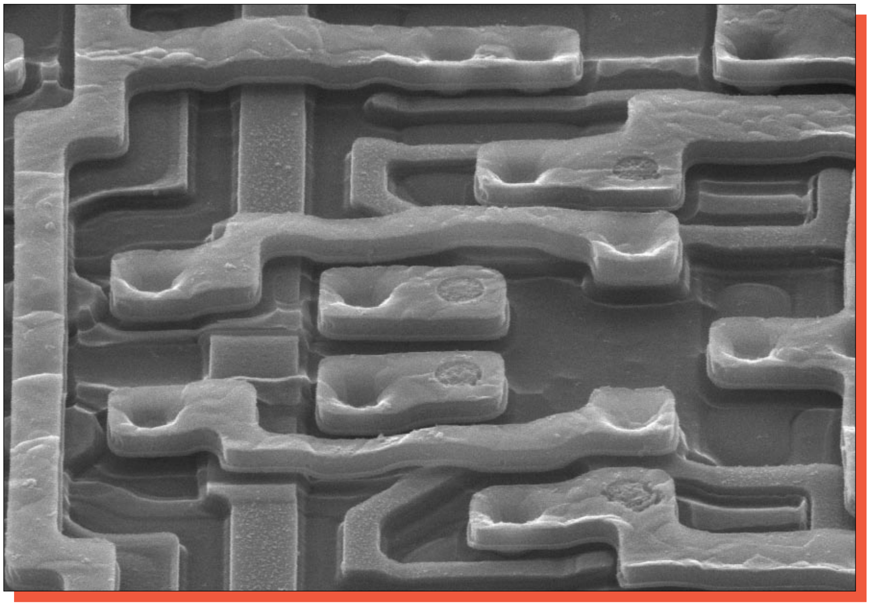
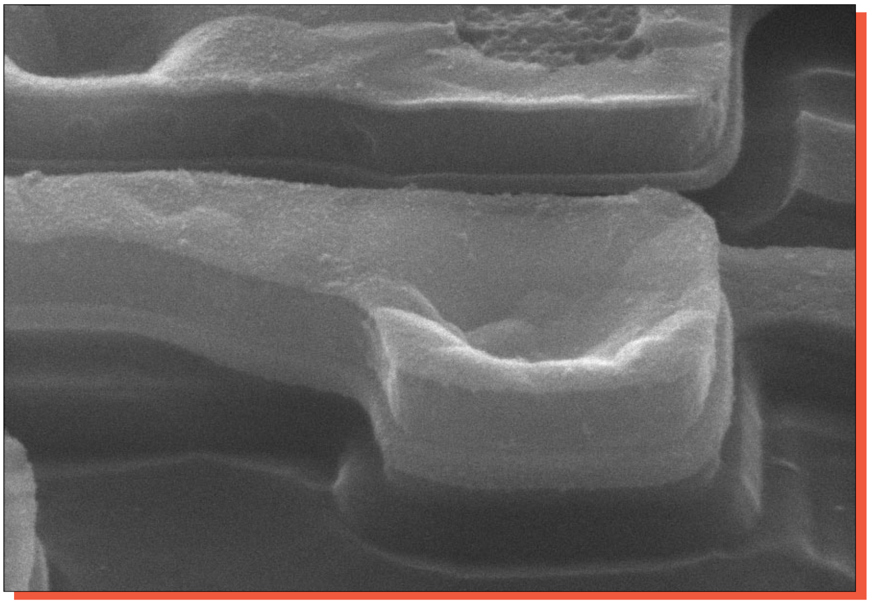


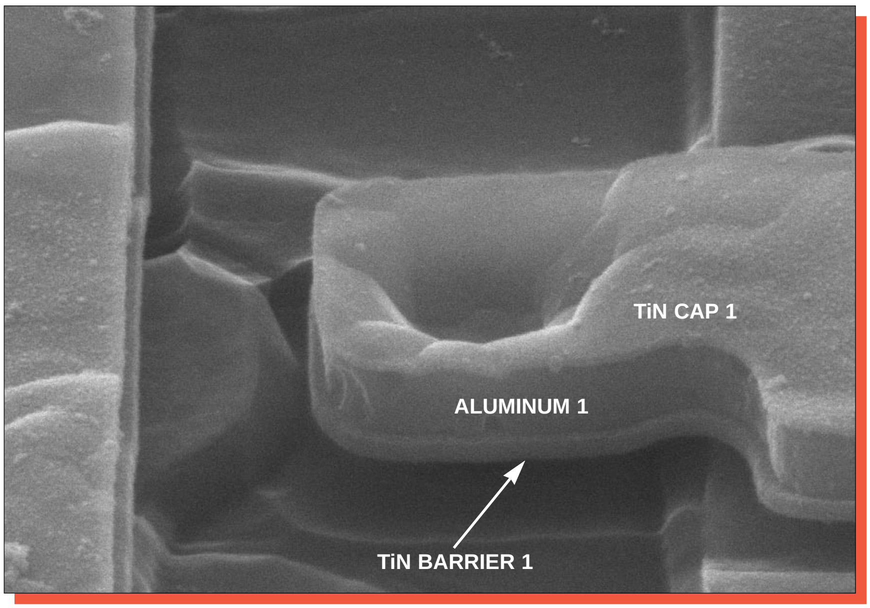
Figure 12. Topological SEM views of metal 1 patterning. Mag. 5000x, 0°.



Mag. 5700x

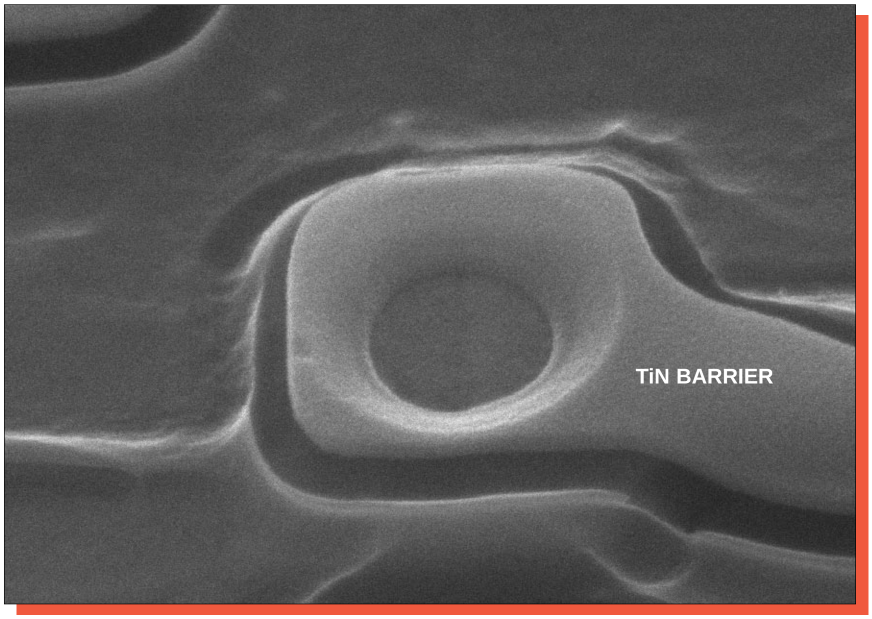


Mag. 23,000x

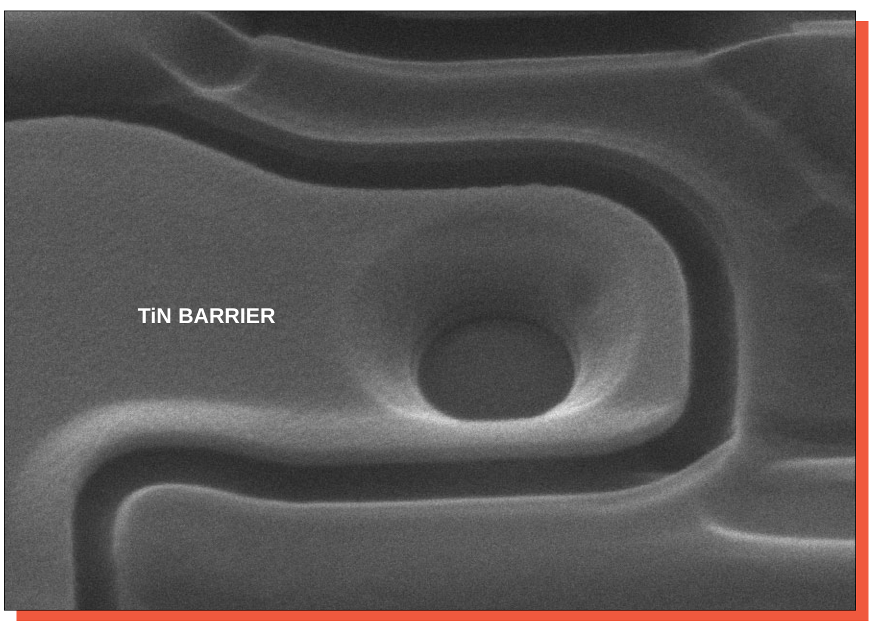


Mag. 23,000x

Figure 13. SEM views illustrating metal 1 coverage. 60°.

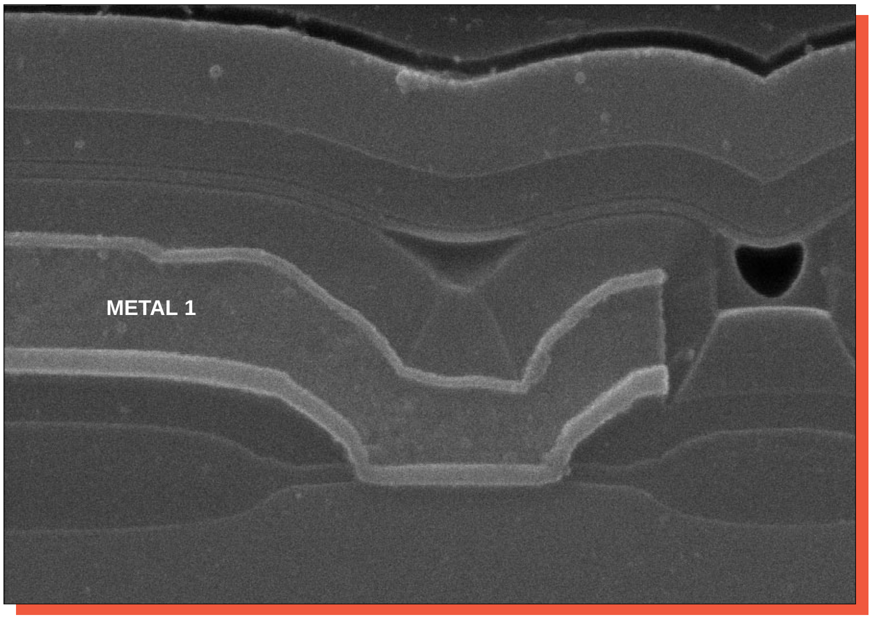


metal 1-to-poly

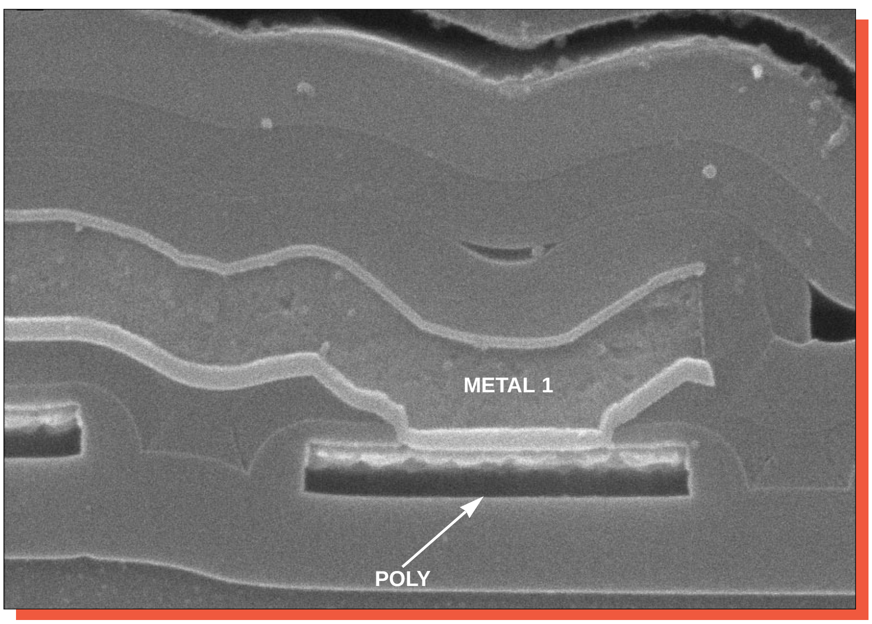


metal 1-to-diffusion

Figure 14. SEM views of the metal 1 barrier following the removal of aluminum.
Mag. 23,000x, 45°.

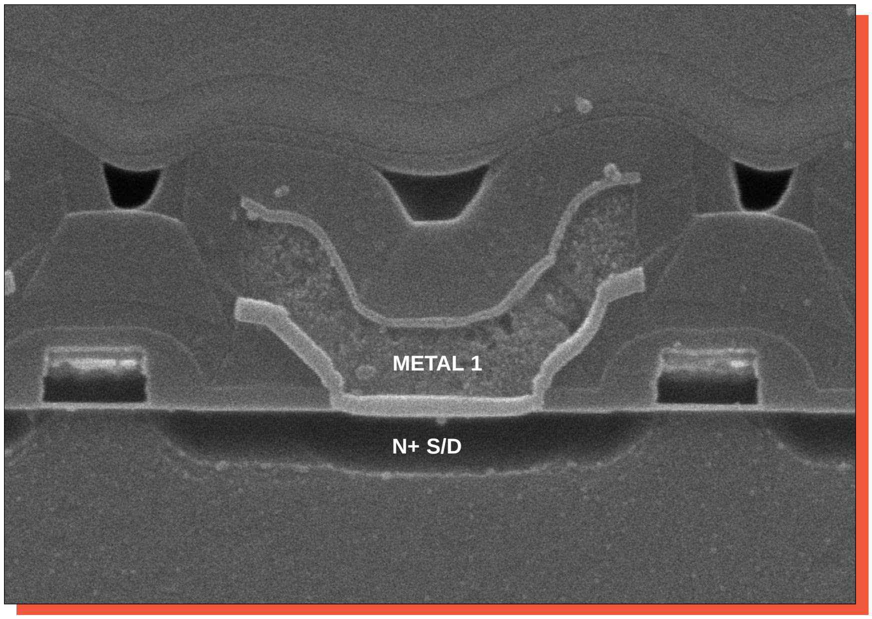


metal 1-to-diffusion, glass etch

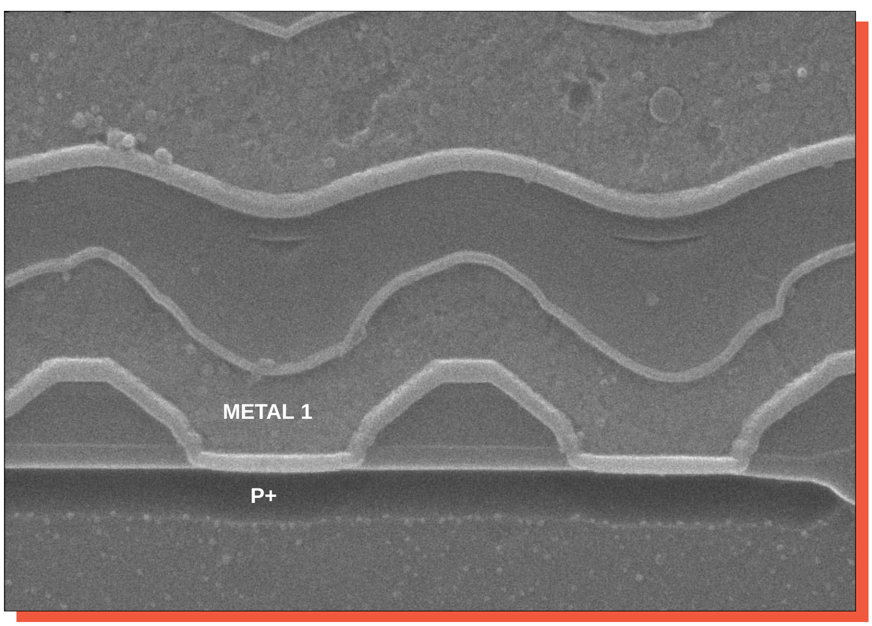


metal 1-to-poly, silicon etch

Figure 15. SEM section views of typical metal 1 contacts. Mag. 26,000x.

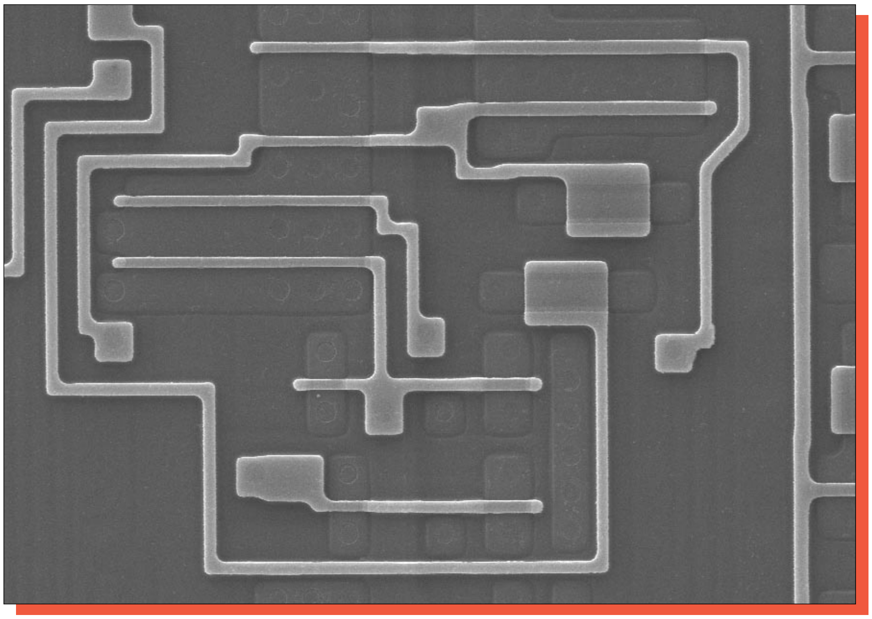


metal 1-to-N+

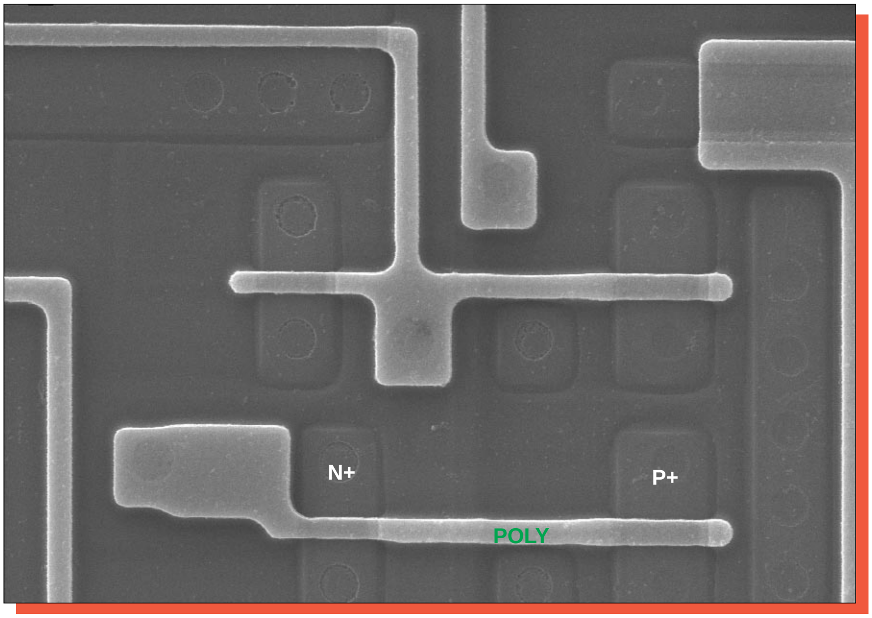


metal 1-to-P+

Figure 16. SEM section views of typical metal 1 contacts. Mag. 26,000x.

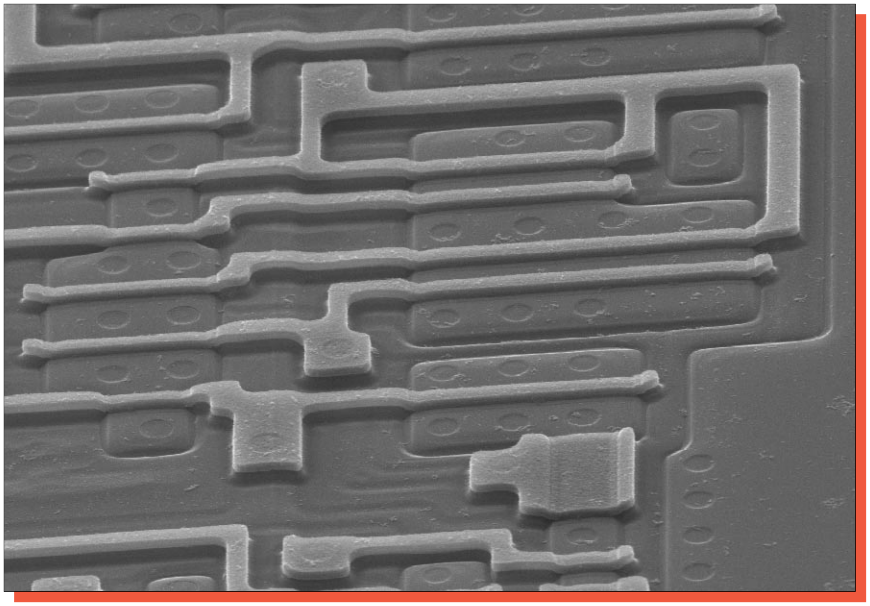


Mag. 2500x

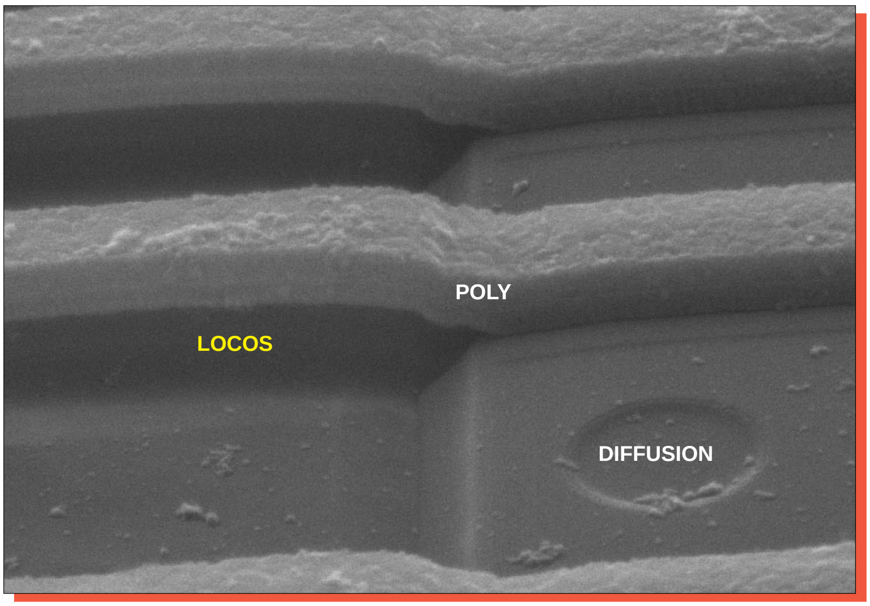


Mag. 5000x

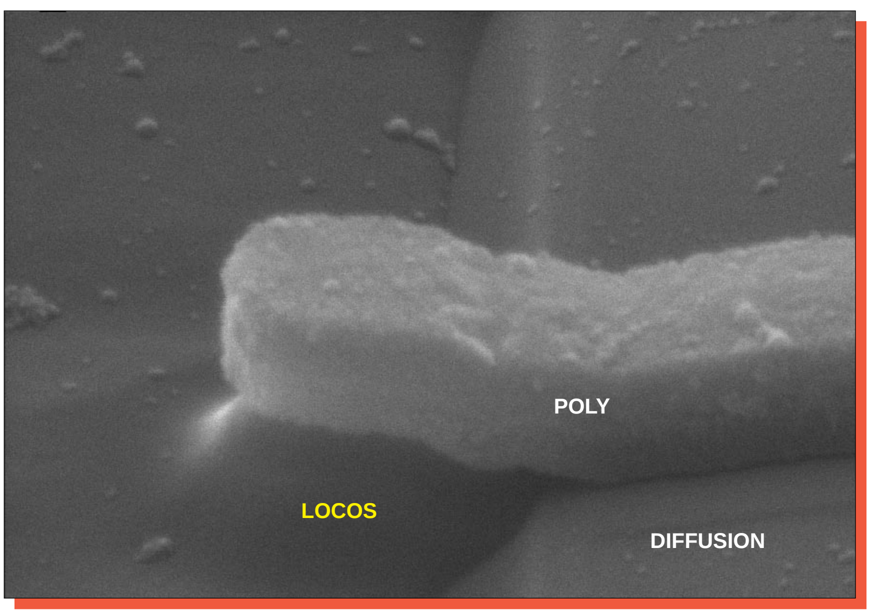
Figure 17. Topological SEM views of poly patterning. 0°.



Mag. 4200x

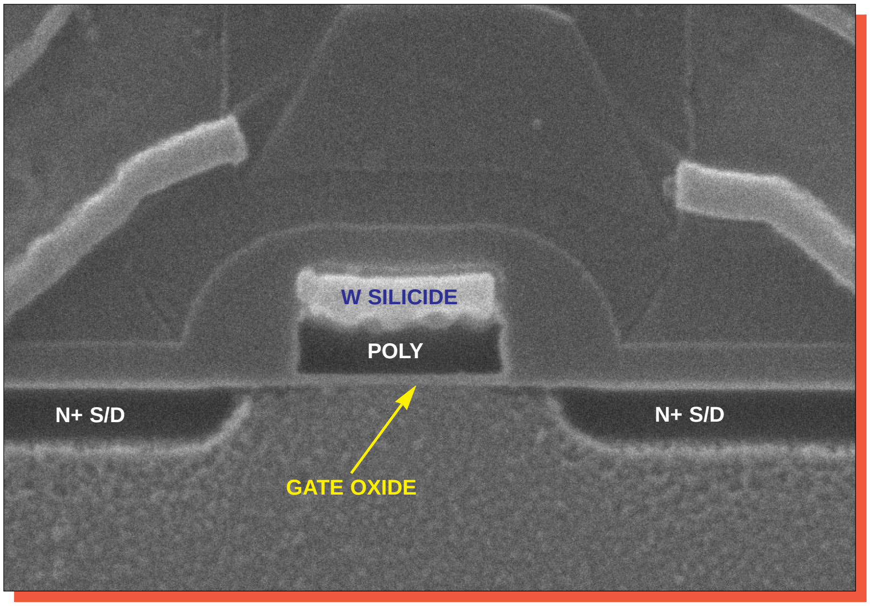


Mag. 26,000x

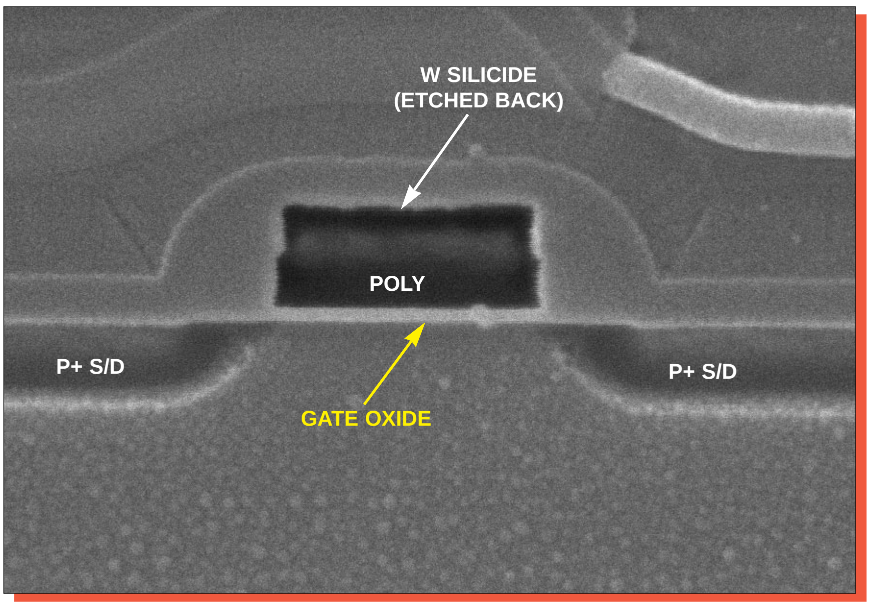


Mag. 52,000x

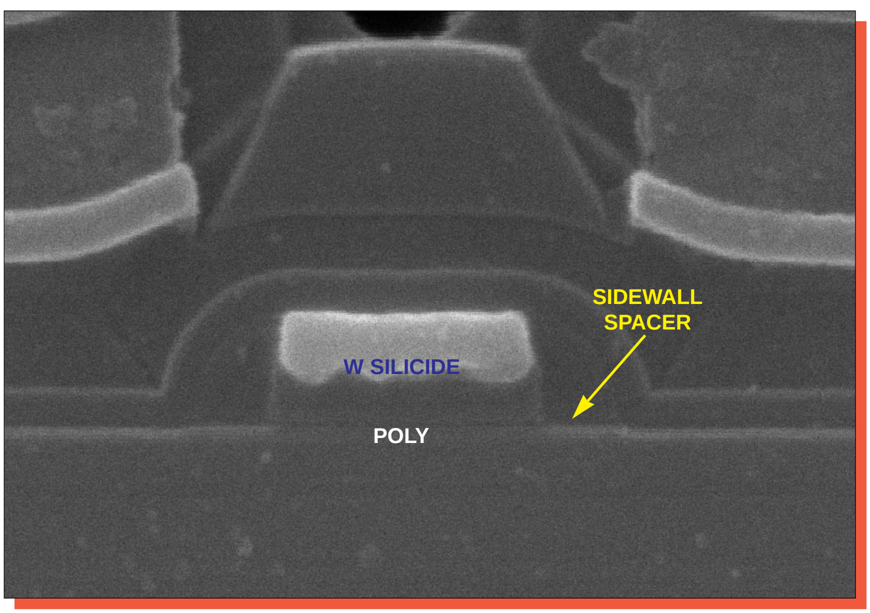
Figure 18. SEM views illustrating poly coverage. 60°.



N-channel



P-channel



glass etch

Figure 19. SEM section views of typical transistors. Mag. 52,000x.

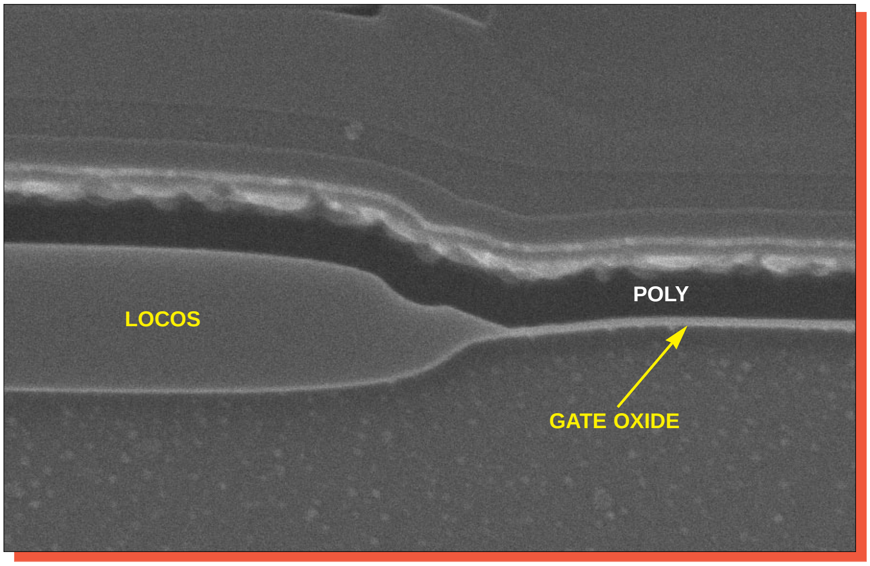
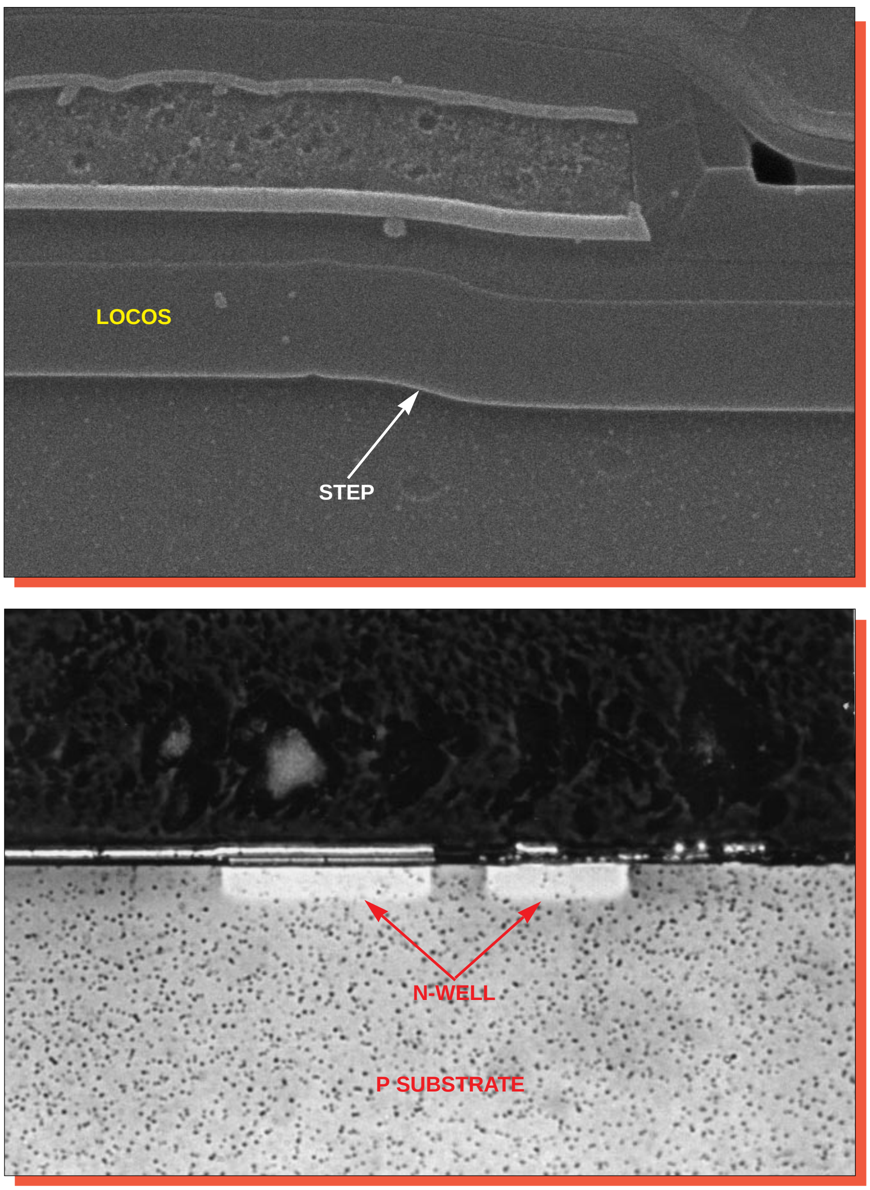


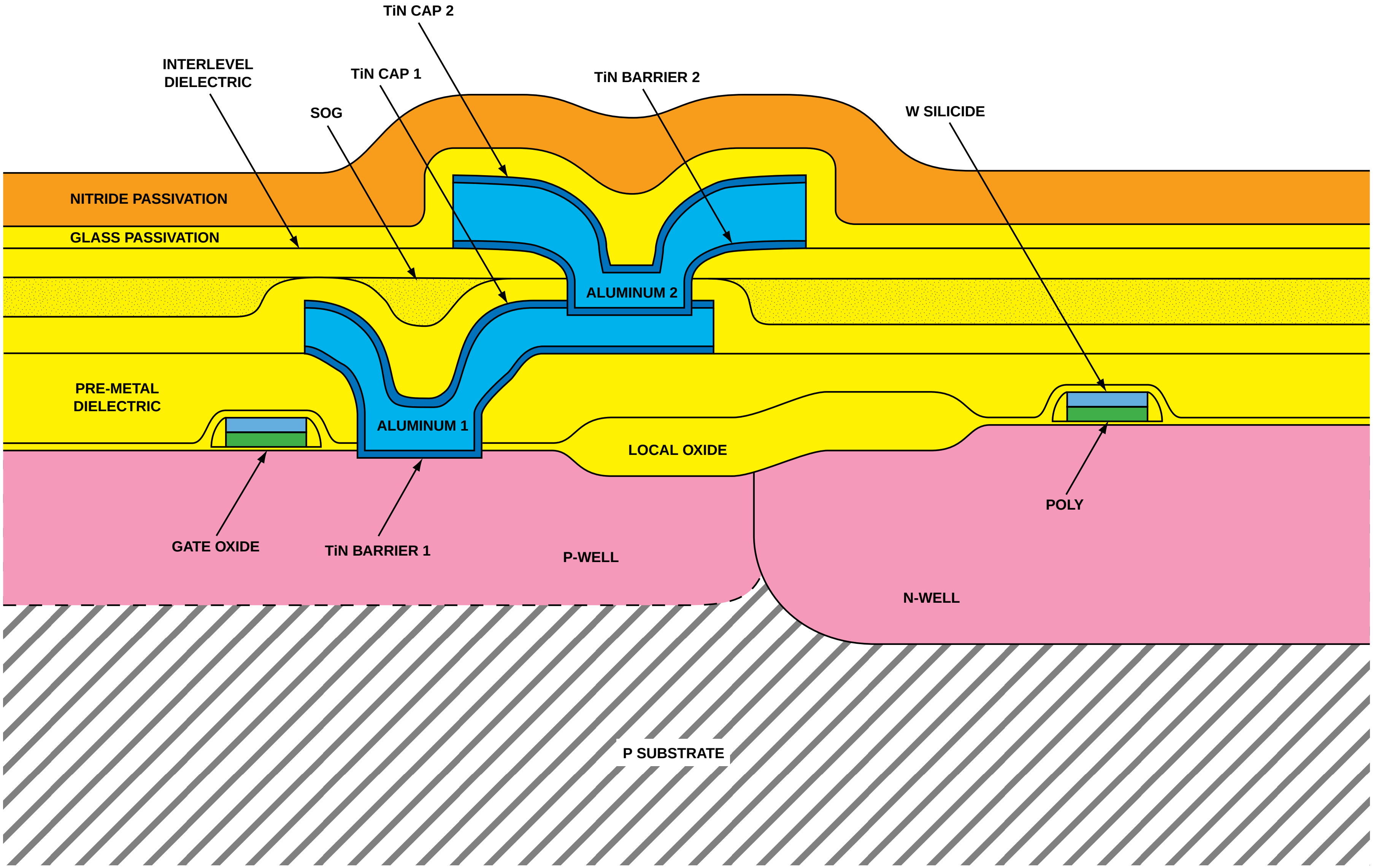
Figure 20. SEM section view of a local oxide birdsbeak. Mag. 40,000x.



Mag. 26,000x

Mag. 800x

Figure 21. Section views of the well structure.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 22. Color cross section drawing illustrating device structure.

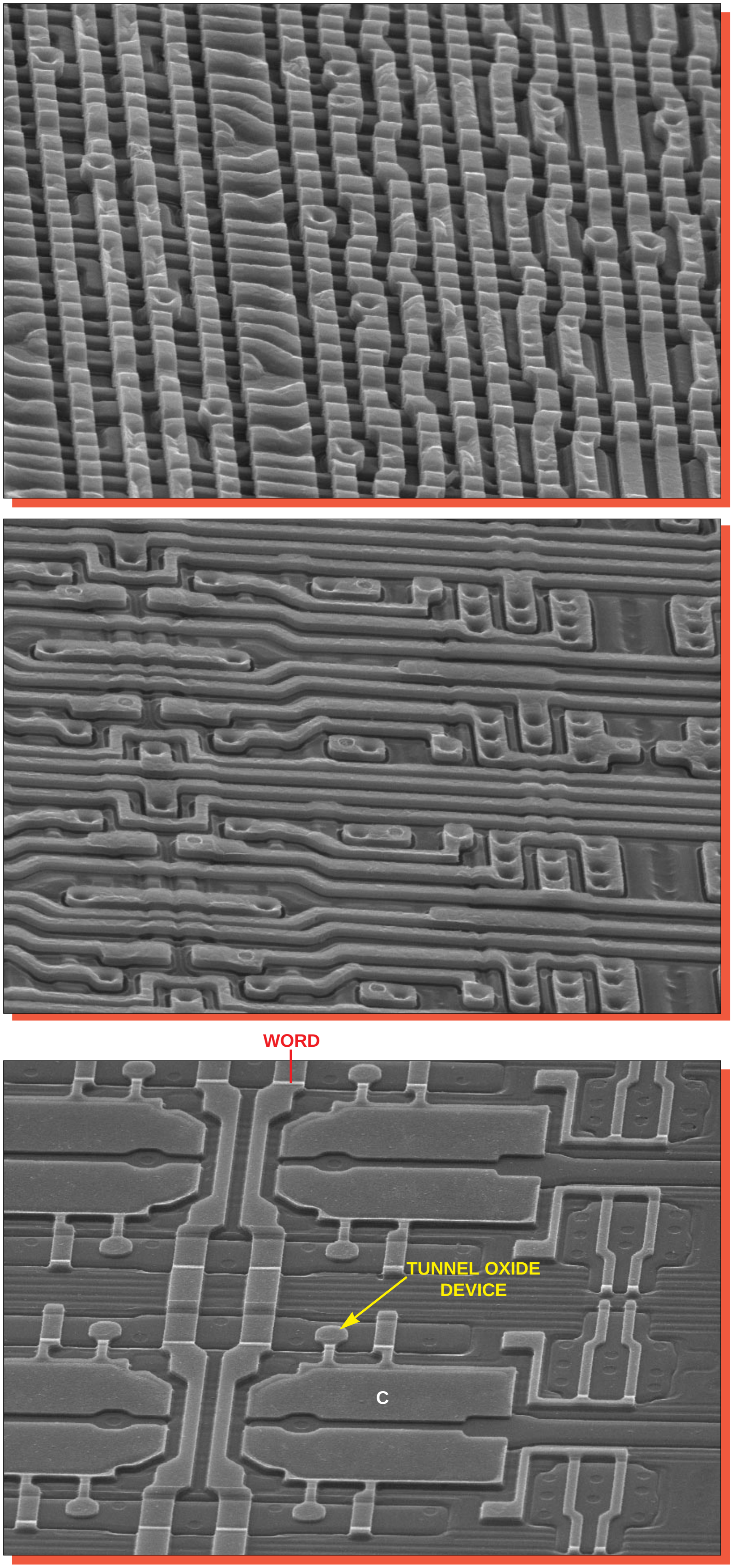
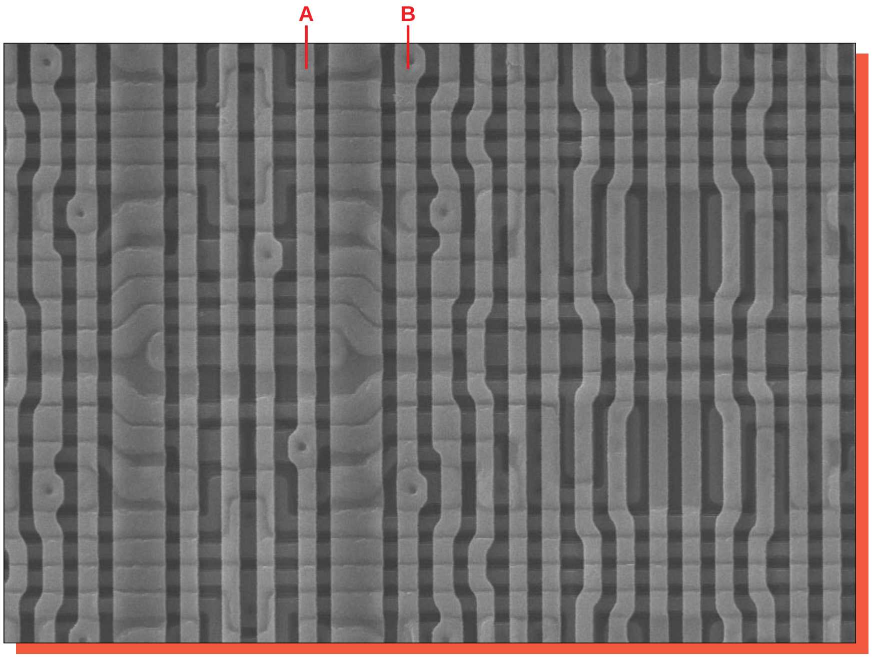
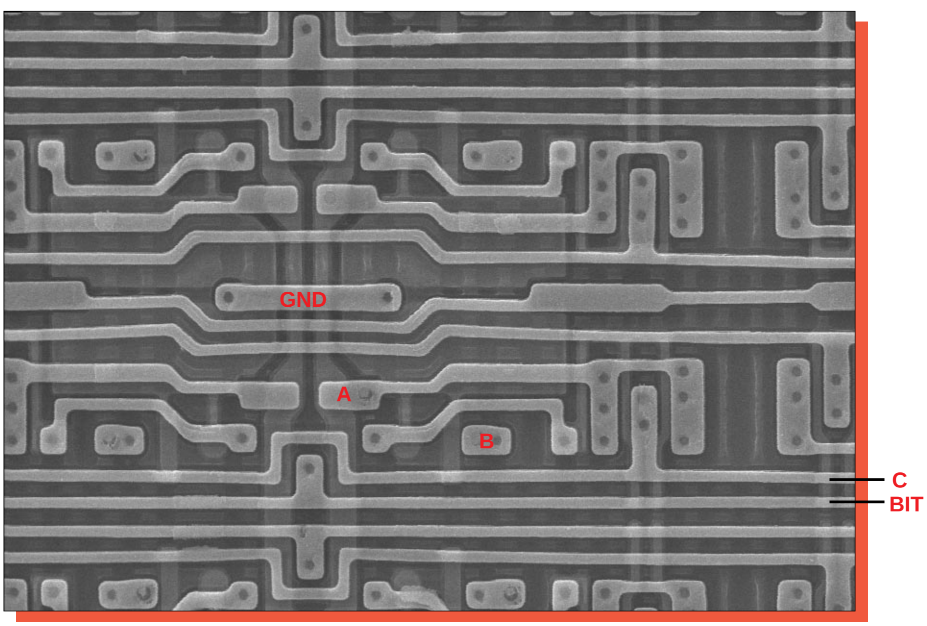


Figure 23. Perspective SEM views of an EEPROM cell layout. Mag. 2300x, 60°.

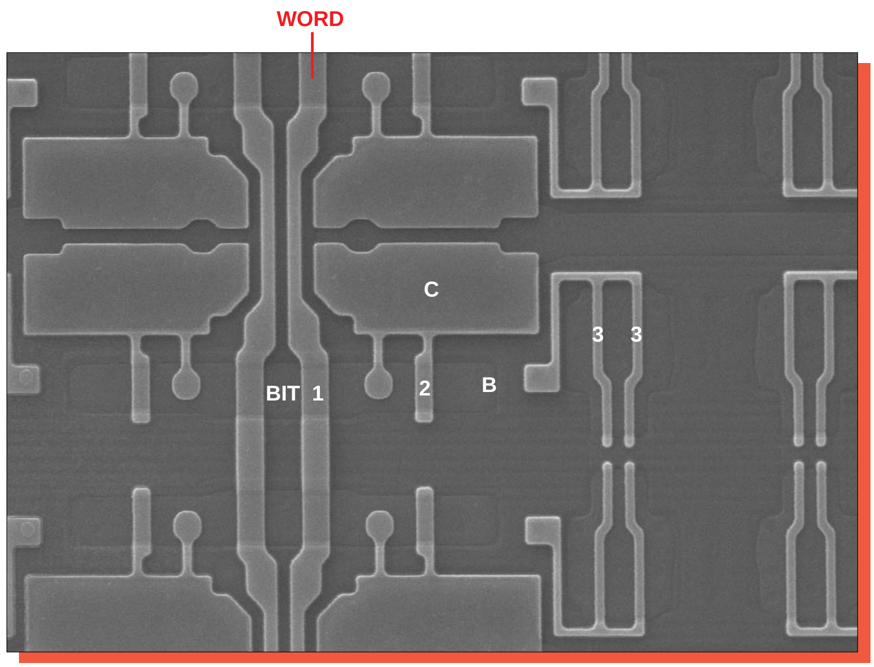


metal 2



metal 1

Figure 24. Topological SEM views of an EEPROM cell layout. Mag. 1600x, 0°.



unlayered

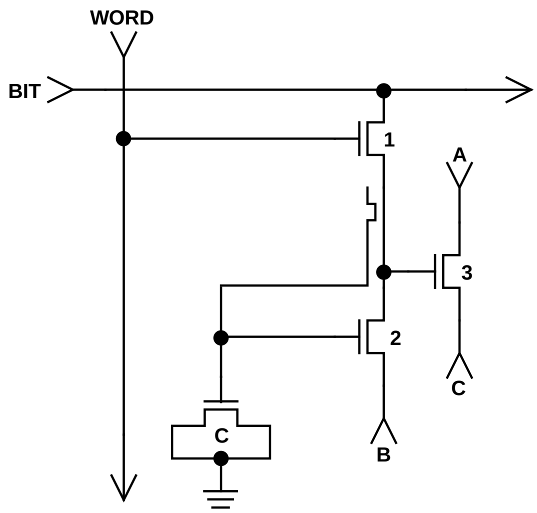
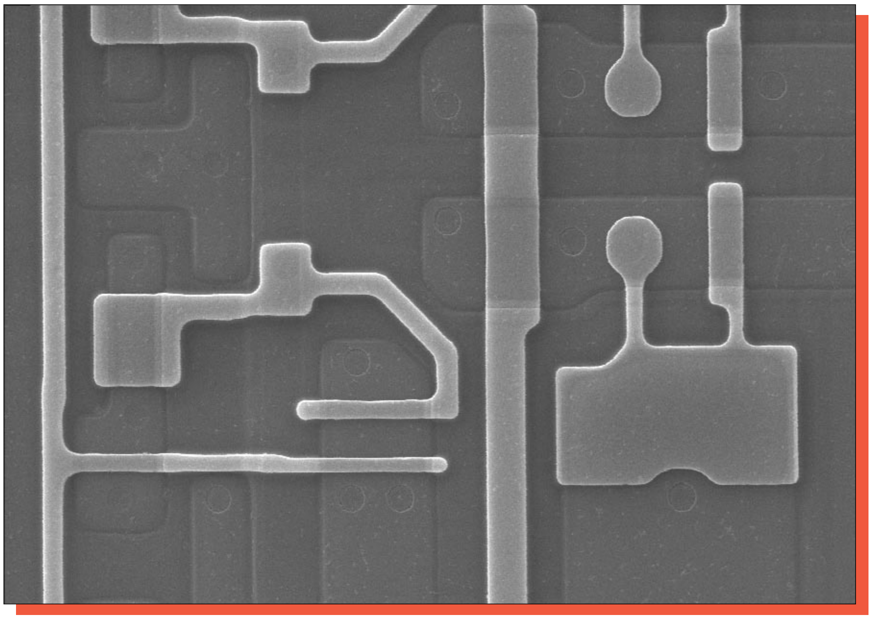
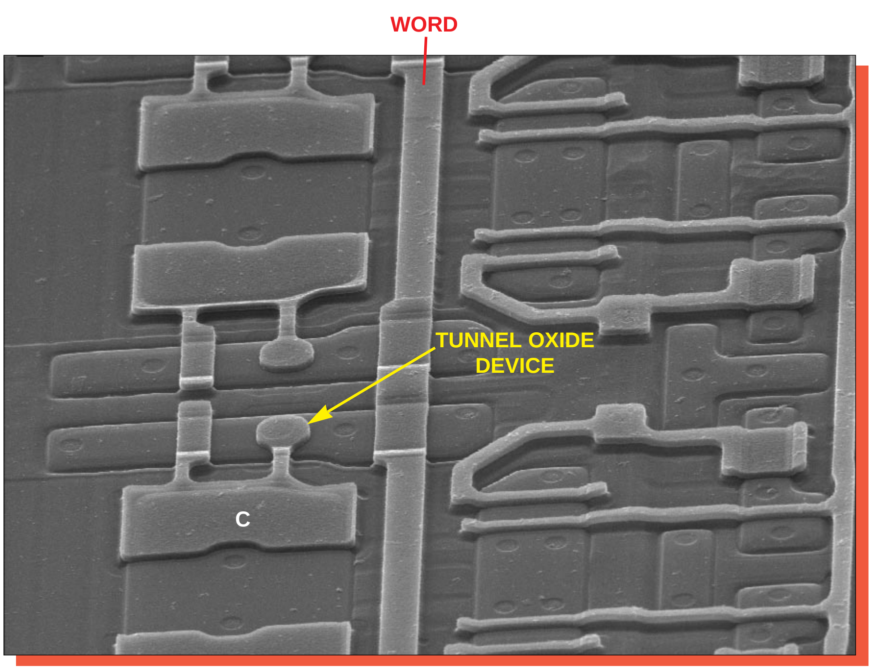


Figure 25. Topological SEM view and schematic of an EEPROM cell. Mag. 1600x, 0°.

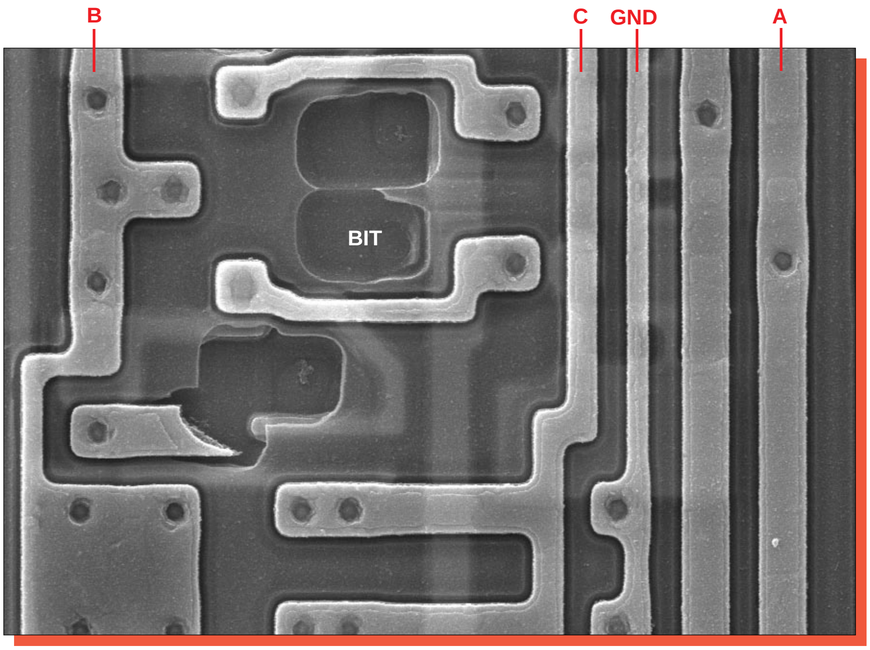


Mag. 3200x

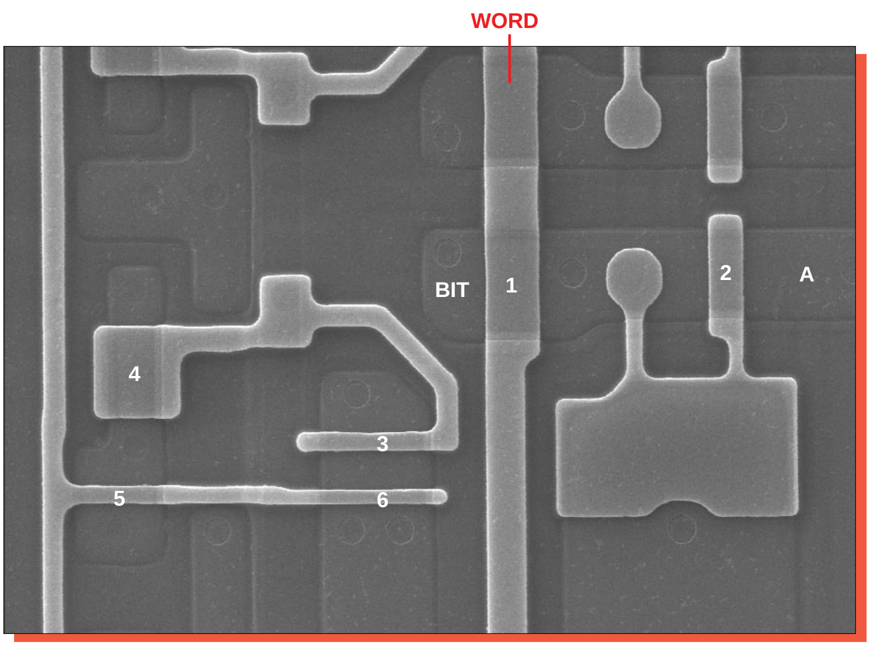


Mag. 3100x

Figure 26. Perspective SEM views of an EEPROM cell (unlayered). 60°.



metal 1



unlayered to poly

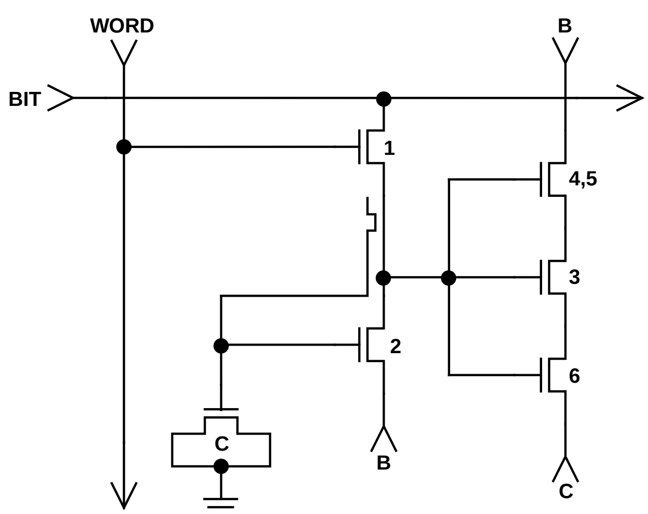
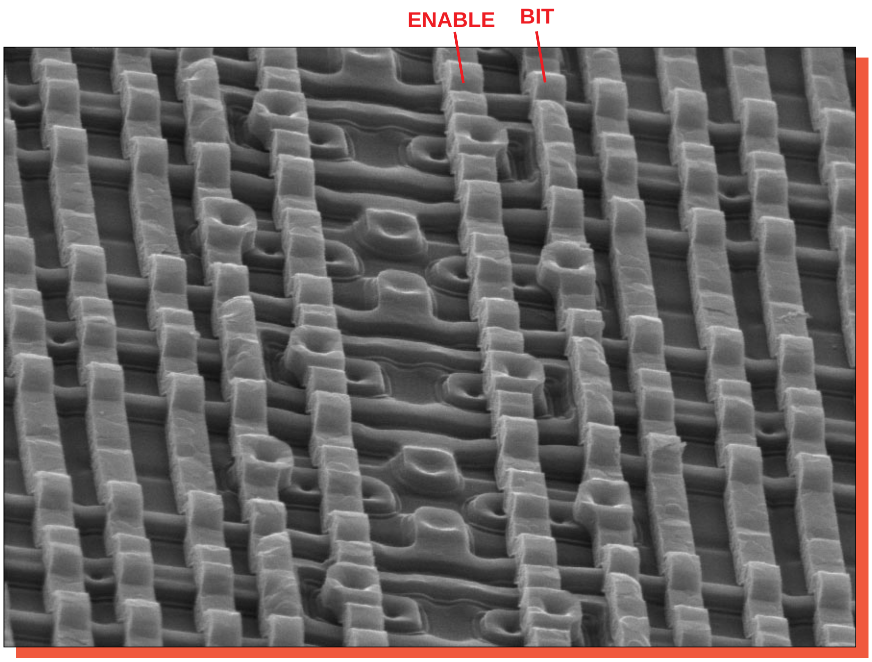
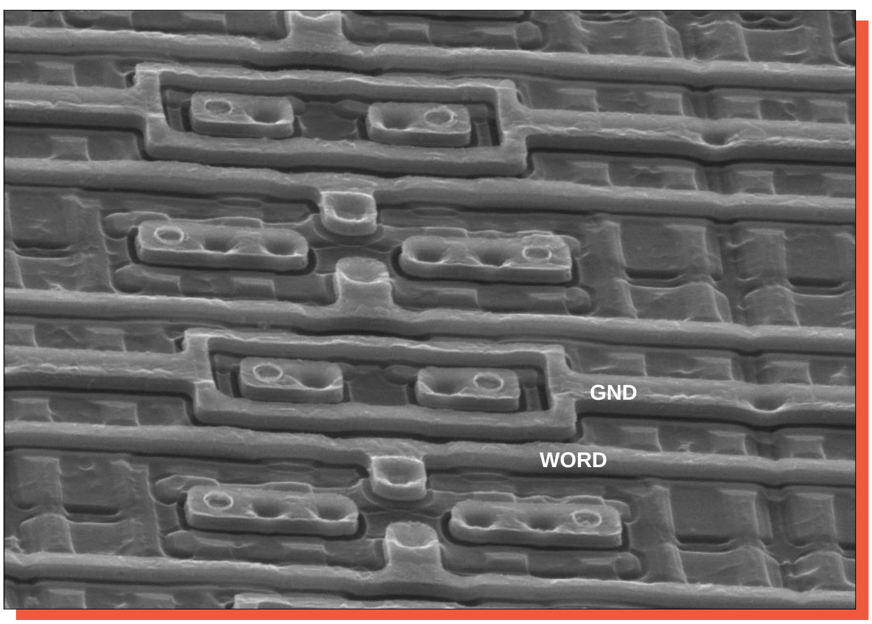


Figure 27. SEM views and schematic of an EEPROM cell. Mag. 3200x, 0°.

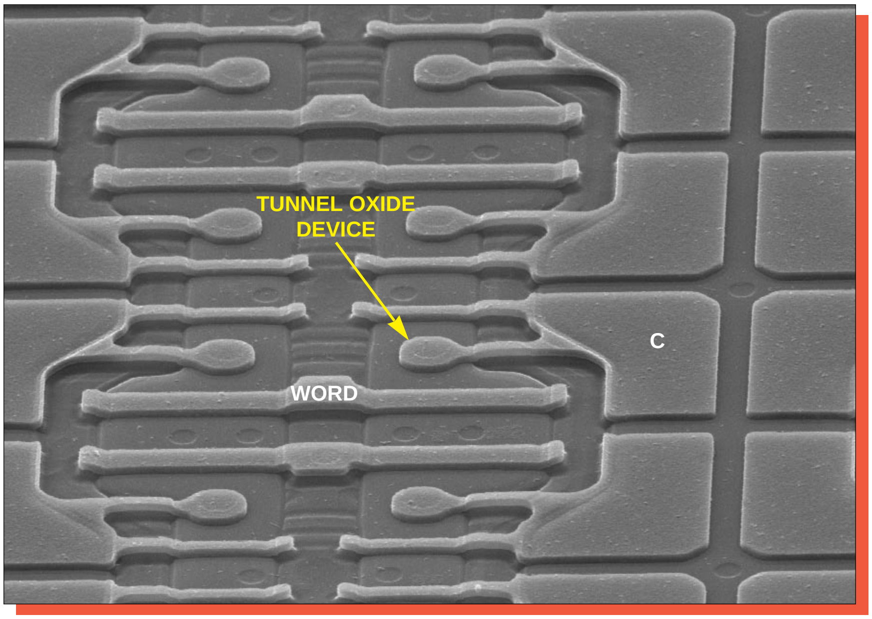


metal 2

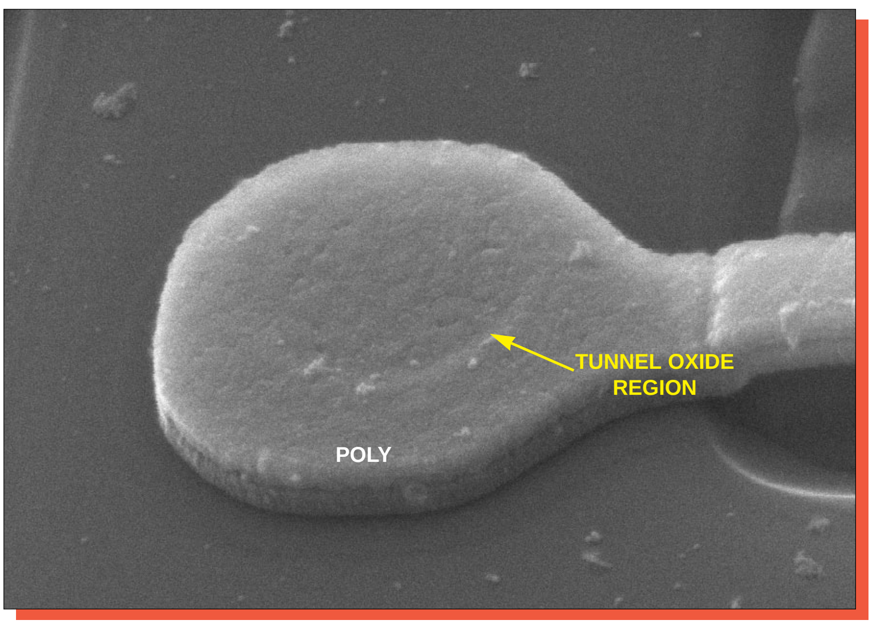


metal 1

Figure 28. Perspective SEM views of an EEPROM cell. Mag. 3400x, 60°.

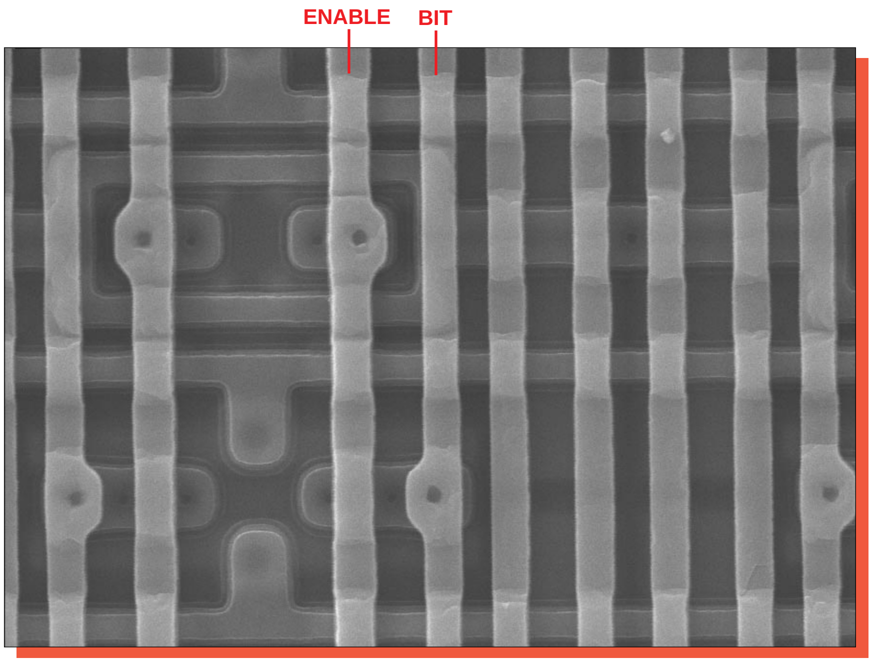


Mag. 3400x

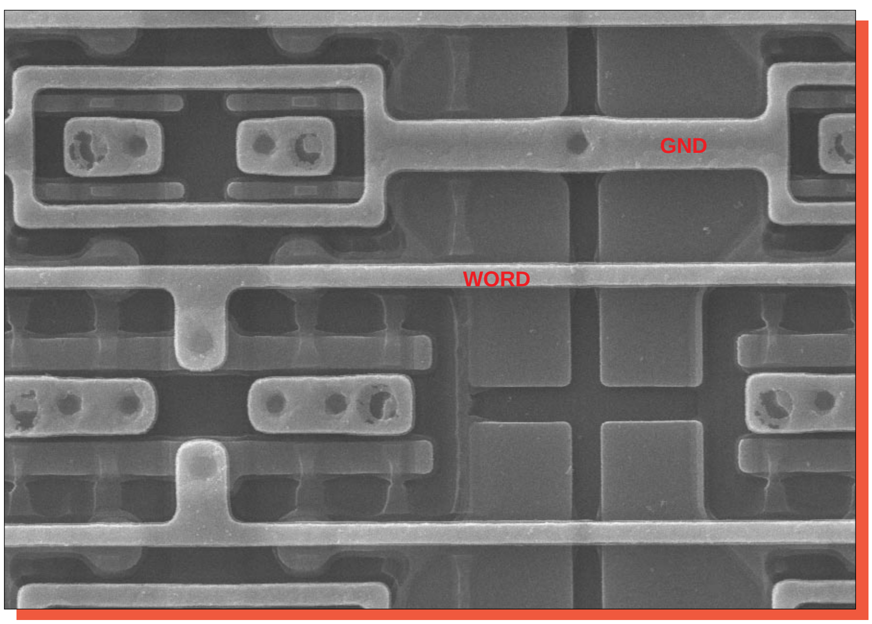


Mag. 27,000x

Figure 29. Perspective SEM views of an EEPROM cell (unlayered). 60°.

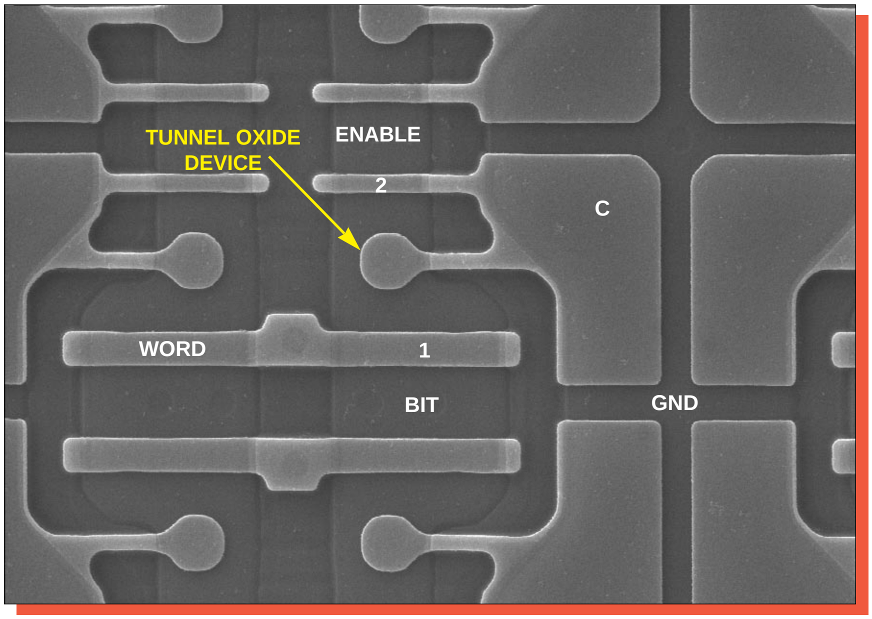


metal 2



metal 1

Figure 30. SEM views of an EEPROM cell. Mag. 3200x, 0°.



unlayered to poly

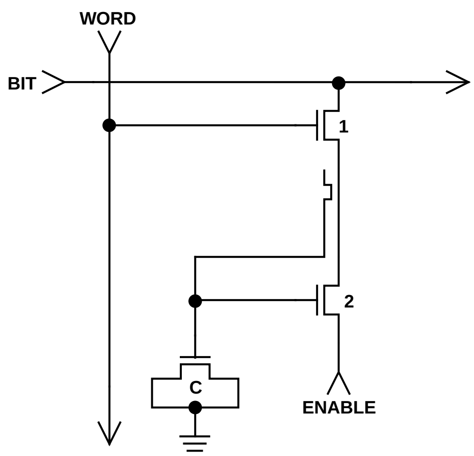
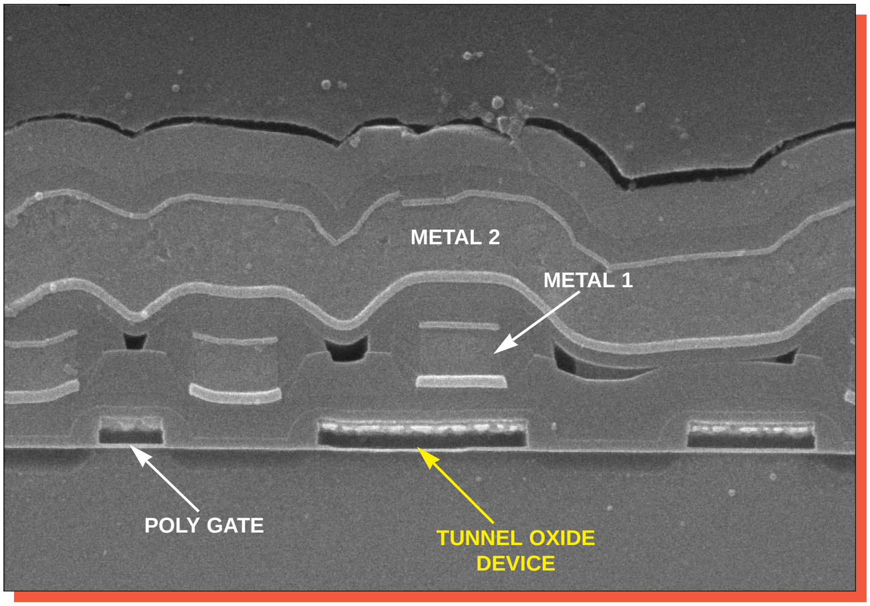
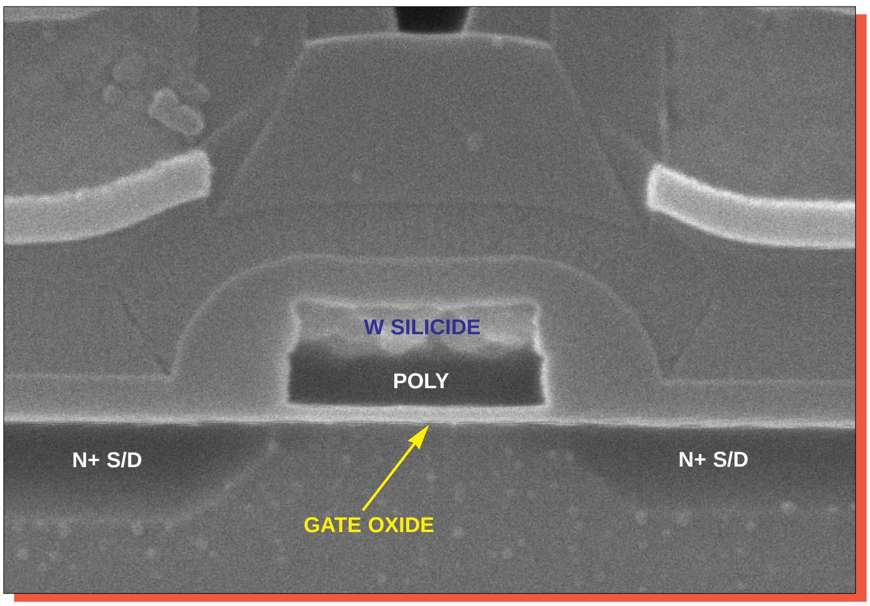


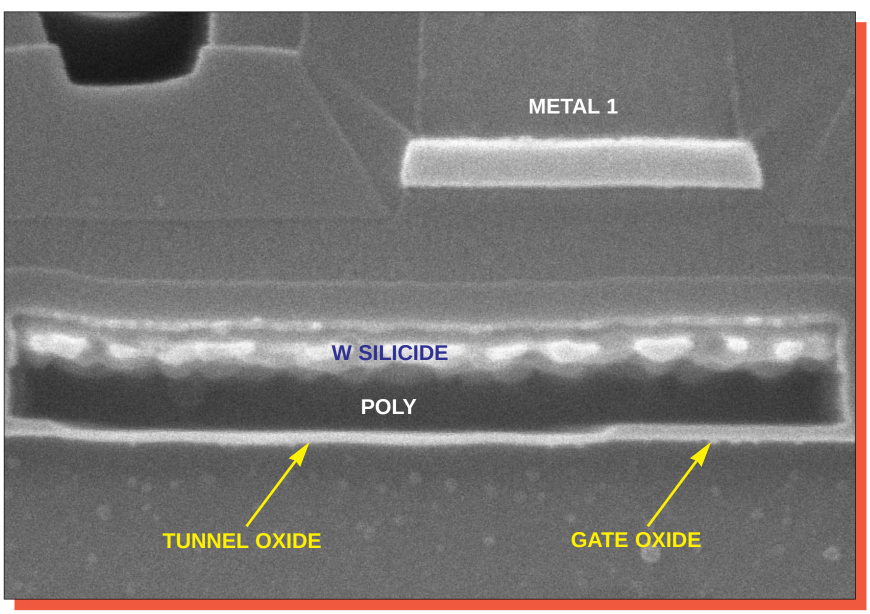
Figure 31. SEM view and schematic of an EEPROM cell. Mag. 3200x, 0°.



Mag. 13,000x

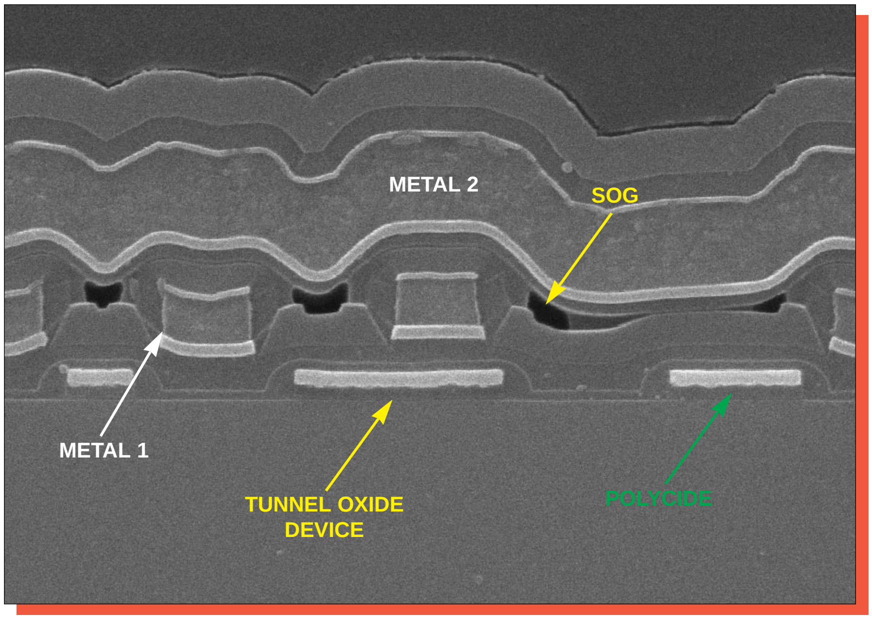


Mag. 52,000x

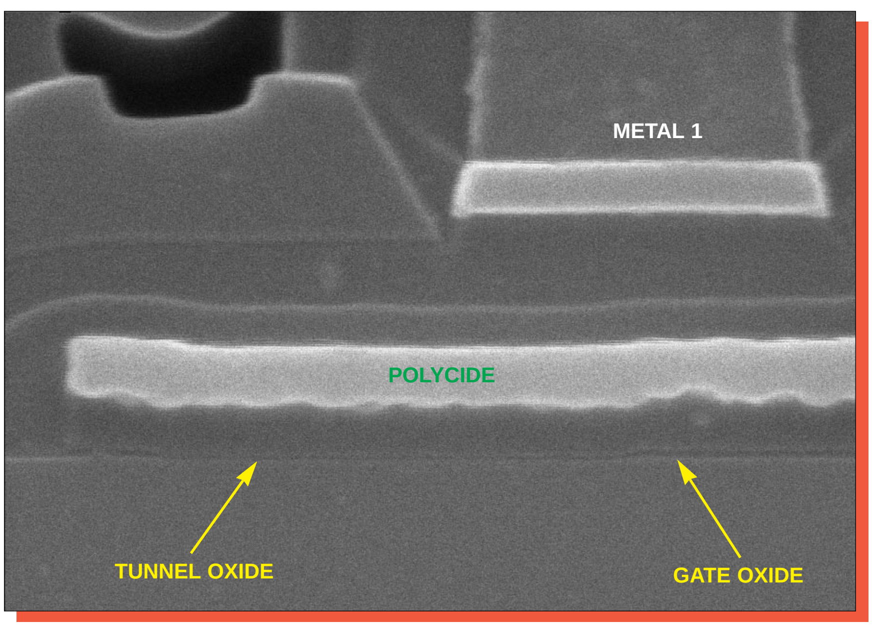


Mag. 52,000x

Figure 32. SEM section views of an EEPROM cell structure (silicon etch).



Mag. 13,000x



Mag. 52,000x

Figure 33. SEM section views of an EEPROM cell structure (glass etch).