

## Construction Analysis

# Xicor X25020P 2K (256 x 8) EEPROM

Report Number: SCA 9612-521



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## **INTRODUCTION**

This report describes a construction analysis of the Xicor X25020P 2K Serial EEPROM. Three devices encapsulated in 8-pin Plastic Dual In-line Packages (PDIPs) were supplied for the analysis. An apparent date code of 9432 was present on all devices.

## **MAJOR FINDINGS**

### **Questionable Items:<sup>1</sup>**

- Aluminum thinning up to 85 percent<sup>2</sup> at contact edges (Figure 14).
- Silicon mound growth occupied up to at least 90 percent of some contact areas (Figures 15 and 16).

### **Special Features:**

- Unique (Xicor) three poly cell design.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## TECHNOLOGY DESCRIPTION

### Assembly:

- Devices were encapsulated in 8-pin Plastic Dual In-line Packages (PDIPs).
- Lead-locking provisions (holes and anchors) at all pins.
- Thermosonic ball bond method employing 1.1 mil O.D. gold wire.
- All pins were connected.
- Sawn dicing (full depth).
- Silver-filled epoxy die attach.

### Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi on a P-substrate.
- Overlay passivation: A single thick layer of silicon-dioxide.
- Metallization: A single level of aluminum metallization was present. No cap or barrier metal was employed. Metal was defined by a dry-etch technique. Standard contacts were used (no plugs).
- Pre-metal dielectric: A borophosphosilicate glass (BPSG) over a densified oxide. This layer was reflowed prior to contact cuts.
- Polysilicon: Three layers of dry-etched polysilicon (no silicide). Poly 3 was apparently used to form all gates in the periphery and word lines in the array. Poly 2 was used to form the floating gates in the cell array. Poly 1 was used in the memory cell as a ground transistor and programming cathode. The poly 2 and 1 surface is

## **TECHNOLOGY DESCRIPTION (continued)**

textured (reportedly) to allow Fowler-Nordheim tunneling through relatively thick oxide thus eliminating the need for a thin tunneling oxide.

- Diffusions: Standard implanted P+ and shallow N+ diffusions formed the sources/drains of transistors. There was difficulty fully delineating the source/drain implants of the N channel transistors. Many attempts were made to try to stain these implants. All attempts resulted in shallow source/drains that do not extend to the end of the gate indicating an LDD process is used. No sidewalls were present on the gates.
- Wells: Twin-wells in a P-epi, on a P substrate.
- Memory: The memory cell design consisted of a word line formed by poly 3. Metal formed the bit lines. Poly 3 to poly 2 coupling serves as the erase tunneling element. Poly 2 is used to form the floating gates in the array . Poly 1 is used in the cell array to distribute ground and as the programming cathode during write operation. Programming is achieved by injecting electrons to and from the floating gate through Fowler-Nordheim tunneling.

## ANALYSIS RESULTS I

### Assembly:

### Figures 1 - 5

**Questionable Items:**<sup>1</sup> None.

### **General Items:**

- Devices were packaged in 8-pin Plastic Dual In-line Packages (PDIPs).
- Overall package quality: Normal. No defects were found on the external or internal portions of the packages.
- Lead-locking provisions (anchors and holes) were present.
- Wirebonding: Thermosonic ball bond method using 1.1 mil O.D. gold wire. No bond lifts occurred and bond pull strengths were good (see page 10). Wire spacing and placement was normal; however, some ball bond overlap was noted at a bonding pad (which damaged the pad window passivation) but no problems are foreseen (Figure 3).
- Die attach: Silver-filled epoxy of normal quantity and quality.
- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## ANALYSIS RESULTS II

### Die Process and Design:

Figures 6 - 30

#### **Questionable Items:<sup>1</sup>**

- Aluminum thinning up to 85 percent<sup>2</sup> at contact edges (Figure 14).
- Silicon mound growth occupied up to at least 90 percent of some contacts (Figures 15 and 16).

#### **Special Features:**

- Unique (Xicor) three poly cell design.

#### **General Items:**

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi on a P substrate.
- Design and layout: Die layout was clean but not efficient. It appeared that a 1K design was changed to 2K by simply extending the cell array. Alignment was good at all levels.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.
- Overlay passivation: A thick layer of silicon-dioxide. Overlay integrity tests indicated defect-free passivation. Edge seal was good. The scribing was close to the passivation edge around the die perimeter on some sides; however, no damage occurred to the metal bus line.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## ANALYSIS RESULTS II (continued)

- Metallization: A single layer of silicon-doped aluminum. No cap or barrier metal was used.
- Metal patterning: The metal layer was patterned by a dry etch of normal quality. All contacts were completely surrounded by aluminum.
- Metal defects: None. No voiding or notching of the metal layer was found. Small and evenly distributed silicon nodules were noted following removal of the metal. Silicon mound growth was noted in the contact areas.
- Metal step coverage: Worst case aluminum thinning was 85 percent at contact edges. Typical aluminum thinning was 80 percent but did not appear of serious concern. MIL-STD allows up to 70 percent metal thinning for contacts of this size.
- Contacts: Metal contact cuts appeared to be defined by a dry-etch. Some over-etching of the contacts was noted at metal-to-poly and N+ diffusion. The metal occupied up to 50 percent of the N+ depth; however, apparent deep N+ contact diffusions were present and no danger appeared to exist. Mounds occupied up to at least 90 percent of some contacts, which will increase contact resistance and possibly correct device performance.
- Pre-metal dielectric: A borophosphosilicate glass (BPSG) over a densified oxide. The glass was reflowed prior to contact cuts. No problems were found.
- Polysilicon: Three layers of dry-etched polysilicon (no silicide). Poly 3 was apparently used to form gates in the peripheral circuits, and word lines in the array. Poly 2 was used to form the floating gates in the cell array. Poly 1 was used in the memory cell as a ground transistor and programming cathode. The poly 2 and 1 surface is textured (reportedly) to allow Fowler-Nordheim tunneling through relatively thick oxide thus eliminating the need for a very thin tunneling oxide. Definition was by a dry etch of good quality and no defects were found.

## **ANALYSIS RESULTS II (continued)**

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeak or elsewhere. A slight step was noted in the LOCOS at the well boundaries indicating a twin-well process was used.
- Diffusions: Standard implanted P+ diffusions were used for sources and drains. There was difficulty fully delineating the source/drain implants of the N channel transistors. All attempts at delineation resulted in shallow source/drains that do not extend to the edge of the gate indicating an LDD process is used although no sidewalls were present on the gates.
- Wells: Twin-wells were used.
- Epi: A P-epi layer was employed. No defects were found in the epi or substrate silicon.
- Buried contacts: Direct poly-to-diffusion (buried) contacts were not used.
- Memory cells: The memory cell design consisted of a word line formed by poly 3. Metal formed the bit lines. Poly 3 to poly 2 also serve as the erase tunneling element. Poly 2 is used to form the floating gates in the array. Poly 1 is used in the cell array to distribute ground and as the programming cathode during write operation. Programming is achieved by injecting electrons to and from the floating gate through Fowler-Nordheim tunneling. Cell pitch was 10 x 10 microns.

## PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulation

Internal optical inspection

SEM inspection of assembly features and passivation

Passivation integrity tests

Wirepull tests

Passivation removal

SEM inspection of metal

Metal removal and inspect contacts and silicon nodules

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)\*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal to Poor

**DETAIL OF EVALUATION**

Package integrity	G
Package markings	G
Die placement	G
Die attach quality	G
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	G
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.
Die attach method	Silver-filled epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity <sup>1</sup>	NP
Contact coverage	G
Contact registration	G
Contact defects	NP

*<sup>1</sup>85 percent metal thinning and silicon mound growth up to 90 percent at contacts.*

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## PACKAGE MARKINGS

### Top

X25020P  
T9432 D

### Bottom

3519A  
L24805 A (plus molded markings)

## WIREBOND STRENGTH

Wire material: 1.1 mil diameter gold

Die pad material: aluminum

Material at package post: silver

**Sample #** 2

# of wires tested: 8

Bond lifts: 0

Force to break - high: 11.5g

- low: 4.5g

- avg.: 9.1g

- std. dev.: 2

## DIE MATERIAL ANALYSIS

Passivation: Single layer of silicon-dioxide.

Metallization: Silicon-doped aluminum.\*

Pre-metal dielectric: A borophosphosilicate glass (BPSG) containing 4.65 wt. % phosphorus and 2.3 wt. % boron over a densified oxide.

\*There is no known method for accurately determining the amount of silicon in the aluminum on a finished die.



## VERTICAL DIMENSIONS

Die thickness: 0.7 mm (27 mils)

### Layers

Passivation:	0.65 micron
Metallization:	1.2 micron
Pre-metal glass:	1.4 micron
Oxide on poly 3:	0.3 micron
Poly 3:	0.35 micron
Poly 2:	0.3 micron
Poly 1:	0.3 micron
Oxide on N+:	0.15 micron
Oxide on P+:	0.1 micron
Local oxide:	0.75 micron
N+ diffusion:	0.2 micron
P+ diffusion:	0.25 micron
N-well:	2.0 microns
P-epi:	15.5 microns

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COLOR DRAWING OF DIE STRUCTURE	Figure 20a
MEMORY CELL	Figures 21 - 29
INPUT PROTECTION CIRCUIT	Figure 30
GENERAL CIRCUIT LAYOUT	Figure 30

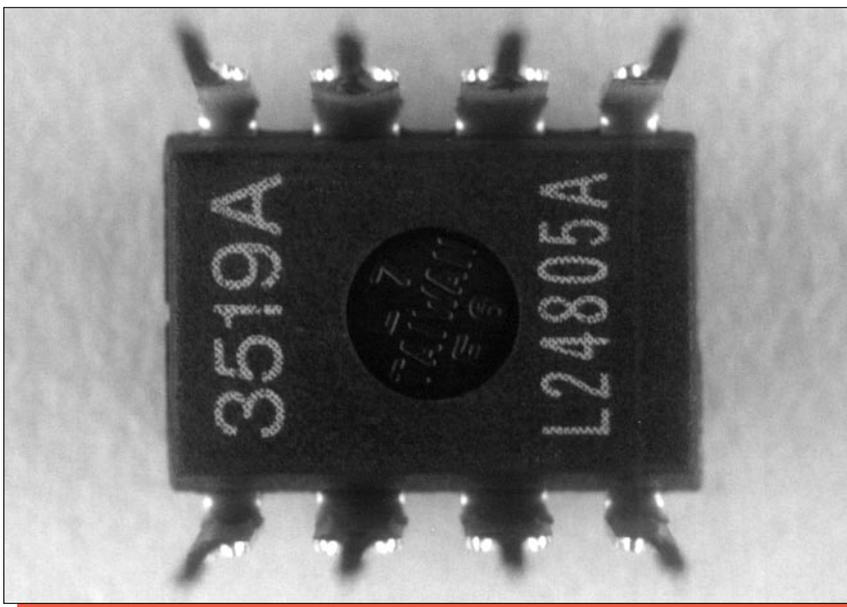
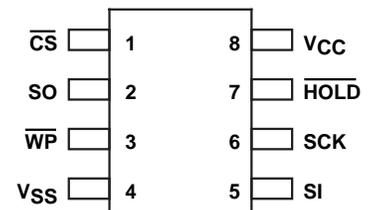
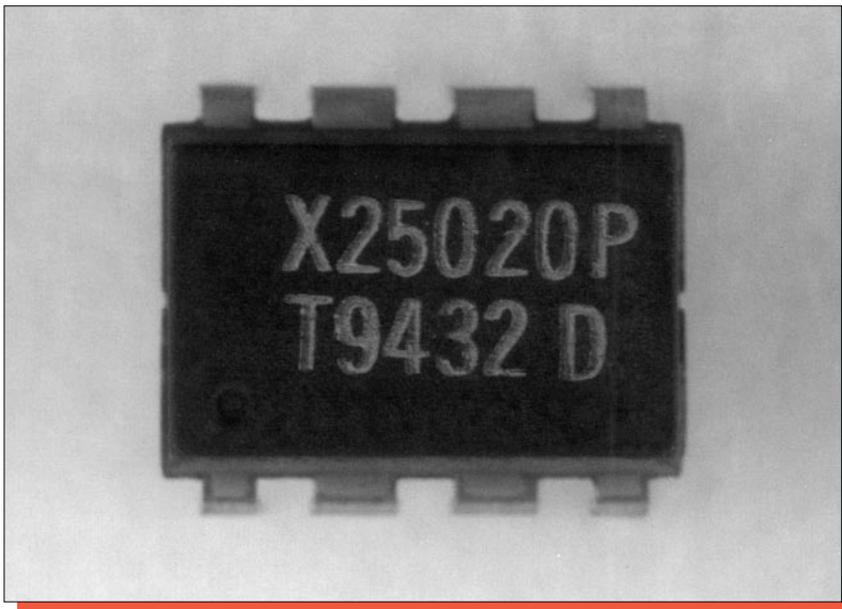
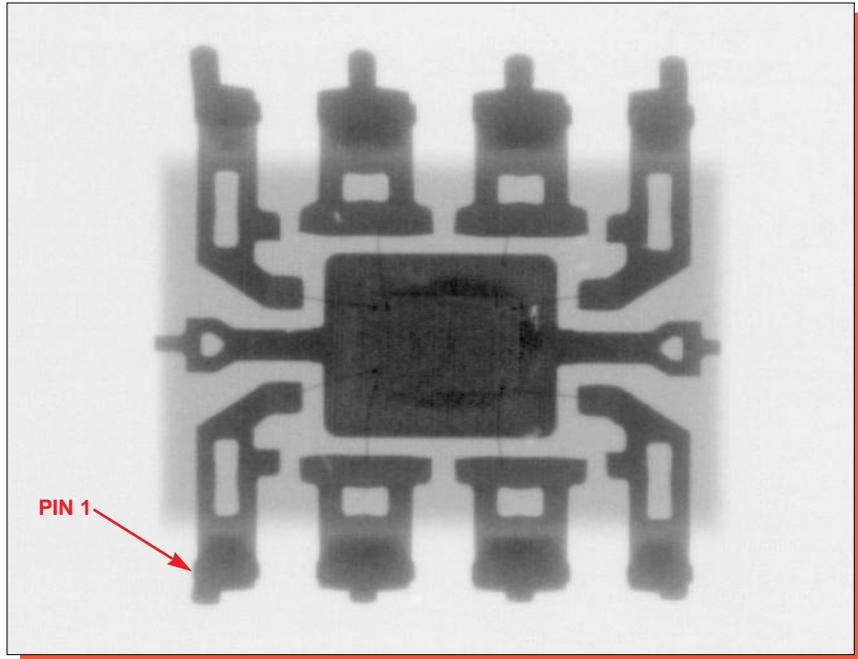
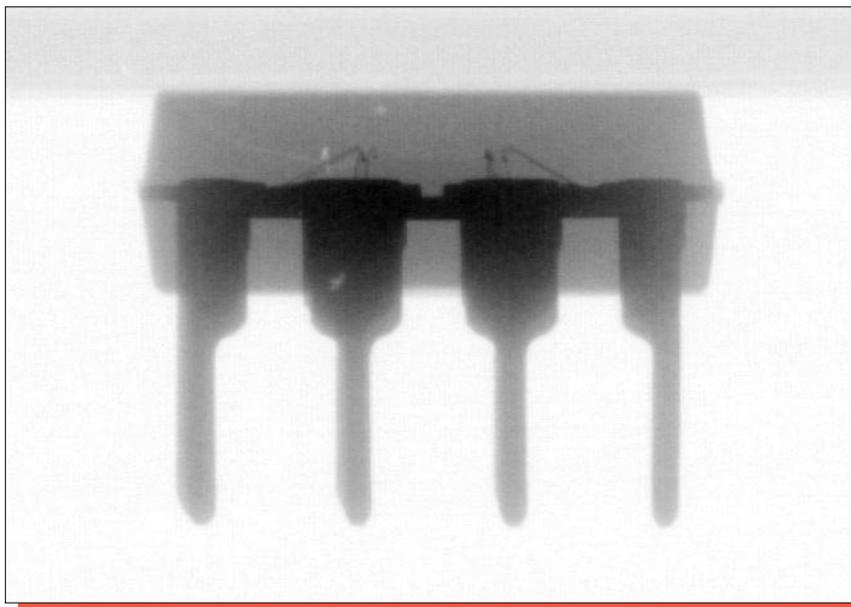


Figure 1. Package photographs and pinout diagram of the Xicor X25020P 2K Serial EEPROM. Mag. 7.5x.

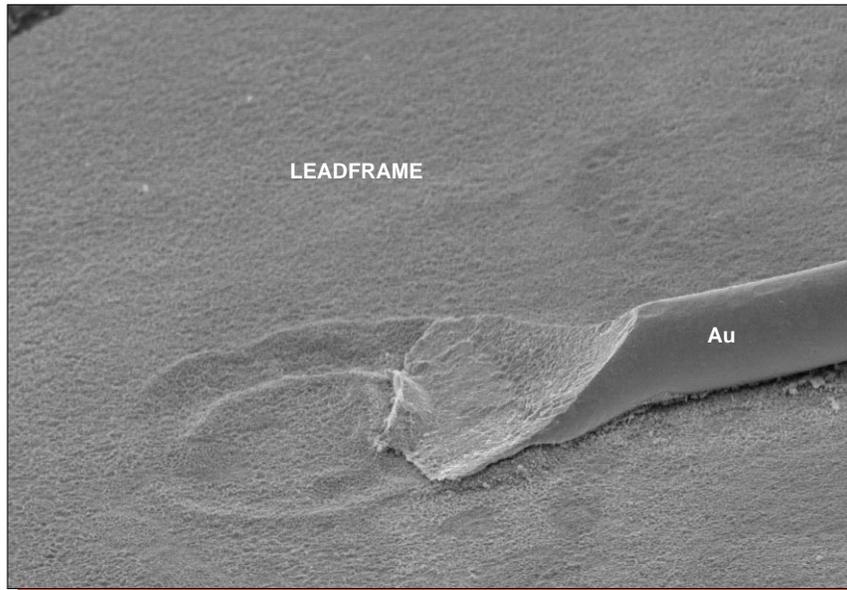


top view

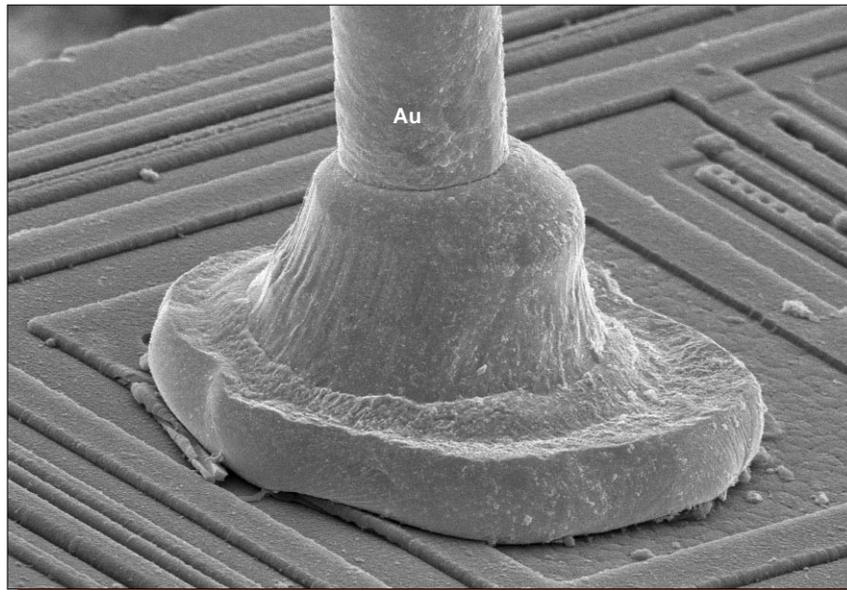


side view

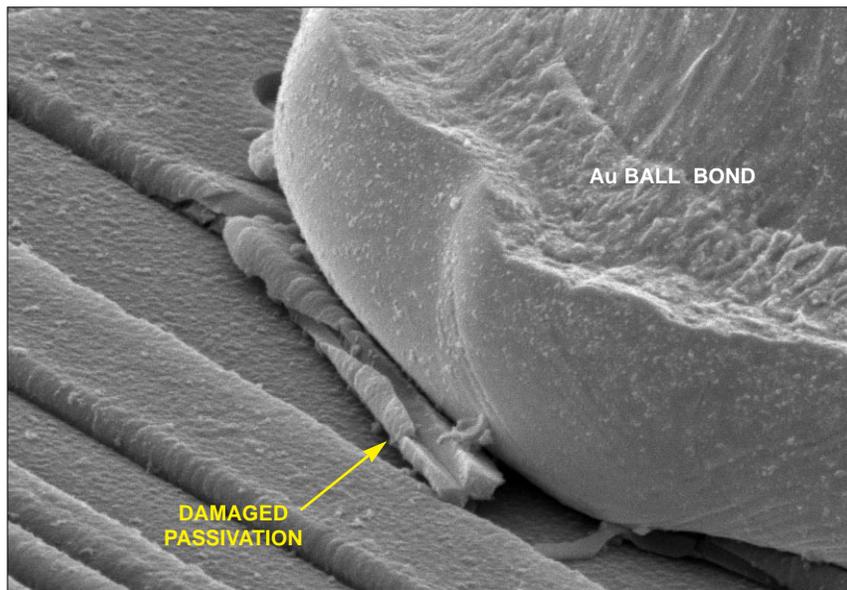
Figure 2. X-ray views of the package. Mag. 8x.



Mag. 500x

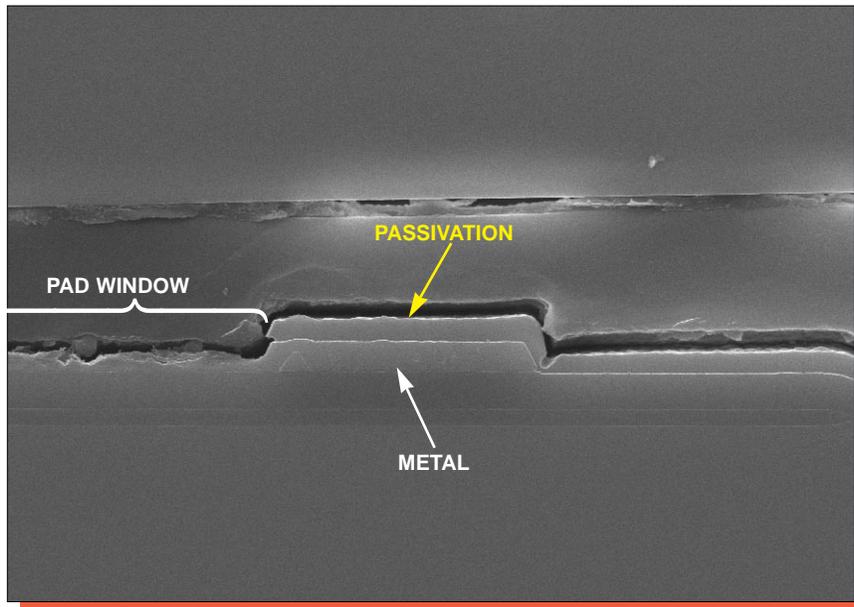


Mag. 900x

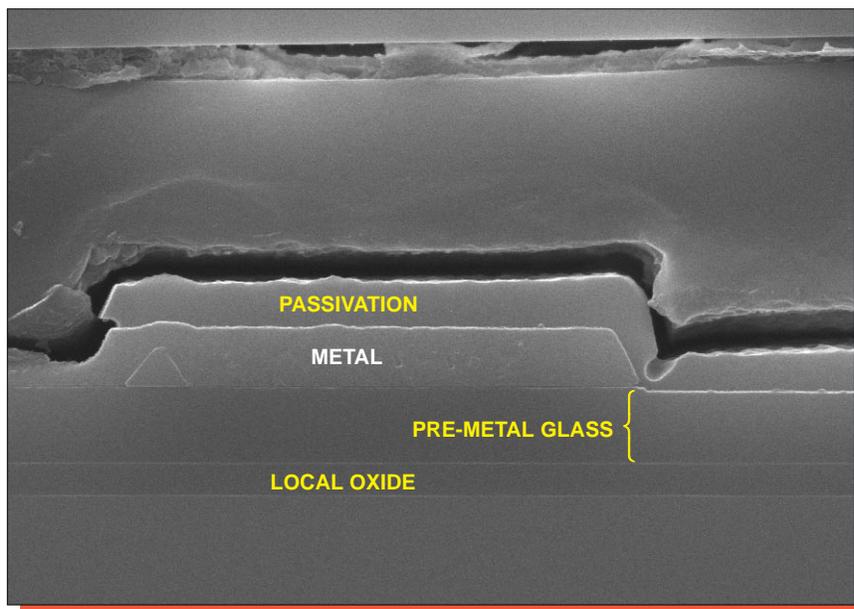


Mag. 2600x

Figure 3. SEM views of typical wirebonds. 60°.

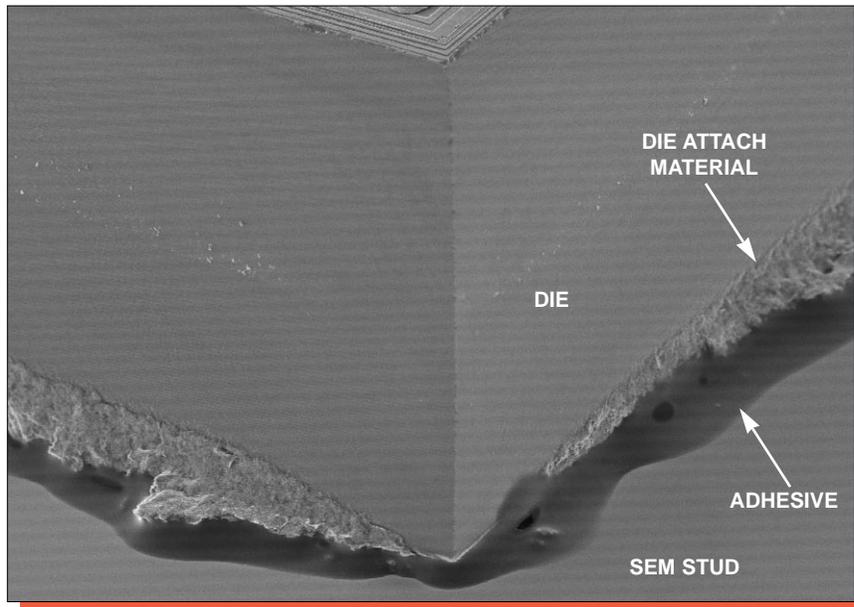


Mag. 3300x

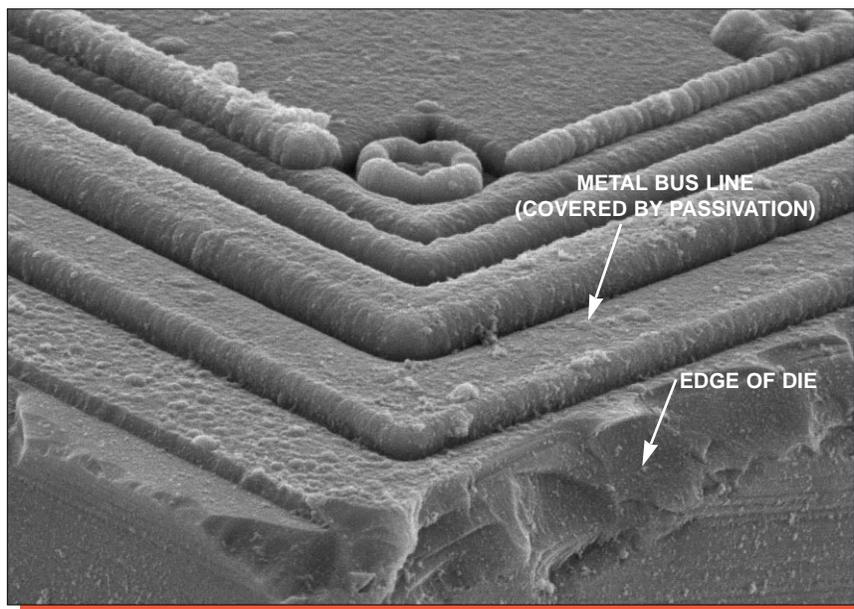


Mag. 6500x

Figure 3a. SEM section views of the bond pad.

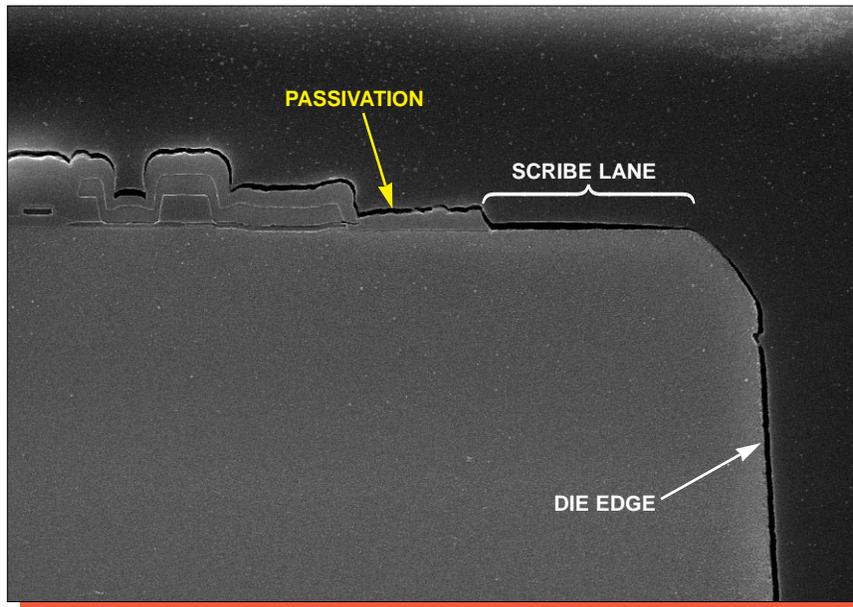


Mag. 100x

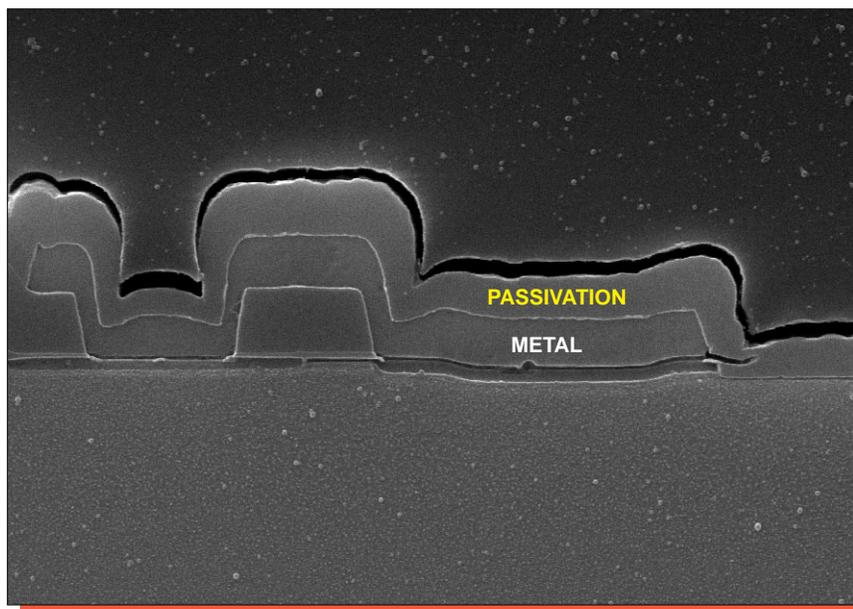


Mag. 2100x

Figure 4. SEM views of die corner and edge seal. 60°.



Mag. 2200x



Mag. 5700x

Figure 5. SEM section views of the edge seal.

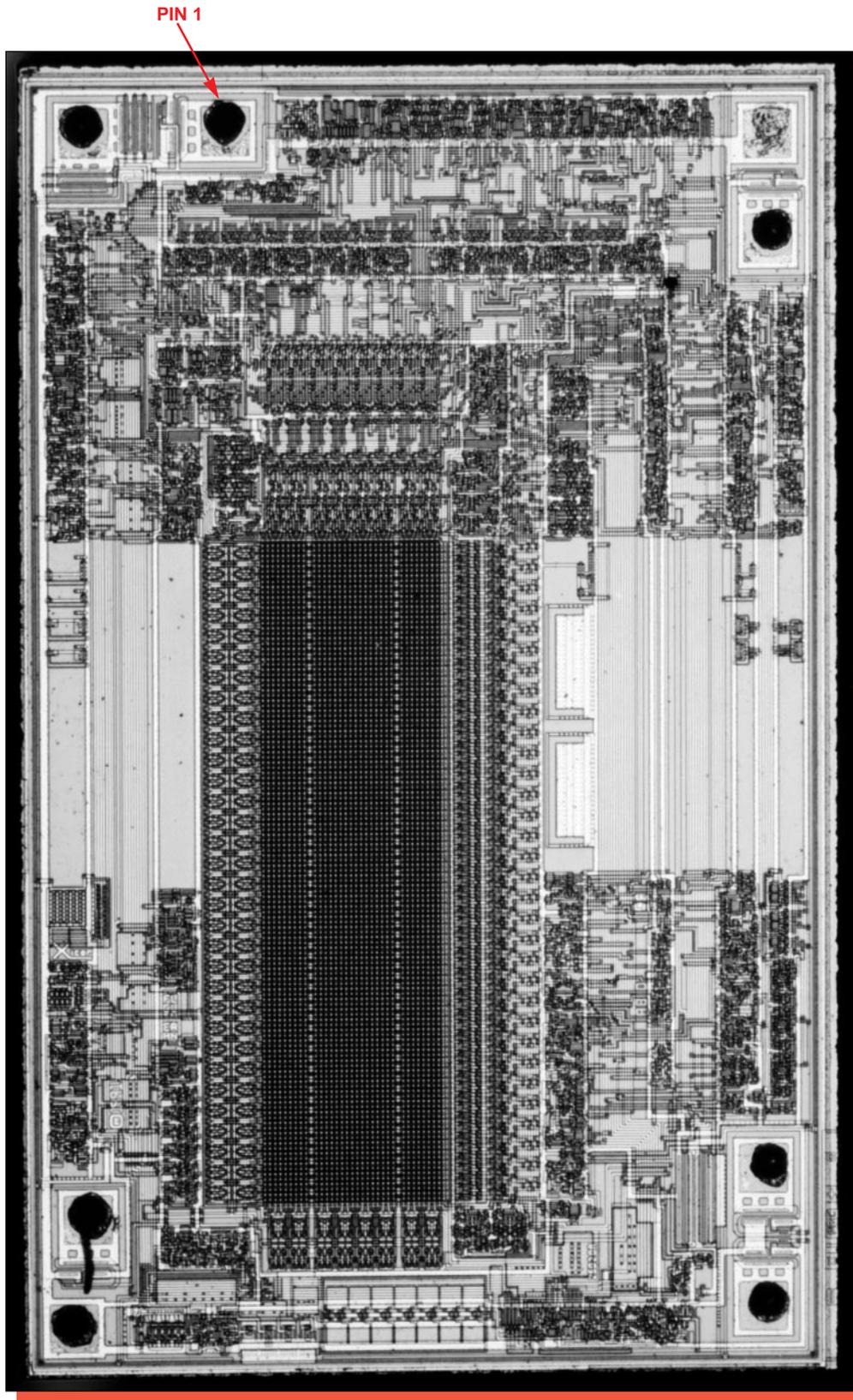


Figure 6. Whole die photograph of the Xicor X25020P 2K EEPROM. Mag. 80x.

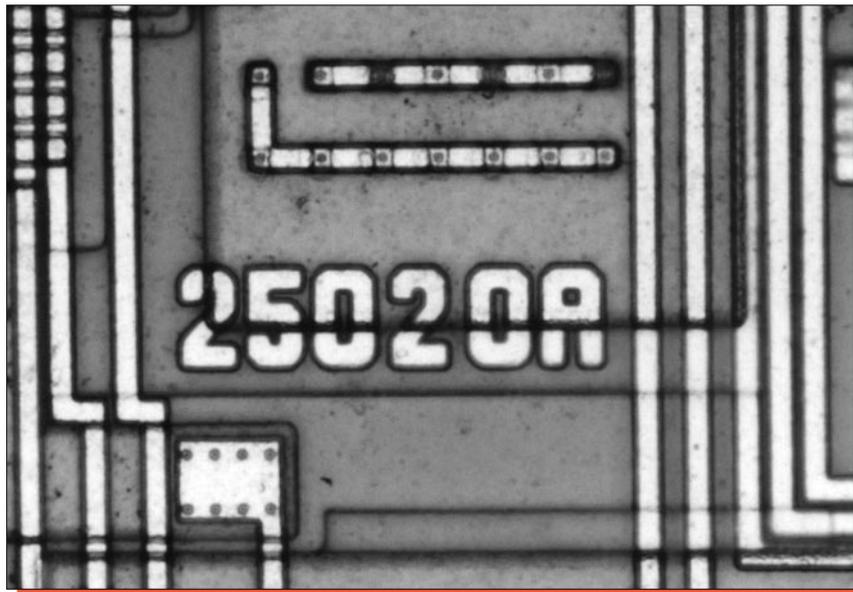
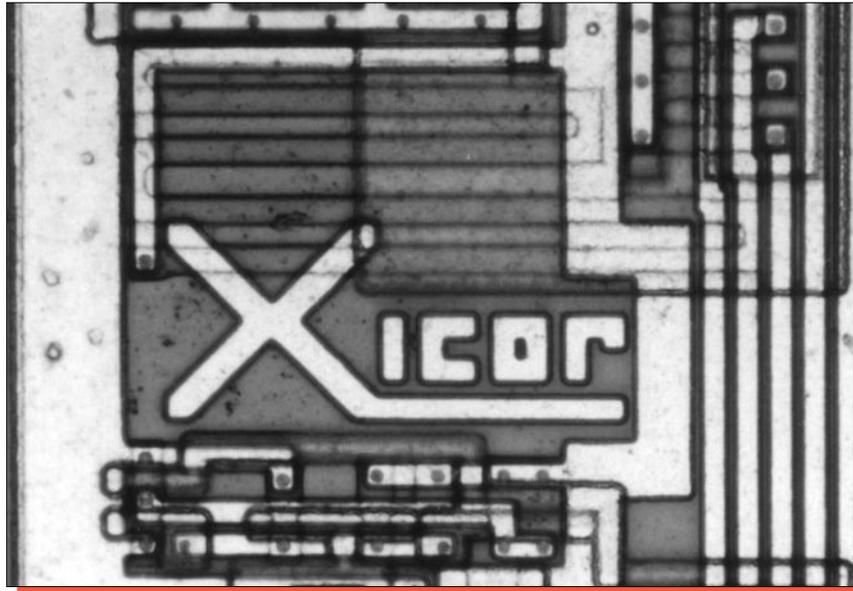
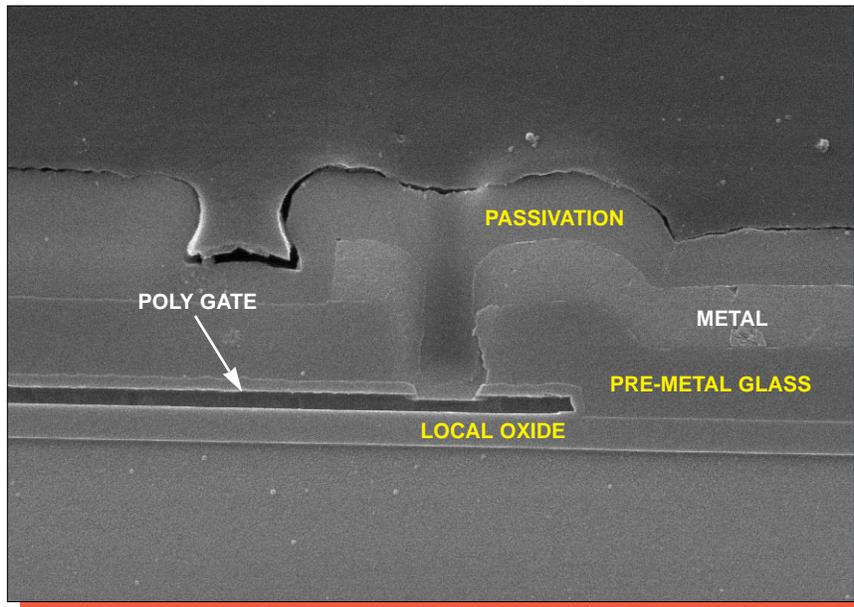
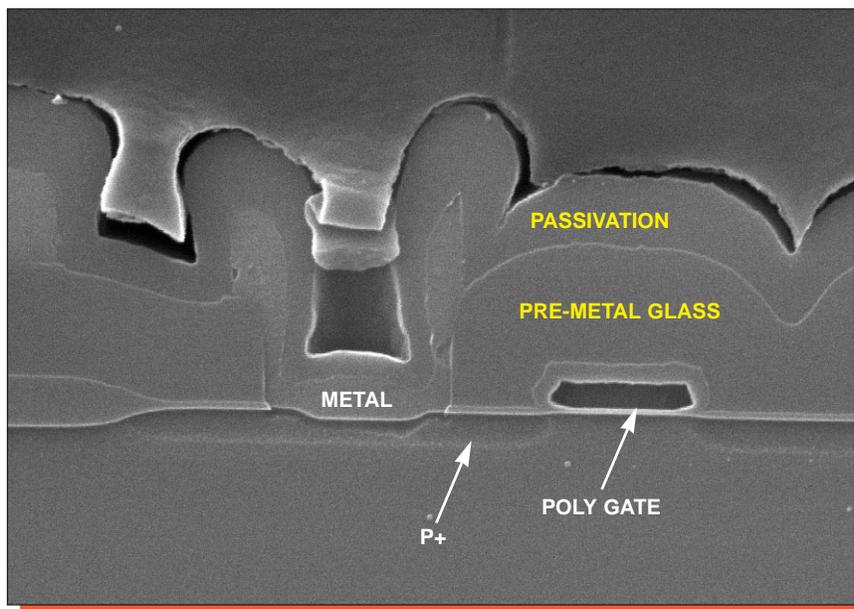


Figure 7. Identification markings from the die surface. Mag. 800x.

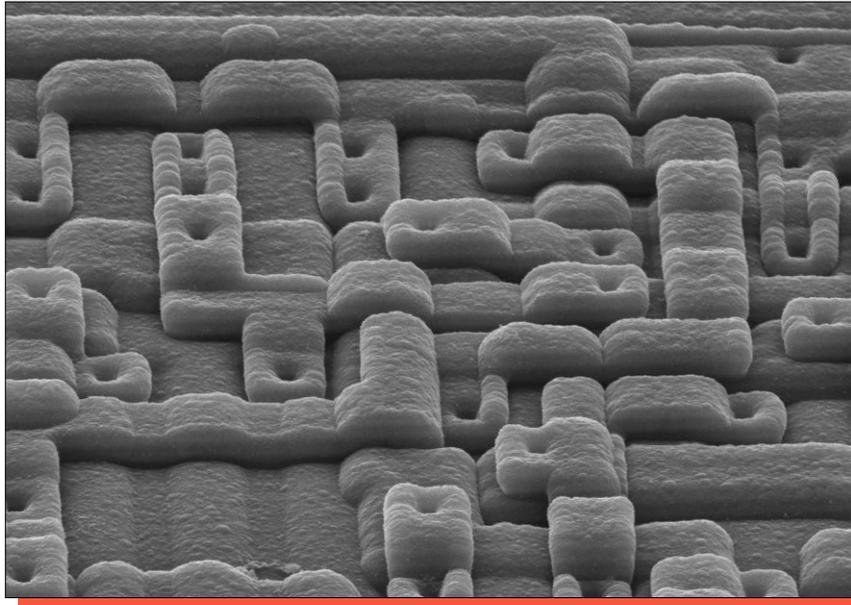


Mag. 6500x

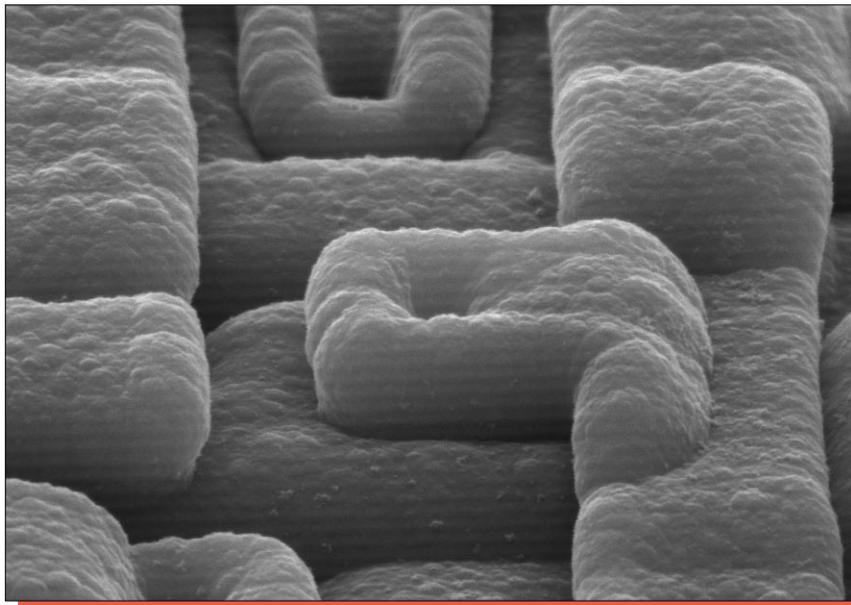


Mag. 10,000x

Figure 8. SEM section views of general device structure.

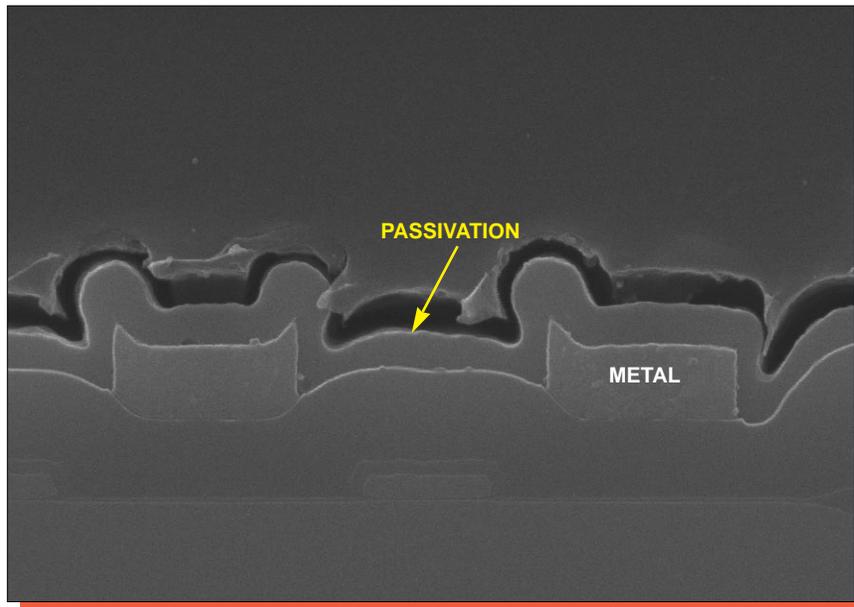


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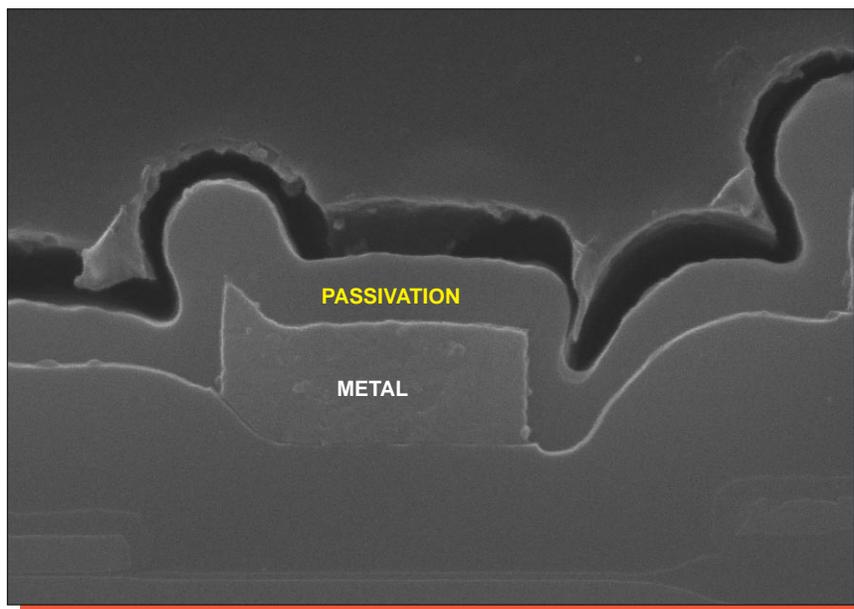


Mag. 8000x

Figure 9. SEM views of overlay passivation coverage. 60°.

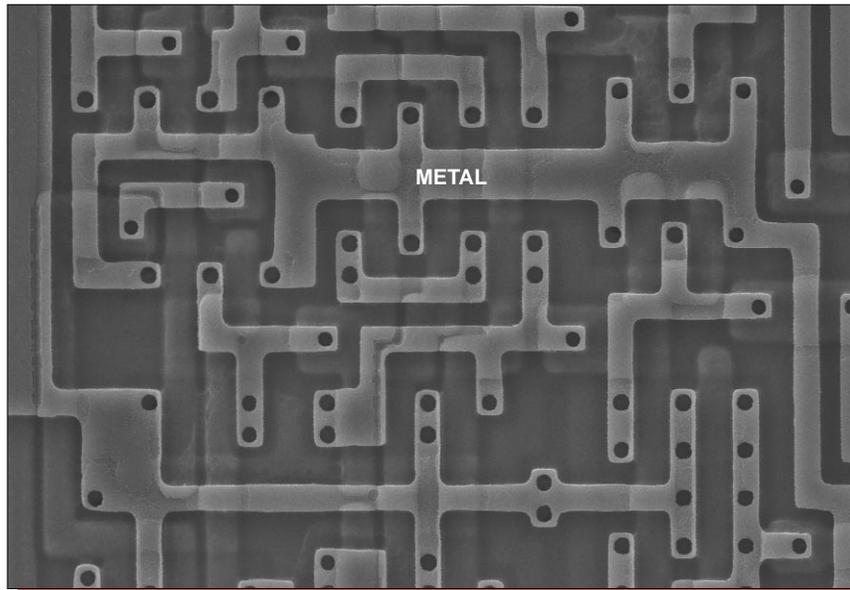


Mag. 8000x

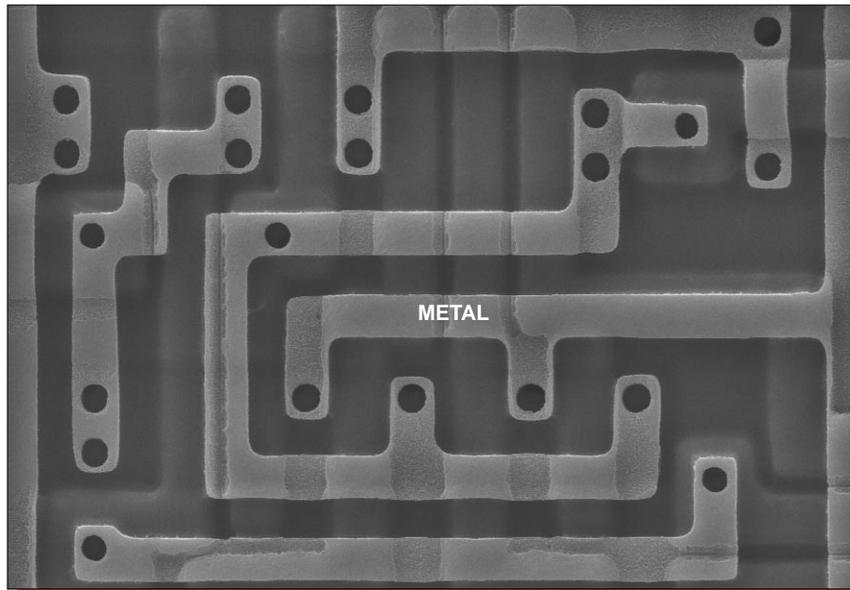


Mag. 13,000x

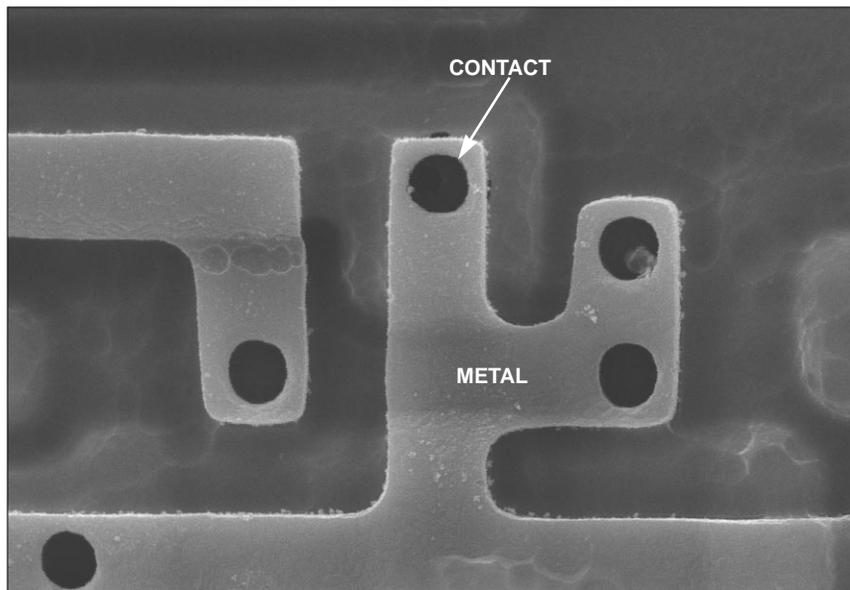
Figure 10. SEM section views of metal line profiles.



Mag. 1200x

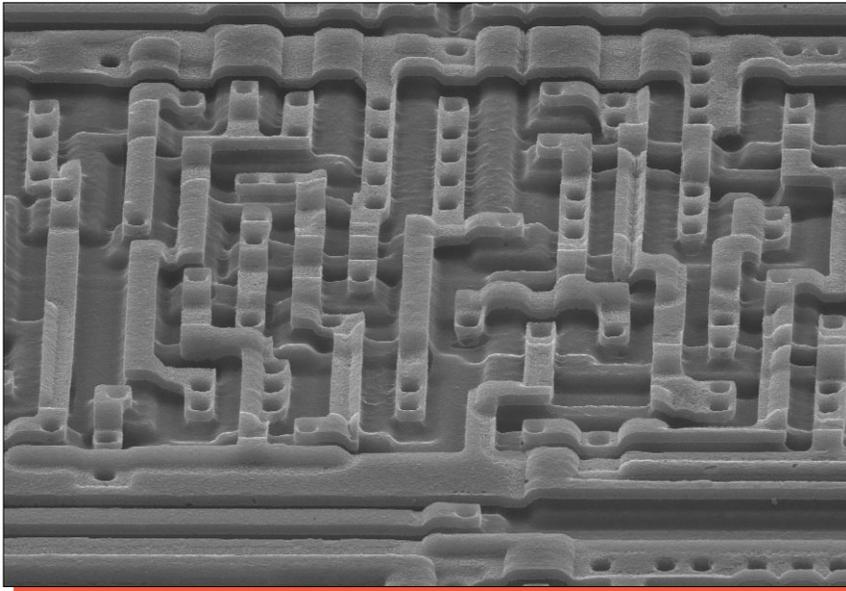


Mag. 2000x

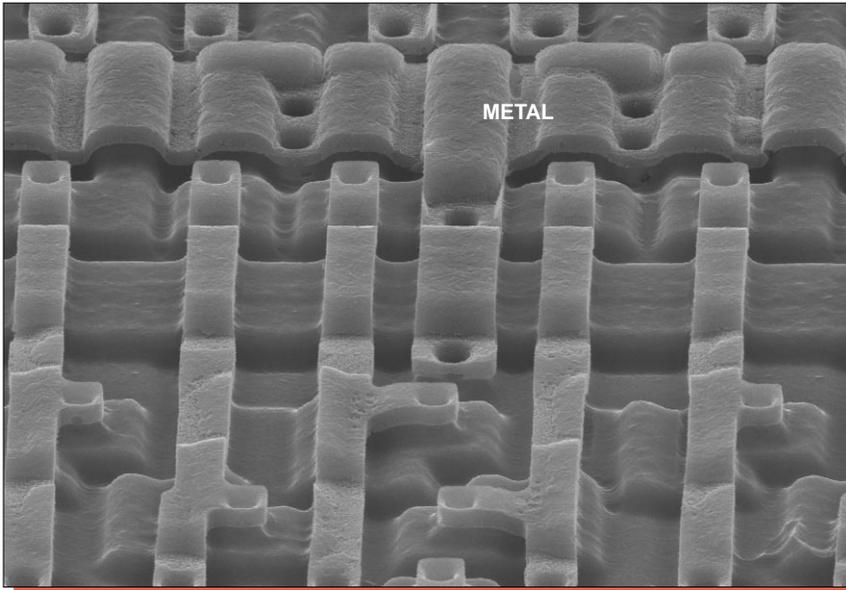


Mag. 5000x

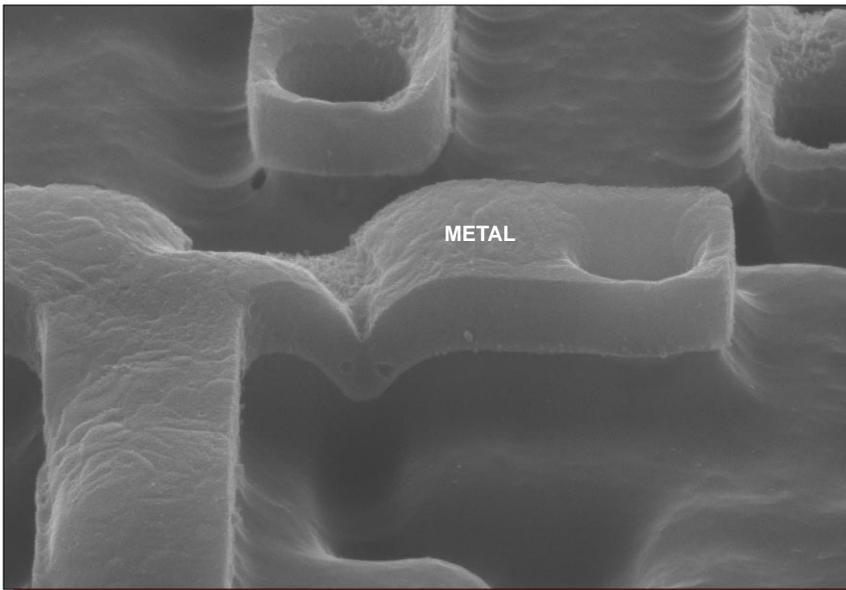
Figure 11. Topological SEM views illustrating metal patterning. 0°.



Mag. 1400x

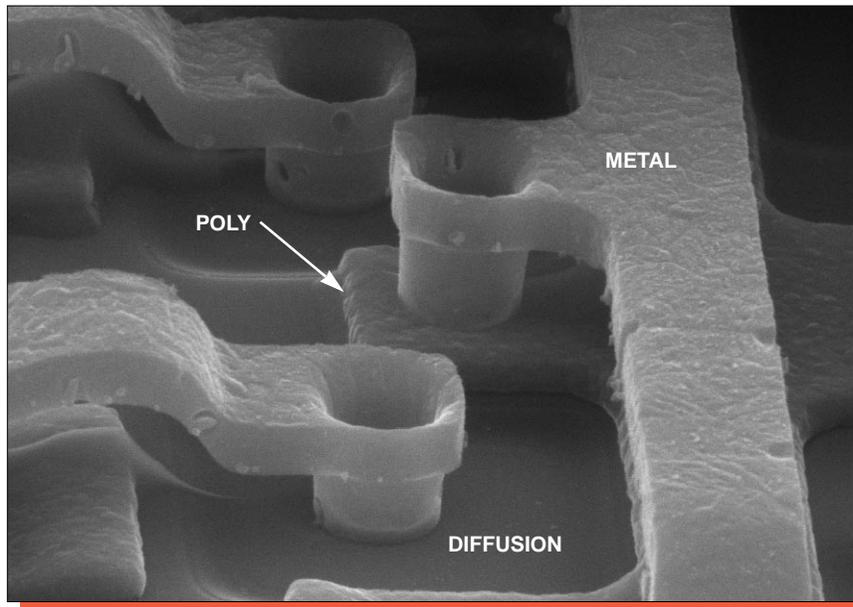


Mag. 2500x

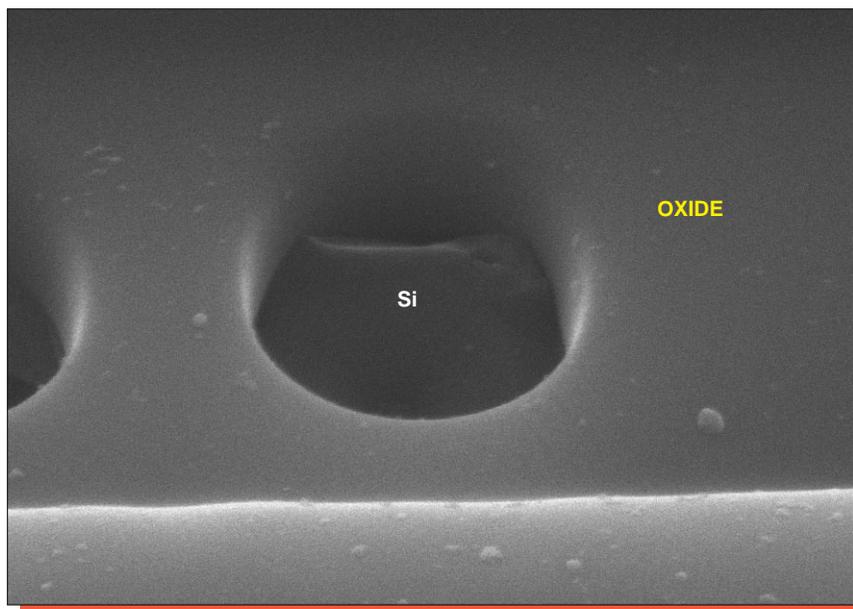


Mag. 10,000x

Figure 12. Perspective SEM views illustrating metal coverage. 60°.

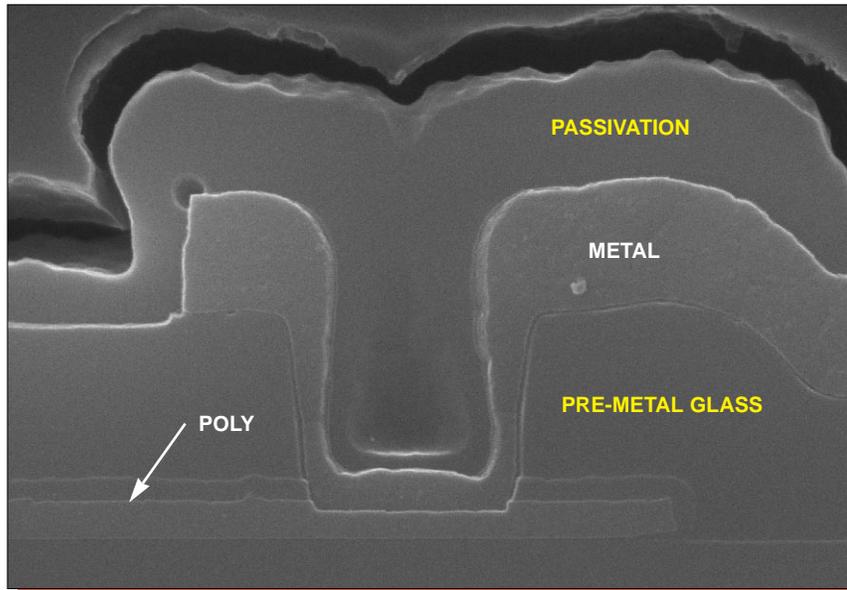


Mag. 8400x, 60°

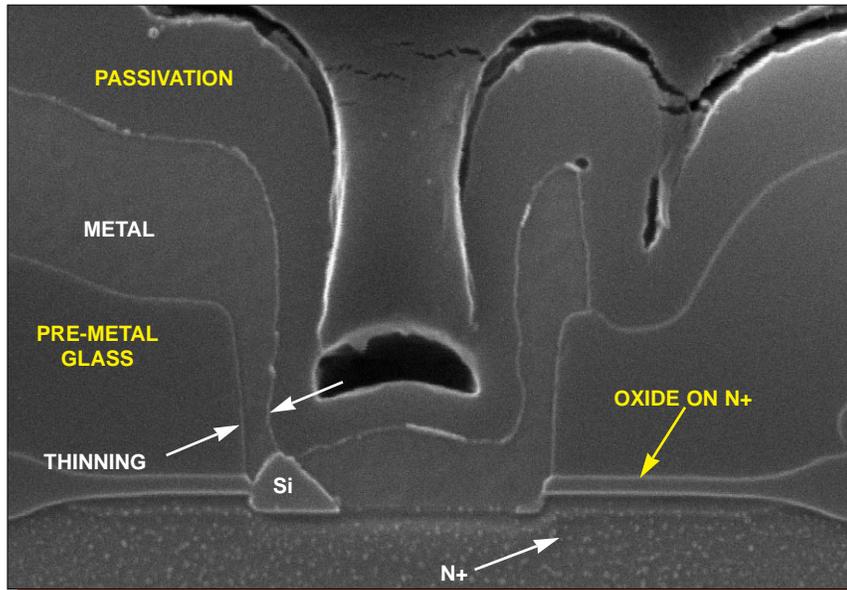


Mag. 19,000x, 45°

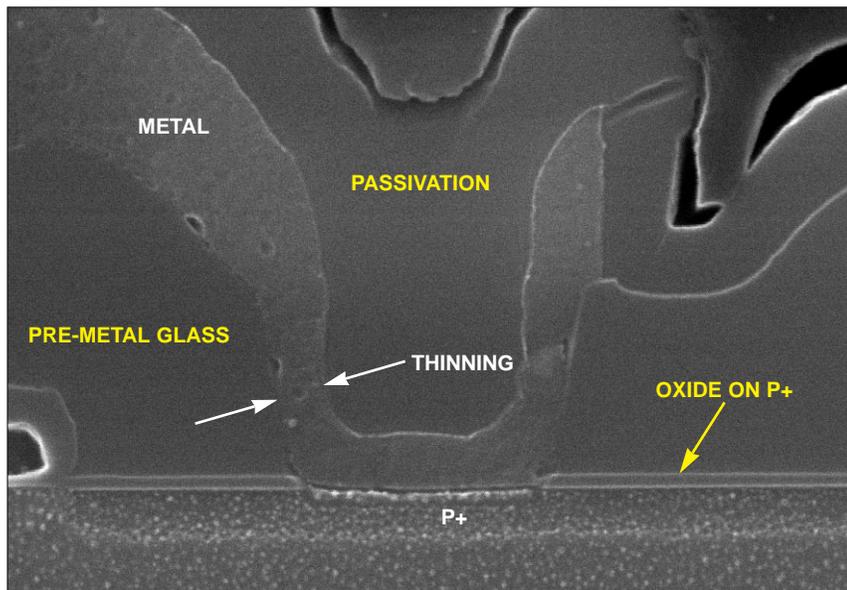
Figure 13. Perspective SEM views of metal contacts and contact cut.



metal-to-poly,  
glass-etch,  
Mag. 13,000x

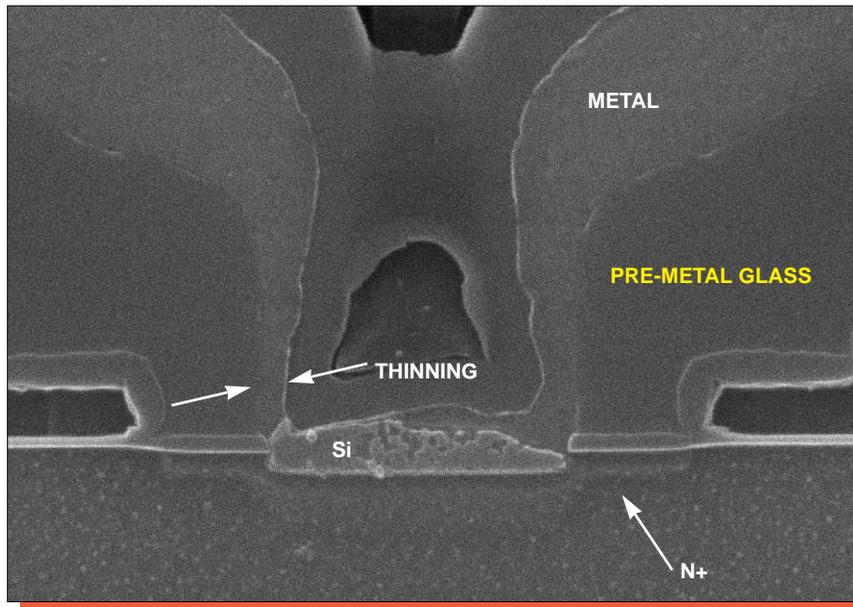


metal-to-N+,  
Mag. 18,000x

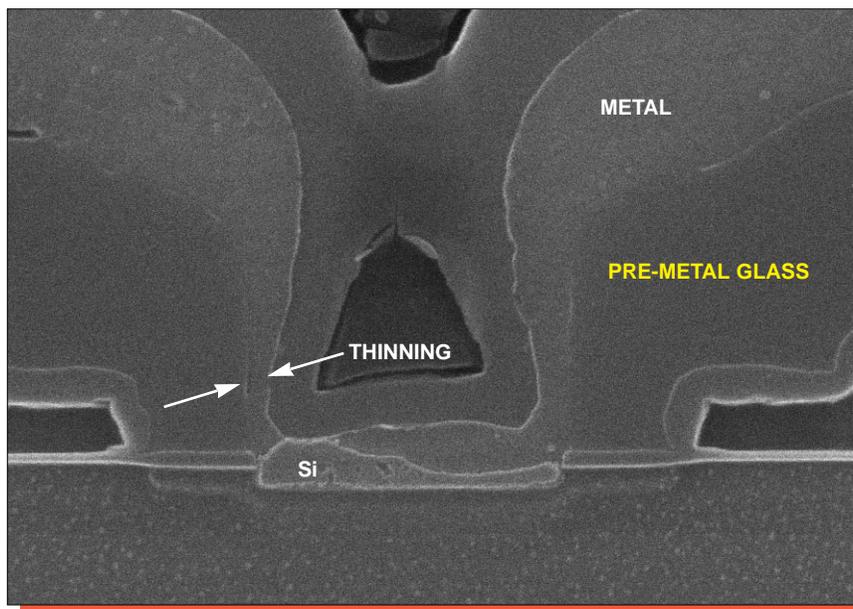


metal-to-P+,  
Mag. 20,000x

Figure 14. SEM section views of typical metal contacts.

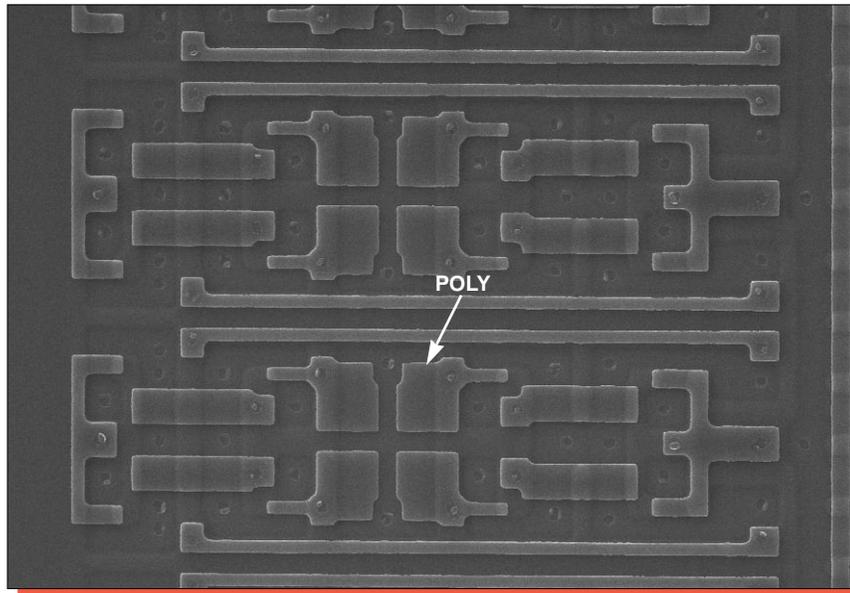


metal-to-N+

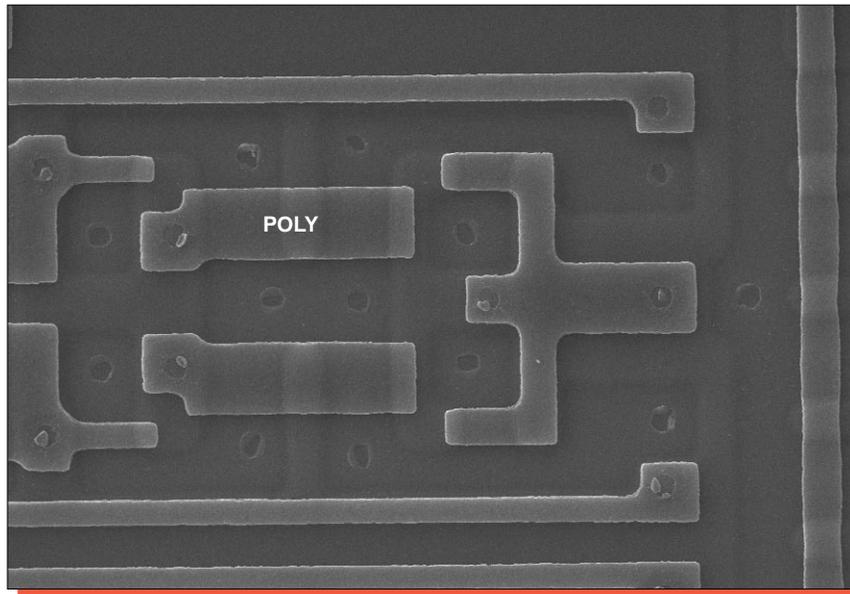


metal-to-N+

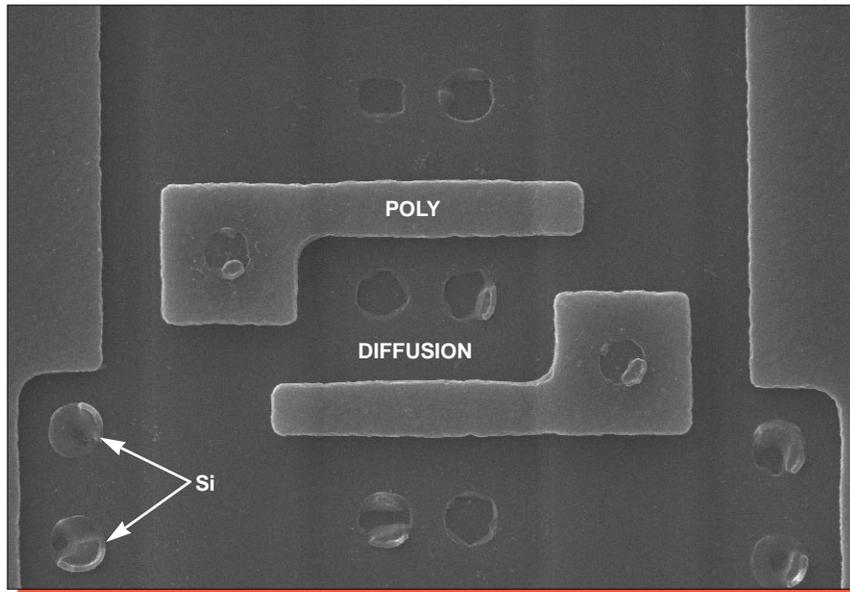
Figure 15. SEM section views illustrating silicon mound growth. Mag. 20,000x.



Mag. 800x

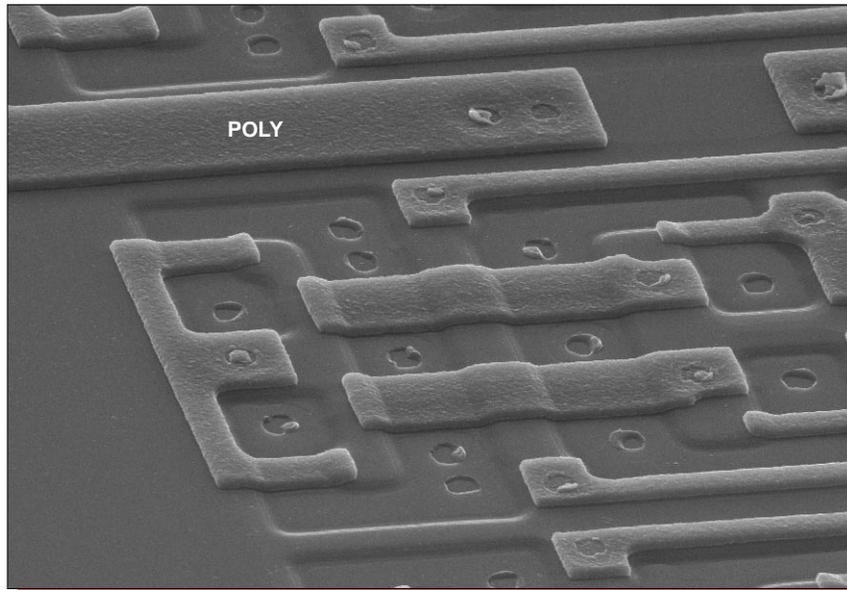


Mag. 1600x

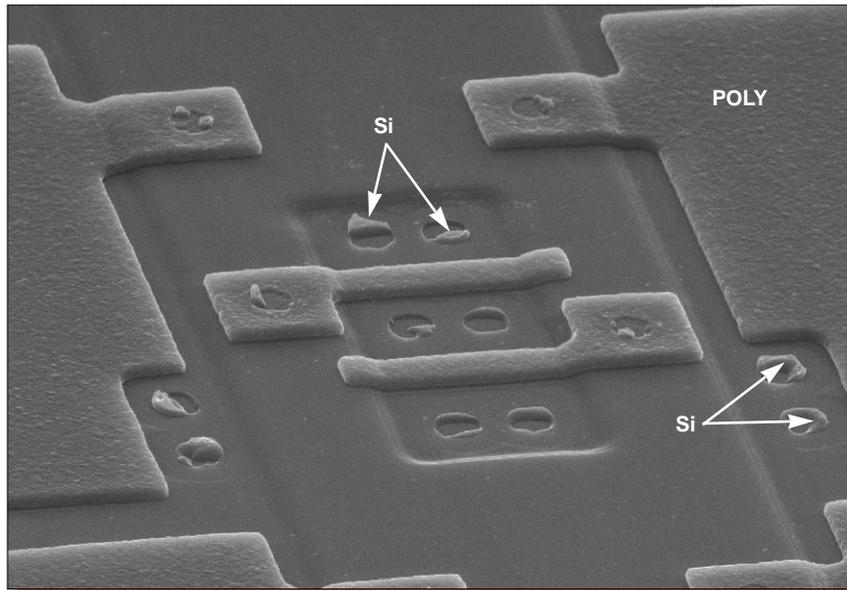


Mag. 3300x

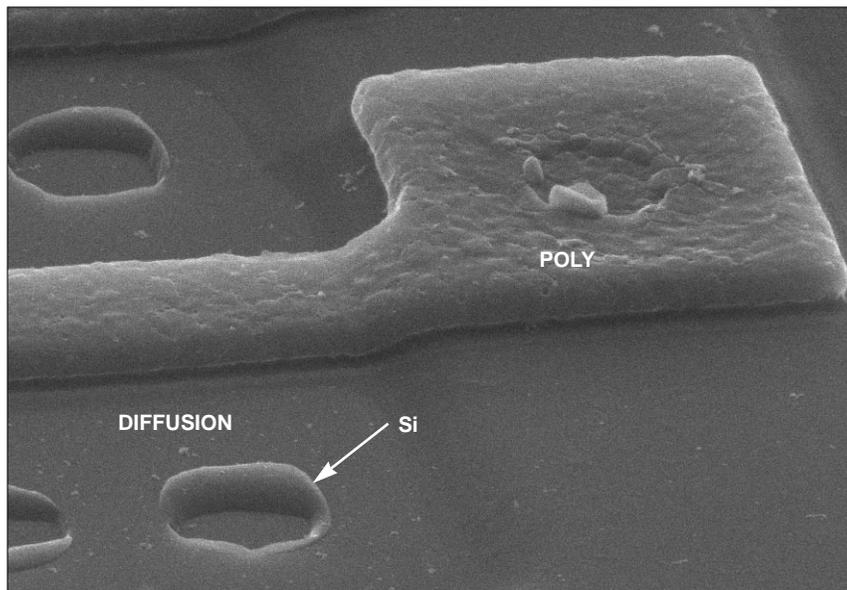
Figure 16. Topological SEM views illustrating poly patterning. 0°.



Mag. 2500x

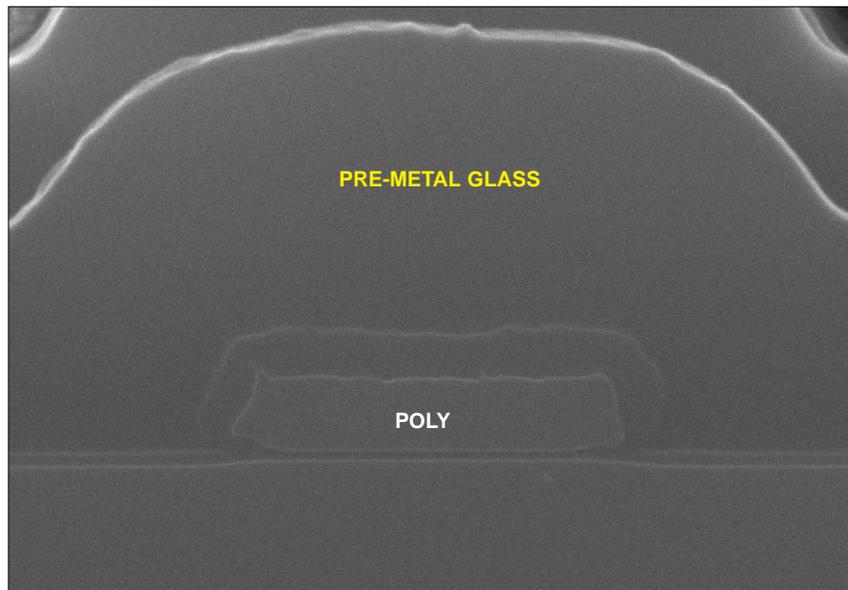


Mag. 3000x

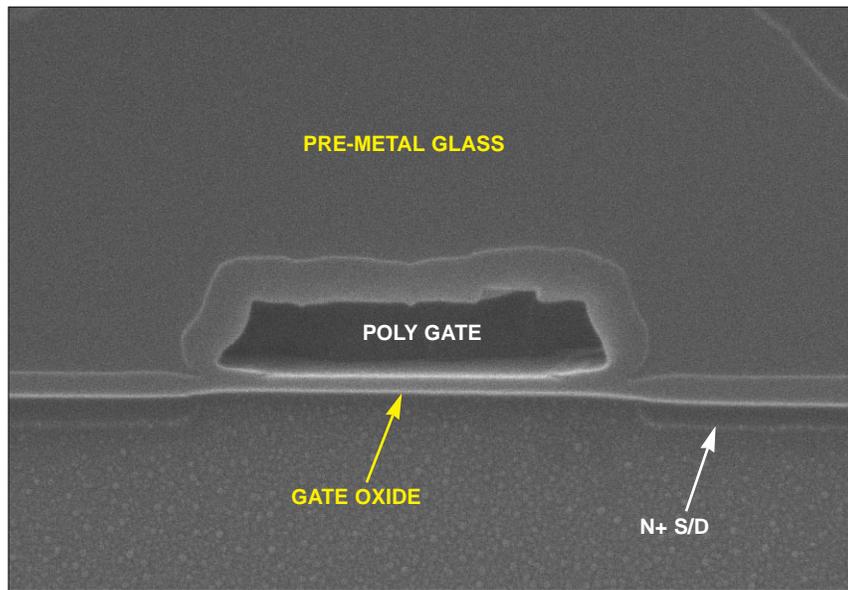


Mag. 10,000x

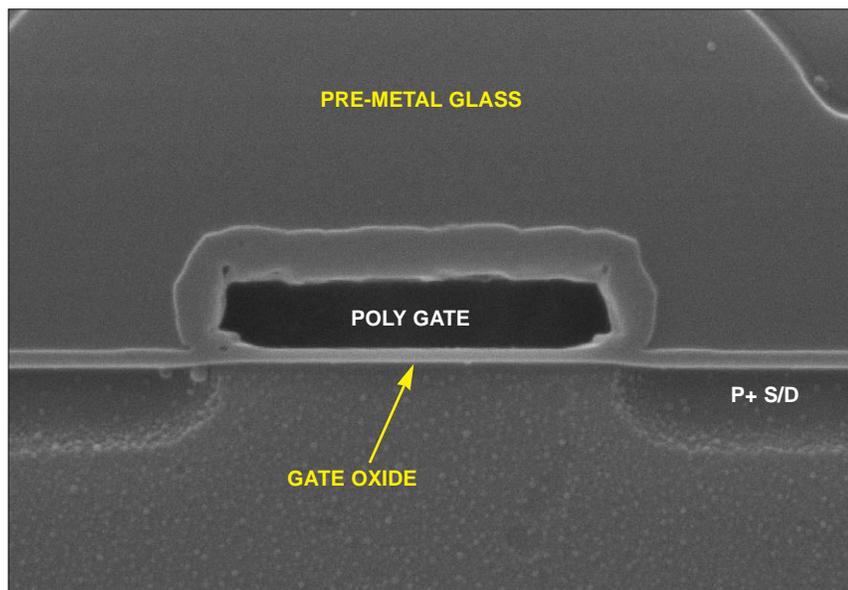
Figure 17. Perspective SEM views illustrating poly coverage. 60°.



glass-etch

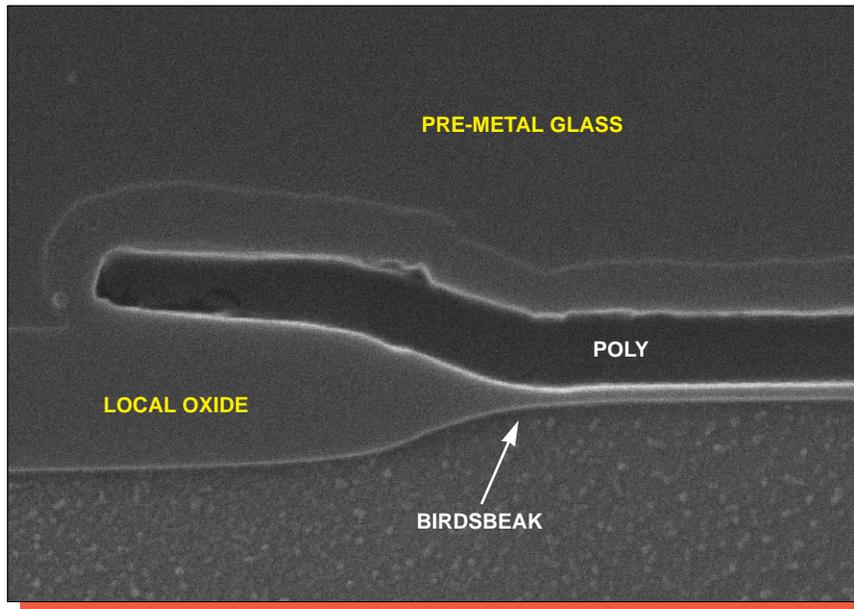


N-channel,  
silicon-etch

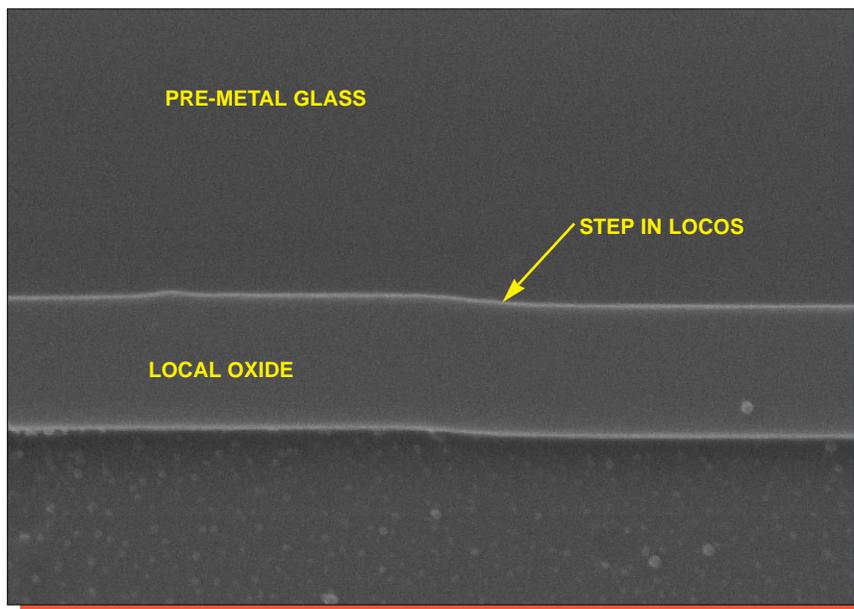


P-channel,  
silicon-etch

Figure 18. SEM section views of typical transistors. Mag. 26,000x.



Mag. 27,000x



Mag. 26,000x

Figure 19. SEM section views of a local oxide birdsbeak and step in the local oxide.

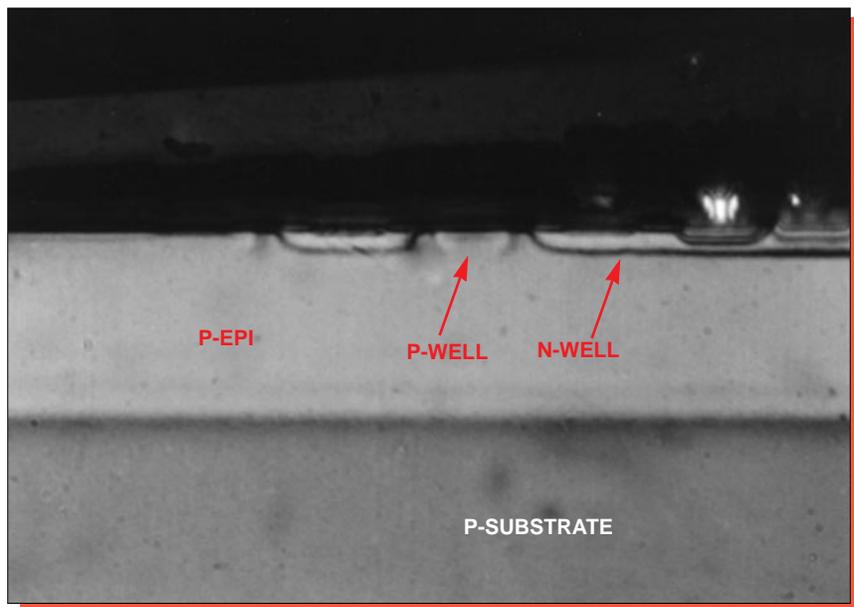
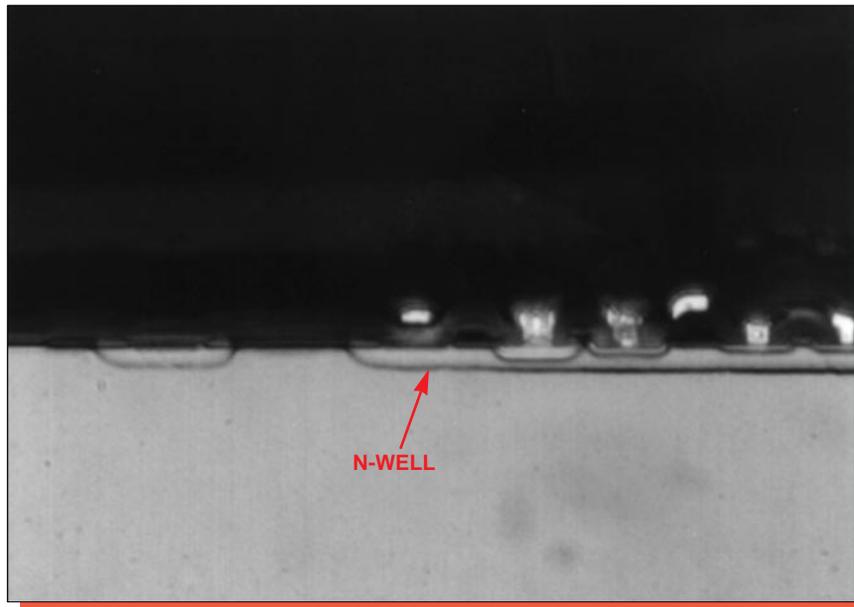
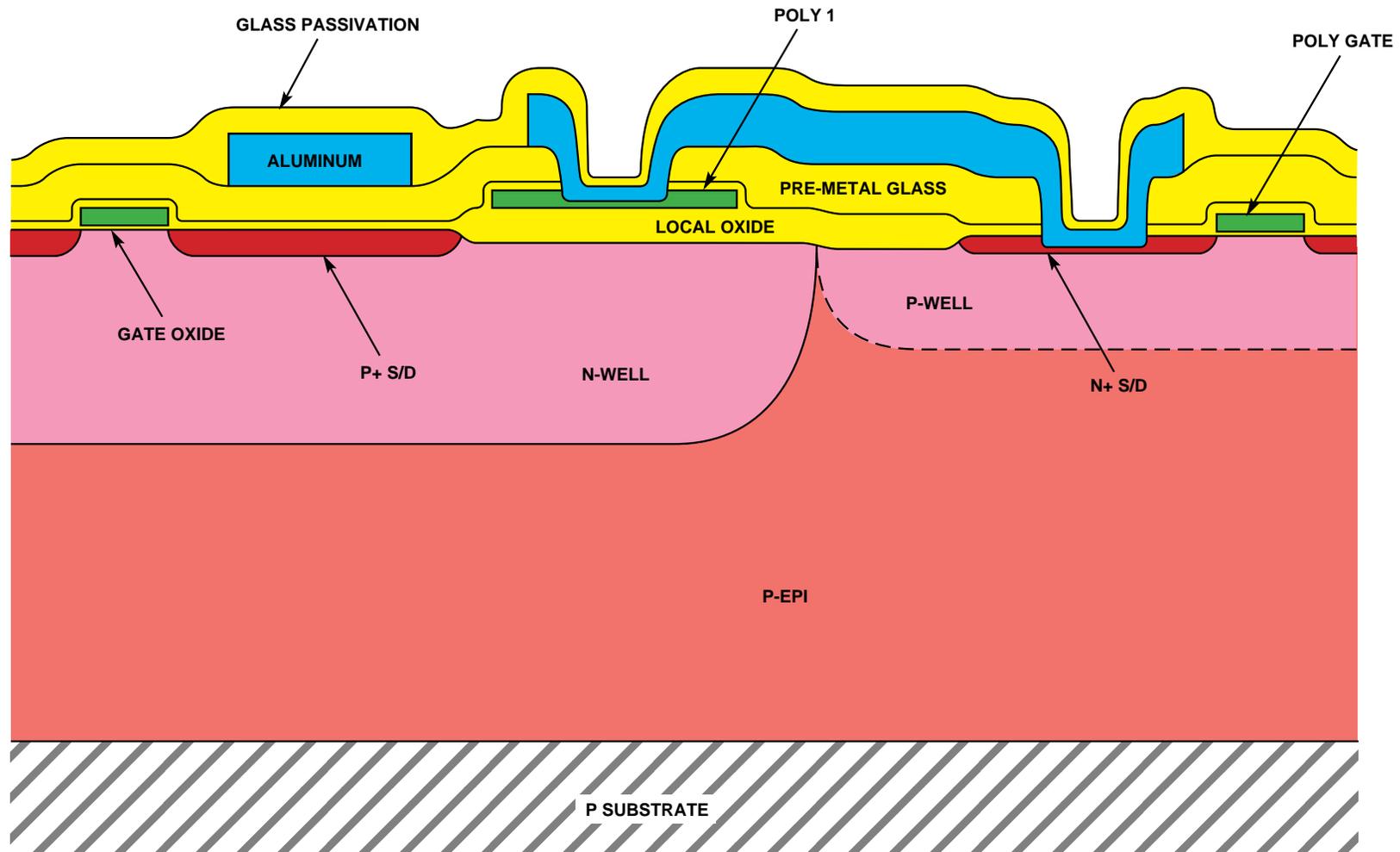


Figure 20. Optical views of the well structure. Mag. 1600x.



Blue = Metal, Yellow = Oxide, Green = Poly,  
Red = Diffusion, and Gray = Substrate

Figure 20a. Color cross section drawing illustrating device structure.

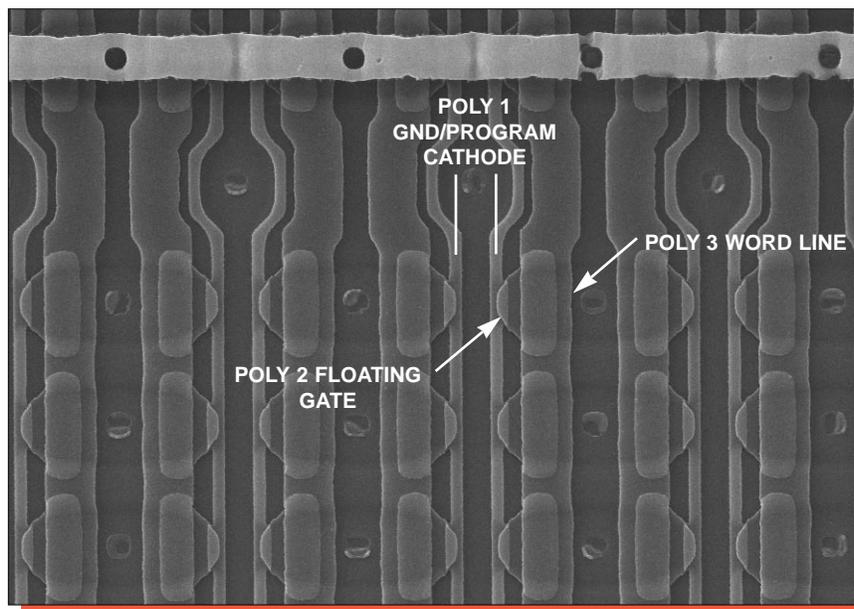
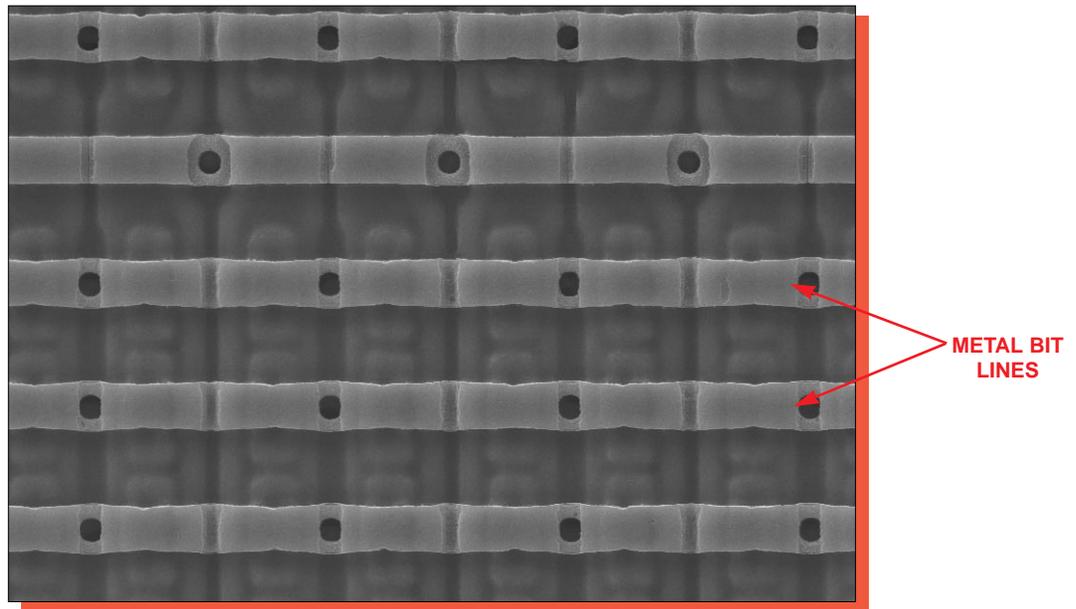


Figure 21. Topological SEM views of the Xicor EEPROM cell array. Mag. 1600x, 0°.

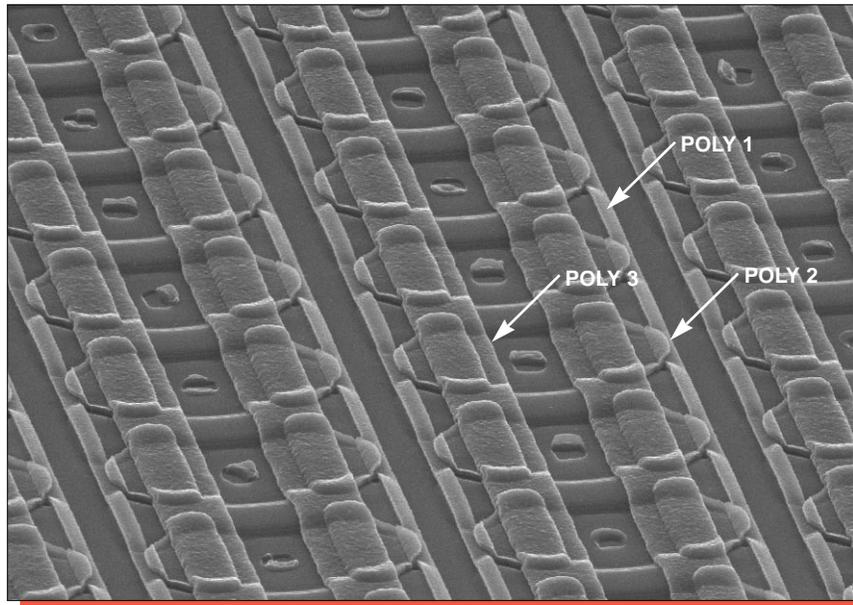
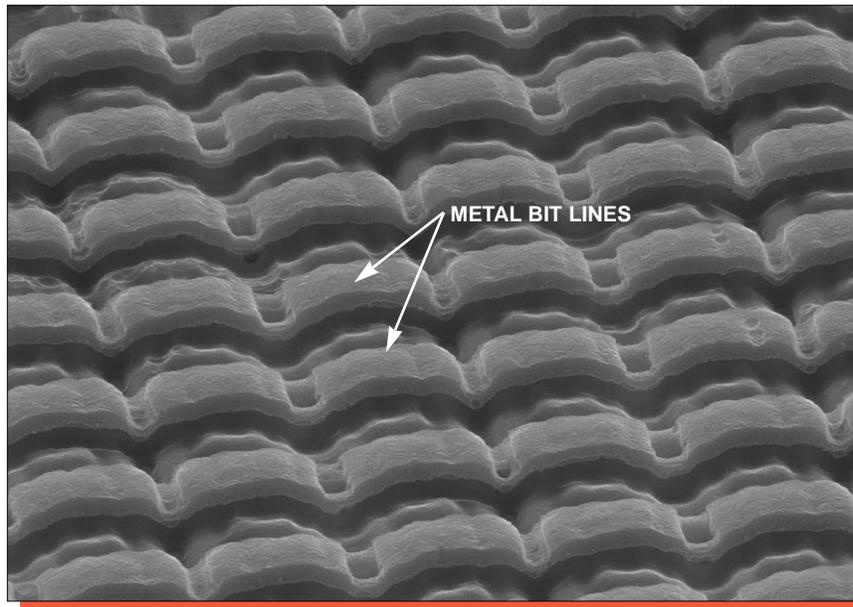


Figure 22. Perspective SEM views of the Xicor 25020P EEPROM cell array.  
Mag. 2500x, 60°.

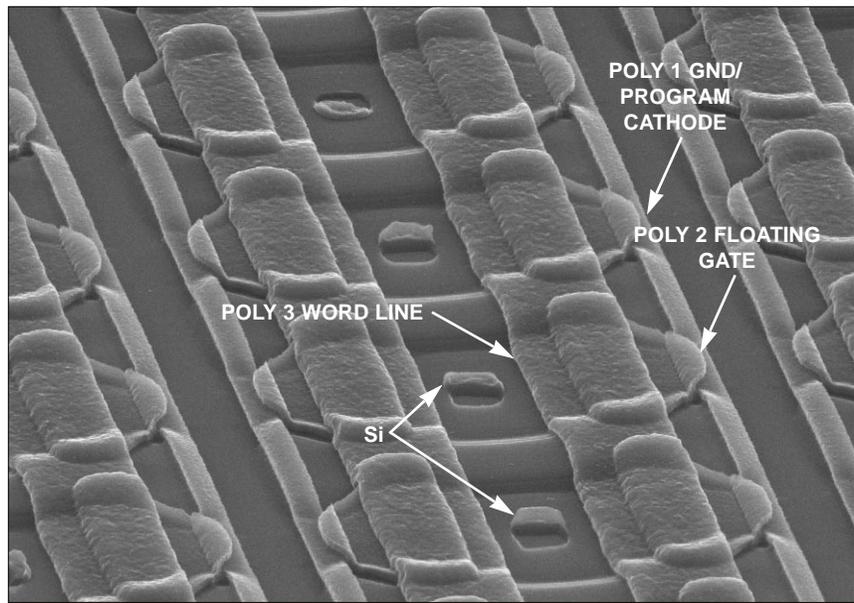
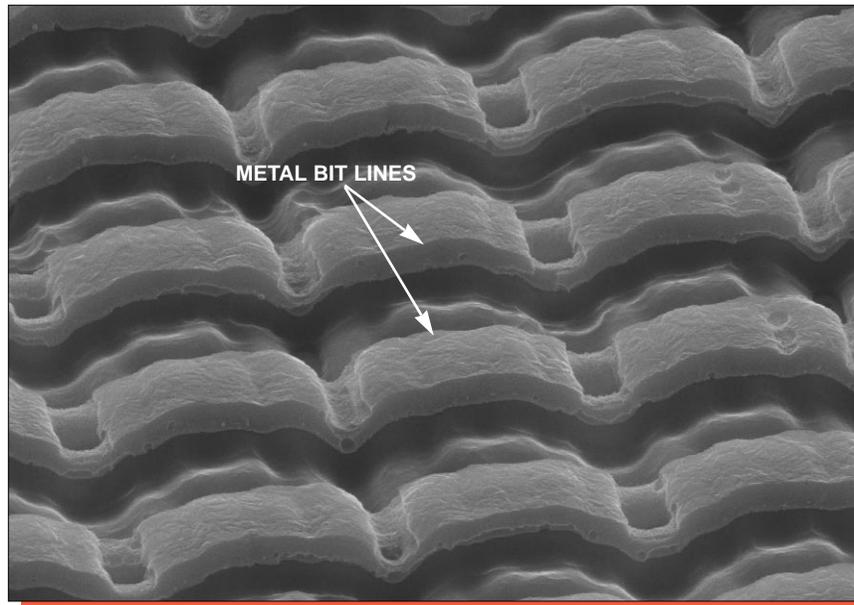
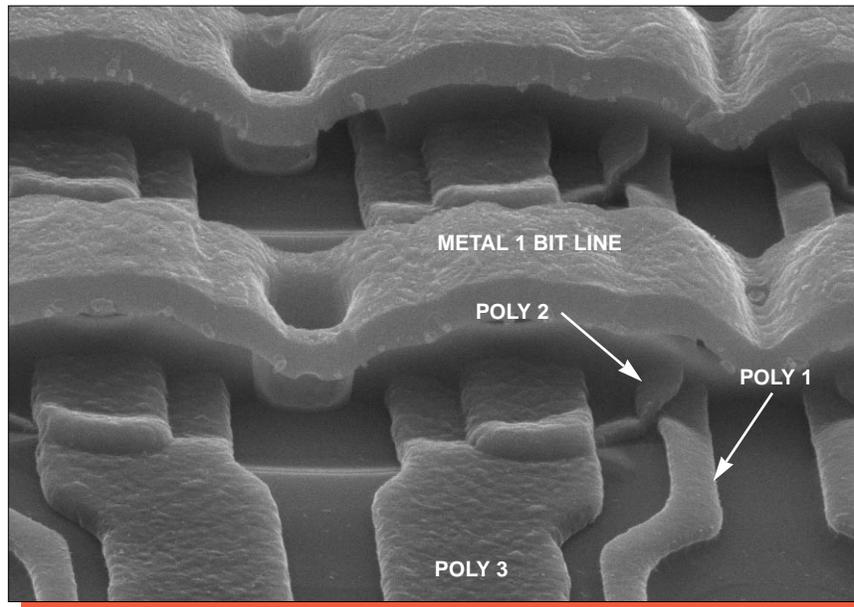
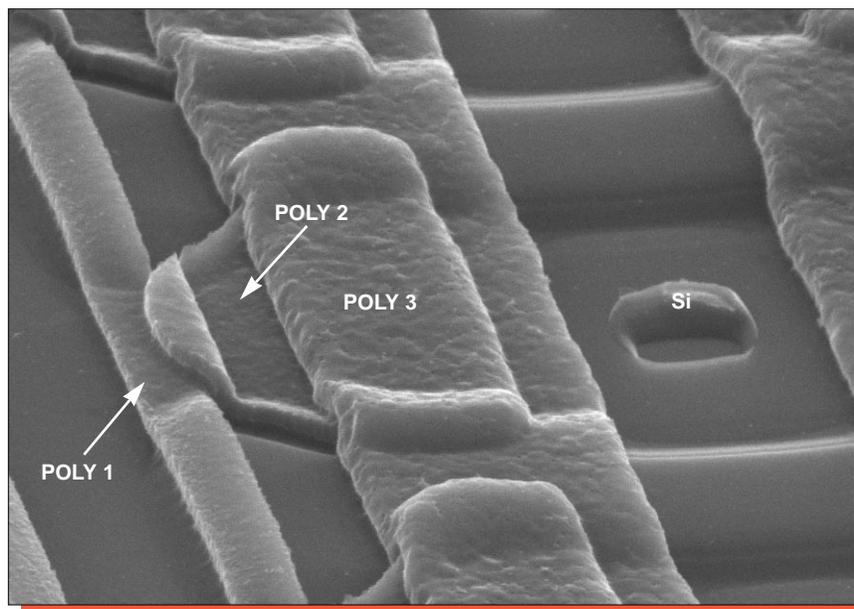


Figure 23. Additional perspective SEM views of the Xicor EEPROM cell array.  
Mag. 4000x, 60°.



Mag. 6500x



Mag. 10,000x

Figure 24. Detailed views of the EEPROM cell. 60°.

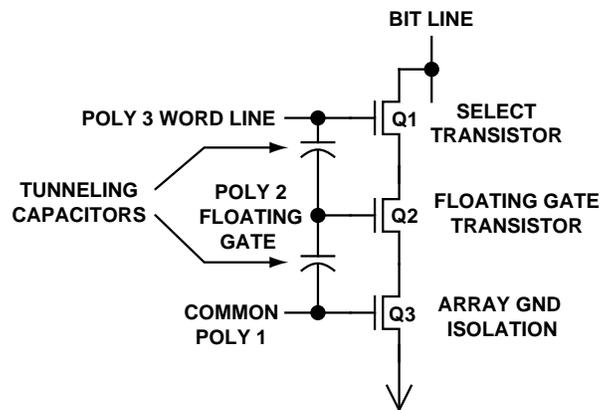
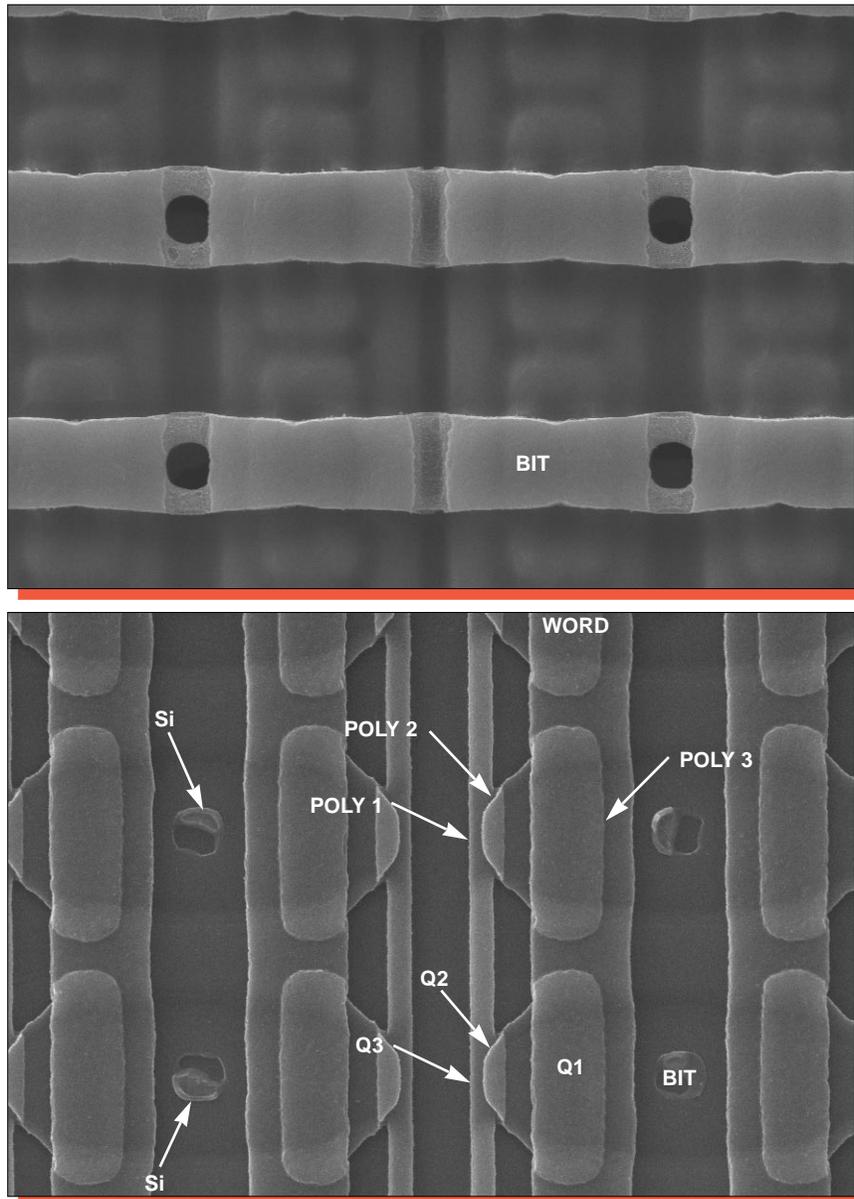
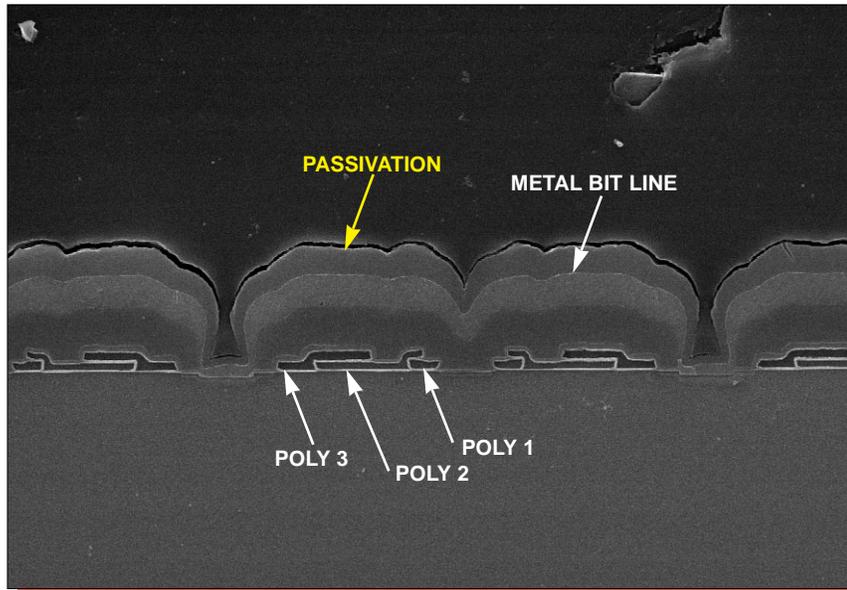
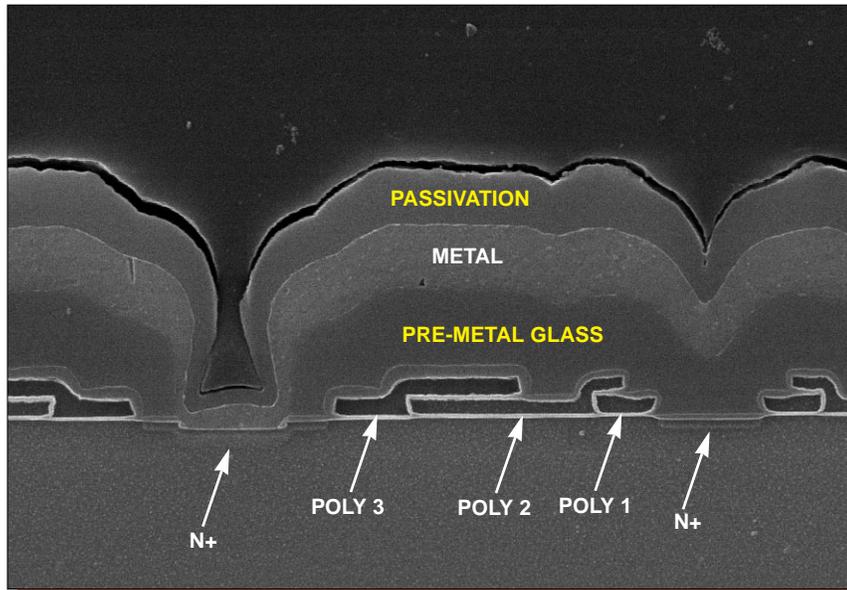


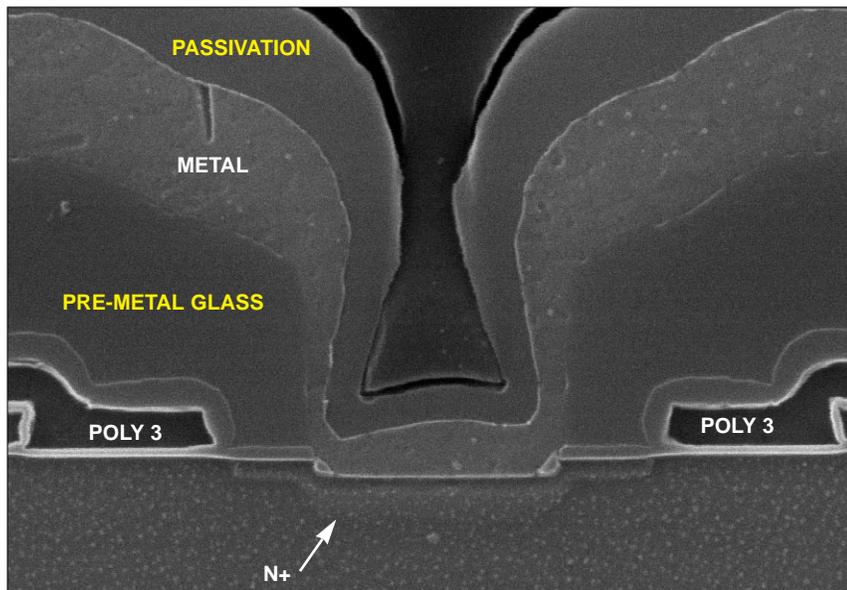
Figure 25. Topological SEM views and schematic of the EEPROM memory cell.  
Mag. 3300x, 0°.



Mag. 3300x

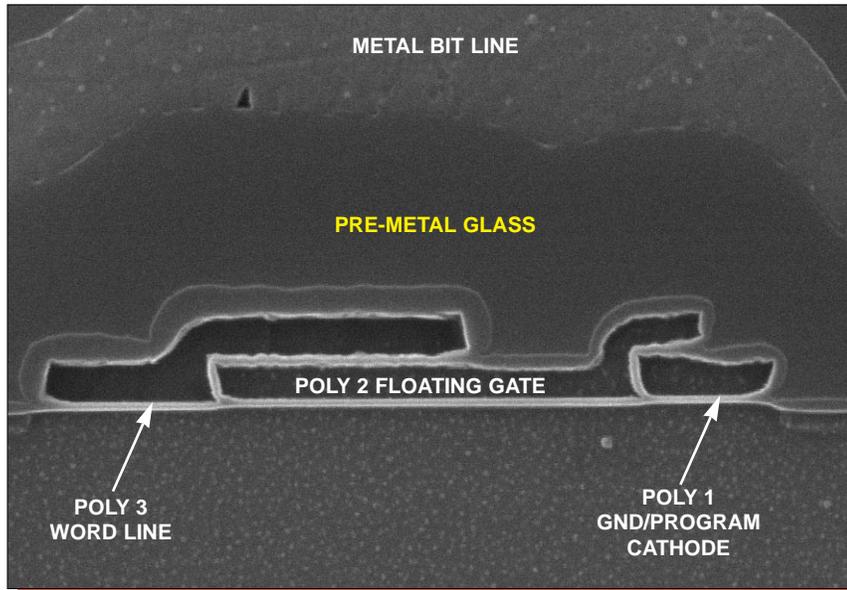


Mag. 6500x

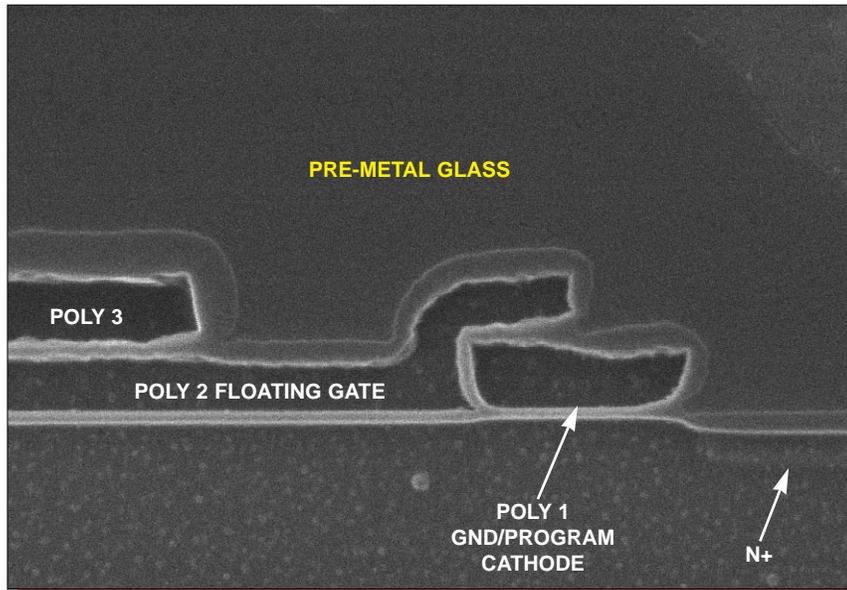


Mag. 15,000x

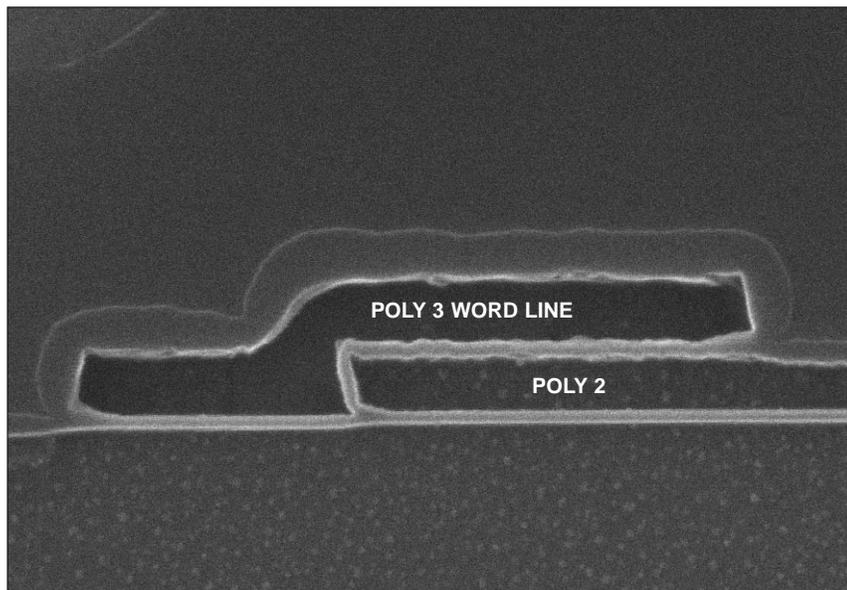
Figure 26. SEM section views illustrating general construction of the EEPRAM array.



Mag. 15,000x

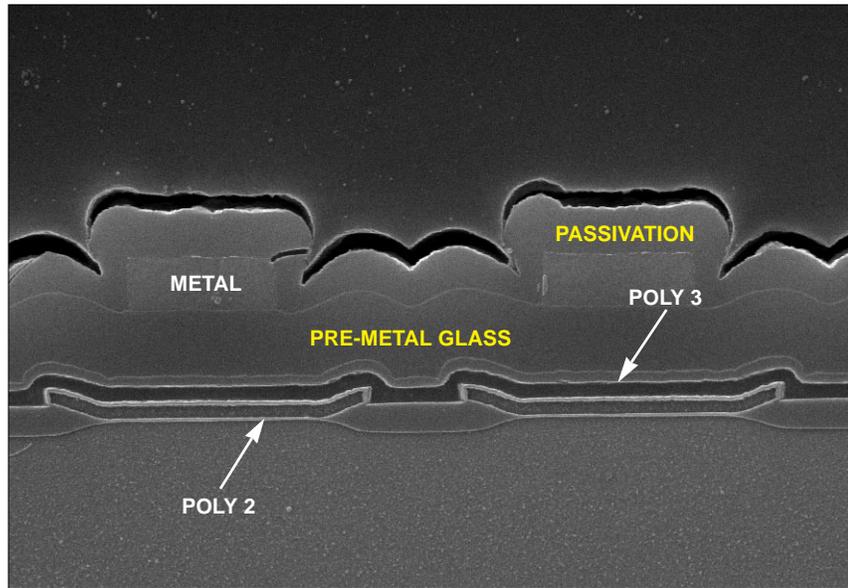


Mag. 25,000x

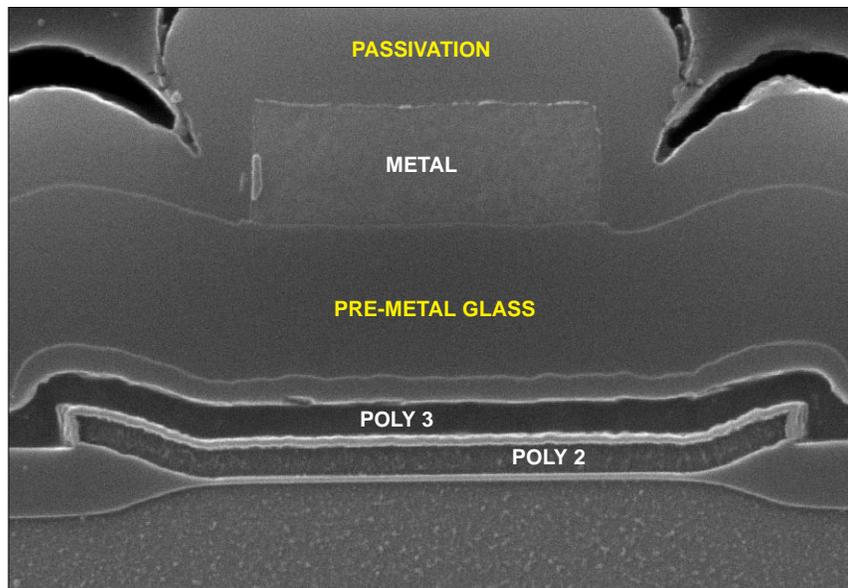


Mag. 25,000x

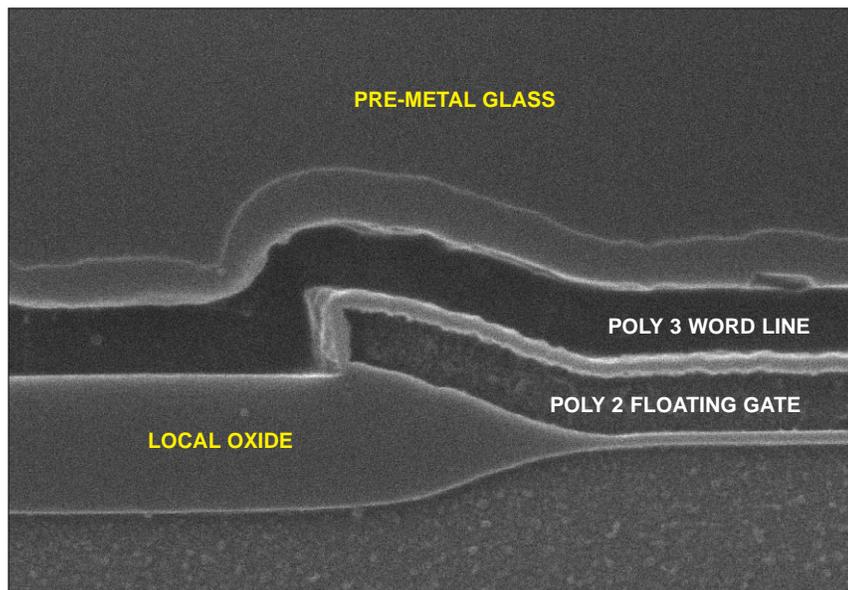
Figure 27. SEM section views illustrating details of the array (parallel to bit line).



Mag. 6000x

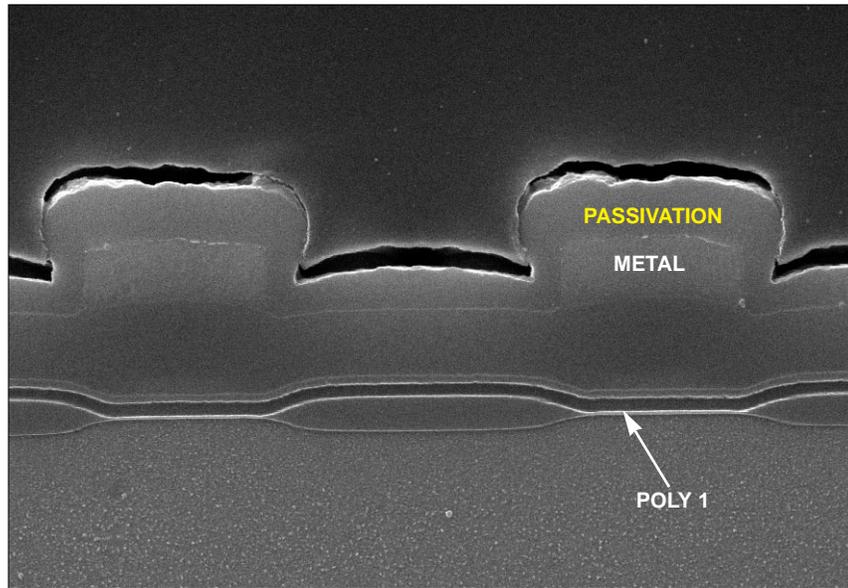


Mag. 13,000x

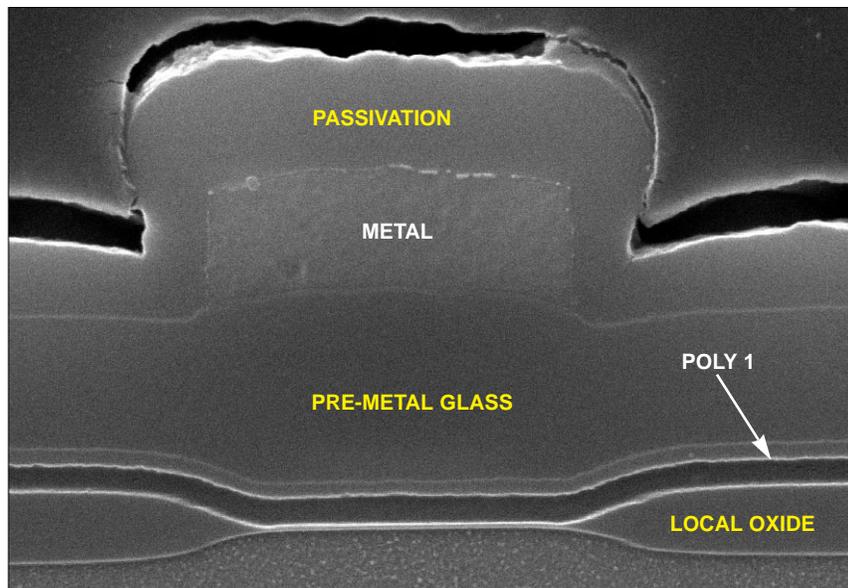


Mag. 25,000x

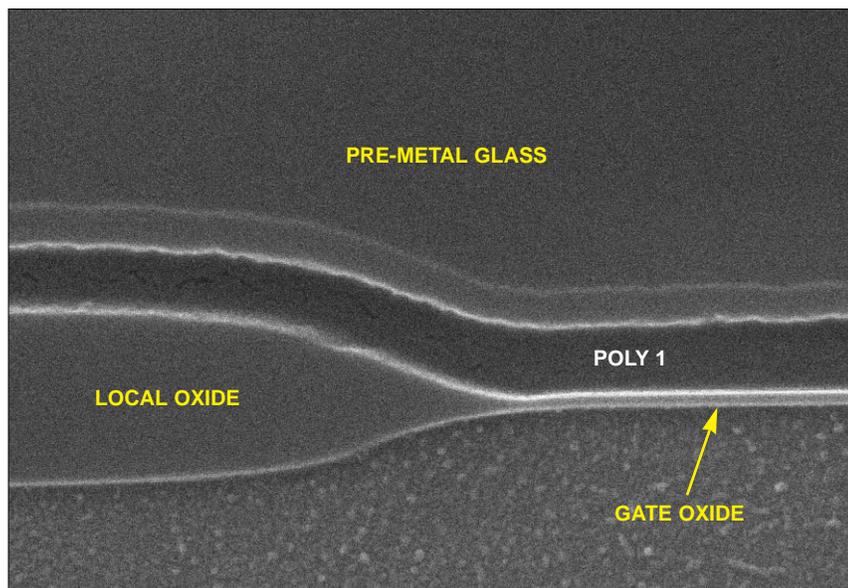
Figure 28. SEM section views illustrating details of the array (perpendicular to bit line).



Mag. 6500x

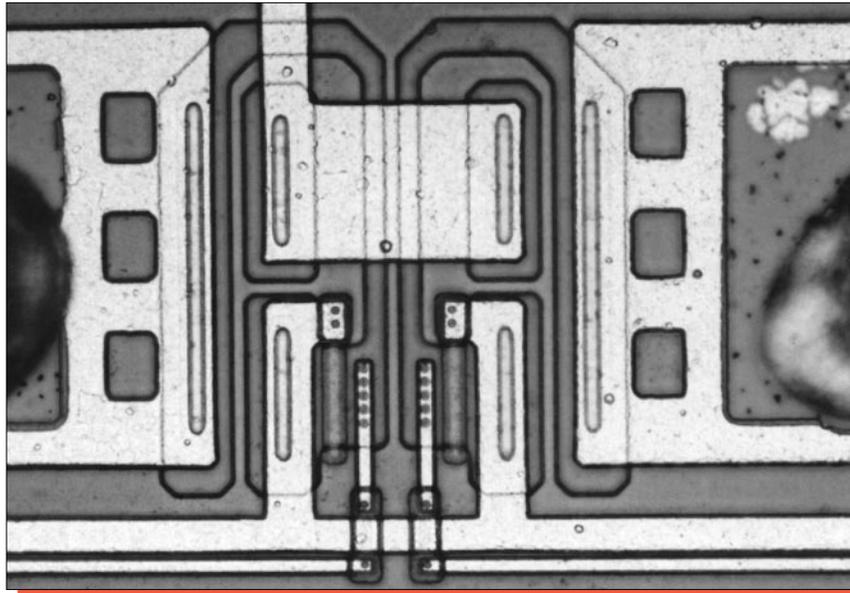


Mag. 13,000x

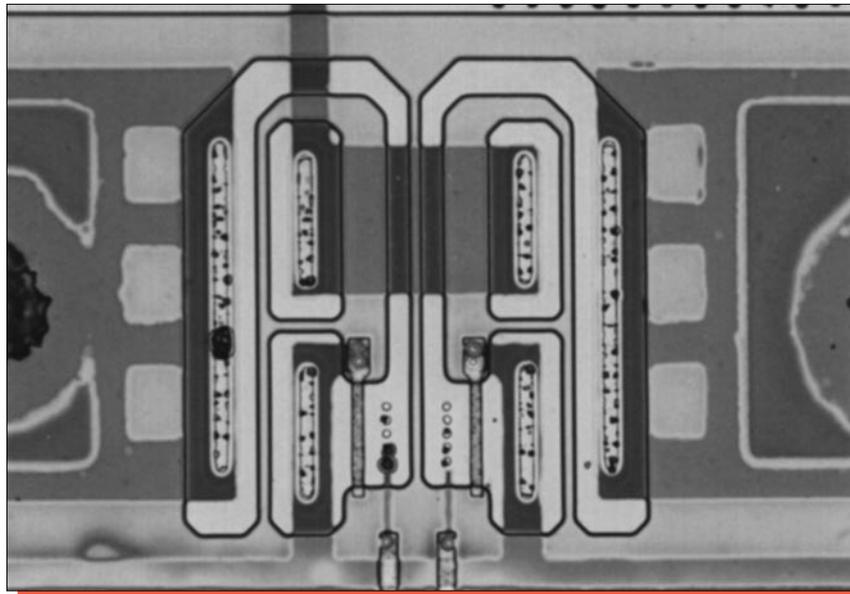


Mag. 31,000x

Figure 29. SEM section views illustrating the details of the array (perpendicular to bit line).



intact



unlayered

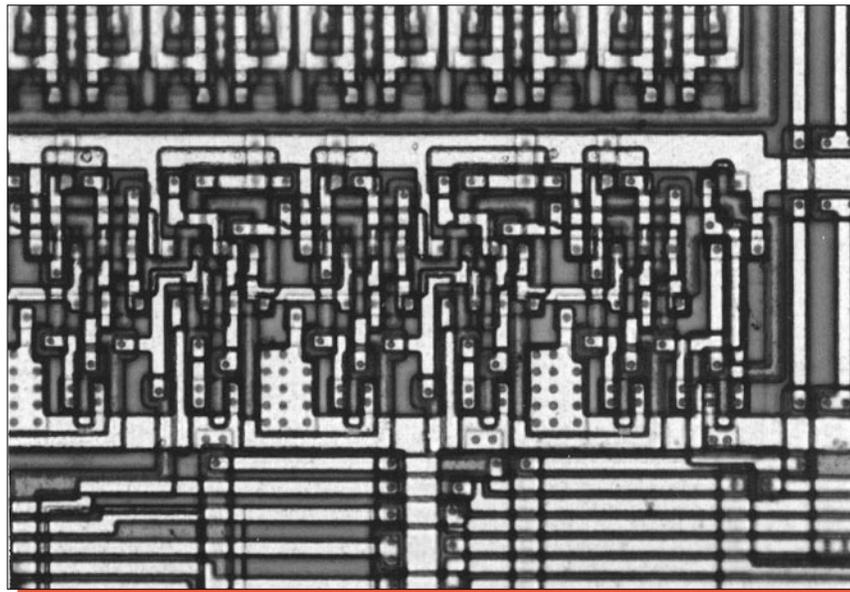


Figure 30. Optical views of the input protection and general circuit layout. Mag. 500x.