

## Construction Analysis

# SGS-Thomson 93C46CB1 1K EEPROM

Report Number: SCA 9612-519



**INTEGRATED CIRCUIT ENGINEERING**

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## **INTRODUCTION**

This report describes a construction analysis of the SGS-Thomson 93C46CB1 1K EEPROM. Four devices packaged in 8-pin Plastic Dual In-line Packages (PDIPs) were received for the analysis. Date codes were not identifiable (possibly 9618).

## **MAJOR FINDINGS**

**Questionable Items:**<sup>1</sup> None.

**Special Features:**

- Twin-well CMOS process with single poly and tunnel oxide windows.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **TECHNOLOGY DESCRIPTION**

### **Assembly:**

- Devices were packaged in 8-pin Plastic Dual In-line Packages (PDIPs).
- The dice were mounted to the paddles using a silver-filled polyimide die attach.
- Die separation was by sawing.
- Wirebonding was by the thermosonic ball bond method using 1.1 mil O.D. gold wire.
- All pins were connected. Lead-locking provisions (anchors) at all pins.

### **Die Process:**

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of a layer of oxy-nitride over a layer of silicon-dioxide.
- Metallization consisted of a single layer of dry-etched aluminum and did not use a cap or barrier. Standard contacts were used (no plugs).
- Pre-metal dielectric consisted of a layer of borophosphosilicate glass (BPSG) over densified oxides. The glass was reflowed following contact cuts.
- A single layer of poly (no silicide) was used to form all gates on the die, the word lines and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Definition of the poly was by a dry etch.

## **TECHNOLOGY DESCRIPTION (continued)**

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.
- Local oxide (LOCOS) isolation. A slight step was present in the oxide at the edge of the well boundaries indicating a twin-well process was used.
- The memory cell consisted of a 3T, single capacitor, EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor and the tunnel-oxide device.
- Two separate small MROM arrays were also present. One of these used poly mask programming, the other field oxide mask (i.e., diffusion) programming.
- Redundancy fuses were not present.

## ANALYSIS RESULTS I

### Package and Assembly:

### Figures 1 - 6

**Questionable Items:**<sup>1</sup> None.

**Special Features:** None.

### **General Items:**

- Devices were packaged in 8-pin Plastic Dual In-line Packages (PDIPs).
- Overall package quality: Good. No significant defects were noted on the external or internal portions of the package. No cracks or voids were noted in the plastic.
- Leadframe: The leadframe was constructed of copper.
- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present.
- Die attach: A silver-filled polyimide of normal quality was used to attach the die to the paddle.
- Wirebonding was by the thermosonic ball bond method using 1.1 mil O.D. gold wire. Bonds were well formed and placement was good. Wirepull strengths were normal with no bond lifts (see page 10).

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## ANALYSIS RESULTS II

### Die Process:

Figures 7 - 33

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Single poly, tunnel oxide windows.

### **General Items:**

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: A layer of oxy-nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good as it extended into the scribe lane to seal the metallization.
- Metallization: A single layer of metal consisting of aluminum. No cap or barrier metals were used.
- Metal patterning: The metal layer was patterned by a dry etch of normal quality. All contacts were completely surrounded by aluminum.
- Metal defects: No voiding, notching, or neckdown was noted in the metal layer. No silicon nodules were noted following the removal of the aluminum layer.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS II (continued)**

- Metal step coverage: Worst case aluminum thinning was 65 percent at contact edges. Typical aluminum thinning was 50 percent. MIL-STD allows up to 70 percent metal thinning for contacts of this size.
- Pre-metal dielectric: A layer of borophosphosilicate glass ( BPSG) over densified oxides was used under the metal. Reflow was performed following contact cuts. No problems were found.
- Contact defects: None. Alignment was good and no significant over-etching of the contacts was noted.
- Polysilicon: A single layer of poly (no silicide) was used to form all gates, word lines, and one plate of the capacitors in the EEPROM cell array. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.
- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. No silicide was present over diffusions.
- Local oxide (LOCOS) isolation was used. No problems were noted. The slight step present in the oxide at the well boundary indicates a twin-well process was employed. The P-well could not be delineated in cross section.
- ROM arrays: Two different MROM array types were present on the device. Both were located at one end of the die. One array was programmed at the poly level (see Figures 21 and 22) and the other array was programmed at the diffusion level (see Figures 23 and 24).
- EEPROM: The EEPROM memory cells used three transistor, single capacitor EEPROM design. Metal was used to form the bit lines. Poly was used to form the word/select lines, one plate of the capacitor, and the tunnel oxide device. Cell pitch was 7.8 x 18.4 microns.
- Redundancy fuses were not present on the die.

## **PROCEDURE**

The devices were subjected to the following analysis procedures:

- External inspection
- X-ray
- Decapsulate
- Internal optical inspection
- SEM of passivation and assembly features
- Passivation integrity test
- Wirepull test
- Passivation removal
- SEM inspection of metal
- Metal removal
- Delayer to silicon and inspect poly/die surface
- Die sectioning (90° for SEM)\*
- Die material analysis
- Measure horizontal dimensions
- Measure vertical dimensions

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Good

**DETAIL OF EVALUATION**

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver-filled polyimide
Dicing method	Sawn
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Contact coverage	G
Contact registration	G

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

**PACKAGE MARKINGS (TOP)**

93C46CB1  
91E618  
(LOGO) MAL

**(BOTTOM)**

NONE

**WIREBOND STRENGTH**

Wire material: 1.1 mil O.D. gold  
Die pad material: aluminum

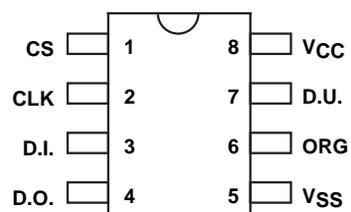
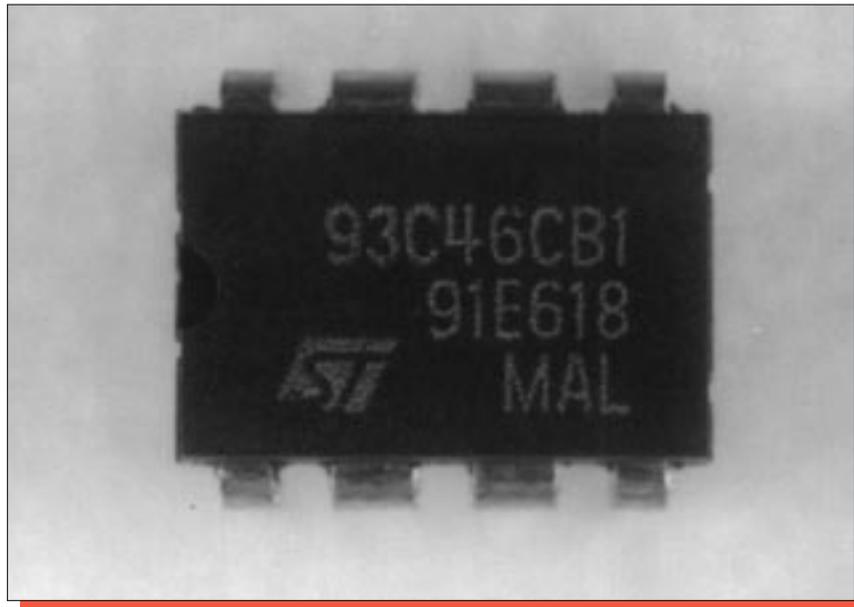
**Sample #** 1  
# of wires pulled: 8  
Bond lifts: 0  
Force to break - high: 9.5g  
- low: 4.5g  
- avg.: 7.5g  
- std. dev.: 1.6

**DIE MATERIAL ANALYSIS**

Overlay passivation: A layer of oxy-nitride over a layer of silicon-dioxide.  
Metallization:\* Aluminum (Al).  
Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) containing 3.4 wt. % phosphorus and 3.6 wt. % boron over various densified oxides.

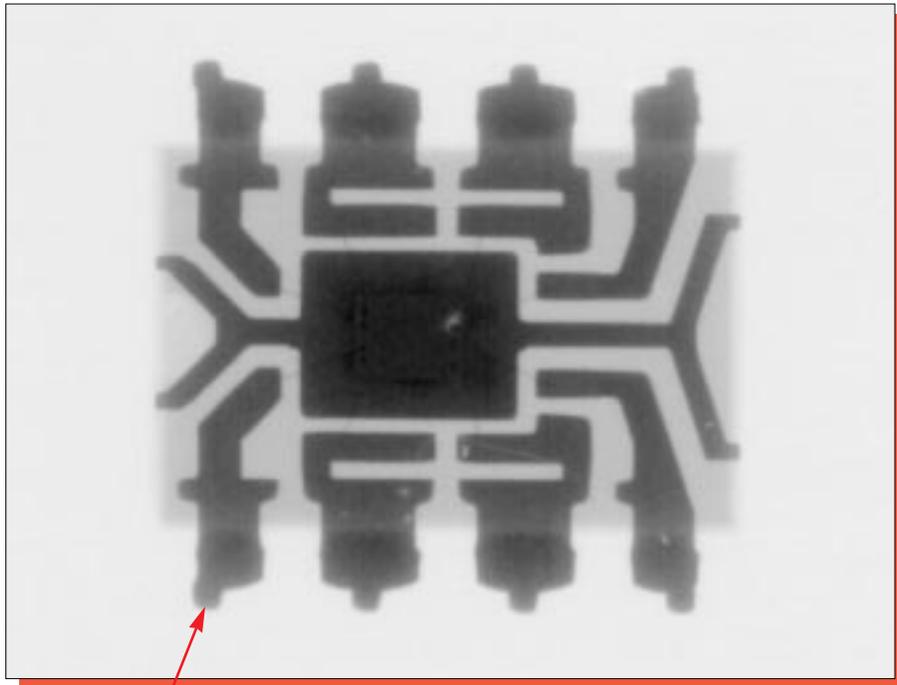
*\*There is no known method for determining the exact amount of silicon or copper in the aluminum of a finished die.*





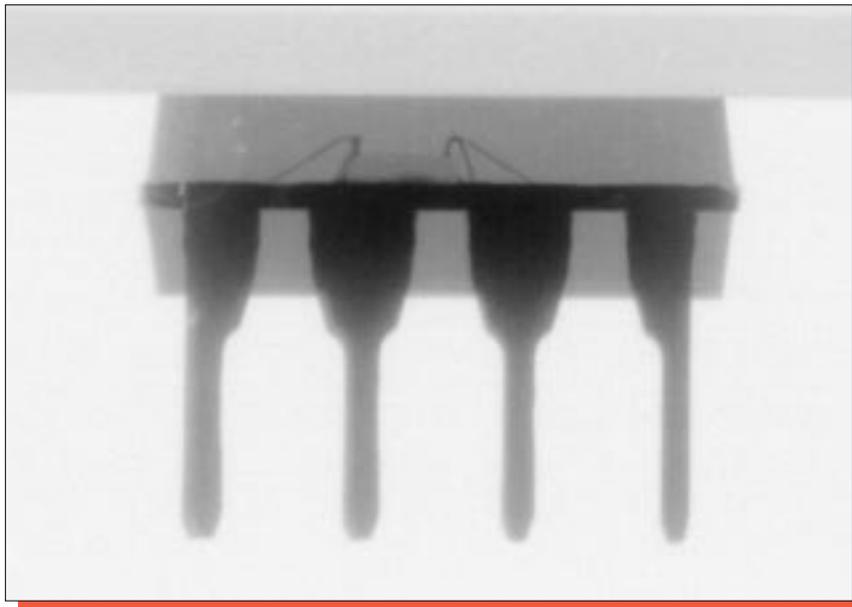
D.U. = DON'T USE

Figure 1. Package photograph and pinout diagram of the SGS-Thomson 93C46CB1 1Kbit EEPROM. Mag. 7.5x.



PIN 1

top view



side view

Figure 2. X-ray views of the package. Mag. 8x.

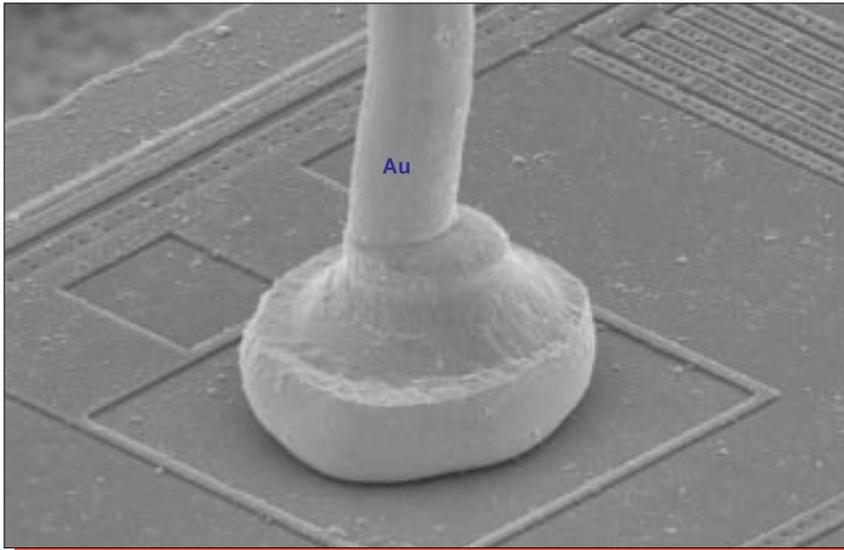
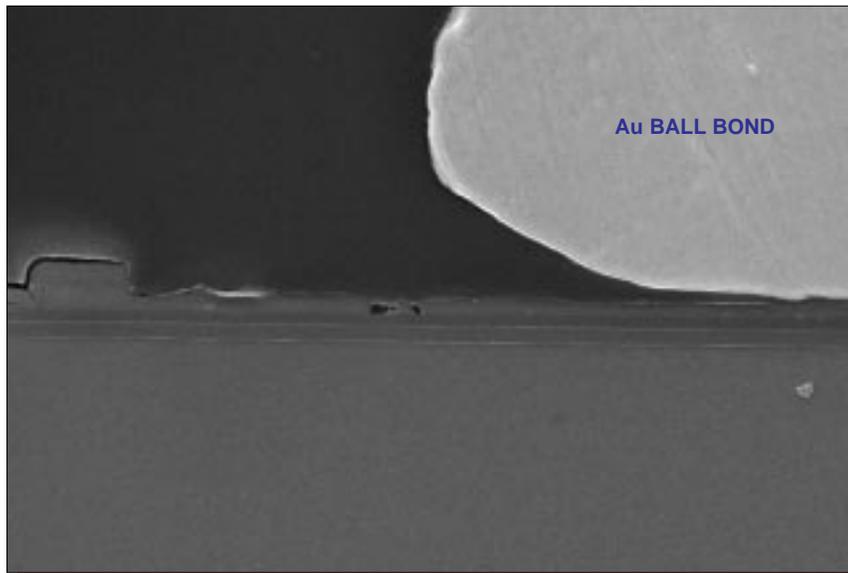
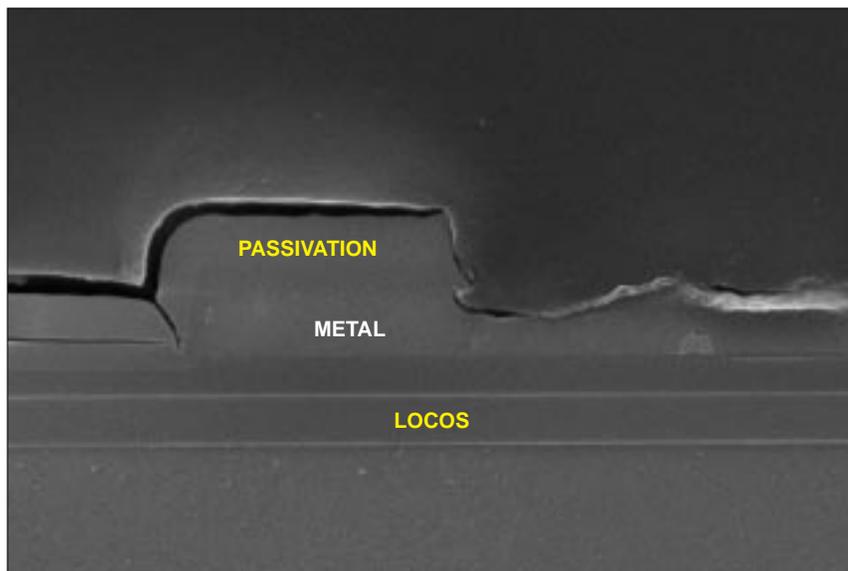


Figure 3. Perspective SEM view of a typical ball bond. Mag. 600x. 60°.

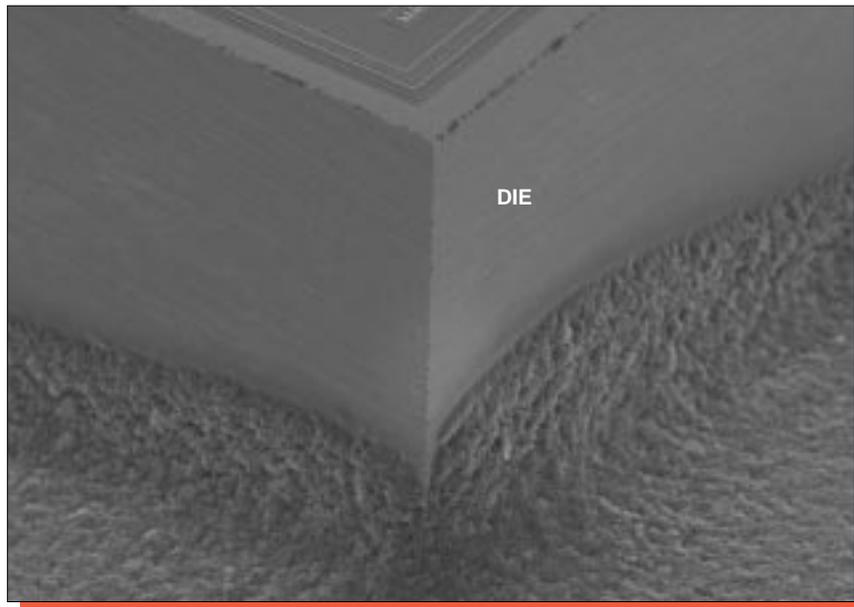


Mag. 3000x

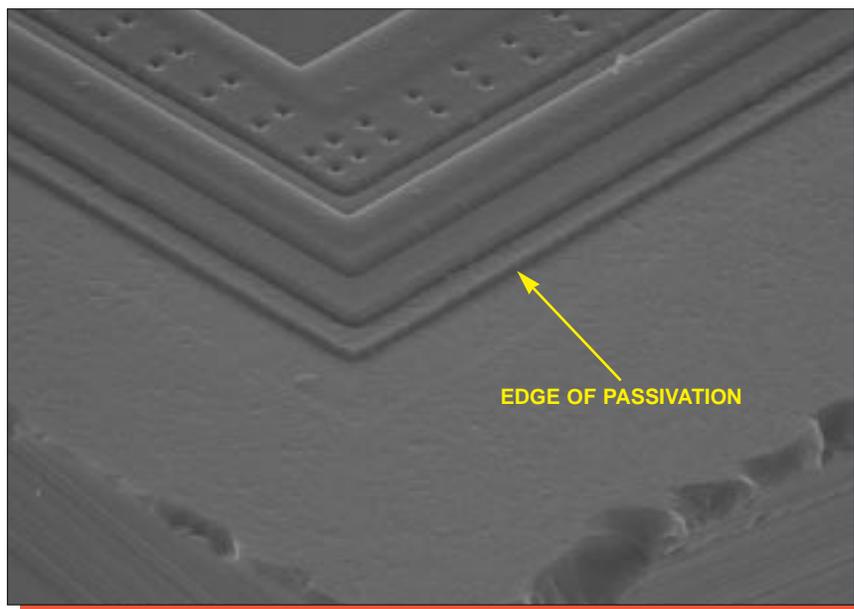


Mag. 10,000x

Figure 4. SEM section views of the bond pad.

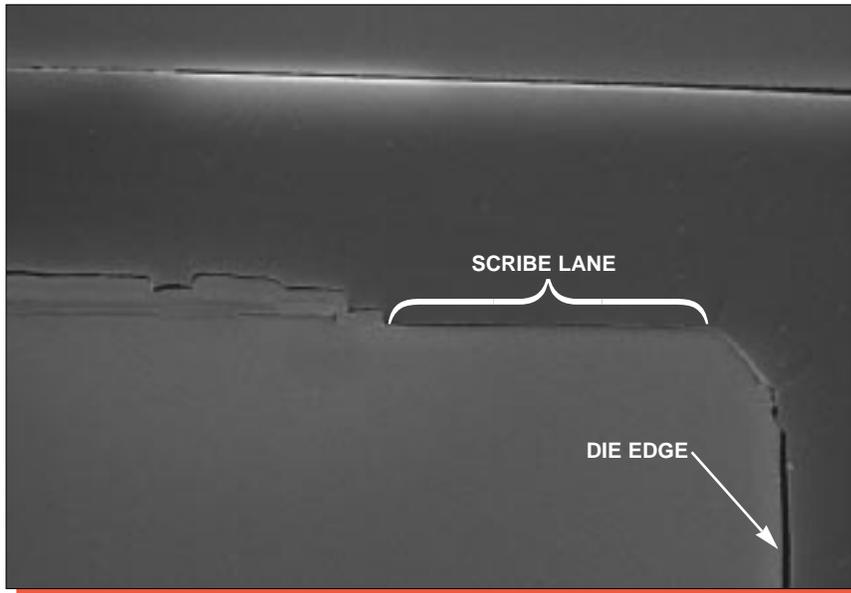


Mag. 150x

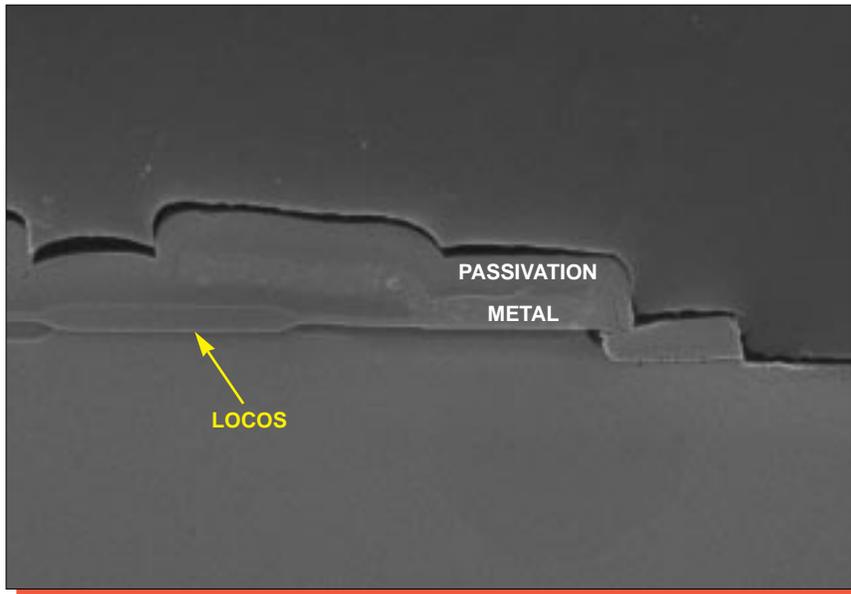


Mag. 1300x

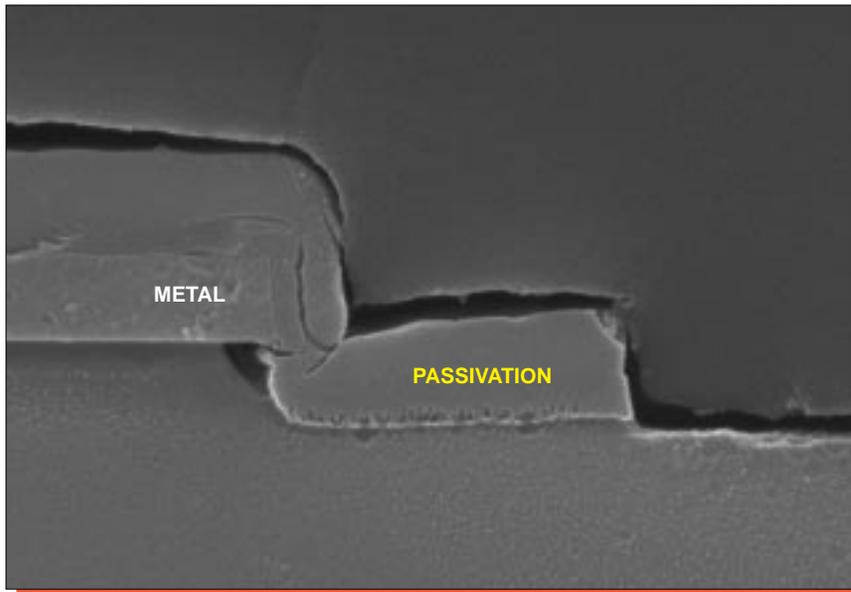
Figure 5. SEM views of die corner and edge seal. 60°.



Mag. 1600x



Mag. 5000x



Mag. 13,000x

Figure 6. SEM views of the edge seal.

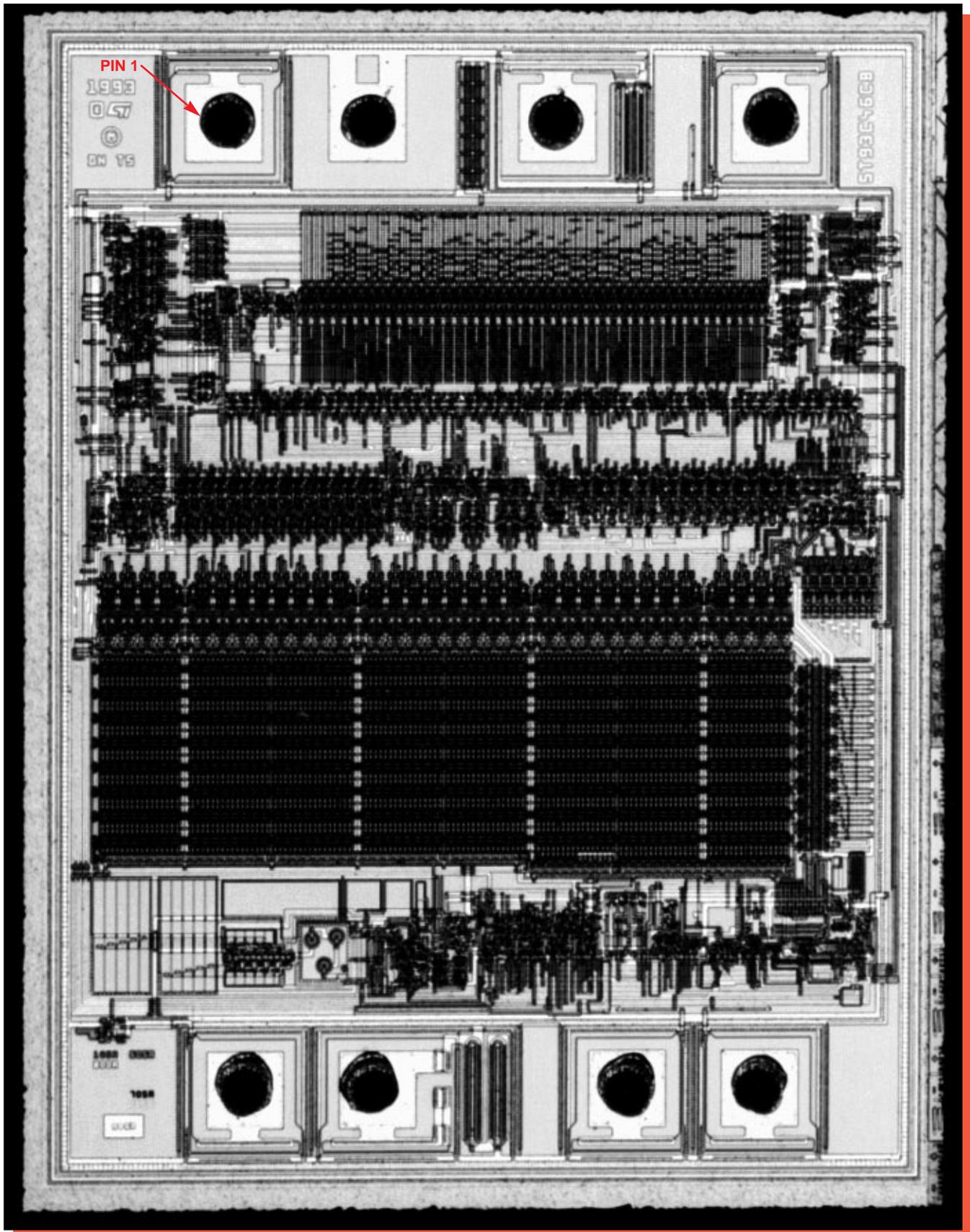


Figure 7. Whole die photograph of the SGS-Thomson 93C46CB1 EEPROM. Mag. 120x.

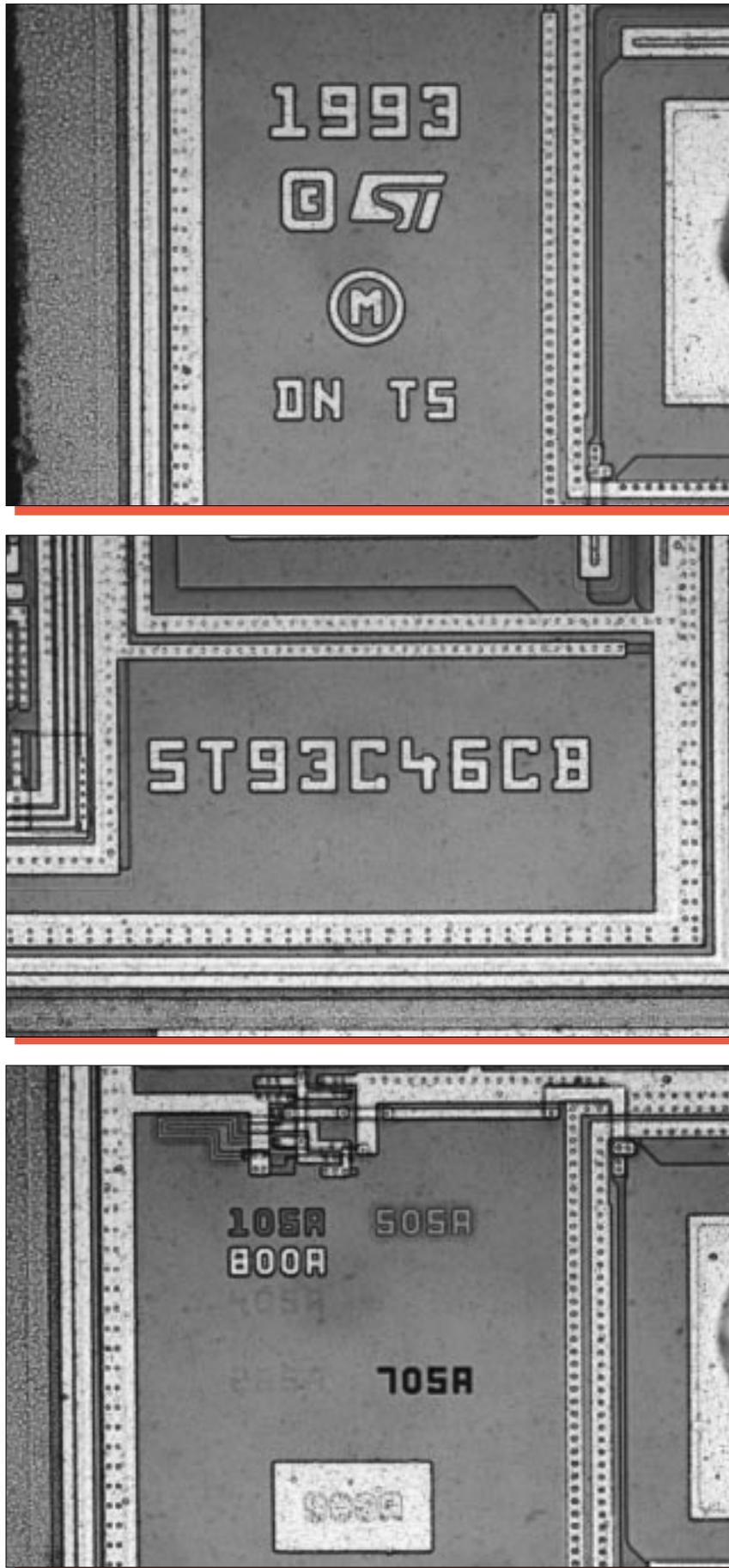
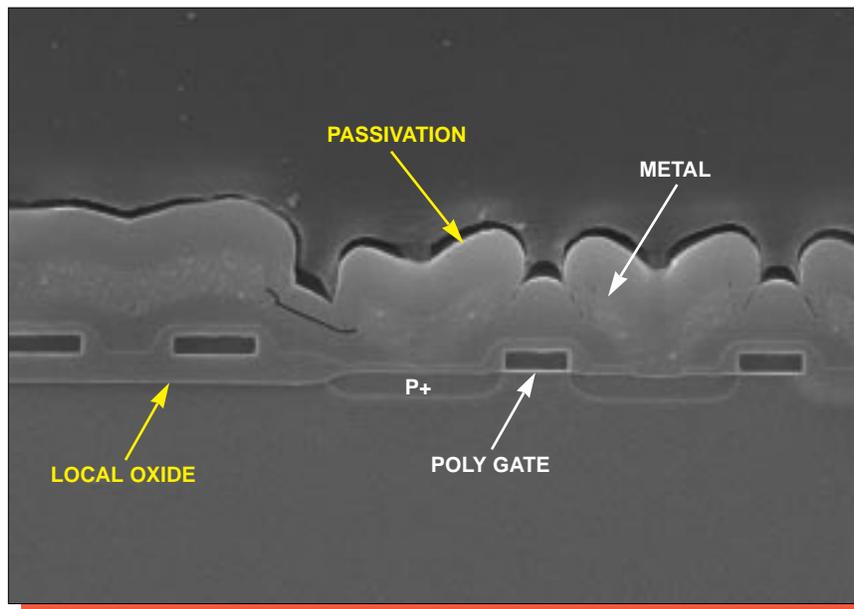
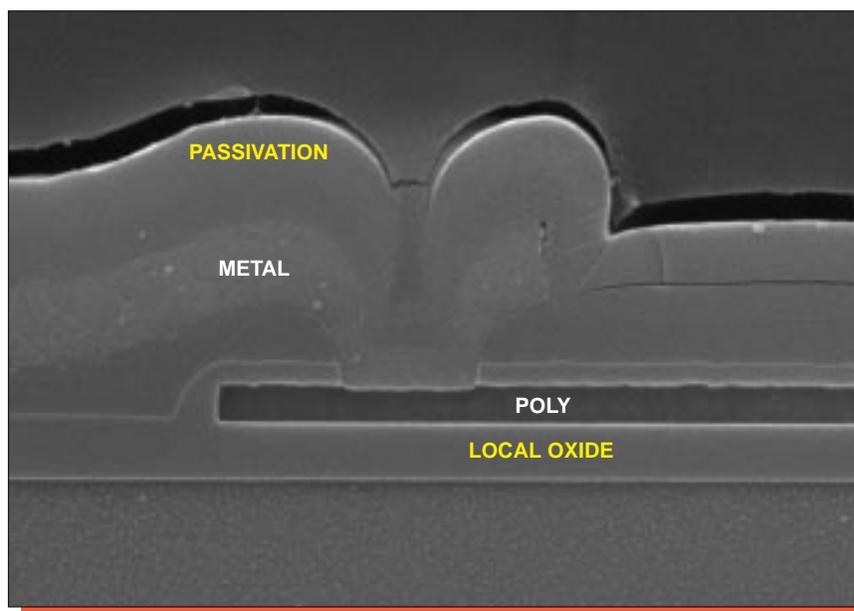


Figure 8. Identification markings from the die surface. Mag. 400x.

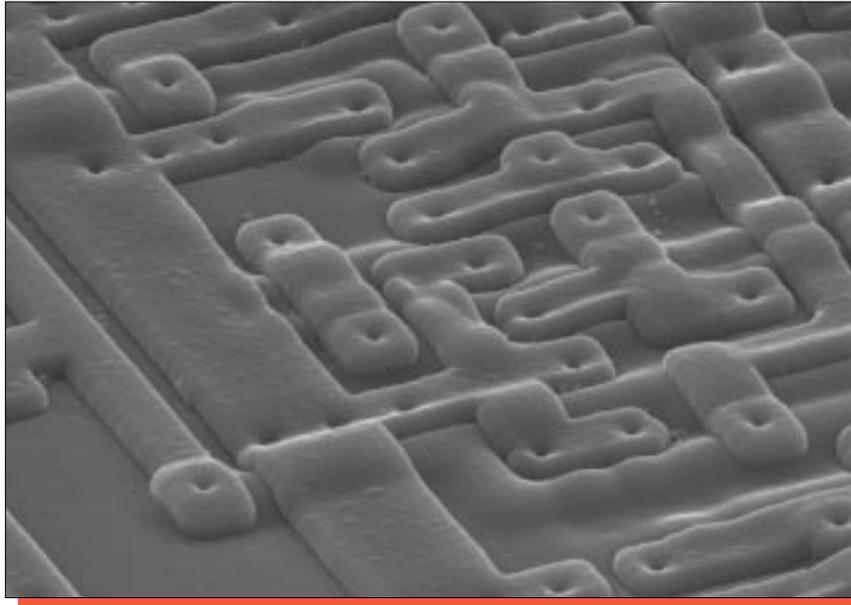


Mag. 6200x

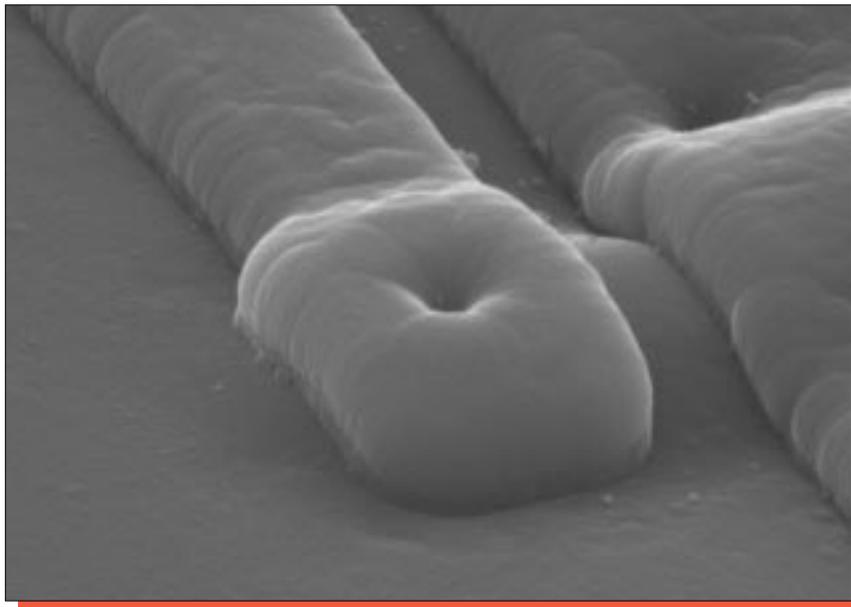


Mag. 13,000x

Figure 9. SEM section views illustrating general device structure.

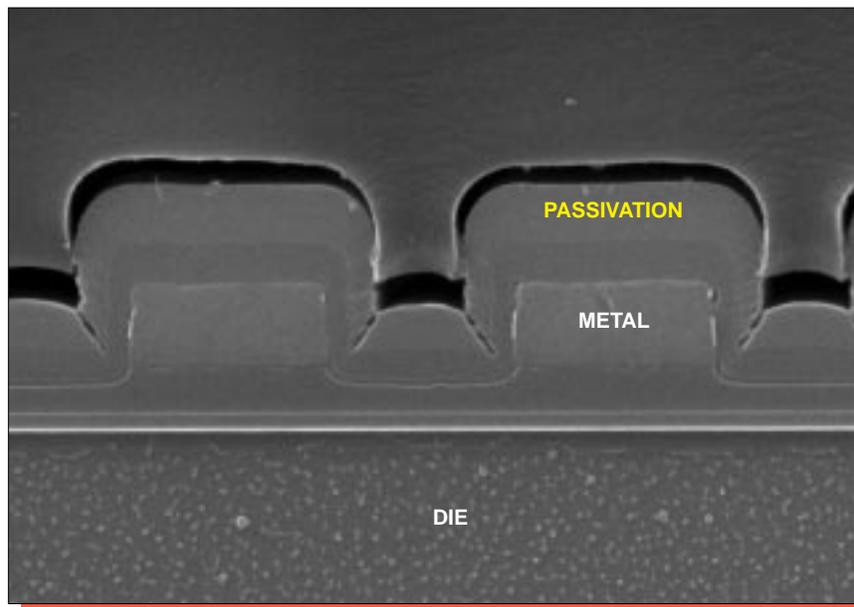


Mag. 2500x

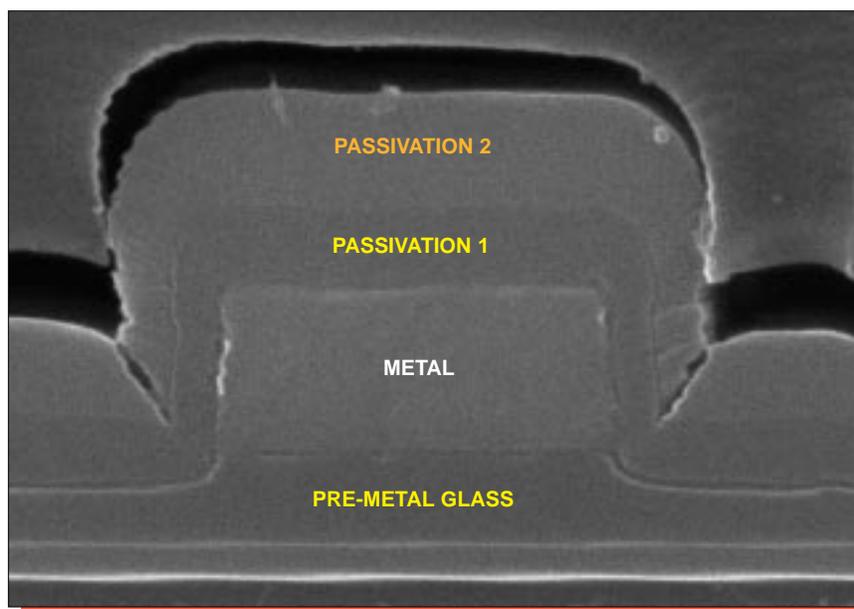


Mag. 10,000x

Figure 10. SEM views of overlay passivation coverage. 60°.

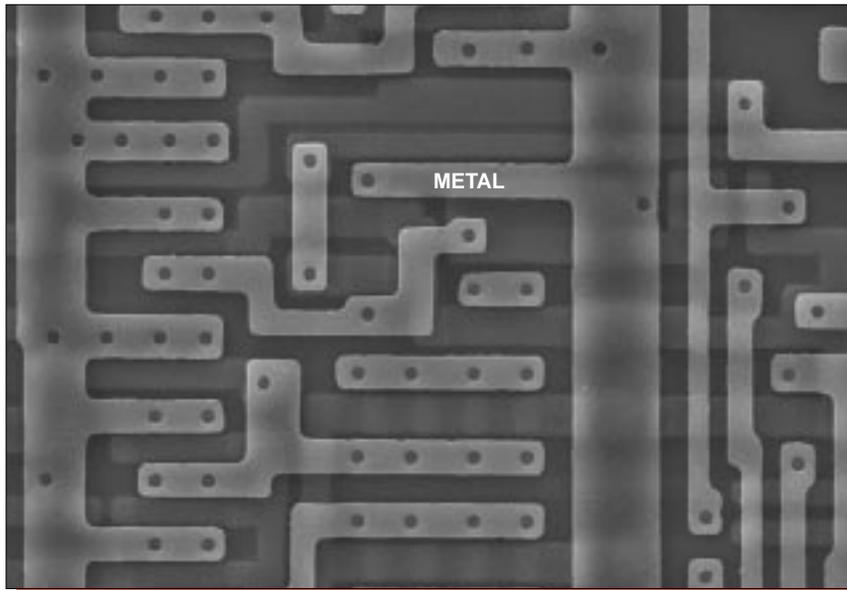


Mag. 13,000x

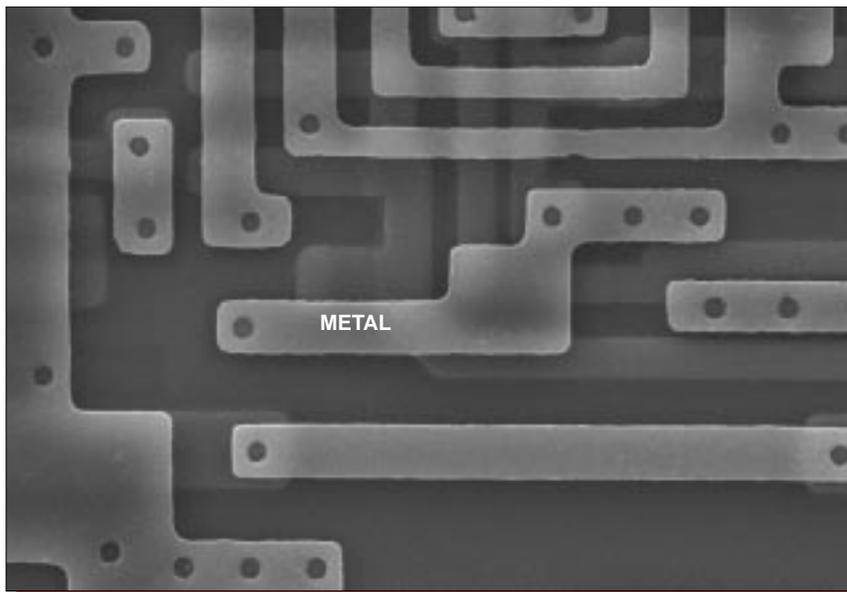


Mag. 26,000x

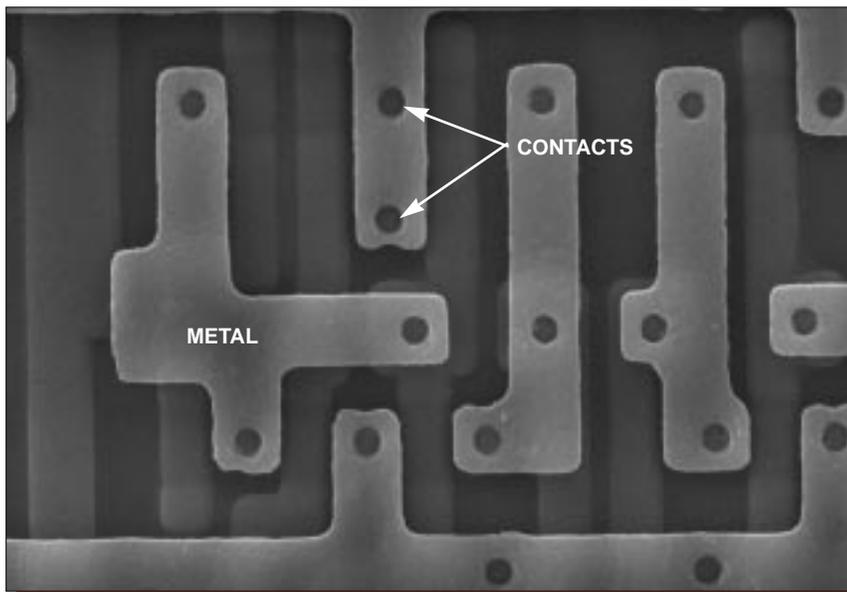
Figure 11. SEM section views of metal line profiles.



Mag. 1600x

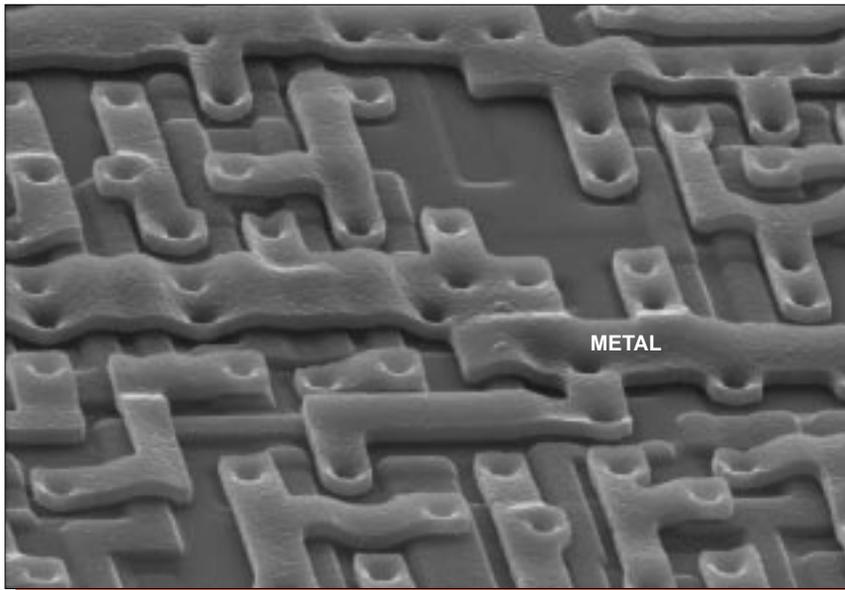


Mag. 2500x

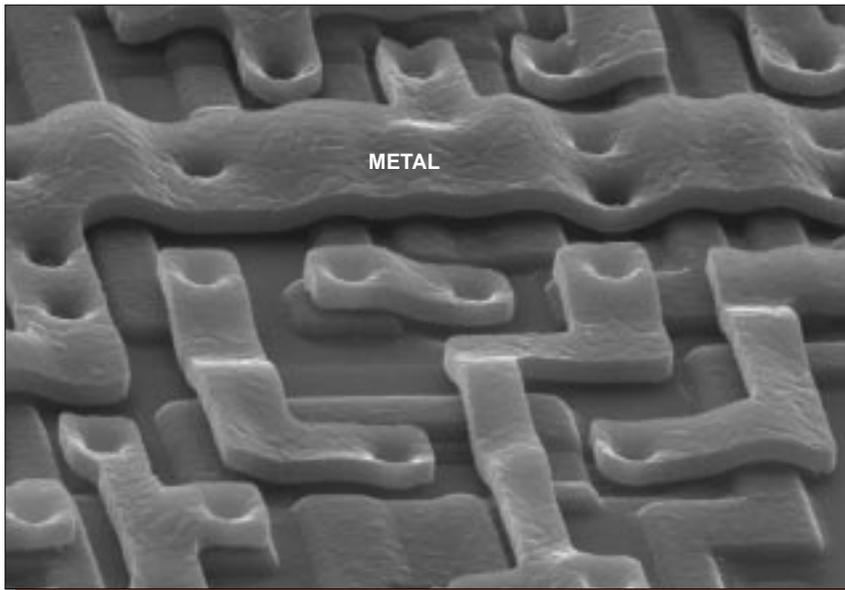


Mag. 3300x

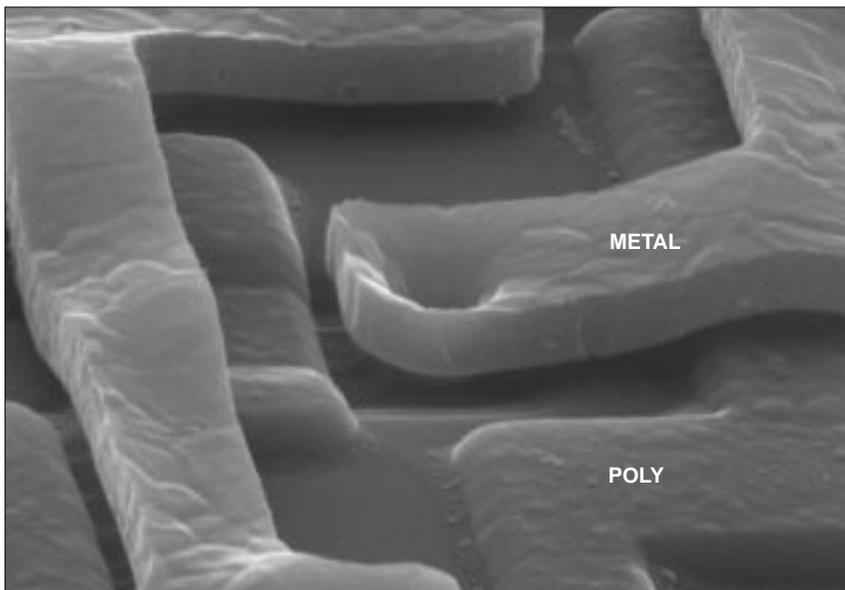
Figure 12. Topological SEM views illustrating metal patterning. 0°.



Mag. 2500x

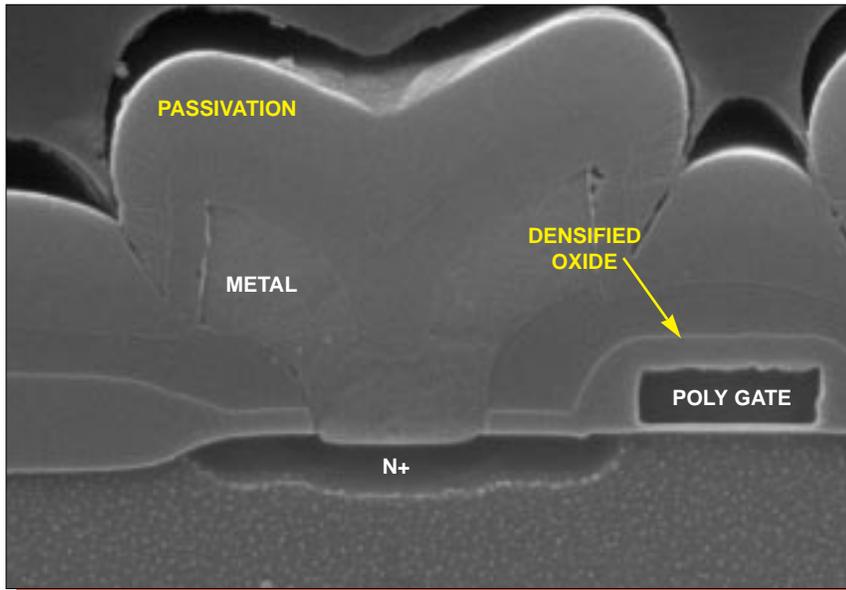


Mag. 4000x

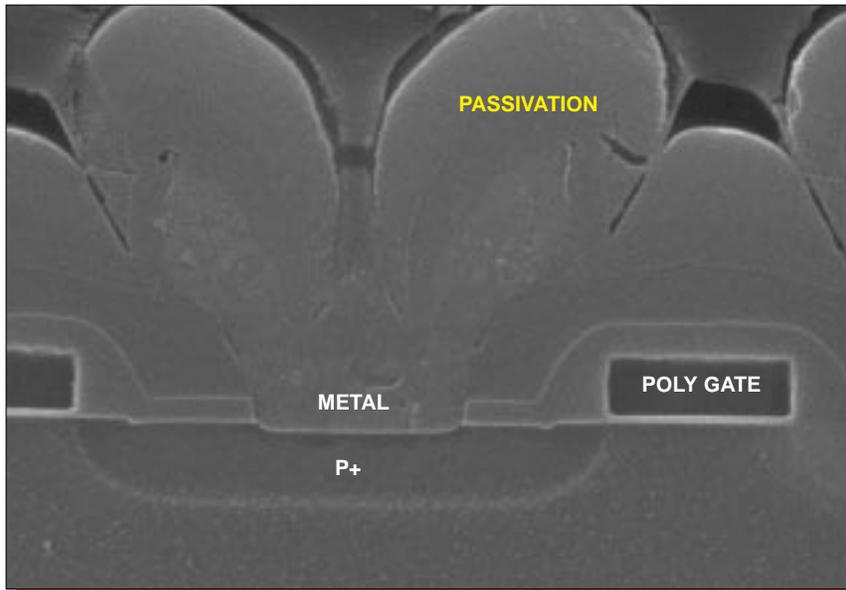


Mag. 10,000x

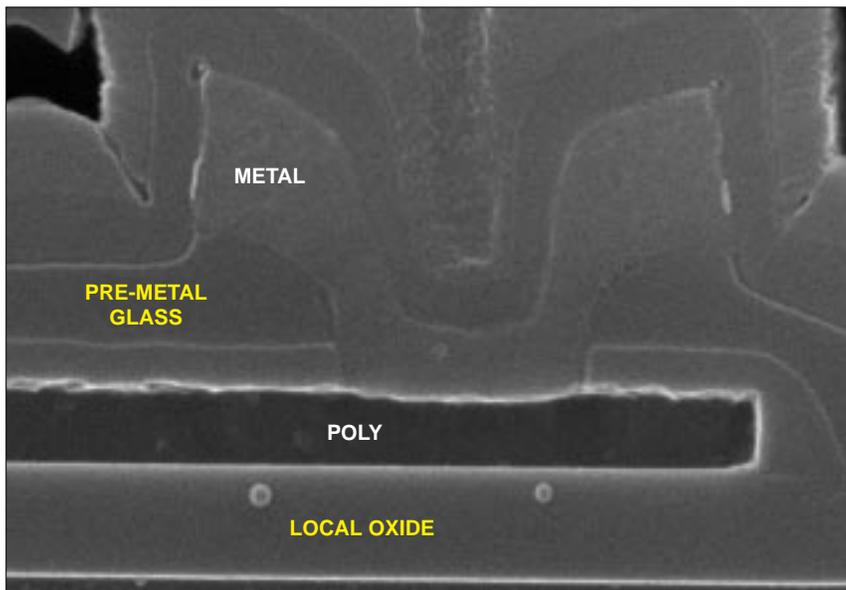
Figure 13. Perspective SEM views illustrating metal coverage. 60°.



metal-to-N+,  
Mag. 20,000x

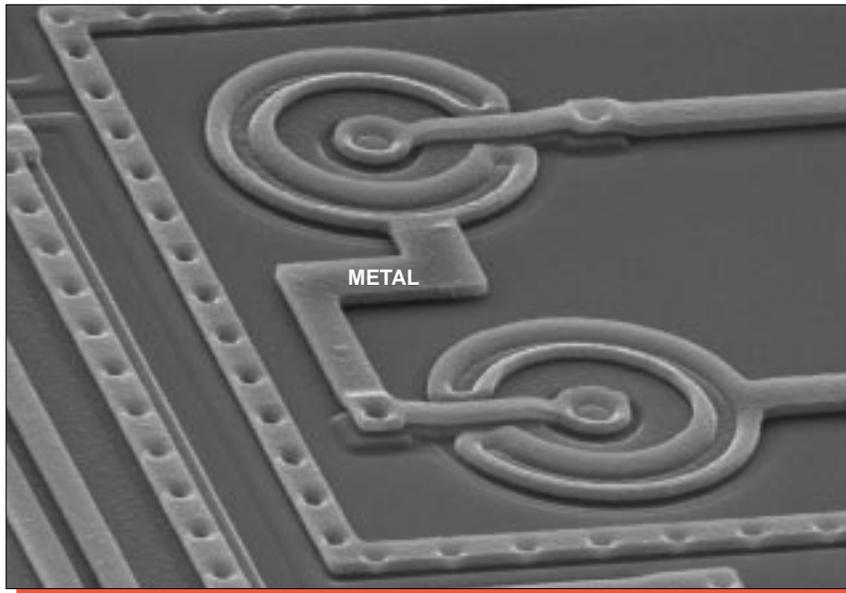


metal-to-P+,  
Mag. 20,000x

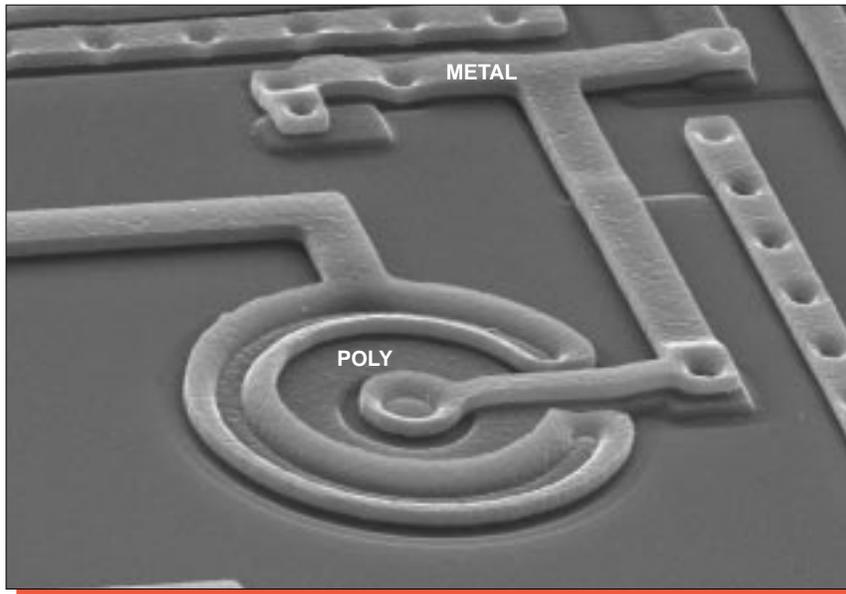


metal-to-poly,  
Mag. 26,000x

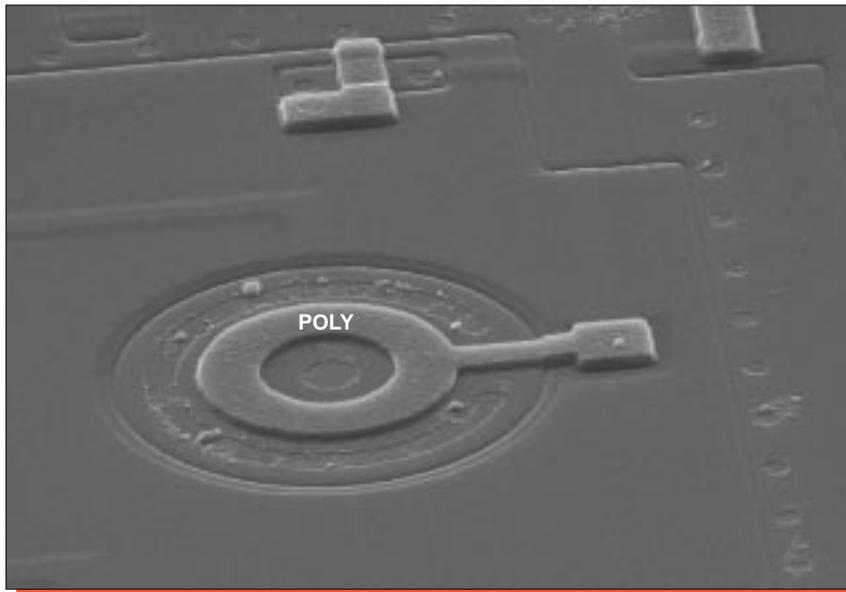
Figure 14. SEM section views of metal contacts.



metal,  
Mag. 1900x

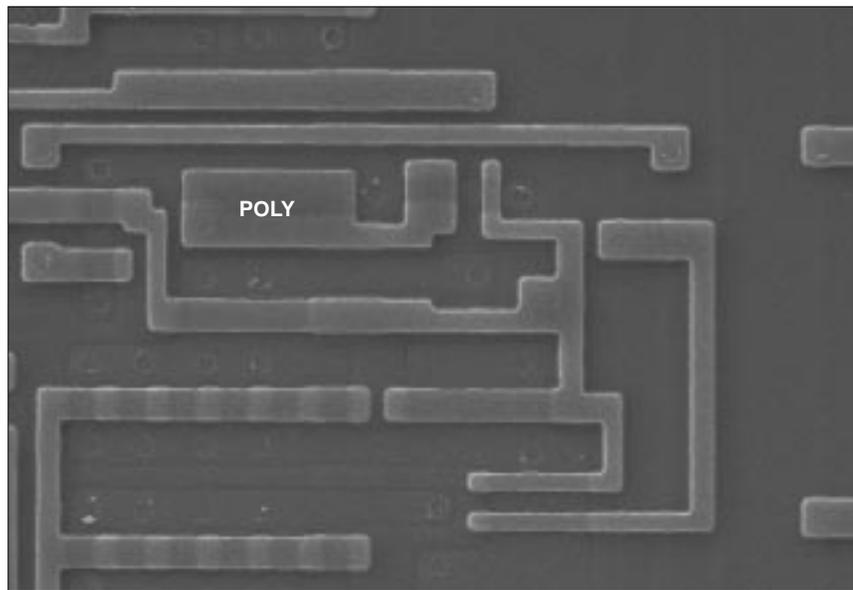


metal,  
Mag. 2500x

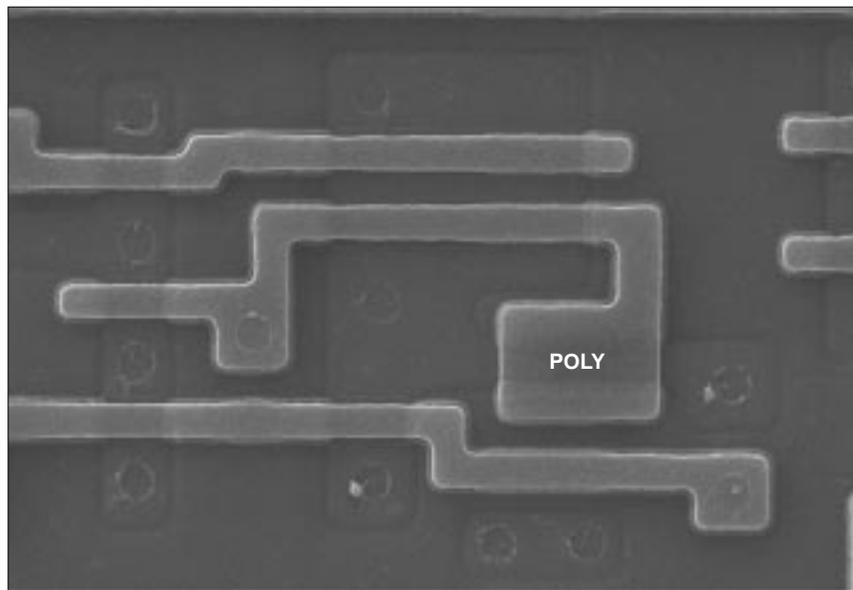


unlayered,  
Mag. 2500x

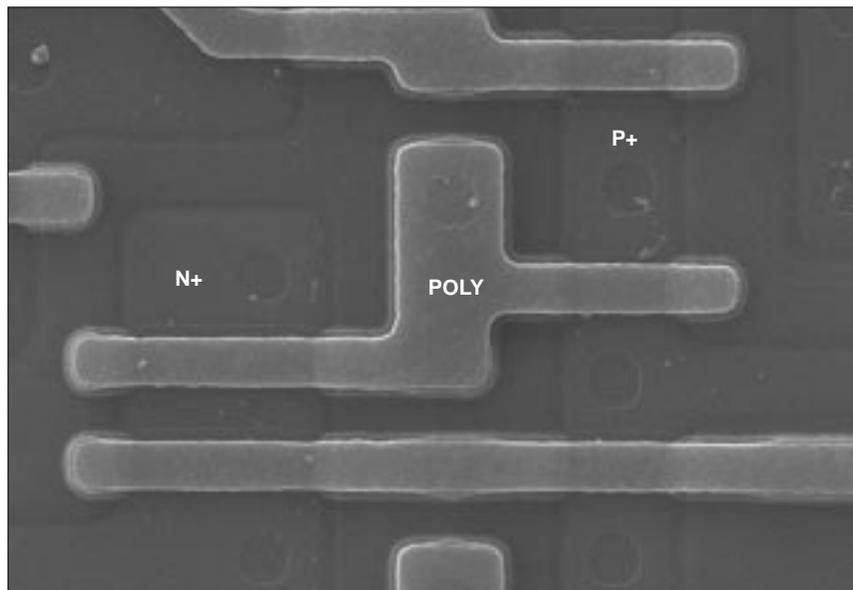
Figure 14a. Perspective SEM views of circular devices. 60°.



Mag. 1600x

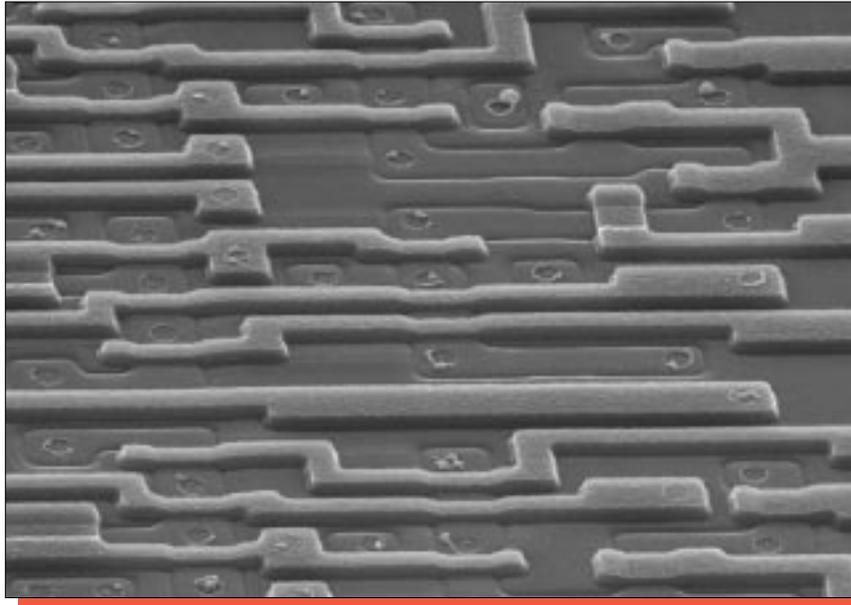


Mag. 3300x

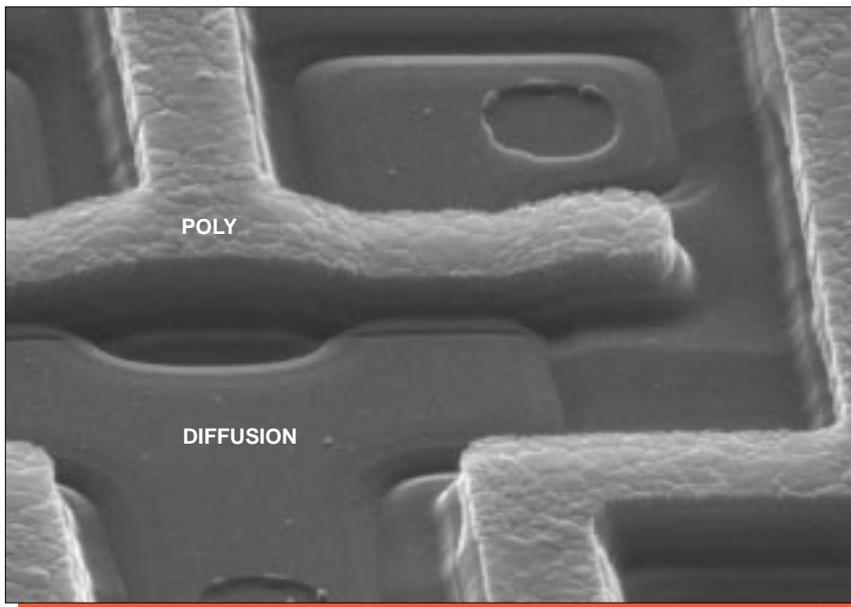


Mag. 5000x

Figure 15. Topological SEM views illustrating poly patterning. 0°.



Mag. 2600x



Mag. 13,000x

Figure 16. SEM views illustrating poly coverage. 60°.

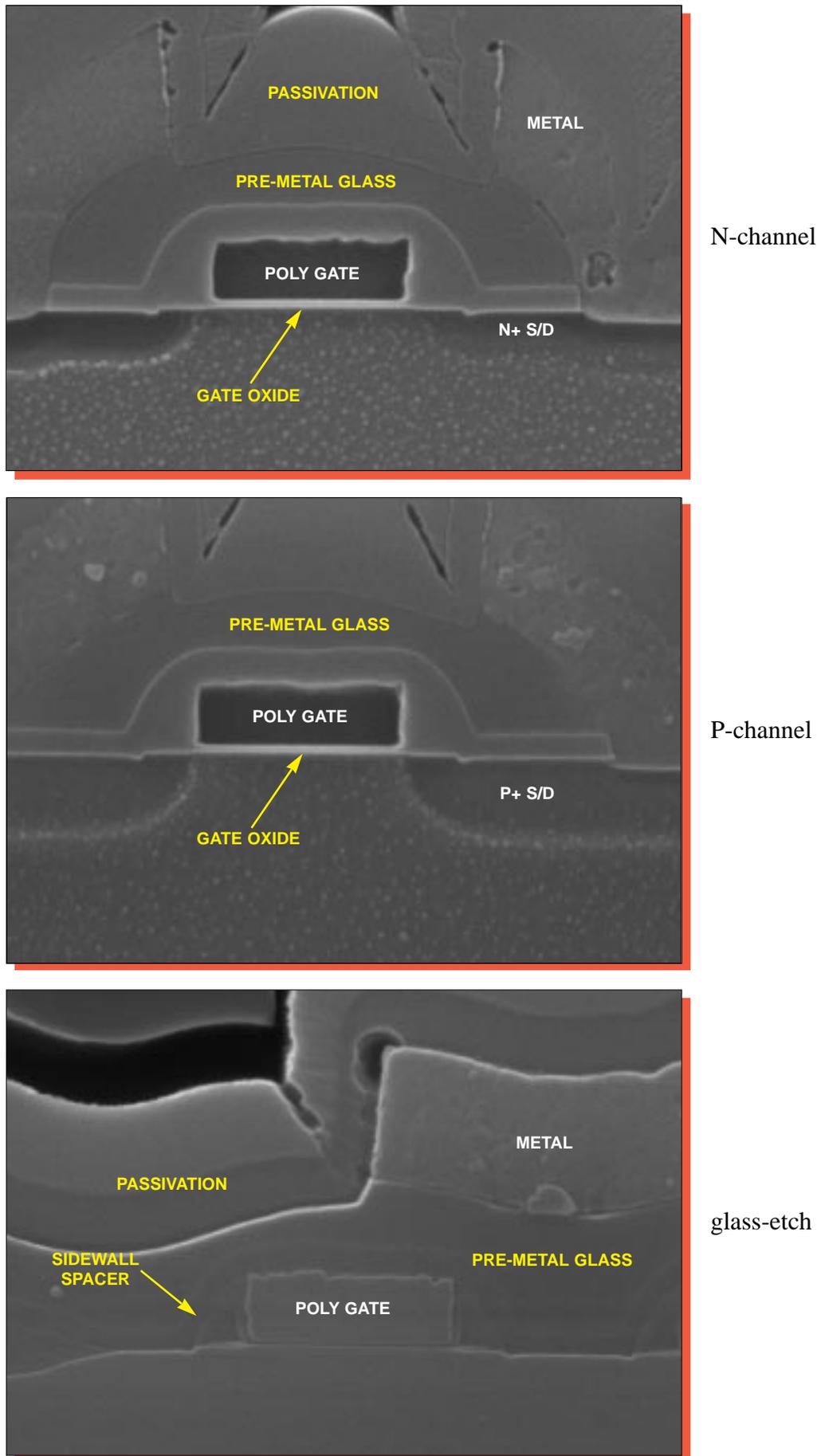


Figure 17. SEM section views illustrating typical gates. Mag. 26,000x.

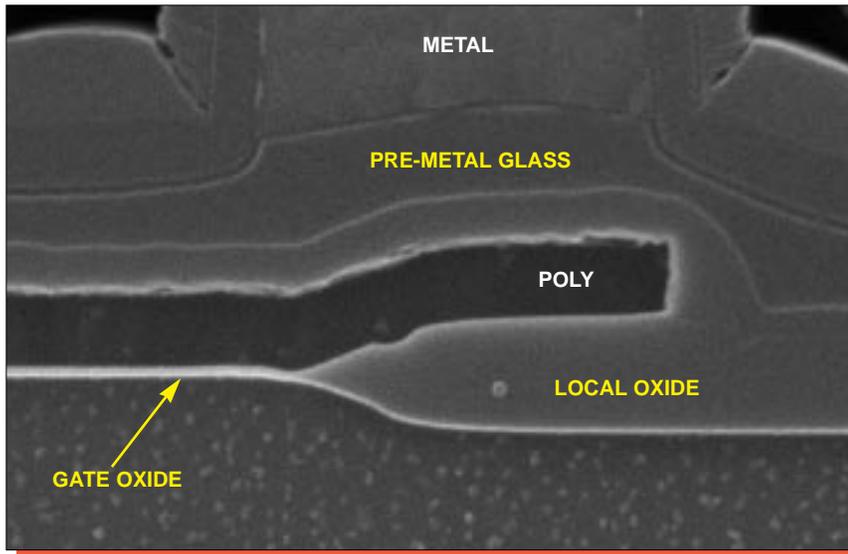
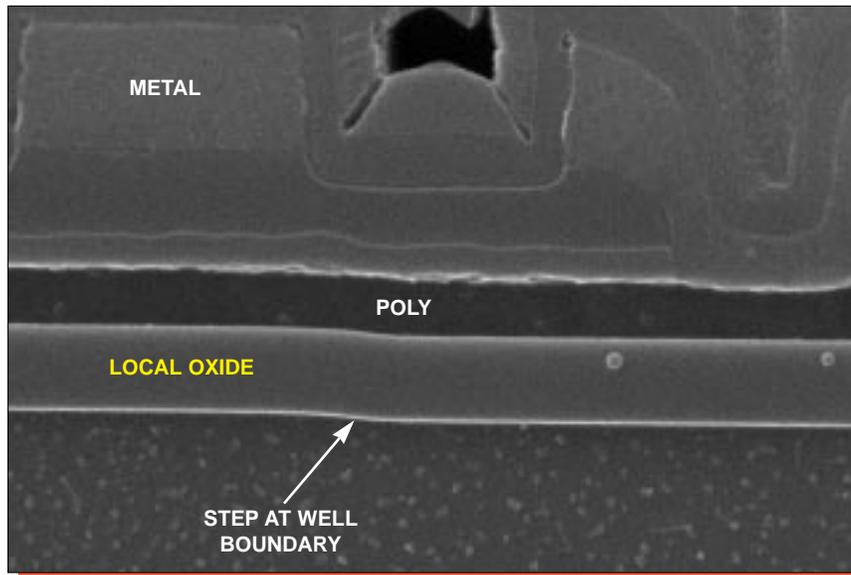
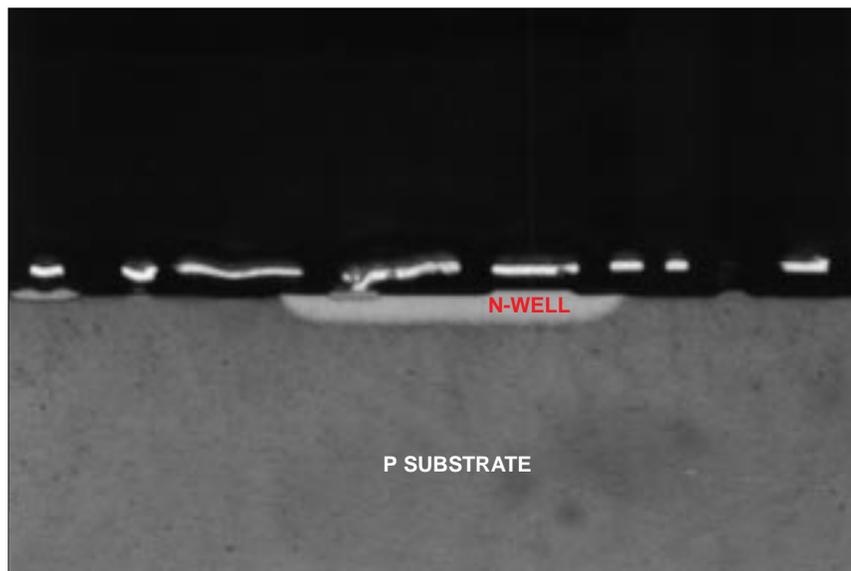


Figure 18. SEM section view of a local oxide birdsbeak profile. Mag. 26,000x.

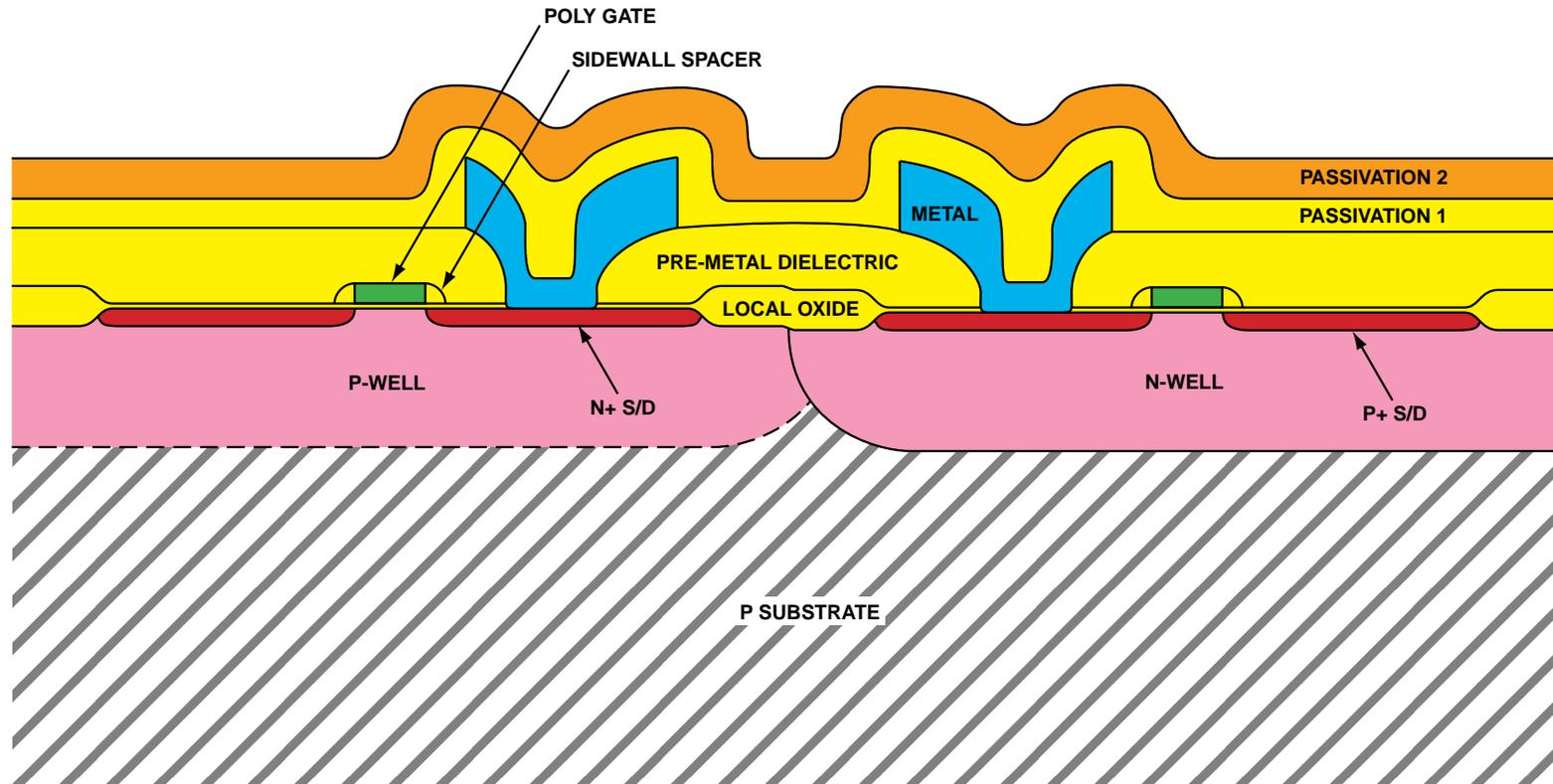


Mag. 20,000x



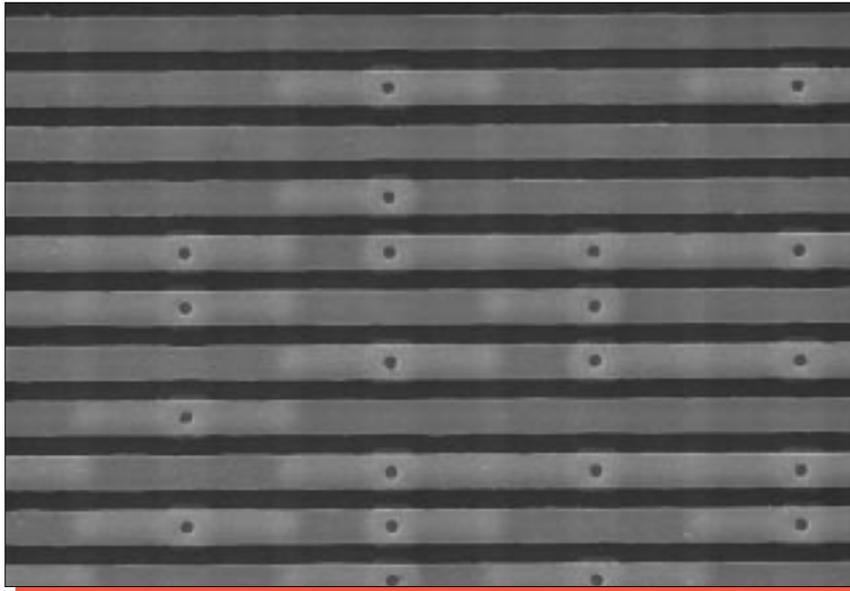
Mag. 1600x

Figure 19. Optical and SEM views illustrating well structure.

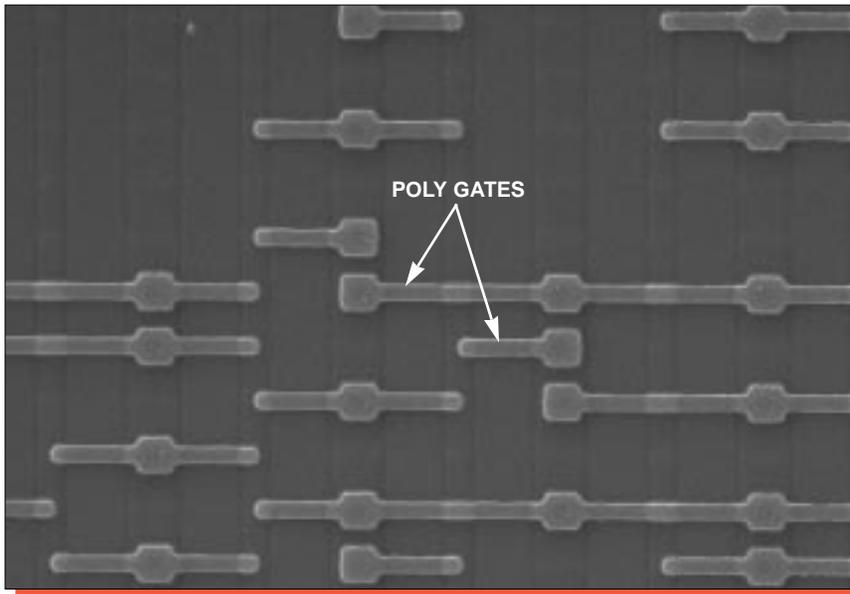


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
Red = Diffusion, and Gray = Substrate

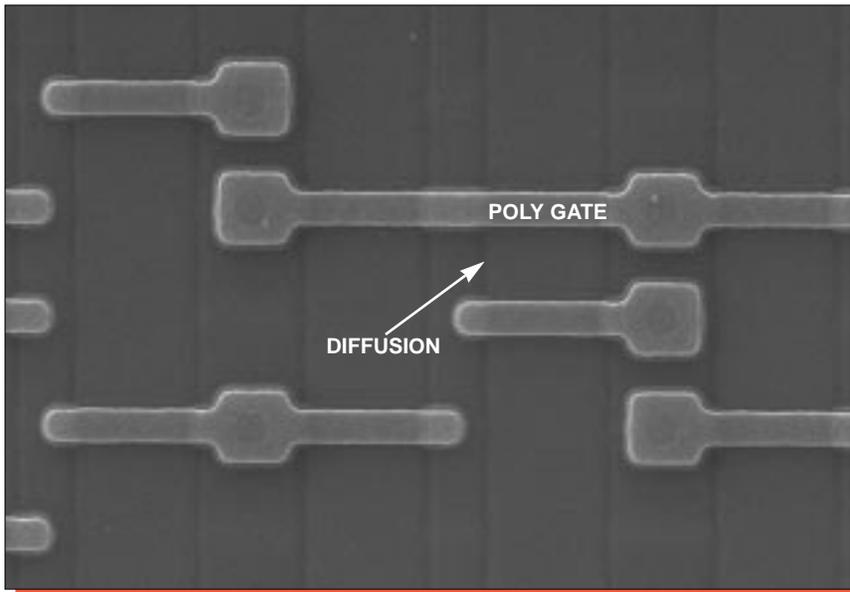
Figure 20. Color cross section drawing illustrating device structure.



metal,  
Mag. 1600x

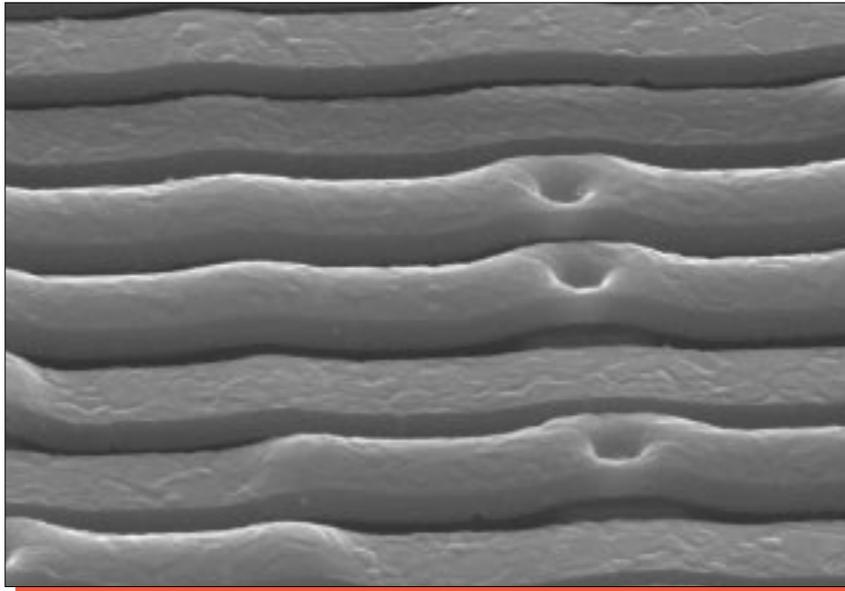


poly,  
Mag. 1600x

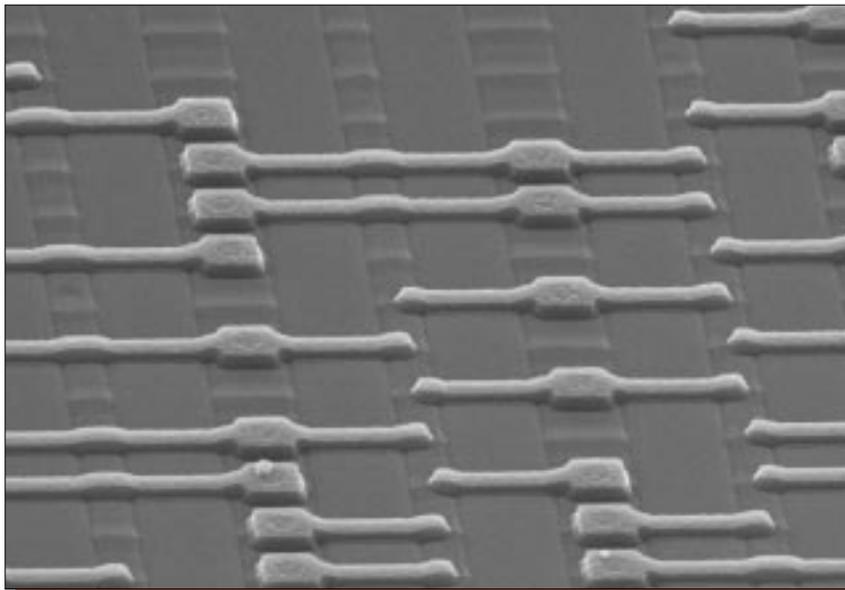


poly,  
Mag. 3300x

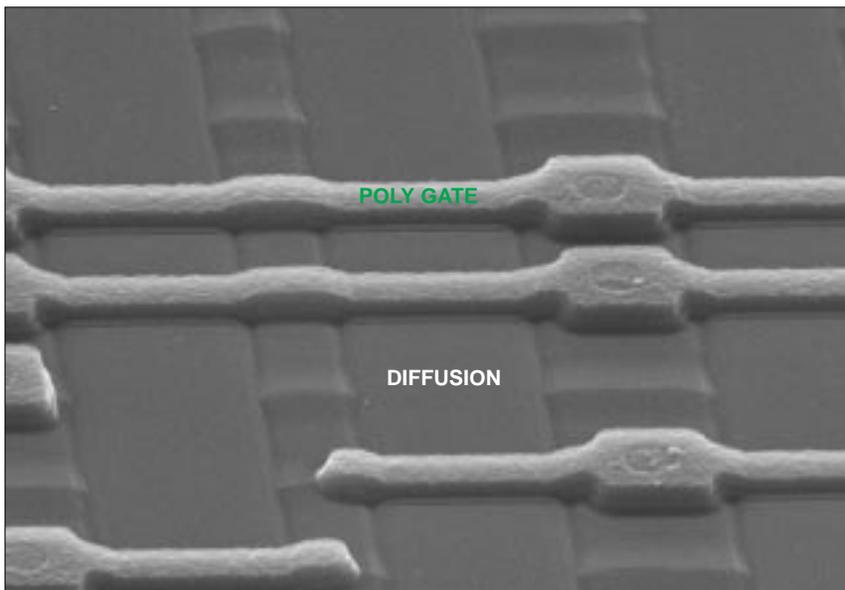
Figure 21. Topological views of an MROM array on the 93C46CB1. 0°.



metal,  
Mag. 5000x

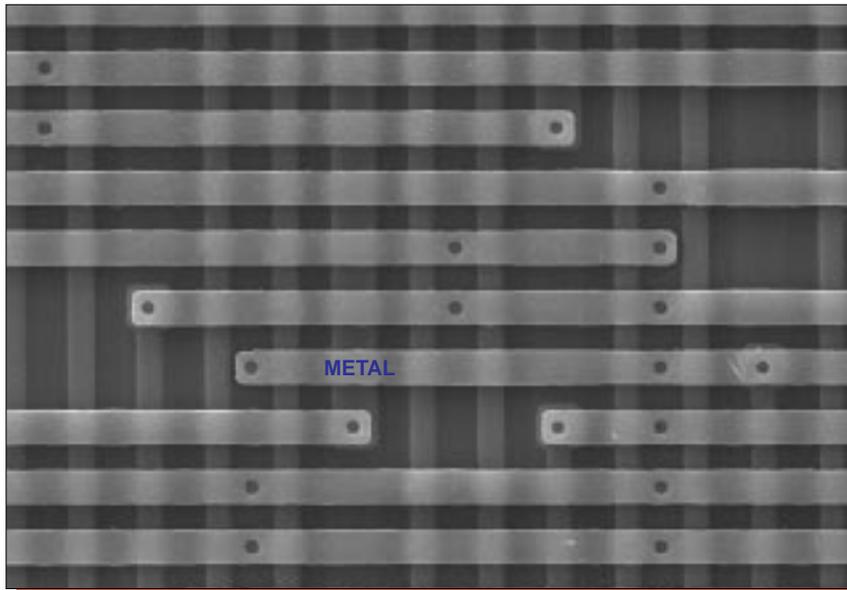


poly,  
Mag. 2600x

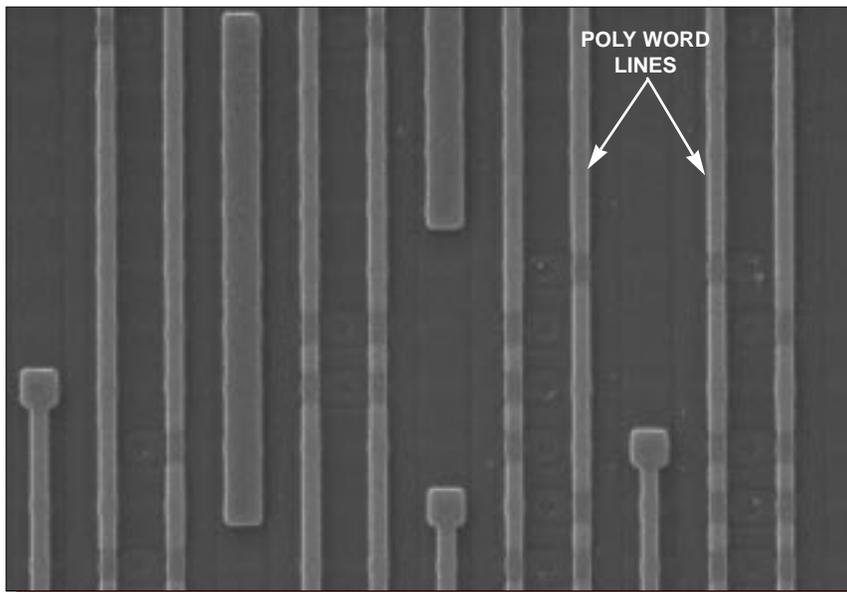


poly,  
Mag. 5000x

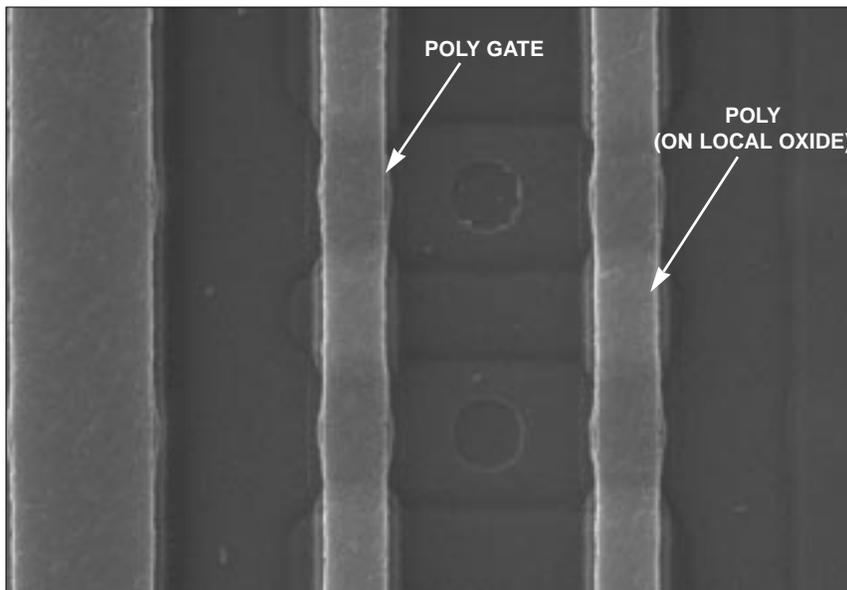
Figure 22. Perspective SEM views of the MROM array. 60°.



metal,  
Mag. 1600x

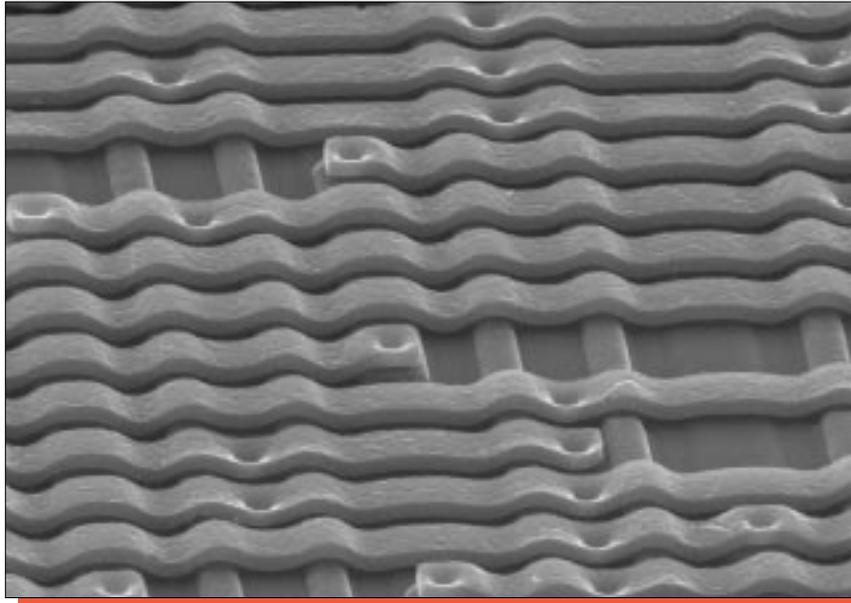


poly,  
Mag. 1600x

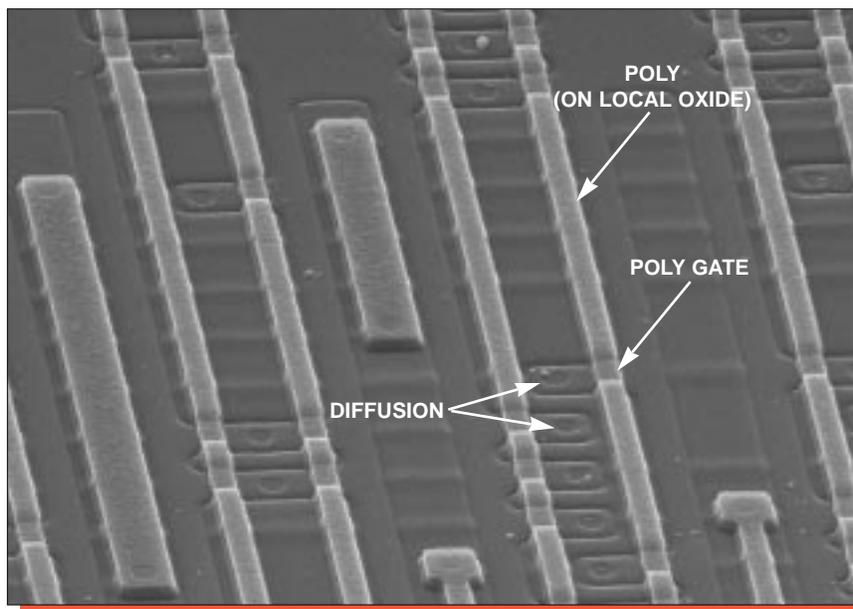


poly,  
Mag. 6500x

Figure 23. Topological SEM views of an additional MROM array on the 93C46CB1. 0°.

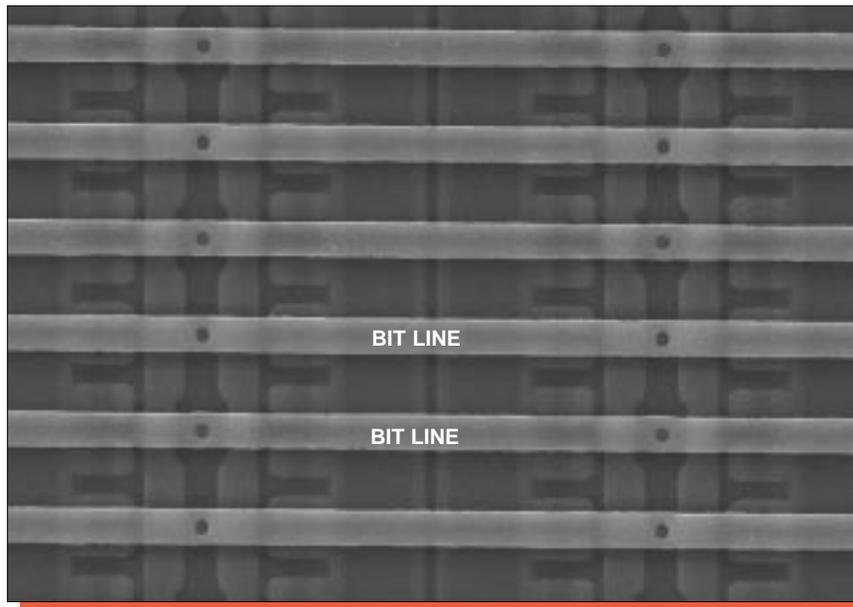


metal

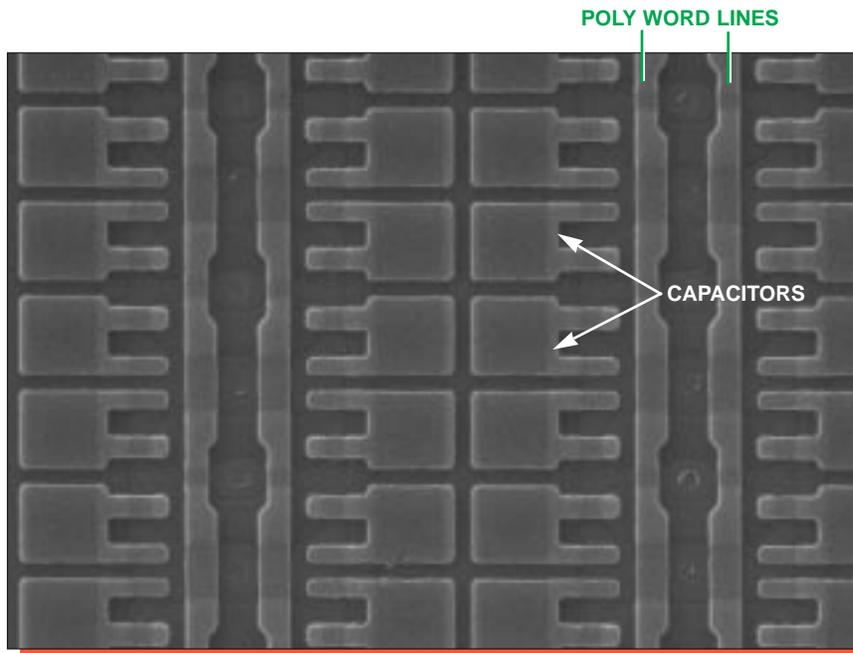


poly

Figure 24. Perspective SEM views of the MROM array. Mag. 2600x, 60°.

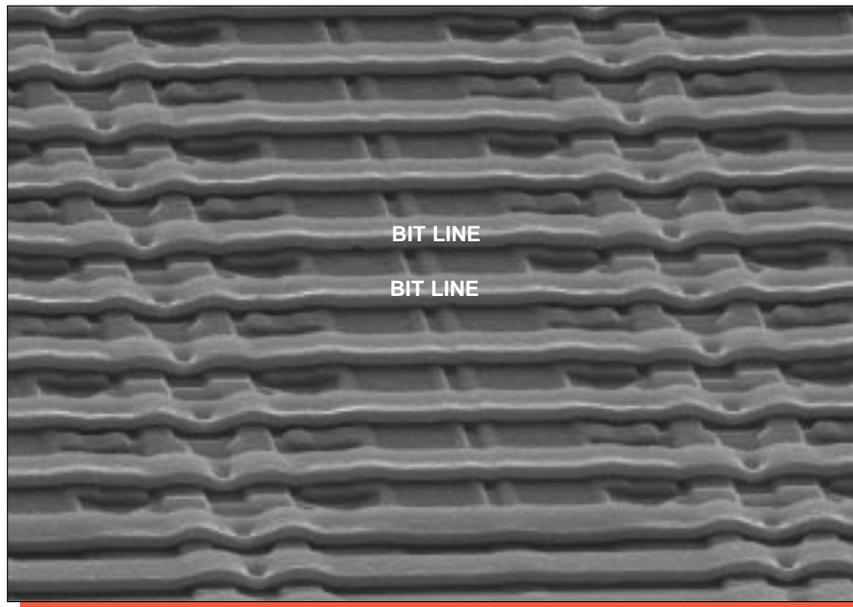


metal

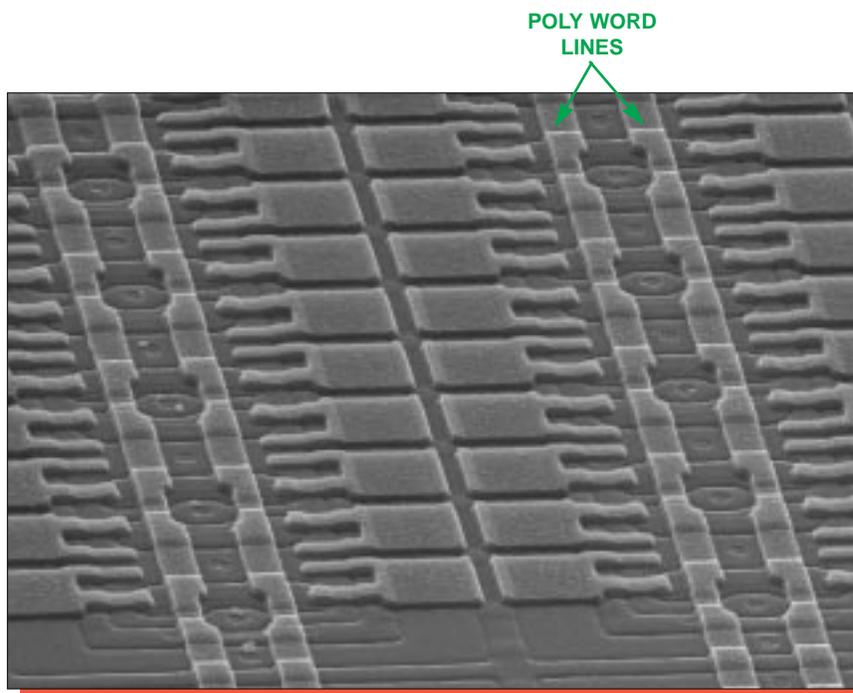


poly

Figure 25. Topological SEM views of the EEPROM array. Mag. 1600x, 0°.

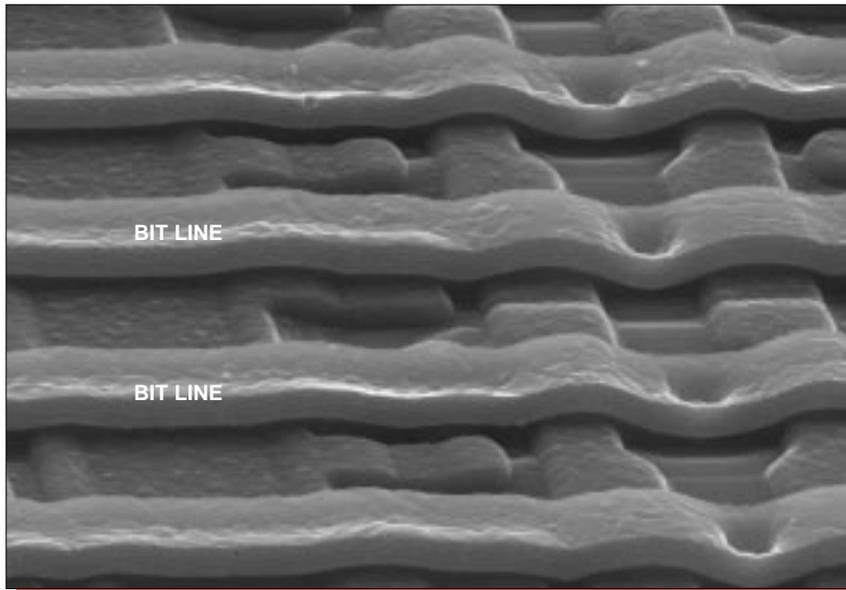


metal



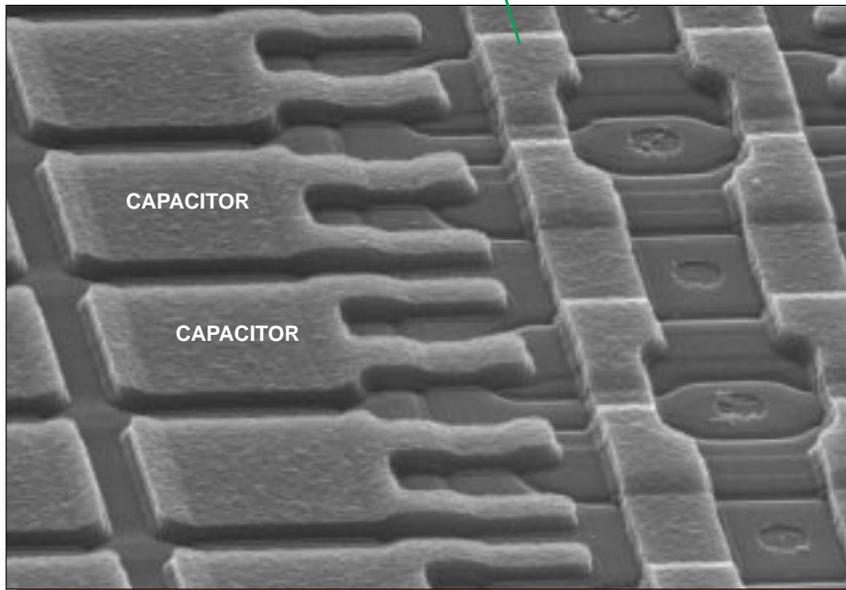
poly

Figure 26. Perspective SEM views of the EEPROM array. Mag. 2000x, 60°.

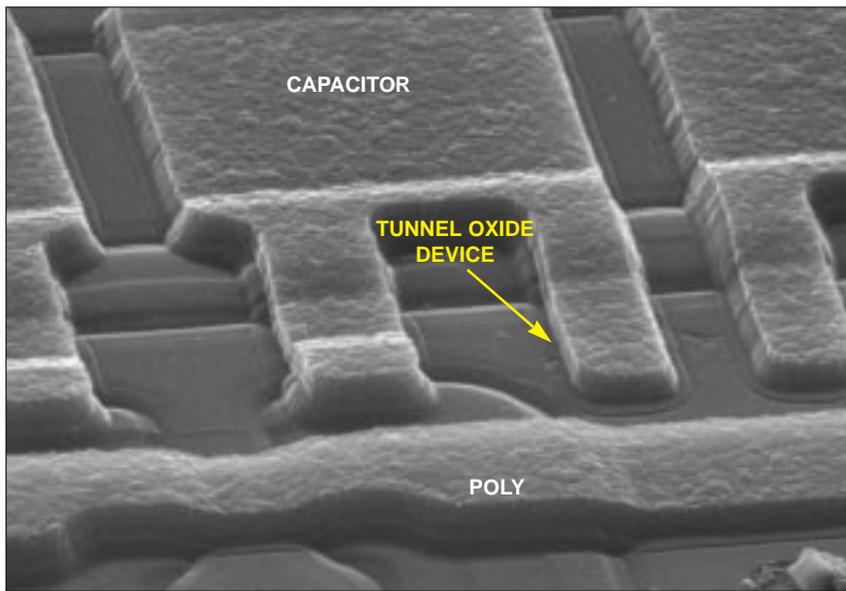


metal,  
Mag. 5000x

POLY WORD LINE



poly,  
Mag. 5000x



poly,  
Mag. 10,000x

Figure 27. Detail views of the EEPROM array. 60°.

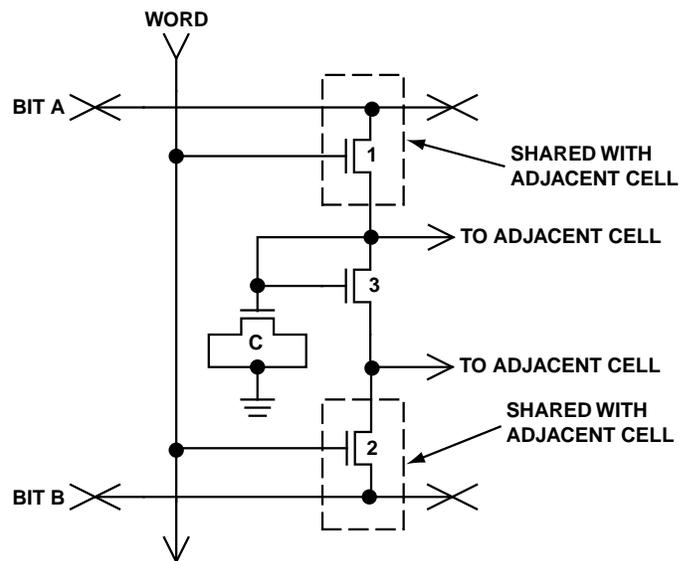
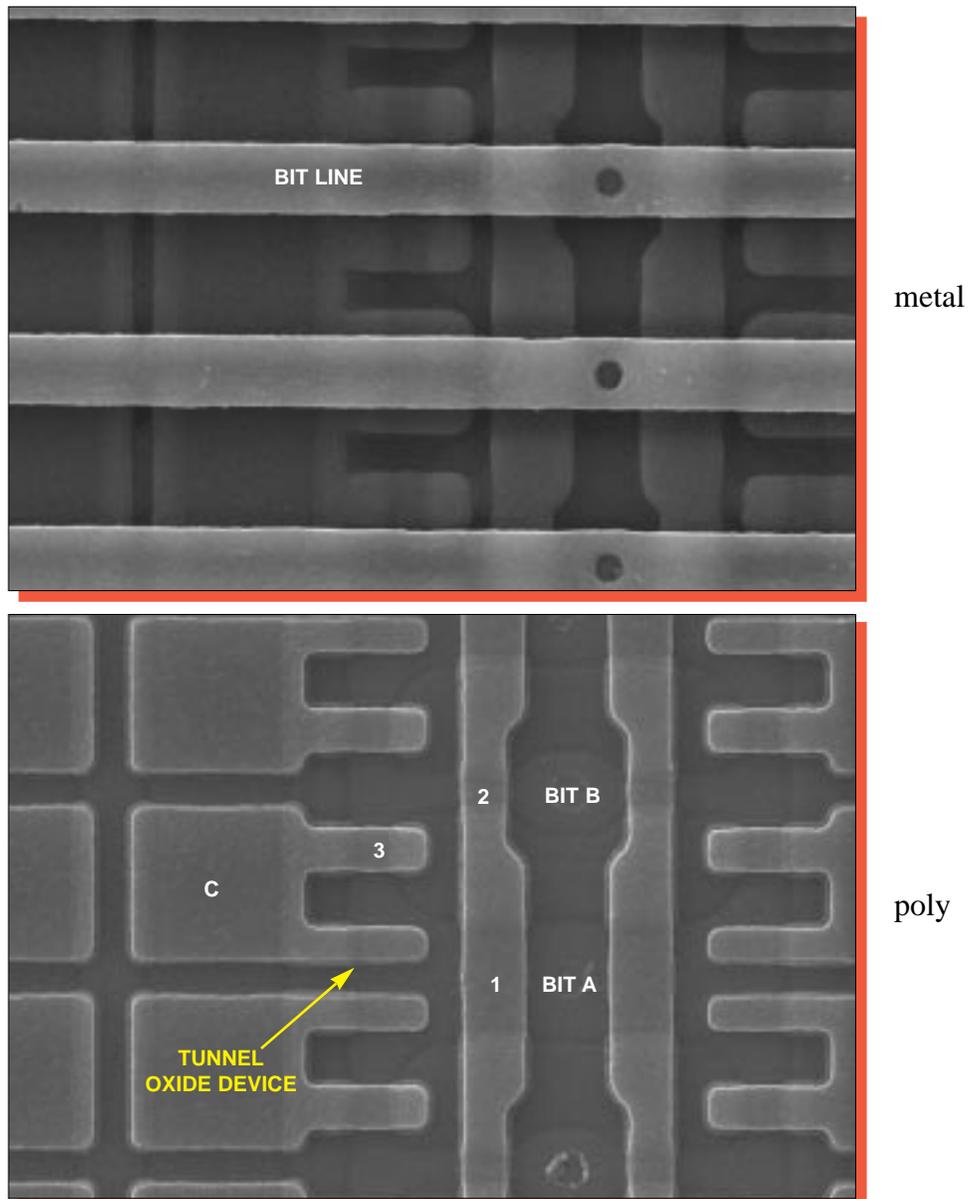


Figure 28. Topological SEM views of an EEPROM cell along with the schematic.  
Mag. 3300x, 0°.

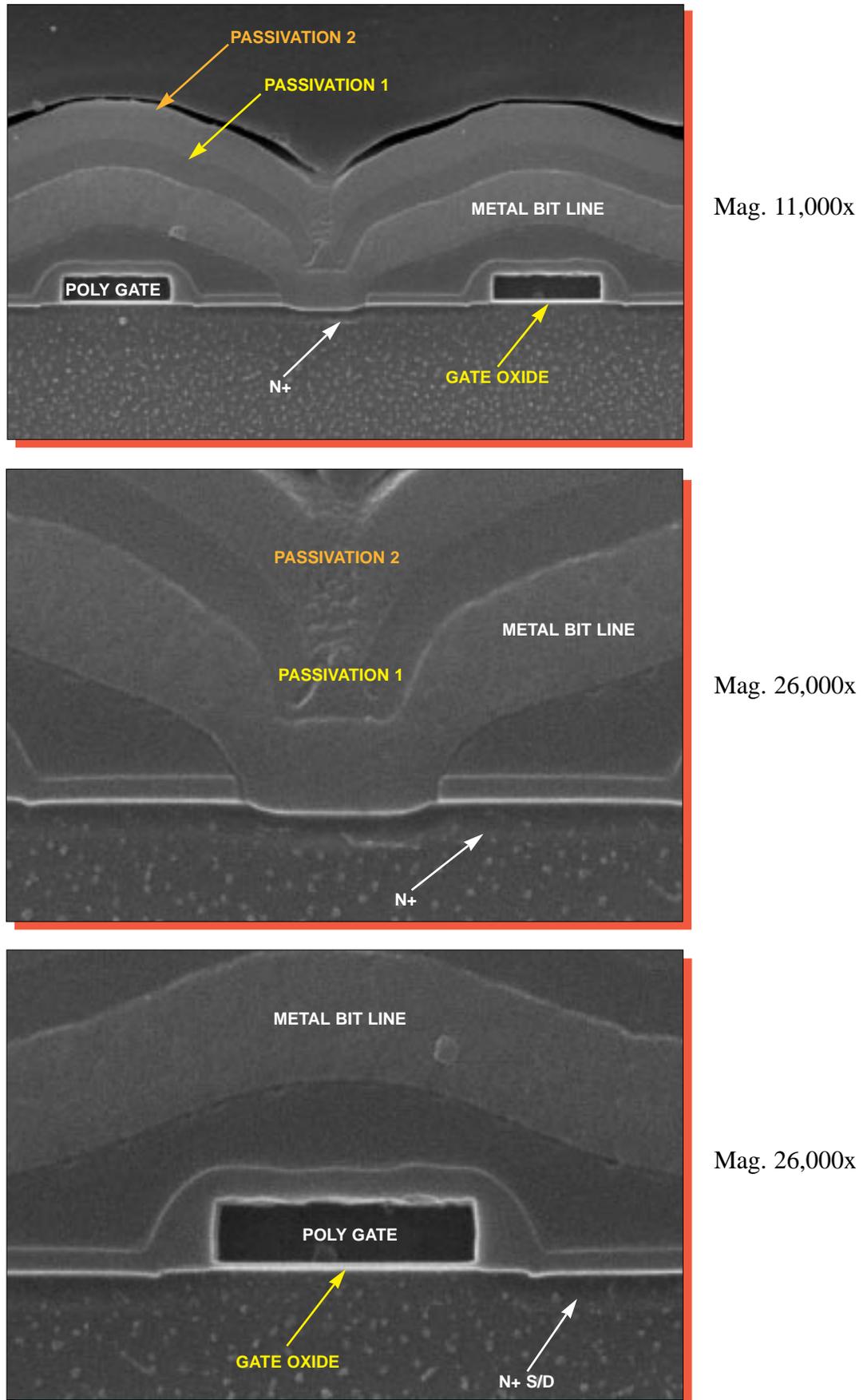
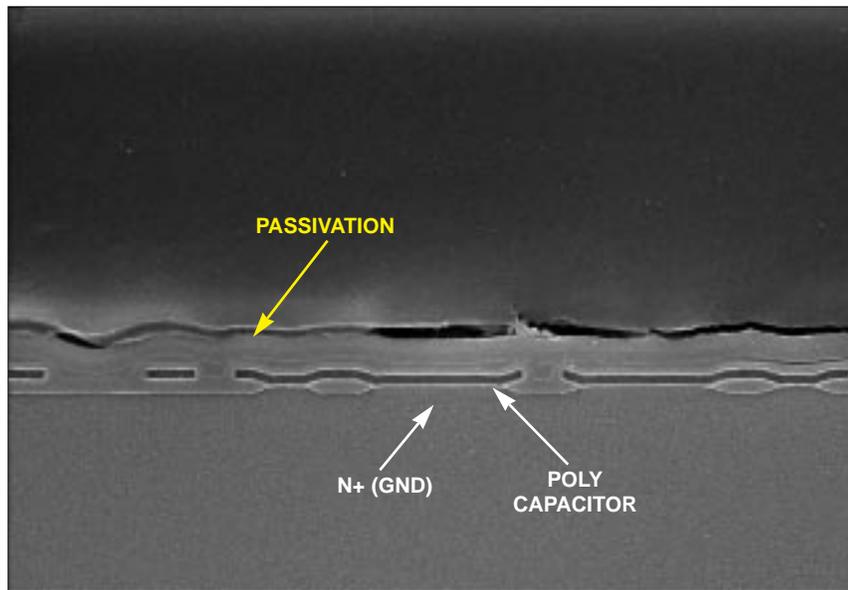
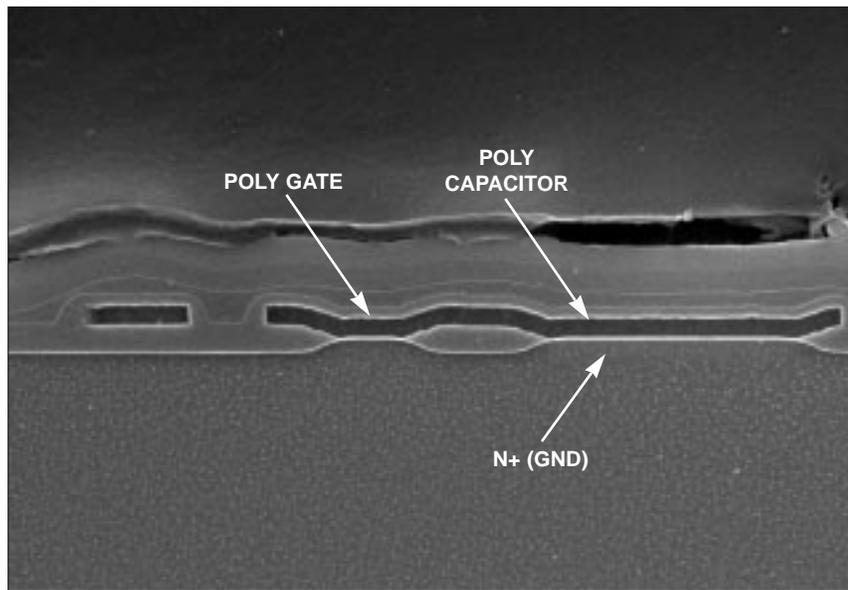


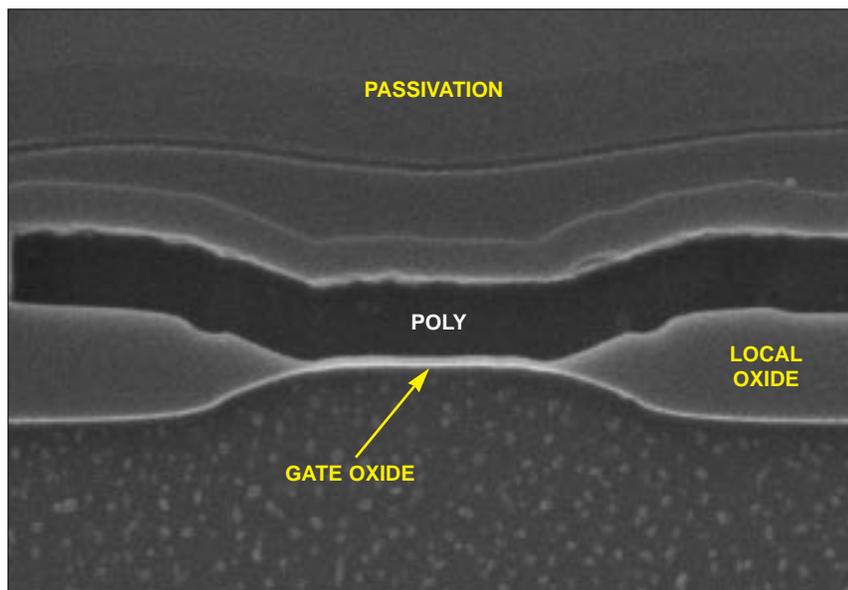
Figure 29. SEM section views of an EEPROM cell illustrating bit line contact and select gate.



Mag. 3300x

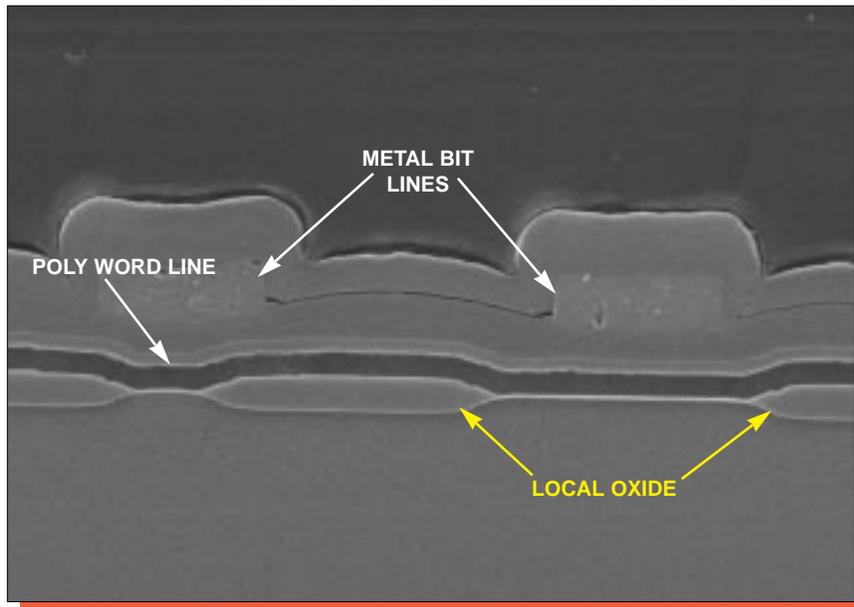


Mag. 6500x

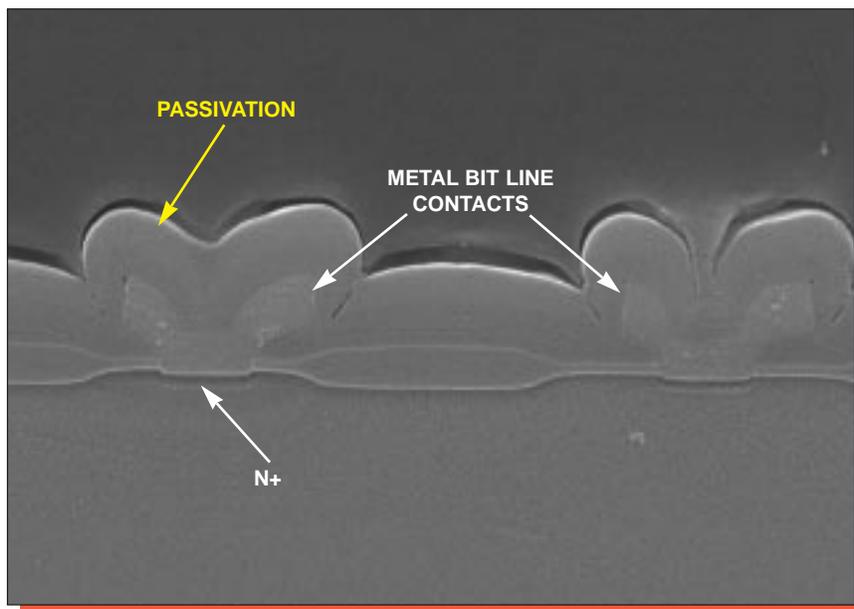


Mag. 26,000x

Figure 30. Detail SEM views of the EEPROM cell structure.

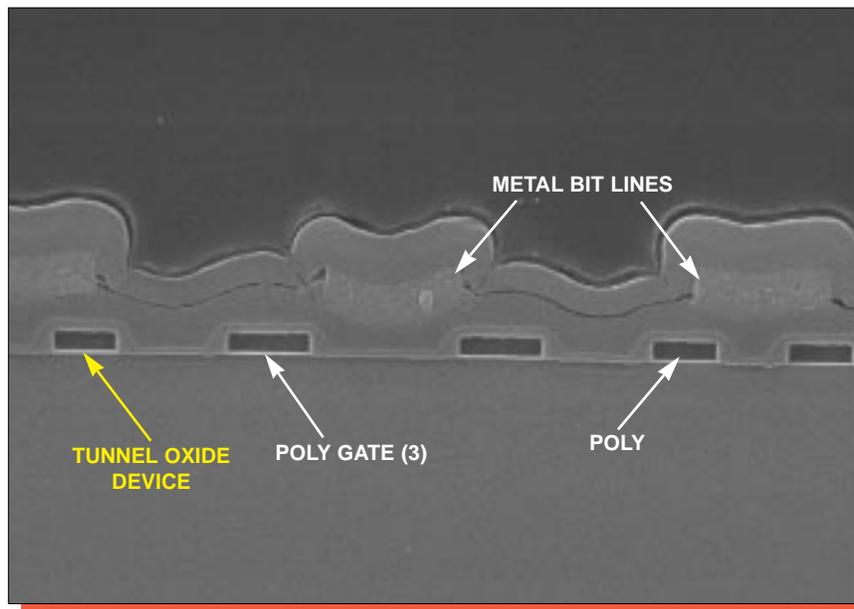


Mag. 8000x

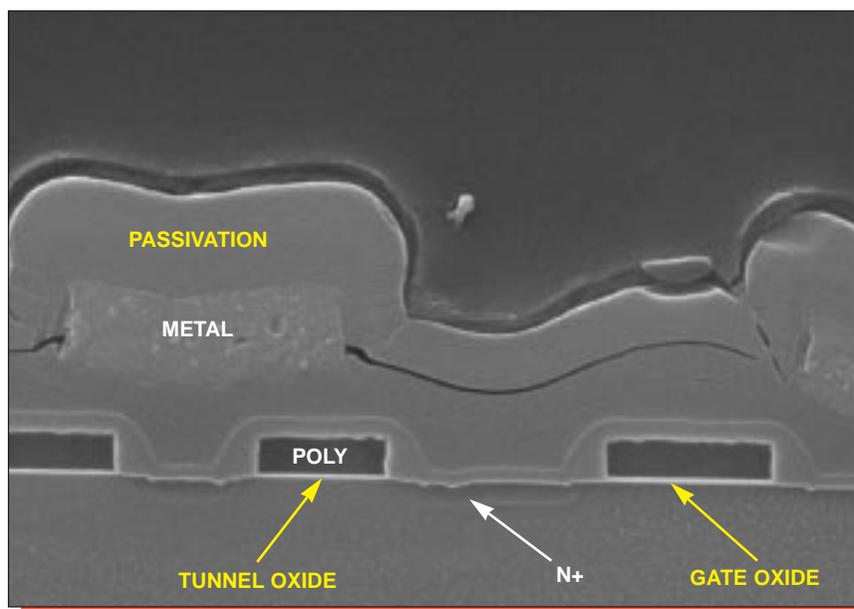


Mag. 9000x

Figure 31. SEM section views of EEPROM cells (perpendicular to bit lines).

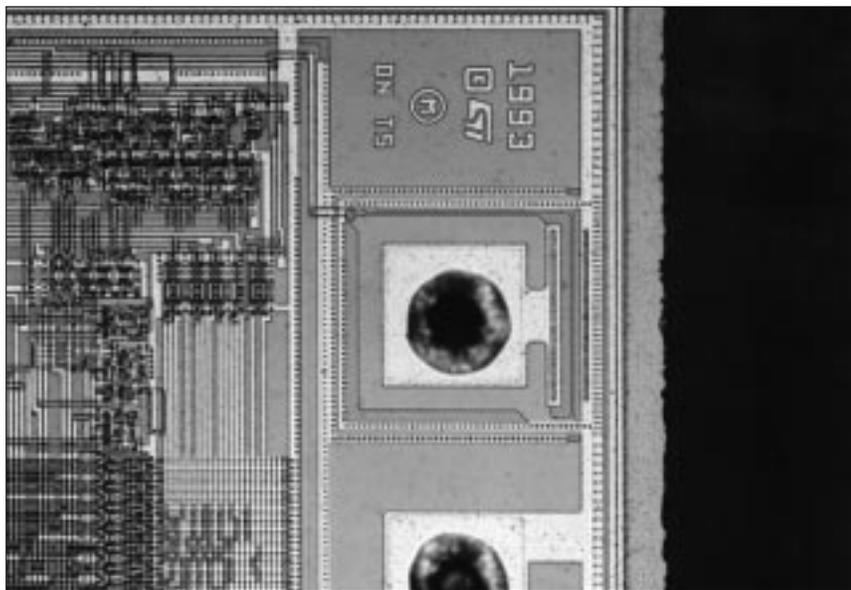


Mag. 6500x

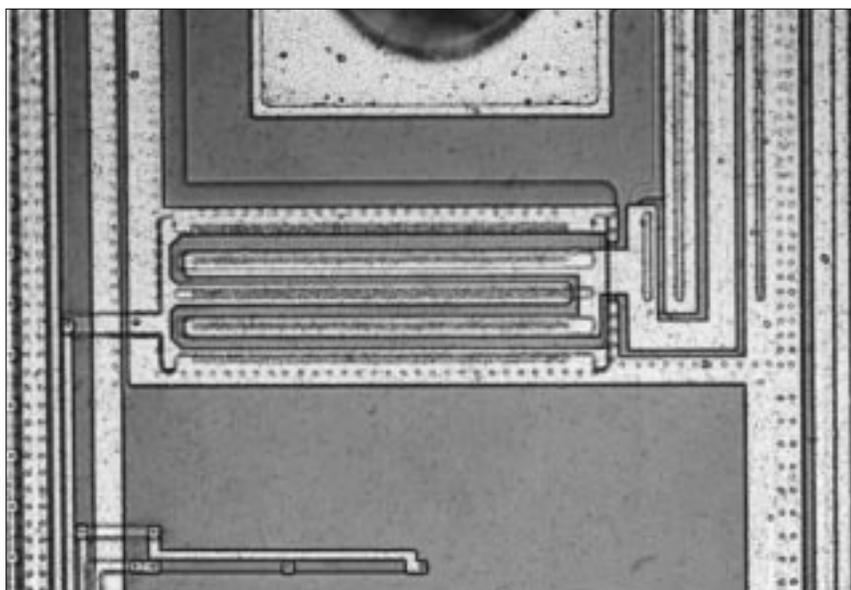


Mag. 13,000x

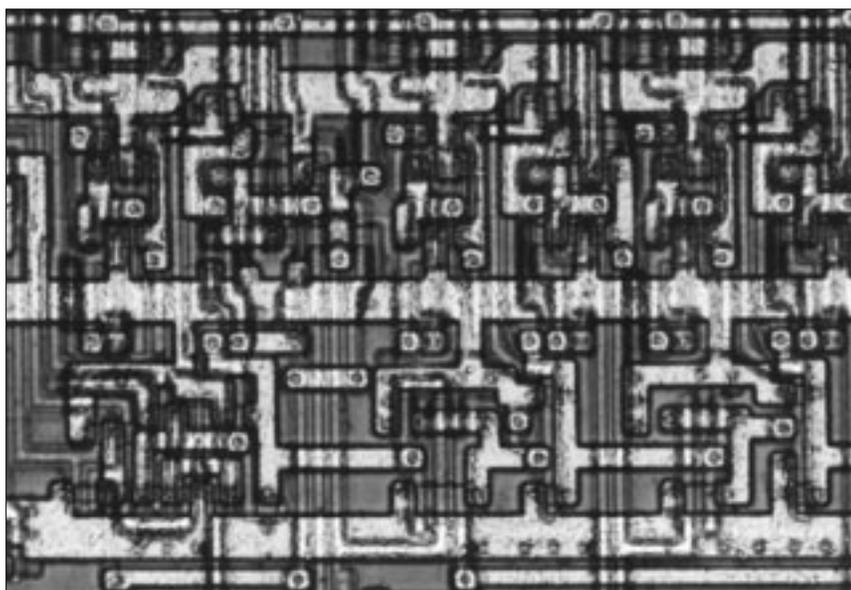
Figure 32. SEM section views of EEPROM cells (perpendicular to bit lines).



Mag. 160x



Mag. 400x



Mag. 800x

Figure 33. Optical views of input protection and typical circuit layout.