# Construction Analysis

# SGS-Thomson M17C1001
# 1Mb UVEPROM

Report Number: SCA 9612-518


INTEGRATED CIRCUIT ENGINEERING

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## INTRODUCTION

This report describes a construction analysis of the SGS M27C1001 1-MEG UVEPROM. Five devices packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs) with a quartz window were received for the analysis. Devices were date coded 9514.

## MAJOR FINDINGS

**Questionable Items:**[1] None.

**Special Features:**

- Tungsten plugs used at all contacts.
- Sub-micron gate lengths (0.5 N-channel and P-channel.)
- Sidewall spacers left in place on only one side in the array.
- Titanium on titanium-nitride barrier metal.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## TECHNOLOGY DESCRIPTION

**Assembly:**

- Devices were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs). A quartz window was present over the die.
- The package consisted of two ceramic halves held together by a glass frit. The die was mounted to the cavity floor using a silver-filled glass.
- Die separation was by sawing.
- Wirebonding was by the ultrasonic wedge bond method using 1.2 mil O.D. aluminum wire.
- All pins were connected and pins 16 and 32 (Vcc and Vss) had multiple bonding wires.

**Die Process:**

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of two layers of silicon-dioxide.
- Metallization consisted of a single layer of dry-etched aluminum with a titanium-nitride cap and titanium over titanium-nitride barrier. Tungsten plugs were used at all contacts.
- Pre-metal dielectric consisted of a layer of borophosphosilicate glass (BPSG) over densified oxides. The glass was reflowed prior to contact cuts only.

**TECHNOLOGY DESCRIPTION (continued)**

- Two layers of poly were used on the die. Poly 2 (tungsten silicide) was used to form all gates on the die and the select/word line in the EPROM cell. Poly 1 (no silicide) was used exclusively in the cell to form the floating gates. Direct poly-to-diffusion (buried) contacts were not used. Interpoly dielectric consisted of oxide only (no nitride).

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A slight step was present at the edge of the well indicating a twin-well process was used.

- Memory cells consisted of a standard stacked poly EPROM design. Metal was used to form the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. Sidewall spacers were left on only one side of the gates in the array.

- Redundancy fuses were not present.

## ANALYSIS RESULTS I

**Package and Assembly:** **Figures 1 - 4**

**Questionable Items:**[1] None.

**Special Features:** None.

**General Items:**

- Devices were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs).
- Overall package quality: Good. No significant defects were noted in the external or internal portions of the package. No cracks or chips were present. The package consisted of two ceramic halves held together by a glass frit. A quartz window was present over the die.
- Leadframe: The leadframe was constructed of iron-nickel. Some small voids were noted internally in the glass frit seal; however; no cracks were noted and the overall effect is insignificant.
- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present.
- Die attach: A silver-filled glass was used to attach the die to the header.
- Wirebonding was by the ultrasonic wedge bond method using 1.2 mil O.D. aluminum wire. The clearance of the wires from the edge of the die was good. All bond pull strengths were normal (see page 10). No bond lifts occurred.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## ANALYSIS RESULTS II

**Die Process:** **Figures 5 - 30**

**Questionable Items:**[1] None.

**Special Features:**

- Tungsten plugs used at all contacts.
- Sub micron gate lengths (0.5 N-channel and P-channel).
- Sidewall spacers on only one side of gates in array.
- Titanium on titanium-nitride barrier metal.

**General Items:**

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: Two layers of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good.
- Metallization: A single layer of metal consisting of aluminum with a titanium-nitride cap and a titanium over titanium-nitride barrier. Tungsten plugs were used at all contacts.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

**ANALYSIS RESULTS II (continued)**

- Metal patterning: The metal layer was patterned by a dry etch of normal quality. Contacts were completely surrounded by metal.

- Metal defects: No voiding, notching, or neckdown was found in the metal layer. No silicon nodules were noted following the removal of the metal layer.

- Metal step coverage: Minimal aluminum thinning was present due to the use of plugs.

- Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) over various densified oxides was used under the metal. The phosphorus level was very high (see page 10). Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Contact cuts were defined by a dry-etch process. No significant over-etching of the contacts was noted.

- Polysilicon: Two layers of poly were used on the die. Poly 2 (tungsten silicide) was used to form all gates on the die and the select/word line in the EPROM cell. Poly 1 (no silicide) was used exclusively in the cell array to form the floating gates. Direct poly-to-diffusion (buried) contacts were not used. Interpoly dielectric consisted of a thin layer of oxide only (no nitride). Definition was by a dry etch of normal quality. No poly stringers or spurs were present.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

- Isolation: Local oxide (LOCOS) isolation was used. The slight step present at the well boundary indicates a twin-well process was employed.

- EPROM array: The memory cells consisted of a standard stacked poly EPROM design. Metal was used to form the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. Interpoly dielectric consisted of oxide only. Cell pitch was 1.9 x 1.9 micron.

- Redundancy fuses were not present on the die.

## PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Delid

Internal optical inspection

SEM of passivation

Passivation integrity test

Wirepull test

Passivation removal

SEM inspection of metal

Metal removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Good

**DETAIL OF EVALUATION**

| | |
|---|---|
| Package integrity | N |
| Package markings | N |
| Die placement | N |
| Wirebond placement | N |
| Wire spacing | N |
| Wirebond quality | N |
| Die attach quality | N |
| Dicing quality | N |
| Die attach method | Silver-filled glass |
| Dicing method | Sawn |
| Wirebond method | Ultrasonic wedge bonds using 1.2 mil aluminum wire. |
| Die surface integrity: | |
| Toolmarks (absence) | G |
| Particles (absence) | G |
| Contamination (absence) | G |
| Process defects (absence) | G |
| General workmanship | G |
| Passivation integrity | G |
| Metal definition | N |
| Metal integrity | N |
| Contact coverage | G |
| Contact registration | G |

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## PACKAGE MARKINGS (TOP)

M27C1001
-15F1
BHHAI
(LOGO) 9514E
KOREA

## (BOTTOM)

M611
4108

## WIREBOND STRENGTH

Wire material: 1.2 mil O.D. aluminum
Die pad material: aluminum

**Sample #**

| | |
|---|---|
| # of wires pulled: | 22 |
| Bond lifts: | 0 |
| Force to break - high: | 7g |
| - low: | 5g |
| - avg.: | 5.8g |
| - std. dev.: | 0.6 |

## DIE MATERIAL ANALYSIS

| | |
|---|---|
| Overlay passivation: | Two layers of silicon dioxide with 4.0 wt. percent phosphorus. |
| Metallization: | Aluminum (Al) with a titanium-nitride (TiN) cap and a titanium (Ti) over titanium-nitride (TiN) barrier. |
| Poly: | Tungsten (W) silicide. |
| Pre-metal dielectric: | A layer of borophosphosilicate glass (BPSG) containing 9.75 wt. % phosphorus and 2.5 wt. % boron over densified oxides. |

## HORIZONTAL DIMENSIONS

| | |
|---|---|
| Die size: | 3.4 x 3.4 mm (134 x 134 mils) |
| Die area: | 11.5 $mm^2$ (17,956 $mils^2$) |
| Min pad size: | 0.14 x 0.14 mm (5.6 x 5.6 mils) |
| Min pad window: | 0.13 x 0.13 mm (5.2 x 5.2 mils) |
| Min pad space: | 1.1 mils |
| Min metal width: | 1.3 micron |
| Min metal space: | 1.0 micron |
| Min metal pitch: | 2.3 microns |
| Min contact: | 0.7 micron |
| Min poly 2 width: | 0.5 micron |
| Min poly 2 space: | 0.6 micron |
| Min poly 1 width: | 0.5 micron |
| Min gate length - (N-channel):* | 0.5 micron |
| - (P-channel): | 0.5 micron |
| Cell gate: | 0.5 micron |
| Cell pitch: | 1.9 x 1.9 micron |
| Cell size: | 3.6 microns |

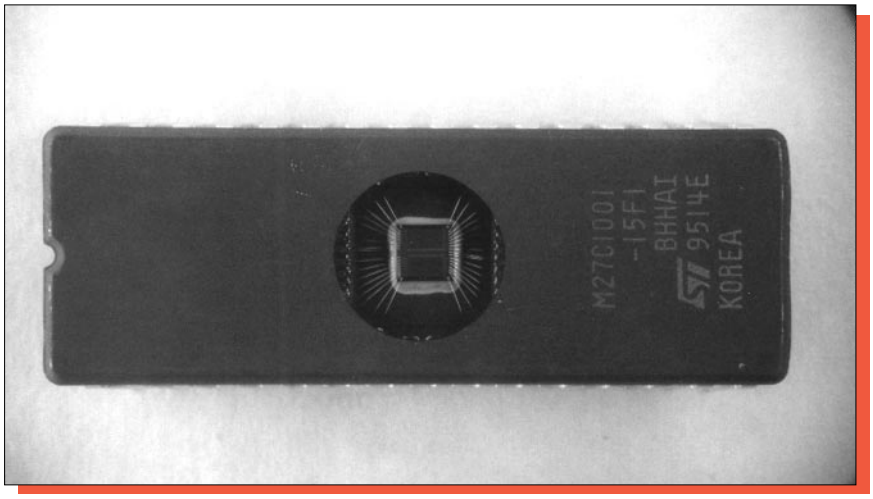
## VERTICAL DIMENSIONS

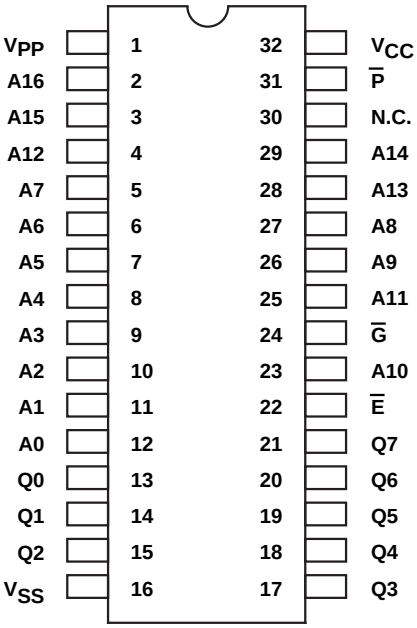
| | |
|---|---|
| Die thickness: | 0.5 mm (19 mils) |

**Layers:**

| | |
|---|---|
| Passivation 2: | 0.4 micron |
| Passivation 1: | 0.35 micron |
| Metal - cap: | 0.04 micron (approximate) |
| - aluminum: | 0.5 micron |
| - barrier: | 0.2 micron |
| - plugs: | 0.9 micron |
| Pre-metal dielectric: | 0.5 - 0.95 micron |
| Oxide on poly 2: | 0.1 micron |
| Poly 2 - silicide: | 0.2 micron |
| - poly 2: | 0.3 micron |
| Poly 1: | 0.15 micron |
| Local oxide: | 0.45 micron |
| N+ S/D: | 0.2 micron |
| P + S/D: | 0.25 micron |
| N-well: | 4.5 microns (approximate) |
| P-well: | Could not delineate |

**Physical gate length.*



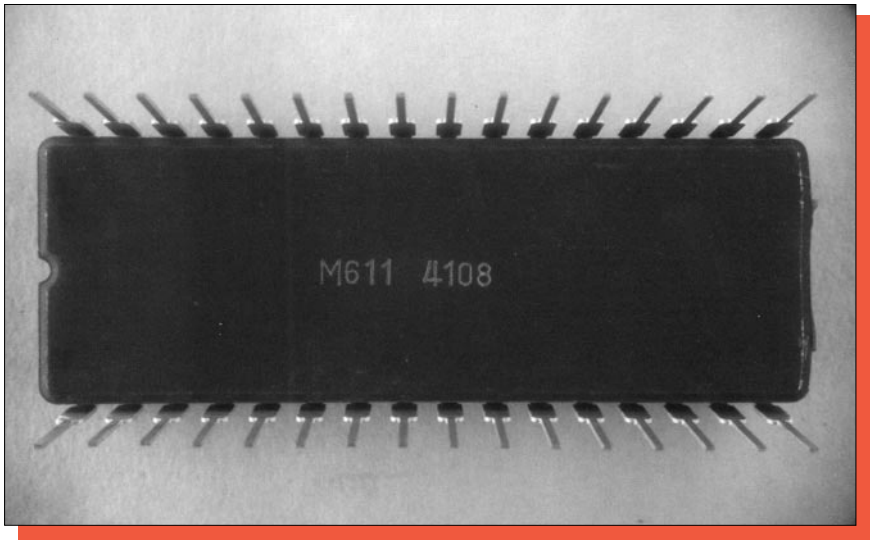




Figure 1. Package photograph and pinout of the SGS M27C1001. Mag. 2.4x.

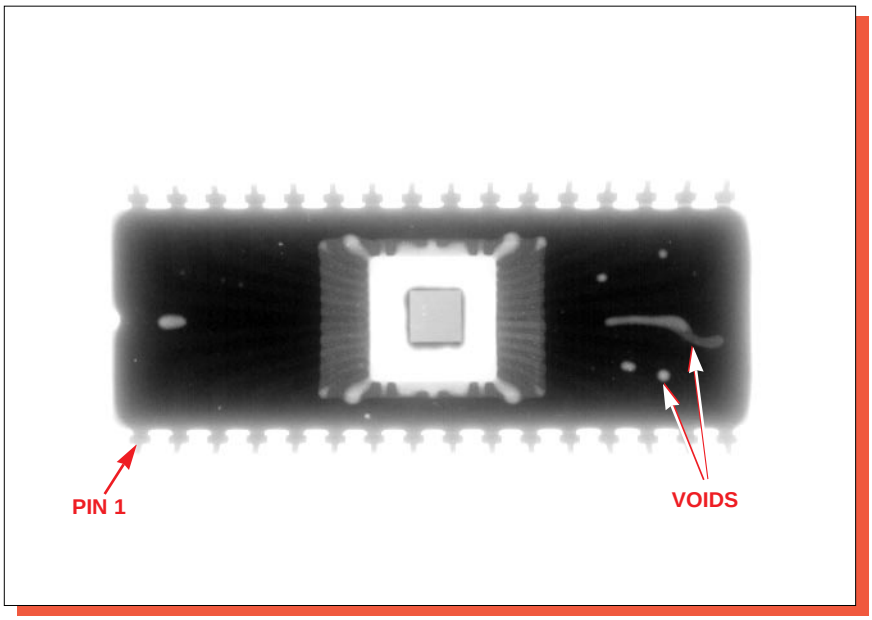
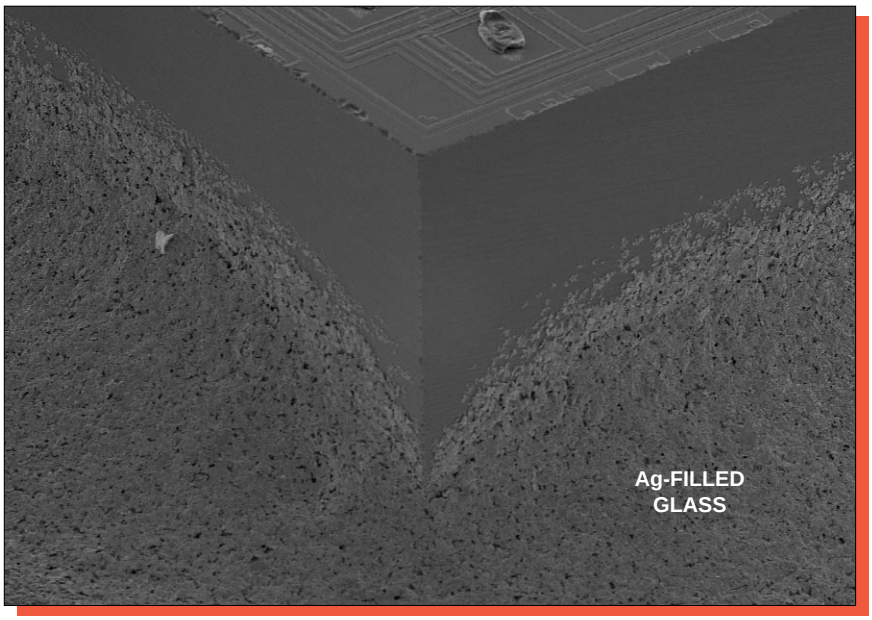
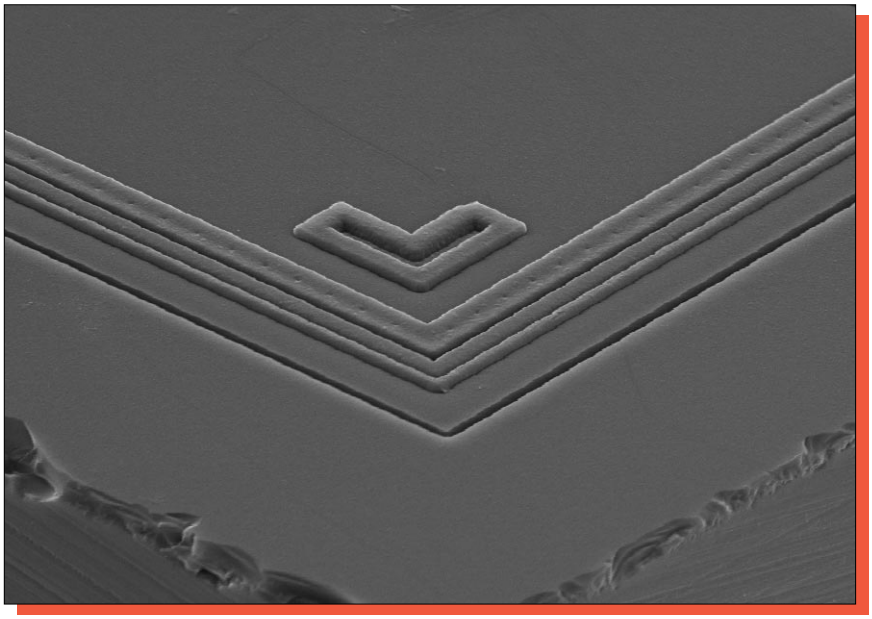



Figure 2. X-ray views of package. Mag. 2x.

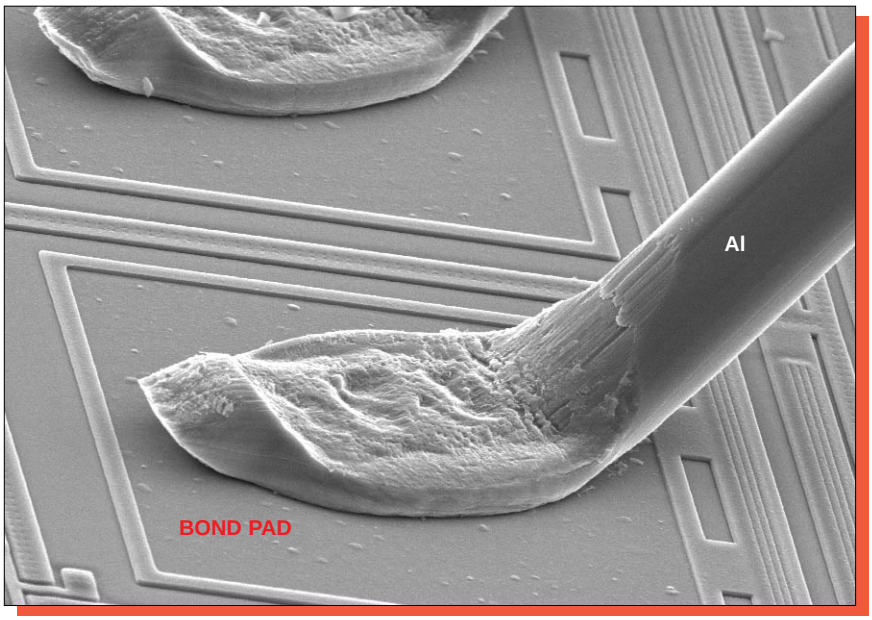



Mag. 100x



Mag. 1100x

Figure 3. SEM views of dicing and edge seal. 60°.



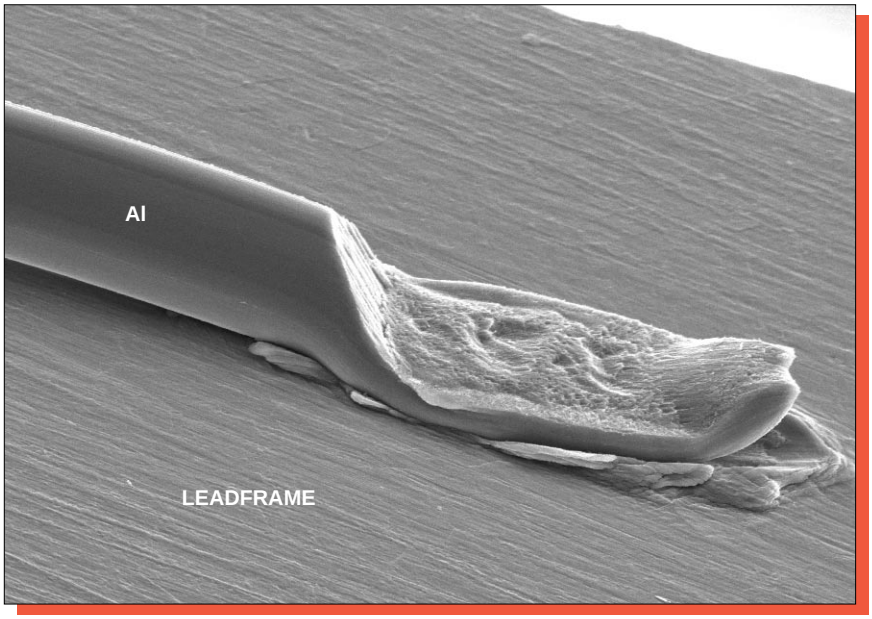




Figure 4. SEM views of typical wirebonding. Mag. 600x, 60°.

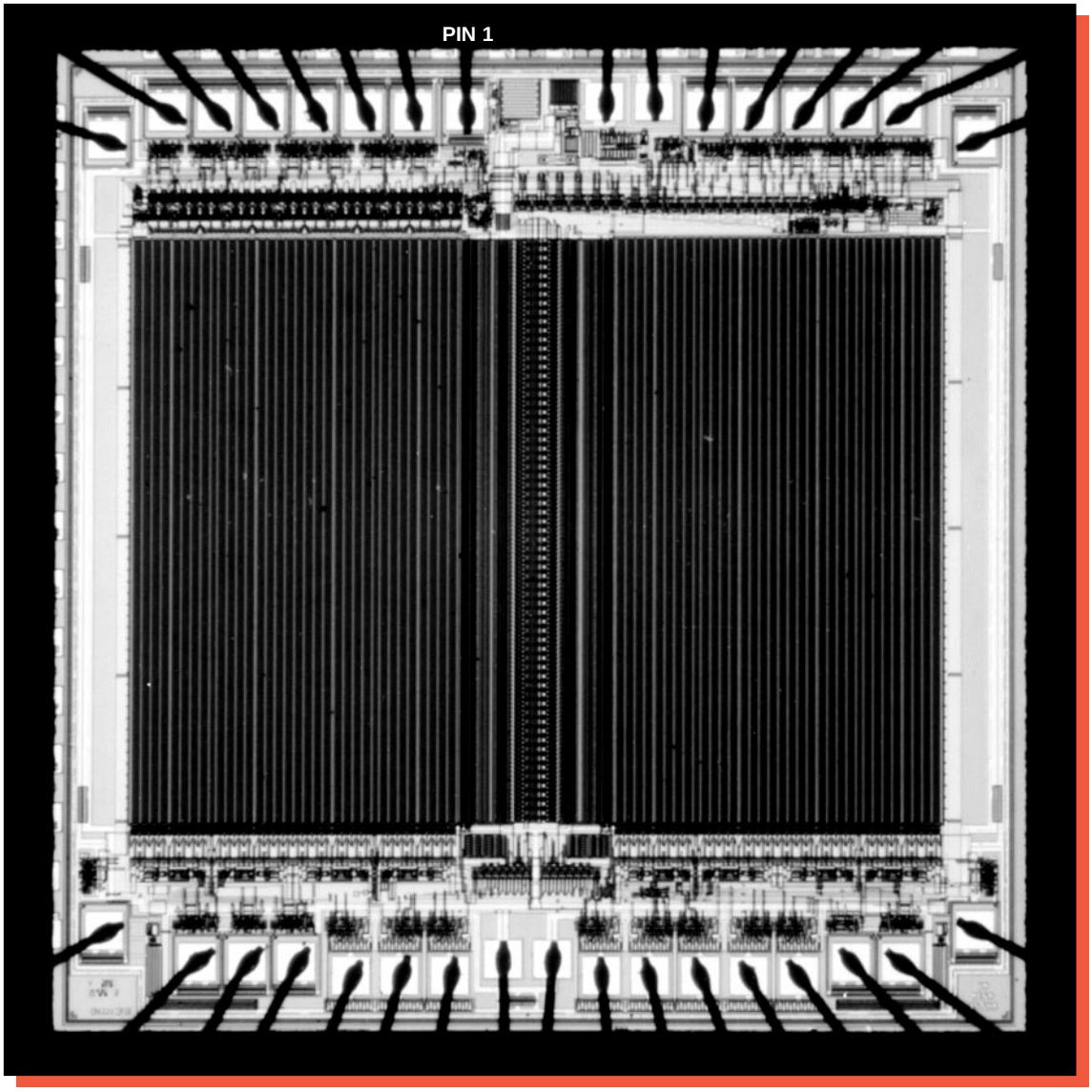



Figure 5. Whole die photograph of the SGS M27C1001. Mag. 40x.

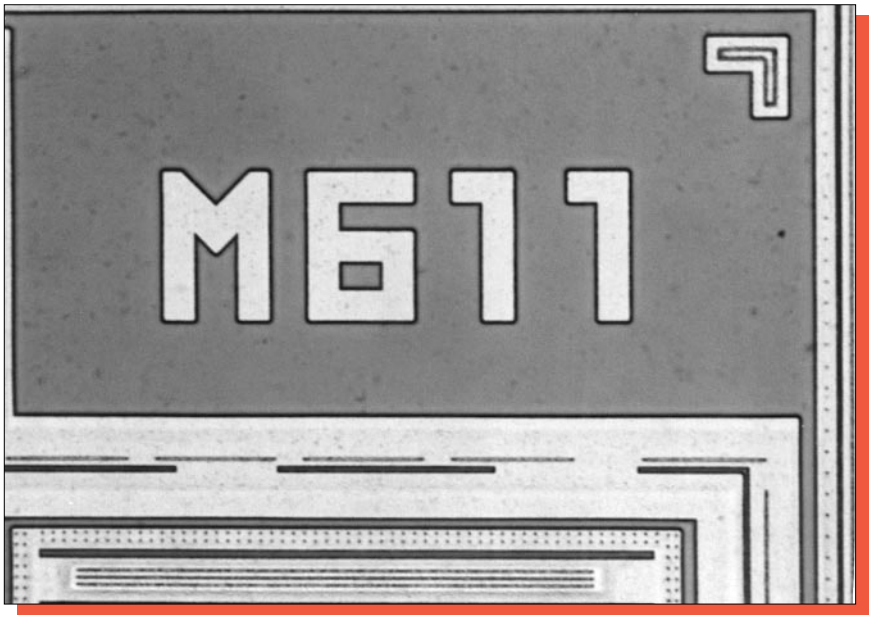
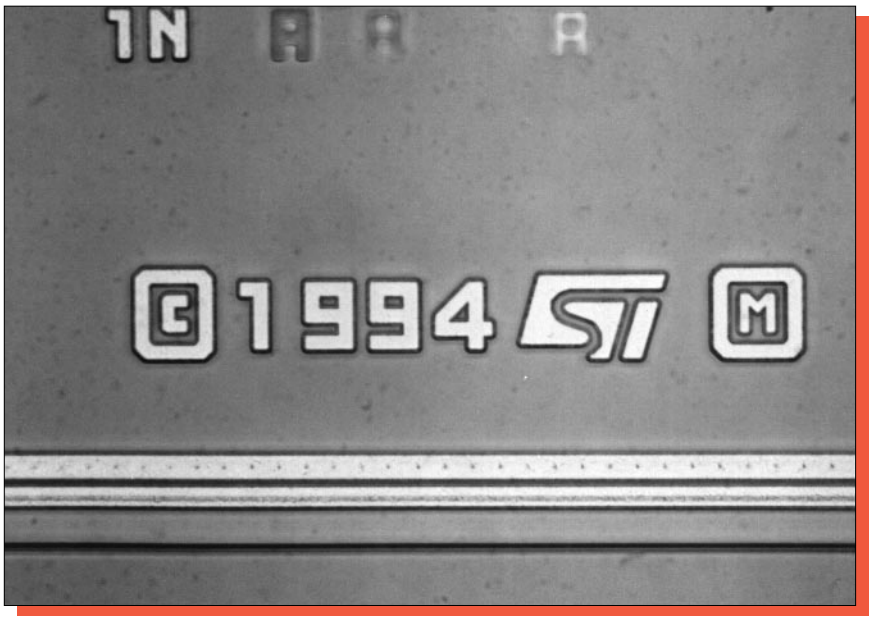
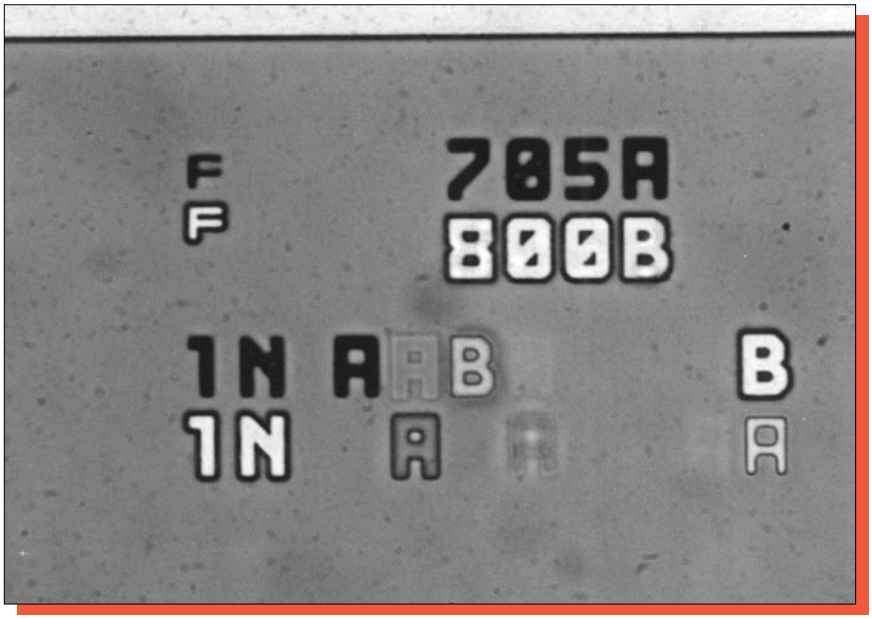




Figure 6. Optical photographs of markings on die surface. Mag. 500x.

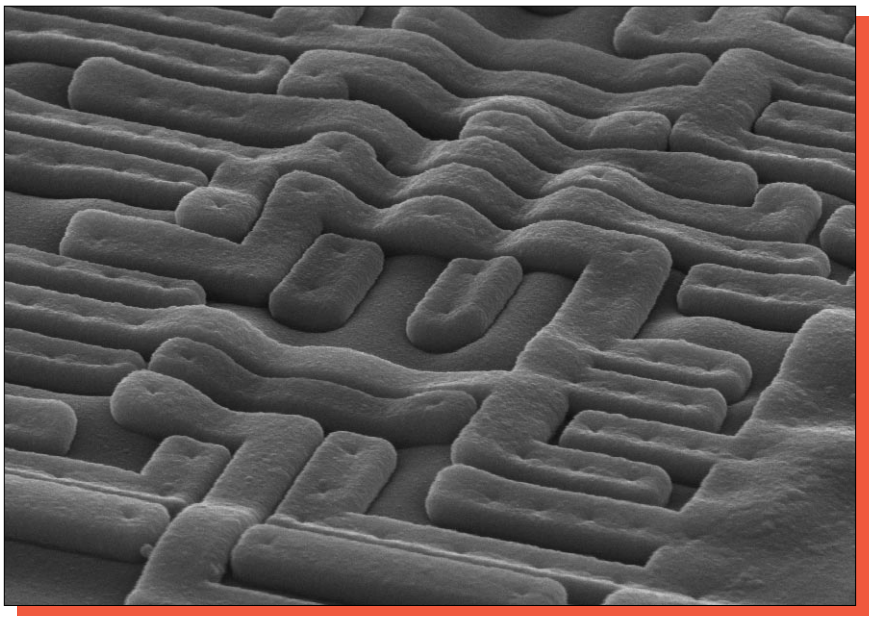



Mag. 645x

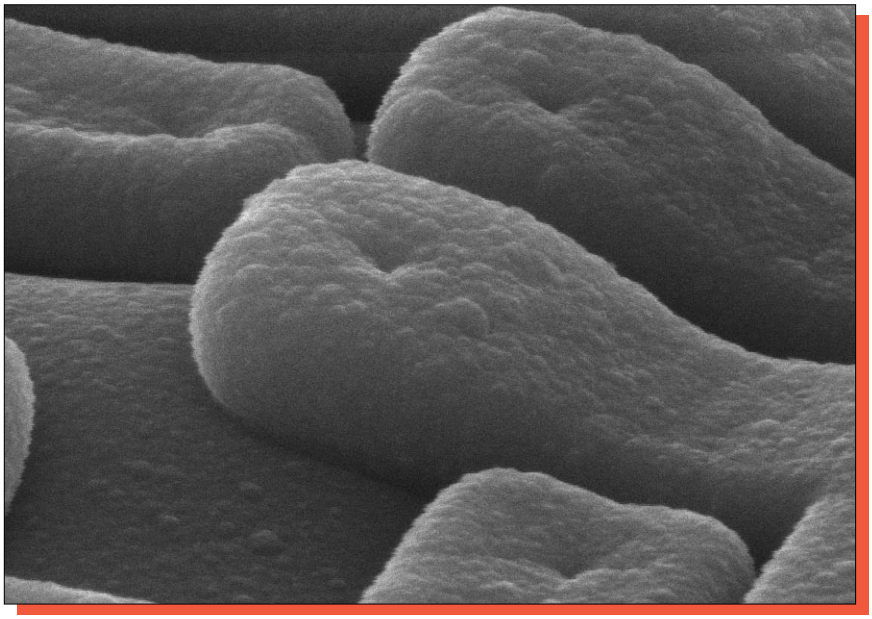



Mag. 800x

Figure 7. Additional optical photographs of markings on die surface.

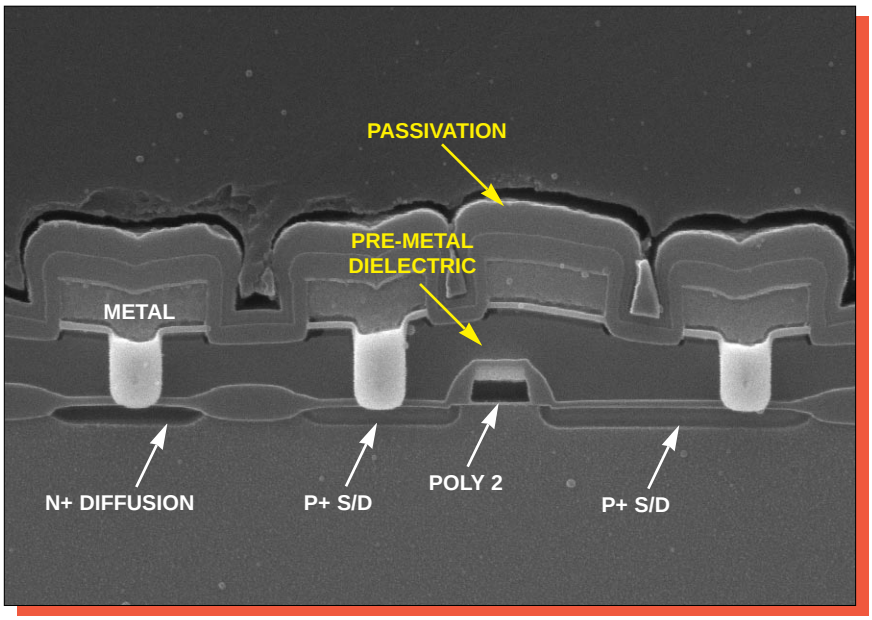


Mag. 3500x

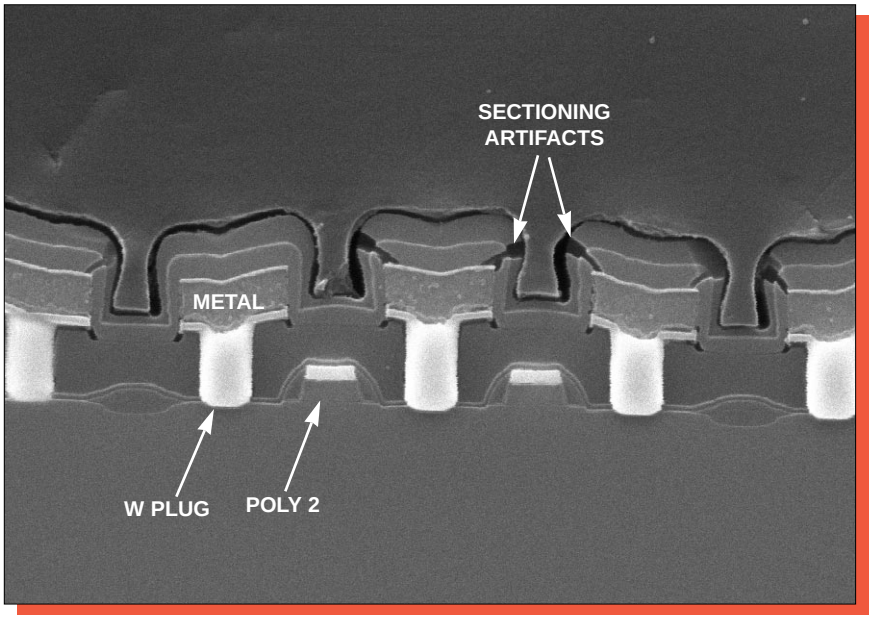


Mag. 17,000x

Figure 8. Perspective SEM views of overlay passivation coverage. 60°.

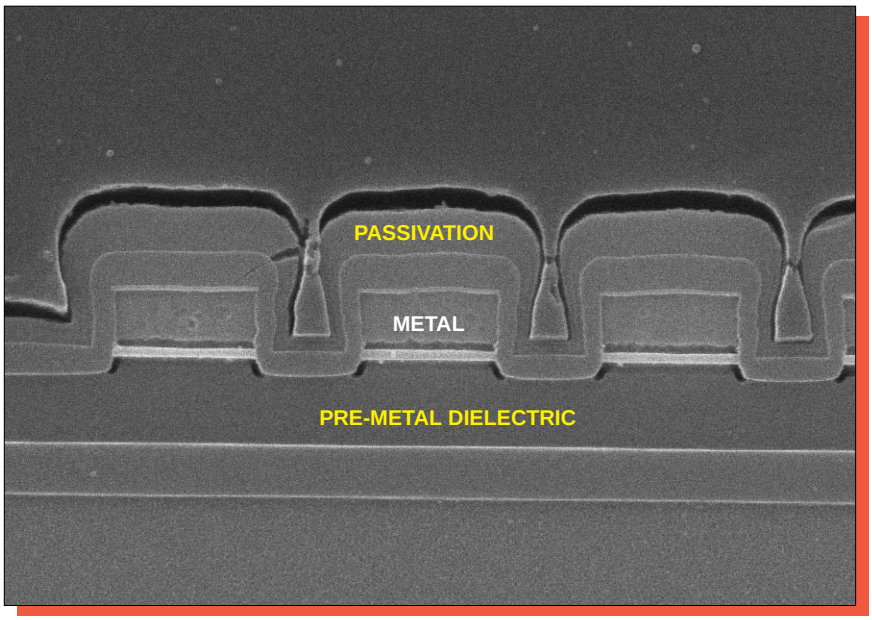



silicon etch

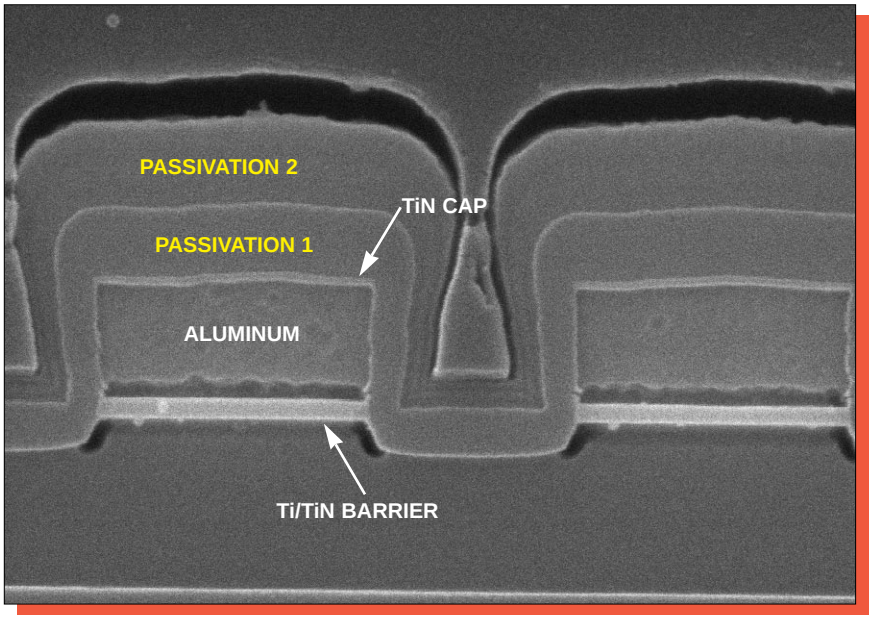



glass etch

Figure 9. SEM section views of general circuitry. Mag. 10,000x.

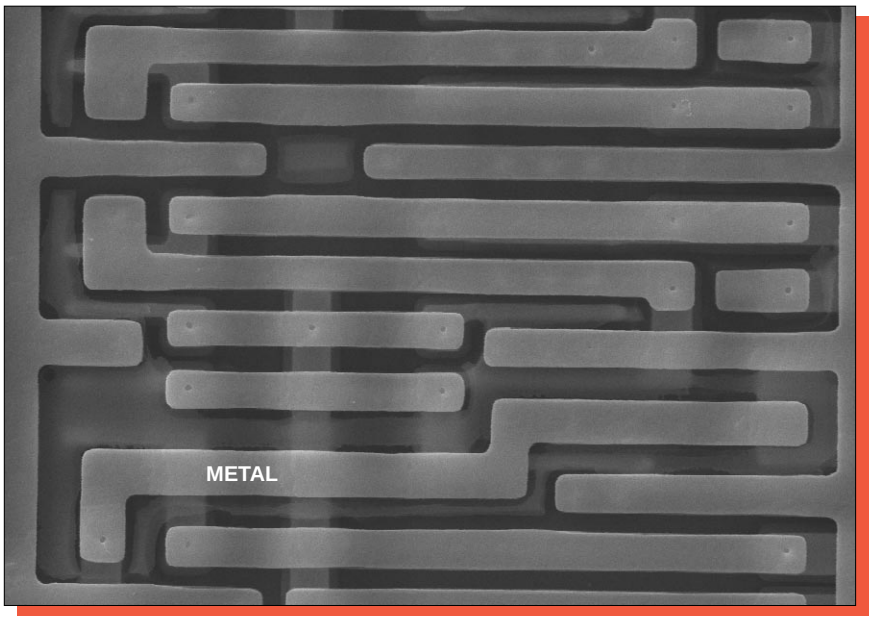



Mag. 13,000x

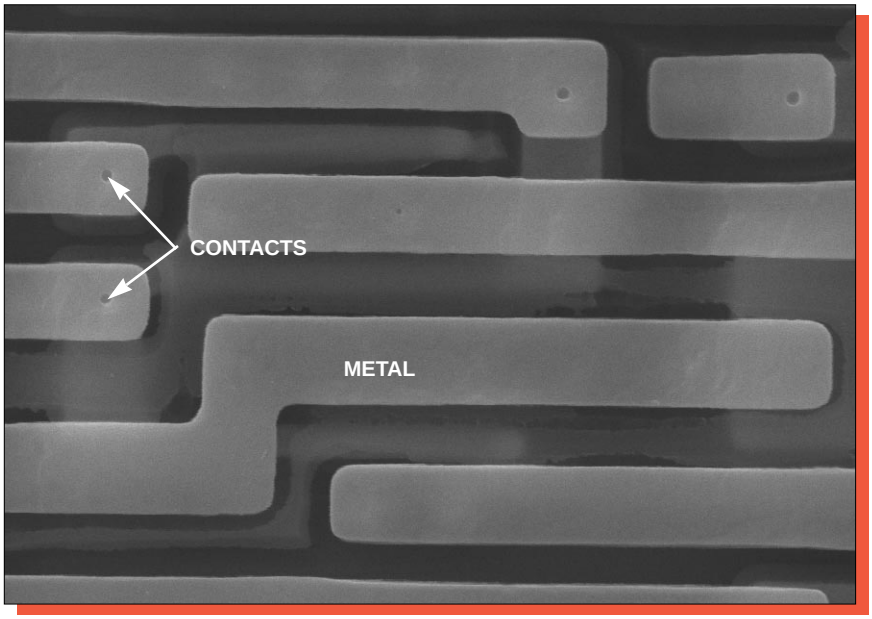



Mag. 26,000x

Figure 10. SEM section views of metal line profiles.

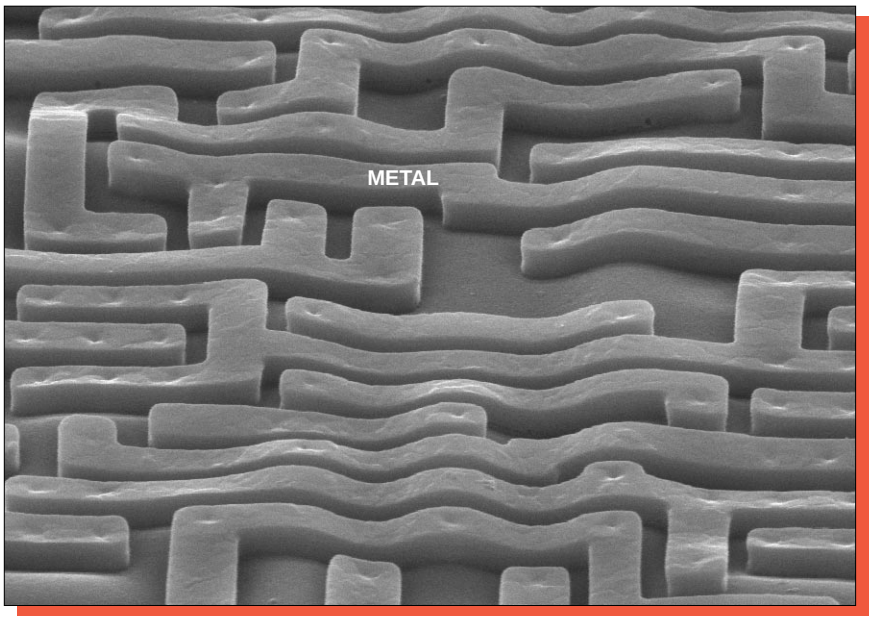



Mag. 3200x

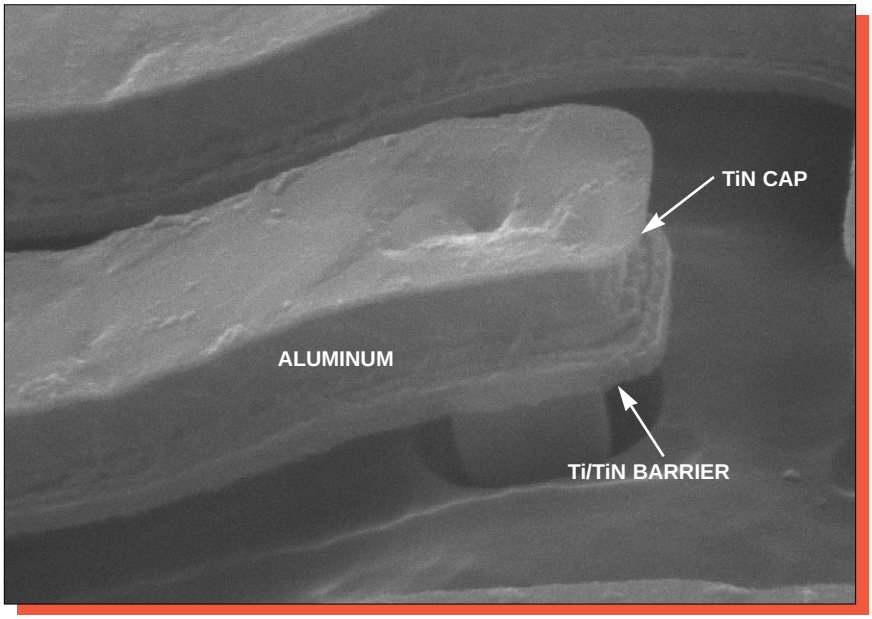



Mag. 6500x

Figure 11. Topological SEM views of metal patterning. 0°.

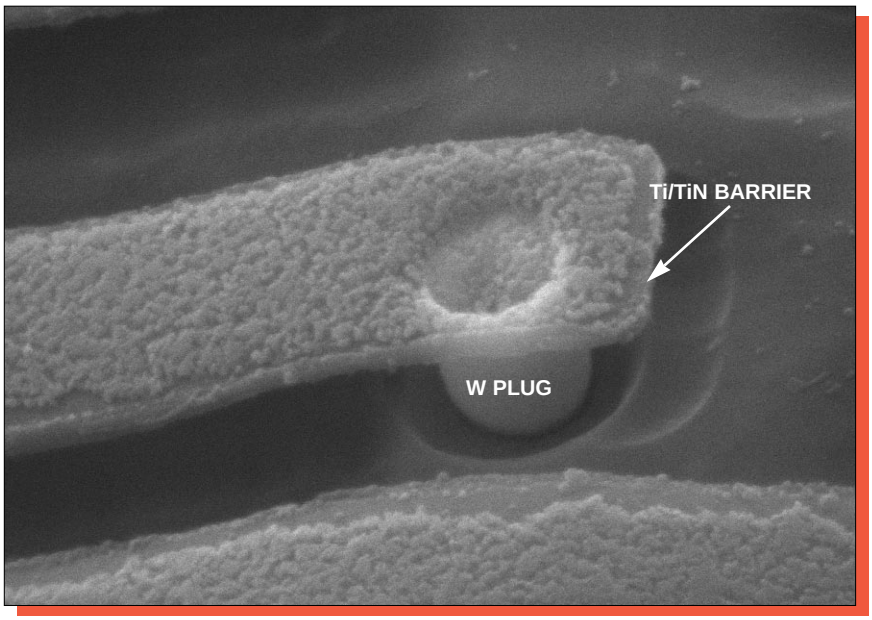



Mag. 4200x

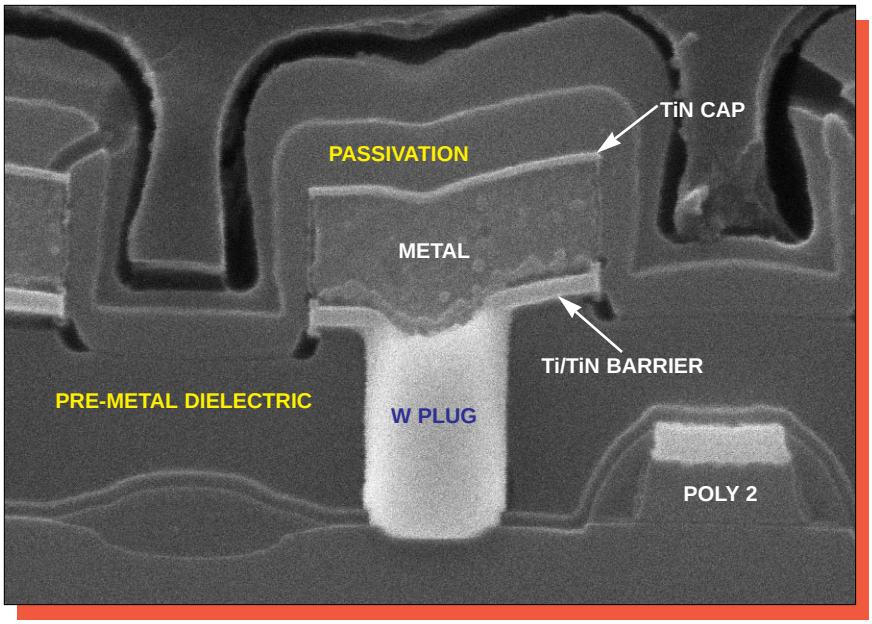



Mag. 26,000x

Figure 12. SEM views of metal coverage. 60°.

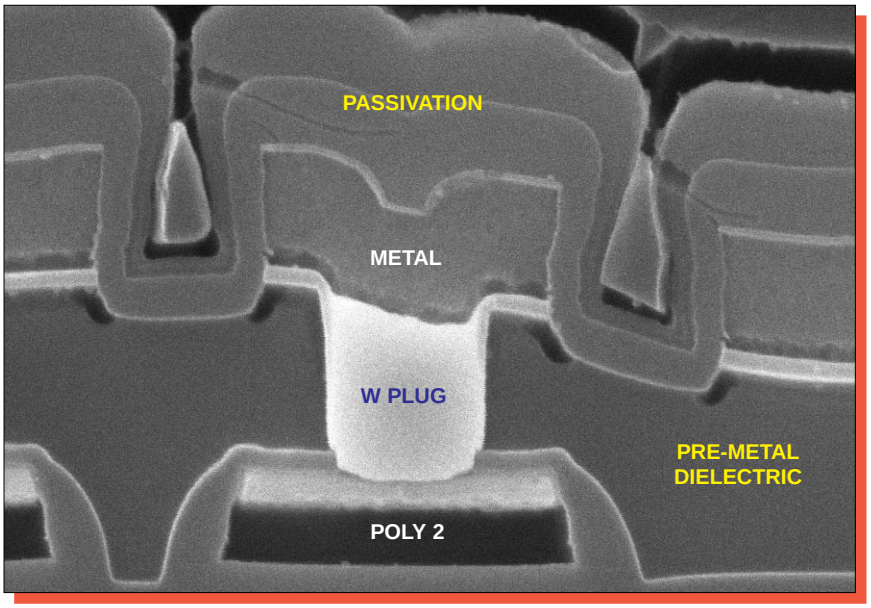



45°

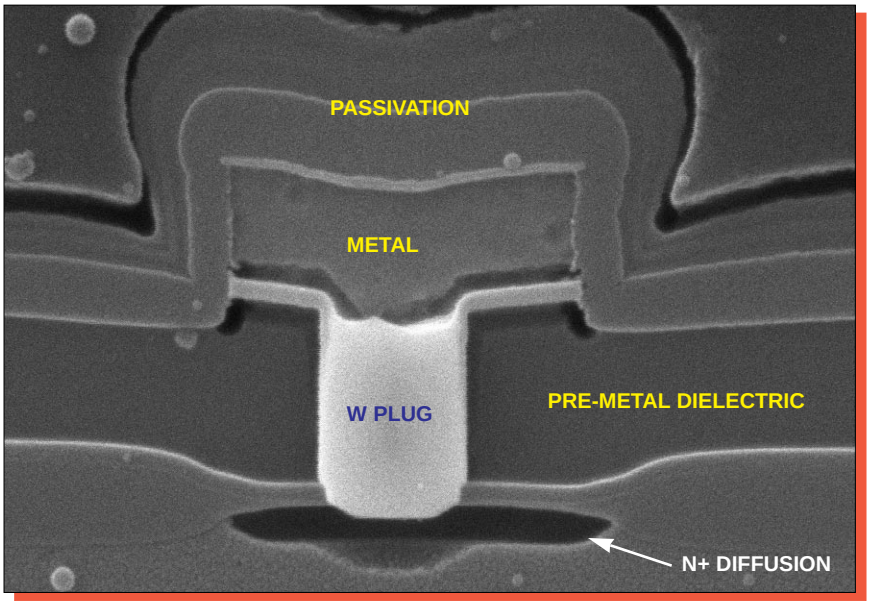



glass etch

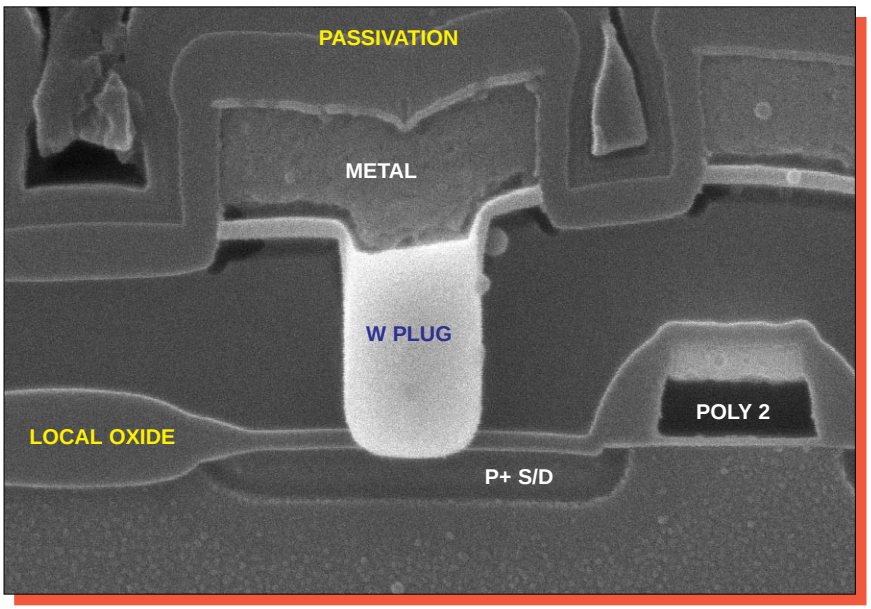
Figure 13. SEM views of barrier coverage and a metal contact. Mag. 26,000x.




metal-to-poly 2

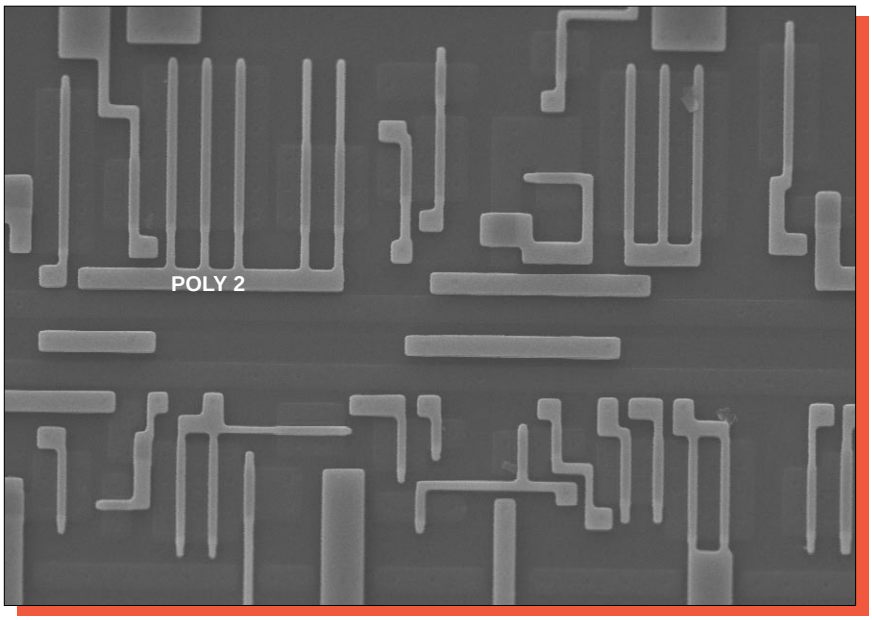



metal-to-N+

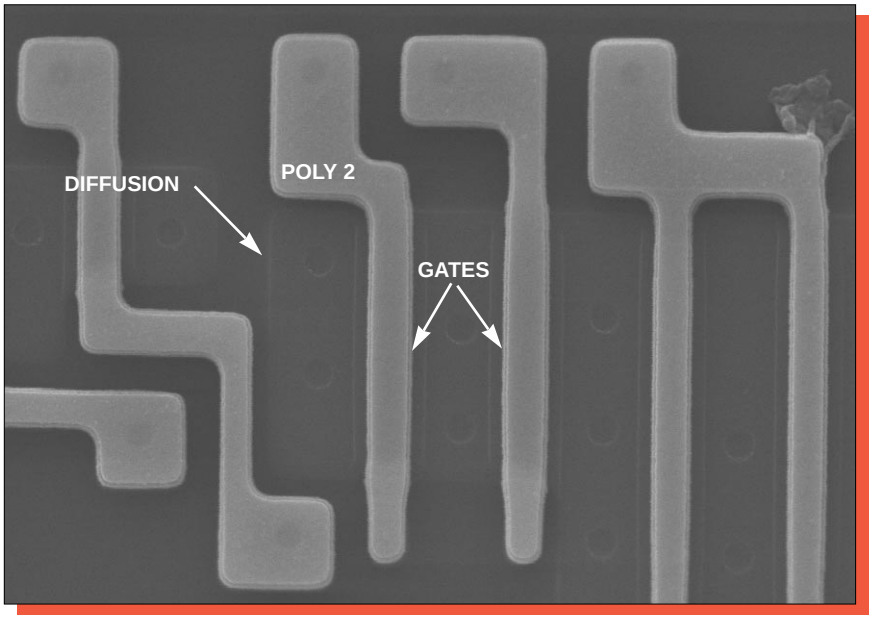



metal-to-P+

Figure 14. SEM section views of metal contacts. Mag. 26,000x.

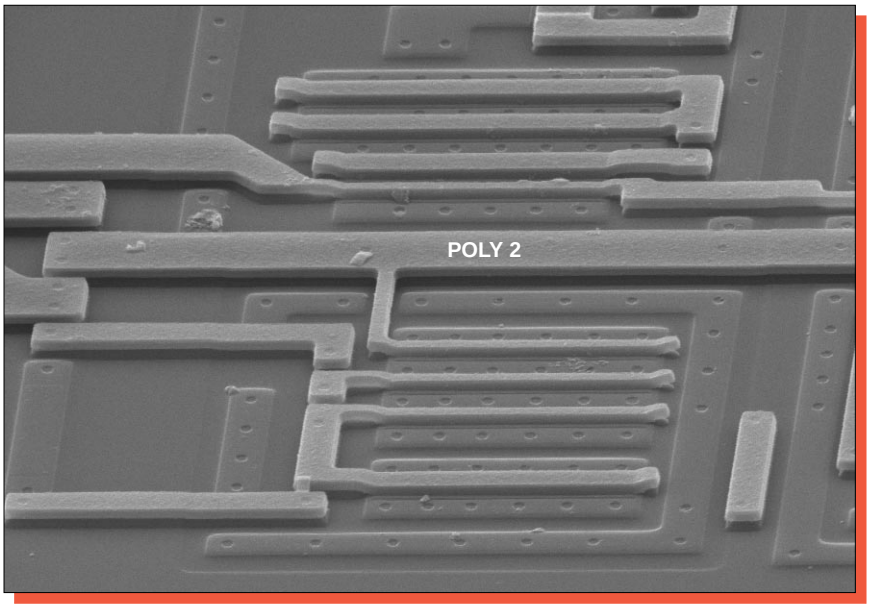



Mag. 1600x

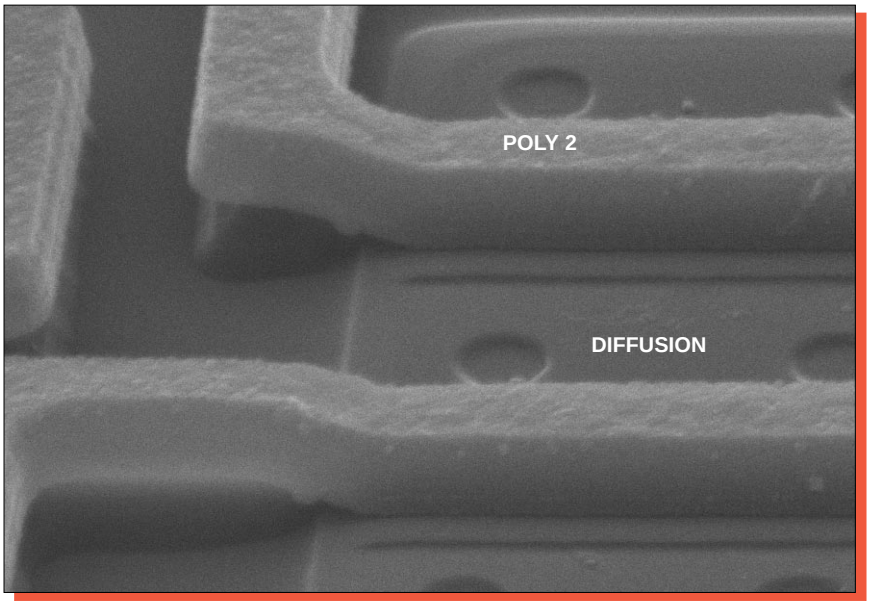



Mag. 6800x

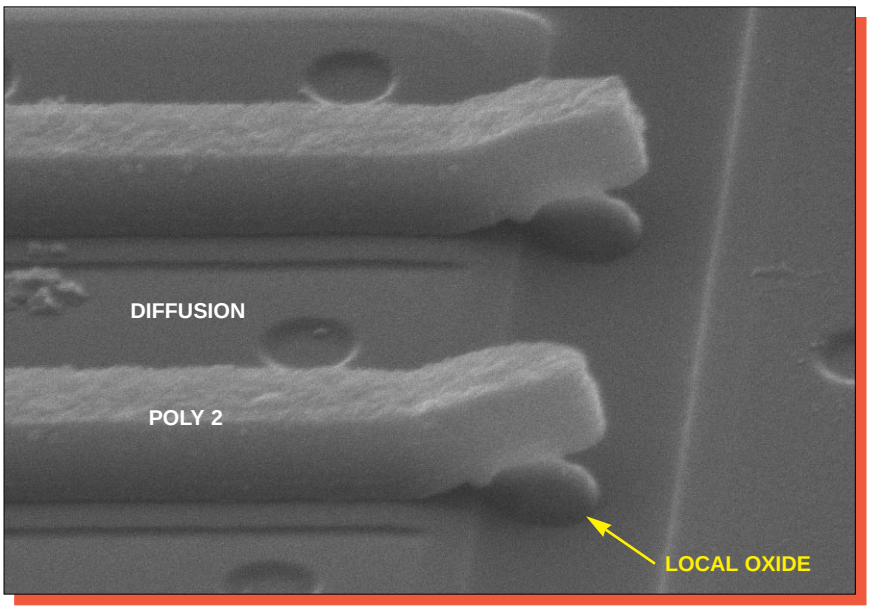
Figure 15. Topological SEM views of poly 2 patterning. 0°.




Mag. 2800x

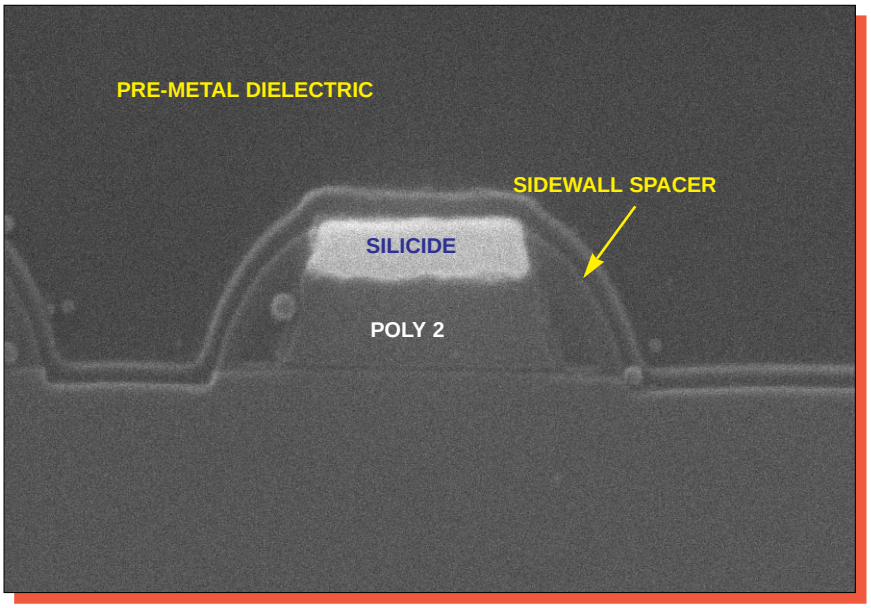



Mag. 22,000x

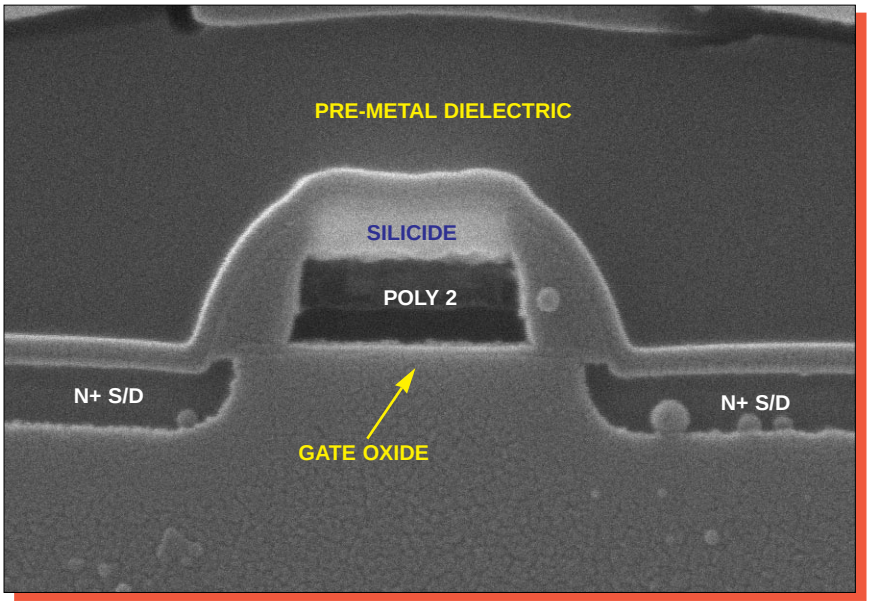



Mag. 22,000x

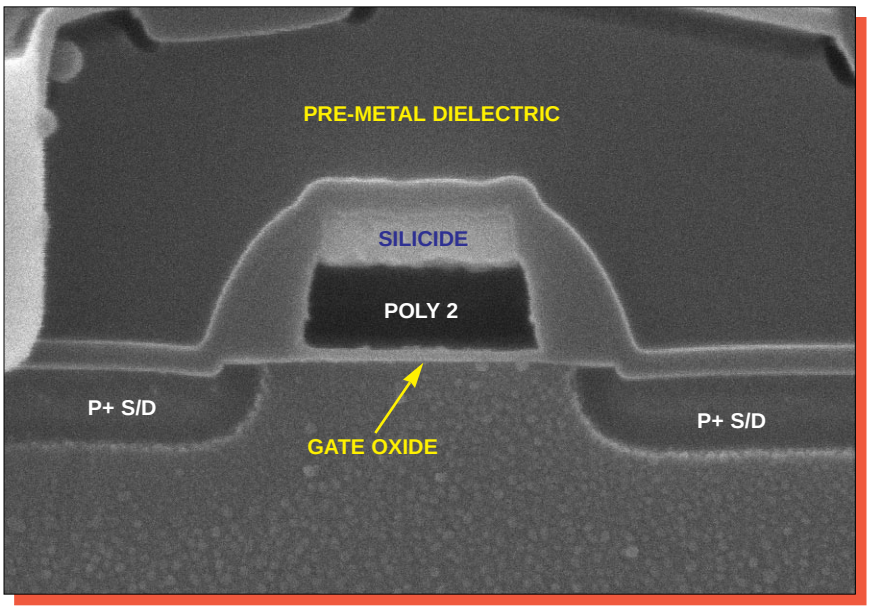
Figure 16. Perspective SEM views of poly coverage. 60°.




glass etch




N-channel




P-channel

Figure 17. SEM section views of typical transistors. Mag. 40,000x.

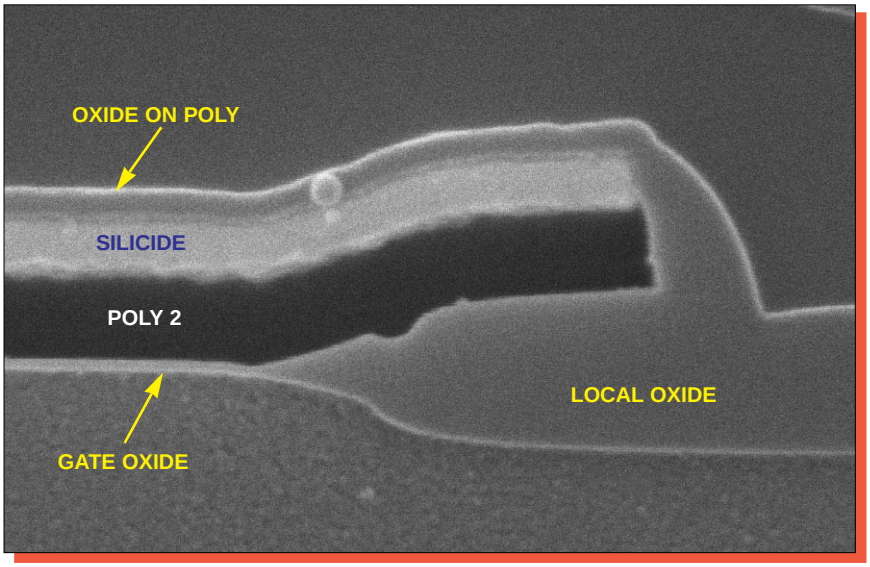
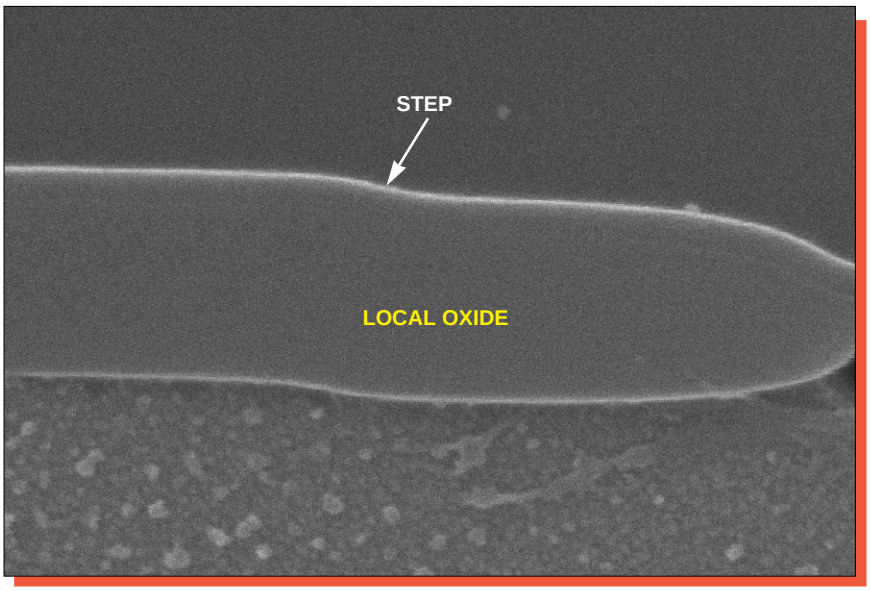
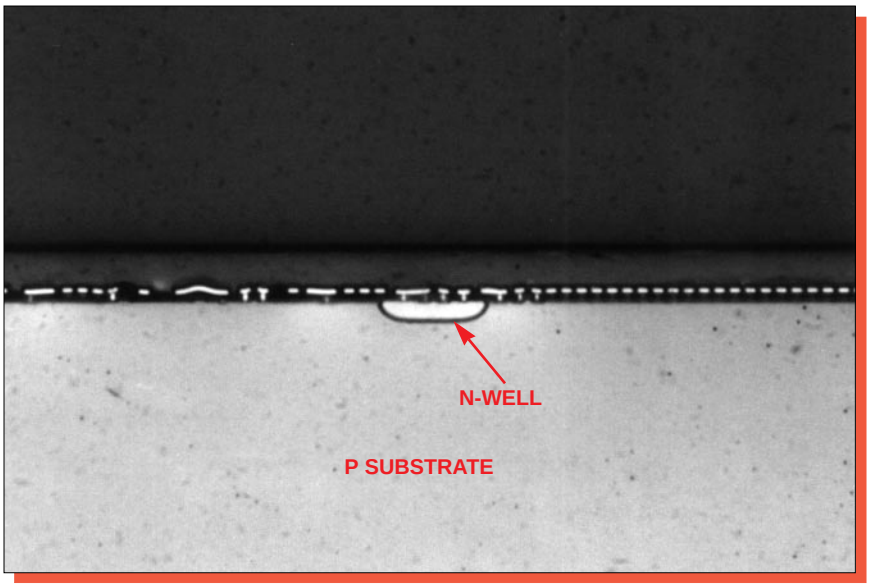



Figure 18. SEM view of a local oxide birdsbeak. Mag. 40,000x.

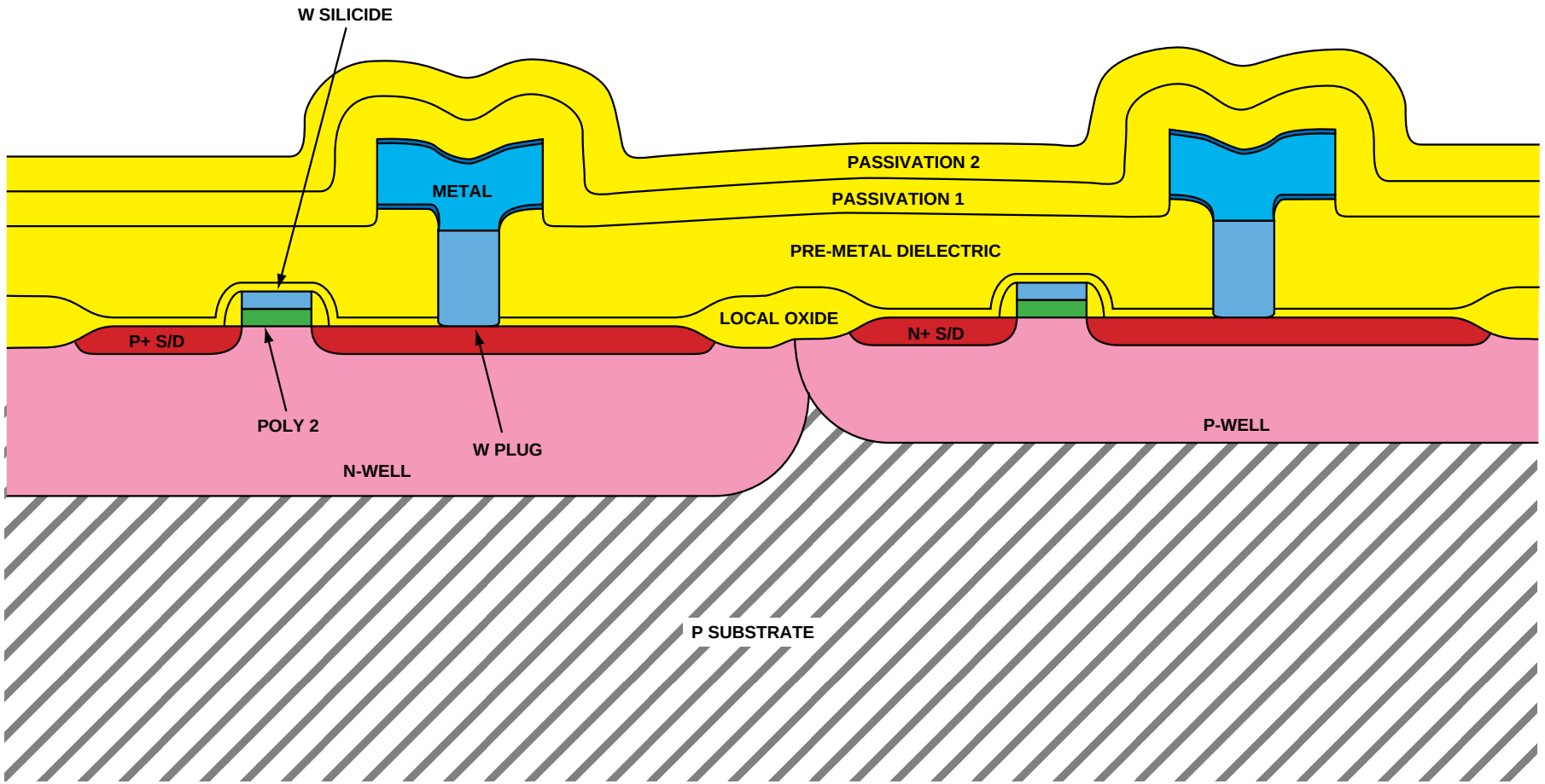



Mag. 52,000x




Mag. 800x

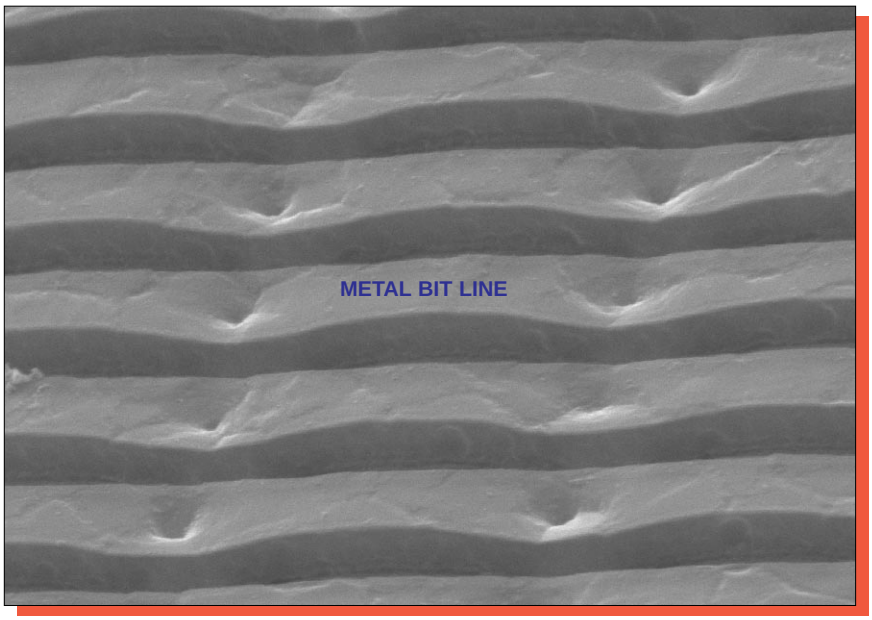
Figure 19. Section views illustrating the well structure.



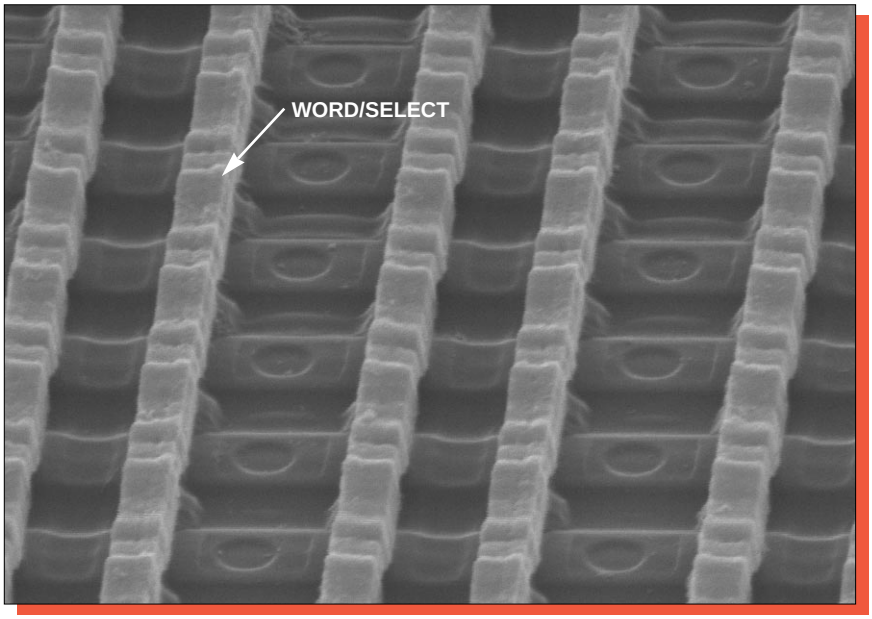

Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 20. Color cross section drawing illustrating device structure.

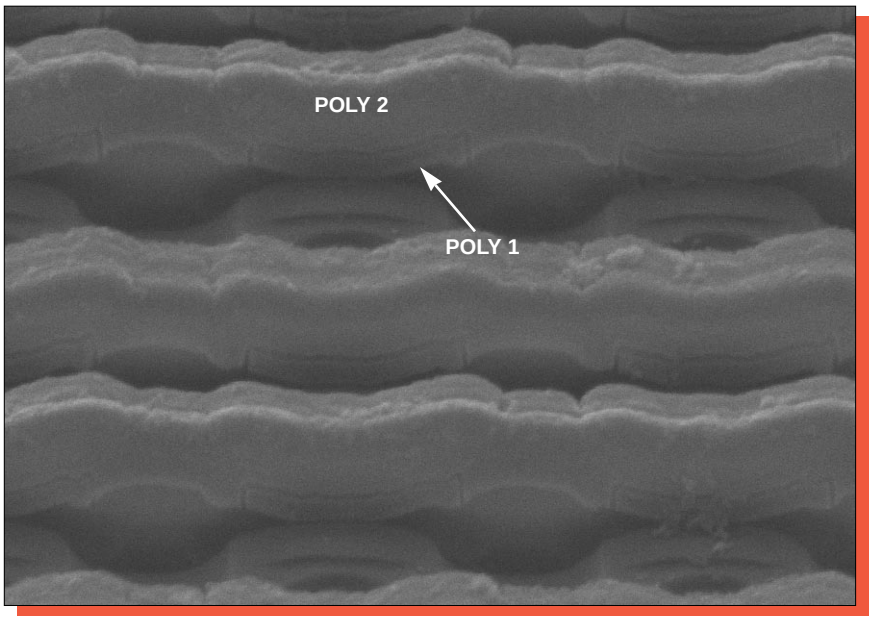



metal

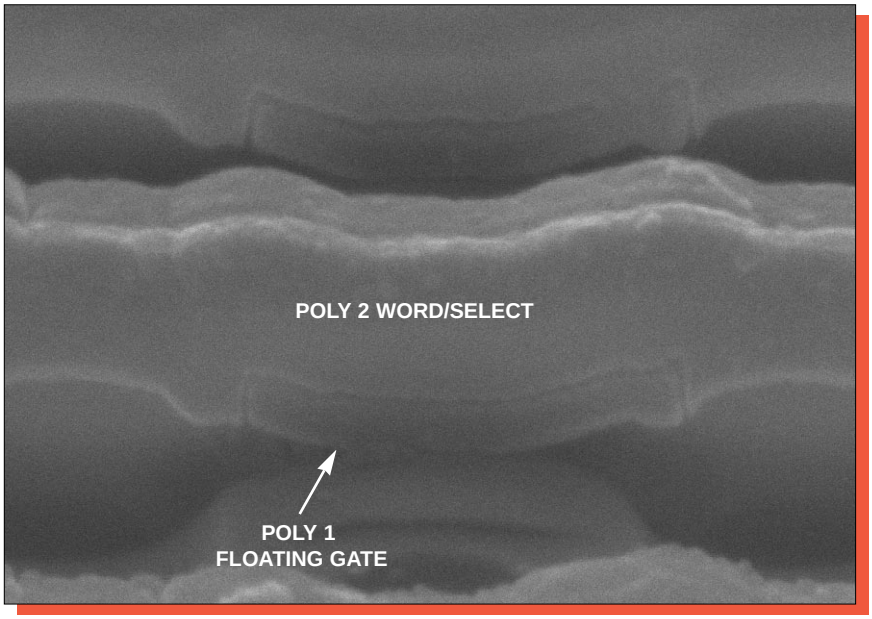



poly

Figure 21. Perspective SEM views of the EPROM cell array. Mag. 13,000x, 60°.

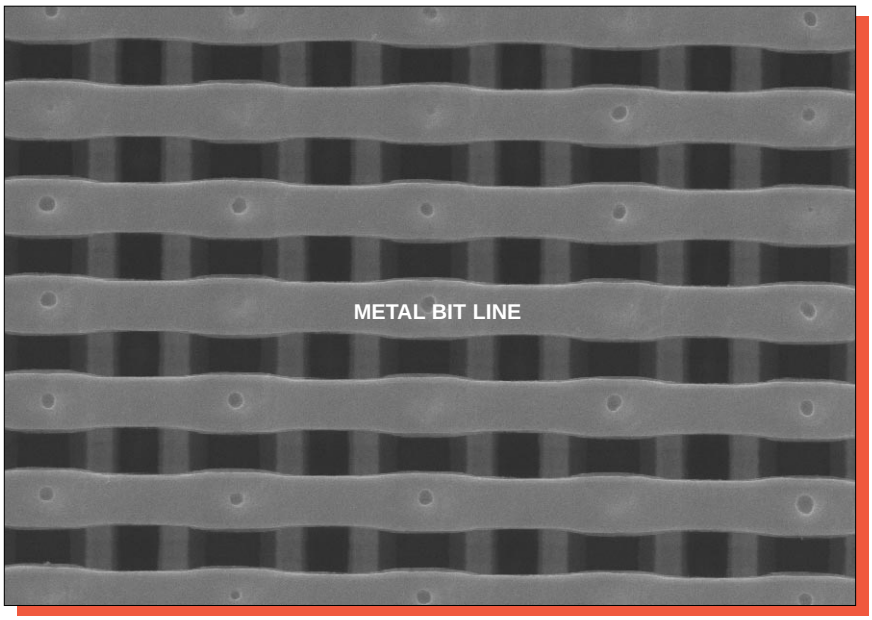



Mag. 26,000x

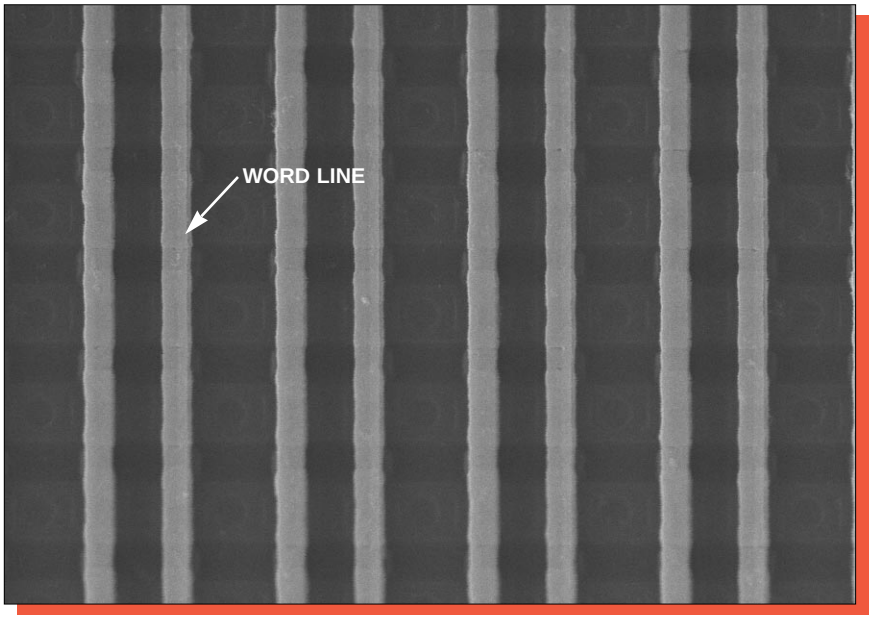



Mag. 52,000x

Figure 22. Perspective SEM views of the EPROM cell array. 60°.

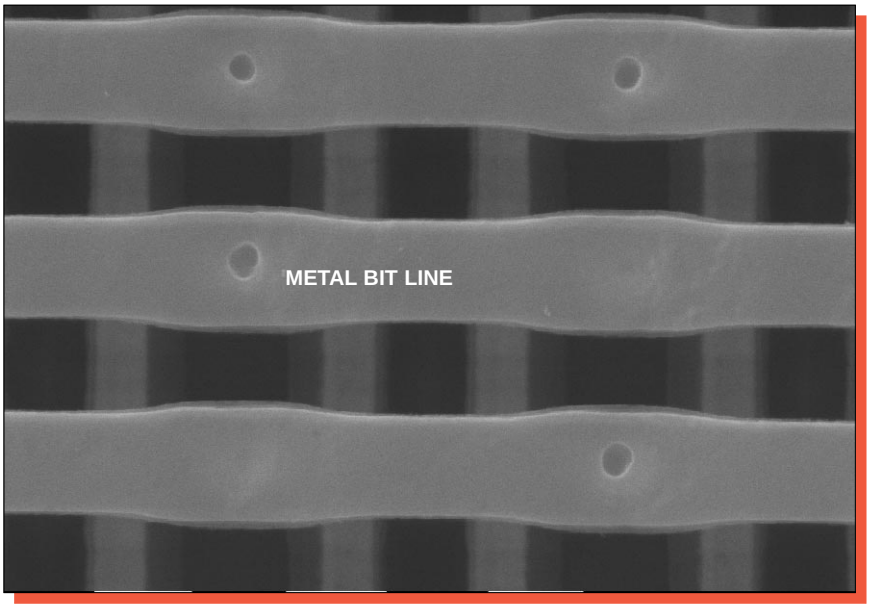



metal

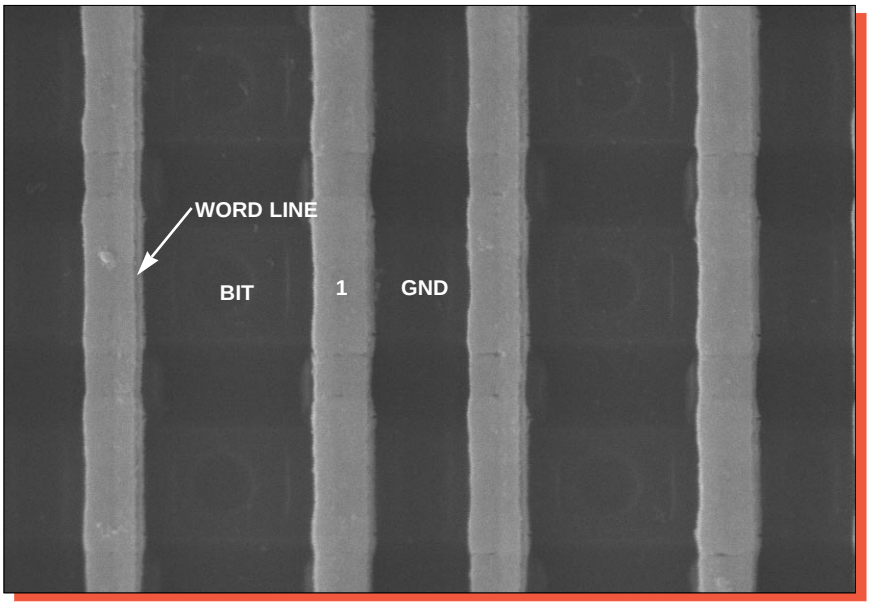



poly

Figure 23. Topological SEM views of the EPROM cell. Mag. 6500x, 0°.




metal




poly

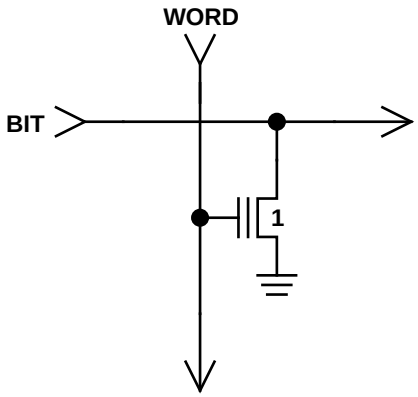
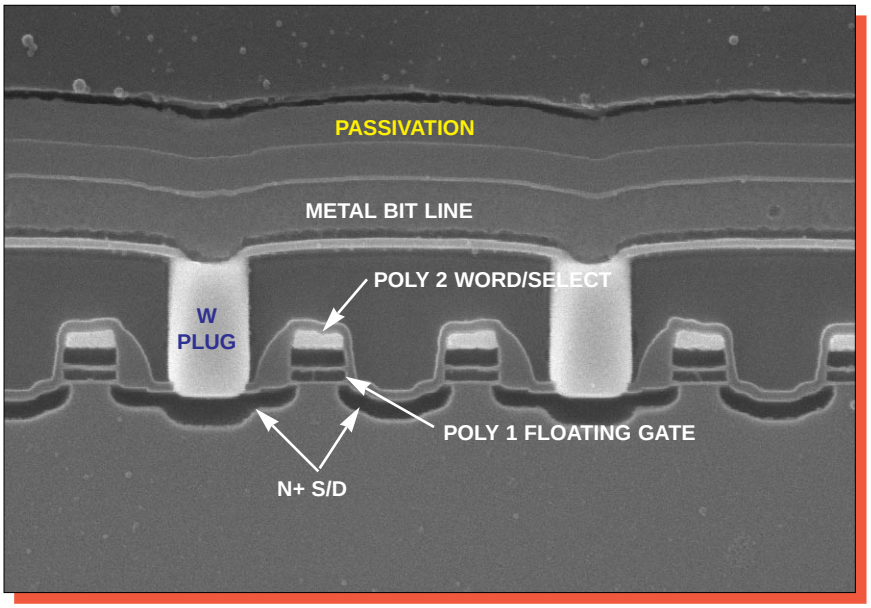
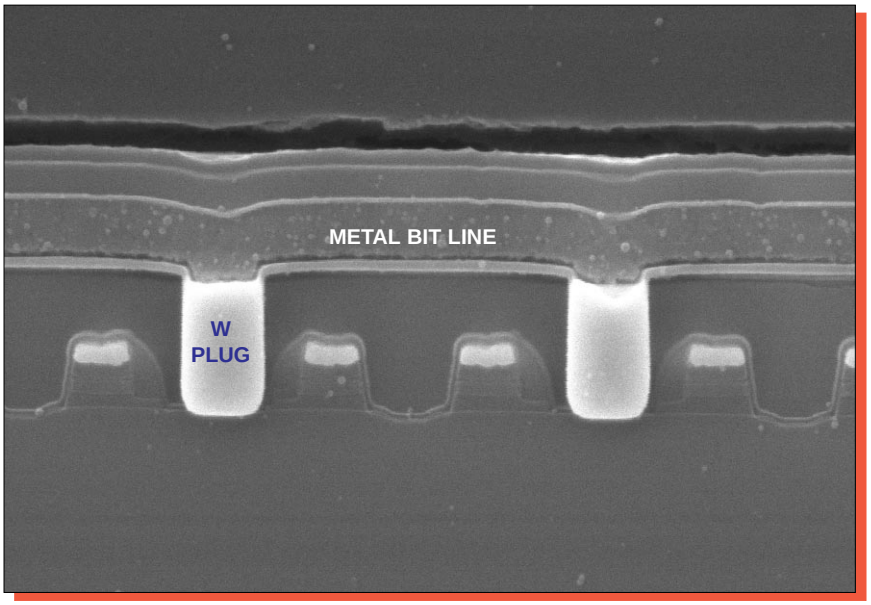


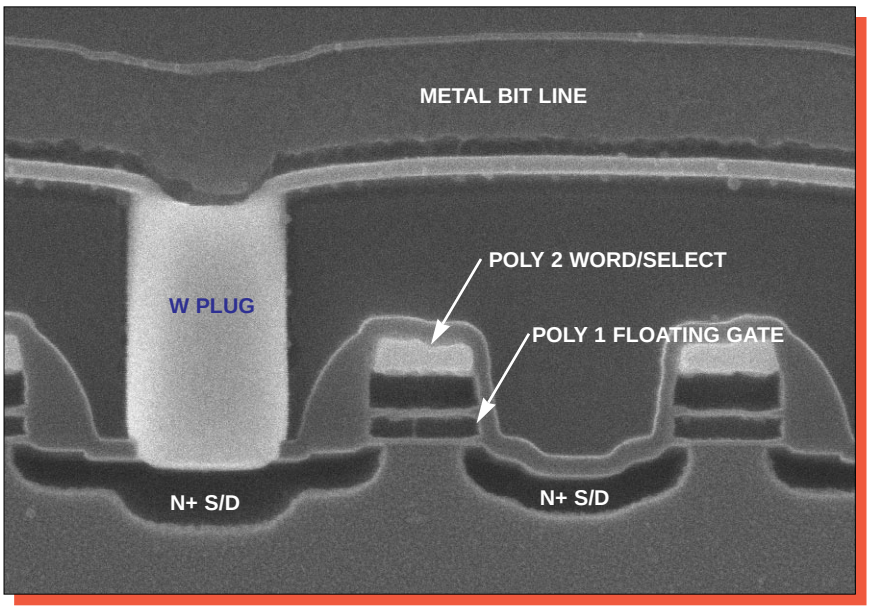

Figure 24. Topological views and schematic of the EPROM cell.
Mag. 13,000x, 0°.




Mag. 13,000x

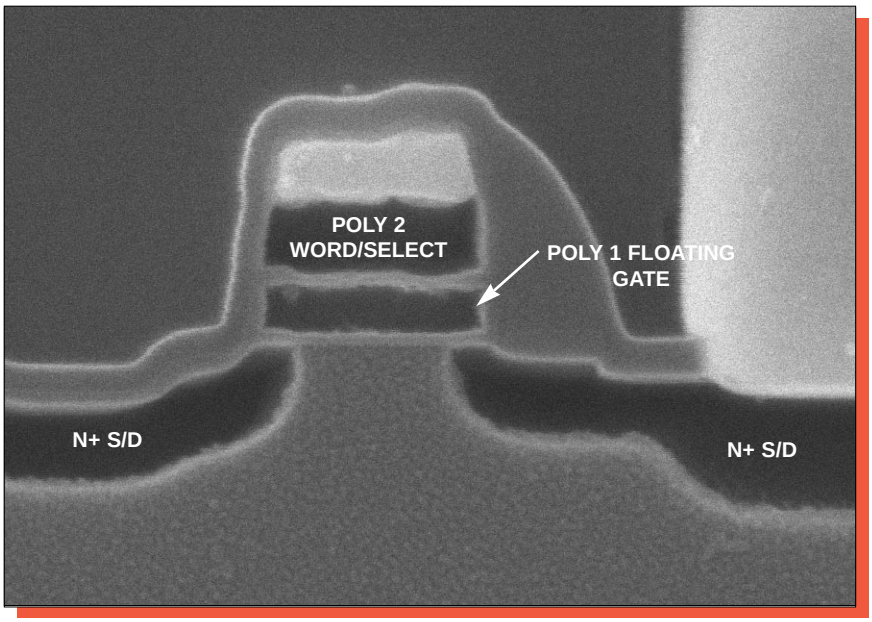


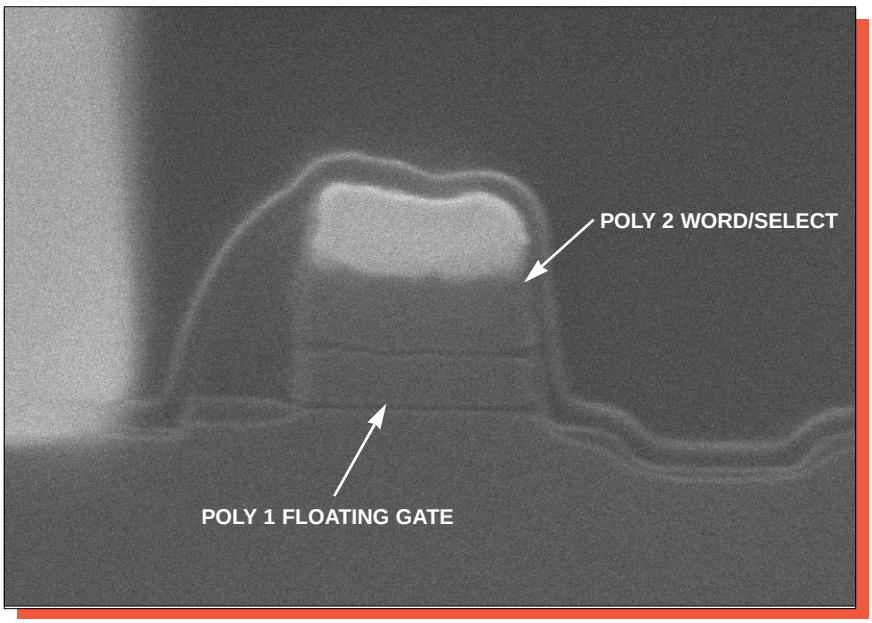

glass etch,
Mag. 13,000x




Mag. 26,000x

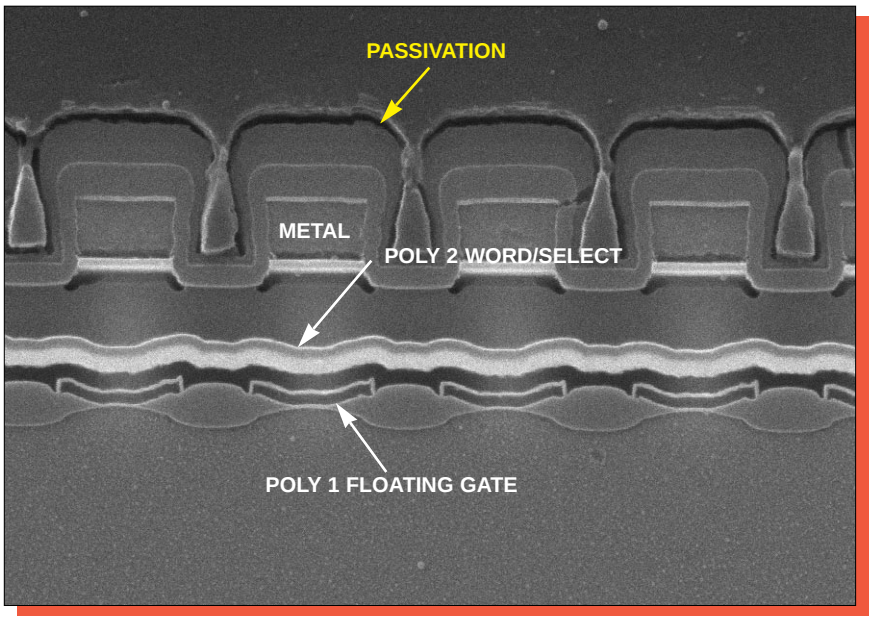
Figure 25. SEM section views of the EPROM cell array (parallel to bit lines).



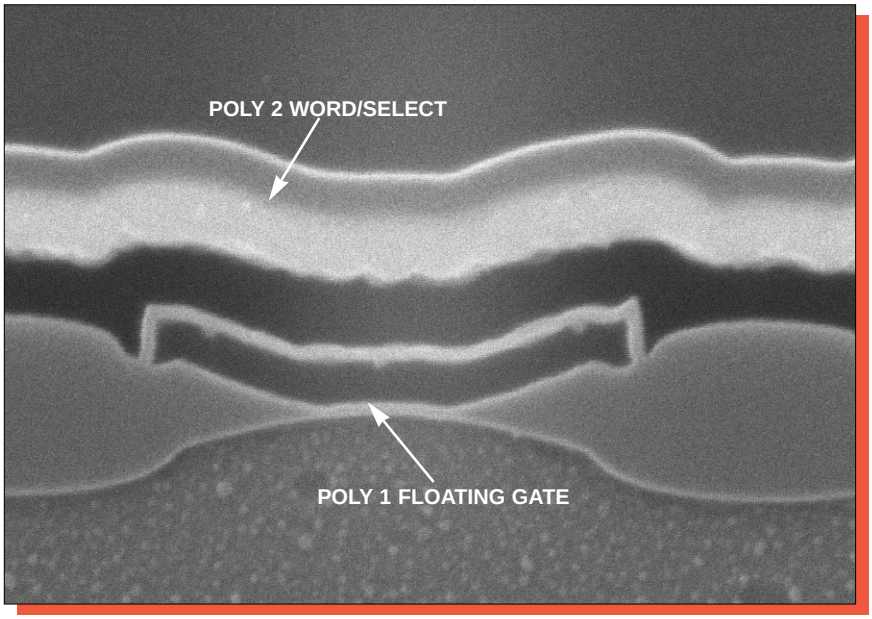




glass etch

Figure 26. SEM section detail views of the EPROM cell (parallel to bit line).
Mag. 52,000x.

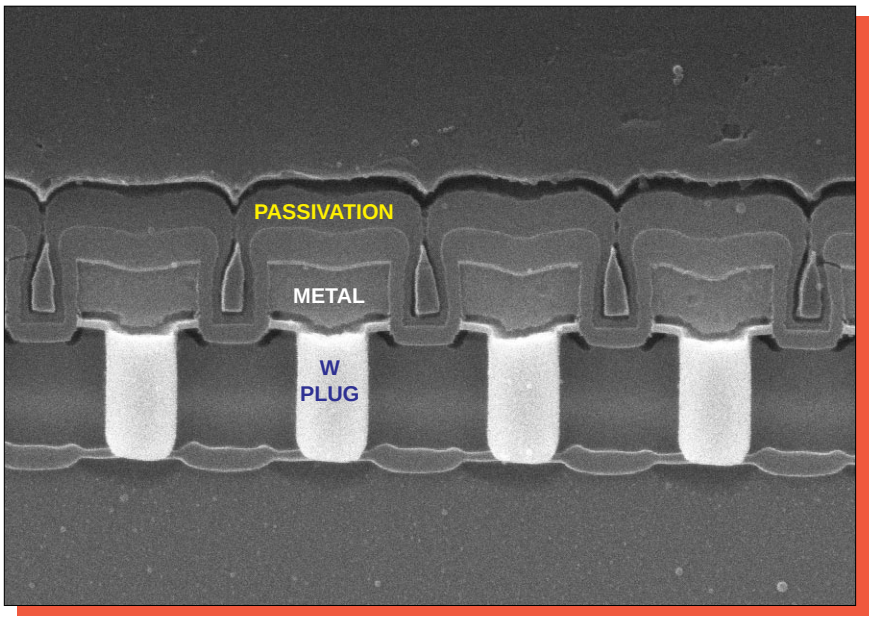



Mag. 13,000x

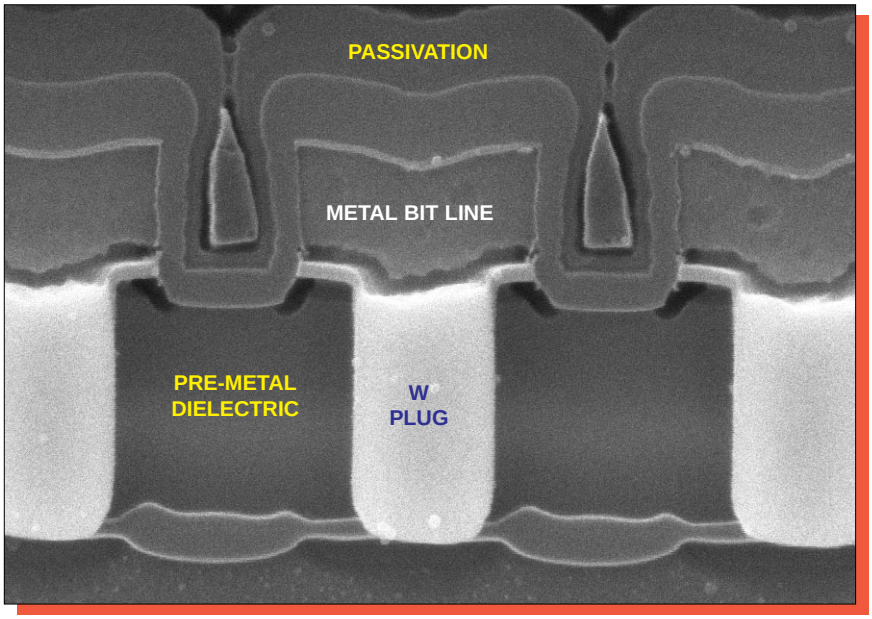



Mag. 52,000x

Figure 27. SEM section views of the EPROM cell array (parallel to word line).

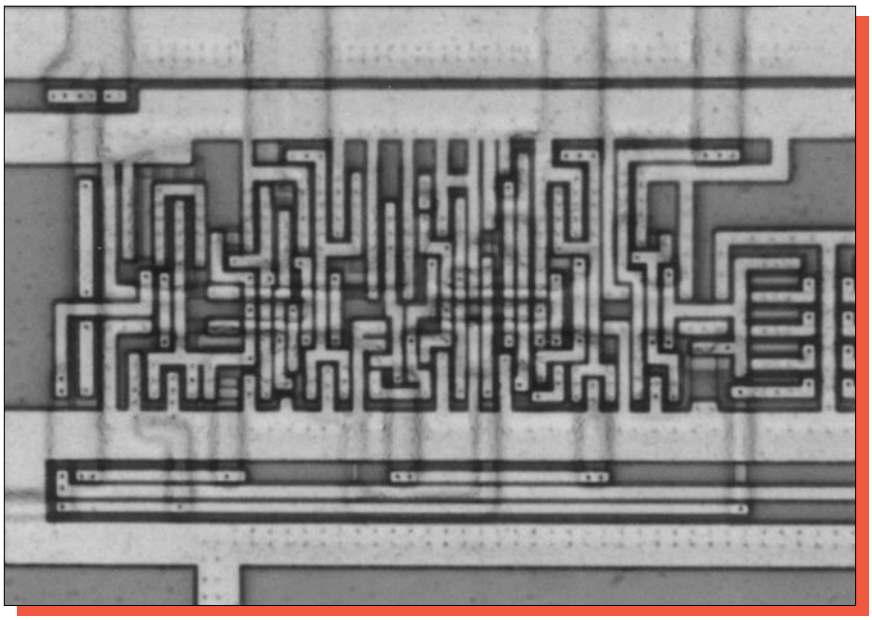



Mag. 13,000x

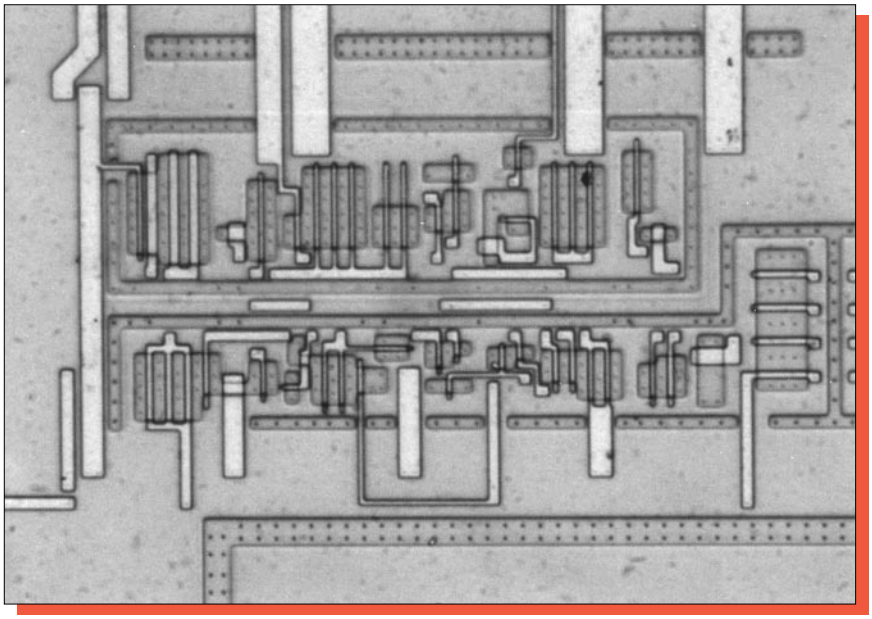



Mag. 26,000x

Figure 28. SEM section views of the EPROM cell array (parallel to word lines).

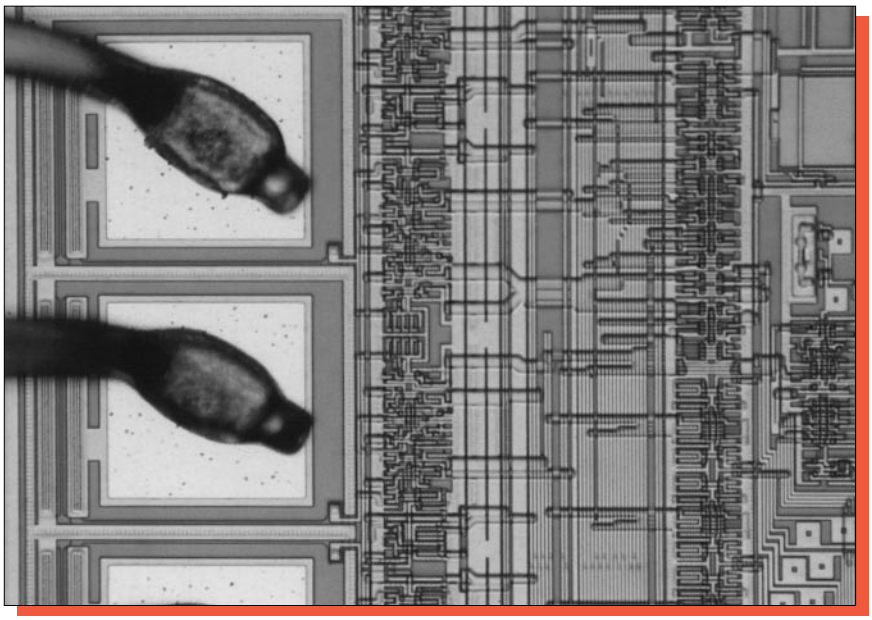


metal

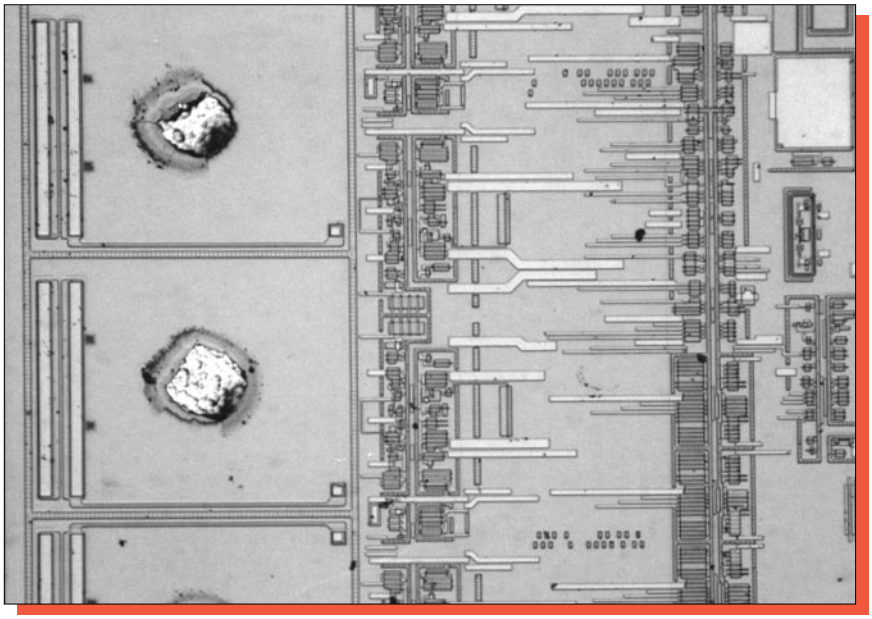


poly

Figure 29. Optical photographs of general circuitry. Mag. 800x.



metal



poly

Figure 30. Optical photographs of a I/O structure. Mag. 200x.