

## Construction Analysis

# AMD AM27C010 1M UVEPROM

Report Number: SCA 9612-517



**INTEGRATED CIRCUIT ENGINEERING**

15022 N. 75th Street  
Scottsdale, AZ 85260-2476  
Phone: 602-998-9780  
Fax: 602-948-1925  
e-mail: [ice@primenet.com](mailto:ice@primenet.com)  
Internet: <http://www.ice-corp.com/ice>

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## **INTRODUCTION**

This report describes a construction analysis of the AMD AM27C010 1M UVEPROM. Five devices packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs) with a quartz window were received for the analysis. Devices were date coded 9634.

## **MAJOR FINDINGS**

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Tungsten plugs used at all contacts.
- Sub-micron gate lengths (0.7 N-channel and 0.8 P-channel.)
- ONO dielectric used in array.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **TECHNOLOGY DESCRIPTION**

### **Assembly:**

- Devices were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs). A quartz window was present over the die.
- The package consisted of two ceramic halves held together by a glass frit. The die was mounted to the cavity floor using a silver-filled glass.
- Die separation was by sawing.
- Wirebonding was by the ultrasonic wedge bond method using 1.2 mil O.D. aluminum wire.
- All pins except pin 30 were connected. No multiple bonding wires were noted.

### **Die Process:**

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- No die coat was present.
- Passivation consisted of two layers of silicon-dioxide.
- Metallization consisted of a single layer of dry-etched metal. The metal layer consisted of aluminum with a titanium-nitride barrier. A thin titanium adhesion layer was used under the metal 1 barrier. Tungsten plugs were used at all contacts.
- Pre-metal dielectric consisted of a layer of borophosphosilicate glass (BPSG) over various densified oxides. The glass was reflowed prior to contact cuts only.

## **TECHNOLOGY DESCRIPTION (continued)**

- Two layers of poly were used on the die. Poly 2 (tungsten silicide) was used to form all gates on the die and the select/word line in the EPROM cell. Poly 1 (no silicide) was used exclusively in the cell to form the floating gates. Direct poly-to-diffusion (buried) contacts were not used. Interpoly dielectric consisted of nitride between two layers of oxide (ONO). Definition of poly was by a dry etch.
- Standard implanted N<sup>+</sup> and P<sup>+</sup> diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.
- Local oxide (LOCOS) isolation. A slight step was present at the edge of the well which indicates a twin-well process was used.
- Memory cell consisted of a standard stacked poly EPROM design. Metal was used to form the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. As mentioned, ONO was used as the interpoly dielectric.
- Redundancy fuses were not present.

## ANALYSIS RESULTS I

### Package and Assembly:

### Figures 1 - 4

**Questionable Items:**<sup>1</sup> None.

**Special Features:** None.

### **General Items:**

- Devices were packaged in 32-pin Ceramic Dual In-Line Packages (CERDIPs).
- Overall package quality: Good. No significant defects were noted in the external or internal portions of the package. No cracks or chips were noted in the packages. The package consisted of two ceramic halves held together by a glass frit. A quartz window was present over the die.
- Leadframe: The leadframe was apparently constructed of iron-nickel. No voids or cracks were in the glass frit seal.
- Die dicing: Die separation was by sawing of normal quality. No large cracks or chips were present.
- Die attach: A silver-filled glass was used to attach the die to the header. No significant voids were noted.
- Wirebonding was by the ultrasonic wedge bond method using 1.2 mil O.D. aluminum wire. The clearance of the wires was normal. Bond pull strengths were normal (see page 10). No problems were noted.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS II**

### **Die Process:**

**Figures 5 - 31**

**Questionable Items:**<sup>1</sup> None.

### **Special Features:**

- Tungsten plugs used at all contacts.
- Sub-micron gate lengths (0.7 micron N-channel and 0.8 P-channel.)
- ONO dielectric used in array.

### **General Items:**

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: Two layers of silicon-dioxide. The top layer was very thin. Overlay integrity test indicated defect-free passivation. Edge seal was good.
- Metallization: A single layer of metal consisting of aluminum with a titanium-nitride barrier. A thin titanium adhesion layer was noted under the barrier. Tungsten plugs were used at all contacts. No problems were noted.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS II (continued)**

- Metal patterning: The metal layer was patterned by a dry etch of normal quality. Contacts were completely surrounded by metal.
- Metal defects: No voiding, notching, or neckdown was noted in the metal layer. Silicon nodules were noted following the removal of the metal. Some nodules occupied up to 50 percent of metal line widths. Silicon nodules which occupy >50 percent of the line widths can cause an increase in the aluminum's susceptibility to electromigration.
- Metal step coverage: Aluminum thinning did not exceed 60 percent due to the presence of the tungsten plugs. MIL-STD allows up to 70 percent metal thinning for contacts of this size.
- Pre-metal dielectric: A layer of borophosphosilicate glass ( BPSG) over various densified oxides was used under the metal. Reflow was performed prior to contact cuts only. No problems were found.
- Contact defects: Contact cuts were defined by a dry-etch process. No over-etching of the contacts was noted.
- Polysilicon: Two layers of poly were used on the die. Poly 2 (tungsten silicide) was used to form all gates on the die and the select/word line in the EPROM cell. Poly 1 (no silicide) was used exclusively in the cell to form the floating gates. Direct poly-to-diffusion (buried) contacts were not used. Interpoly dielectric consisted of a layer of nitride between two layers of oxide (ONO). Definition was by a dry etch of normal quality. No poly stringers or spurs were present.
- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place.

## **ANALYSIS RESULTS II (continued)**

- Isolation: Local oxide (LOCOS) isolation was used. The slight step present at the well boundary indicates a twin-well process was employed.
- EPROM array: Memory cell consisted of a standard stacked poly EPROM design. Metal was used to form the bit lines. Poly 2 was used to form the word/select lines, and poly 1 was used exclusively to form the floating gates. As mentioned, ONO was used as the interpoly dielectric. Cell pitch was 2.3 x 2.4 microns.
- Redundancy fuses were not present on the die.

## **PROCEDURE**

The devices were subjected to the following analysis procedures:

External inspection  
X-ray  
Delid  
Internal optical inspection  
SEM of passivation  
Passivation integrity test  
Wirepull test  
Passivation removal  
SEM inspection of metal  
Metal removal and inspect barrier  
Delayer to silicon and inspect poly/die surface  
Die sectioning (90° for SEM)\*  
Die material analysis (EDX and WDX)  
Measure horizontal dimensions  
Measure vertical dimensions

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Good

**DETAIL OF EVALUATION**

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver-filled glass
Dicing method	Sawn
Wirebond method	Ultrasonic wedge bonds using 1.2 mil aluminum wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Contact coverage	N
Contact registration	G

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## **PACKAGE MARKINGS (TOP)**

MALAYSIA (LOGO)  
AM27C010  
-200DC  
9634APA  
12.75V PGM

## **WIREBOND STRENGTH**

Wire material: 1.2 mil O.D. aluminum  
Die pad material: aluminum

<b><u>Sample #</u></b>	<b>1</b>
# of wires pulled:	21
Bond lifts:	0
Force to break - high:	5.5g
- low	4g
- avg.	4.7g
- std. dev.:	0.45

## **DIE MATERIAL ANALYSIS (EDX and WDX)**

Overlay passivation: Two layers of silicon dioxide with 4.86 percent phosphorus.

Metallization: Aluminum (Al) with a titanium-nitride (TiN) barrier and thin titanium (Ti) adhesion layer.

Poly 2: Tungsten (W) silicide.

Pre-metal dielectric: A layer of borophosphosilicate glass (BPSG) containing 3.81 wt. percent phosphorus and 2.3 wt. percent boron over various densified oxides.



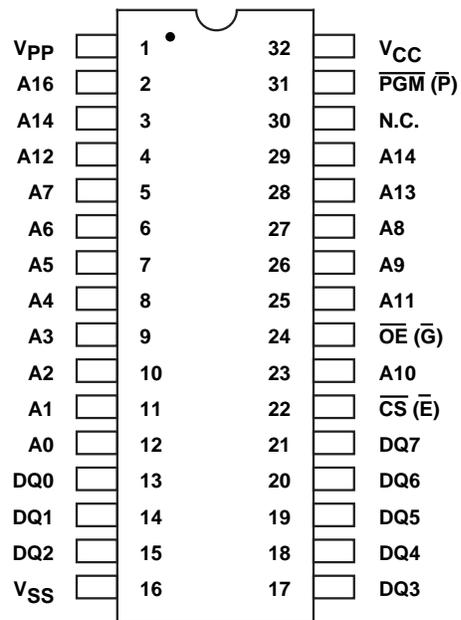
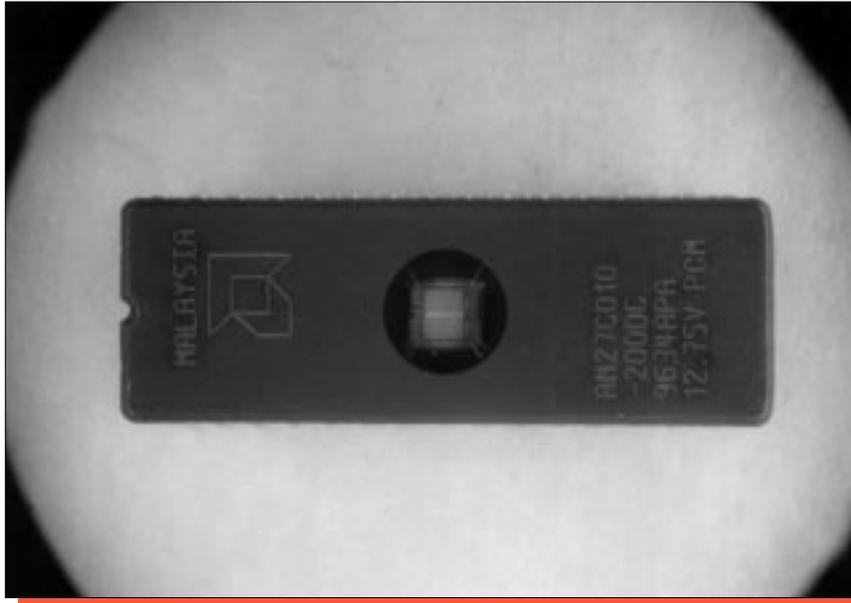
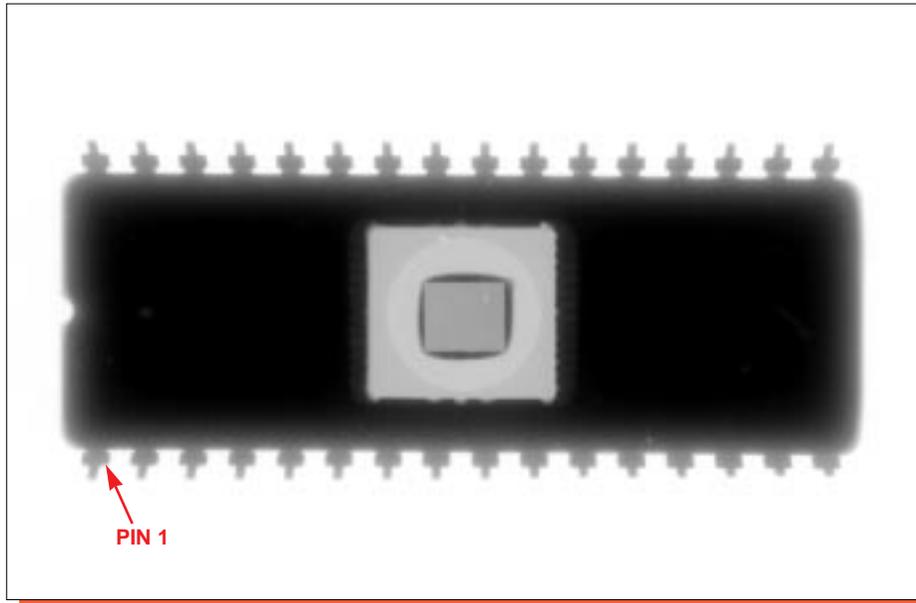
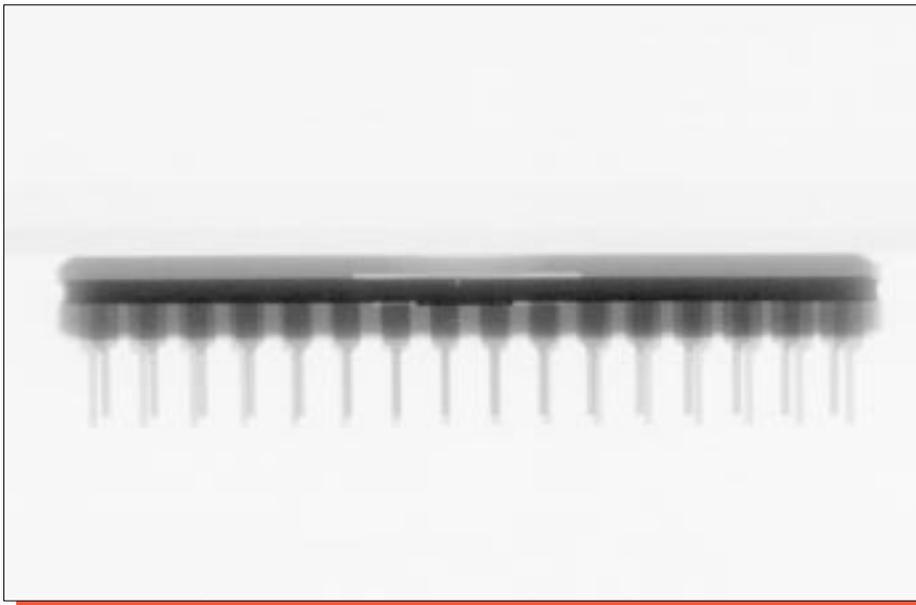


Figure 1. Package photograph and pinout of the AMD AM27C010. Mag. 2.1x.

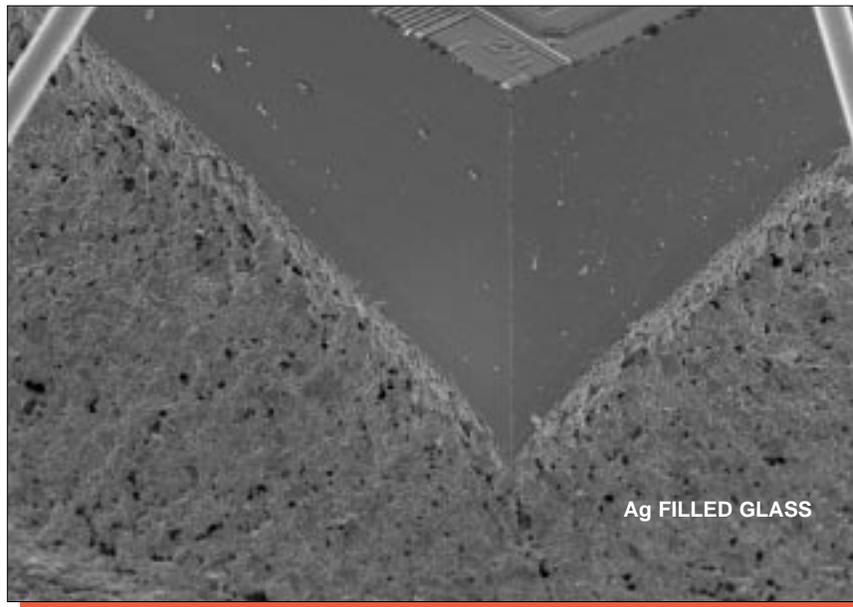


top

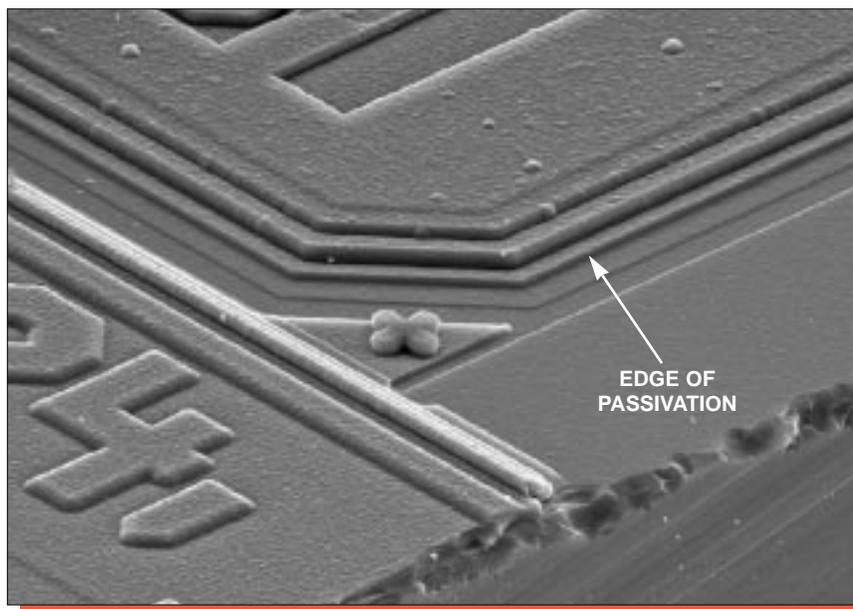


side

Figure 2. X-ray views of the package. Mag. 2.5x.



Mag. 150x



Mag. 1200x

Figure 3. SEM views of dicing and edge seal. 60°.

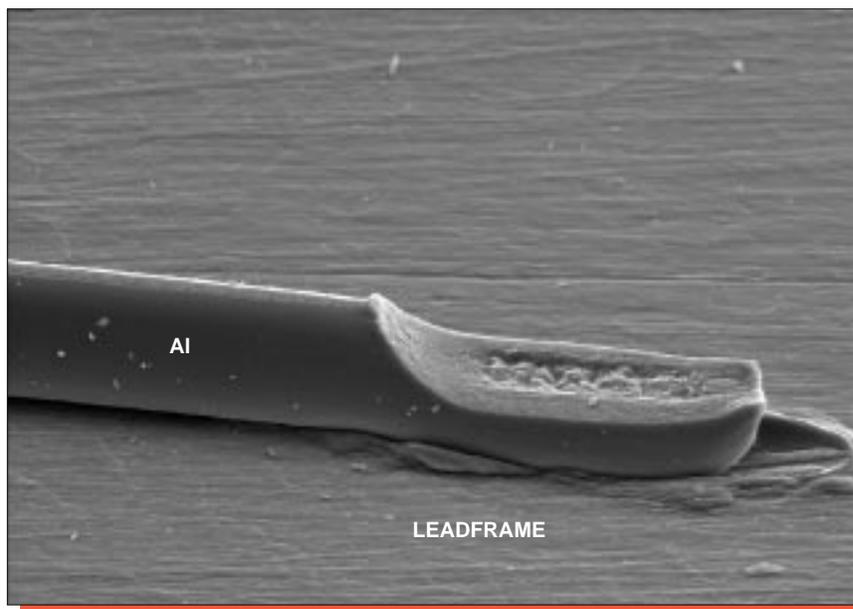
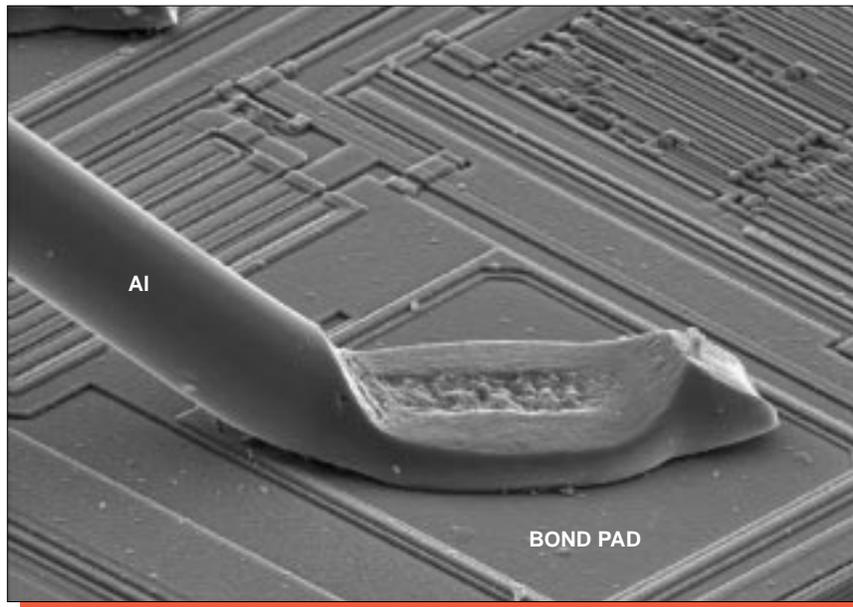


Figure 4. SEM views of typical wirebonding. 60°.

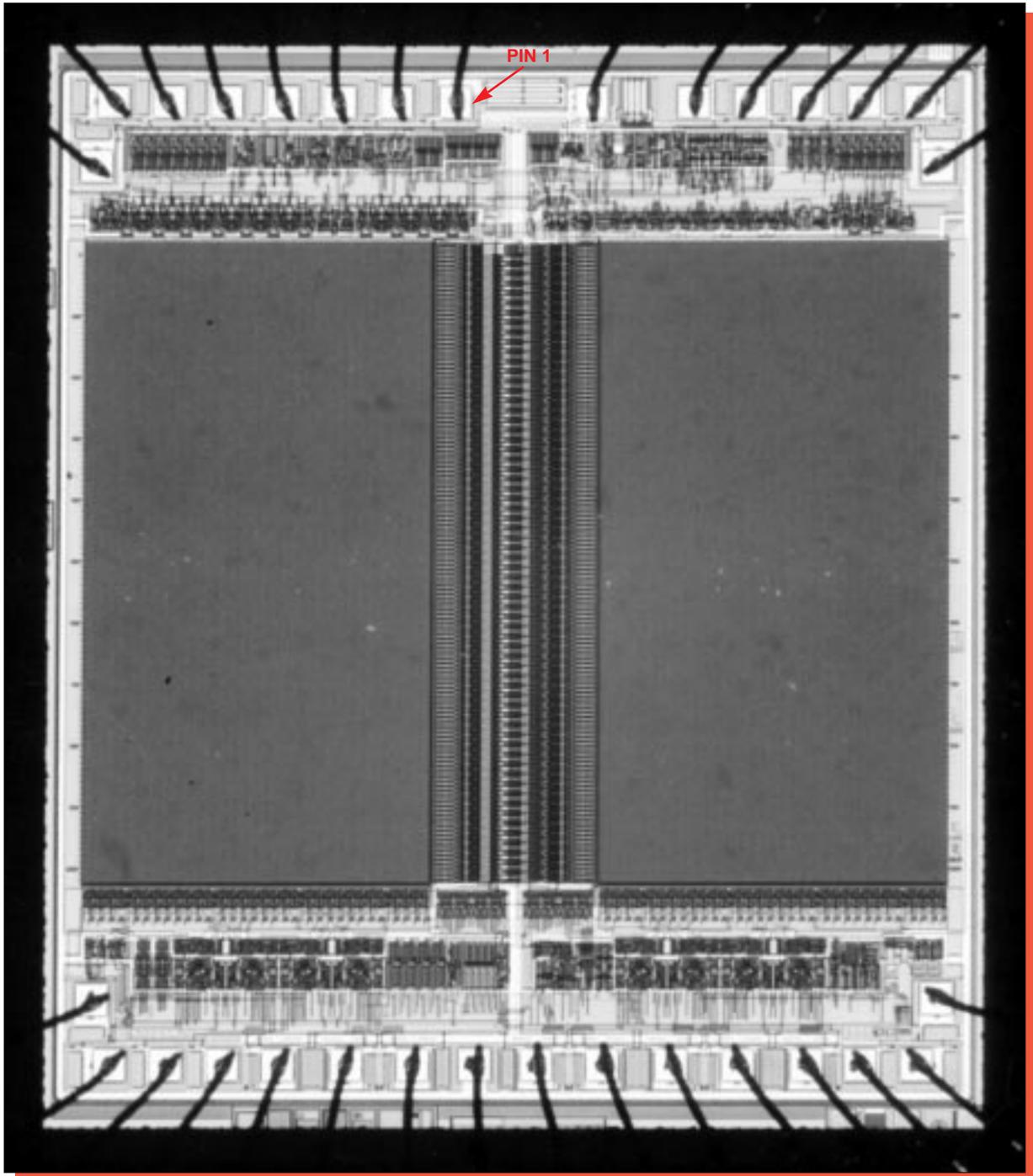


Figure 5. Whole die photograph of the AMD AM27C010. Mag. 40x.

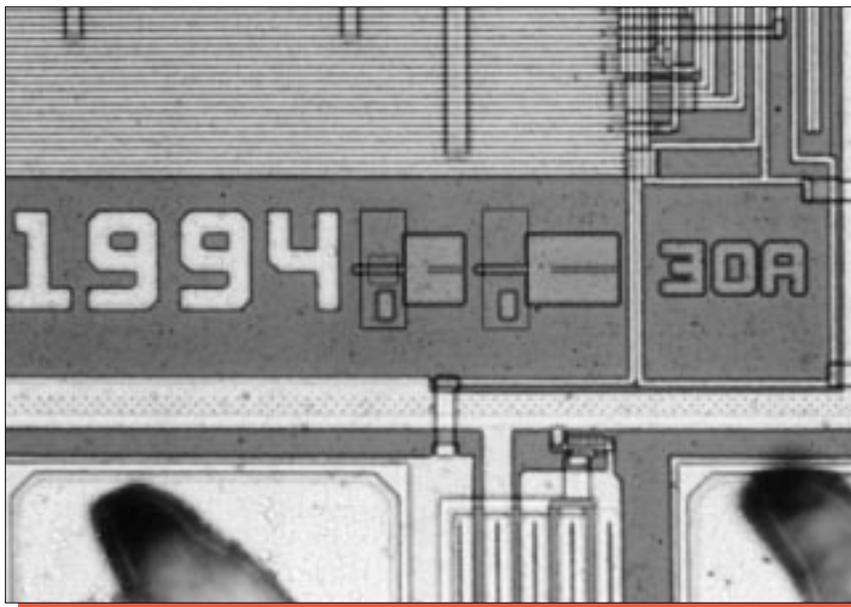
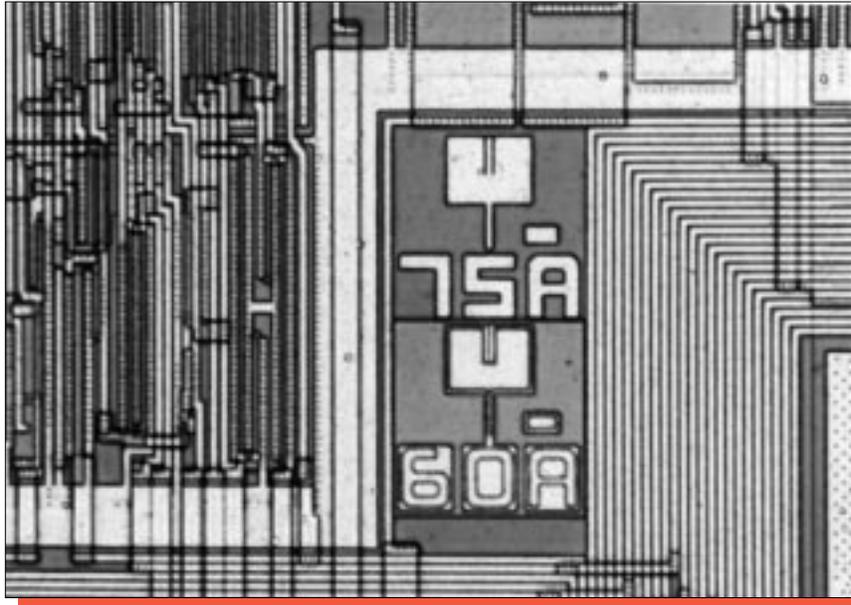
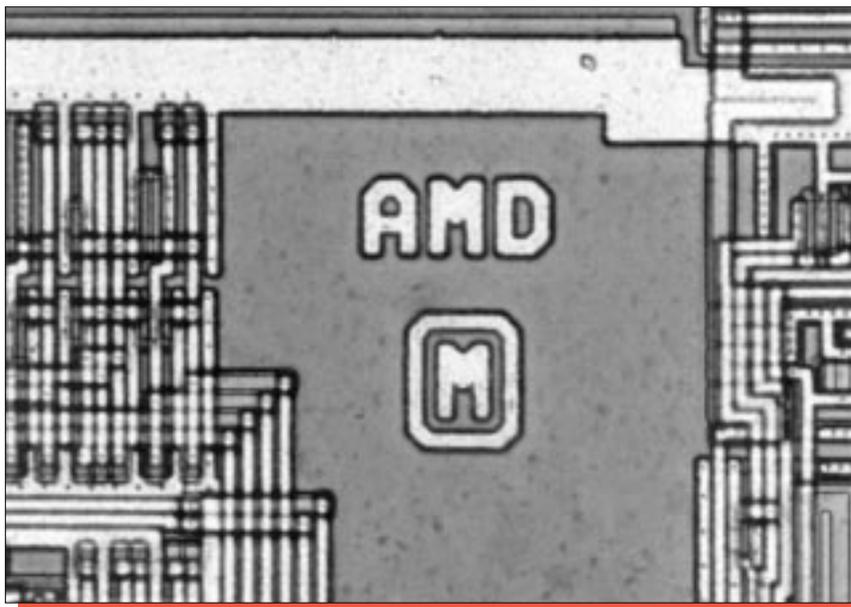


Figure 6. Optical views of markings on the die surface. Mag. 400x.

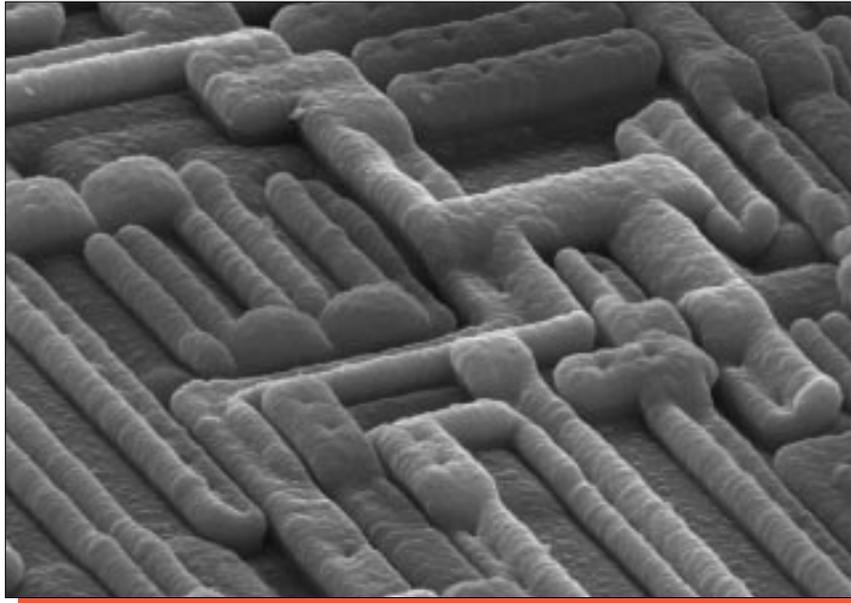


Mag. 500x

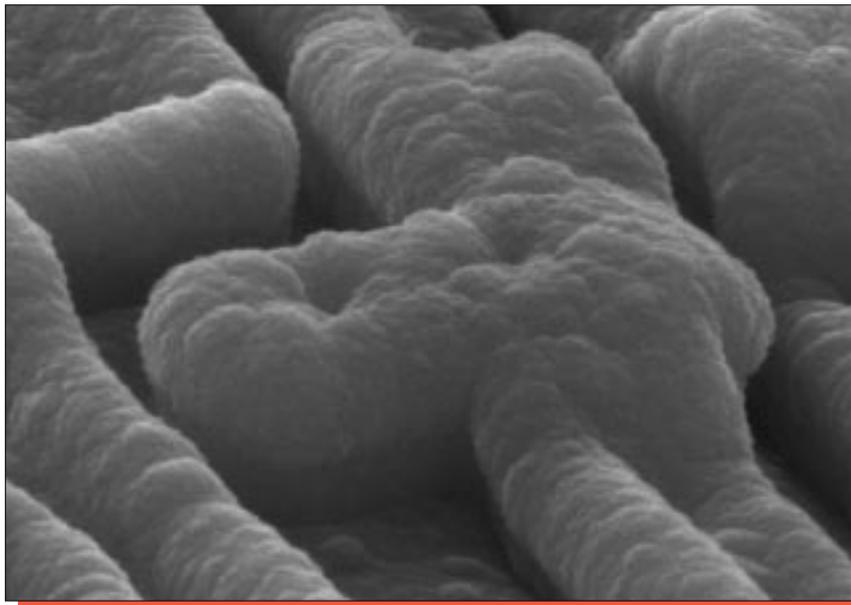


Mag. 800x

Figure 7. Optical views of markings on the die surface.

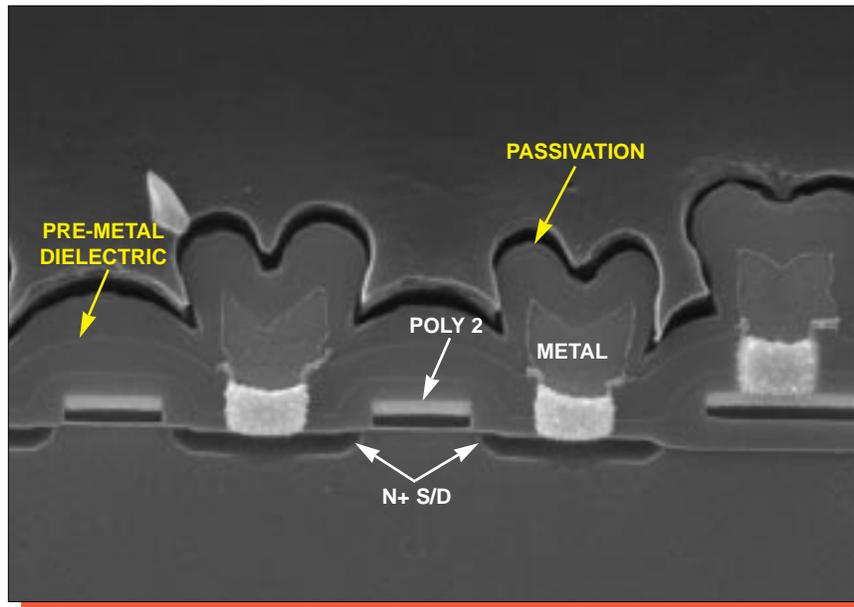


Mag. 4000x

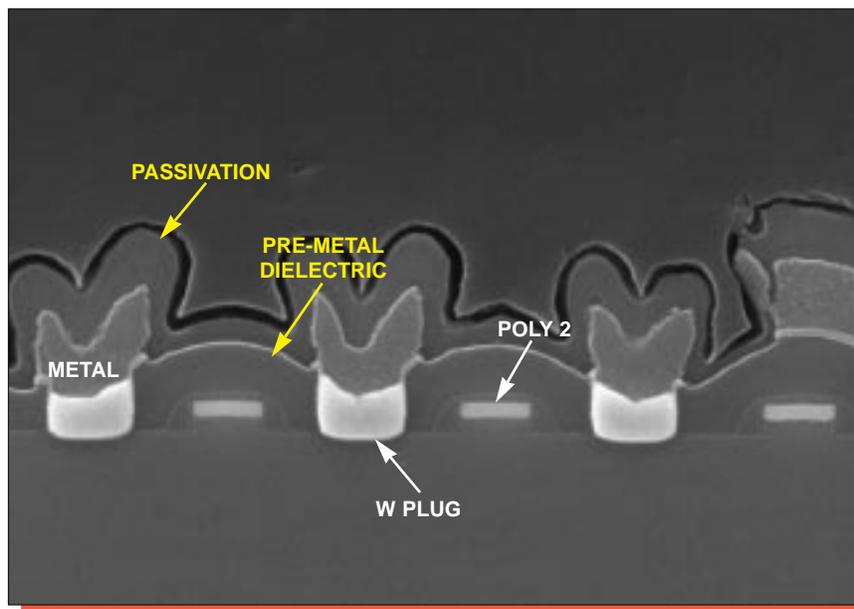


Mag. 15,000x

Figure 8. Perspective SEM views of overlay passivation coverage. 60°.

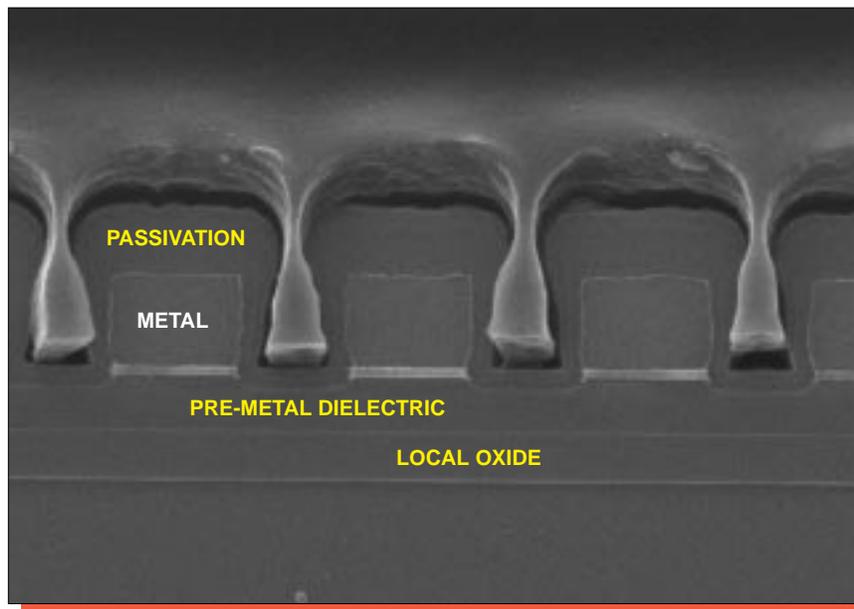


silicon-etch

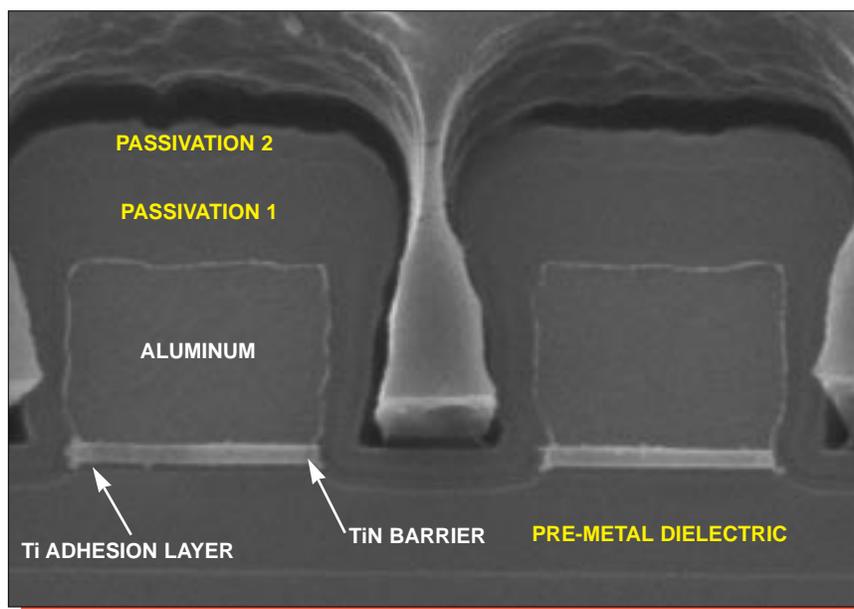


glass etch

Figure 9. SEM section views of general device structure. Mag. 10,000x.

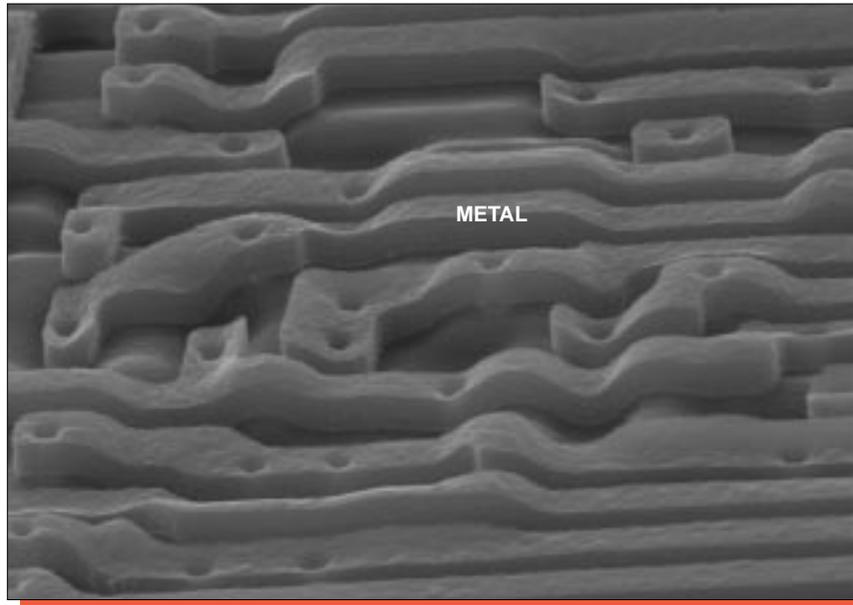


Mag. 13,000x

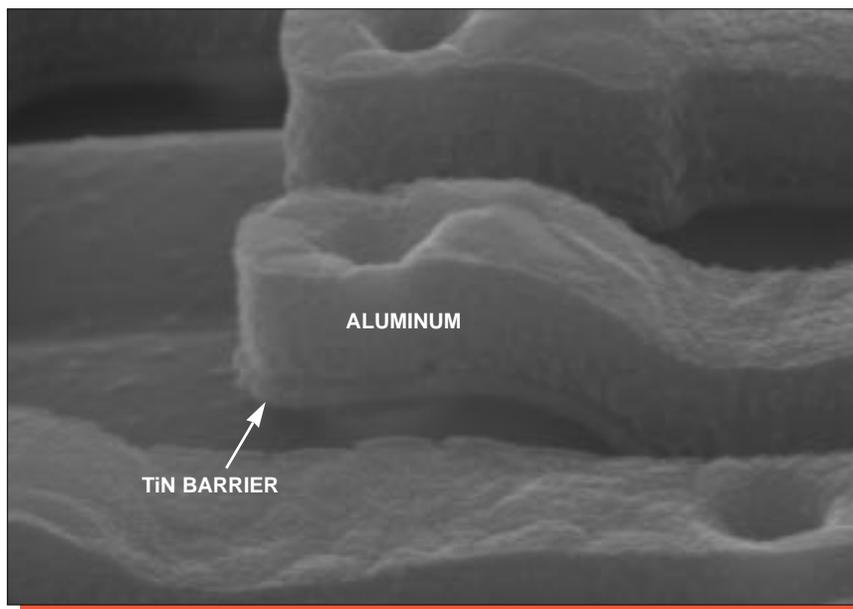


Mag. 26,000x

Figure 10. SEM section views of metal line profiles.

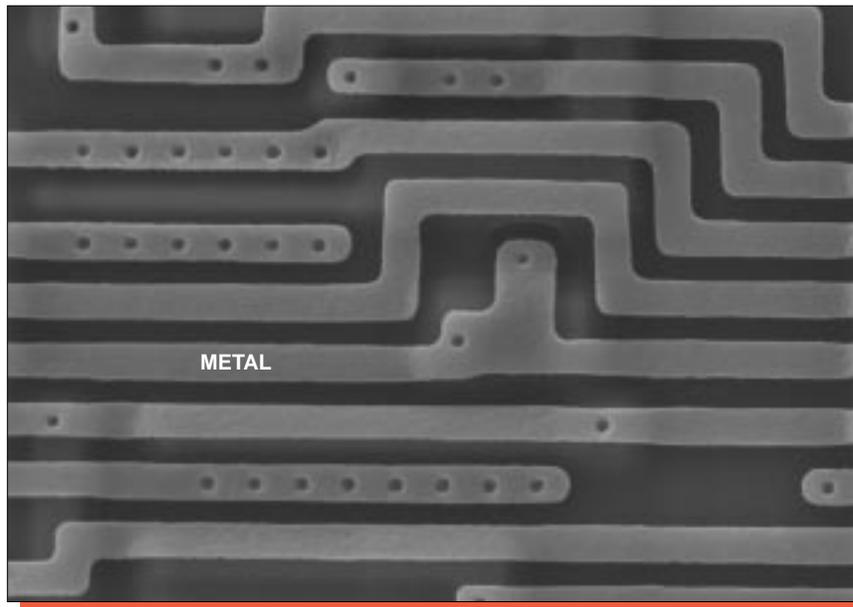


Mag. 5000x

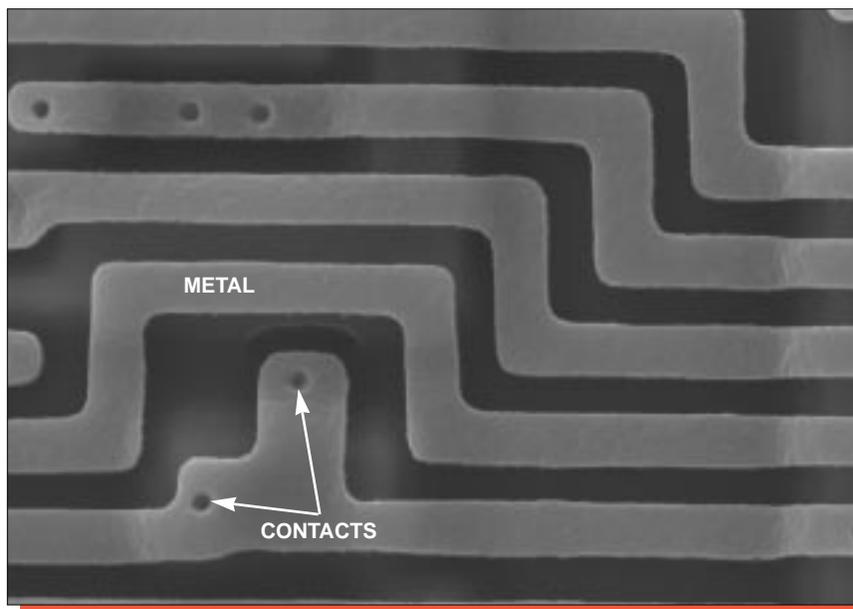


Mag. 20,000x

Figure 11. SEM views of metal coverage. 60°.

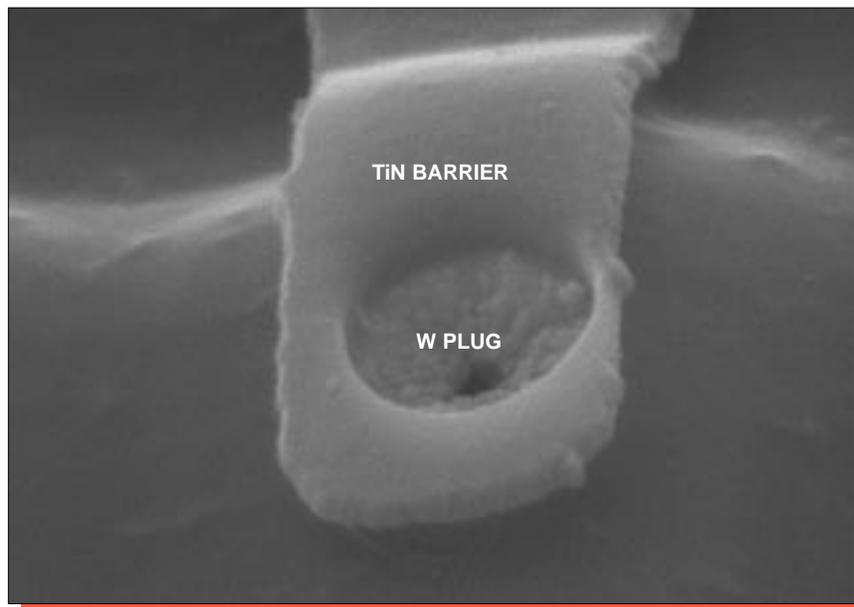


Mag. 3200x

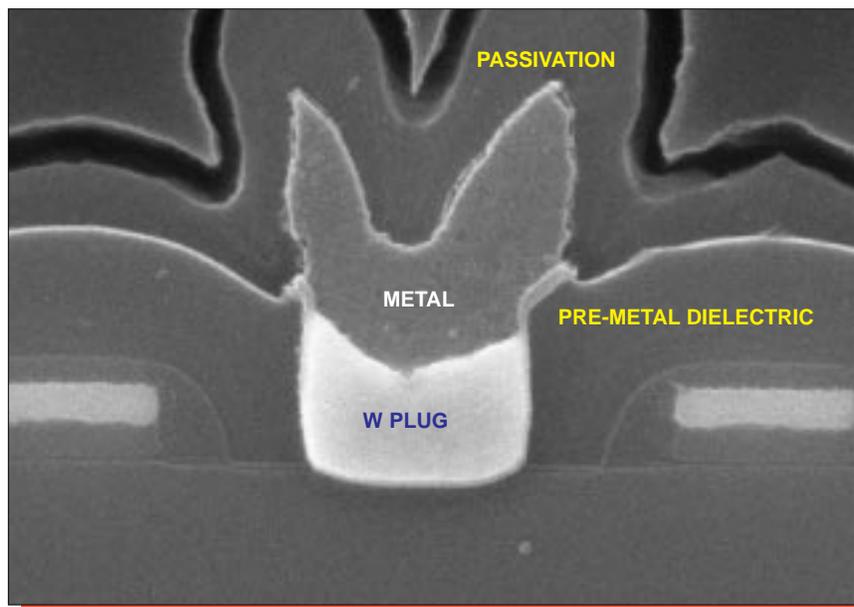


Mag. 5000x

Figure 12. Topological SEM views of metal patterning. 0°.

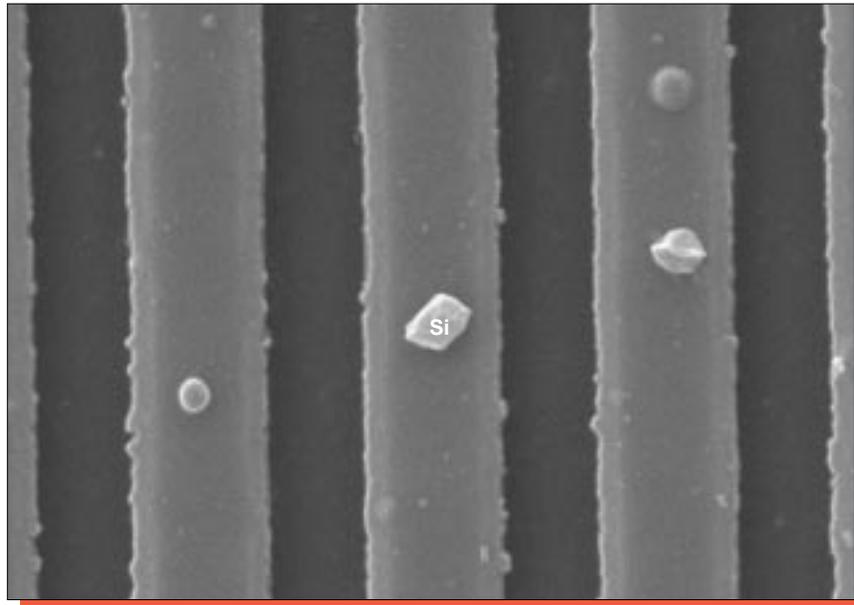


Mag. 35,000x, 45°

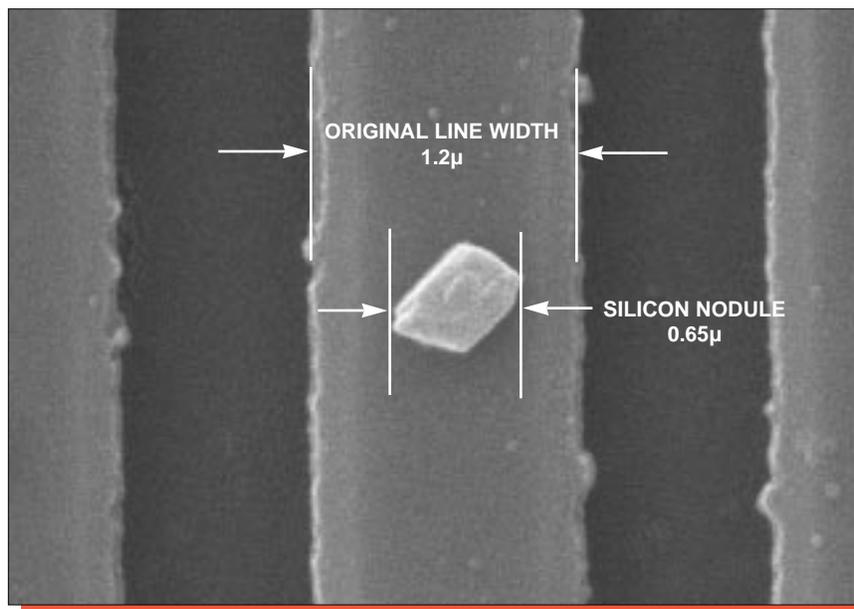


glass etch, Mag. 26,000x

Figure 13. SEM views of barrier coverage and a metal contact.



Mag. 13,000x



Mag. 26,000x

Figure 14. SEM views of silicon nodules following the removal of the aluminum. 0°.

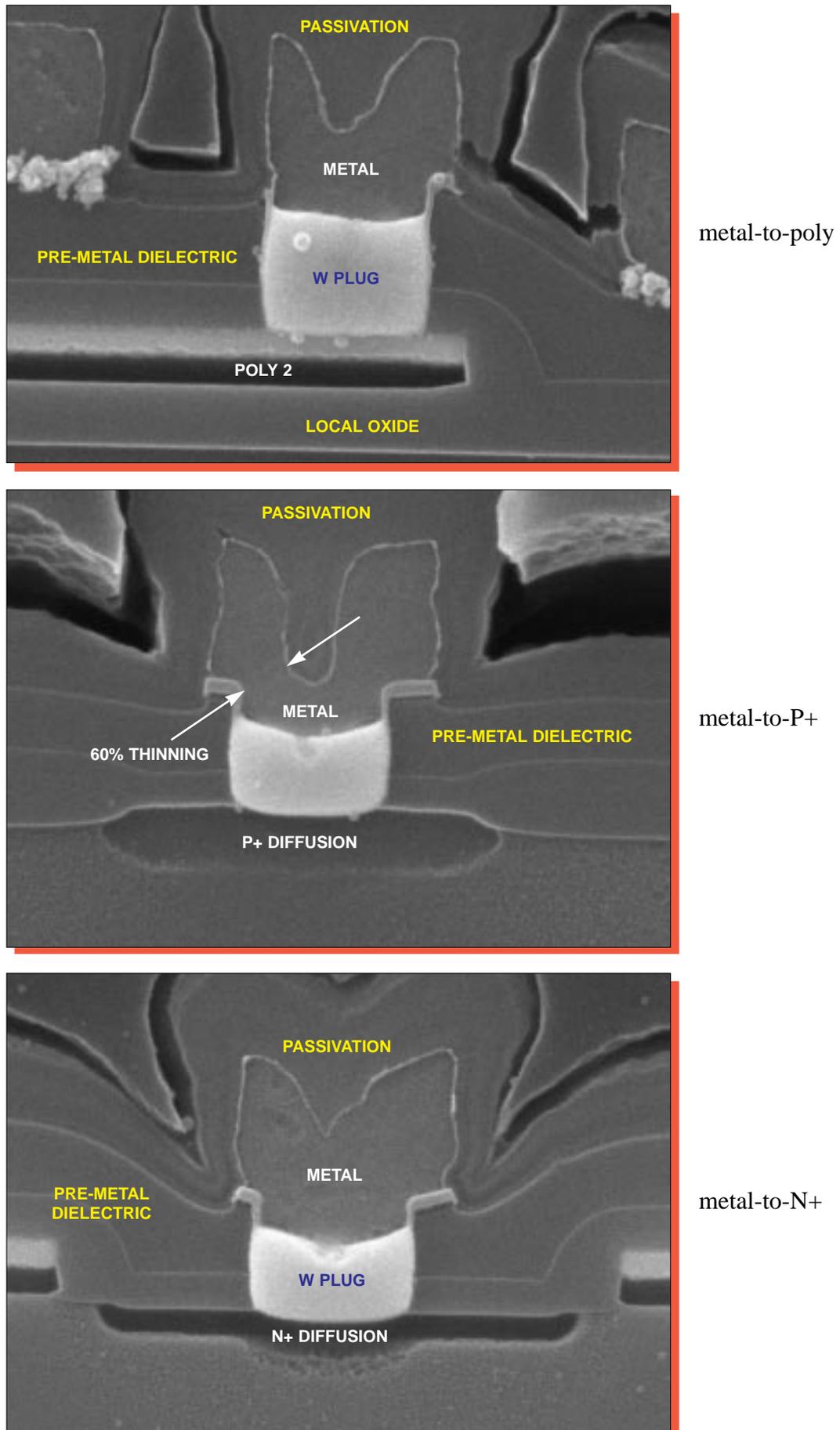
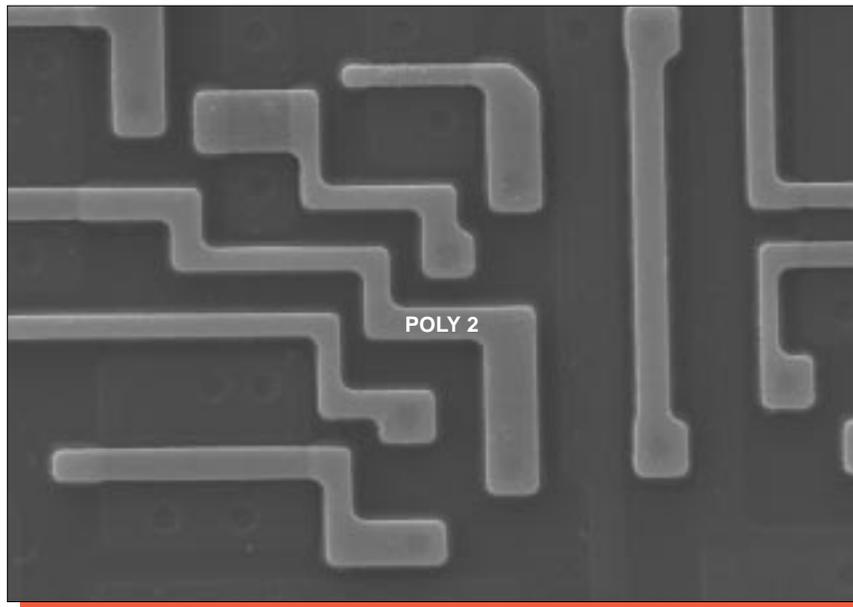
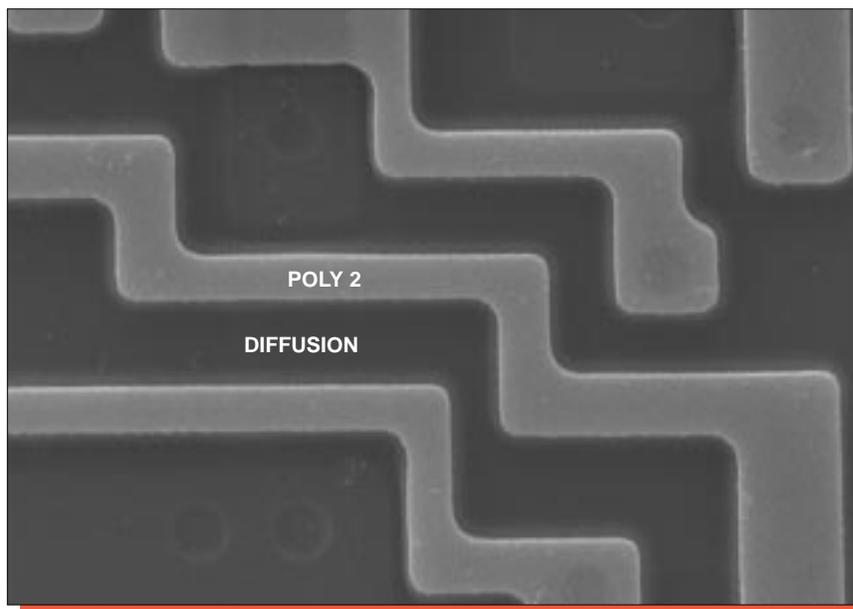


Figure 15. SEM section views of metal contacts. Silicon etch, Mag. 26,000x.

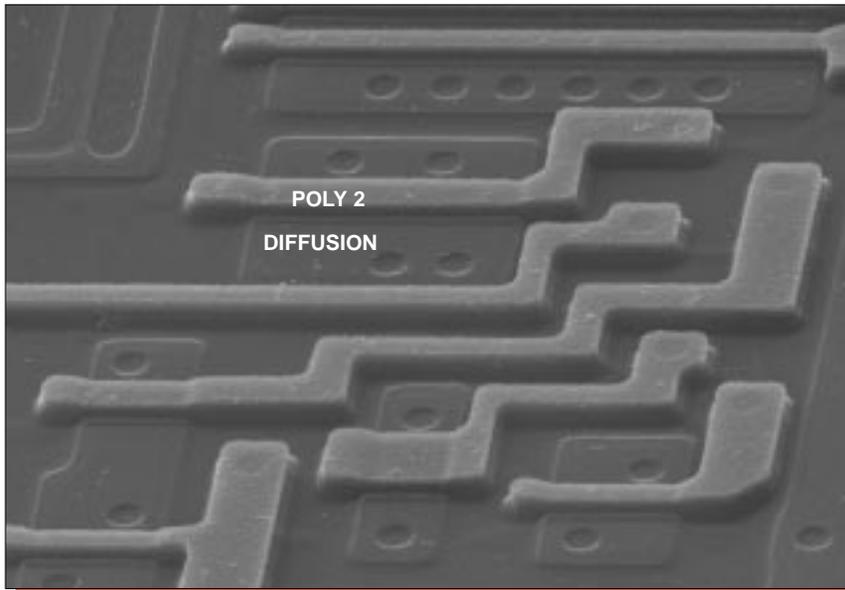


Mag. 3500x

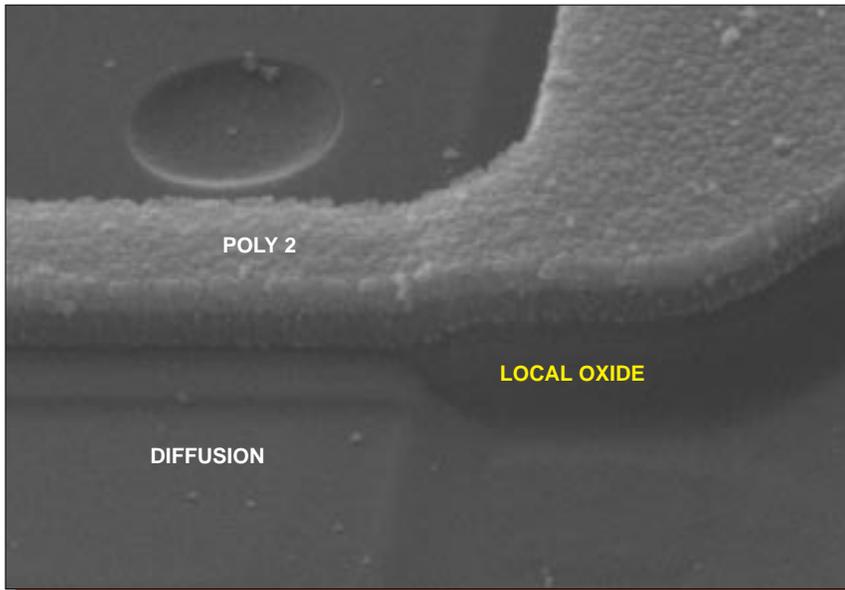


Mag. 7100x

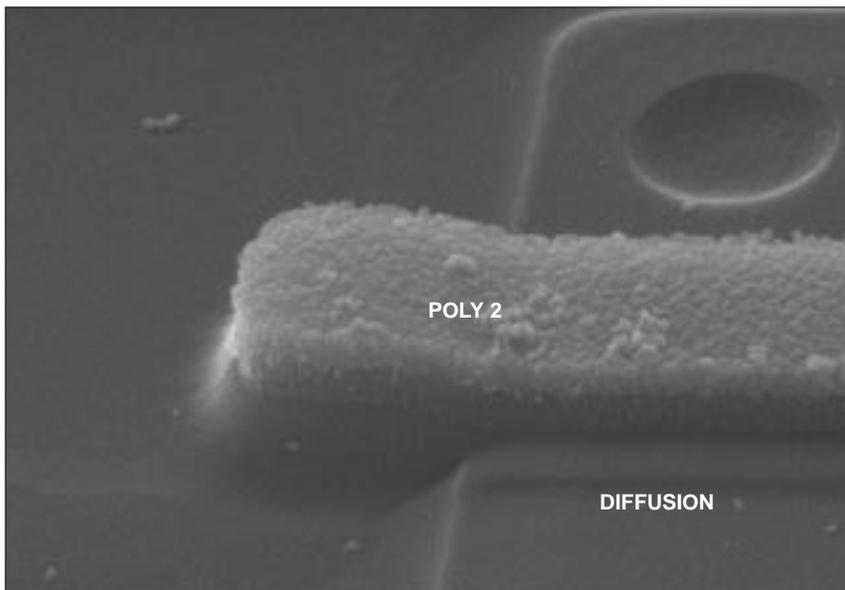
Figure 16. Topological SEM views of poly 2 patterning. 0°.



Mag. 4600x



Mag. 26,000x



Mag. 26,000x

Figure 17. SEM views of poly 2 coverage. 60°.

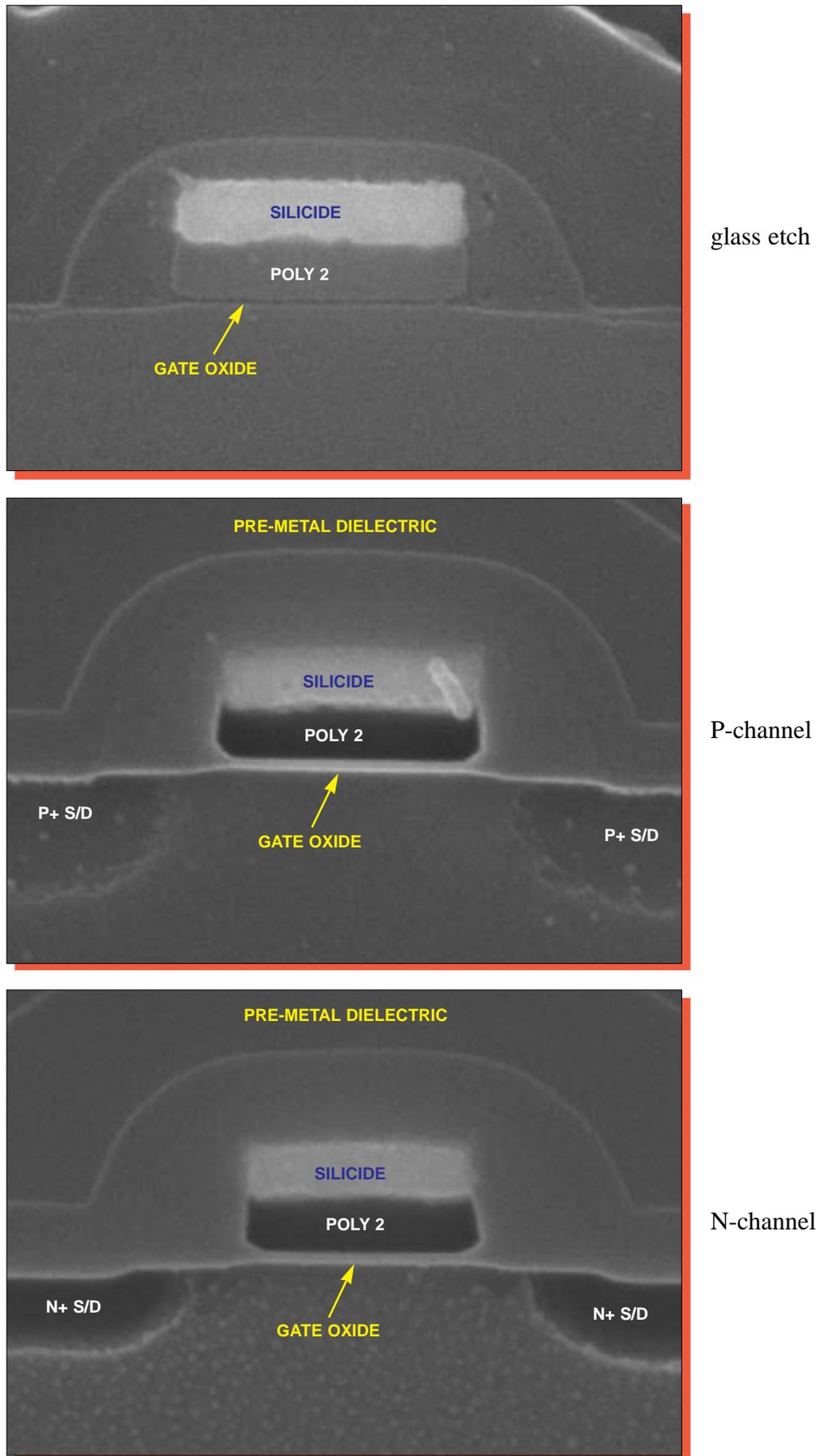


Figure 18. SEM section views of typical transistors. Mag. 52,000x.

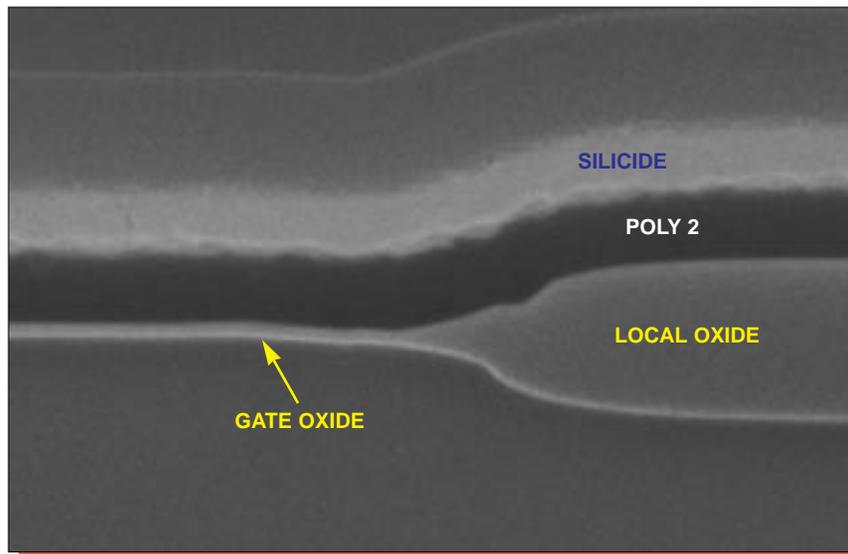
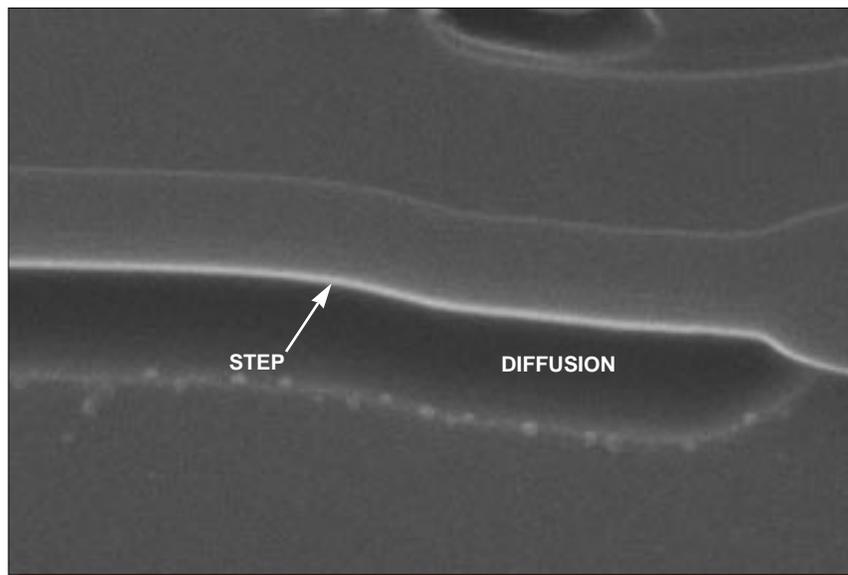
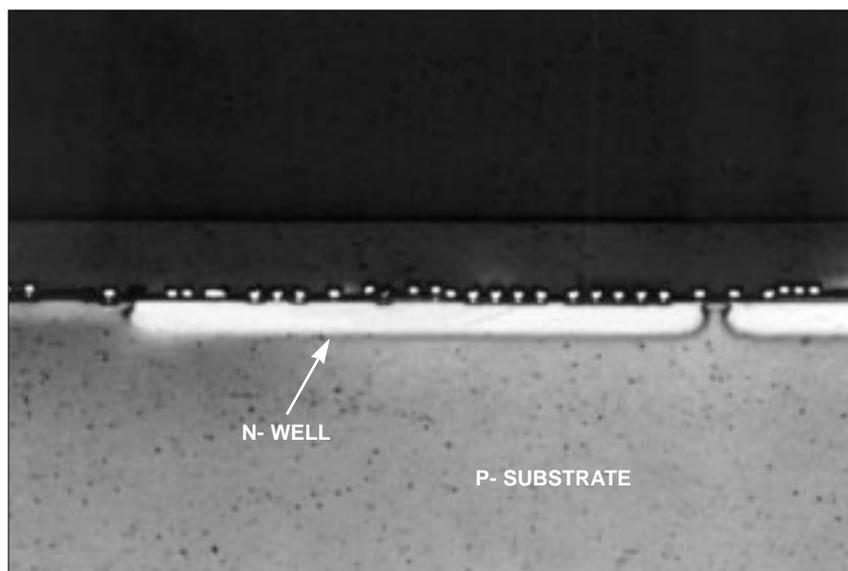


Figure 19. SEM section view of a local oxide birdsbeak. Mag. 52,000x.

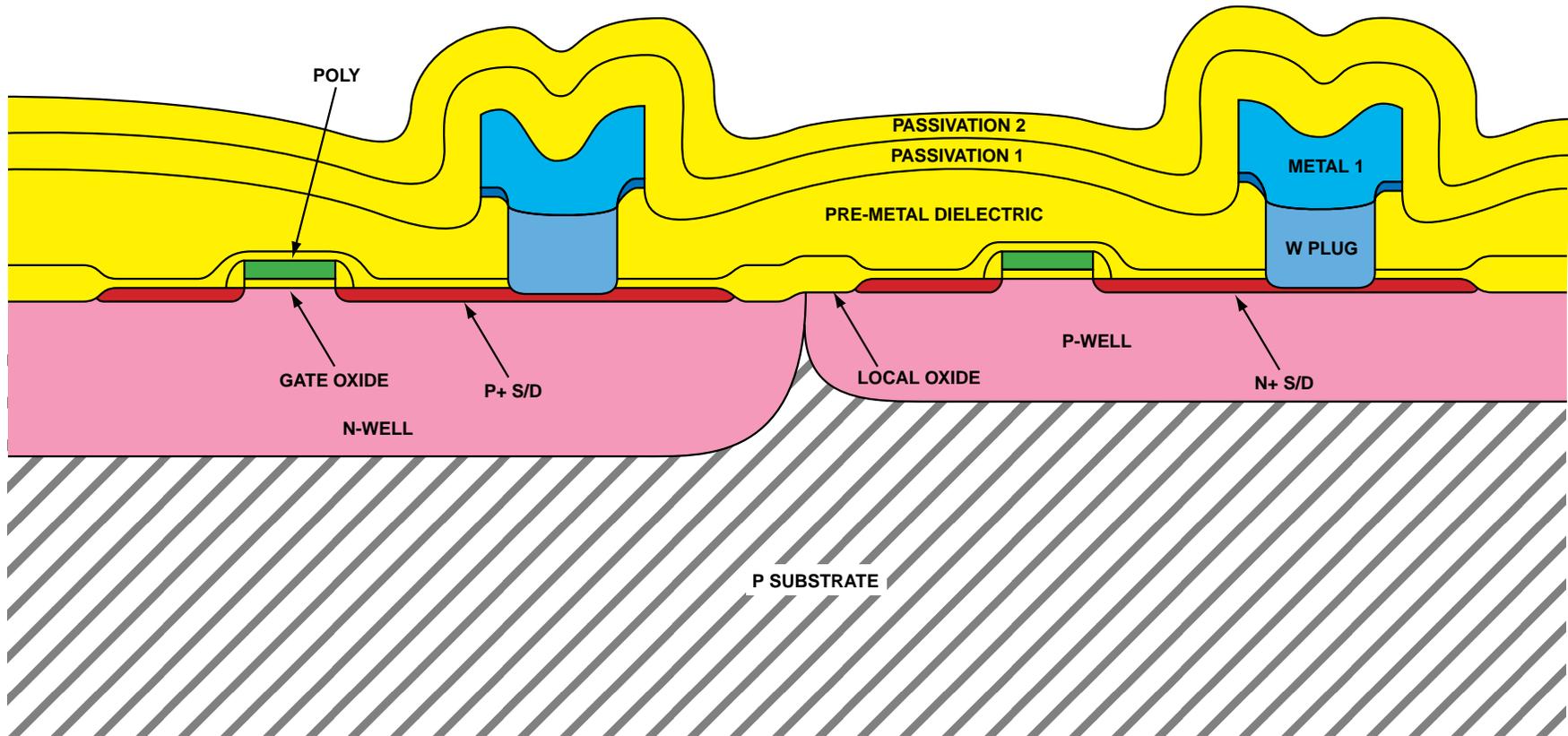


Mag. 52,000x



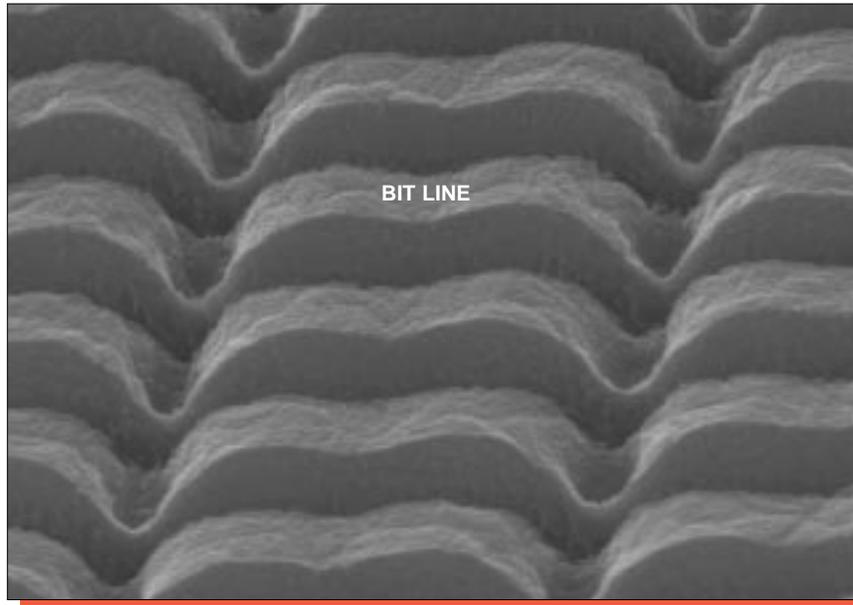
Mag. 800x

Figure 20. Section views illustrating the well structure.

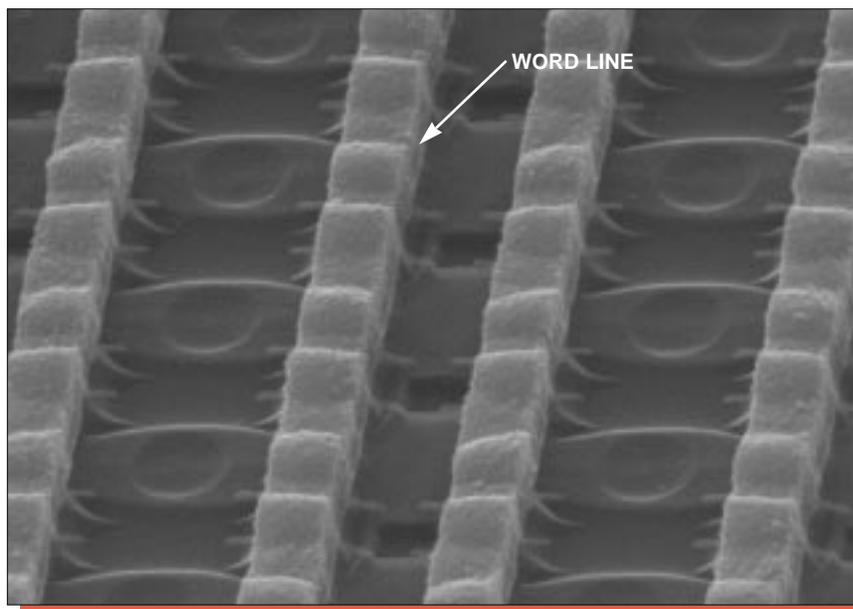


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
Red = Diffusion, and Gray = Substrate

Figure 21. Color cross section drawing illustrating device structure.

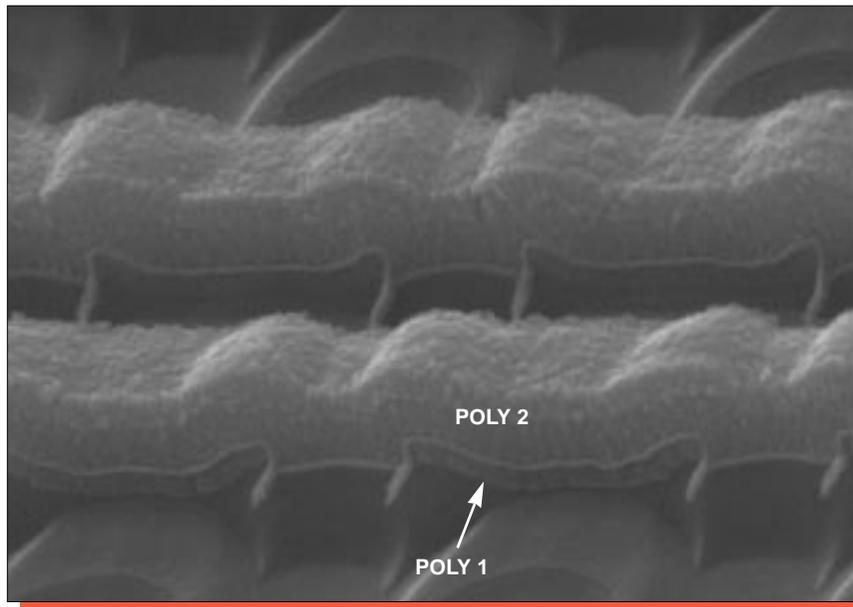


metal

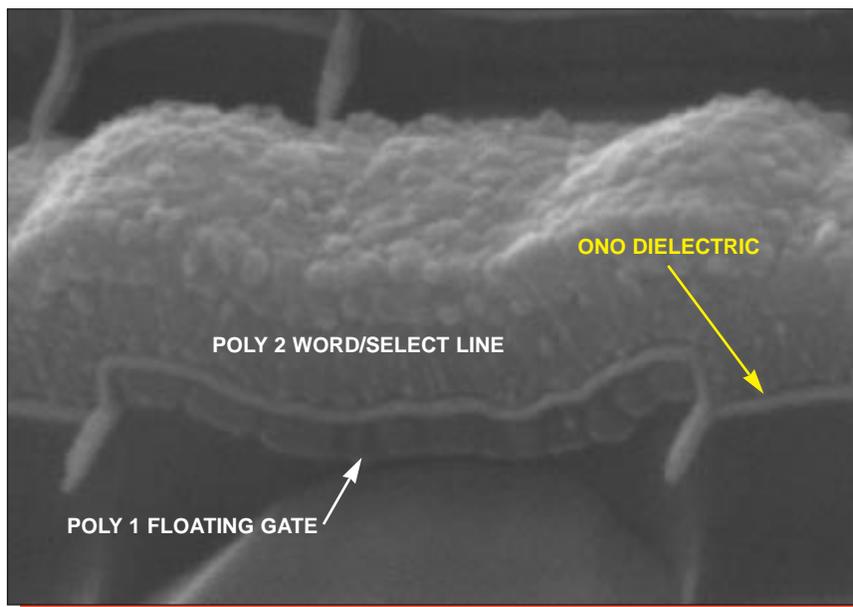


poly

Figure 22. Perspective SEM views of EPROM cell array. Mag. 13,000x, 60°.

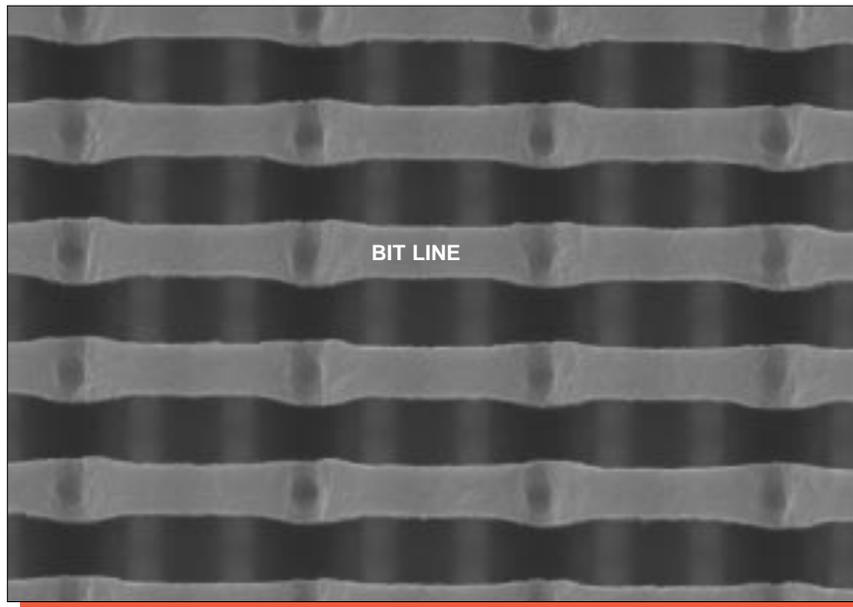


Mag. 26,000x

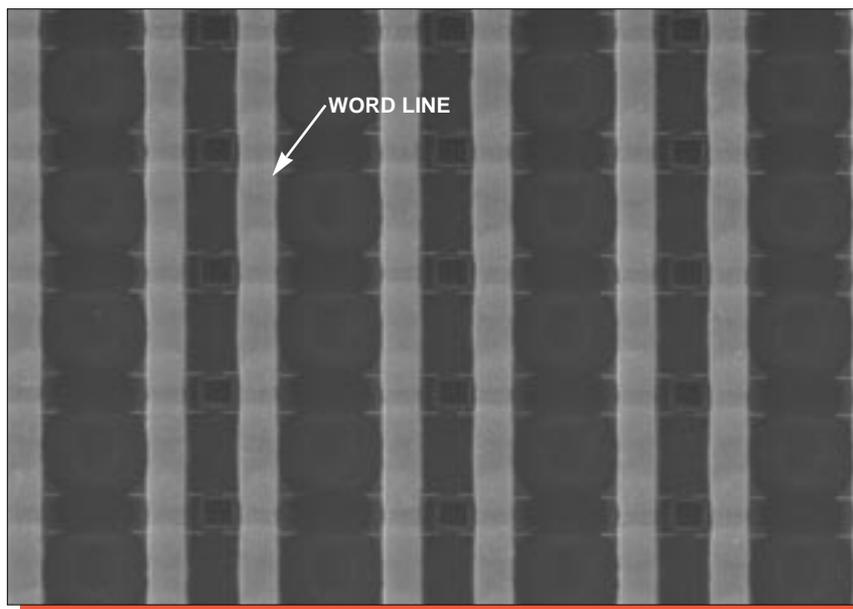


Mag. 52,000x

Figure 23. Detailed SEM views of the EPROM cell array. 60°.



metal



poly

Figure 24. Topological SEM views of the EPROM cell array. Mag. 6500x, 0°.

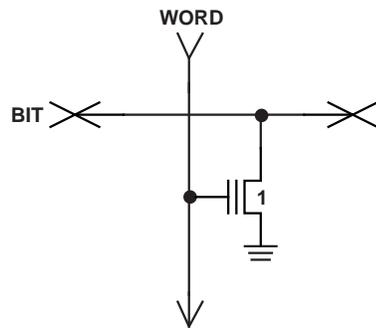
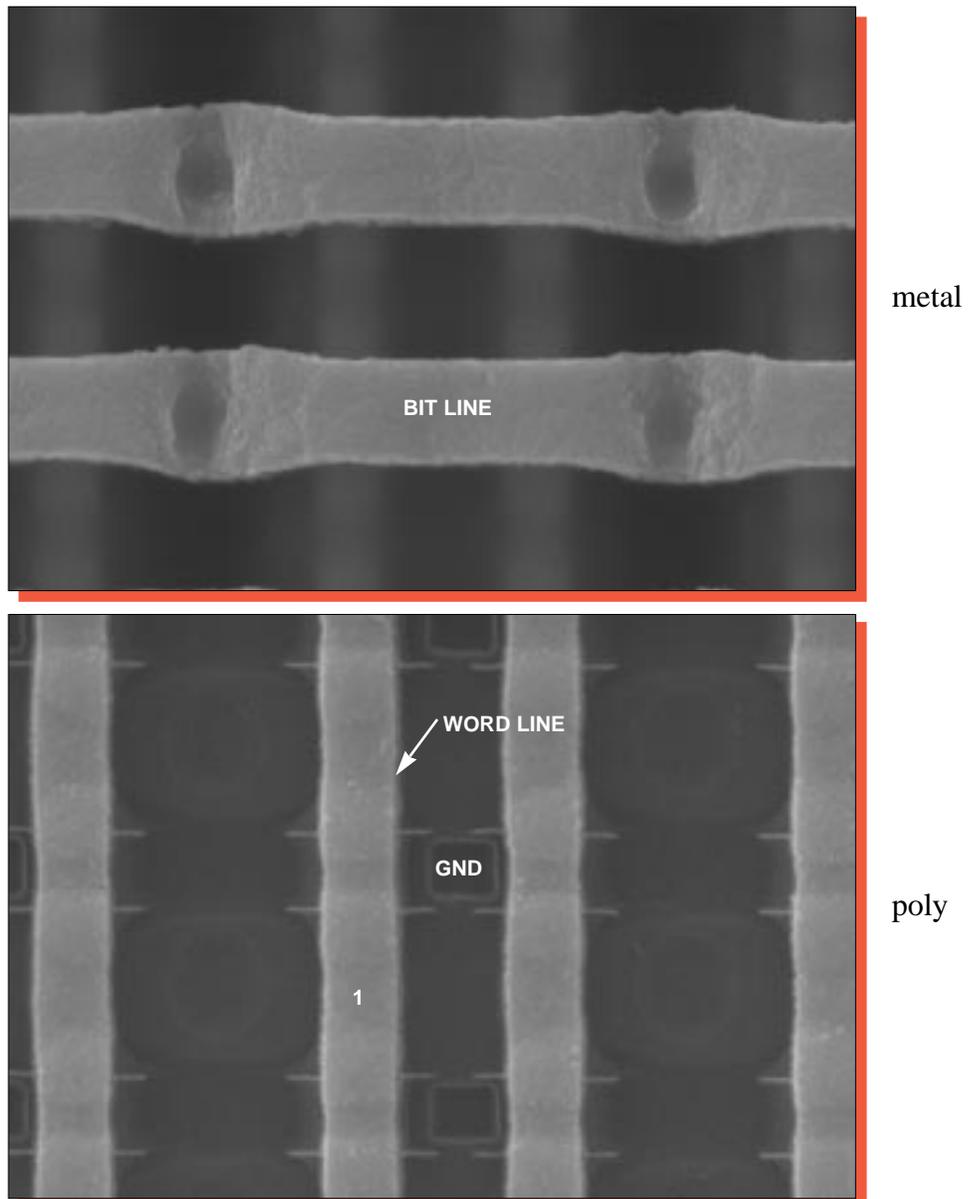
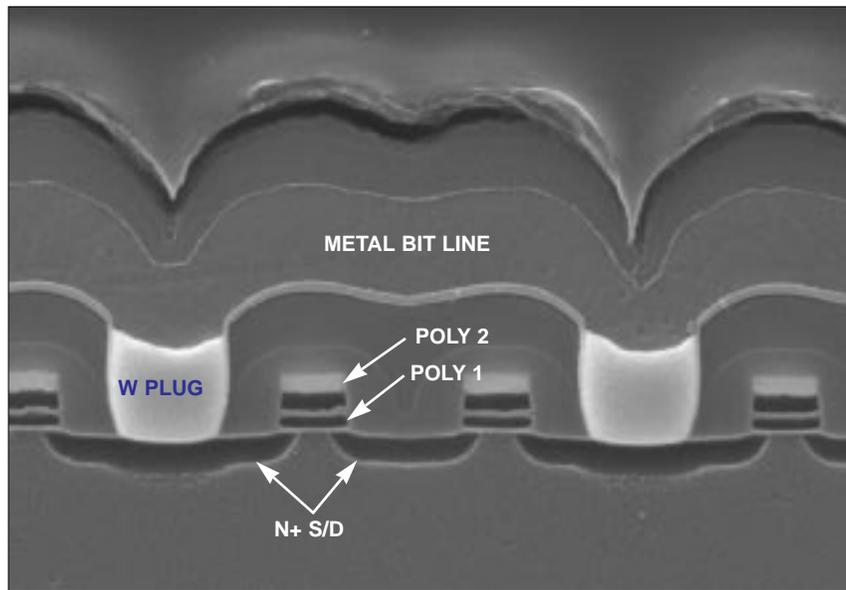
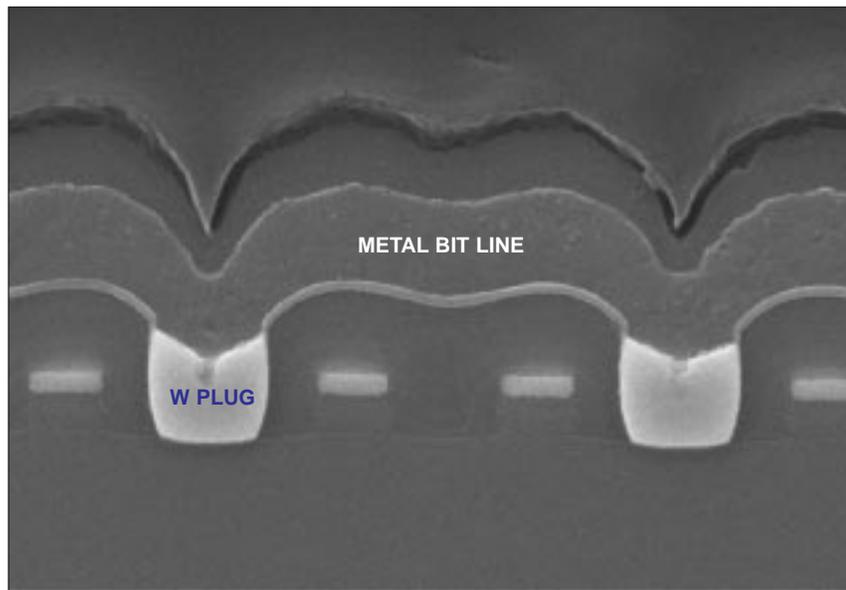
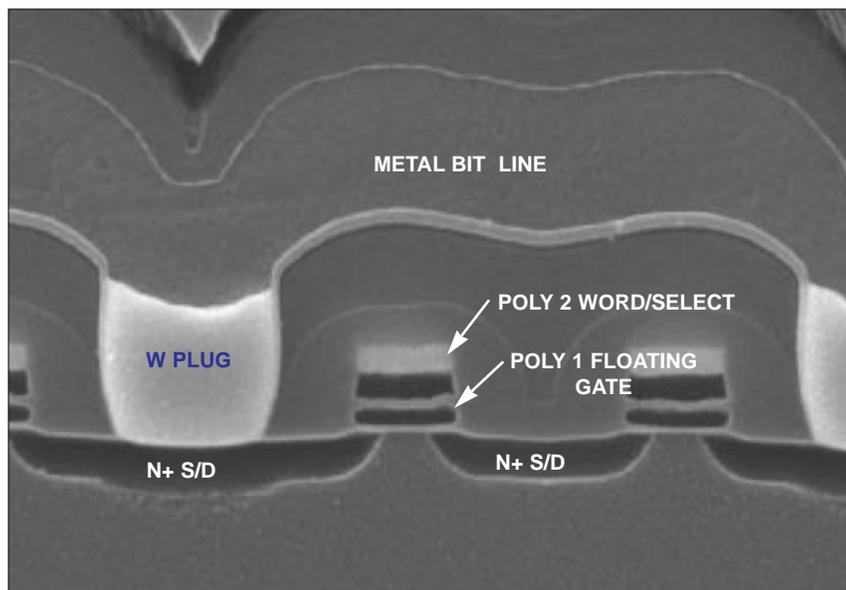


Figure 25. Topological SEM views and schematic of the EPROM cell array.  
Mag. 13,000x, 0°.

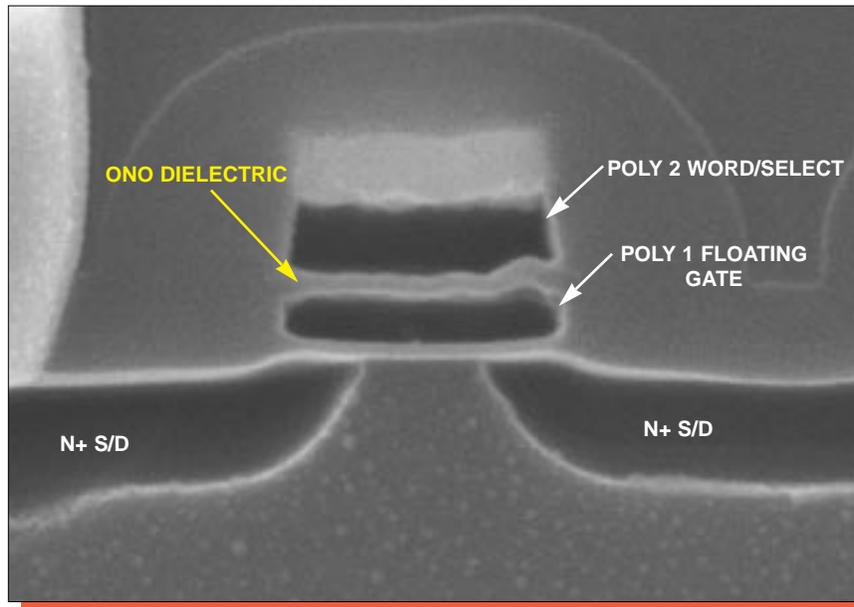


Mag. 13,000x

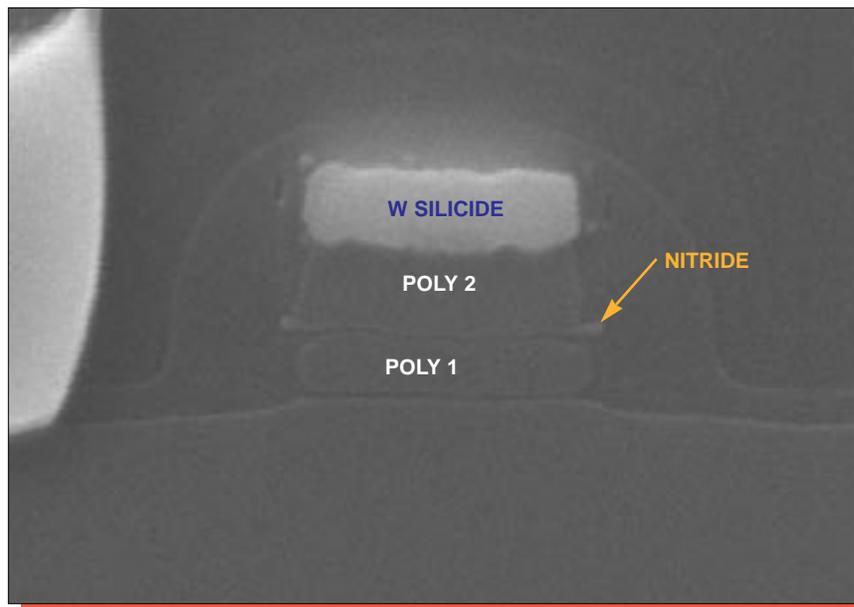
glass etch,  
Mag. 13,000x

Mag. 20,000x

Figure 26. SEM section views of EPROM cell array (parallel to bit line).

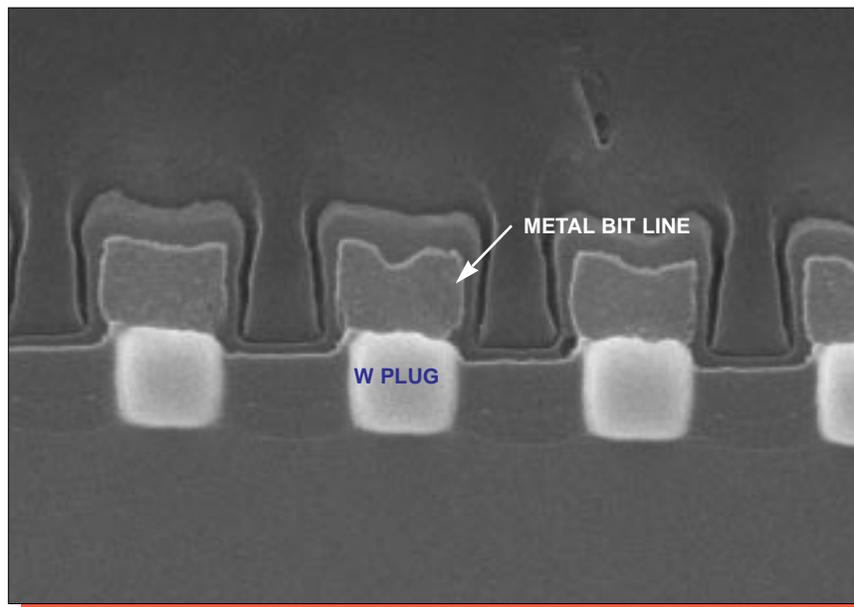


silicon etch

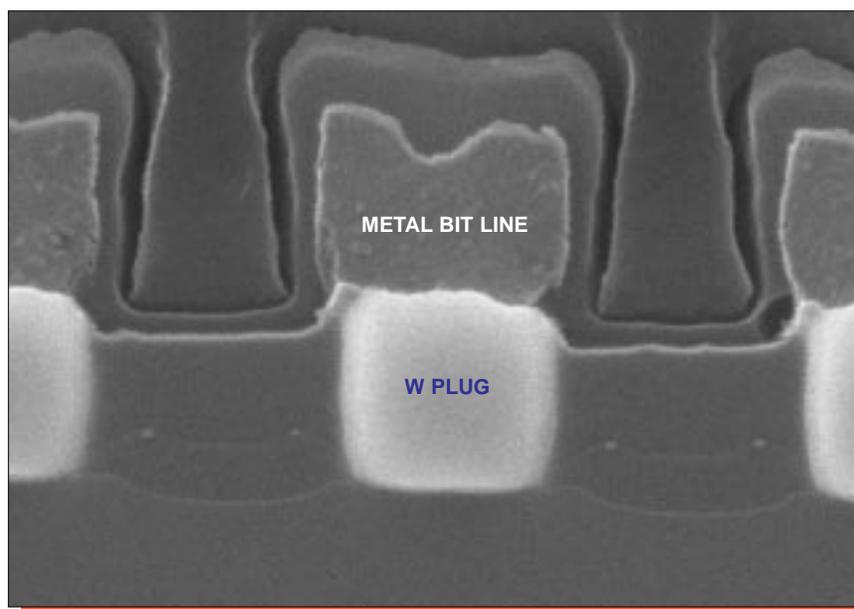


glass etch

Figure 27. Detailed SEM views of the EPROM array (parallel to bit lines).  
Mag. 52,000x.

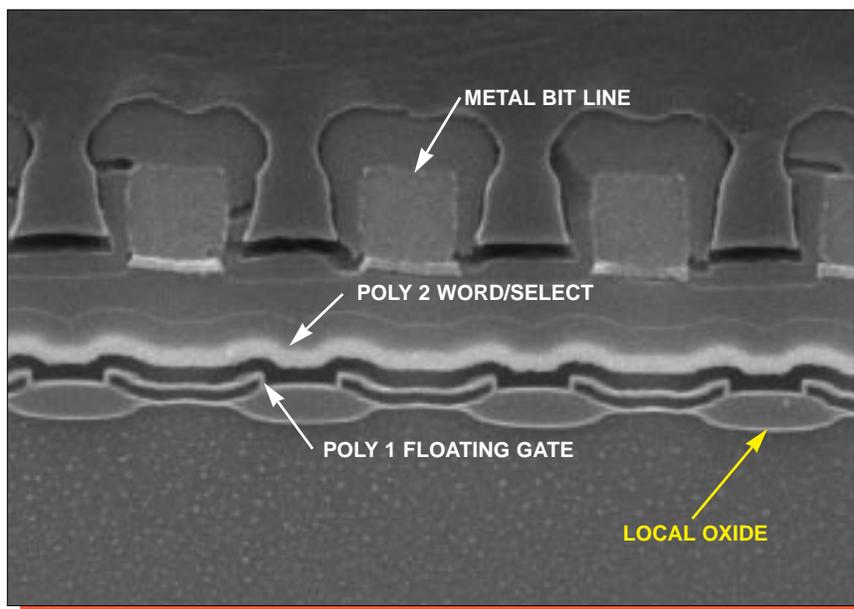


Mag. 13,000x

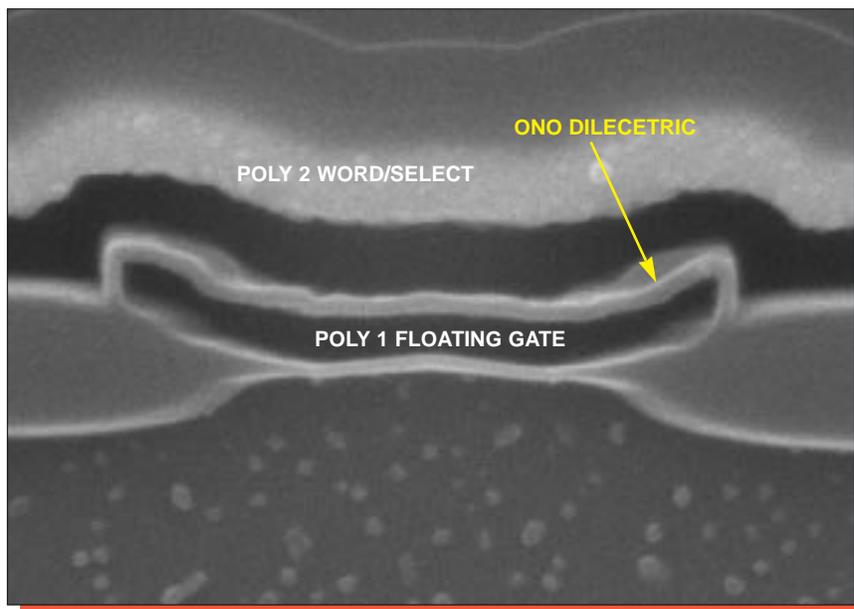


Mag. 26,000x

Figure 28. SEM views of the EPROM cell array (parallel to word lines). Glass etch.

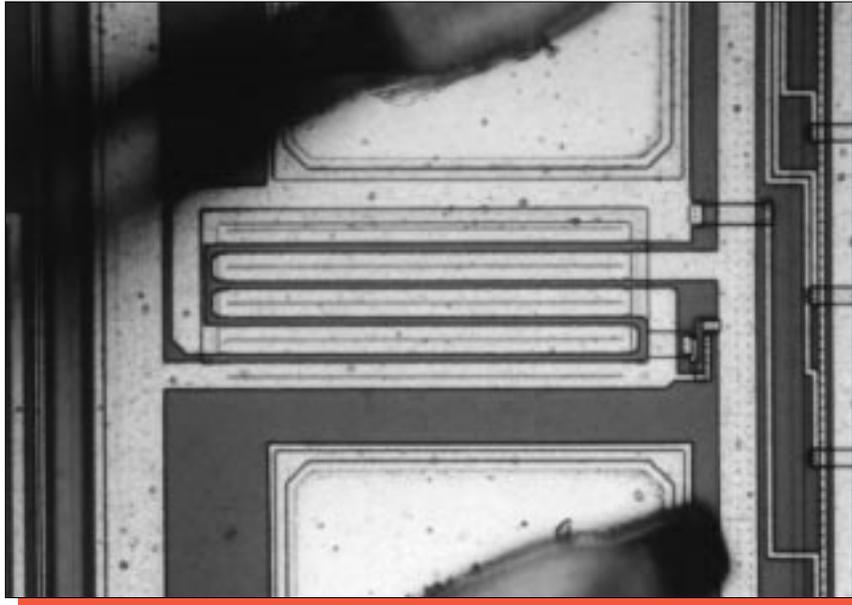


Mag. 13,000x

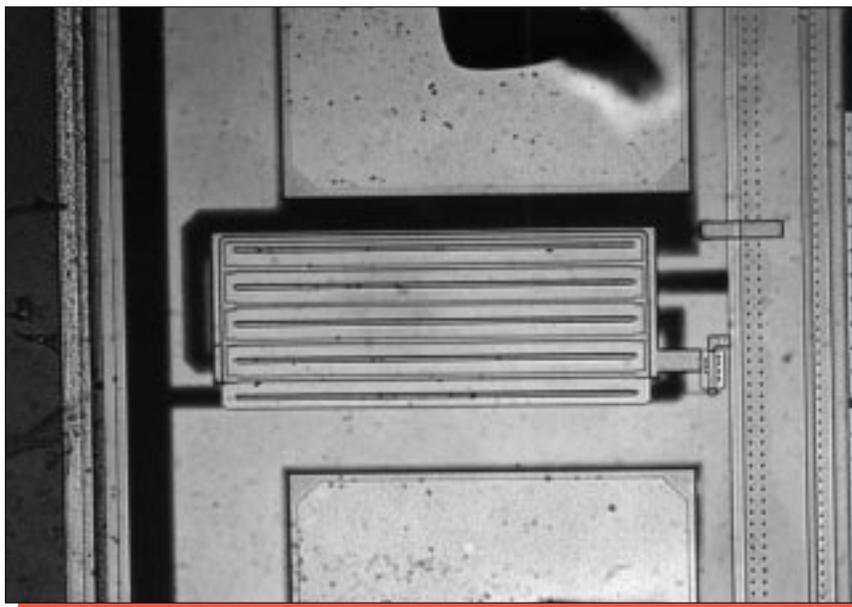


Mag. 52,000x

Figure 29. SEM views of the EPROM cell array (parallel to word line).

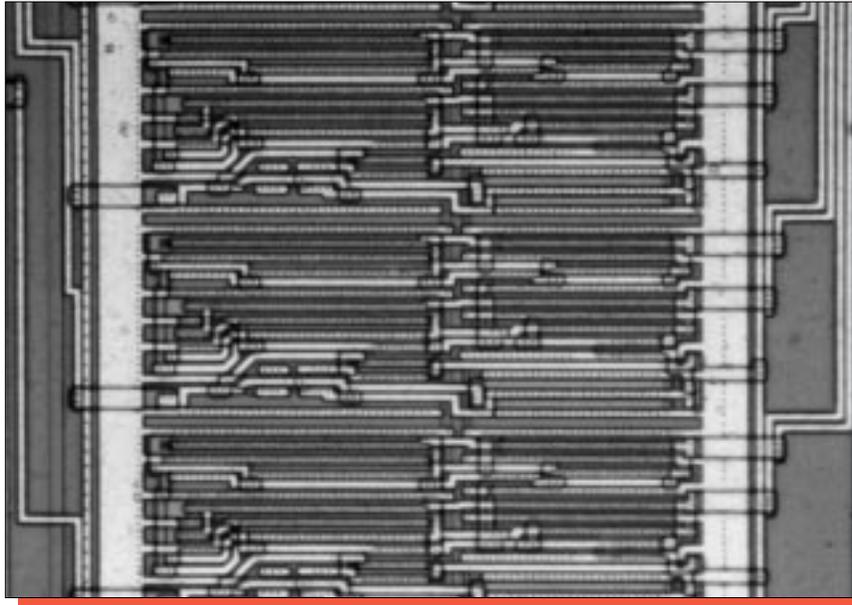


intact

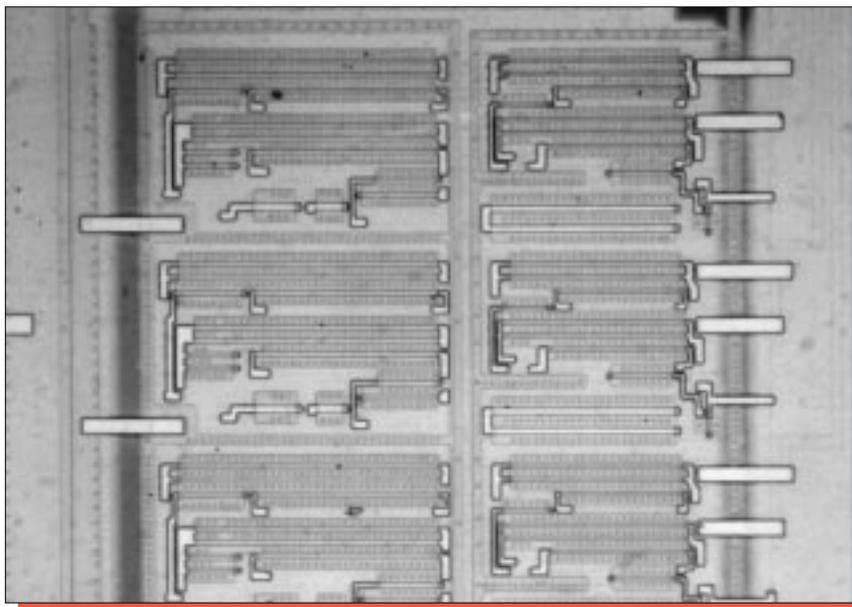


delayed

Figure 30. Optical photographs of input protection structure. Mag. 400x.



intact



delayed

Figure 31. Optical views of general circuitry. Mag. 500x.