# Construction Analysis

# Microchip 93LC86
# 16K Serial EEPROM

Report Number: SCA 9612-515


15022 N. 75th Street
Scottsdale, AZ 85260-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: http://www.ice-corp.com/ice

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## INTRODUCTION

This report describes a construction analysis of the Microchip 93LC86 16K Serial EEPROM. Six devices encapsulated in 8-pin plastic Small Outline IC packages (SOICs) were supplied for the analysis. All devices were date coded 9540.

## MAJOR FINDINGS

**Questionable Items:**[1] None.

**Special Features:**

- Two poly with tunnel-oxide window cells.
- Active load devices, poly capacitors and diffused resistors.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

# TECHNOLOGY DESCRIPTION

## Assembly:

- Devices were encapsulated in 8-pin plastic SOICs.
- Copper (Cu) leadframe internally plated with silver (Ag).
- External pins (gull wing) were tinned with tin/lead (SnPb) solder.
- Lead-locking provisions (anchors) at all pins.
- Thermosonic ball bond method employing 0.9 mil O.D. gold wire.
- Sawn dicing (full depth).
- Silver-epoxy die attach.

## Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells, on an N substrate.
- Overlay passivation: A thin silicon-nitride over a multilayered glass and a densified oxide.
- Metallization: A single metal layer consisted of silicon and copper doped aluminum. No cap or barrier metals were employed.
- Intermediate glass: A single layer of BPSG over grown/densified oxides. The glass was reflowed following the contact cuts.

## TECHNOLOGY DESCRIPTION (continued)

- Polysilicon: Two layers of dry-etched polysilicon (no silicide). Poly 2 was used to form word lines and program lines in the cell array and all gates on the die. Poly 1 was used to form the floating gates in the array and to form poly-to-poly capacitors.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. No sidewall spacers were present on the gates and no evidence of LDD structures were found.

- Wells: Twin-wells in an N substrate. No step was noted in the field oxide at well boundaries.

- Memory cells: The memory cell design consisted of a poly 2 word line and program line and a poly 1 floating gate. Metal formed the bit lines. Programming is achieved through an ultra-thin (tunnel) oxide. The interpoly dielectric consisted of oxide-nitride-oxide (ONO).

- Fuses: No redundancy fuses were present.

- Buried contacts: Direct poly-to-diffusion (buried) contacts were not used.

## ANALYSIS RESULTS I

**Assembly:** **Figures 1 - 11**

**Questionable Items:**[1] None.

**Special Features:** None.

**General Items:**

- Devices were packaged in 8-pin plastic SOICs with gull wing leads for surface mount applications.

- Overall package quality: Normal. The leadframe was constructed of copper (Cu) and internal portions spot-plated with silver (Ag). Pins were plated externally with tin-lead (SnPb). Small gaps were noted at the lead exits; however, they do not appear to be severe enough to be a concern (Figure 4).

- Die dicing: Die separation was by full-depth sawing and showed normal quality workmanship. No large chips or cracks were noted at die edges.

- Die attach: The die was attached using an adequate amount of silver-epoxy. No significant voids were noted.

- Wirebonding: Thermosonic ball bond method using 0.9 mil O.D. gold wire. Intermetallic formation was complete. No bond lifts occurred and bond pull strengths were good (see page 10). Wire spacing and placement was also good.

- No die coat was employed.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## ANALYSIS RESULTS II

**Die Process and Design:** **Figures 12 - 36**

**Questionable Items:**[1] None.

**Special Features:**

- Two poly with tunnel-oxide window cells.
- Active load devices, poly capacitors and diffused resistors.

**General Items:**

- Fabrication process: Selective oxidation CMOS process employing twin-wells in an N substrate.
- Design and layout: Die layout was clean and efficient. Alignment was good at all levels.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.
- Overlay passivation: A thin layer of silicon-nitride over a multilayered glass and undoped oxide. The silicon-nitride layer thinned on the sidewalls (Figure 16); however, overlay integrity tests indicated defect-free passivation. Edge seal was good.
- Metallization: The single metal layer consisted of silicon and copper doped aluminum. No cap or barrier metals were employed. A thin layer appeared to be present on top and under the metal layer. After extensive WDX and EDX analysis

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

**ANALYSIS RESULTS II (continued)**

it appears to be a non-typical material that resulted from the production process. No problems are foreseen.

- Metal patterning: The metal layer was defined by a dry etch of good quality. No problems were noted.

- Metal defects: No voiding, notching, or neckdown of the metal layers was found. Silicon nodules occupied up to 50 percent of the metal line widths. Silicon nodules > 50 percent of the line widths can cause an unacceptable increase in the aluminum's susceptibility to electromigration, but this is entirely dependent on the design specifications.

- Aluminum thinned up to 75 percent at some contact edges (Figure 21). MIL-STD-883D states up to 70 percent thinning is allowable for contacts of this size.

- Contacts: Metal contact cuts appeared to be defined by a wet-etch, followed by a glass reflow. All contacts were completely surrounded by metal.

- Pre-metal dielectric: A layer of BPSG over grown oxides. This layer was well reflowed following contact cuts and no problems were found.

- Sidewall spacers: Oxide sidewall spacers were not used. The reflow glass deposited after S/D implant did not completely fill the corners left by the outside edges of the poly oxide, leaving what we term "worm holes". The effects on product performance or reliability are unknown.

- Polysilicon: Two levels of polysilicon. Poly 2 formed all gates on the die, the program lines and word lines (select gates) in the array. Poly 1 formed the floating gates in the array and to form poly-to-poly capacitors. Definition was by a dry etch of good quality. As noted previously, poly-to-poly capacitors were used, and active loads (fairly unusual in modern technology) were also employed.

**ANALYSIS RESULTS II (continued)**

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeak or elsewhere.

- Diffusions: Standard implanted N+ and P+ diffusions were used for sources and drains. No problems were found. As mentioned, no evidence of any LDD structure was present and sidewall spacers were not used on the poly gates.

- Wells: Twin-wells were used. No step was noted in the field oxide at well boundaries. Definition was normal.

- Buried contacts: Direct poly-to-diffusion (buried) contacts were not used.

- Memory cells: The memory cell design consisted of a poly 2 word line (select gate) and program line and a poly 1 floating gate. Programming is achieved through an ultra thin (tunnel) oxide window. The interpoly dielectric consisted of oxide-nitride-oxide (ONO). Metal formed the bit lines. The cell size is 5.5 x 11 microns (60.5 microns$^2$).

- Fuses: No fuses were used.

**Special Items:**

- ESD sensitivity: ESD tests were performed on samples 1 and 2 and revealed that all pins tested passed pulses of up to $\pm$4000V.

- Latch up: Latch-up tests were performed on samples 3 and 4. Pins were tested at $\pm$200 mA per the JEDEC Standard No.17 and revealed that no pin latched up on either sample.

## PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

ESD sensitivity test

Latch-up sensitivity test

X-ray

Package section

Decapsulation

Internal optical inspection

SEM inspection of assembly features and passivation

Passivation integrity test

Wirepull test

Passivation removal

SEM inspection of metal

Metal removal and inspect silicon nodules and contacts

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

| | |
|---|---|
| Package integrity | N (small gaps at lead exits) |
| Package markings | G |
| Die placement | G |
| Die attach quality | N |
| Wire spacing | G |
| Wirebond placement | G |
| Wirebond quality | G |
| Dicing quality | G |
| Wirebond method | Thermosonic ball bonds using 0.9 mil gold wire. |
| Die attach method | Silver-epoxy |
| Dicing method: | Sawn (full depth) |
| | |
| Die surface integrity: | |
| Tool marks (absence): | G |
| Particles (absence): | G |
| Contamination (absence): | G |
| Process defects (absence): | G |
| General workmanship | G |
| Passivation integrity | G |
| Metal definition | G |
| Metal integrity | NP[1] |
| Contact coverage | G |
| Contact registration | G |
| Contact defects | G |

[1] *Silicon nodules occupied up to 50 percent of metal line widths.*

*G = Good, P = Poor, N = Normal, NP = Normal/Poor*

## PACKAGE MARKINGS

| Top | Bottom |
|---|---|
| 93LC86 | 9540 |
| (Logo) I/SN | CAW |

## WIREBOND STRENGTH

| | |
|---|---|
| Wire material: | 0.9 mil diameter gold |
| Die pad material: | aluminum |
| Material at package post: | silver |
| **Sample #** | **5** |
| # of wires tested: | 8 |
| Bond lifts: | 0 |
| Force to break - high: | 14.0g |
| - low: | 8.0g |
| - avg.: | 10.5g |
| - std. dev.: | 1.9 |

## DIE MATERIAL ANALYSIS

| | |
|---|---|
| Passivation:* | A layer of silicon-nitride over a multilayered glass and an undoped oxide. |
| Metal: | Aluminum doped with silicon and copper.* |
| Intermediate oxide:* | Borophosphosilicate glass (BPSG) containing 3.2 wt. percent boron and 5.7 wt. percent phosphorus. |

**There is no known method for determining the exact amount of silicon or copper in the aluminum of a finished die.*

## PACKAGE MATERIAL ANALYSIS

| | |
|---|---|
| Leadframe: | Copper (Cu) |
| Internal plating: | Silver (Ag) |
| External plating: | Tin-lead (SnPb) |
| Die attach: | Silver-epoxy (Ag) |

## HORIZONTAL DIMENSIONS

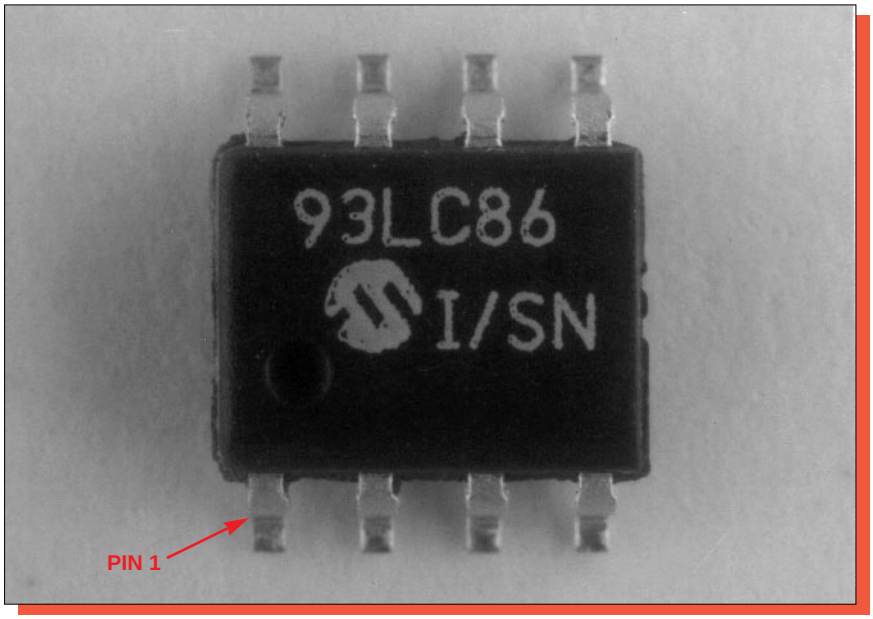
| | |
|---|---|
| Die size: | 1.9 x 3.2 mm (75 x 125 mils) |
| Die area: | 6.0 $mm^2$ (9,375 $mils^2$) |
| Min pad size: | 0.1 x 0.1 mm (4.2 x 4.2 mils) |
| Min pad window: | 0.09 x 0.09 mm (3.6 x 3.6 mils) |
| Min pad space: | 0.1 mm (3.7 mils) |
| Min pad-to-metal: | 17.5 microns |
| Min metal width: | 1.9 micron |
| Min metal space: | 1.3 micron |
| Min metal pitch: | 3.2 microns |
| Min contact: | 1.6 micron (round) |
| Min contact space (arrays): | 2.2 microns |
| Min poly 2 width: | 2.0 microns |
| Min poly 2 space: | 1.3 micron |
| Min poly 1 width: | 3.3 microns |
| Min poly 1 space: | 1.5 micron |
| Min gate length - (N-channel): | 2.0 microns |
| - (P-channel): | 2.8 microns |
| Cell size: | 60.5 $microns^2$ |
| Cell pitch: | 5.5 x 11 microns |

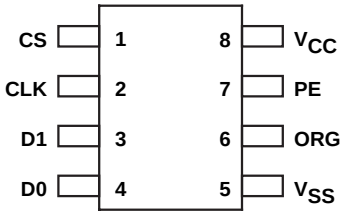
## VERTICAL DIMENSIONS

| | |
|---|---|
| Die thickness: | 0.4 mm (15 mils) |

**Layers**

| | |
|---|---|
| Passivation: | 0.8 micron |
| Metallization: | 1.0 micron |
| Pre-metal glass: | 1.5 micron |
| Oxide on poly 2: | 0.15 micron |
| Poly 2: | 0.4 micron |
| Poly 1: | 0.35 micron |
| Local oxide: | 1.0 micron |
| N+ S/D diffusion: | 0.3 micron |
| P+ S/D diffusion: | 0.35 micron |
| N-well: | 2.0 microns (approx.) |
| P-well: | 2.5 microns (approx.) |



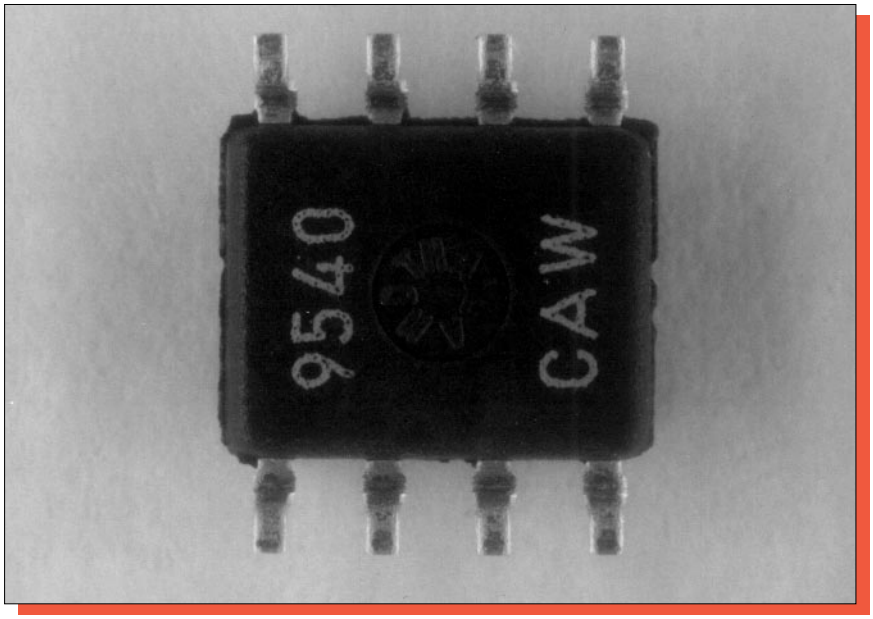
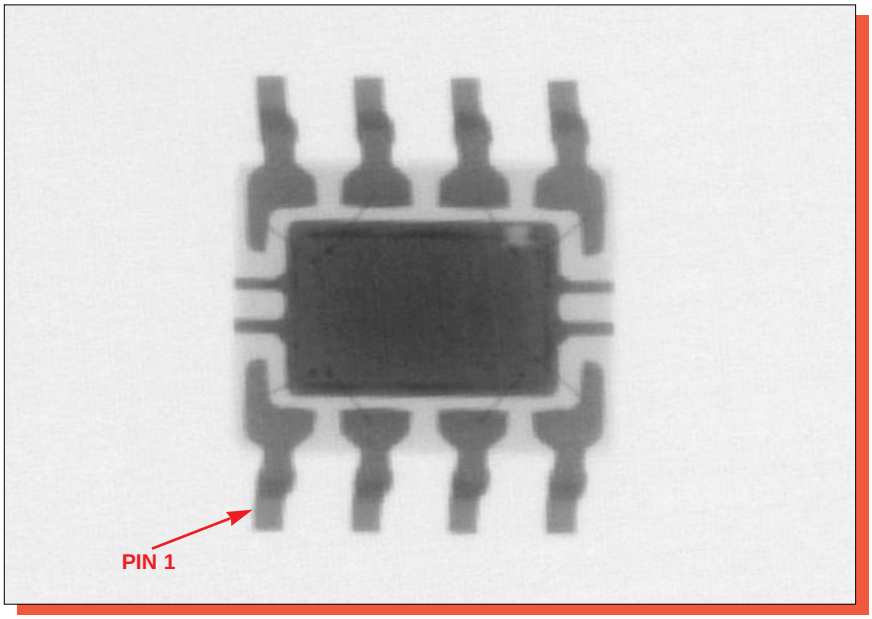




Figure 1. Package photographs and pinout of Microchip 93LC86 16K Serial EEPROM. Mag. 10x.



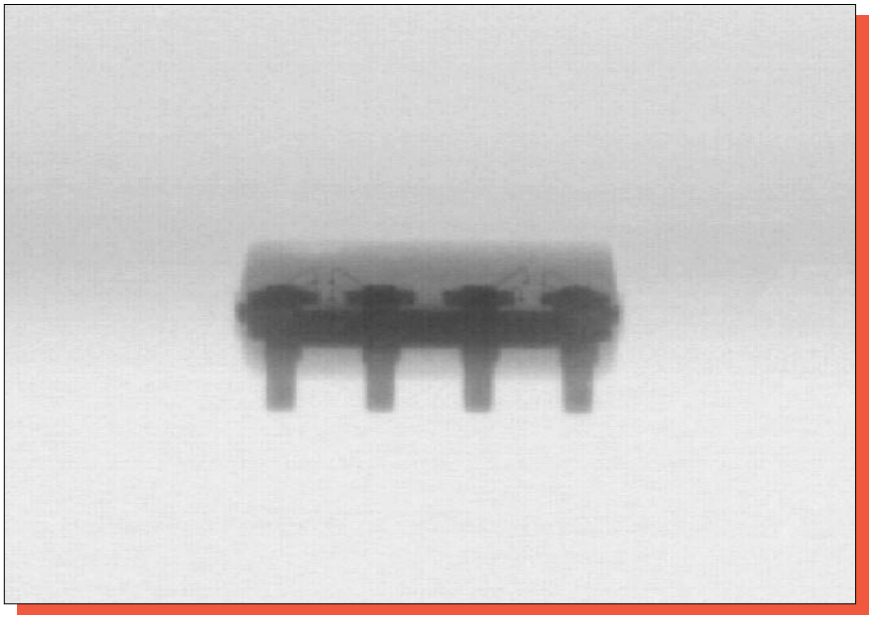



Figure 2. X-ray views of the Microchip 93LC86 16K Serial EEPROM. Mag 10x.

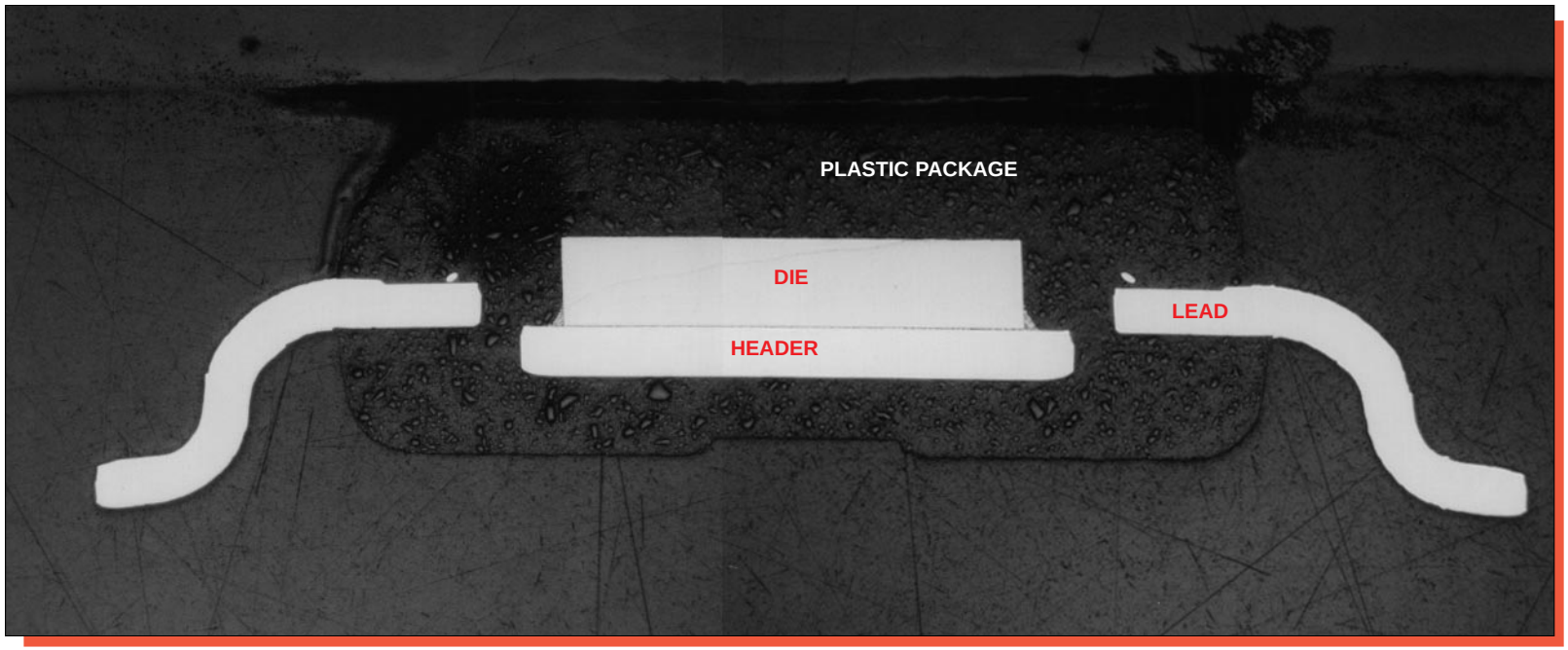
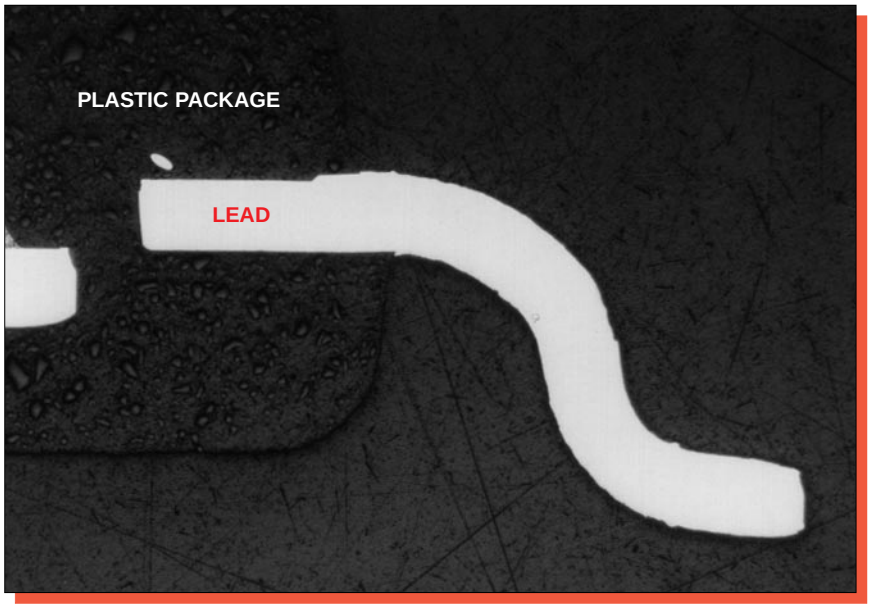
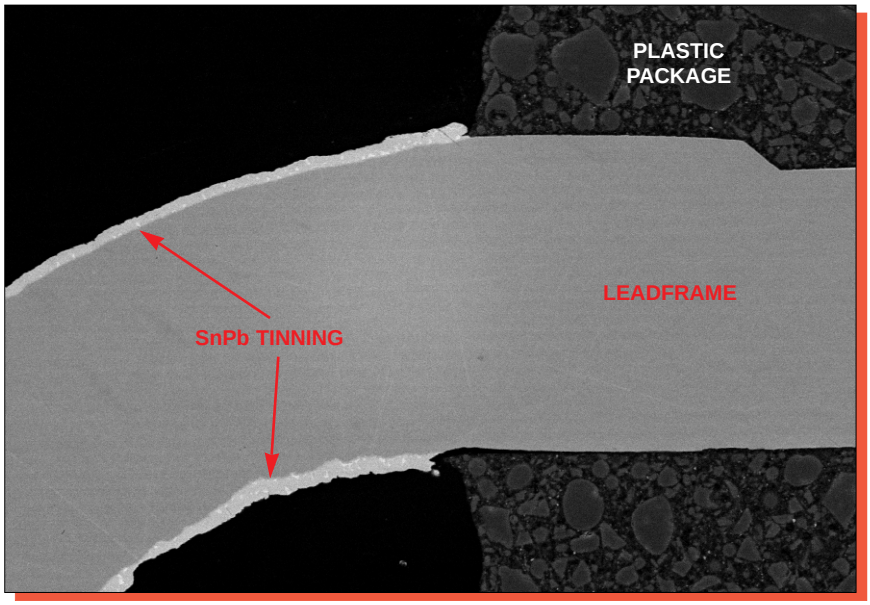


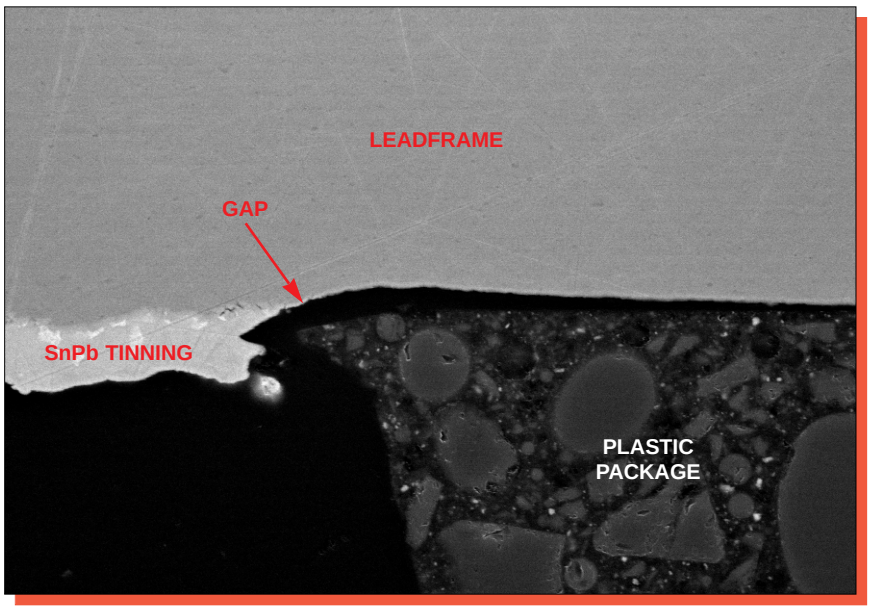

Figure 3. Optical section view of general package construction. Mag. 30x.




Mag. 50x

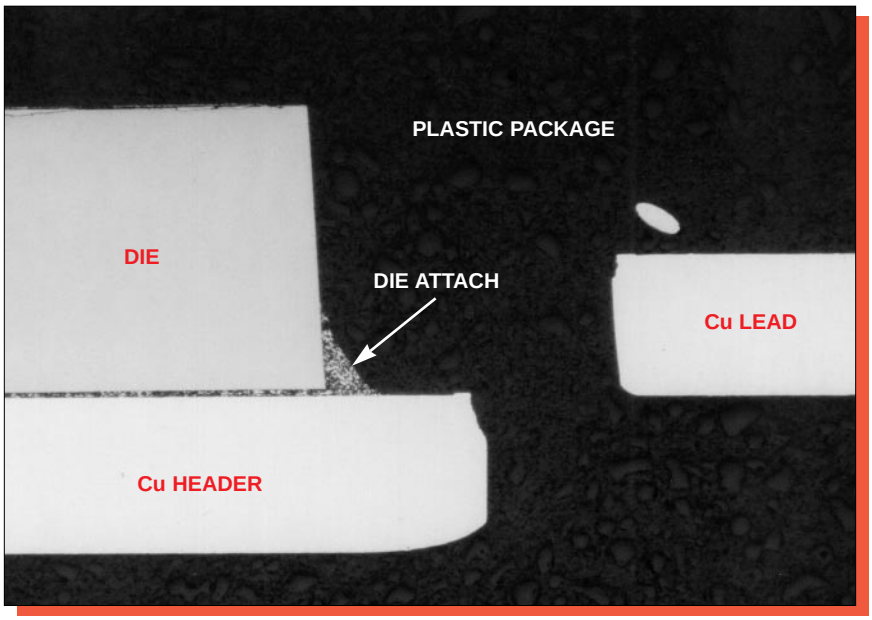



Mag. 200x

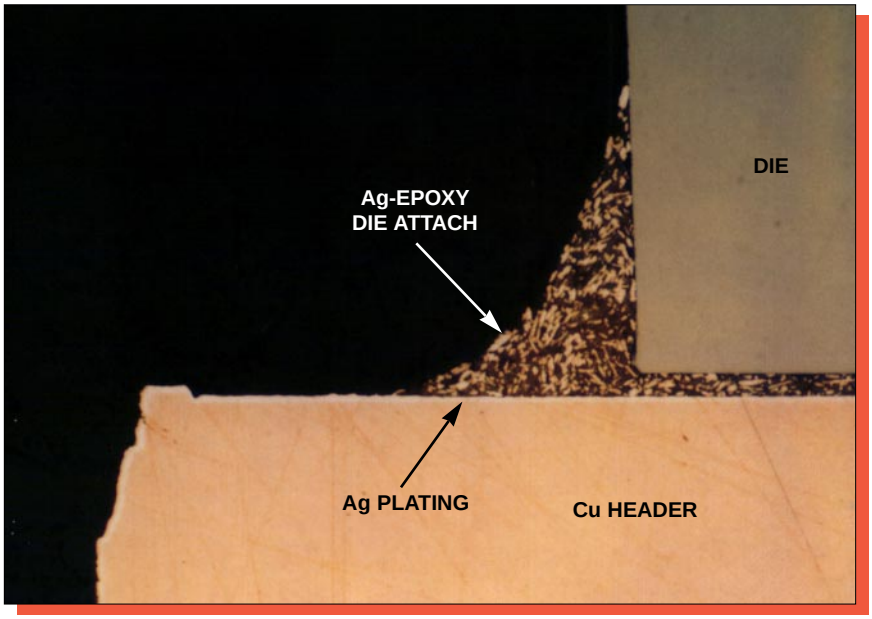



Mag. 800x

Figure 4. Section views illustrating lead formation and lead exit.

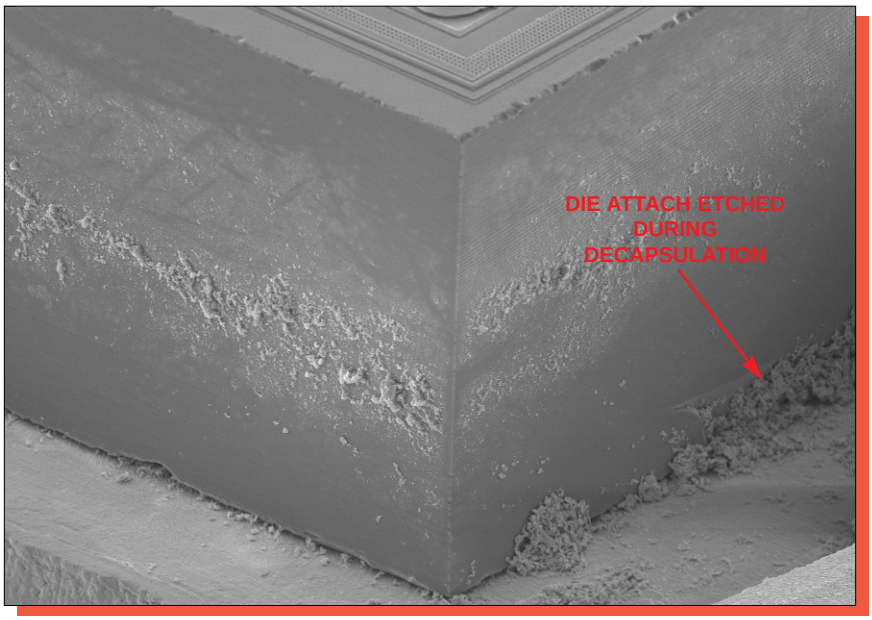



Mag. 100x

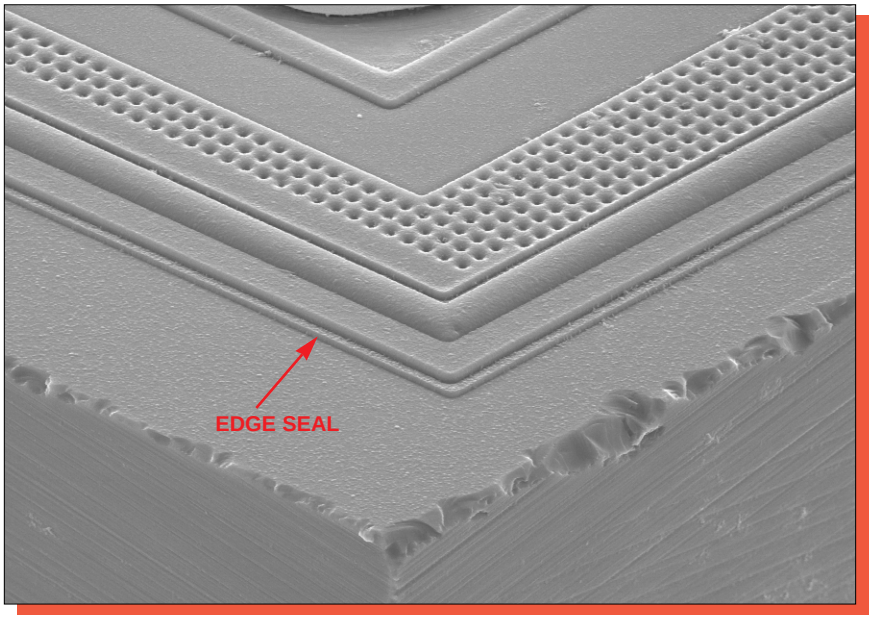



Mag. 400x

Figure 5. Section views illustrating general construction.

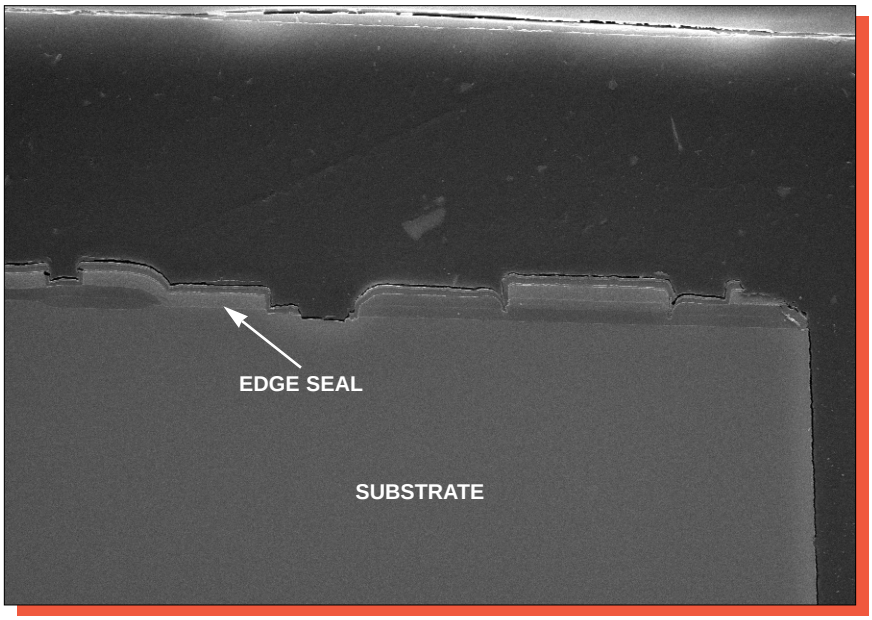



Mag. 190x

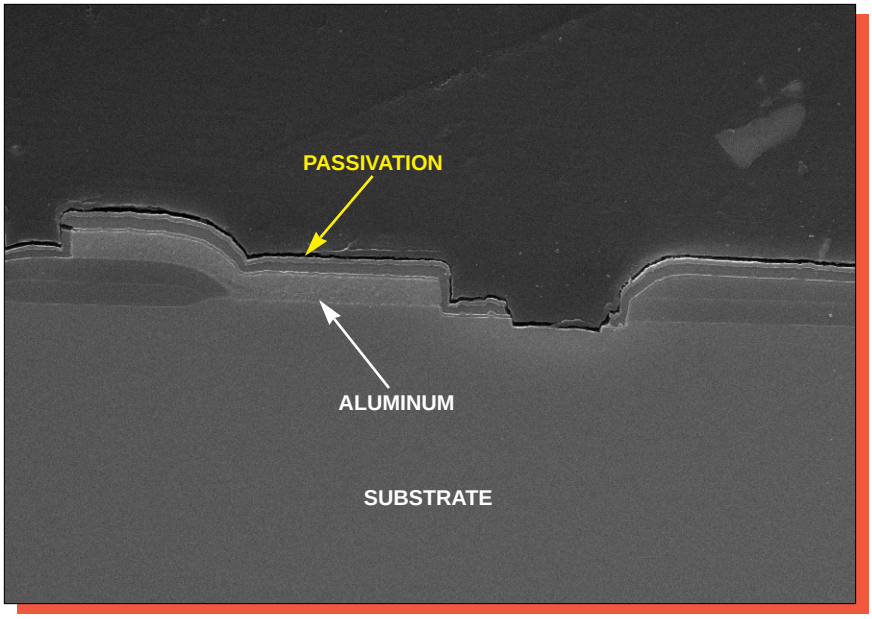



Mag. 810x

Figure 6. SEM views illustrating dicing and edge seal. 60°




Mag. 1600x




Mag. 3250x

Figure 7. SEM section views of edge seal.

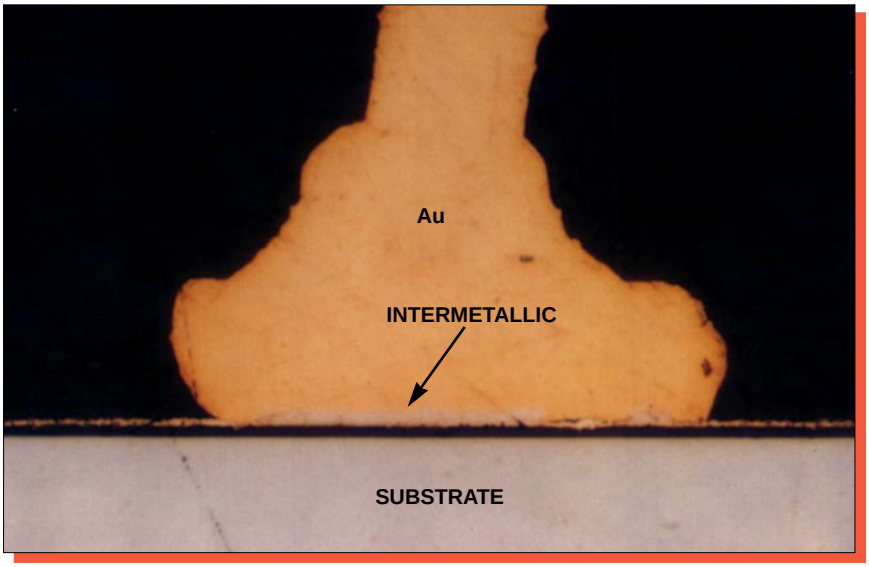



Figure 8. Optical section view of a ball bond. Mag 800x.

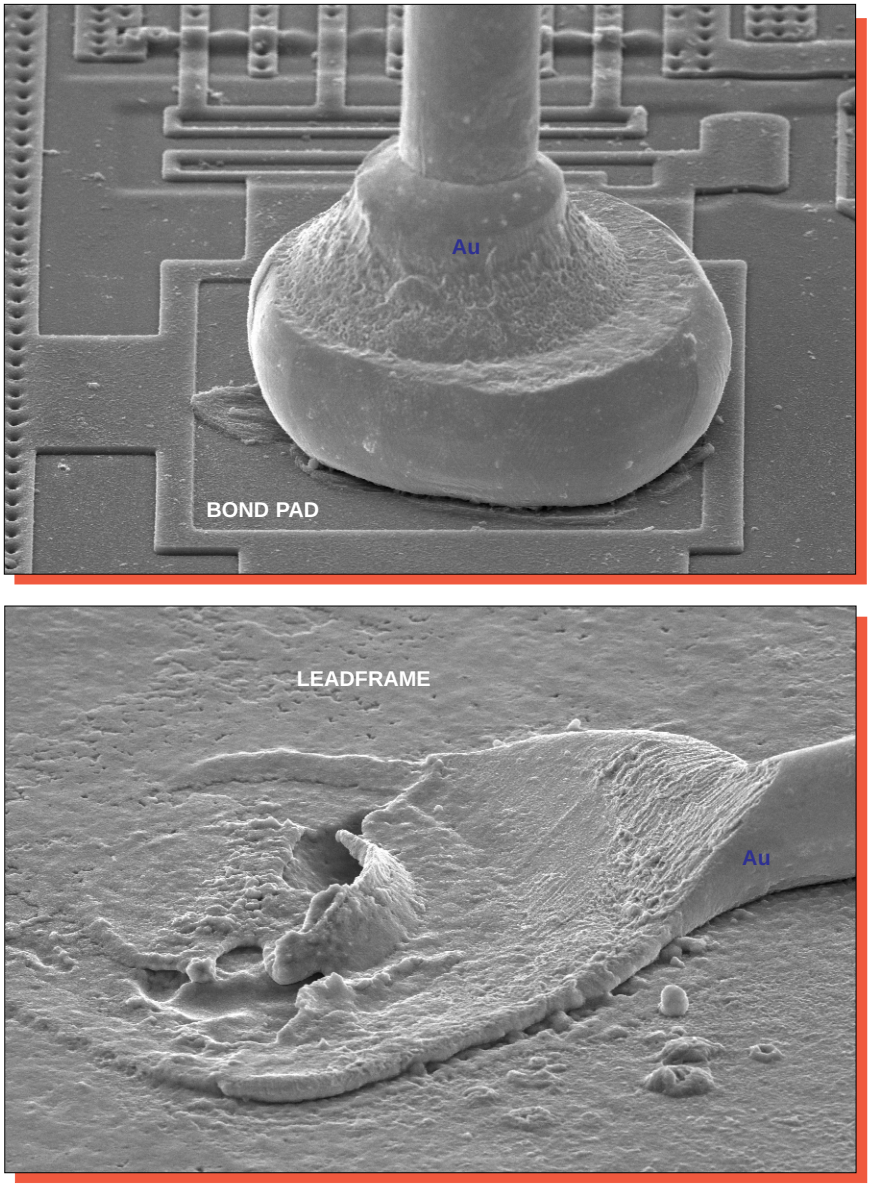



Figure 9. SEM views of typical wirebonds. Mag. 700x, 60°.

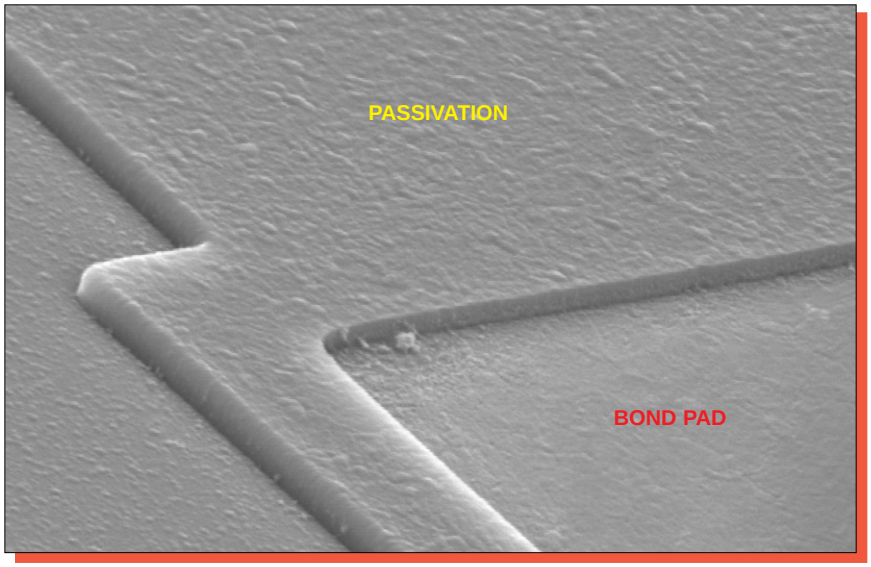
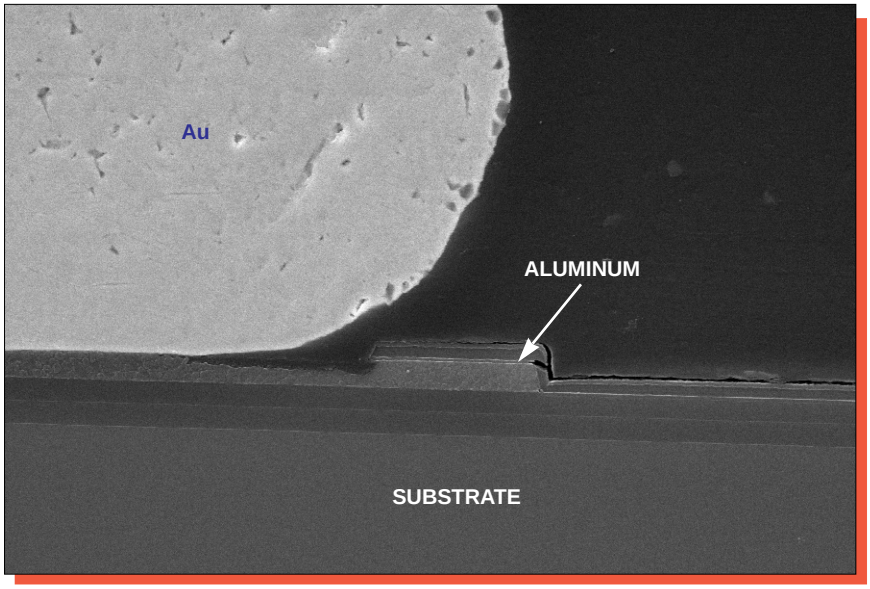
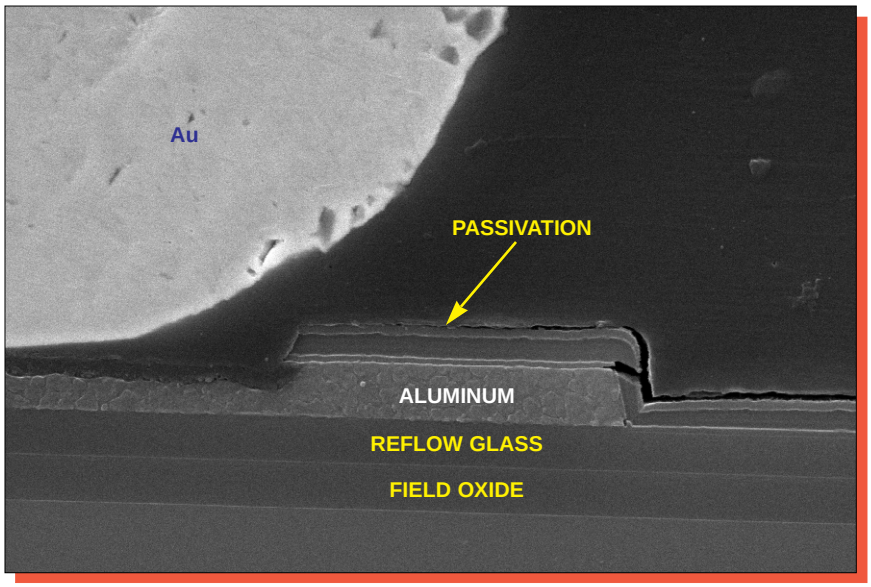



Figure 10. SEM view of a bond pad. Mag. 3000x, 60°.




Mag. 3250x




Mag. 6500x

Figure 11. SEM section views illustrating a bond pad.

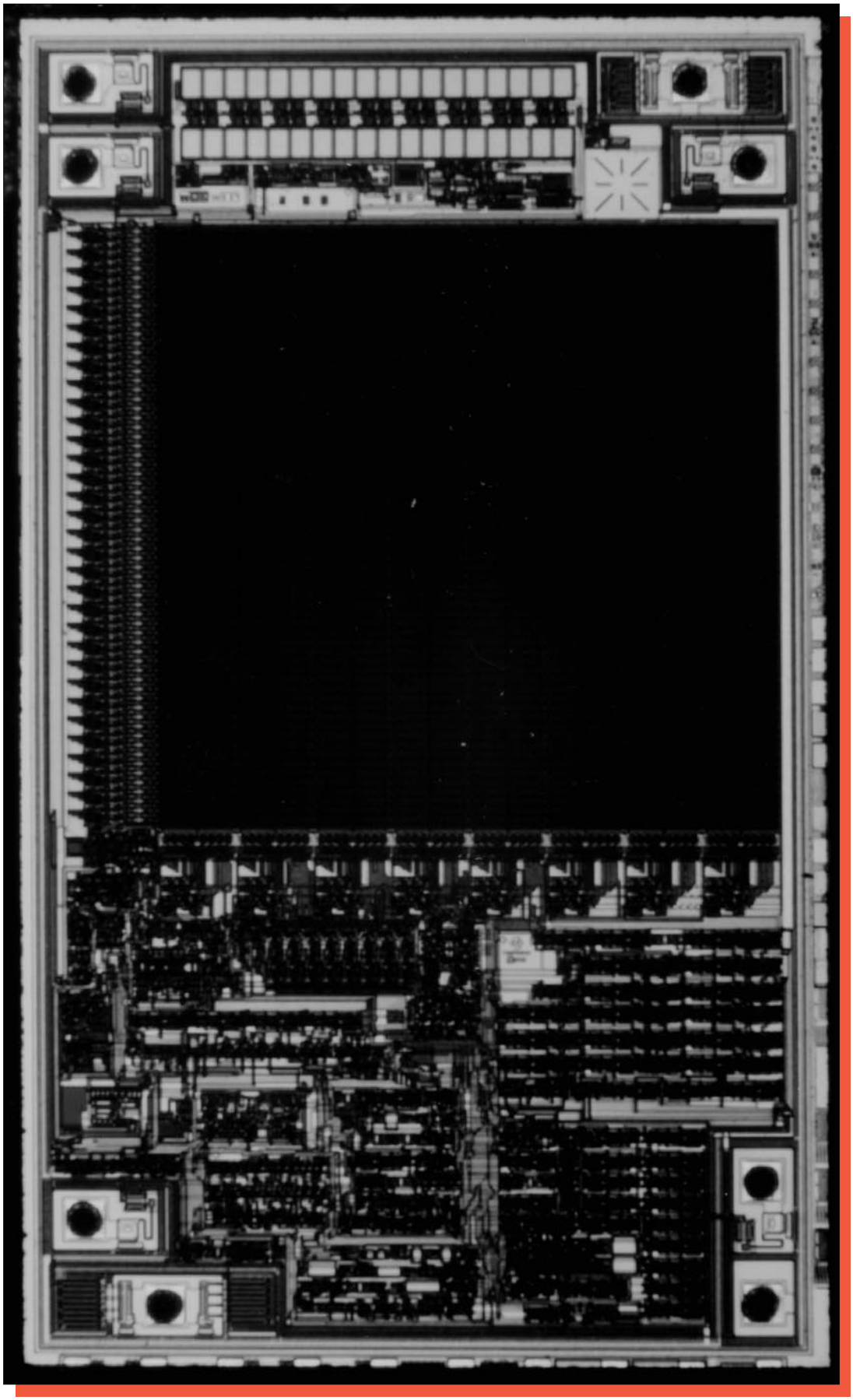
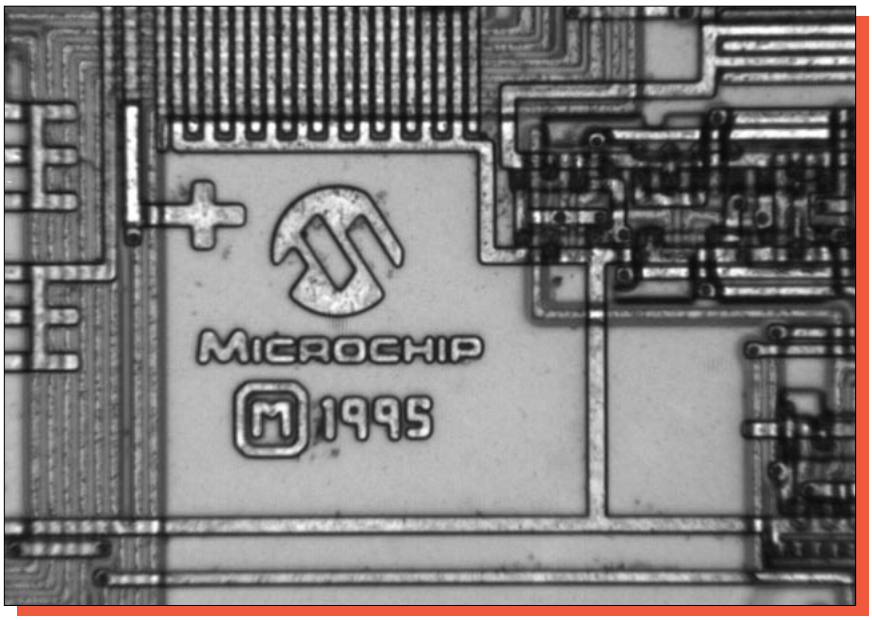
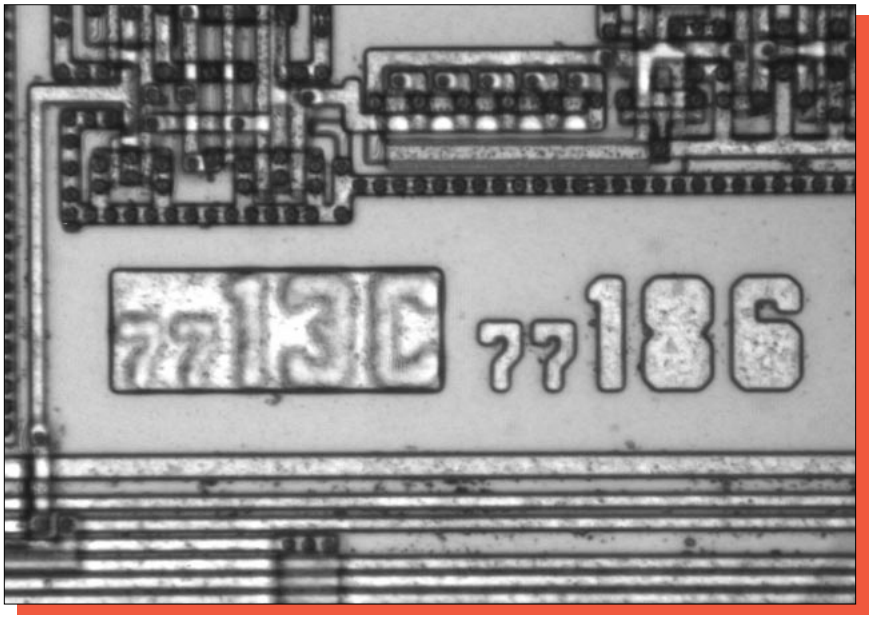


Figure 12. Whole die photograph of the Microchip 93LC86 16K Serial EEPROM. Mag. 64x.

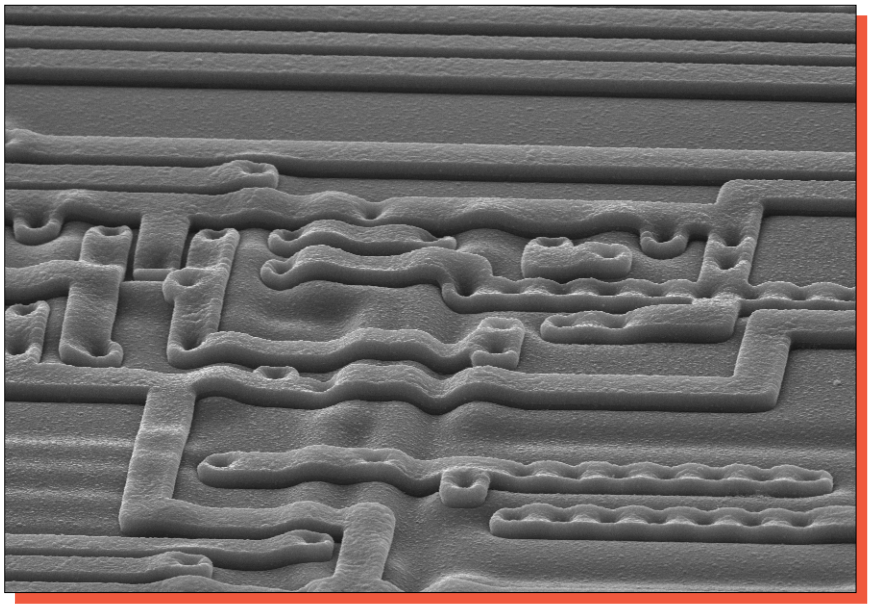



Mag. 600x

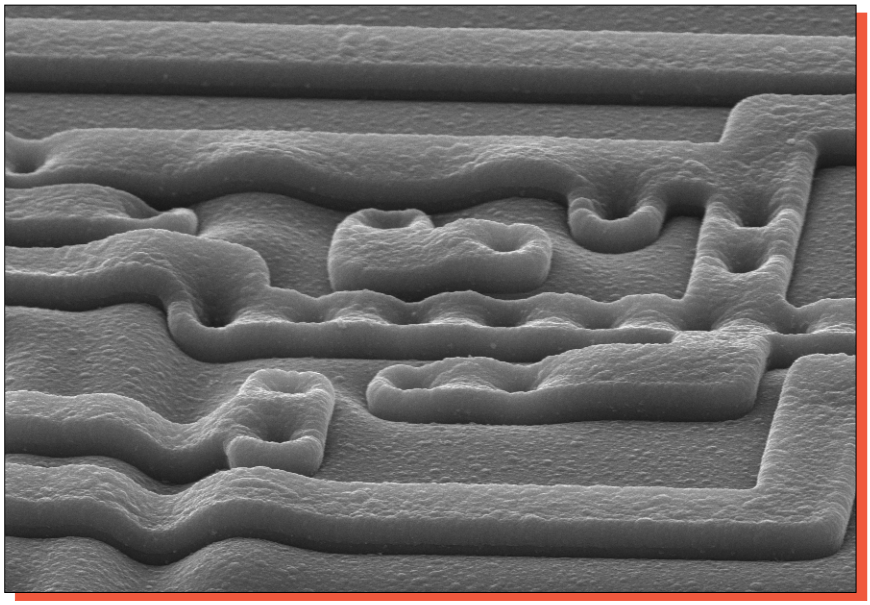



Mag. 700x

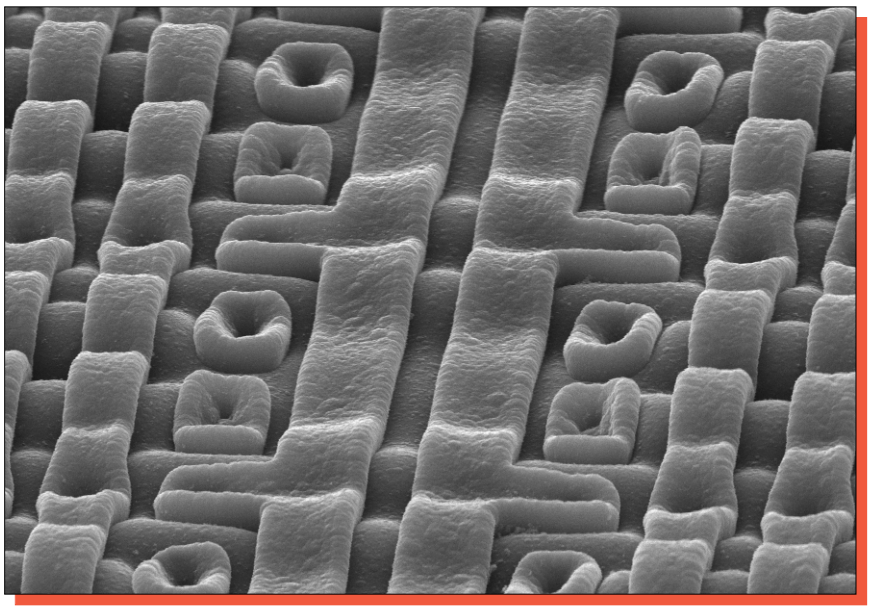
Figure 13. Optical views of die identification markings.



Mag. 1500x

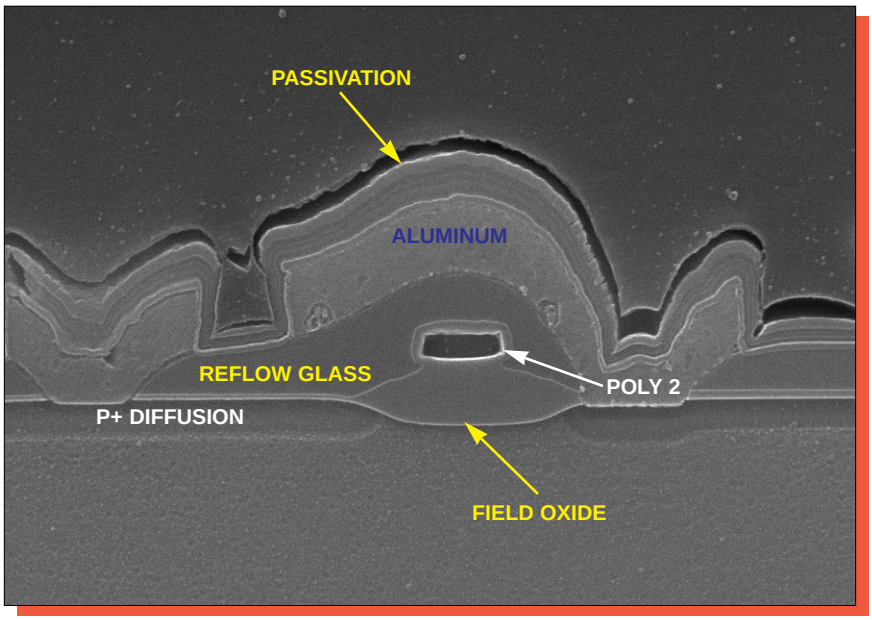


Mag. 3000x

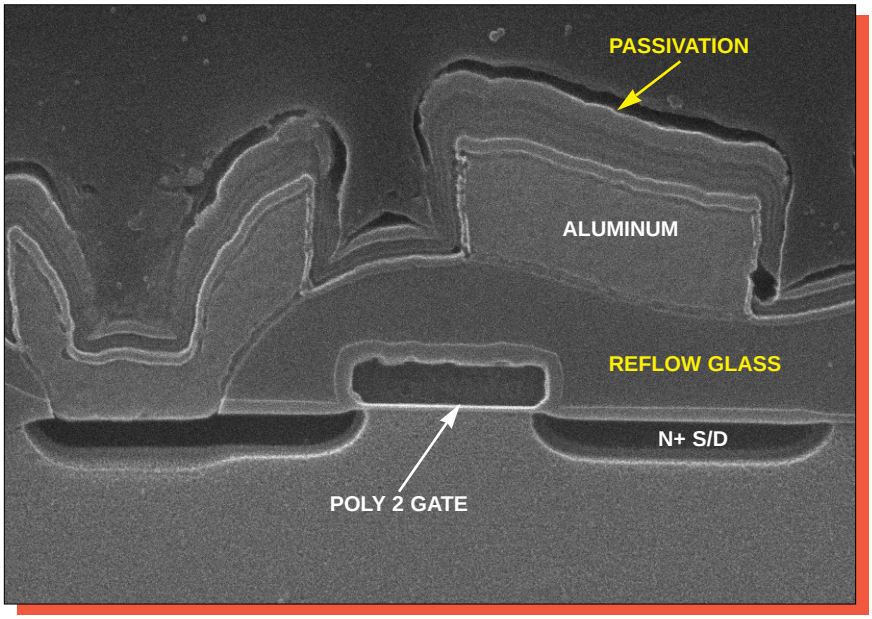


Mag. 3000x

Figure 14. SEM views of passivation. 60°.

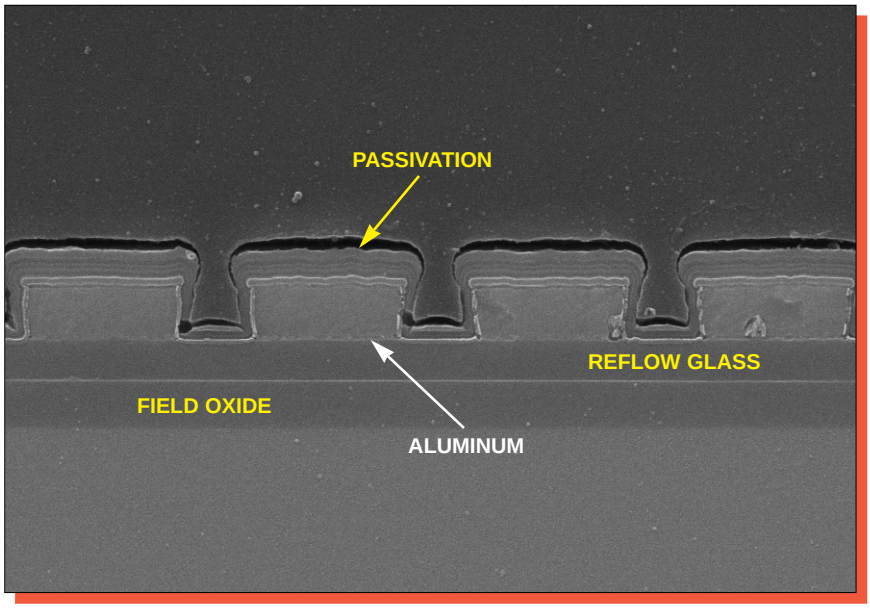



Mag. 8500x

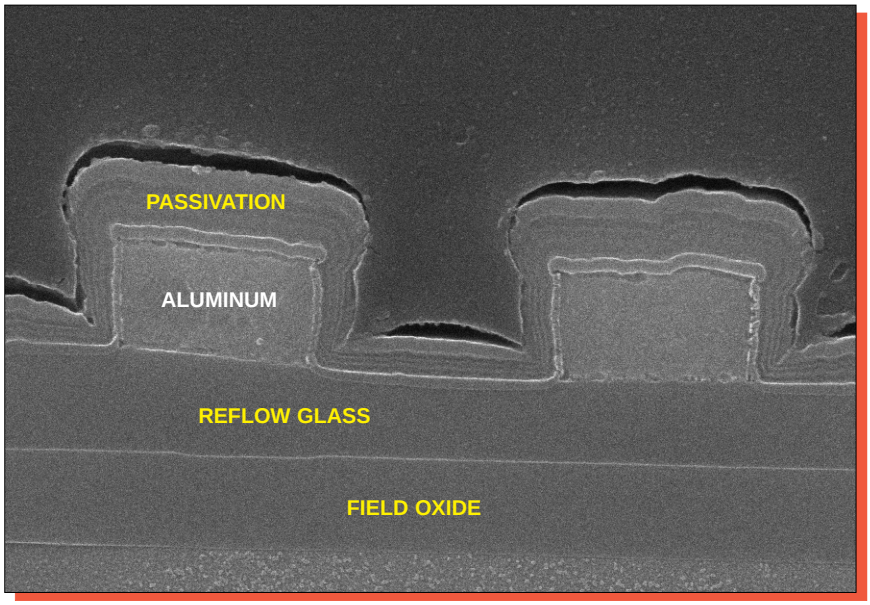



Mag. 13,000x

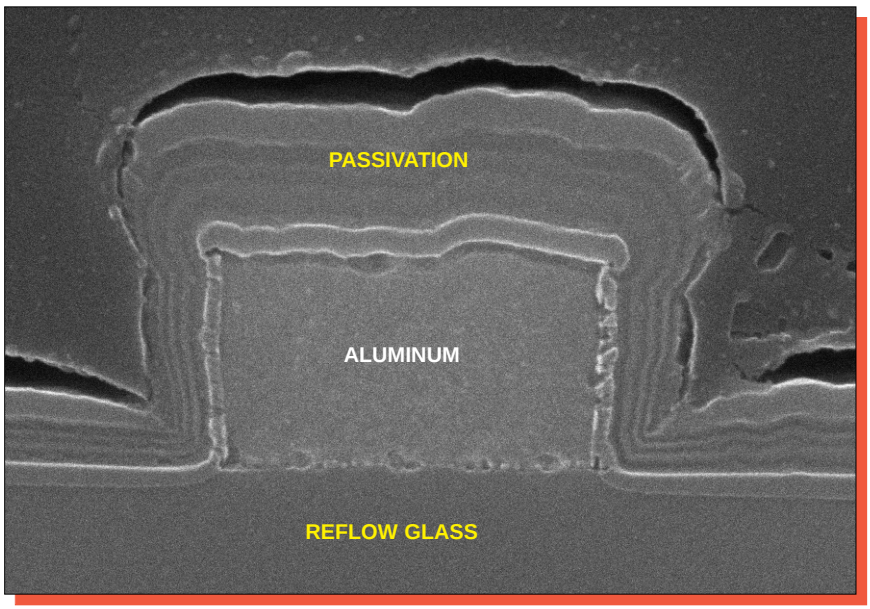
Figure 15. SEM section views illustrating general structure.




Mag. 6500x




Mag. 13,000x




Mag. 26,000x

Figure 16. SEM section views of metal line profiles.

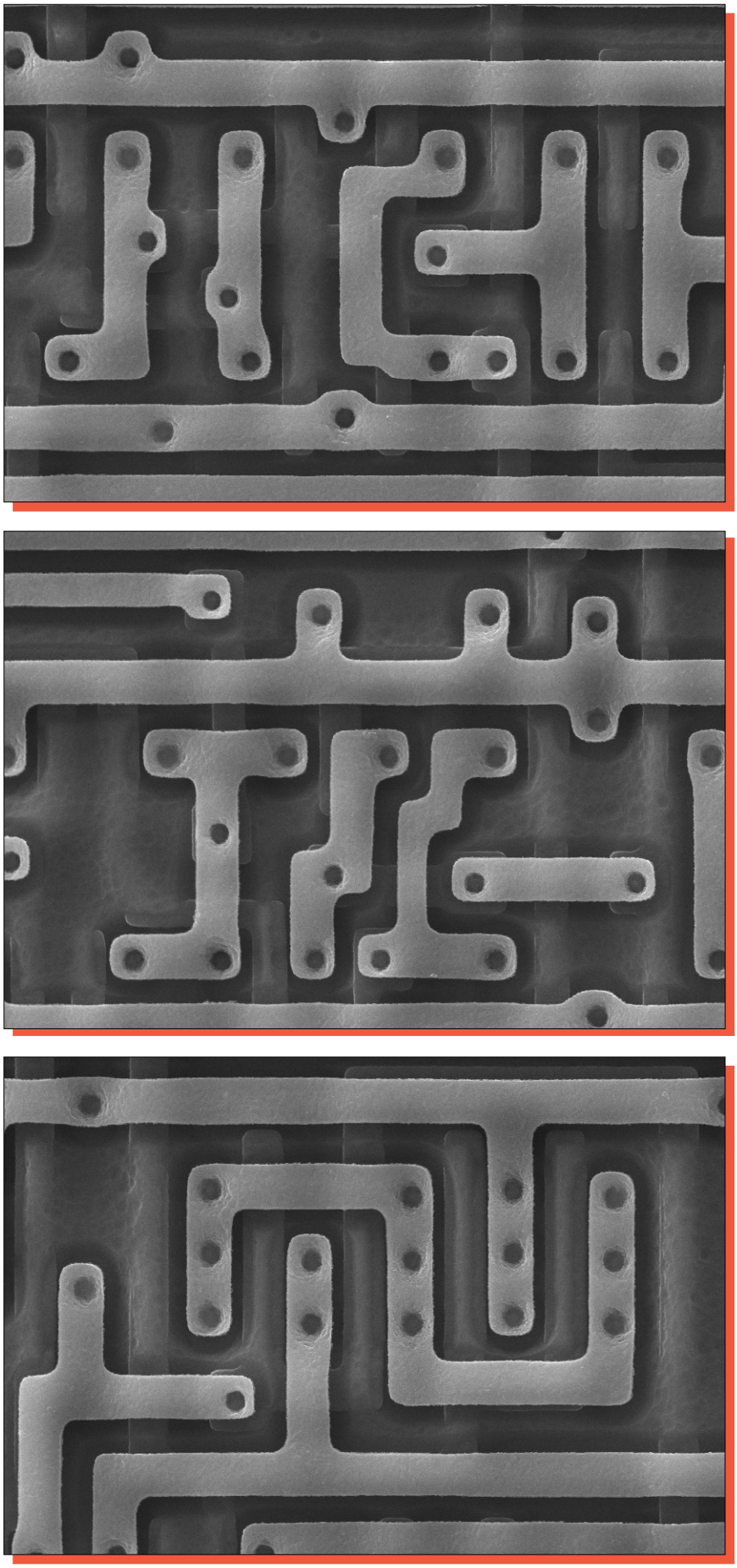
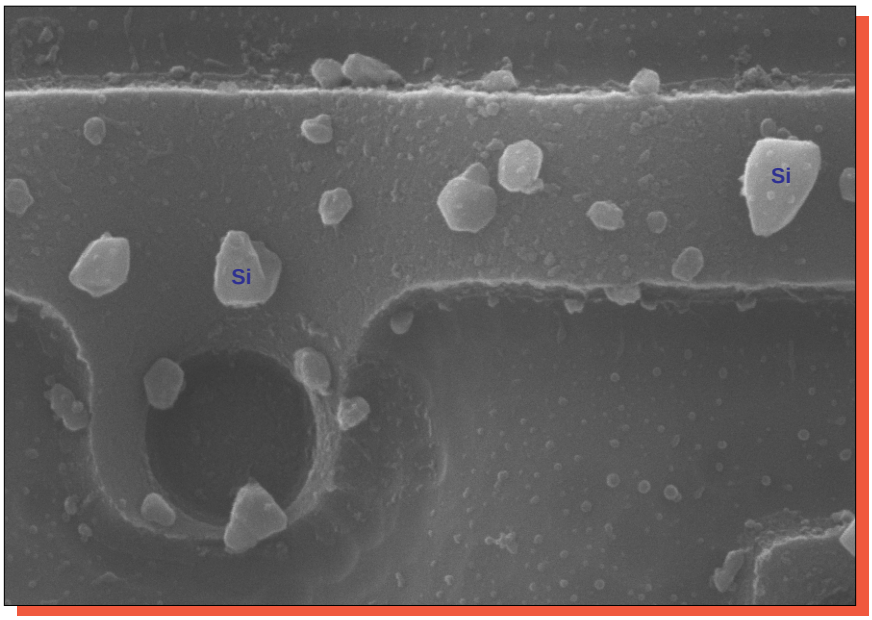
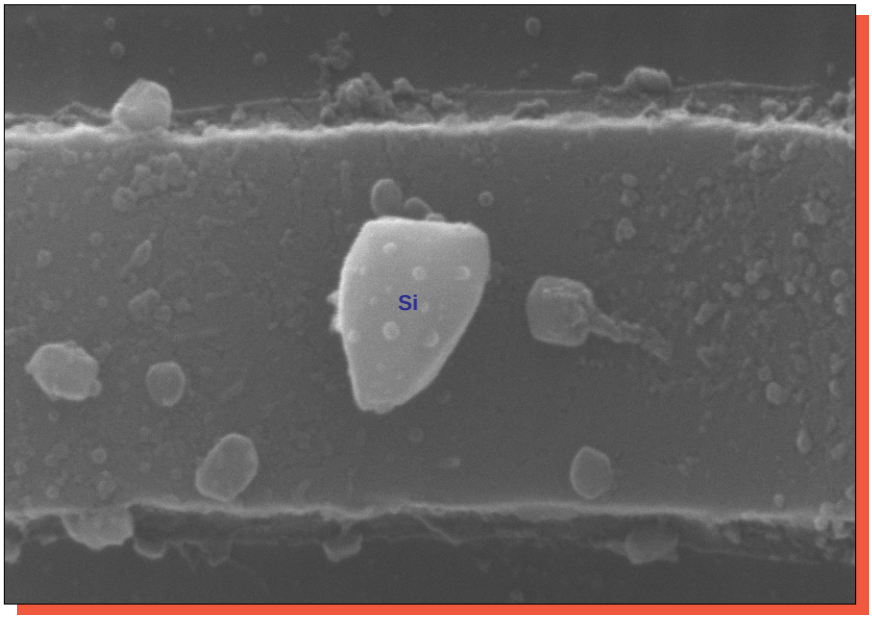


Figure 17. Topological SEM views of metal patterning. Mag. 24,000x, 0°.

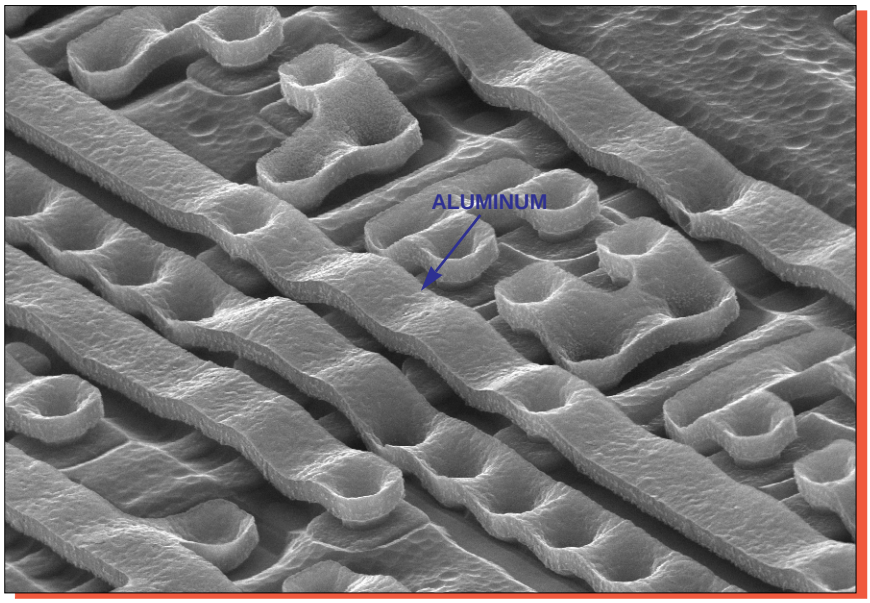



Mag. 12,500x

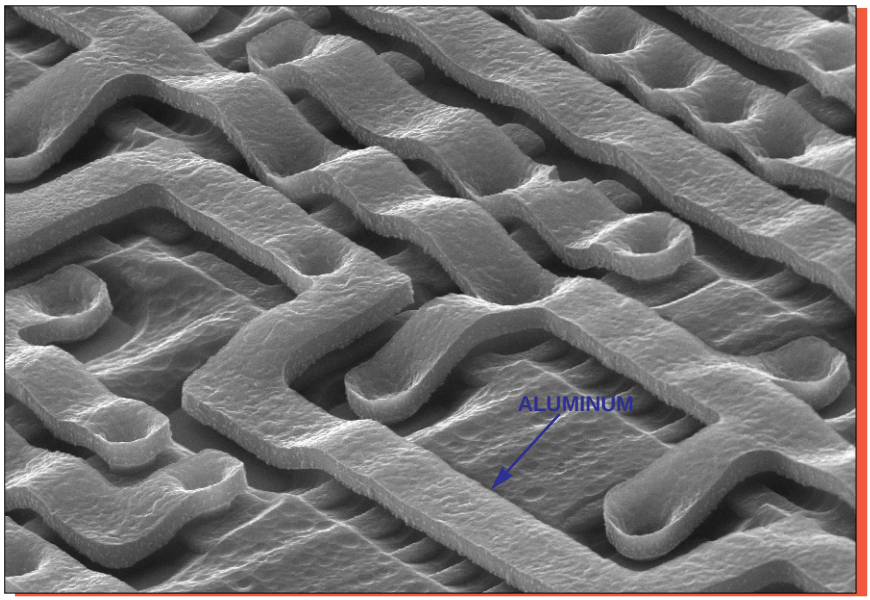



Mag. 25,000x

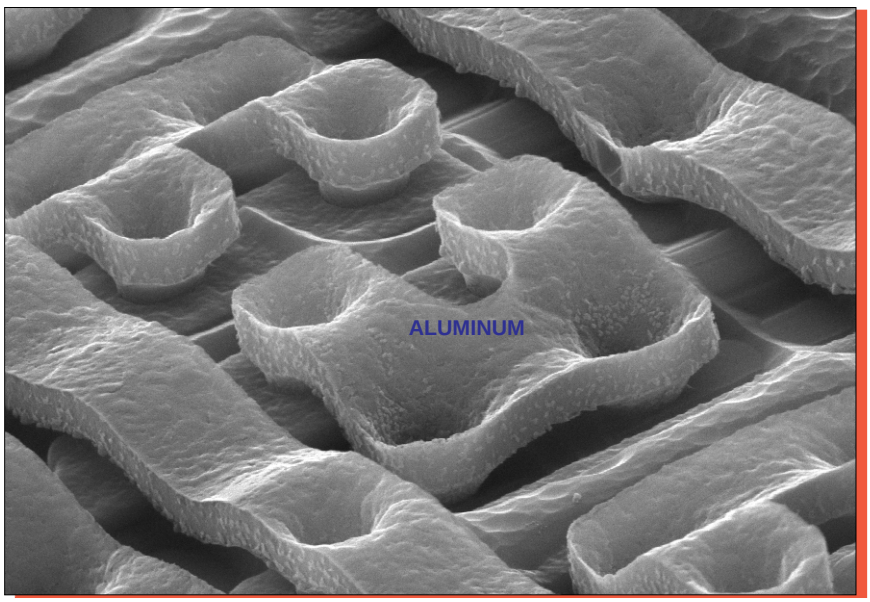
Figure 18. Topological SEM views of silicon nodules. 0°.




Mag. 3250x




Mag. 3250x




Mag. 6500x

Figure 19. SEM views of metal step coverage. 60°.

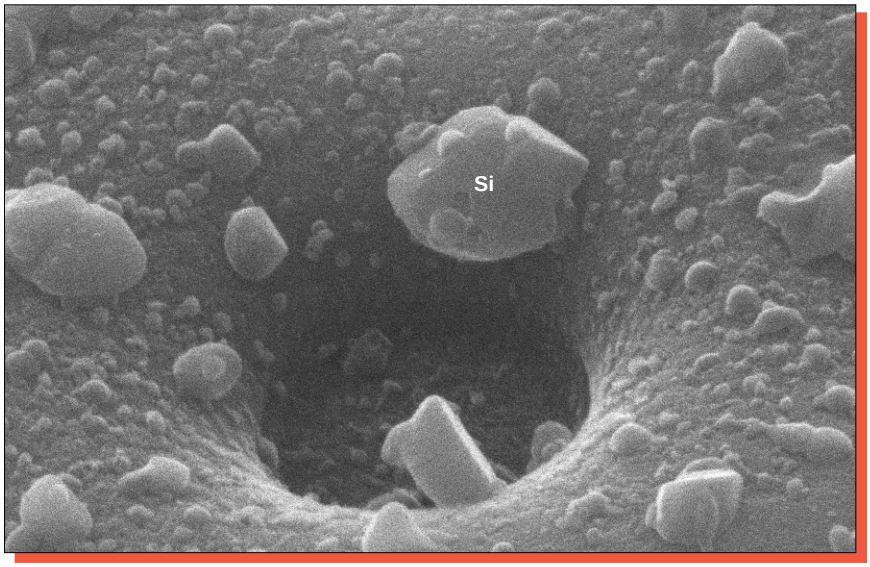
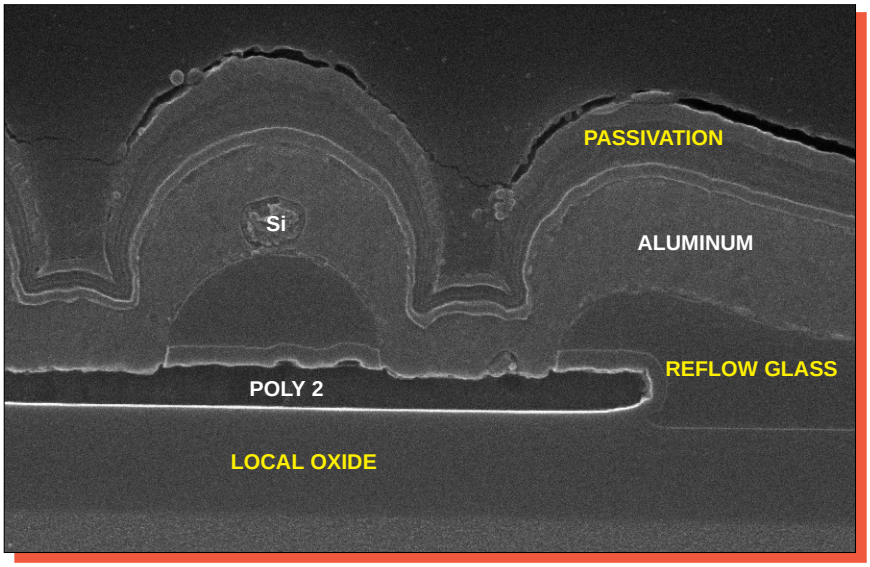
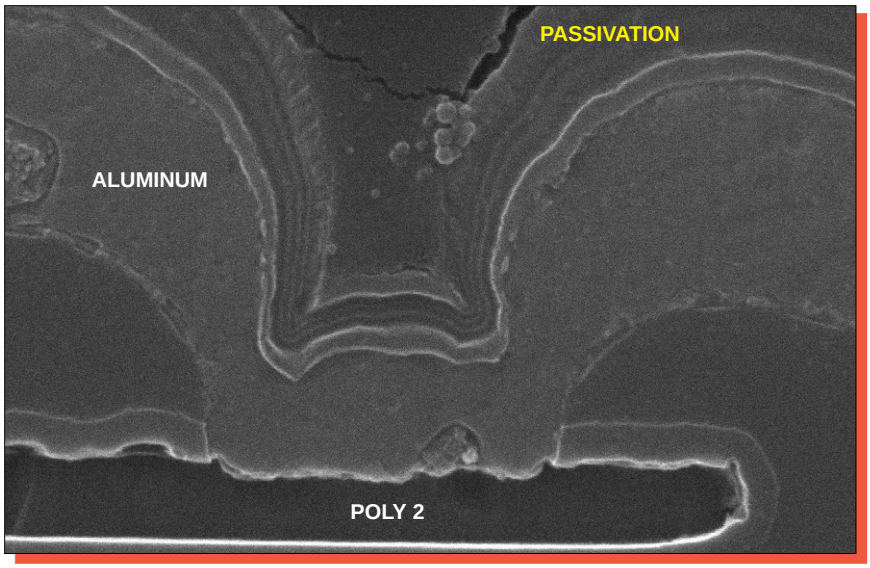



Figure 20. SEM view illustrating a contact cut. Mag. 24,000x.

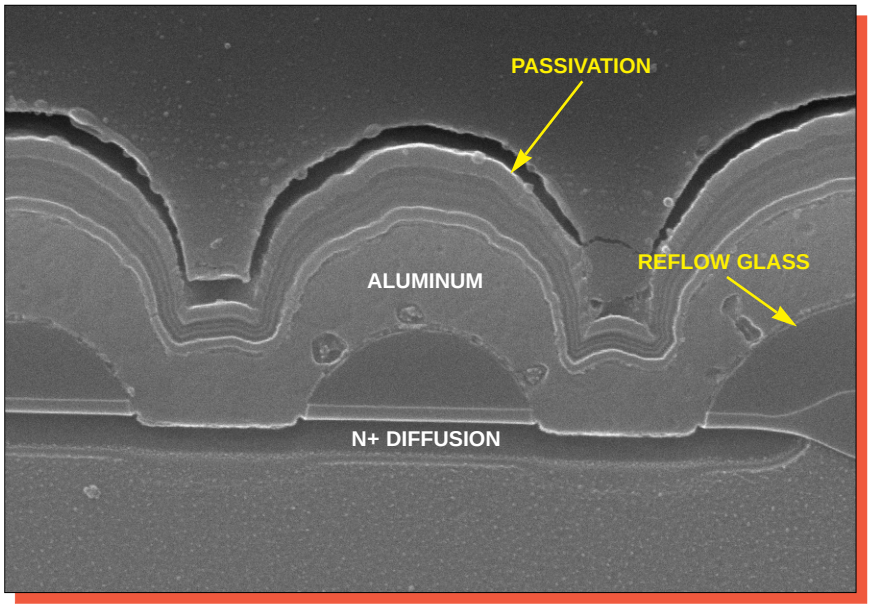



Mag. 13,000x.

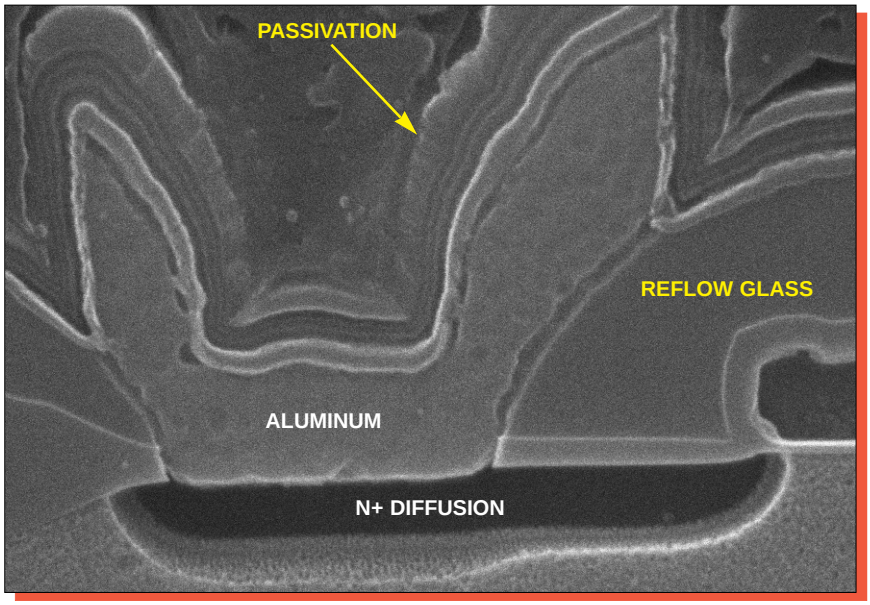



Mag. 26,000x.

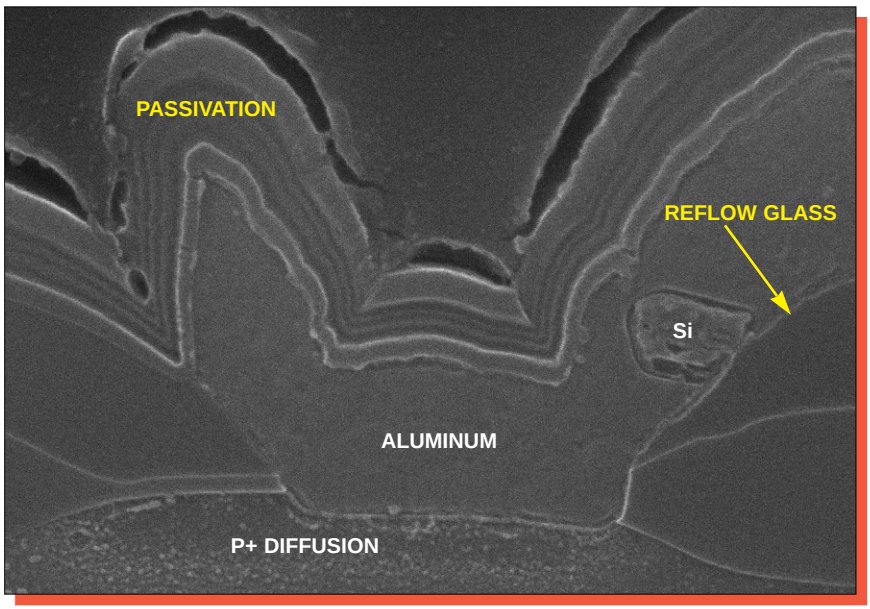
Figure 21. SEM section views illustrating a metal-to-poly 2 contact.




N+ diffusion,
Mag. 13,000x

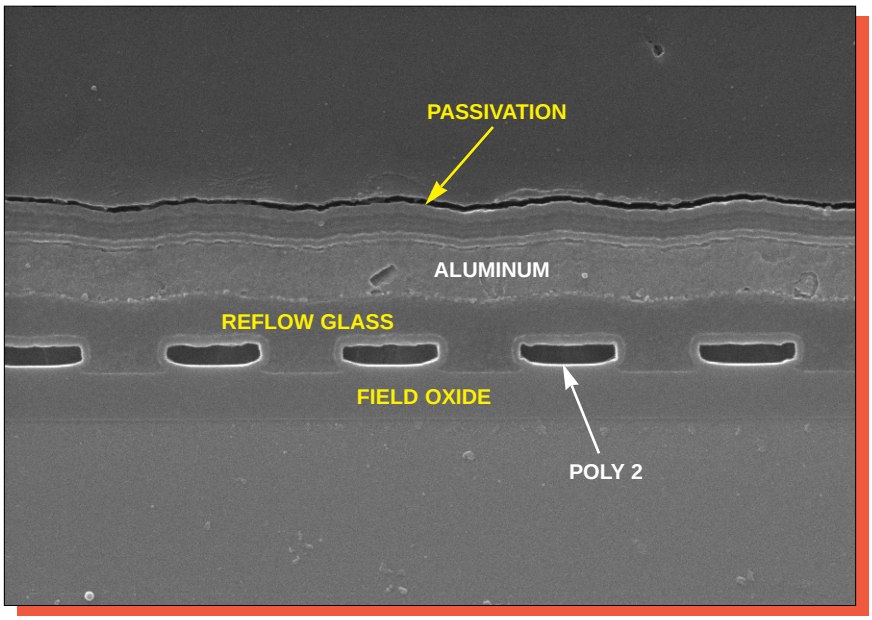



N+ diffusion,
Mag. 26,000x

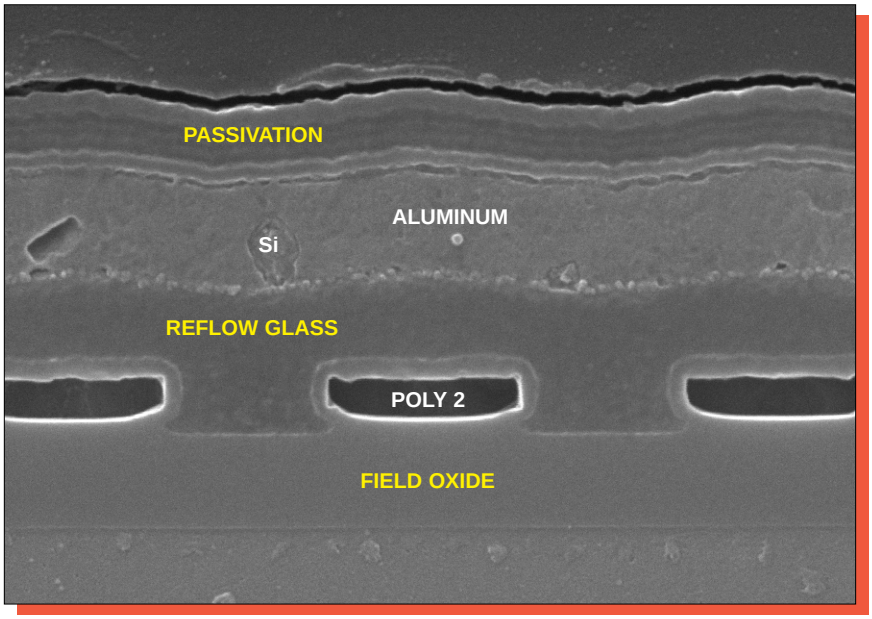



P+ diffusion,
Mag. 26,000x

Figure 22. SEM section views illustrating metal-to-diffusion contacts.

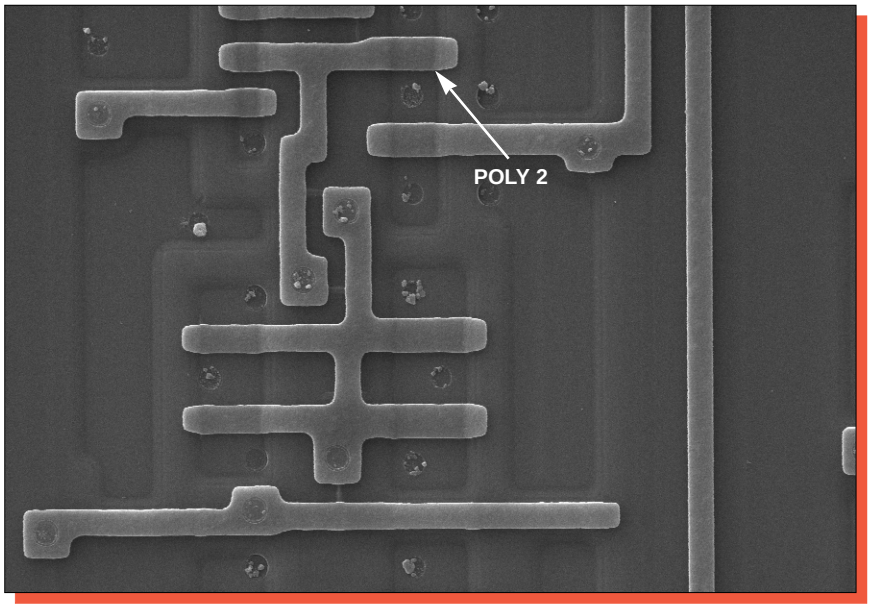



Mag. 6500x

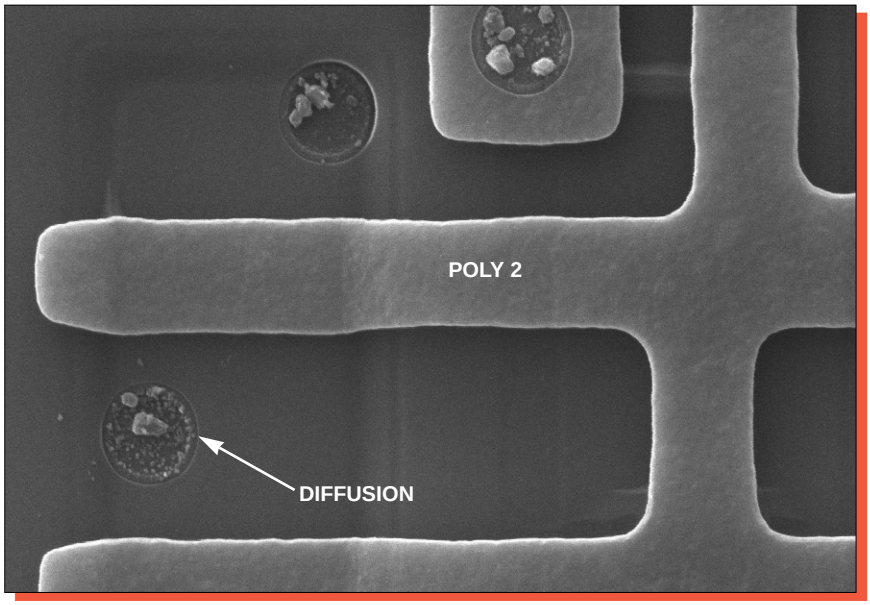



Mag. 13,000x

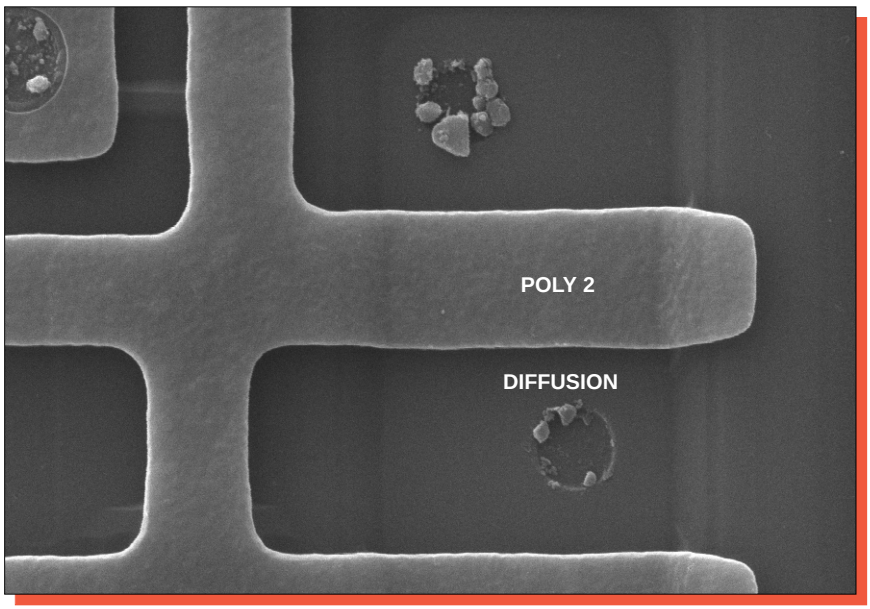
Figure 23. SEM section views illustrating poly 2 spacing.




Mag. 1600x

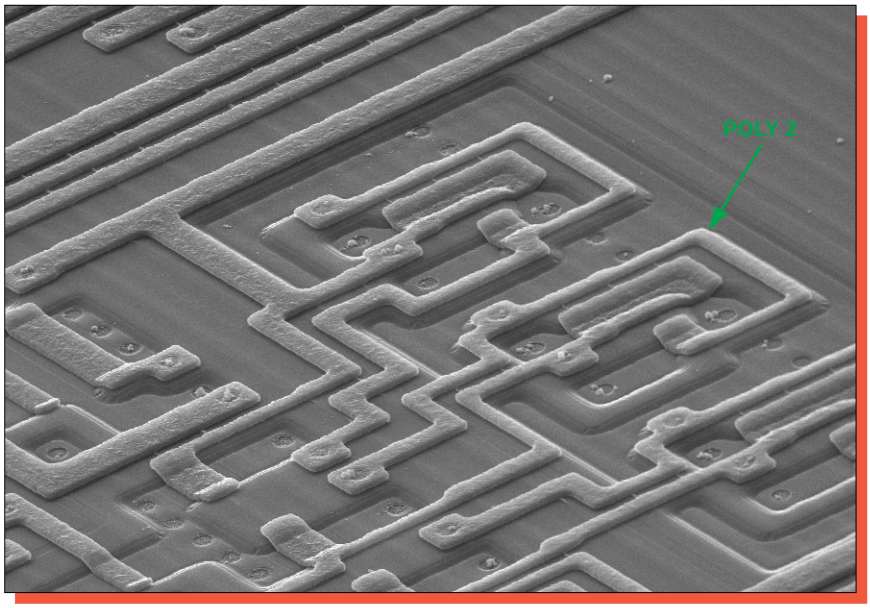



Mag. 6500x

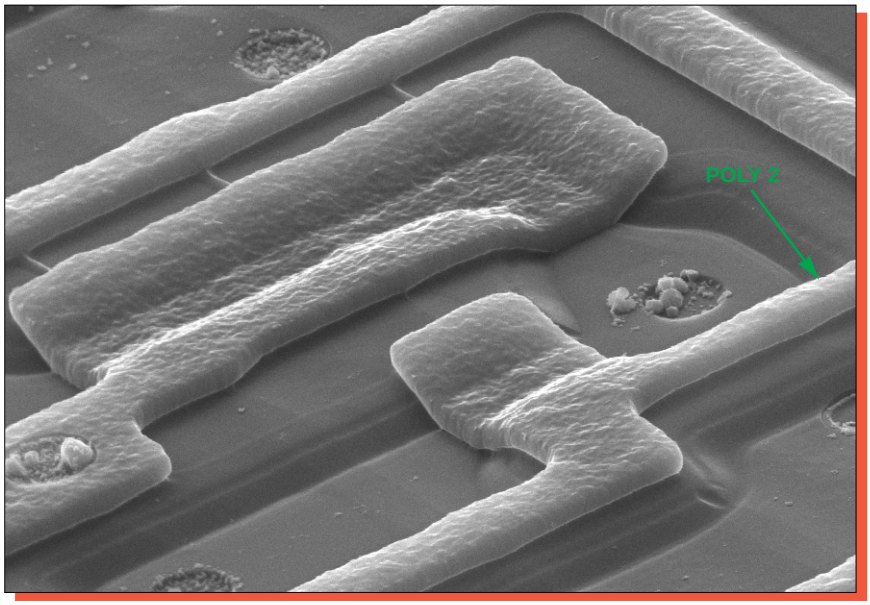



Mag. 6500x

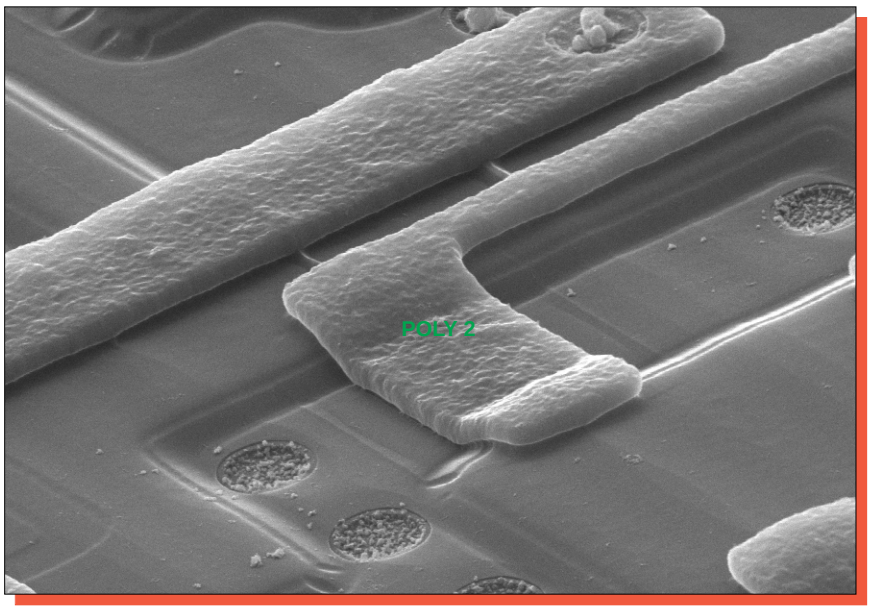
Figure 24. Topological SEM views illustrating poly 2 patterning. 0°.




Mag. 1600x

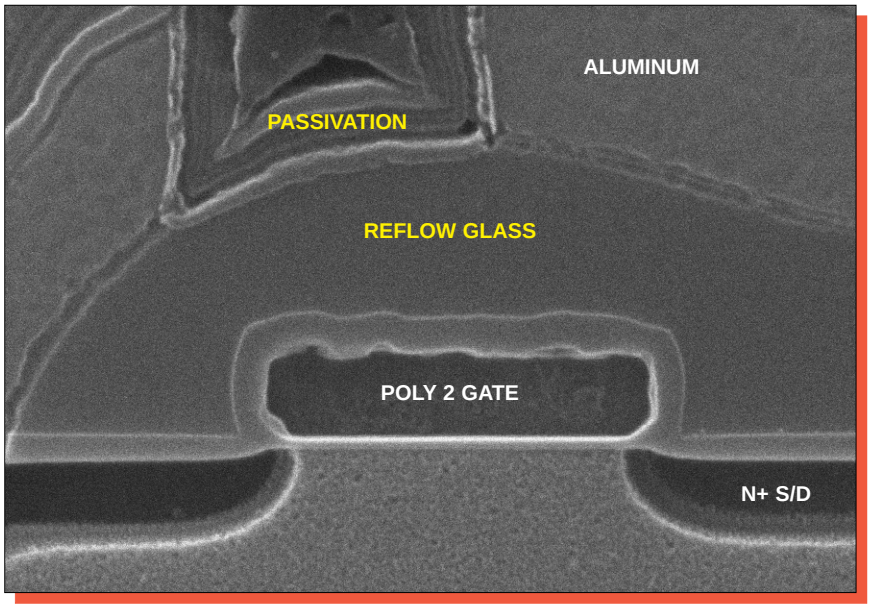



Mag. 6500x

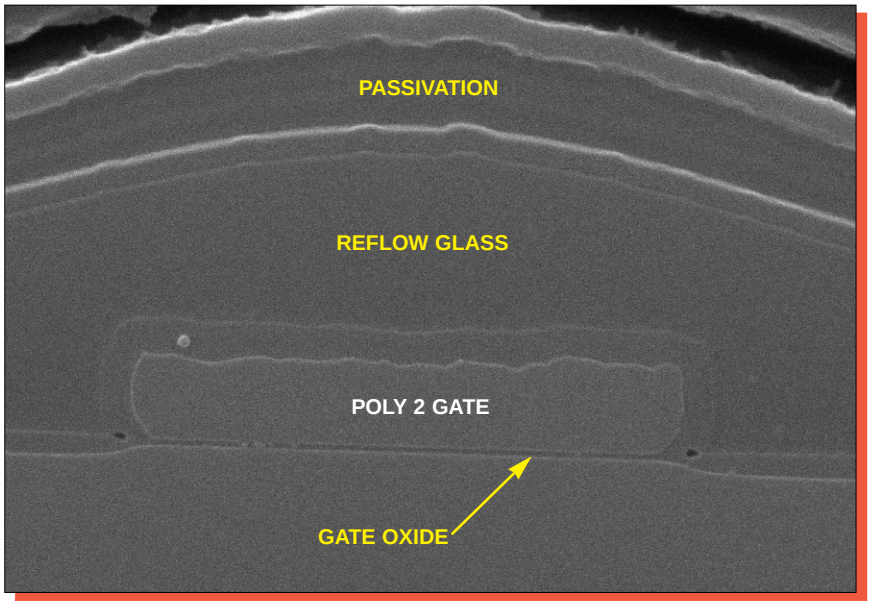



Mag. 6500x

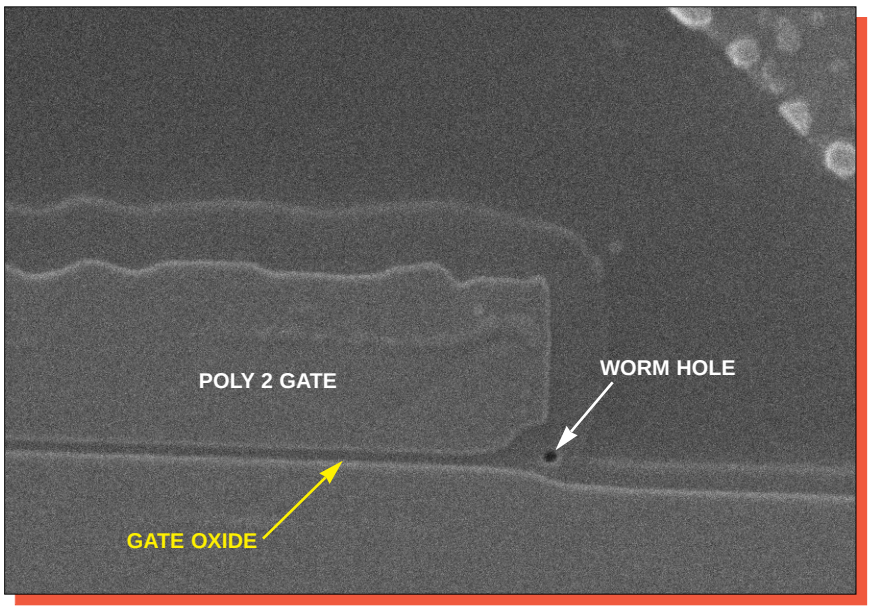
Figure 25. SEM views illustrating poly 2 step coverage. 60°.




Mag. 26,000x

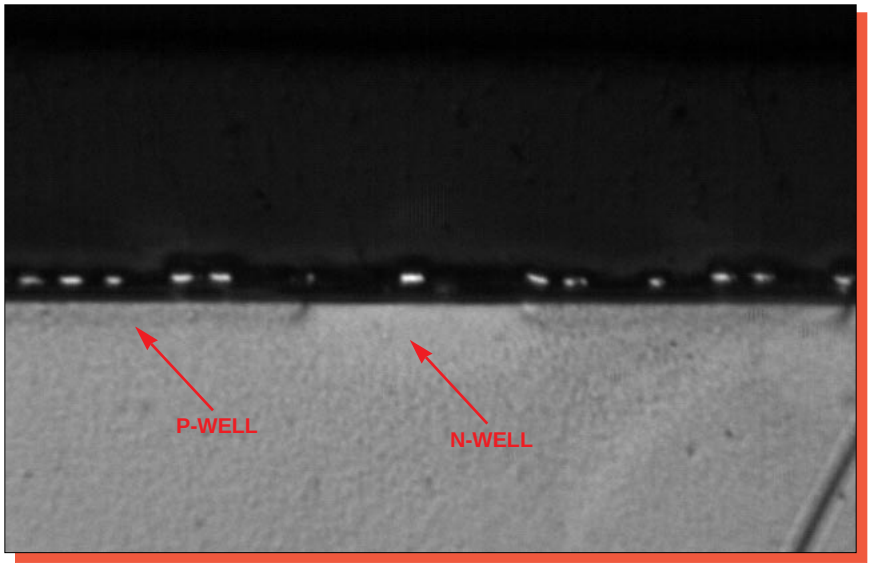



glass etch,
Mag. 26,000x

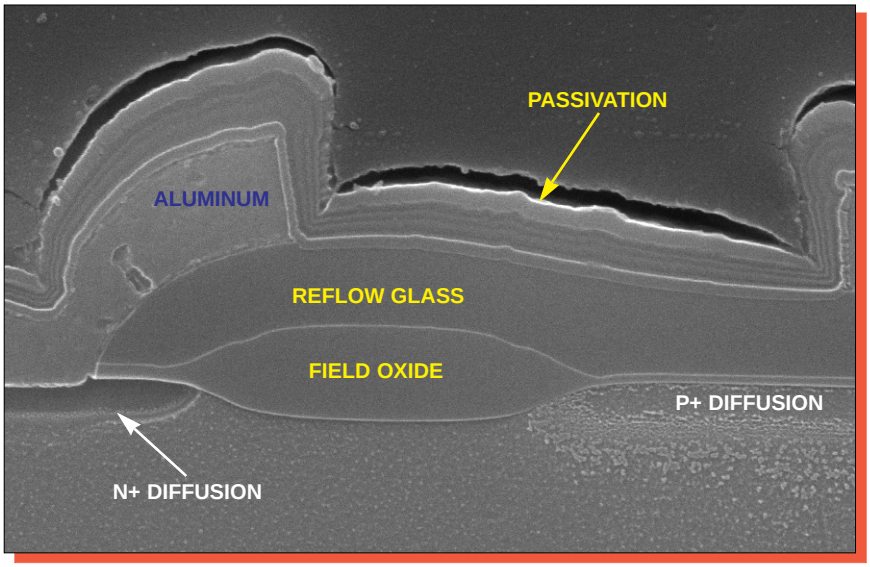



Mag. 52,000x

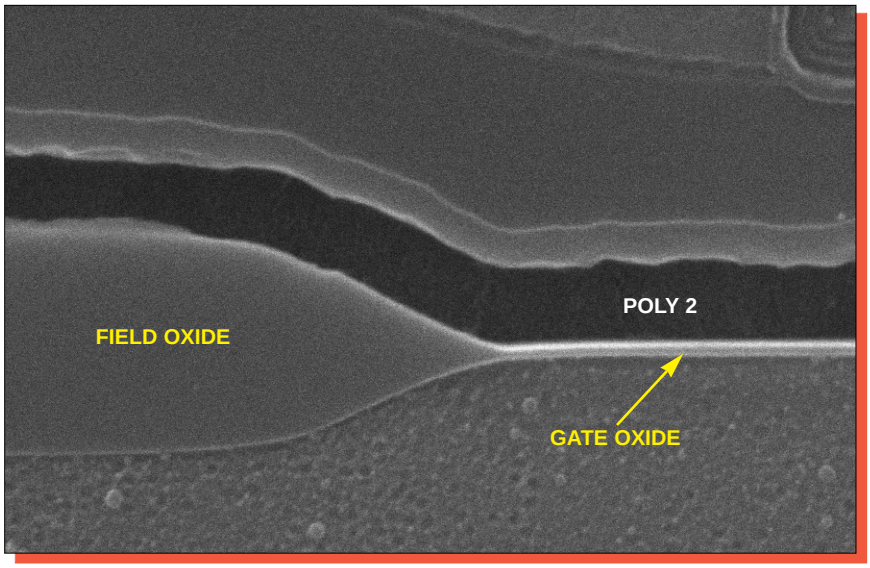
Figure 26. SEM section views illustrating typical gate structure.




Mag. 1200x

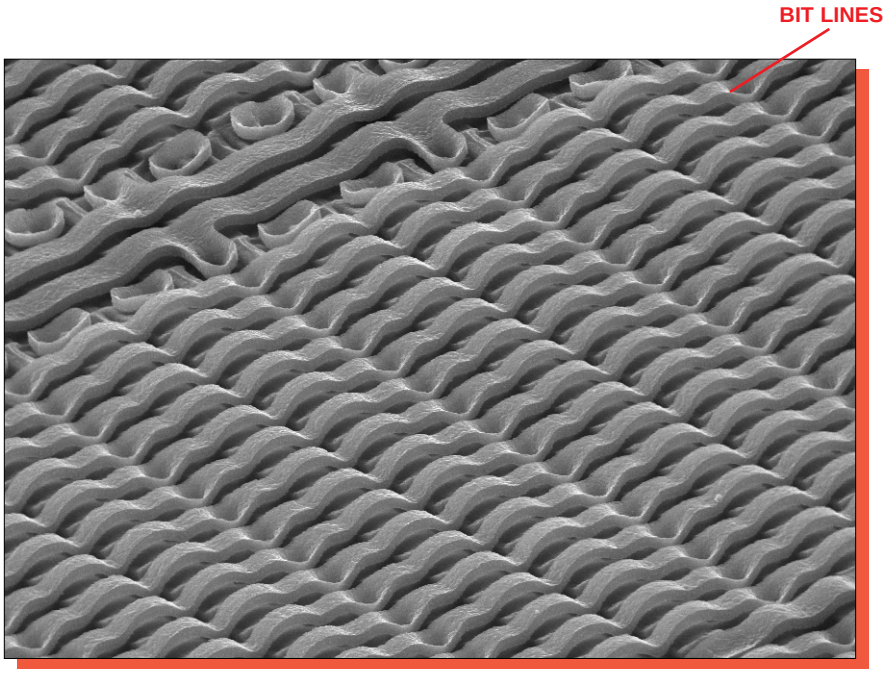



Mag. 13,000x

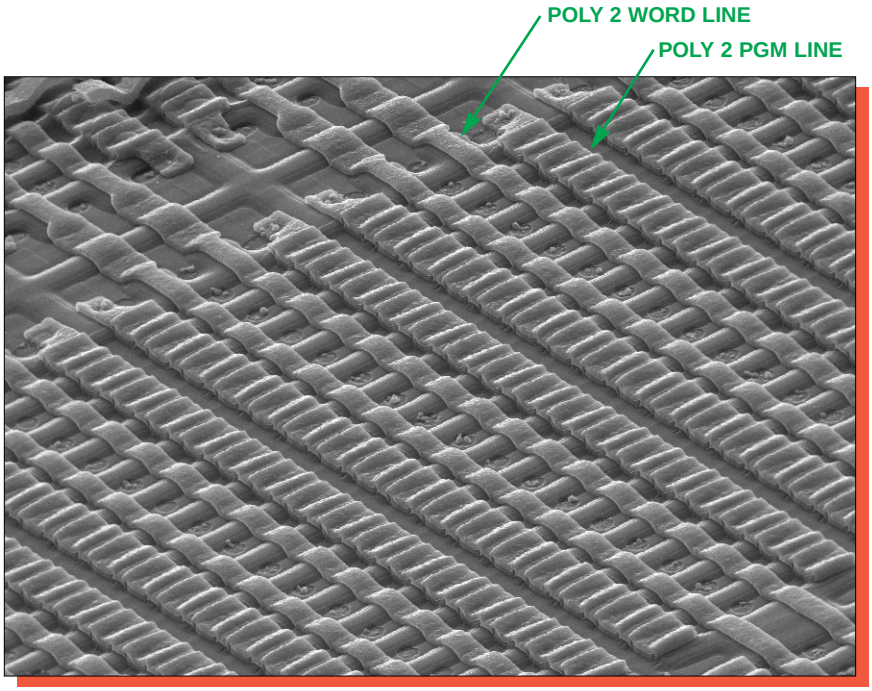



Mag. 26,000x

Figure 27. Section views illustrating well structure, field oxide isolation and a typical birdsbeak.

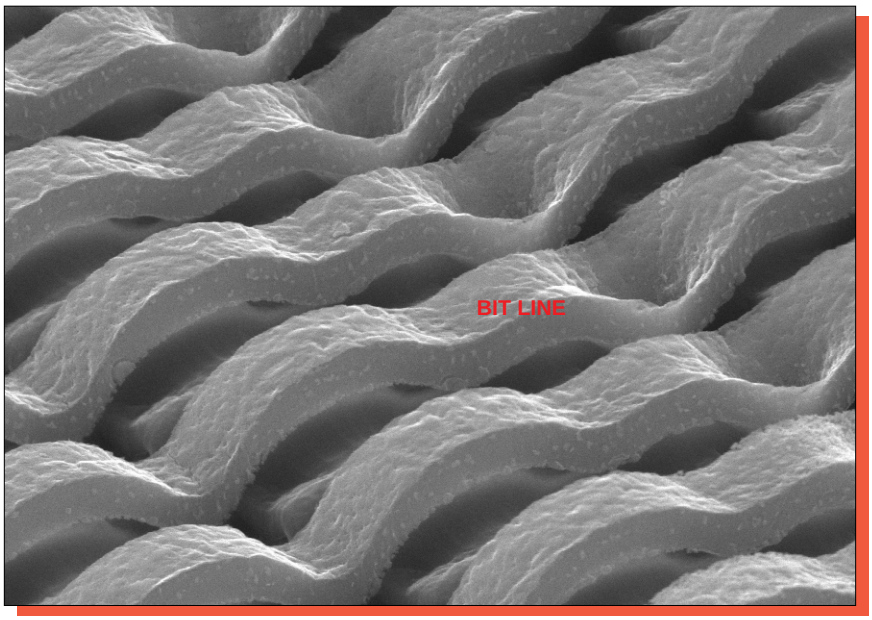



aluminum

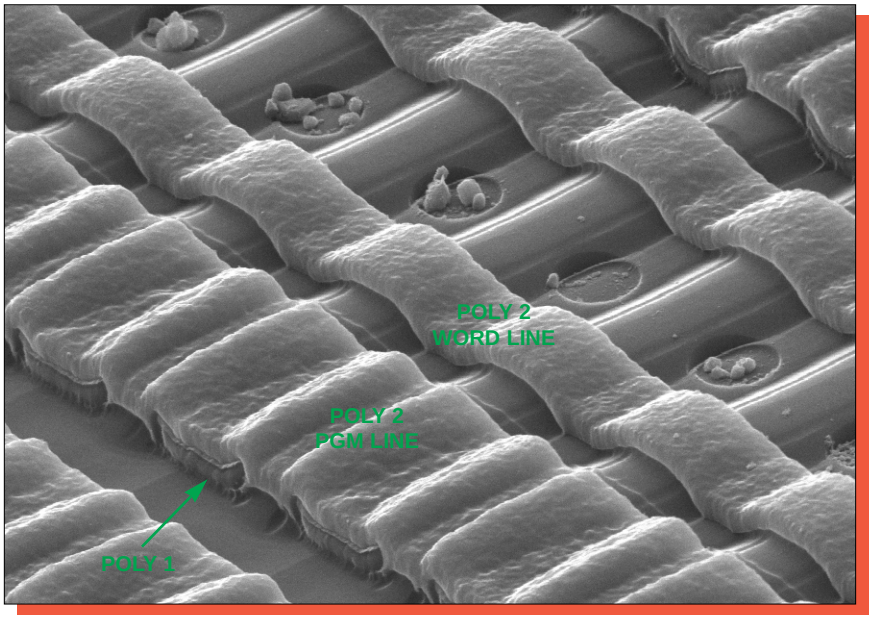



poly 2

Figure 28. SEM views illustrating EEPROM cell array. Mag. 1600x, 60°.

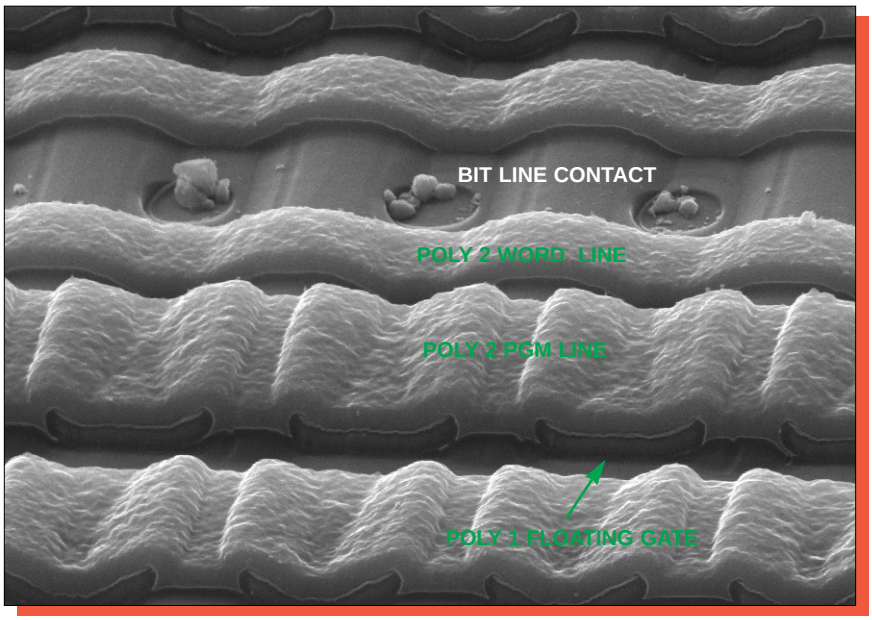



aluminum

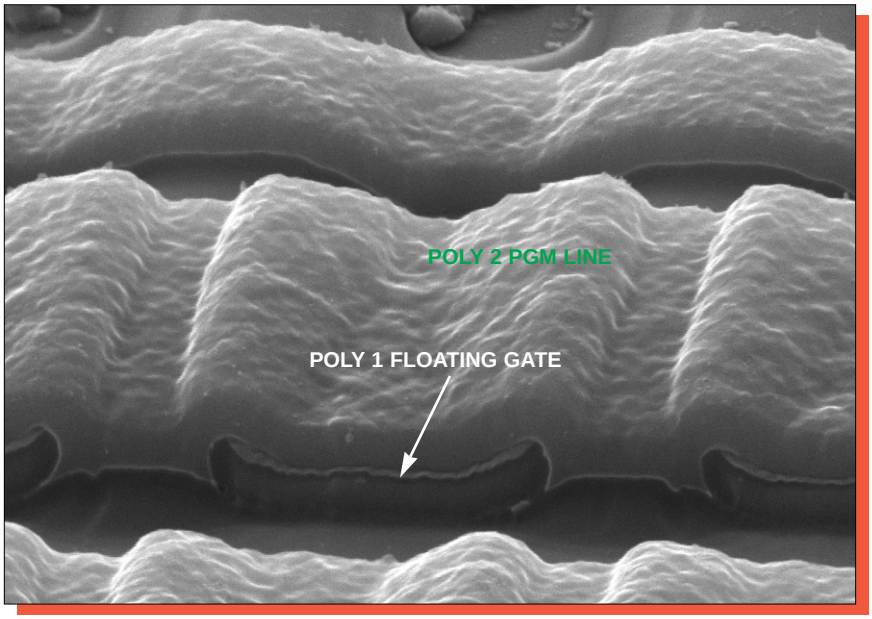



poly 2

Figure 29. SEM views illustrating EEPROM cell array. Mag. 6500x, 60°.

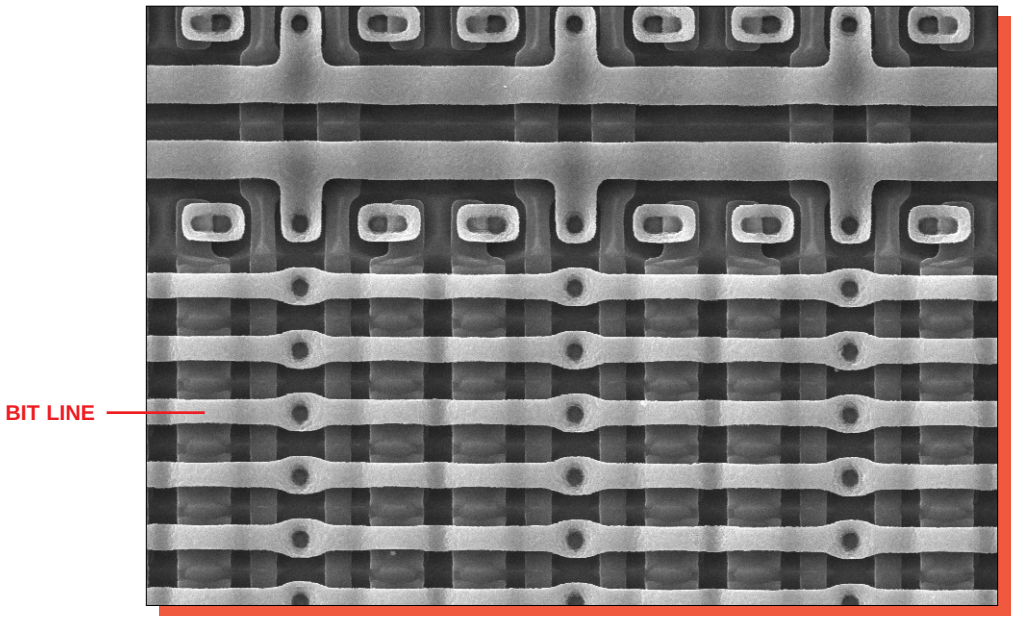



Mag. 6500x

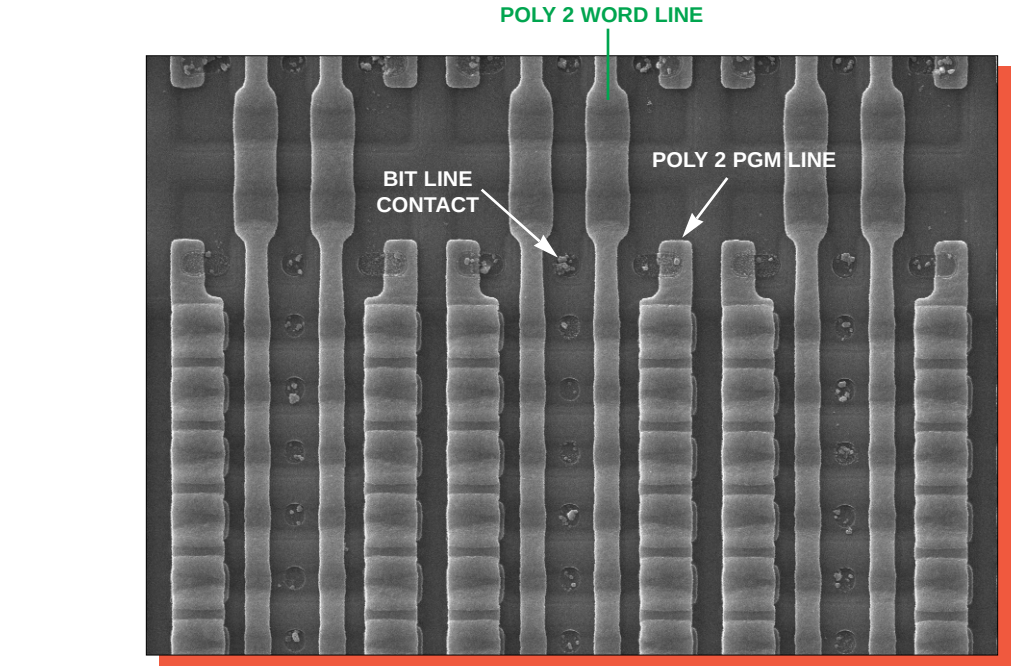



Mag. 13,000x

Figure 29a. Additional SEM views illustrating EEPROM cell array. 60°.

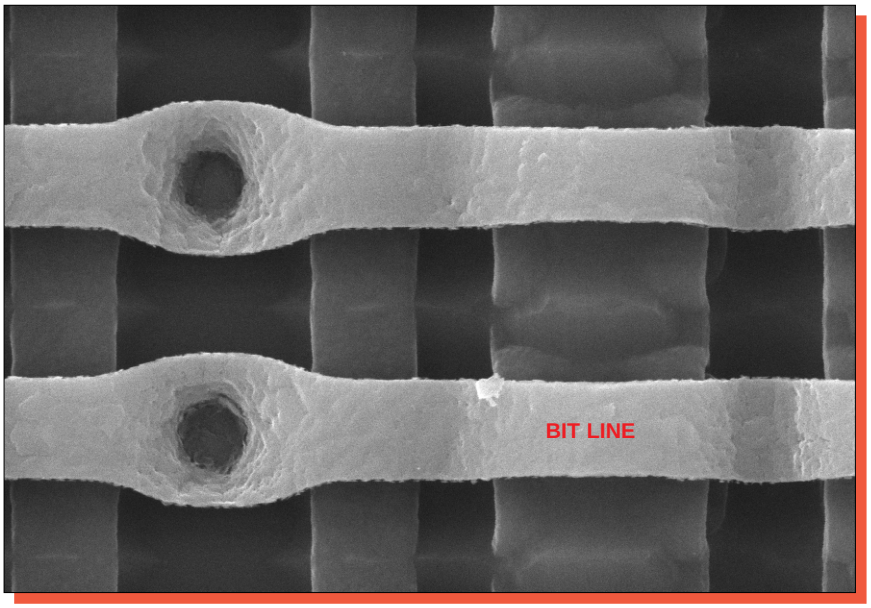



aluminum

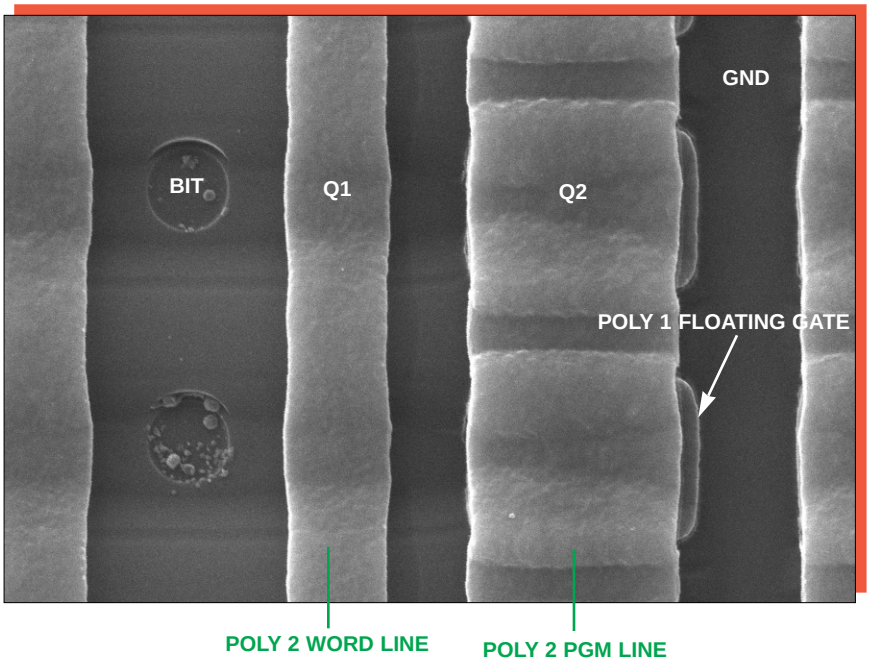



poly 2

Figure 30. Topological SEM views illustrating EEPROM cell array. Mag. 1600x, 0°.




aluminum




unlayered

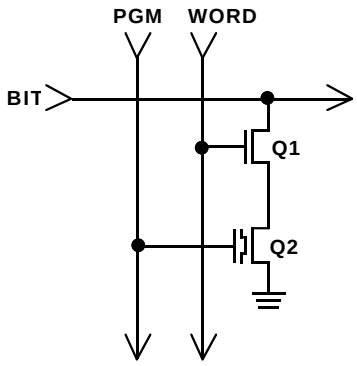
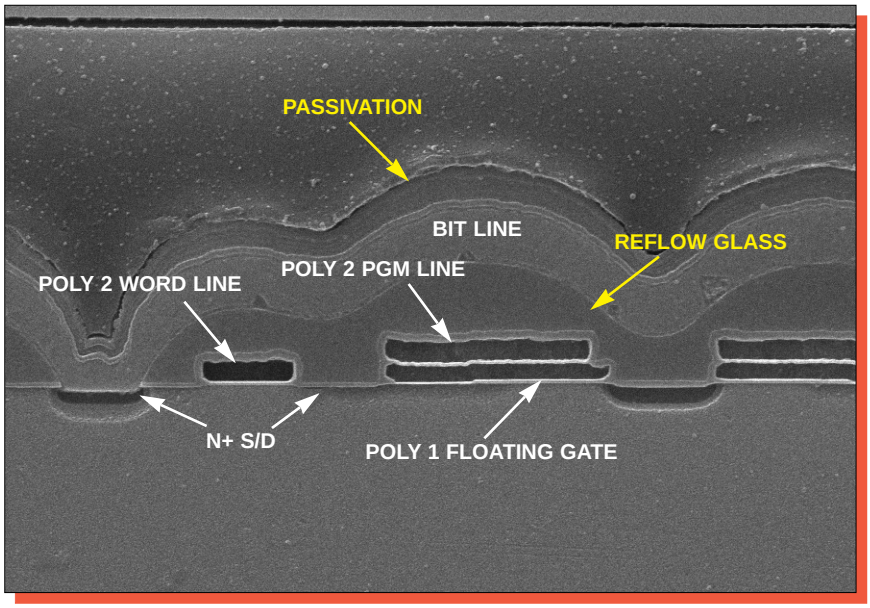
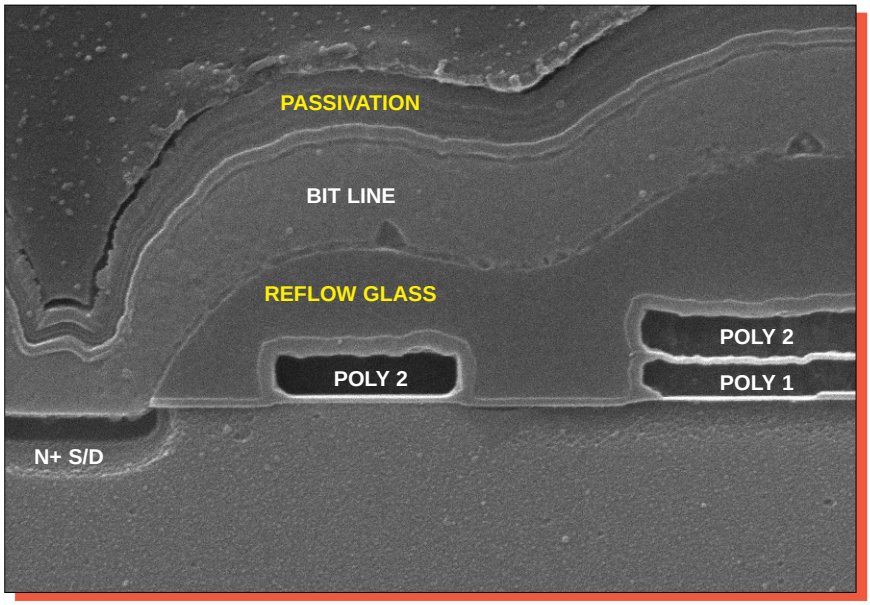


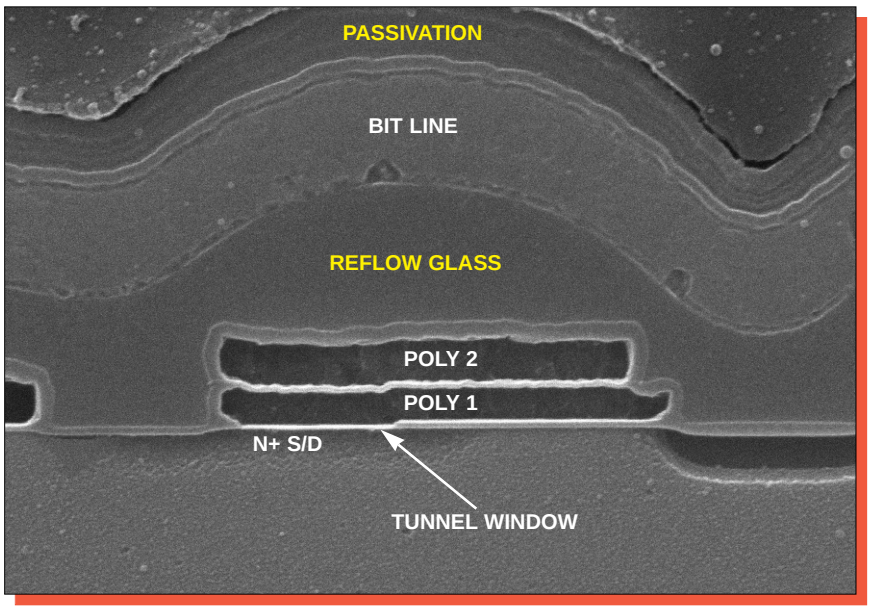

Figure 31. Topological SEM views illustrating EEPROM cell array and schematic. Mag. 6500x.




Mag. 6,500x

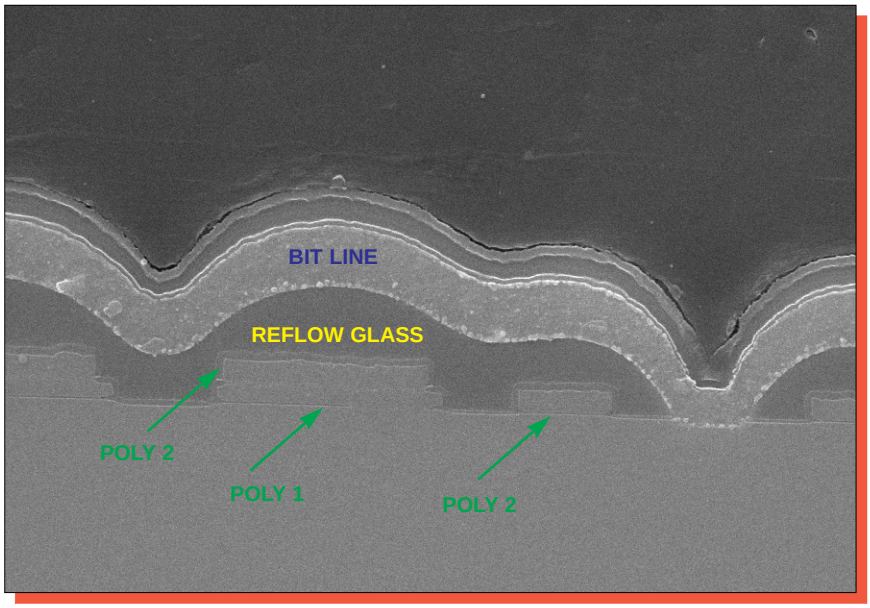



Mag. 13,000x

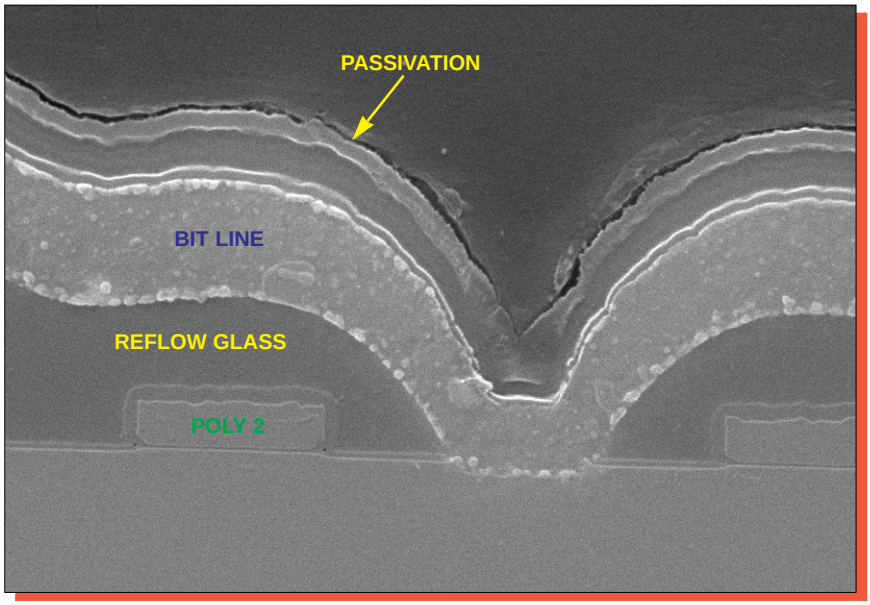



Mag. 13,000x

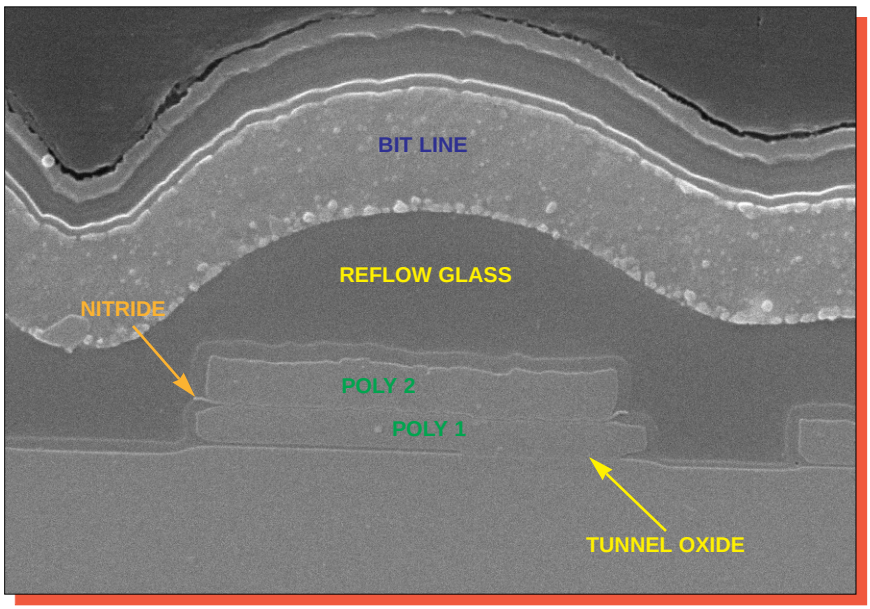
Figure 32. SEM section views illustrating EEPROM cell.




Mag. 6500x

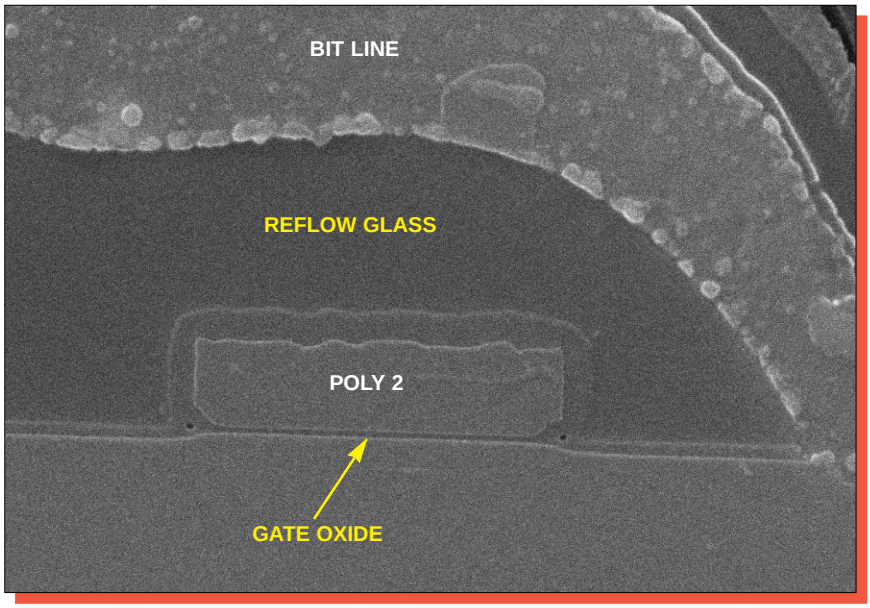



Mag. 13,000x

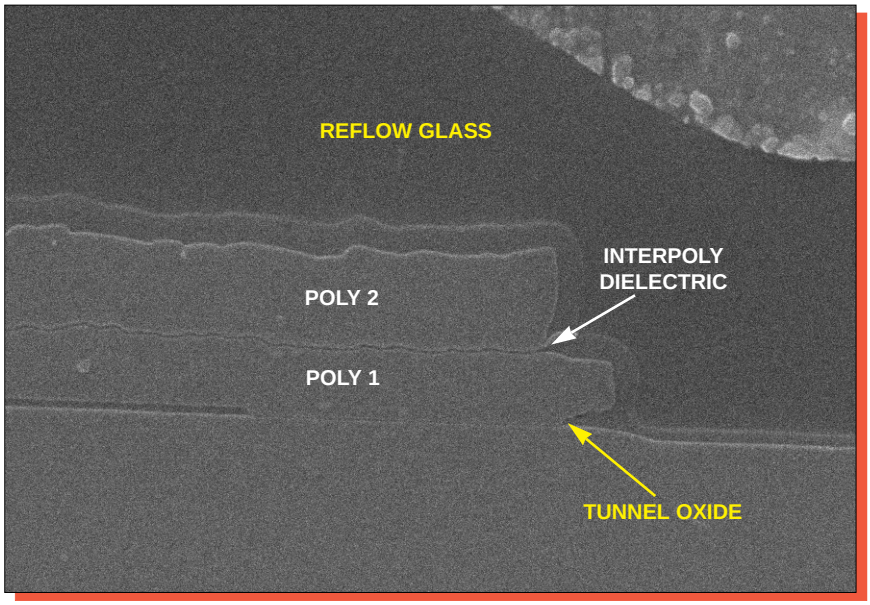



Mag. 13,000x

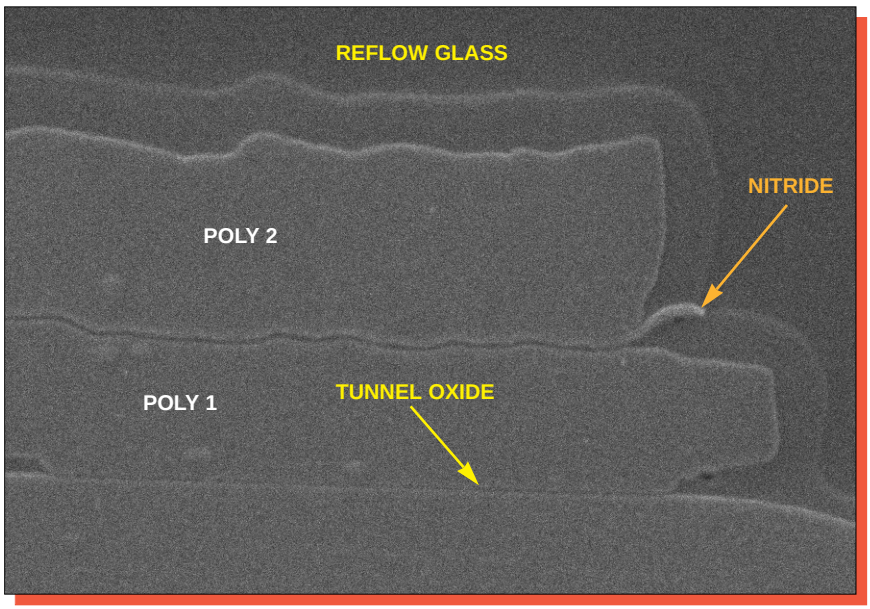
Figure 32a. SEM section views illustrating a EEPROM cell. Glass etch.




Mag. 26,000x

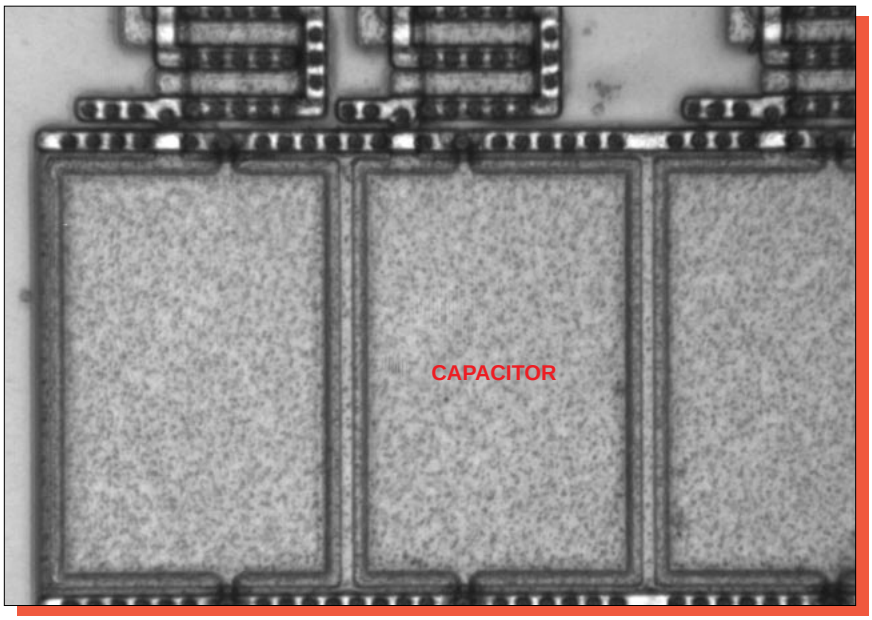



Mag. 26,000x

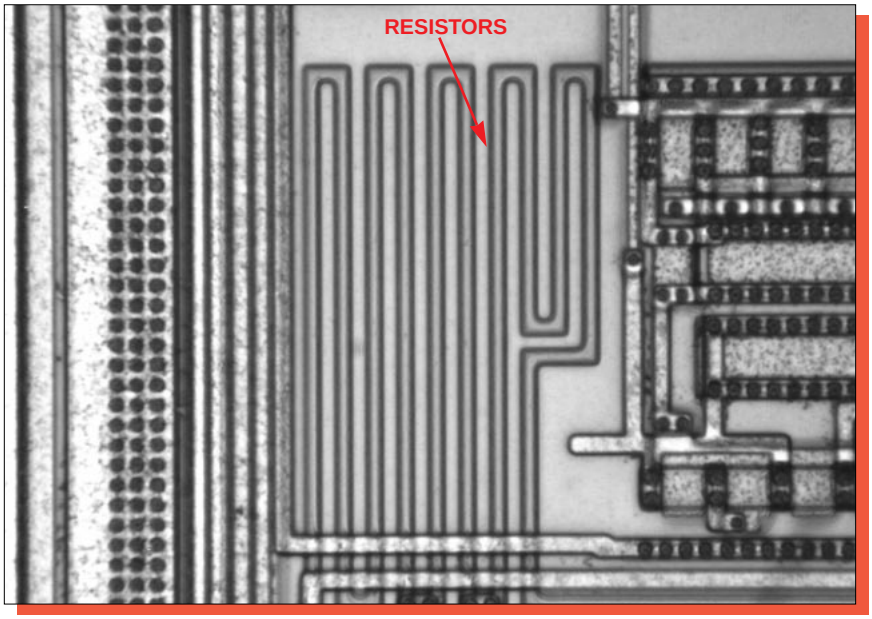



Mag. 52,000x

Figure 32b. Additional SEM section views illustrating a EEPROM cell. Glass etch.

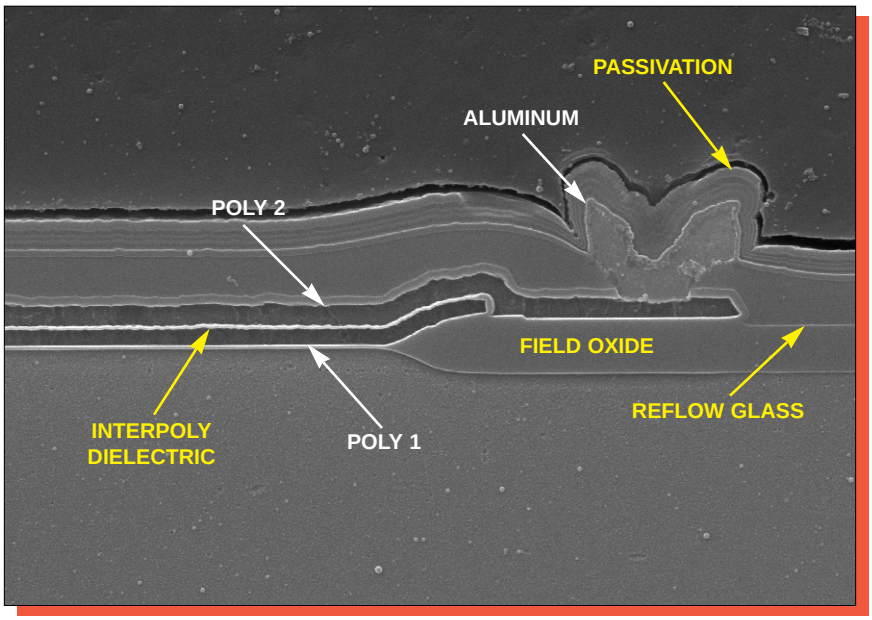



Mag. 840x

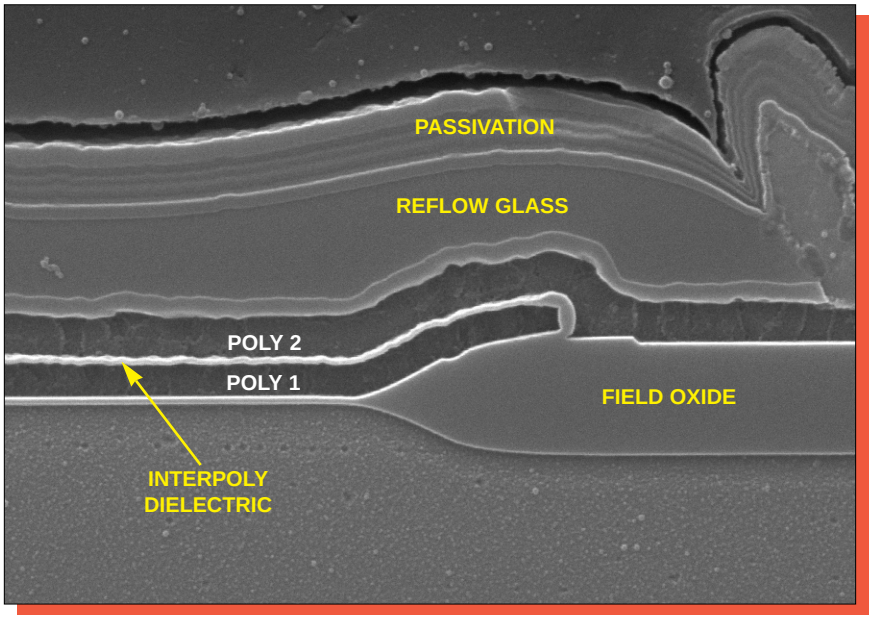



Mag. 700x

Figure 33. Optical views of capacitors and resistors.

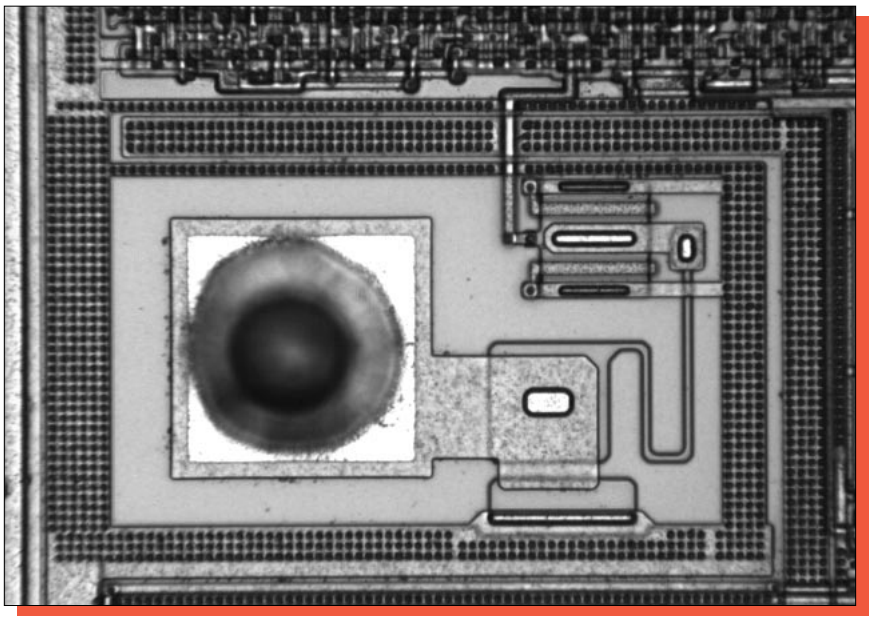



Mag. 6500x

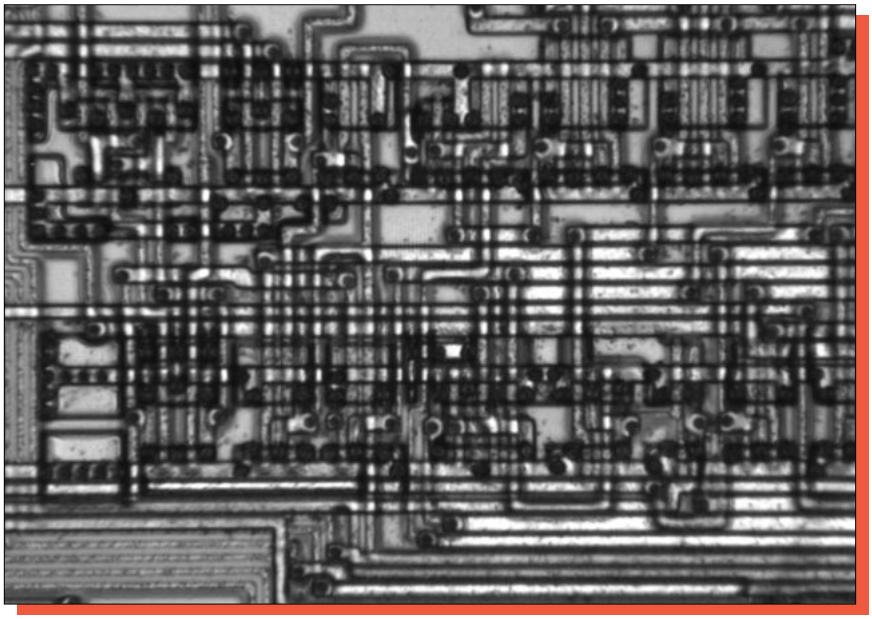



Mag. 13,000x

Figure 34. SEM section views illustrating a poly-to-poly capacitor.

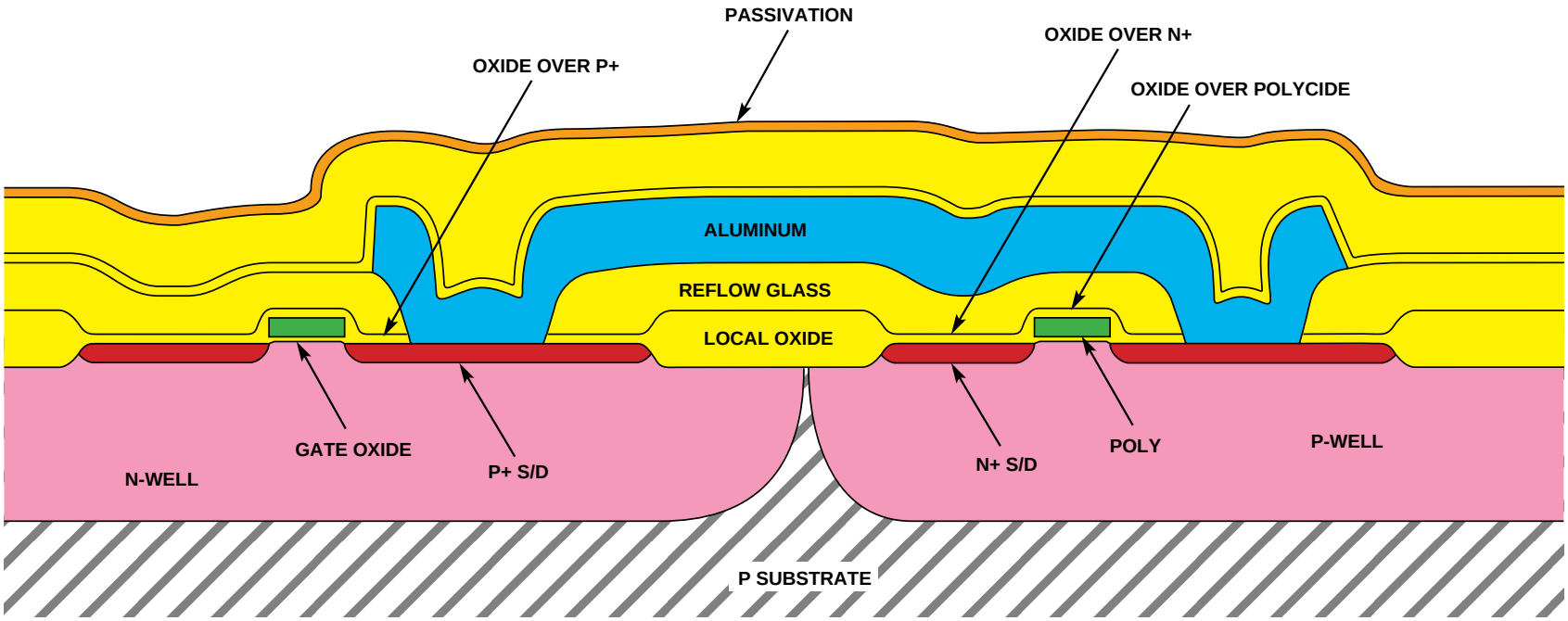


Mag. 350x



Mag. 600x

Figure 35. Optical views of an input structure and typical circuitry.




Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 36 . Color cross section drawing illustrating device structure.