Construction Analysis

QuickLogic QL24x32B CMOS FPGA

Report Number: SCA 9612-510

INTEGRATED CIRCUIT ENGINEERING

15022 N. 75th Street
Scottsdale, AZ 85260-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: http://www.ice-corp.com/ice

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INTRODUCTION

This report describes a construction analysis of the Quick Logic QL24 x 32 Field Programmable Gate Array with 8000 usable gates. One device was supplied for the analysis. It was packaged in an 84-pin Plastic Quad Flat Pack (PQFP) that had been partially decapsulated.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 1 aluminum thinning up to 100 percent[2] at some contact edges (Figure 14). Barrier maintained continuity. With the addition of the cap and barrier metal, overall metal thinning was 85 percent.

Special Features:

- Antifuse technology, reportedly using amorphous silicon as a programming dielectric.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Die Process and Design:

- Fabrication process: Devices were fabricated using a selective oxidation CMOS process with twin wells. No epi was present.

- Overlay passivation: A layer of nitride over silicon-dioxide.

- Metallization: Metal conductors consisted of two levels of aluminum defined by dry-etch techniques. Titanium-tungsten caps and barriers were employed on both metal layers. Metal 2 utilized titanium-tungsten plugs while metal 1 employed standard contacts.

- Interlevel dielectric: Interlevel dielectric consisted of two layers of glass with a spun-on glass (S.O.G.) between to aid in planarization.

- Pre-metal glass: A layer of a CVD glass that had been reflowed prior to contact cuts.

- Polysilicon: One level of dry-etched polysilicon was used. This poly level formed the gates of all transistors on the die.

- Buried contacts: No poly-to-diffusion (buried) contacts were used.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the transistors. Oxide sidewall spacers were used to provide the LDD spacing.

- Isolation: LOCOS (Local oxide).

- Wells: Twin-wells were employed on a P substrate. A step was noted in the LOCOS at the well boundaries.

TECHNOLOGY DESCRIPTION (continued)

- Memory cell: The antifuse memory cells consist of a dielectric (reportedly amorphous silicon) sandwiched between metal 2 and the tungsten plugs. The metal 2 “piggyback” line is used as the upper electrode while the tungsten plug connected to metal 1 is used as the lower electrode. The amorphous-silicon “ViaLink” is used as the conductive link connecting metal 2 to metal 1. The dielectric insulates the two electrodes until a programming voltage is applied to selected vias which creates a conductive path between the electrodes by converting the silicon to a low resistance state.

ANALYSIS RESULTS

Die Process and Design **Figures 1 - 28**

Questionable Items:[1]

- Metal 1 thinning up to 100 percent[2] at some contact edges (Figure 14). Barrier maintained continuity. With the addition of a cap and barrier metal, overall metal thinning was 85 percent.

Special Features:

- Antifuse technology, reportedly using amorphous silicon as a programming dielectric.

Design Features:

- Metal 1 array of contacts.

- Wide metal 1 and 2 bus lines.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a p-substrate. No epi was used.

- Design and layout: Die layout was clean and efficient. Alignment was good at all layers and contacts were completely surrounded by metal.

- Die surface defects: No damage, process defects, or contamination was found.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS (continued)

- Overlay passivation: A layer of nitride over silicon-dioxide. Coverage of the passivation was good with no defects noted following integrity tests. There was no hillock growth present in the aluminum.

- Metallization: Both metal 1 and 2 levels consisted of aluminum with titanium-tungsten caps and barriers and were defined using dry-etch techniques. No thinning of metal 2 was noted due to the use of titanium-tungsten plugs. Metal 2 made direct contact to metal 1 and the antifuse dielectric. The metal 2 plugs varied slightly depending on where they were located (i.e. under M2 barrier or antifuse dielectric).

- Antifuse dielectric: A dielectric layer reportedly of amorphous silicon was used between metal 2 and the titanium-tungsten plugs in the antifuse array, as the programming material (see below).

- Metal step coverage: Maximum metal 1 thinning of 100 percent at some contact edges (barrier maintained continuity). Total metal 1 thinning varied from 70 percent to 90 percent (including cap and barrier). MIL-STD-883 allows up to 70 percent metal thinning for contacts of this size. Metal 1 used standard contacts to poly and diffusions.

- Interlevel dielectric: The interlevel dielectric consisted of a multilayered, silicon-dioxide separated by a spun-on glass (SOG) to aid in planarization. No problems were found with these layers.

- Pre-metal glass: A single layer of a CVD glass. This layer had been reflowed following contact cuts.

- Polysilicon: Definition of poly was by a dry-etch technique and was good. A single layer of poly-silicon (no silicide) formed all the transistors on the die.

- Isolation: Local oxide (LOCOS) isolation. No problems were present at the birdsbeaks or elsewhere.

ANALYSIS RESULTS (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. An LDD process was used employing oxide sidewall spacers. The spacers were left in place. Diffusions were not silicided No problems were found in these areas.

- Wells: Twin-wells in a P-substrate. Definition was normal. A step was noted in the local oxide at the well boundaries.

- Memory cell: The antifuse memory cell consists of a dielectric (reportedly amorphous silicon) sandwiched between metal 2 and the tungsten plugs to metal 1. The metal 2 “piggyback” line is used as the upper electrode while plugs are used as the lower electrodes. The amorphous silicon (ViaLink) is used as the programmed conductive element connecting metal 2 to metal 1. The amorphous silicon acts as a dielectric that insulates the two electrodes until a programming voltage is applied to selected vias, creating a conductive link between the electrodes by converting the amorphous silicon to a low resistance state.

PROCEDURE

The sample was subjected to the following analysis procedures:

Optical inspection

SEM inspection of assembly features and passivation

Divide die into 2 pieces

Passivation removal and inspect metal 2

Aluminum removal (metal 2) and inspect barrier

Delayer to metal 1 and inspect

Aluminum removal (metal 1) and inspect barrier

Delayer to poly/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Material analysis (die)

**Delineation of cross-sections is by silicon-etch unless otherwise indicated*

OVERALL QUALITY EVALUATION: Overall Rating: Normal/Poor

DETAIL OF EVALUATION

Dicing quality	G
Wirebond method	Thermosonic ball bonds
Die attach method	Silver epoxy
Dicing method	Sawing
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity[1]	NP
Metal registration	N
Contact coverage	G
Contact registration	G

[1]100 percent metal 1 aluminum thinning.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

CONTACT MATRIX

	Metal 2	**Metal 1**	**Poly**	**+N**	**P+**
Metal 2		X			
Metal 1	X		X	X	X

DIE MATERIAL ANALYSIS

Passivation:	A layer of nitride over silicon-dioxide.
Metal 2:	Aluminum with a titanium-tungsten cap and barrier.
Antifuse dielectric:	Amorphous silicon.
M2 plugs:	Titanium-tungsten plugs.
Interlevel dielectric 1 (M2 and M1):	Two thick layers of silicon-dioxide with a spun-on glass (SOG) in between.
Metal 1:	Aluminum with a titanium-tungsten cap and barrier. A titanium adhesion layer was present under the metal.
Pre-metal glass:	A single layer of reflow glass over a layer of densified oxide.
Poly:	Polysilicon (no silicide).

HORIZONTAL DIMENSIONS

Die size (scribe to scribe):	10.4 x 12.4 mm (410 x 491 mils)
Die size (seal to seal):	10.3 x 12.3 mm (406 x 487 mils)
Die area (scribe to scribe):	128.9 mm^2 (201,310 $mils^2$)
Die area (seal to seal):	126.7 mm^2 (197,722 $mils^2$)
Min pad size:	0.10 x 0.10 mm (4.3 x 4.3 mils)
Min pad window:	0.09 x 0.09 mm (3.9 x 3.9 mils)
Min pad space:	0.06 mm (2.5 mils)
Min pad to metal:	10 microns
Min metal 2 width:	2.0 microns
Min metal 2 space:	1.0 micron
Min metal 2 pitch:	3.0 microns
Min plug (M2 - M1):	0.9 micron
Min plug space (M2 - M1):	2.0 microns
Min metal 1 width:	1.0 micron
Min metal 1 space:	0.5 micron
Min metal 1 pitch:	1.5 micron
Min contact:	1.0 micron
Min contact space:	0.8 micron
Min polycide width:	0.65 micron
Min polycide space:	0.85 micron
Min polycide pitch:	1.5 micron
Min gate length* - (N-channel):	0.65 micron
- (P-channel):	0.65 micron
Antifuse area (amorphous silicon):	2 microns (dia.)
Antifuse space (amorphous silicon):	1.0 micron
Antifuse pitch:	3 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.5 mm (19.5 mils)
Layers:	
Passivation 2:	0.45 micron
Passivation 1:	0.5 micron
Metal 2 - cap:	0.05 micron
- aluminum:	0.9 micron
- barrier:	0.2 micron
Antifuse - (amorphous Si):	0.15 micron (approximate)
- TiW plug	1.2 micron
Interlevel dielectric:	0.95 micron
Metal 1- cap:	0.15 micron
- aluminum:	0.6 micron
- barrier:	0.15 micron
Adhesion layer:	0.05 micron
Pre-metal glass:	0.3 - 0.85 micron
Oxide on poly:	0.25 micron
Poly:	0.2 micron
Local oxide:	0.6 micron
N+ diffusion:	0.2 micron
P+ diffusion:	0.2 micron
N-well:	3.5 microns
P-well:	1.5 micron

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ANTIFUSE ARRAY STRUCTURE AND GENERAL CIRCUIT LAYOUT	Figures 21 - 24
IO LAYOUT	Figures 25 - 27
COLOR DRAWING OF DIE STRUCTURE	Figure 28

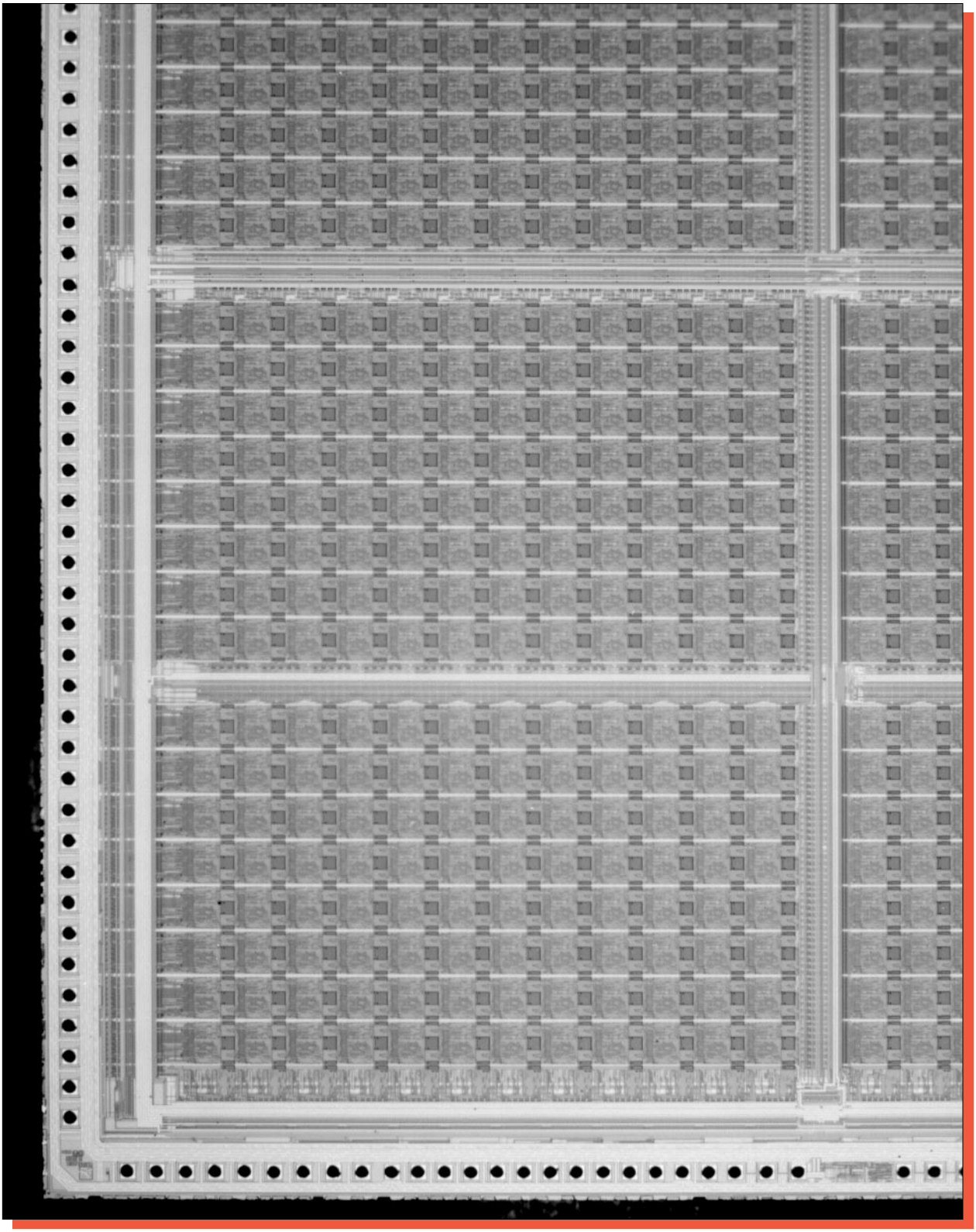


Figure 1. Portion of the QuickLogic 24X32 intact circuit die. Mag. 26x.

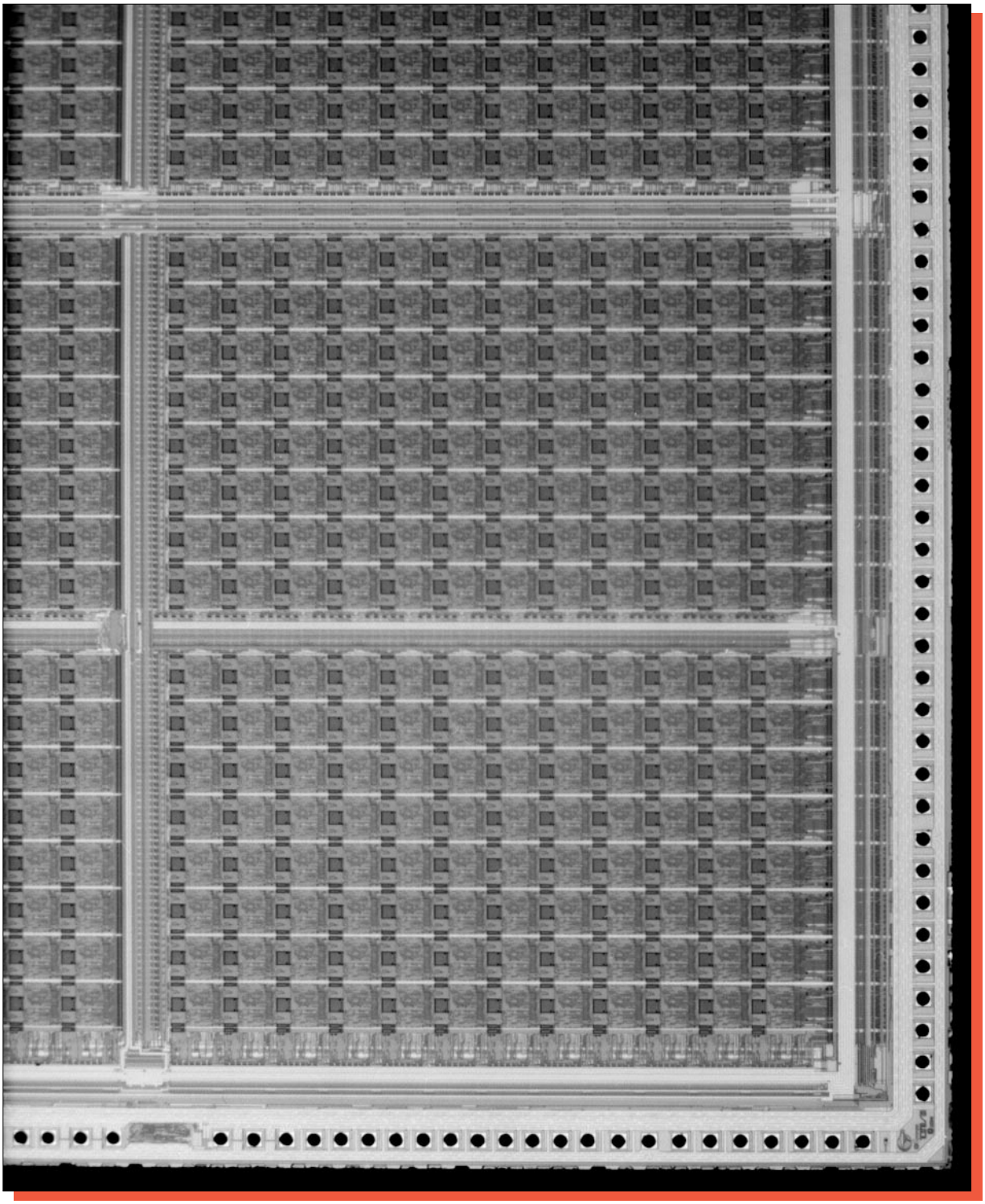


Figure 1a. Portion of the QuickLogic 24X32 intact circuit die. Mag. 26x.

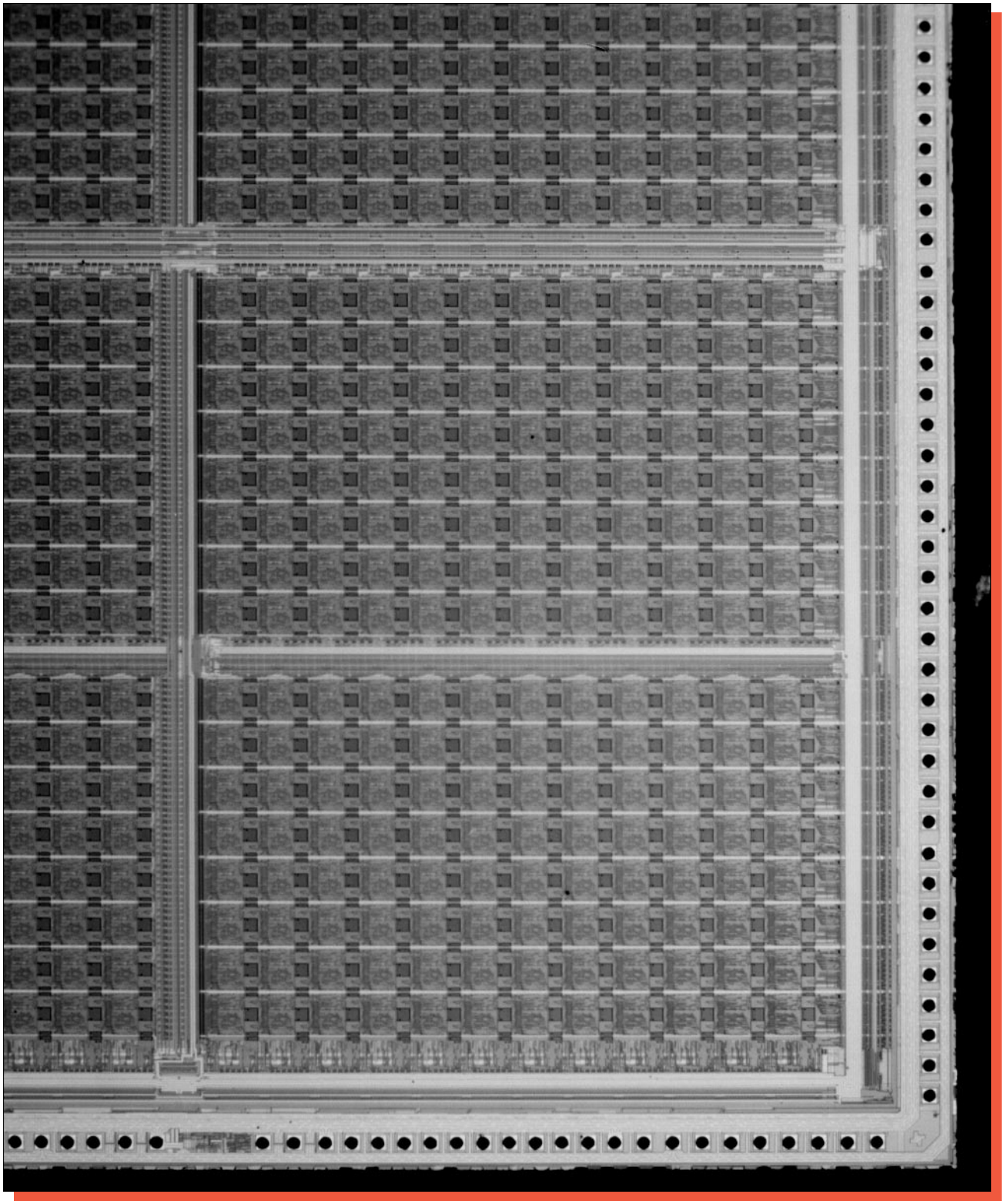


Figure 1b. Portion of the QuickLogic 24X32 intact circuit die. Mag. 26x.

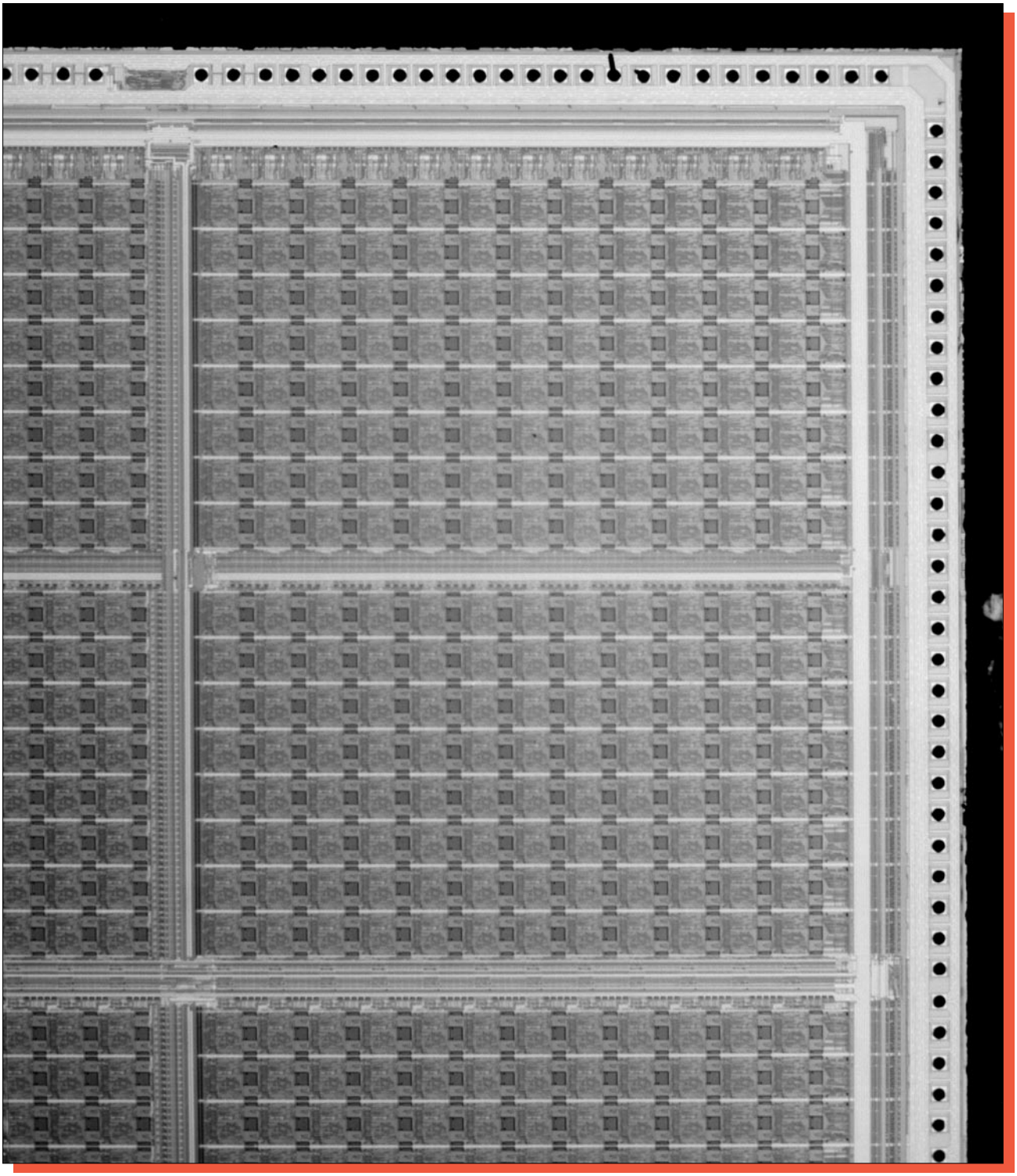
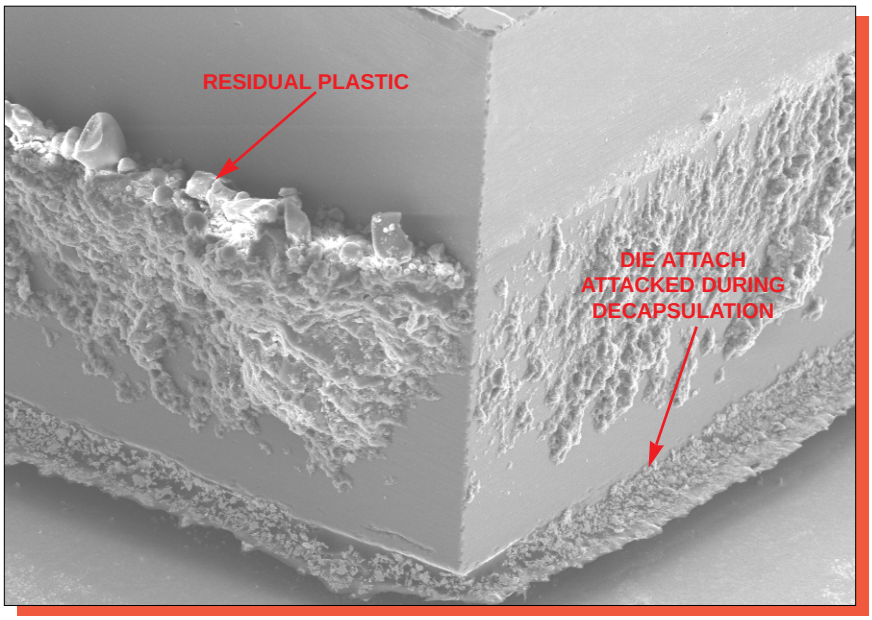
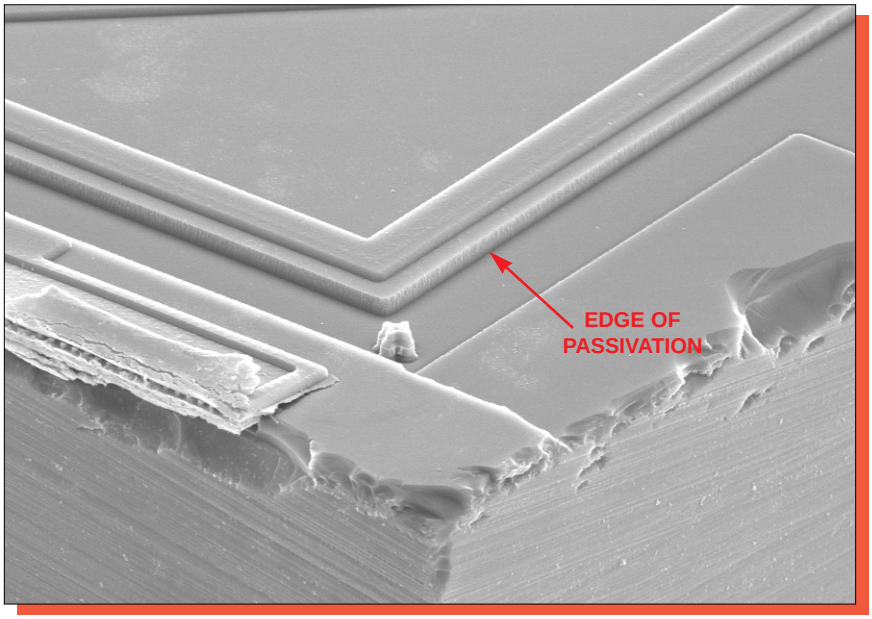


Figure 1c. Remaining portion of the QuickLogic 24X32 intact circuit die. Mag. 26x.

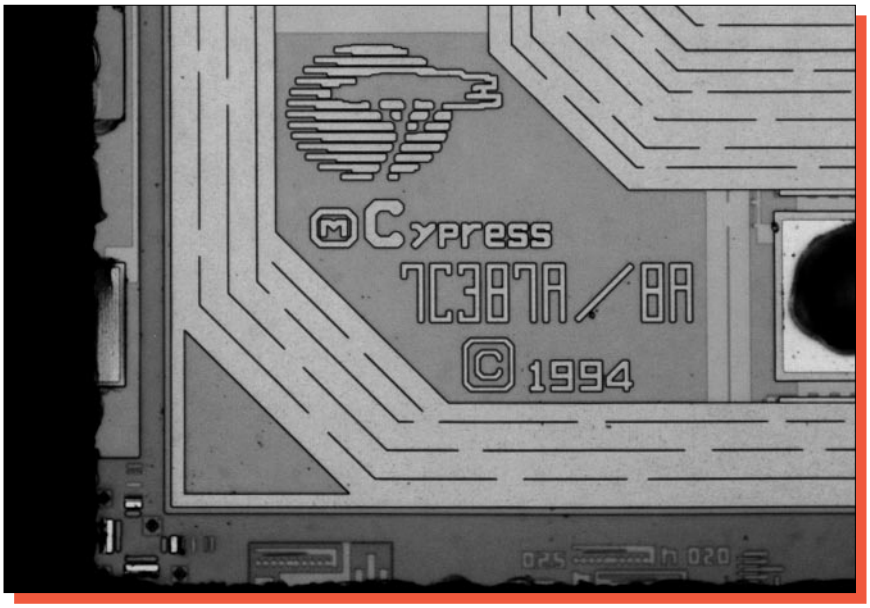


Mag. 160x

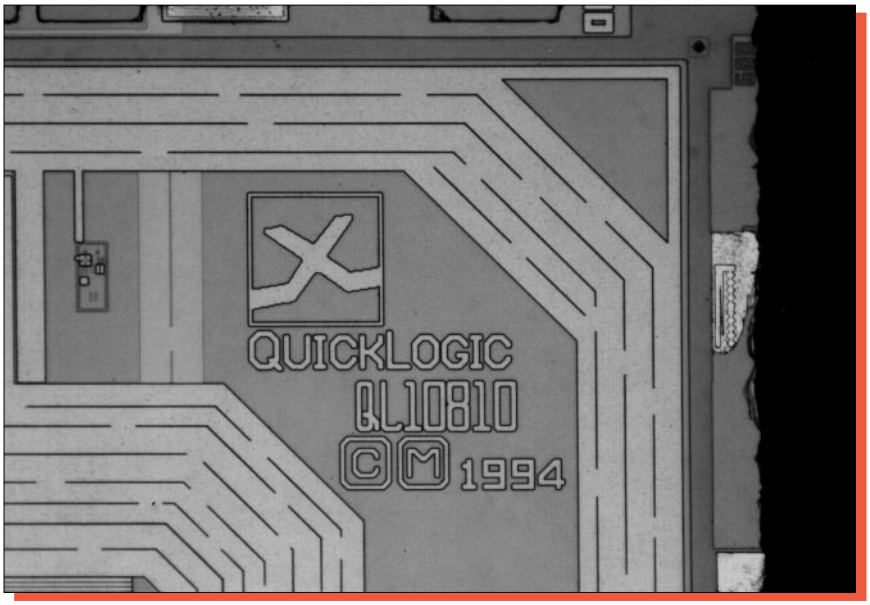


Mag. 800x

Figure 2. SEM views of a die corner and edge seal.



Mag. 200x



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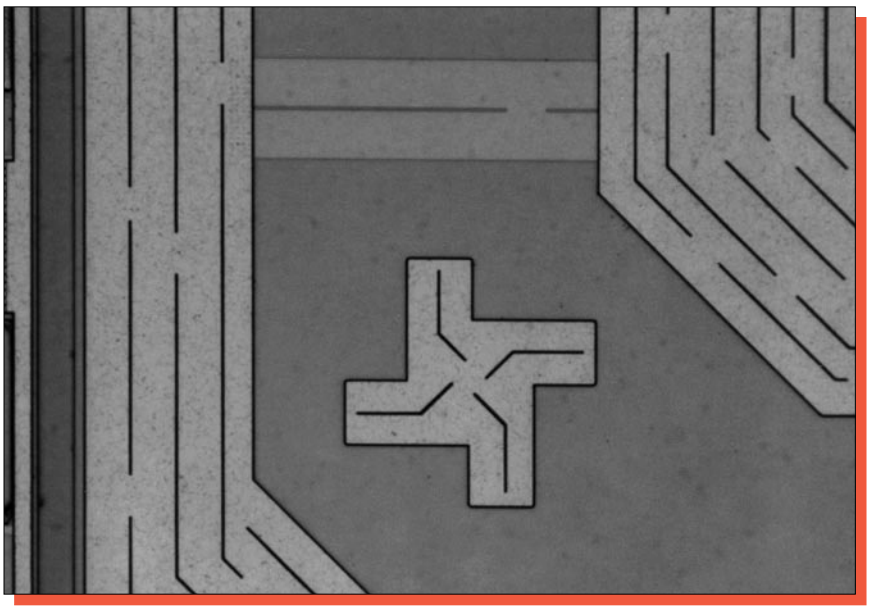
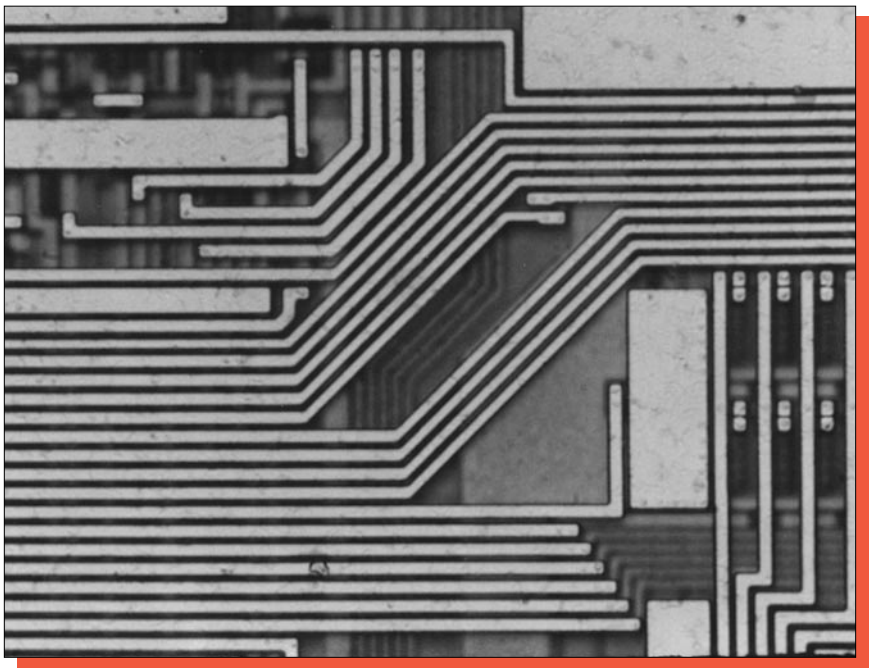
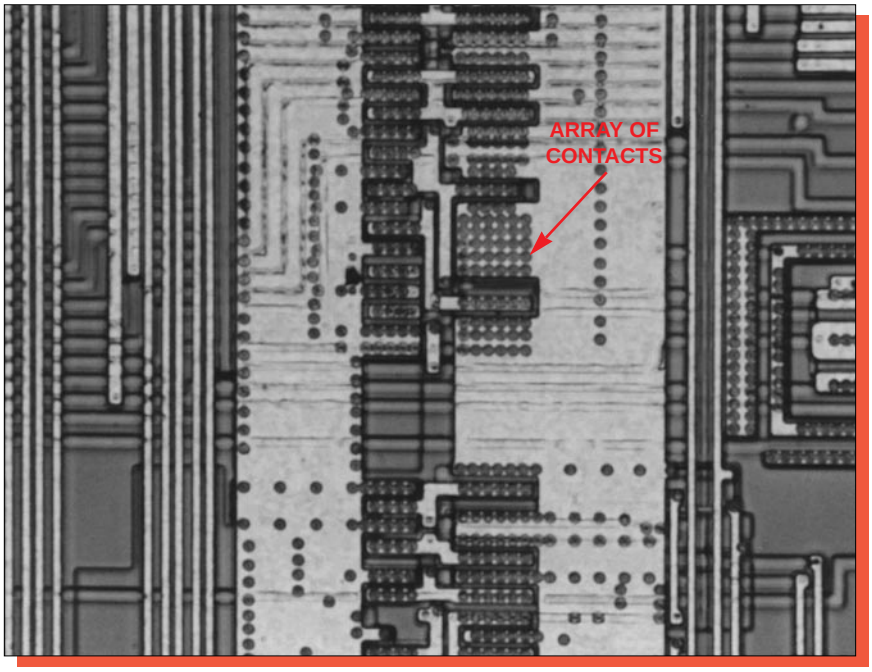


Mag. 320x

Figure 3. Markings from the die surface and measurement points.

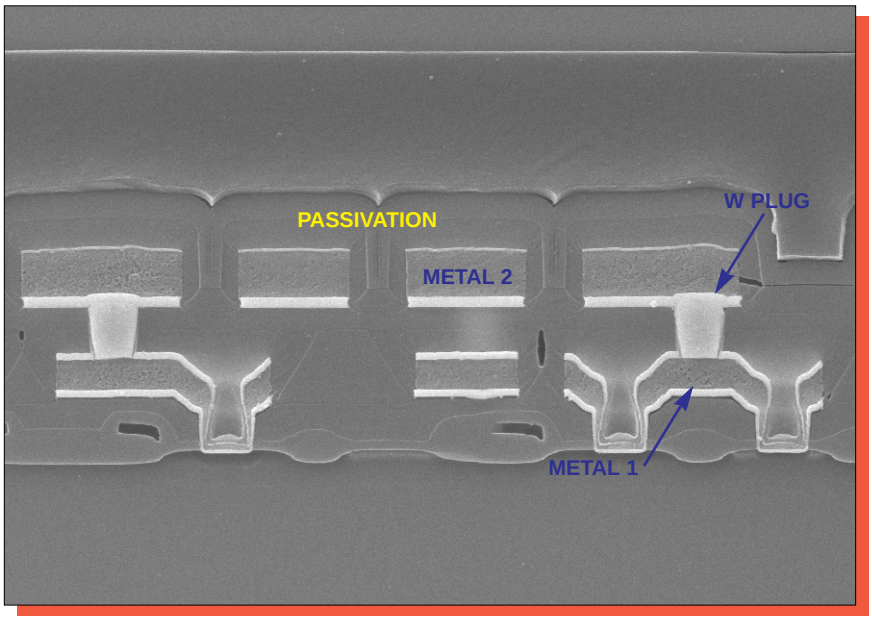


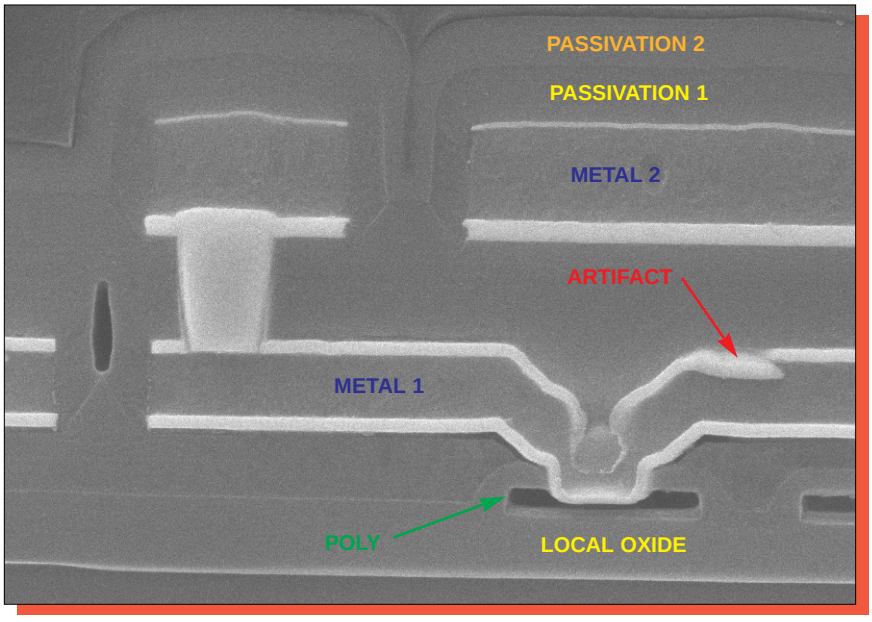
metal 2



metal 1

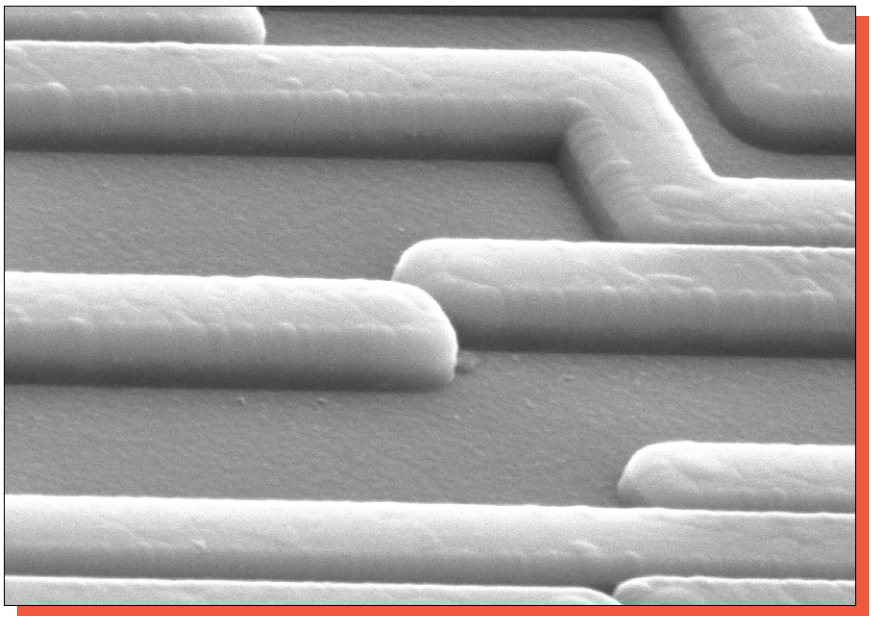
Figure 4. Optical views of metal layout features. Mag. 800x.



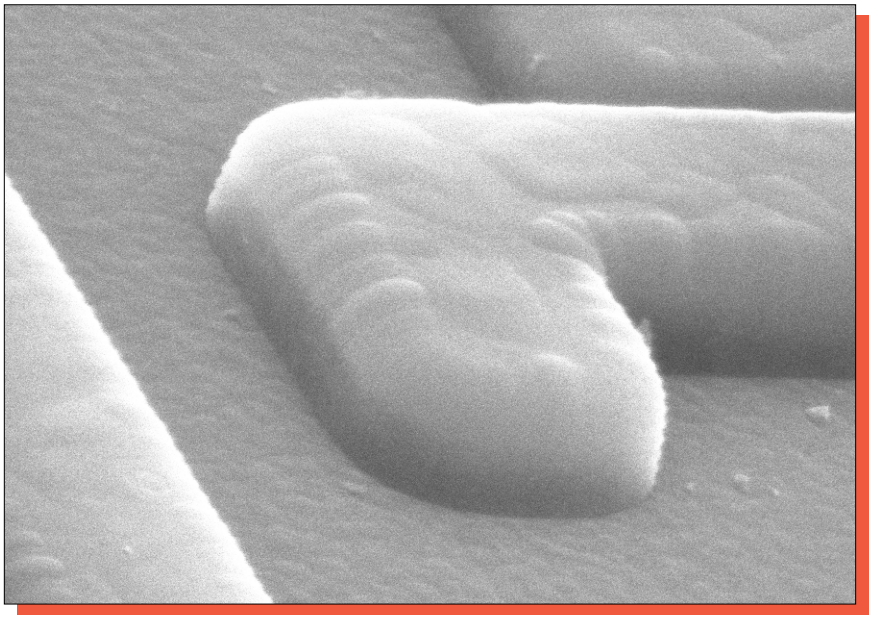


Mag. 6500x

Figure 5. SEM section views of general structure.



Mag. 5000x



Mag. 12,000x

Figure 6. SEM views of overlay passivation coverage. 60°.

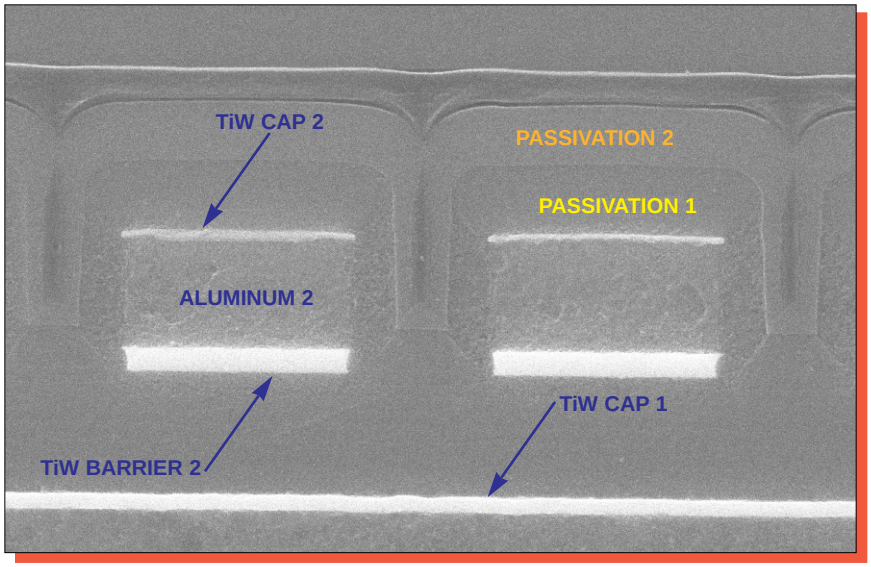
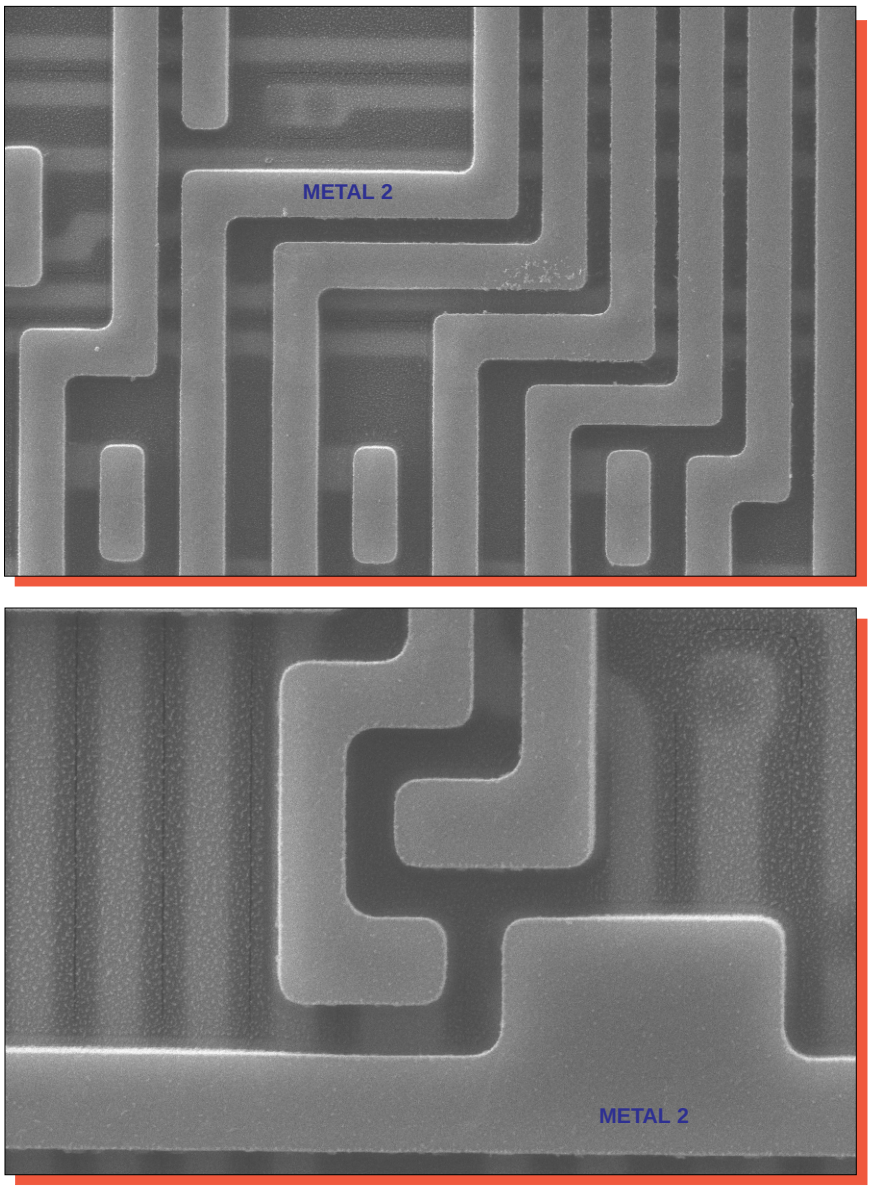


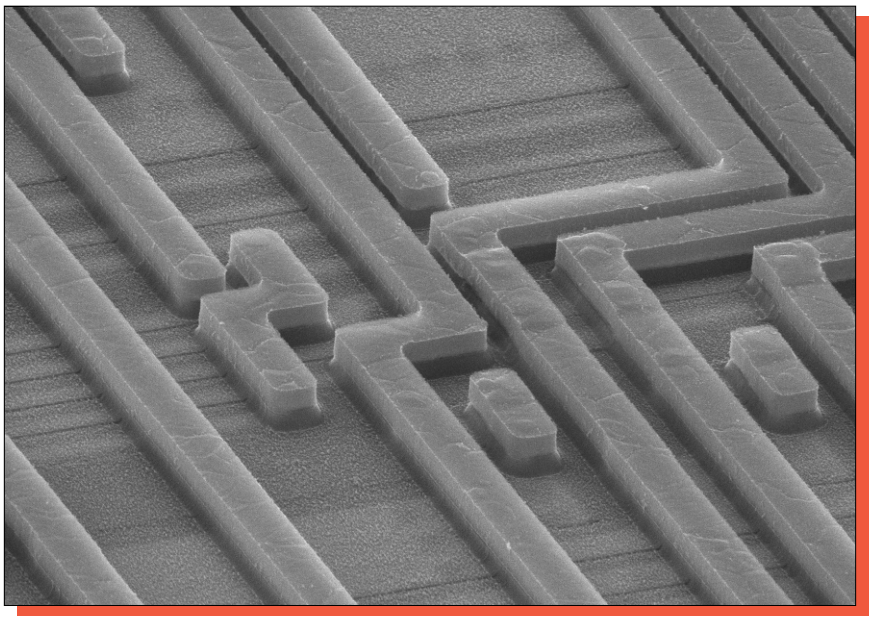
Figure 7. SEM section view of metal 2 line profiles. Mag. 16,000x.



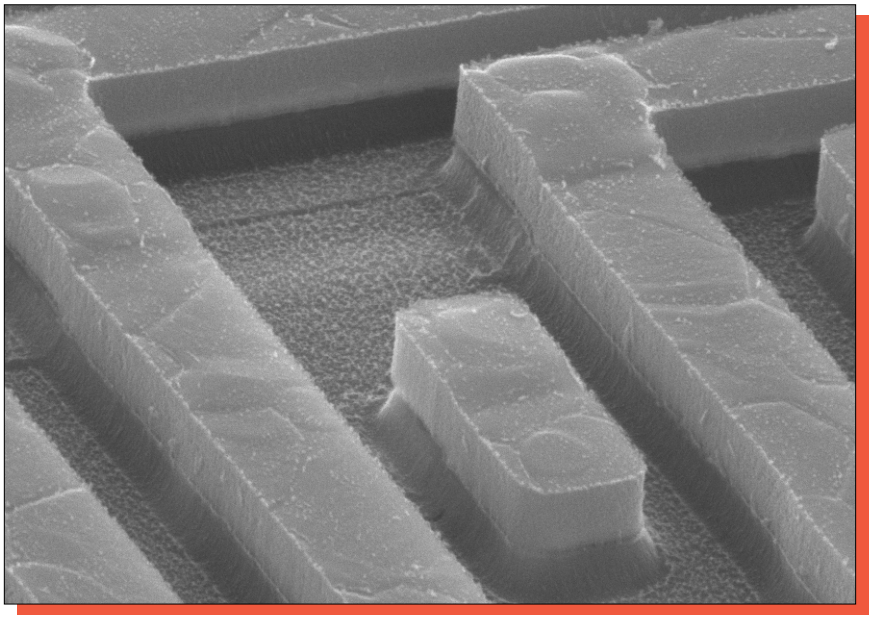
Mag. 3000x

Mag. 6000x

Figure 8. Topological SEM views of metal 2 patterning. 0°.

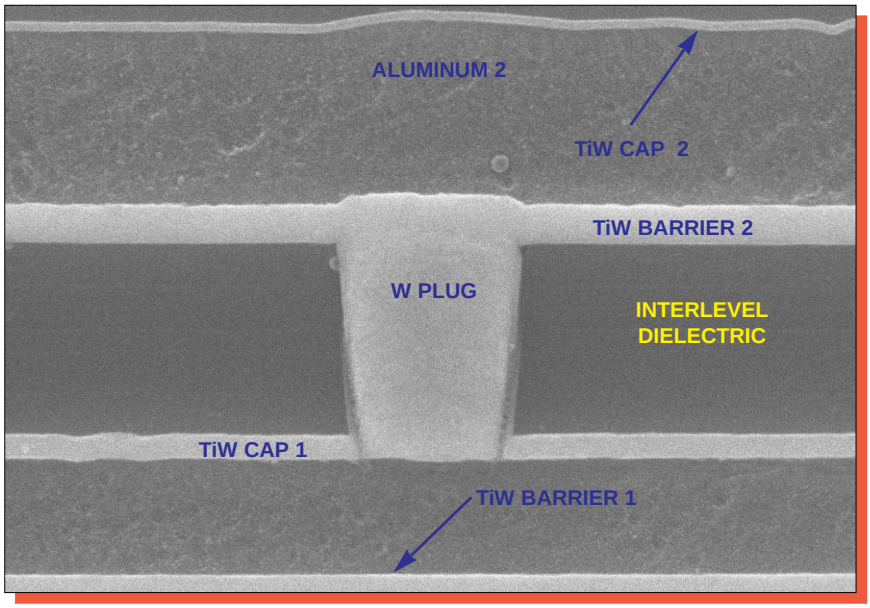


Mag. 3000x

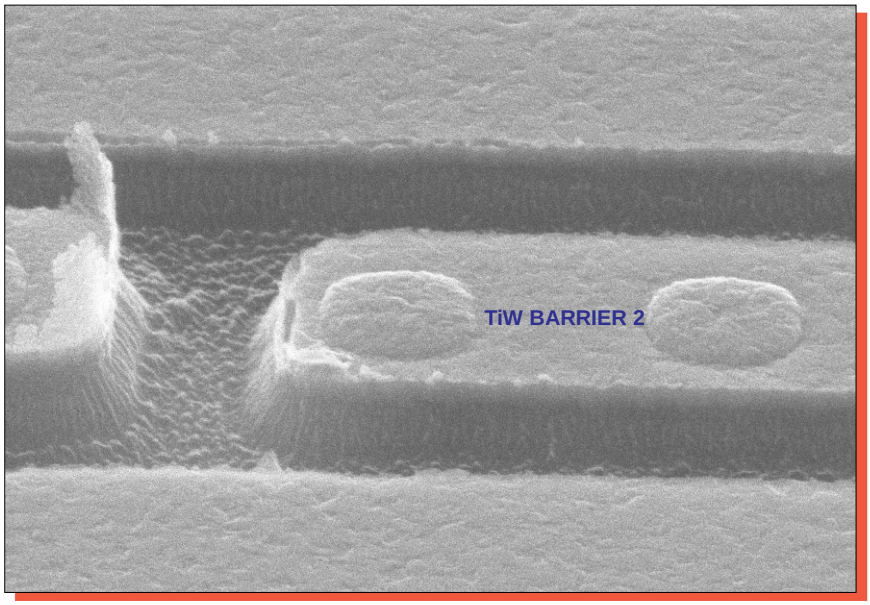


Mag. 10,000x

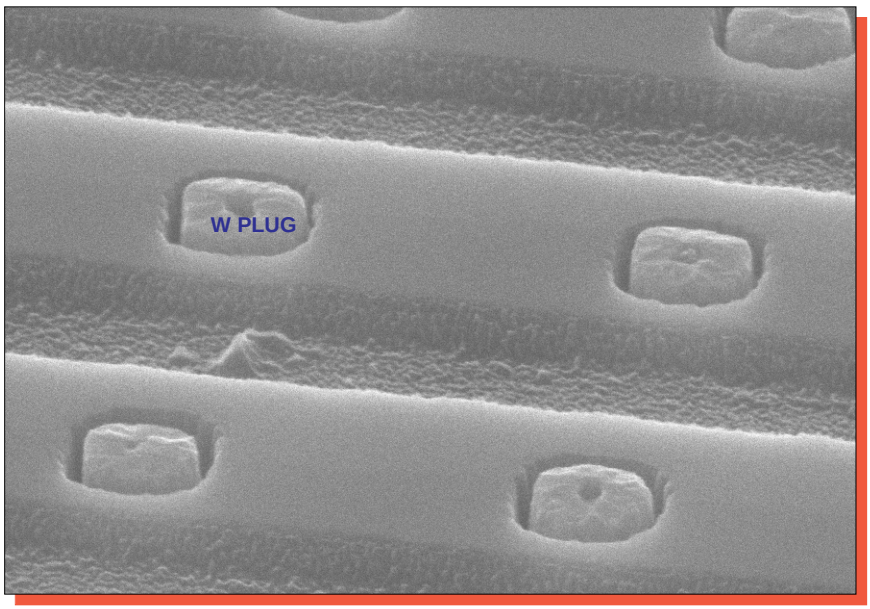
Figure 9. SEM views of general metal 2 integrity.



Mag. 25,000x



Mag. 20,000x



Mag. 20,000x

Figure 10. SEM views of metal 2-to-metal 1 via and barrier.

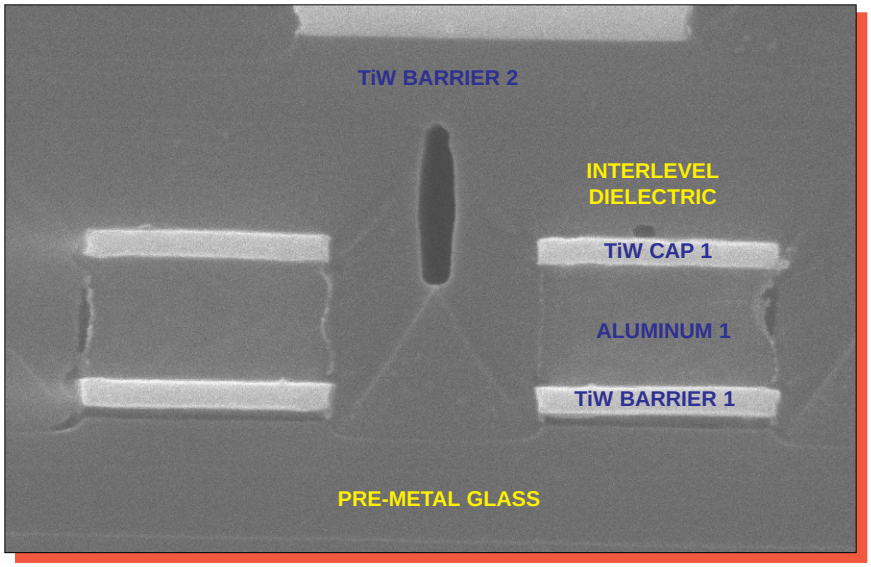


Figure 11. SEM section view of metal 1 line profiles. Mag. 26,000x.

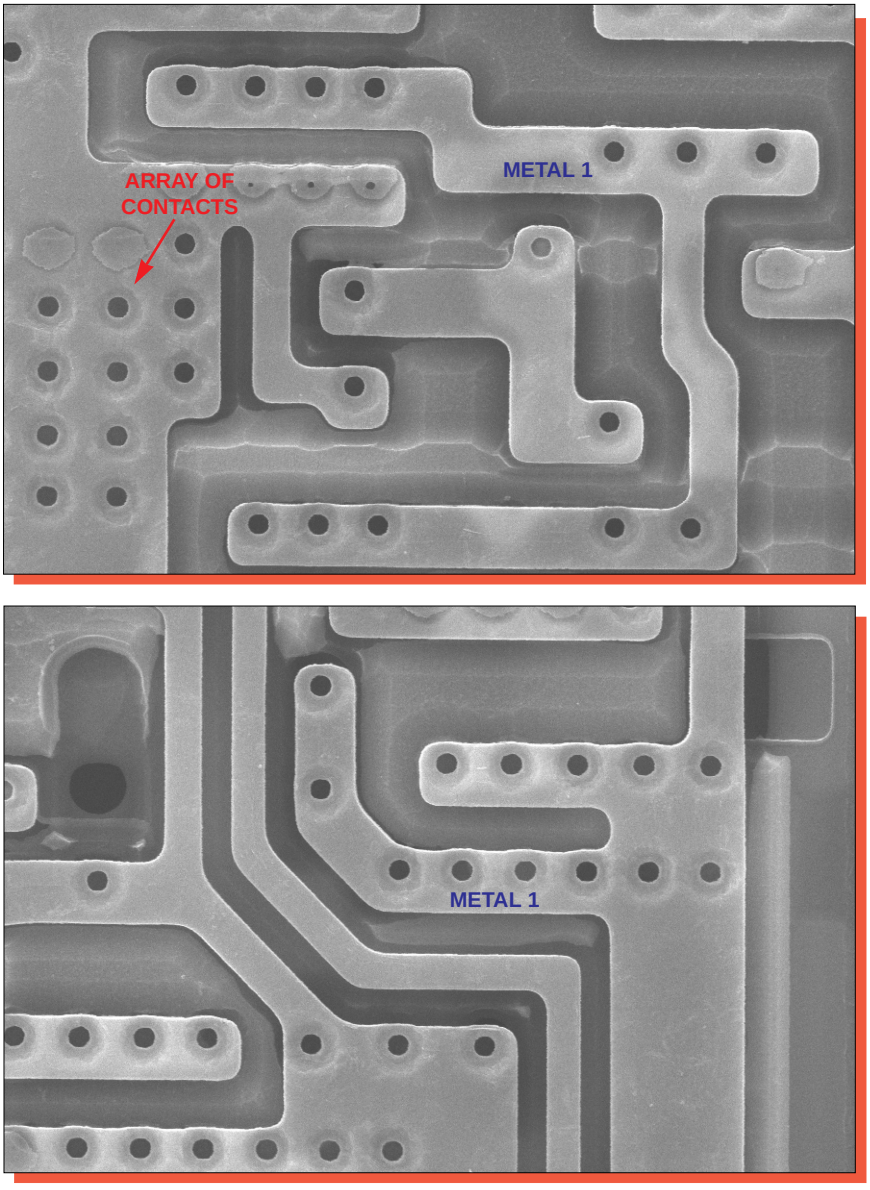
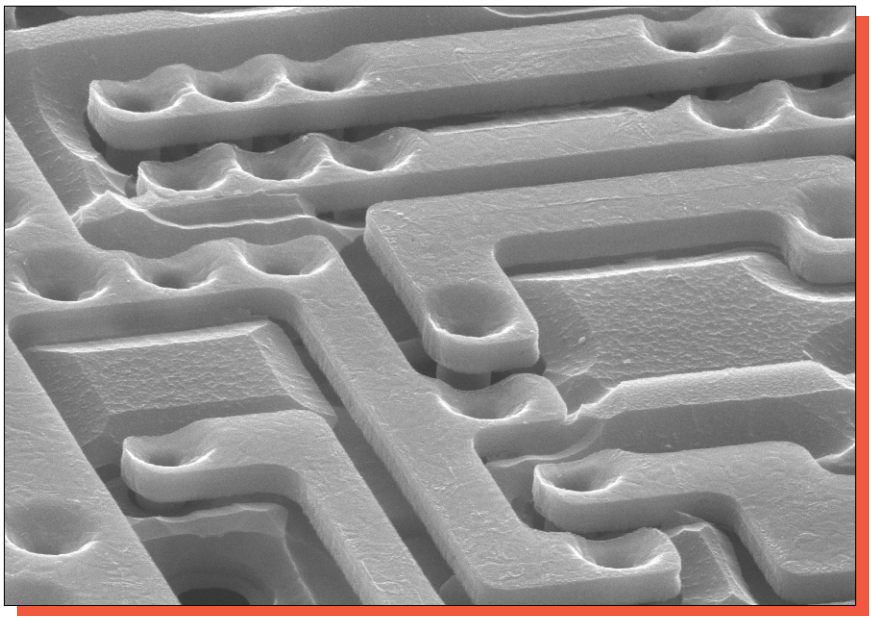
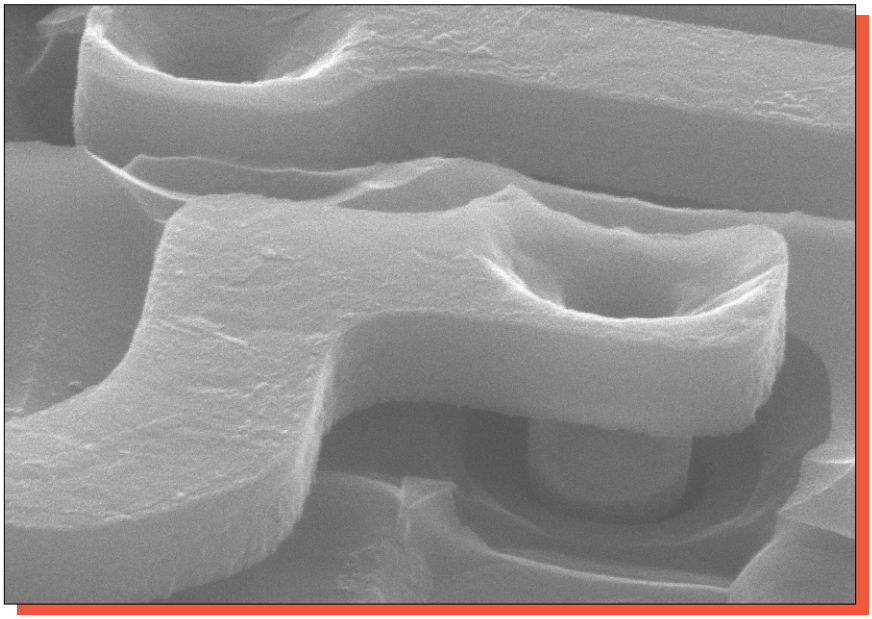


Figure 12. Topological SEM views of metal 1 patterning. Mag. 4200x, 0°.

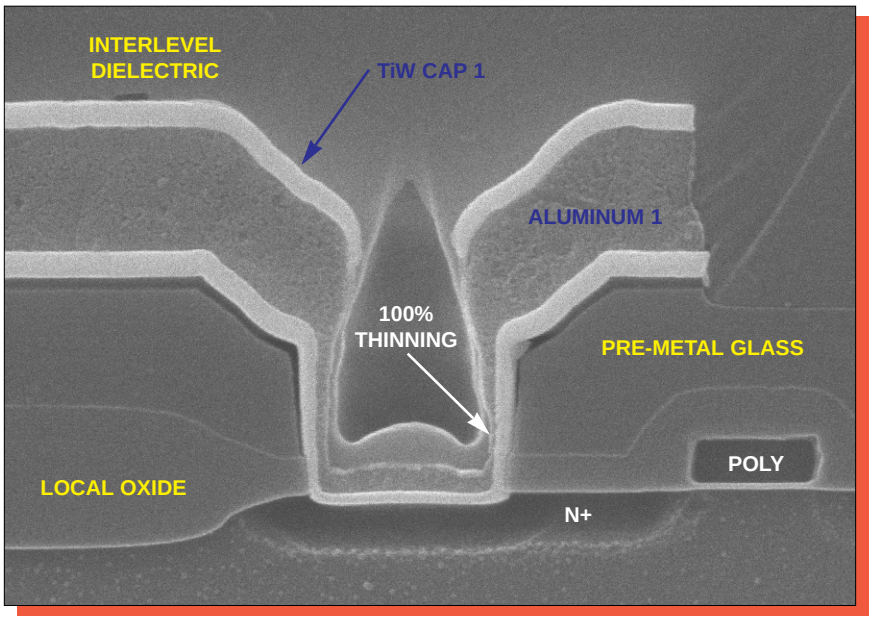


Mag. 7000x



Mag. 21,000x

Figure 13. SEM views of general metal 1 integrity.



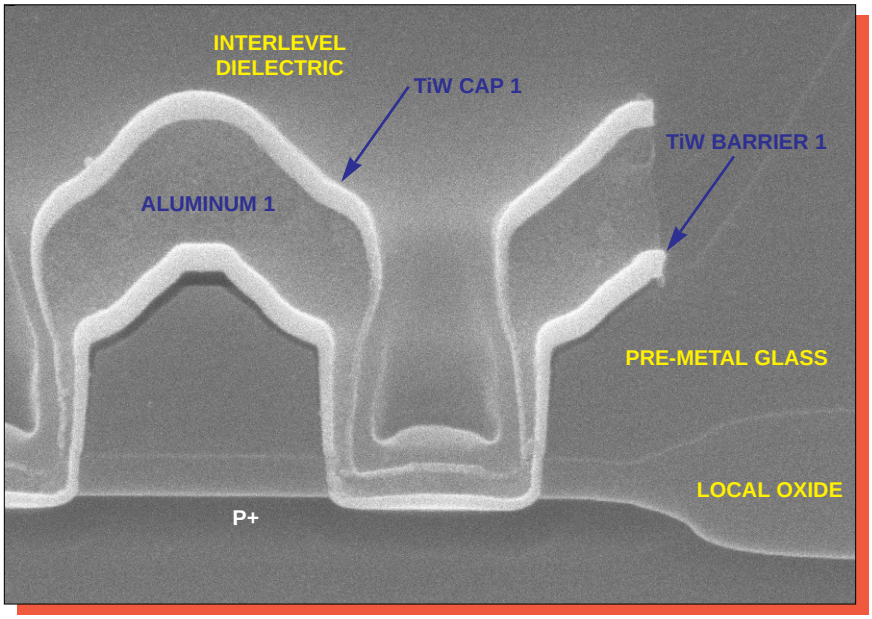
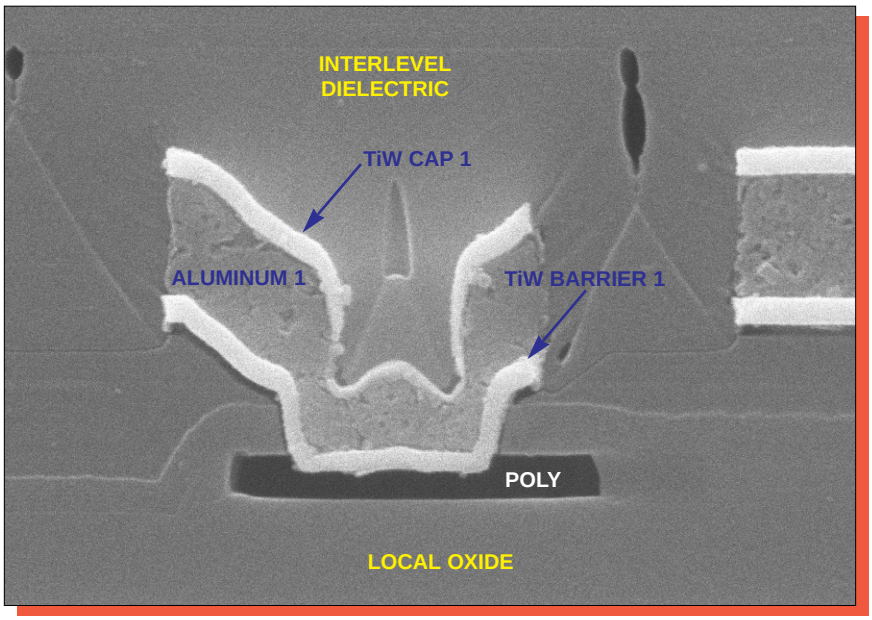
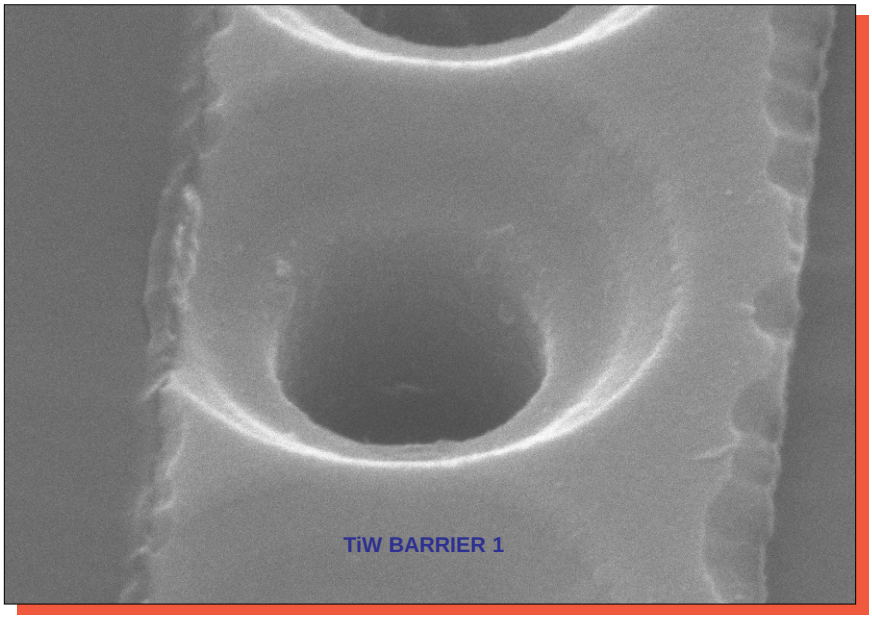


Figure 14. SEM section views of metal 1-to-diffusion contacts. Mag. 26,000x.

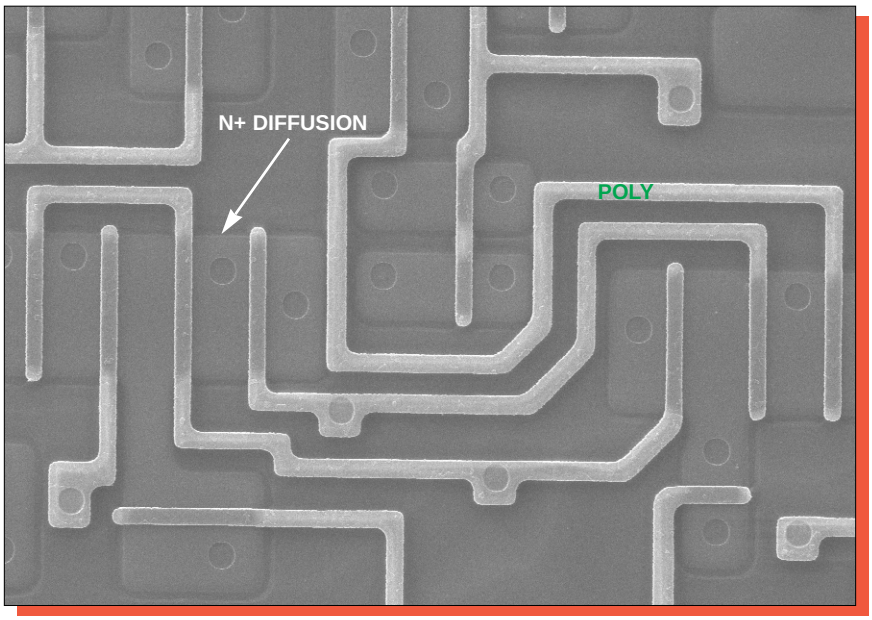


Mag. 26,000x

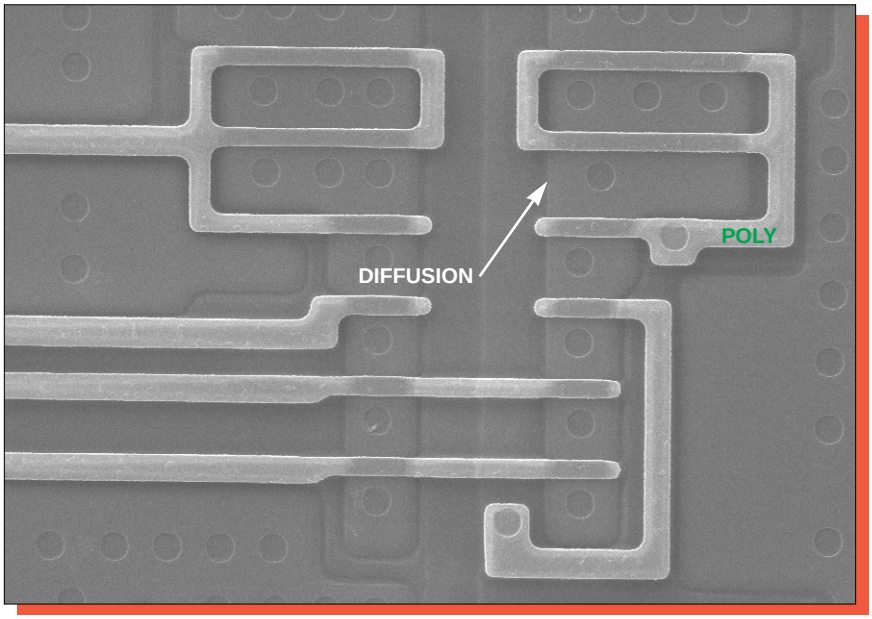


Mag. 40,000x

Figure 15. SEM section views of metal 1-to-poly and TiW barrier.

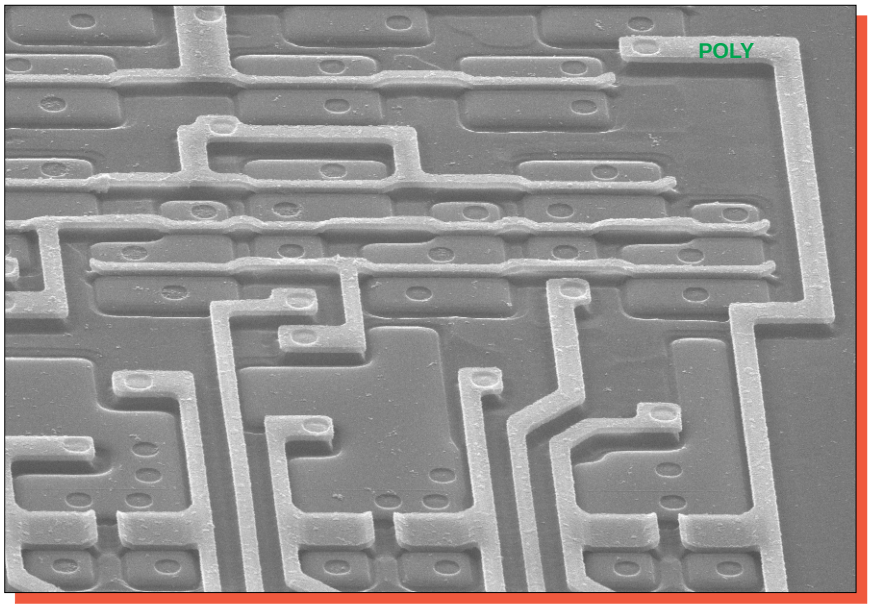


Mag. 3200x

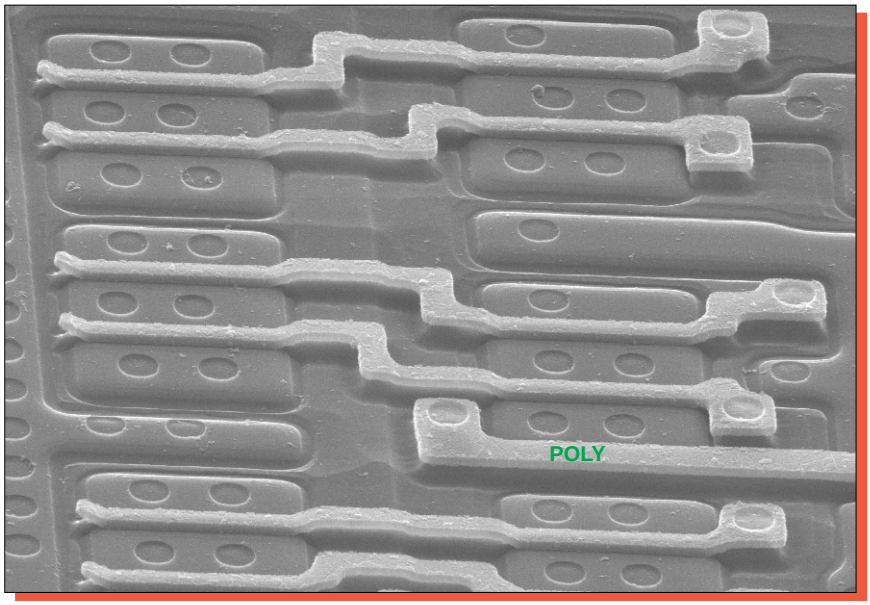


Mag. 3500x

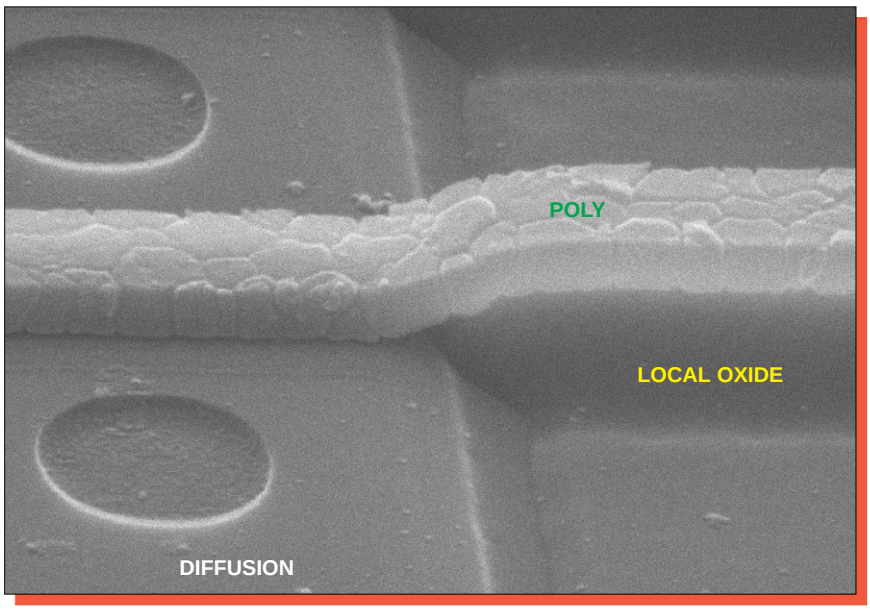
Figure 16. Topological SEM views of poly patterning. 0°.



Mag. 3500x

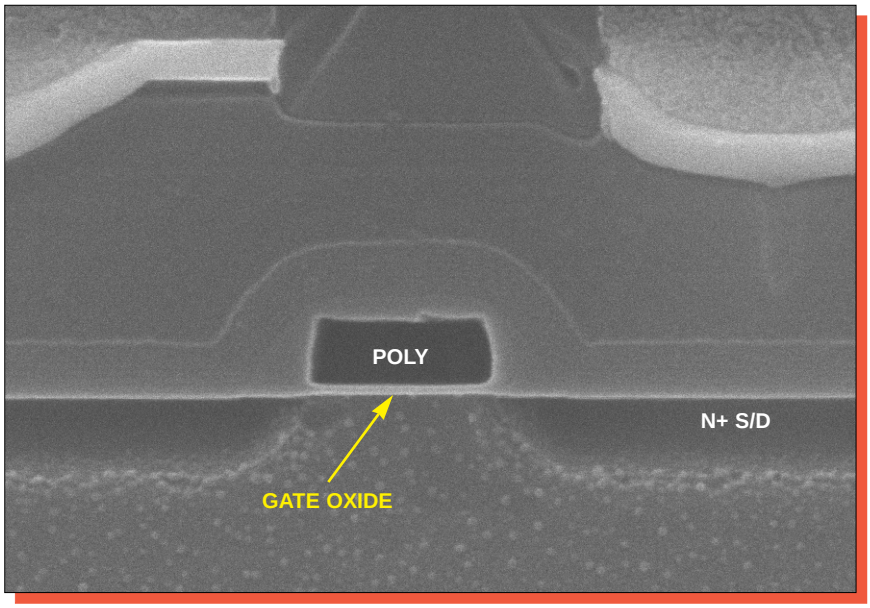


Mag. 5200x

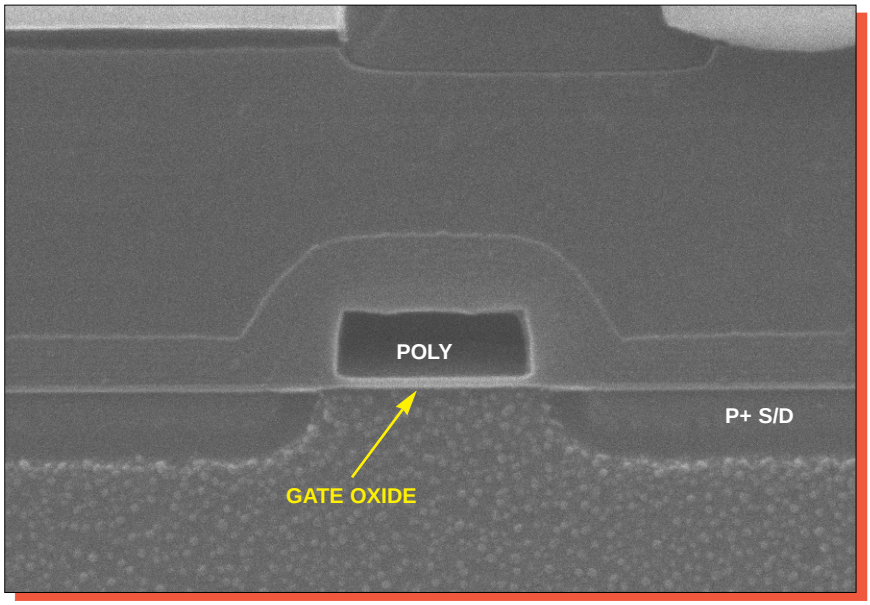


Mag. 30,000x

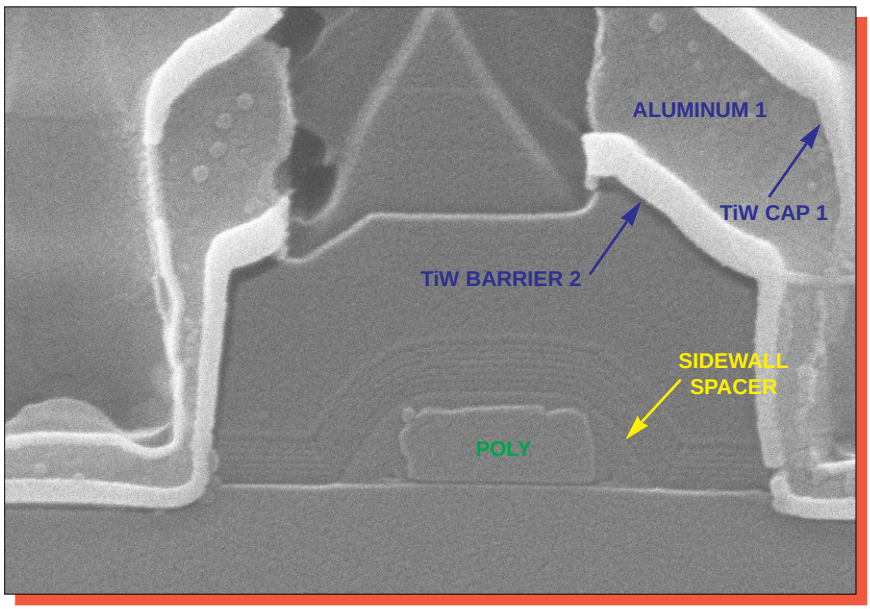
Figure 17. SEM views of poly coverage. 60.°



N-channel



P-channel



glass etch

Figure 18. SEM section views of typical gate structures. Mag. 40,000x.

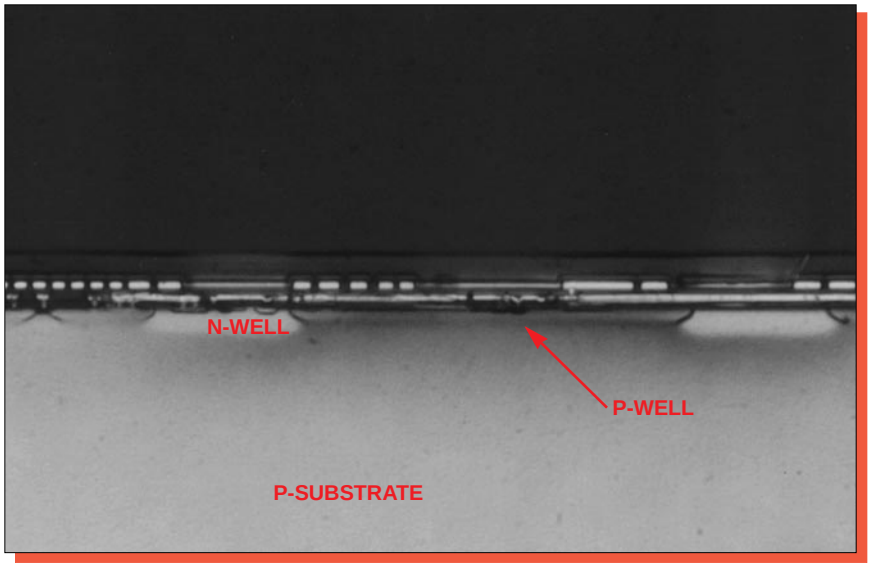
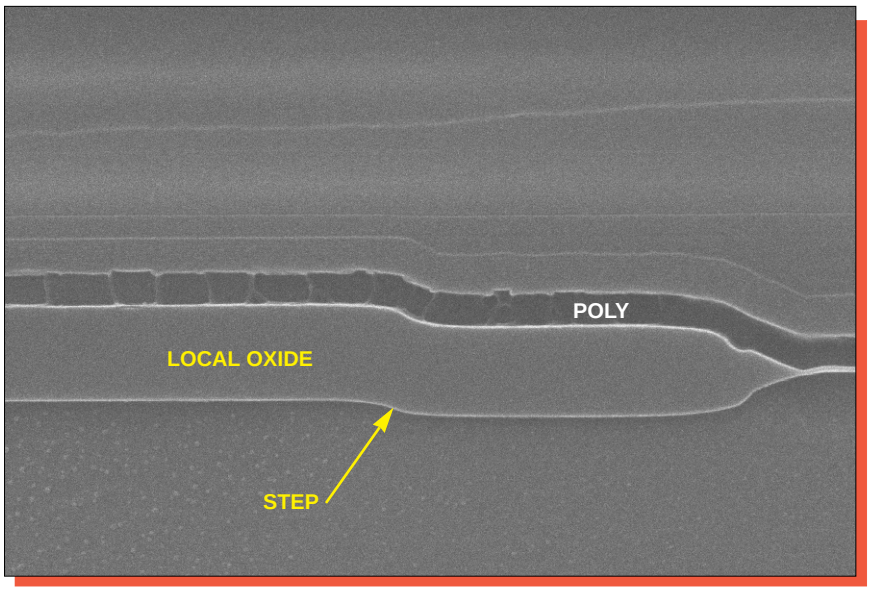
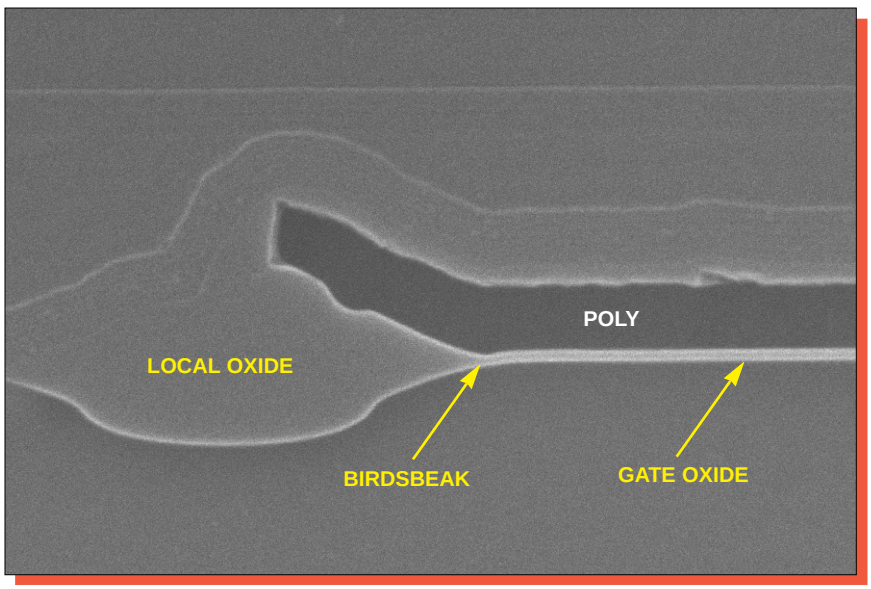


Figure 19. Optical view of the well structure. Mag. 800x.



Mag. 20,000x



Mag. 40,000x

Figure 20. SEM section views of step in local oxide and birdsbeak.

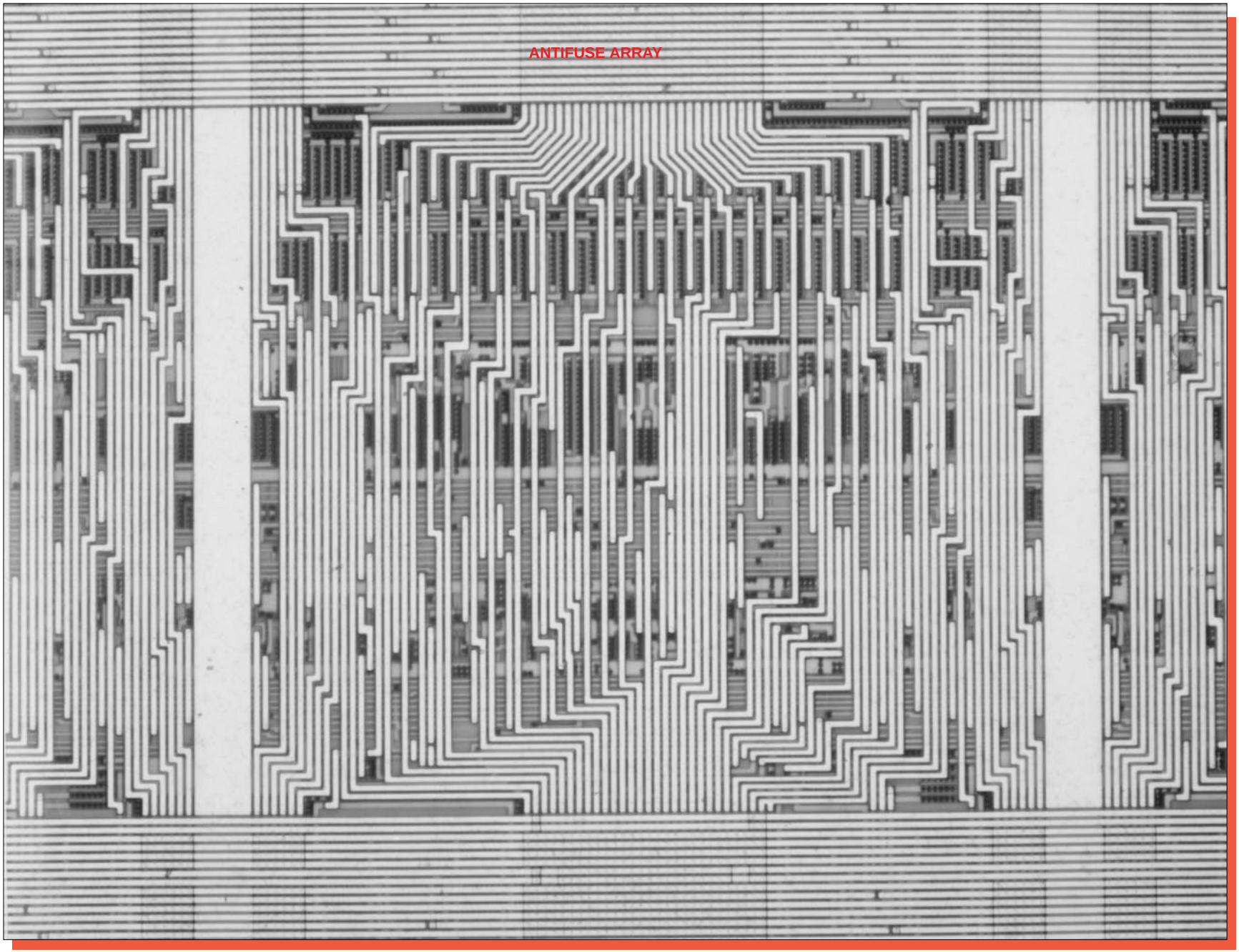


Figure 21. Optical view of typical device circuitry. Metal 2, Mag. 520x.

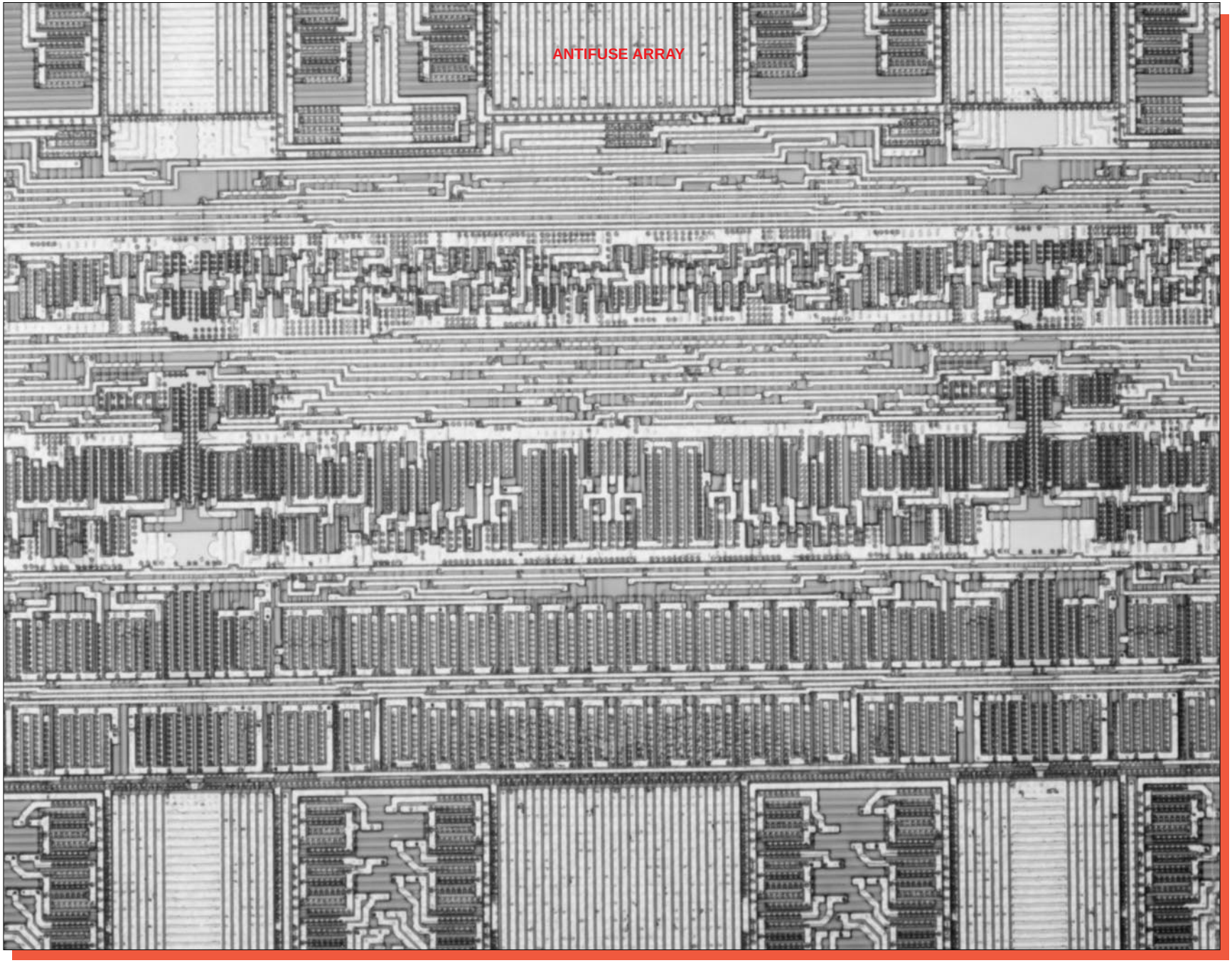


Figure 21a. Optical view of typical device circuitry. Metal 1, Mag. 520x.

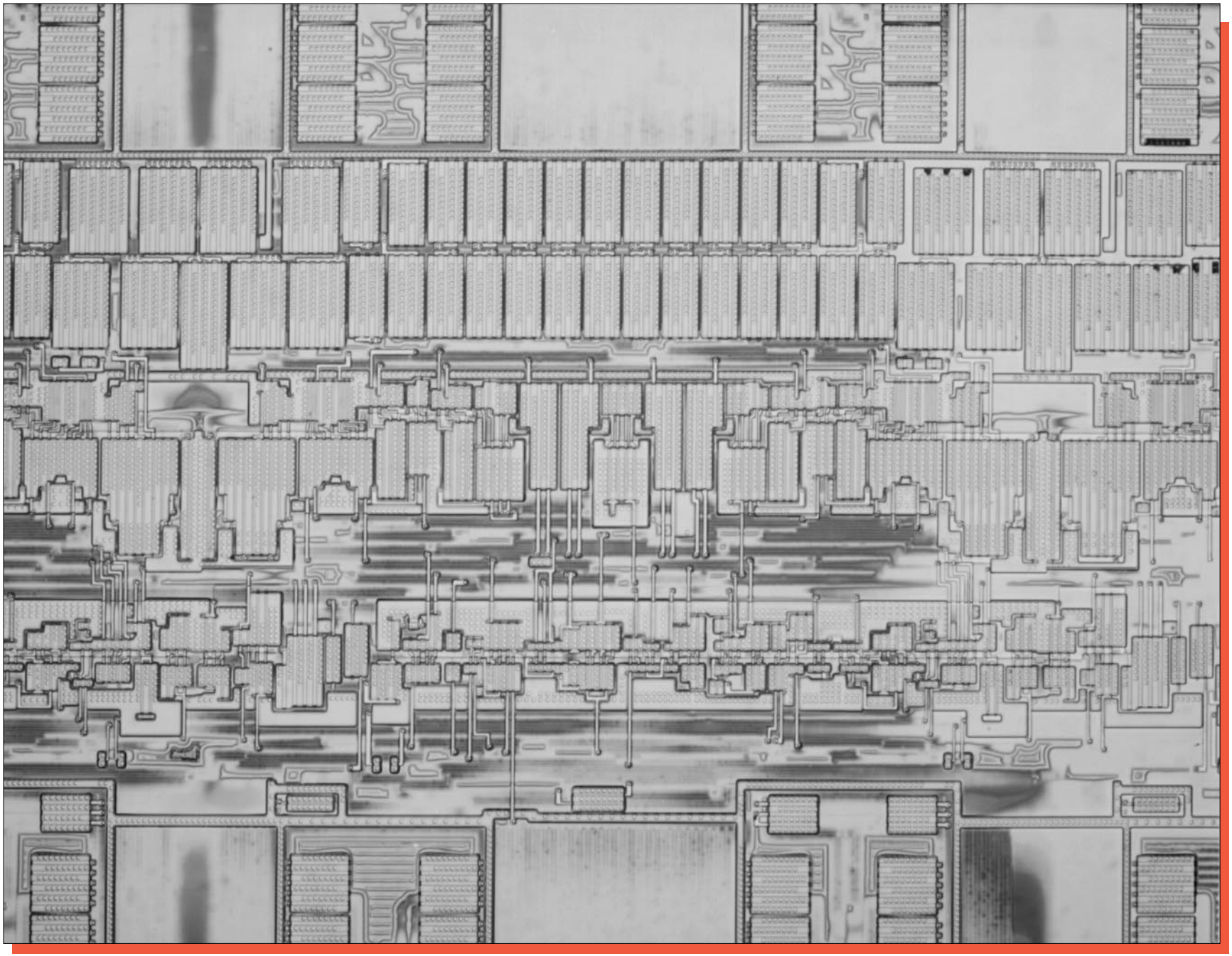
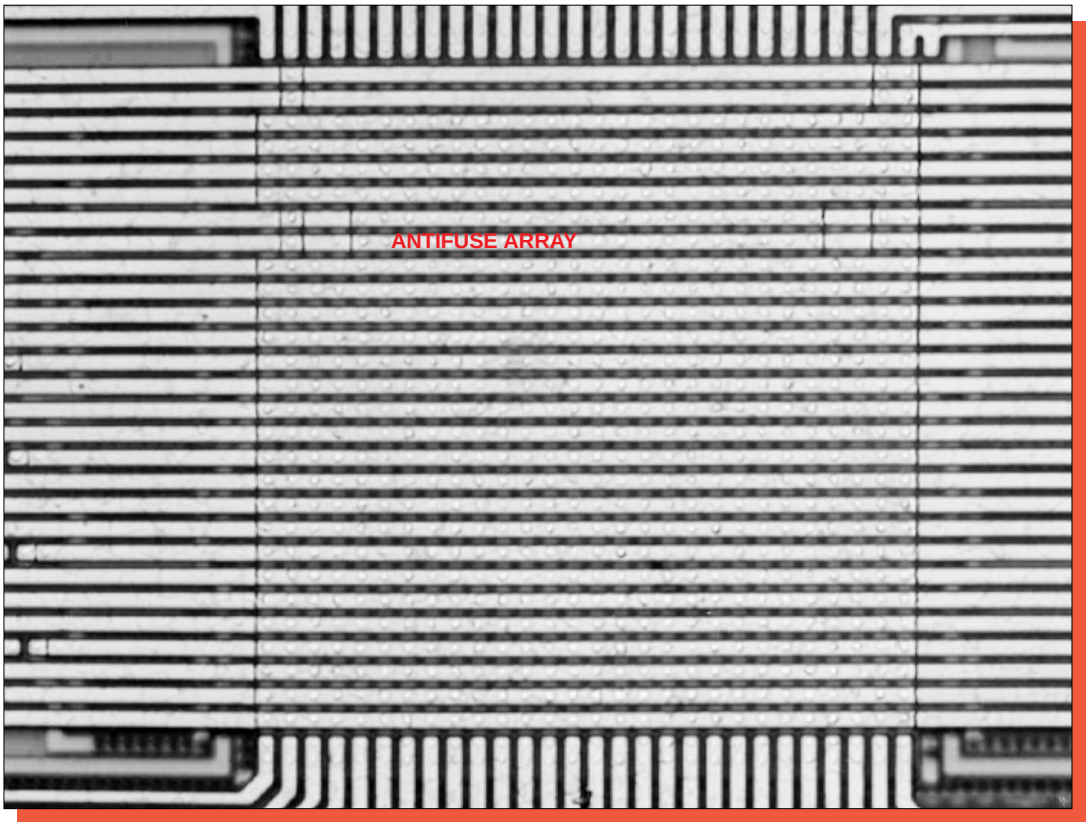
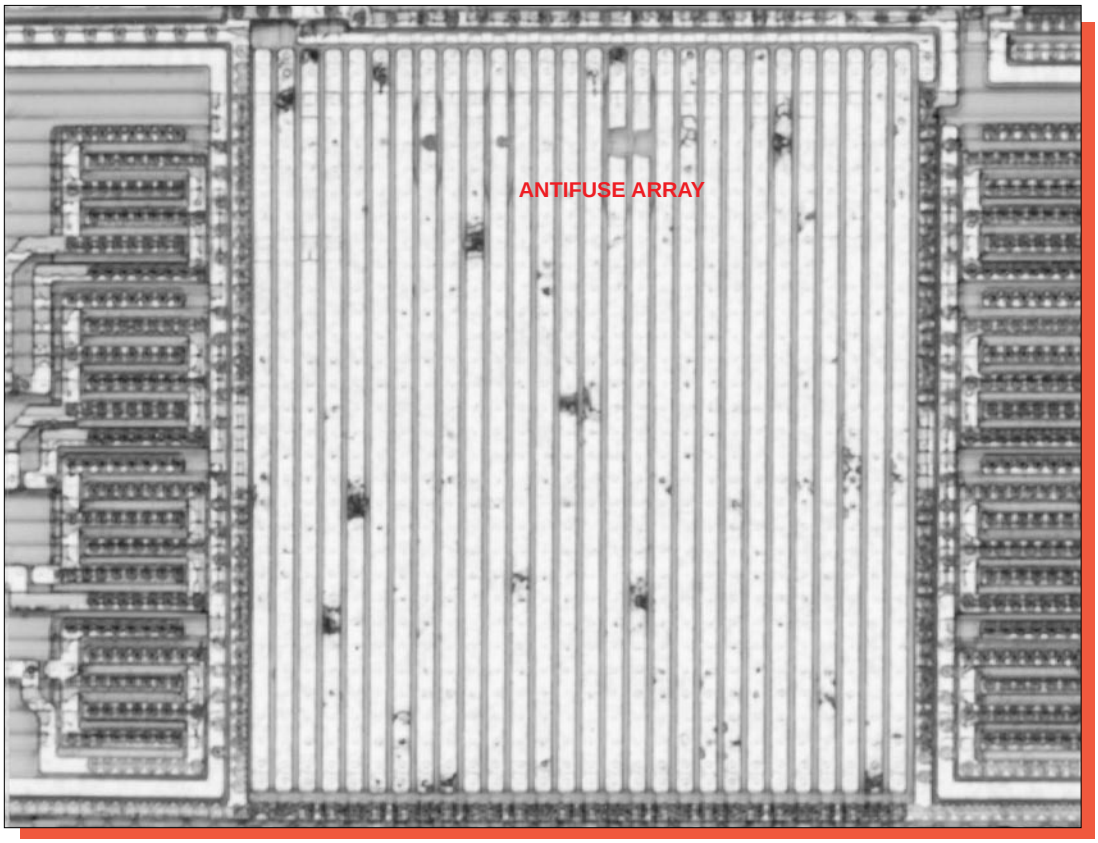


Figure 21b. Optical view of typical device circuitry. Poly, Mag. 520x.

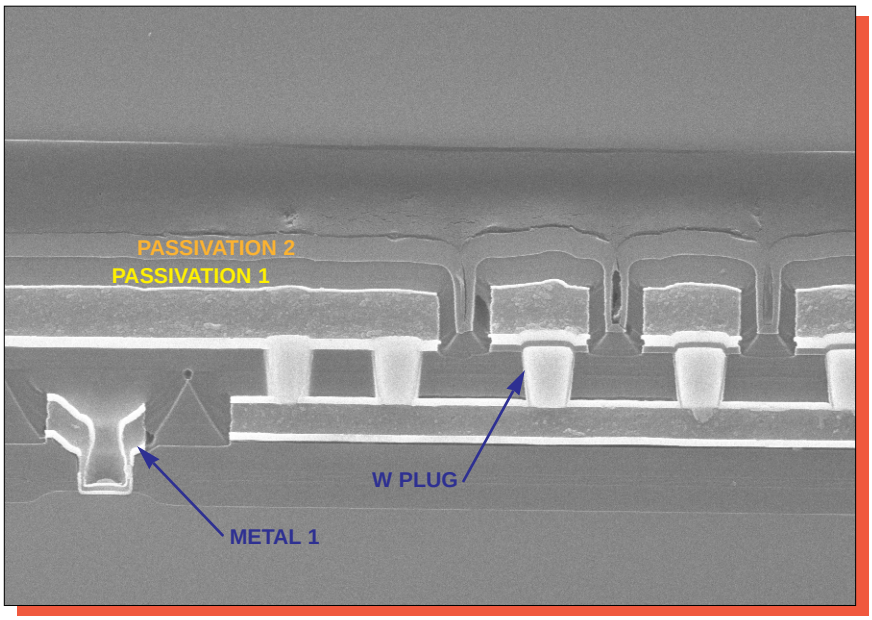


metal 2

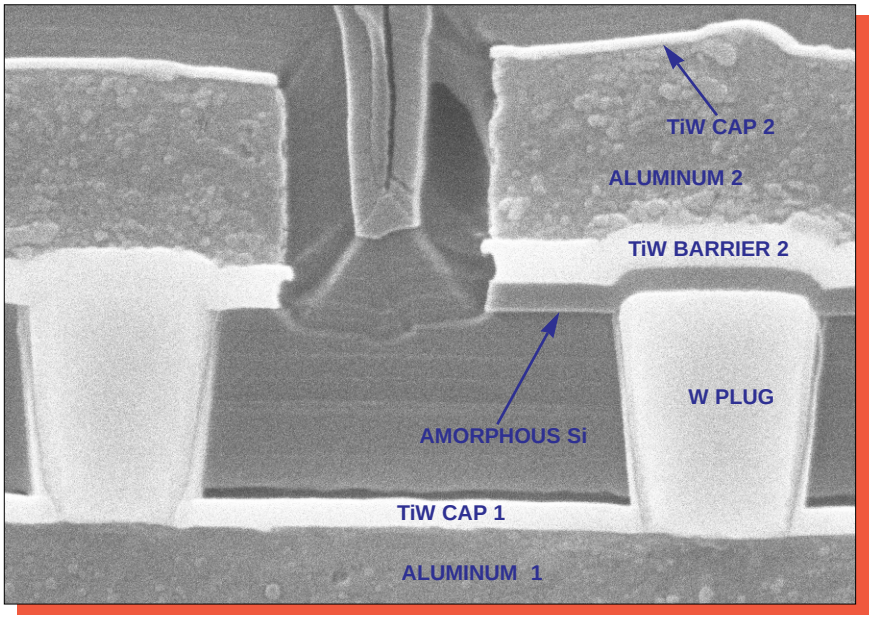


metal 1

Figure 22. Optical view of Quicklogic CMOS antifuse array. Mag. 1000x.

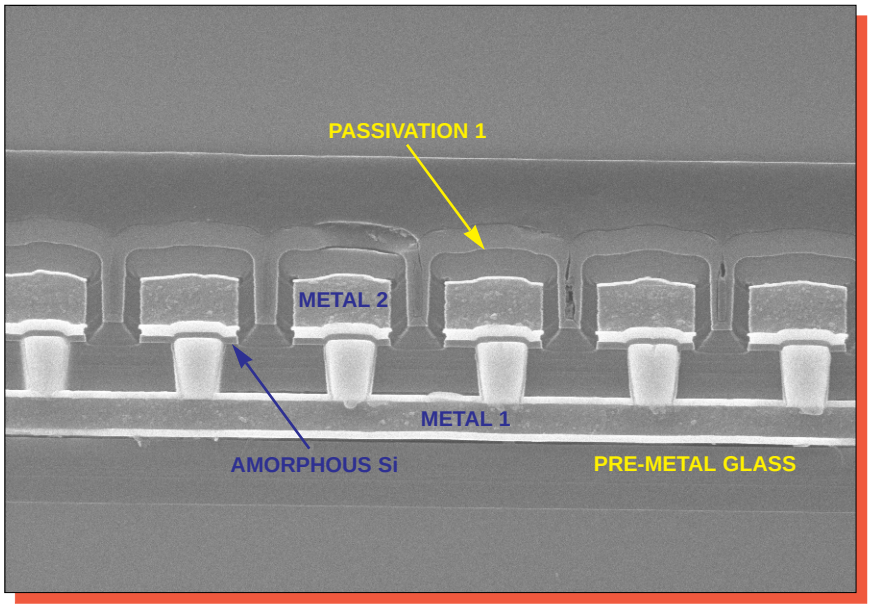


Mag. 6500x

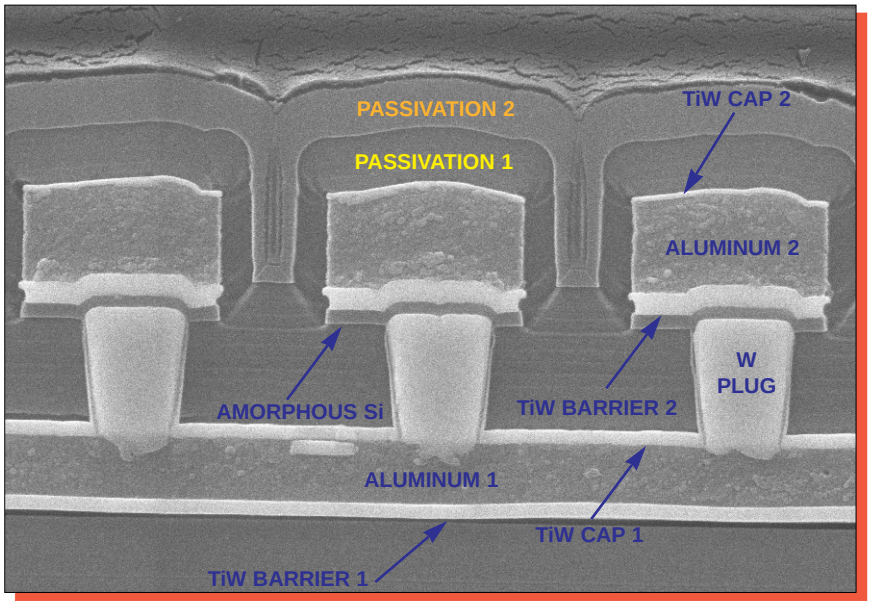


Mag. 26,000x

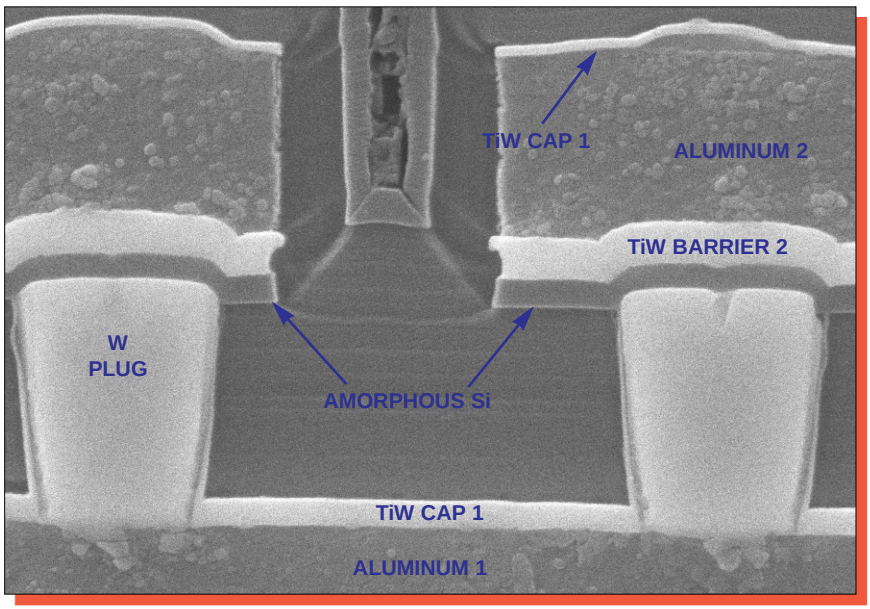
Figure 23. SEM section views of antifuse array.



Mag. 6500x



Mag. 13,000x



Mag. 26,000x

Figure 24. SEM section views of antifuse array.

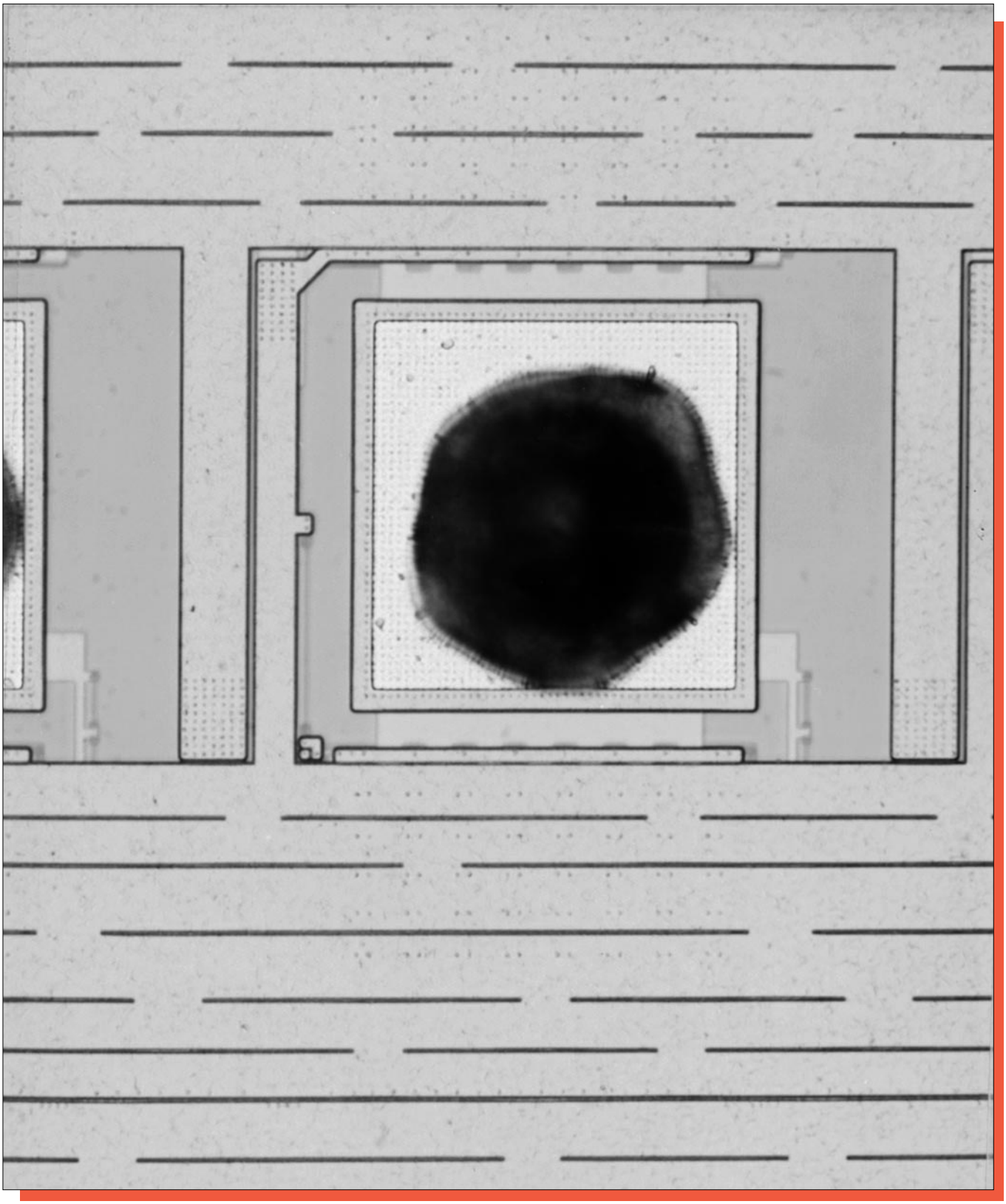


Figure 25. Optical view of the I/O layout. Metal 2, Mag. 640x.

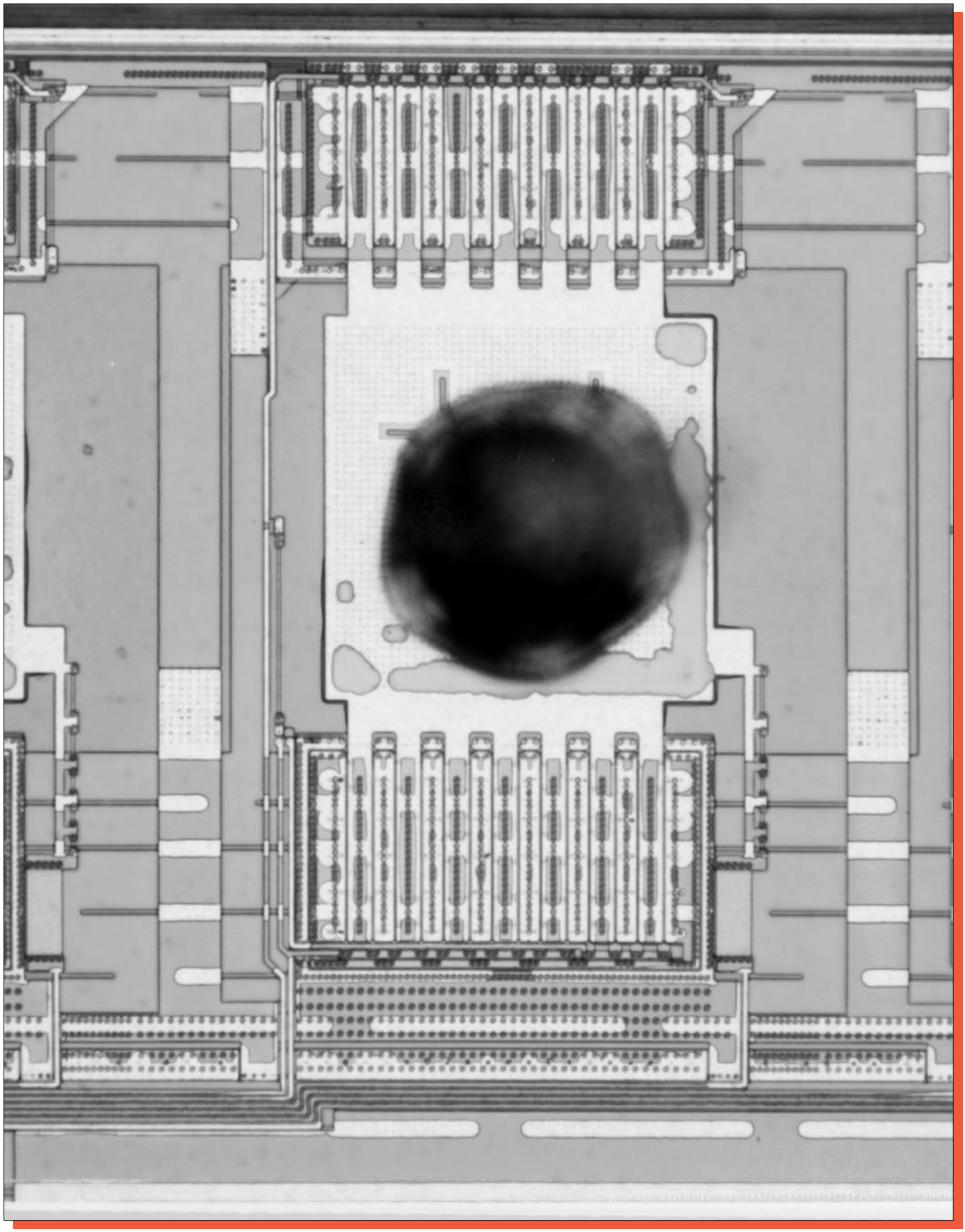


Figure 26. Optical view of the I/O layout. Metal 1, Mag. 640x.

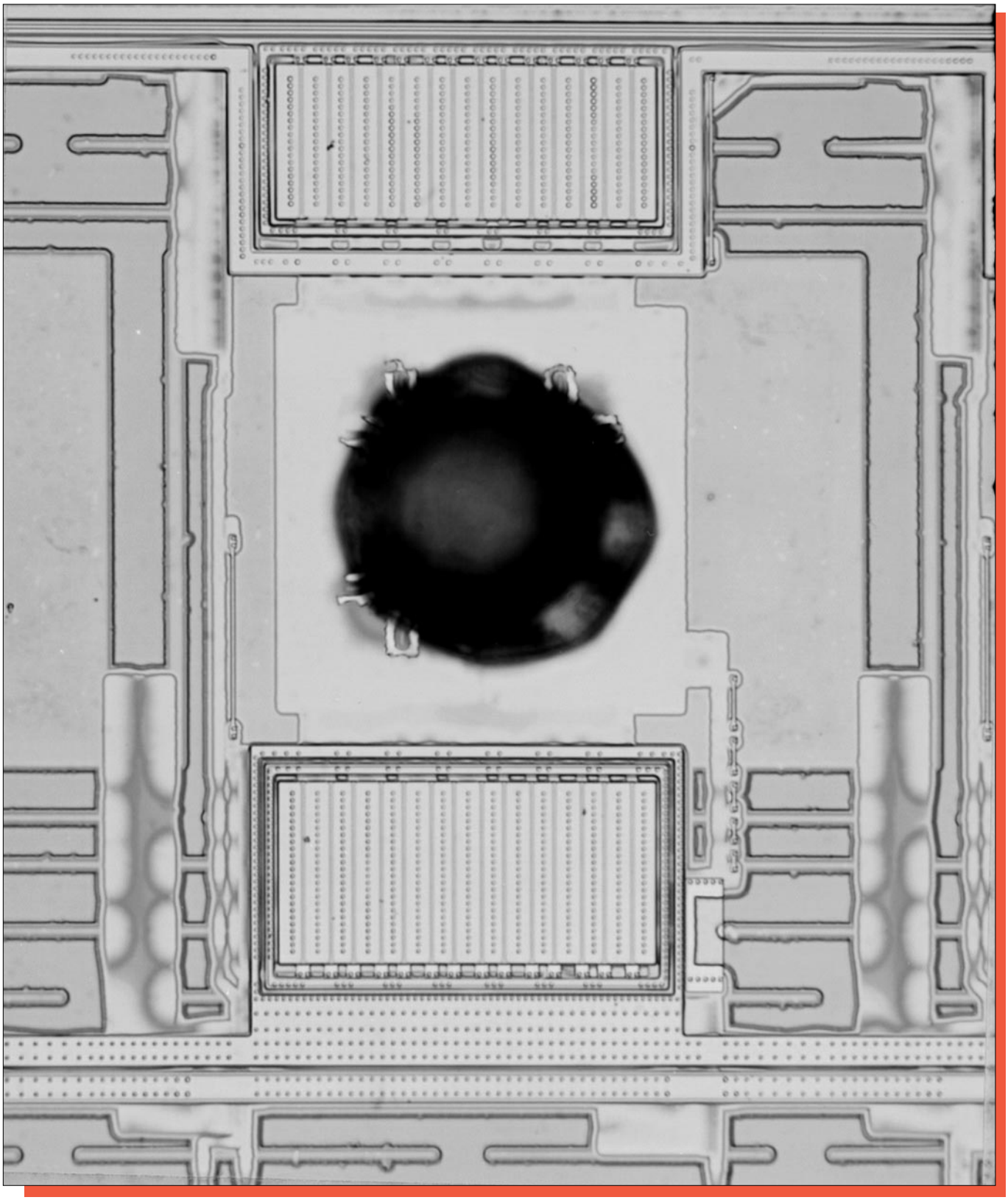
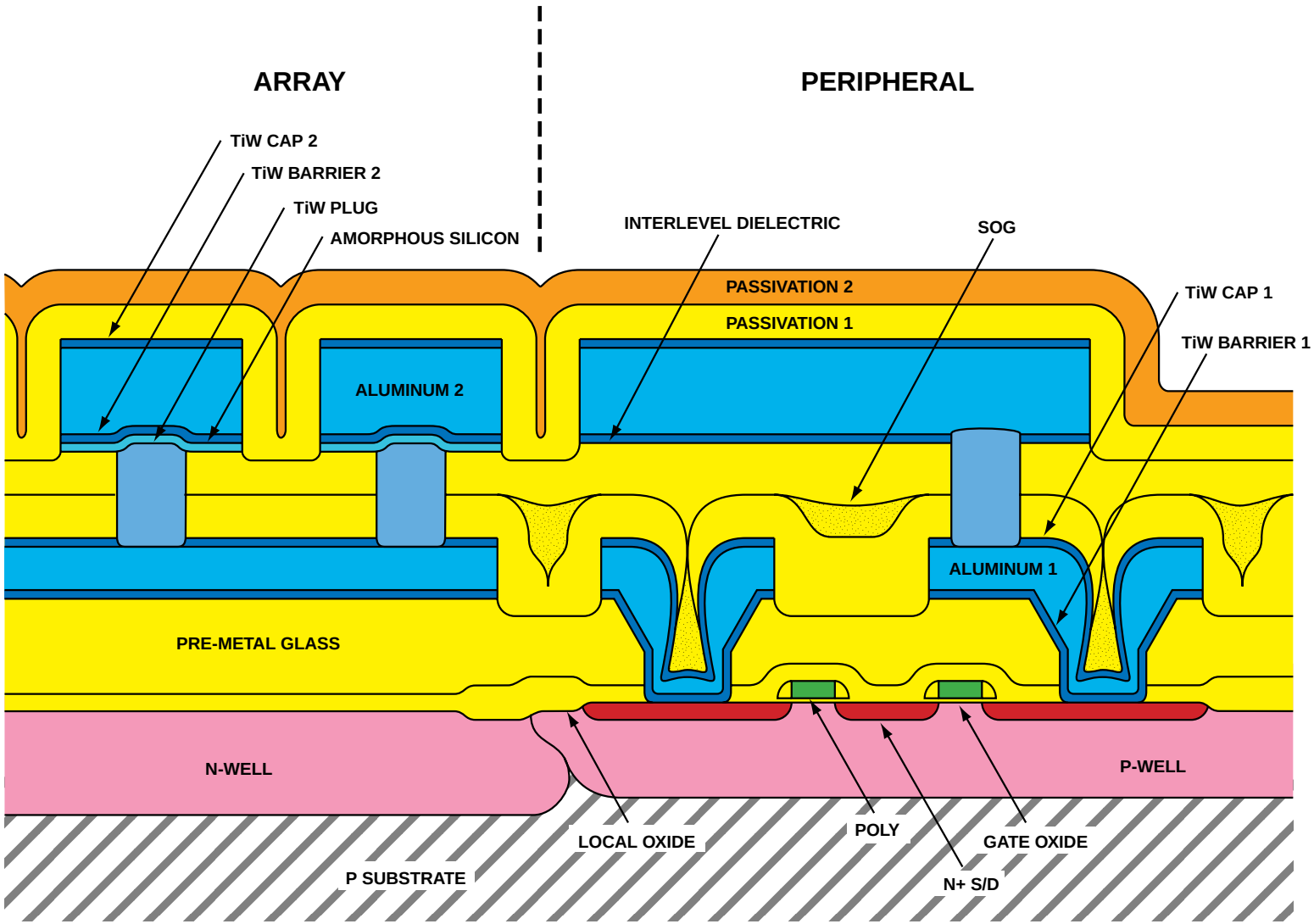


Figure 27. Optical view of the I/0 layout. Poly, Mag. 640x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 28. Color cross section drawing illustrating device structure.