Construction Analysis

Philips PZ5032-10A44
32 Macrocell PLD

Report Number: SCA 9611-501

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INTRODUCTION

This report describes a construction analysis of the Philips PZ5032-10A44 32 macrocell CPLD. Five devices packaged in 44-pin Plastic Leaded Chip Carriers (PLCCs) were received for the analysis. Devices were date coded 9622.

MAJOR FINDINGS

Questionable Items:[1] None. We found no deficiencies in the quality of process implementation.

Special Features:

- Twin-well CMOS process in an N substrate (no epi).
- Sub-micron gate lengths (0.35 micron N-channel and 0.4 micron P-channel).
- Tungsten plugs used under all metal layers.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 44-pin J-lead Plastic Leaded Chip Carriers (PLCCs) for surface mount applications.

- The leadframe was constructed of copper and plated externally with tin-lead solder and internally with silver.

- Lead-locking provisions (anchors) were present at all leads for added package strength.

- Die separation was by sawing (full depth). Silver-filled polyimide was used to attach the die to the paddle/header.

- Wirebonding was by the thermosonic ball bond method using 1.2 mil O.D. gold wire.

- All pins were connected and multiple bonds were present on pins 3, 22, 23, 30, 35, and 42 (VDD and GND).

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in an N substrate. No epi was used.

- No die coat was present.

- Passivation consisted of a layer of nitride over a thin layer of glass.

TECHNOLOGY DESCRIPTION (continued)

- Metallization consisted of three levels of metal. Each metal level consisted of aluminum with titanium-nitride cap and barrier. Tungsten plugs were used to form all vias and contacts.

- Interlevel dielectric consisted of four layers of silicon-dioxide with a planarizing glass (probably SOG) layer in between glasses 2 and 4. An etchback was performed prior to the deposition of the planarizing glass.

- Pre-metal dielectric consisted of a layer of reflow glass (probably BPSG) over various densified oxides. The glass was reflowed prior to contact cuts only.

- A single layer of polycide (tungsten silicide) was used to form all gates on the die and the top plates of all poly-to-diffusion capacitors. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with oxide sidewall spacers left in place. Very light and shallow implants were present in the capacitor areas of the EEPROM cells. Very thin tunnel oxide windows were used in these cells also.

- Local oxide (LOCOS) isolation was used. A step was present at the edge of the well which indicates a twin-well process was used.

- A specialized 10T SRAM cell design was used as part of the programmable elements. It employed the same process features as the rest of the die (at least to our ability to detect). The process used for the EEPROM cells appeared to differ only in the use of very thin tunnel oxide windows in the programming elements and a very shallow lightly doped diffusion under the polycide in the capacitor storage elements

- Redundancy fuses were not present.

ANALYSIS RESULTS I

Package and Assembly: **Figures 1 - 6**

Questionable Items:[1] None.

General Items:

- Devices were packaged in 44-pin J-lead Plastic Leaded Chip Carriers (PLCCs) for surface mount applications.

- Overall package quality: Good. No significant defects were found in the external or internal portions of the package. No cracks or voids were present.

- Leadframe: The leadframe was constructed of copper (Cu) and plated externally with tin-lead (Sn-Pb) solder and internally spot plated with silver (Ag). No voids or cracks were visible at lead exits.

- Die dicing: Die separation was by sawing (full depth) of normal quality. No large cracks or chips were present. A silver-filled polyimide was used to attach the die to the header. It was of normal thickness and the area was well controlled.

- Wirebonding was by the thermosonic ball bond method using 1.2 mil O.D. gold wire. Bond pull strengths were normal (see page 11). No bond lifts occurred. All three metal levels and multiple vias were used at bond pads. No problems are foreseen.

- All pins were connected and multiple bonds were present on pins 3, 22, 23, 30, 35, and 42 (VDD and GND).

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process: **Figures 7 - 40**

Questionable Items:[1] None.

Special Features:

- CMOS twin-well process in an N substrate (no epi).
- Sub-micron gate lengths (0.35 micron N-channel and 0.4 micron P-channel).
- Tungsten plugs were used for all vertical interconnect.

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in an N substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found.
- Die coat: No die coat was present.
- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good.
- Metallization: Three levels of metal. All consisted of aluminum with titanium-nitride caps and barriers. Tungsten plugs were used at all contacts and vias.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal patterning: All metal layers were patterned by a dry etch of normal quality. No problems were found in this area.

- Metal defects: No voiding, notching, or neckdown was noted in any of the metal layers. All tungsten plugs were completely filled. No silicon nodules were noted following the removal of any metal layer. Slotted metal bus lines were used to relieve stress.

- Metal step coverage: Virtually no metal thinning was present at any contacts or vias due to the presence of tungsten plugs.

- Interlevel dielectric consisted of four layers of silicon-dioxide with a planarizing glass (probably SOG) layer in between glasses 2 and 4. No problems were found in any of these layers. An etchback was performed prior to the deposition of the filler glass.

- Pre-metal dielectric: A layer of reflow glass (probably BPSG) over various densified oxides was used under metal 1. Reflow was performed prior to contact cuts only. No problems were found.

- Vias and contacts: Via and contact cuts were defined by a dry etch process. No significant over-etching of the contacts or vias was noted. The titanium-nitride barrier metal was present beneath the tungsten plugs.

- A single layer of polycide (tungsten silicide) was used to form all gates on the die and the top plates of all poly-to-diffusion capacitors. Direct poly-to-diffusion (buried) contacts were not used. Definition was by dry-etch of normal quality and no problems were found.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors and a shallow light implant in capacitor areas of the EEPROM cells. An

ANALYSIS RESULTS II (continued)

LDD process was used at gates with oxide sidewall spacers left in place. No problems were found.

- Local oxide (LOCOS) isolation was used. The step present at the well boundary indicates a twin-well process was employed. No problems were found here either.

- SRAM and EEPROM cells were present on the die to provide the programming capability.

  - 10T special SRAM. Metal 3 was used to form the "piggyback" word lines and the ϕ and $\overline{\phi}$ lines (via metals 2 and 1). Metal 2 was used to form the bit and output lines, and to distribute VDD and GND (via metal 1). Metal 1 was used to provide cell interconnect. Polycide was used to form all gates, and overall the process was the same as in peripheral circuits.

  - EEPROM. Metal 3 was not used in the cell. Metal 2 was used to form the "B" and bit lines, and to distribute GND (via metal 1). Metal 1 was used for the "A" and "piggyback" word lines. Polycide provided all gates and the top plates of all poly-to-diffusion capacitors. Programming is achieved through an ultra-thin tunnel oxide window.

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Decapsulate

Internal optical inspection

SEM of passivation

Passivation integrity test

Wirepull test

Passivation removal

SEM inspection of metal 3

Metal 3 removal and inspect barrier

Delayer to metal 2 and inspect

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good.

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver-filled polyimide
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.2 mil gold wire.

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	N
Metal registration	G
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (TOP)

PHILIPS LOGO
PZ5032 - 10A44
KRK75359622h -

(BOTTOM)

KRK7535
9622

WIREBOND STRENGTH

Wire material:	1.2 mil O.D. gold
Die pad material:	aluminum
Material at package lands:	silver

# of wires pulled:	20
Bond lifts:	0
Force to break - high:	12.5g
- low:	9.5g
- avg.:	10.9g
- std. dev.:	1.3

DIE MATERIAL ANALYSIS

Overlay passivation:	A layer of nitride over a layer of silicon-dioxide.
Metallization 3:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Plugs:	Tungsten (W).
Poly:	Tungsten (W) silicide.

HORIZONTAL DIMENSIONS

Die size:	2.3 x 5.2 mm (90 x 205 mils)
Die area:	12.0 mm^2 (18,400 $mils^2$)
Min pad size:	0.01 x 0.01 mm (3.9 x 3.9 mils)
Min pad window:	0.09 x 0.09 mm (3.5 x 3.5 mils)
Min pad space:	0.04 mm (1.5 mils)
Min metal 3 width:	0.7 micron
Min metal 3 space:	0.85 micron
Min metal 3 pitch:	1.55 micron
Min via 2 size (M3-to-M2):	0.75 micron
Min metal 2 width:	0.7 micron
Min metal 2 space:	0.8 micron
Min metal 2 pitch:	1.5 micron
Min via 1 size (M2- to-M1):	0.75 micron
Min metal 1 width:	0.65 micron
Min metal 1 space:	0.6 micron
Min metal 1 pitch:	1.25 micron
Min metal 1 plug size:	0.6 micron
Min poly width:	0.35 micron
Min poly space:	0.5 micron
Min poly pitch:	0.85 micron
Min gate poly to contact space:	0.3 micron
Min gate length* - (N-channel):	0.35 micron
- (P-channel):	0.4 micron
SRAM cell pitch:	3.0 x 28.5 microns
SRAM cell size:	85.5 $microns^2$
EEPROM cell pitch:	9.6 x 10.6 microns
EEPROM cell size:	101.8 $microns^2$

**Physical gate length*

VERTICAL DIMENSIONS

Layers:

Passivation 2:		0.6 micron
Passivation 1:		0.15 micron
Metal 3 - cap:		0.05 micron (approximate)
- aluminum:		0.9 micron
- barrier:		0.08 micron (approximate)
Interlevel dielectric 2	- glass 2 - 4:	0.2 micron
	- glass 2 - 3 (SOG):	0.0 - 0.6 micron
	- glass 2 - 2:	0.3 - 0.4 micron
	- glass 2 - 1:	0.15 micron
Metal 2 - cap:		0.15 micron
- aluminum:		0.45 micron
- barrier:		0.08 micron (approximate)
Interlevel dielectric 1	- glass 1 - 4:	0.2 micron
	- glass 1 - 3 (SOG):	0.0 - 0.6 micron
	- glass 1 - 2:	0.1 - 0.2 micron
	- glass 1 - 1:	0.15 micron
Metal 1 - cap:		0.15 micron
- aluminum:		0.45 micron
- barrier:		0.1 micron
Pre-metal dielectric:		0.65 micron (average)
Oxide on poly:		0.2 micron
Poly - silicide:		0.1 micron
- poly:		0.12 micron
Local oxide:		0.4 micron
N+ S/D:		0.15 micron
P + S/D:		0.15 micron
N-well:		Could not delineate
P-well:		2.5 microns (approximate)

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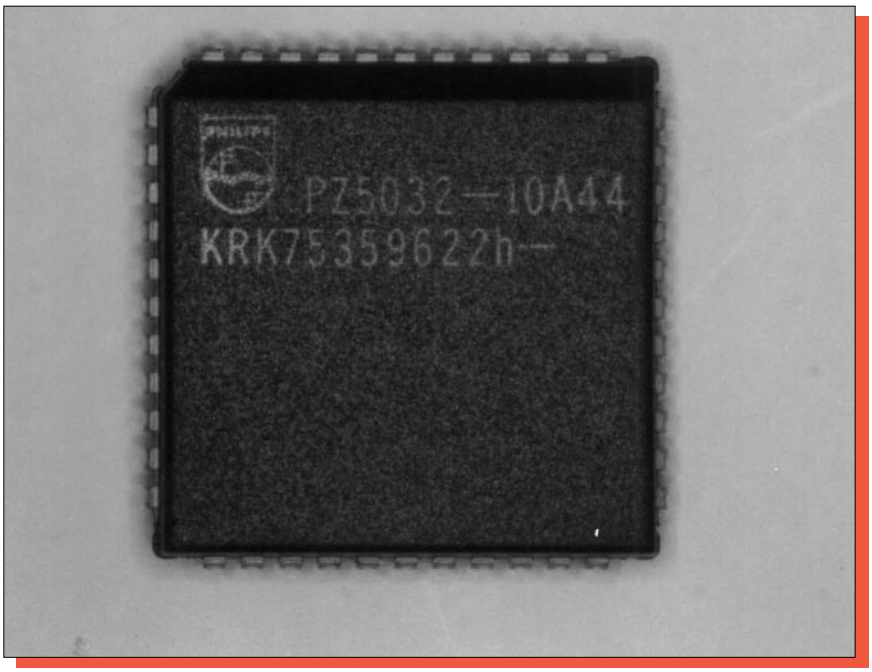


Figure 1. Optical views of the package. Mag. 4x.

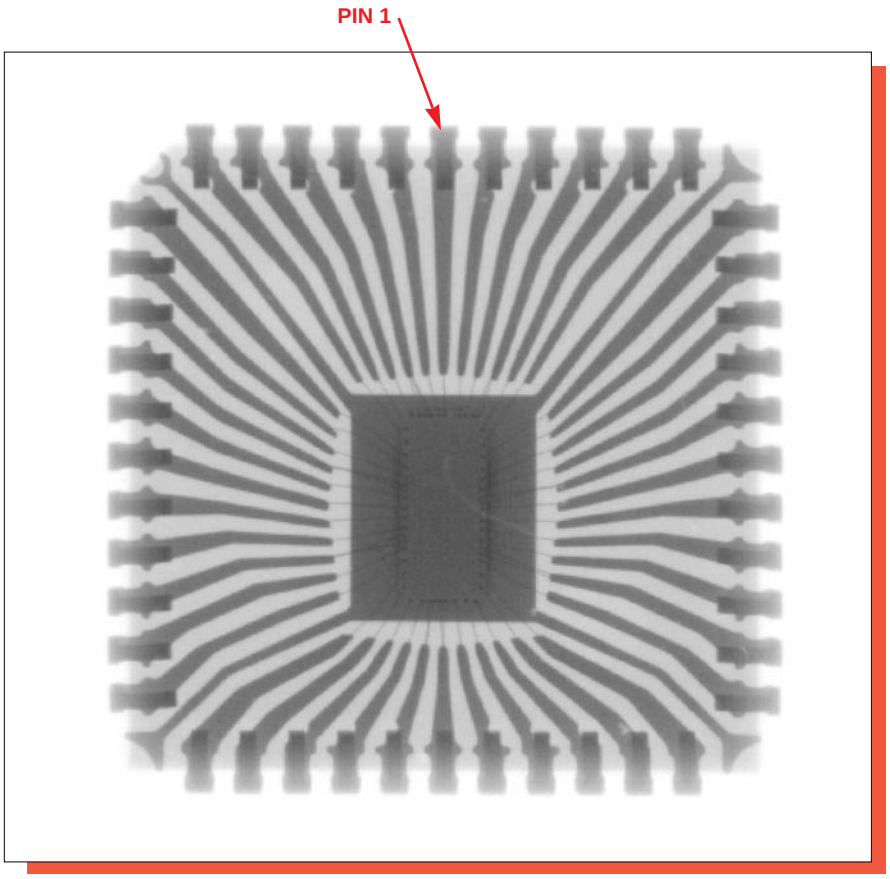
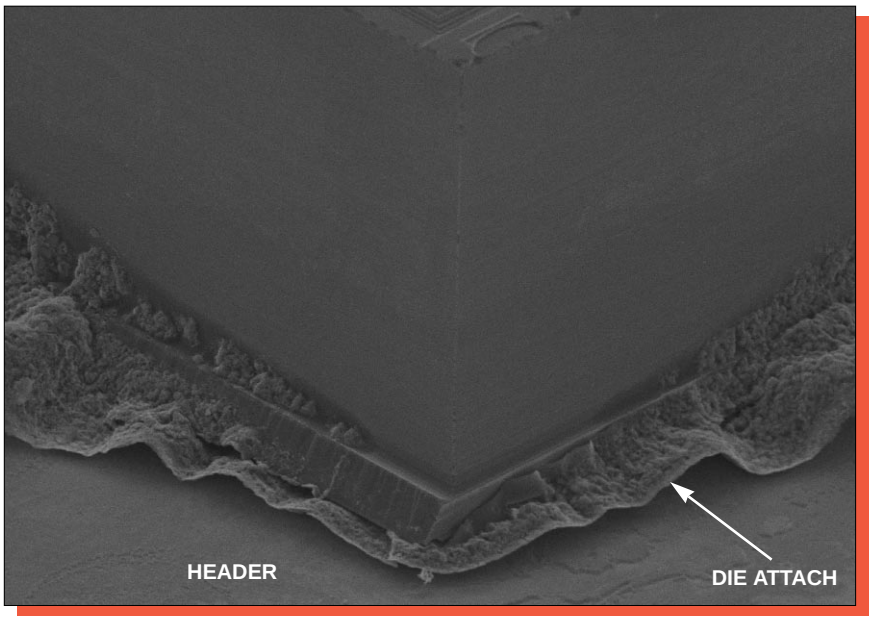
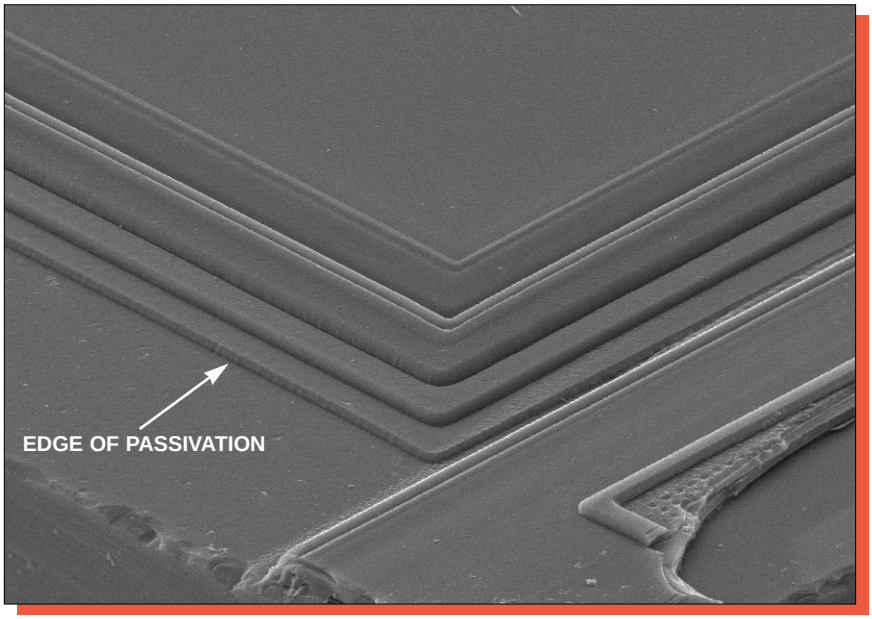


Figure 2. X-ray view of the package. Mag. 5x.

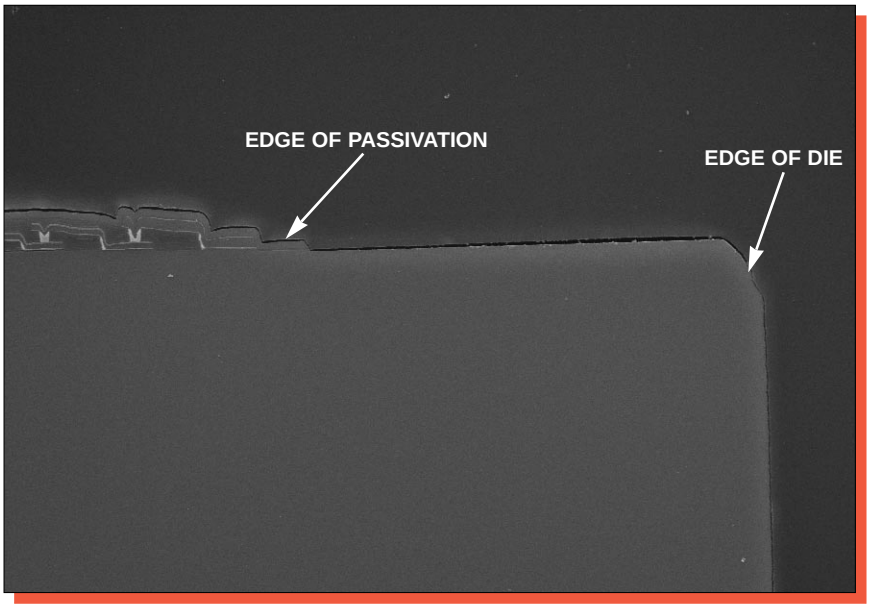


Mag. 150x

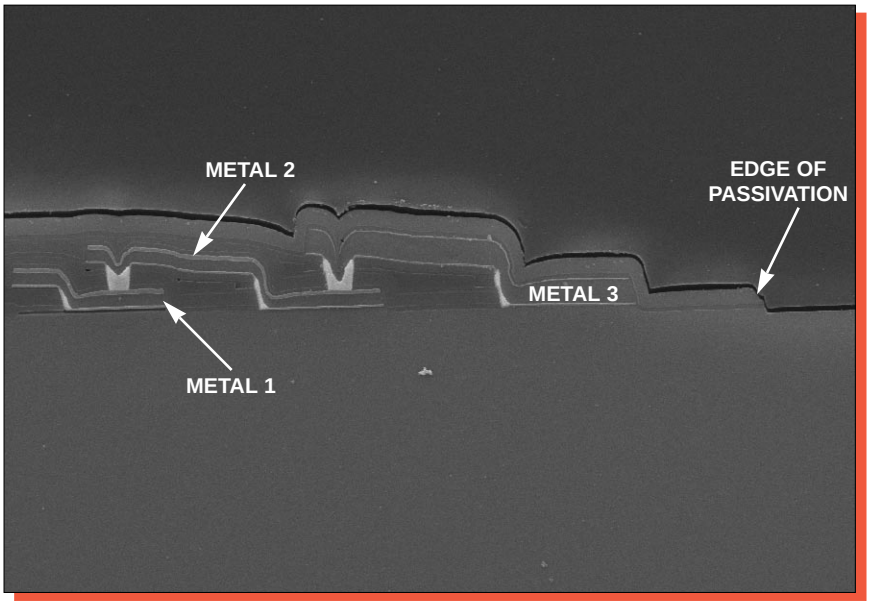


Mag. 1100x

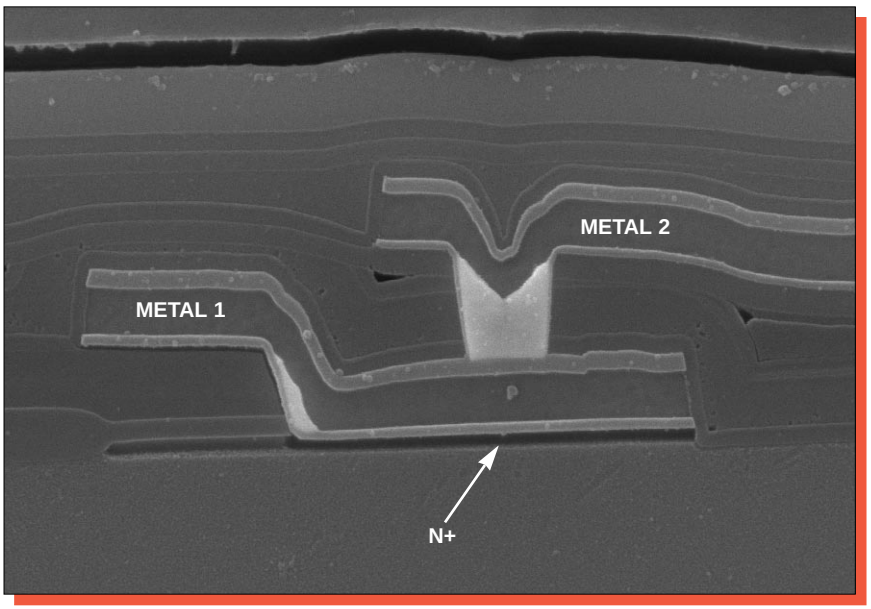
Figure 3. Optical views illustrating dicing, die attach, and edge seal. 60°.



Mag. 1400x

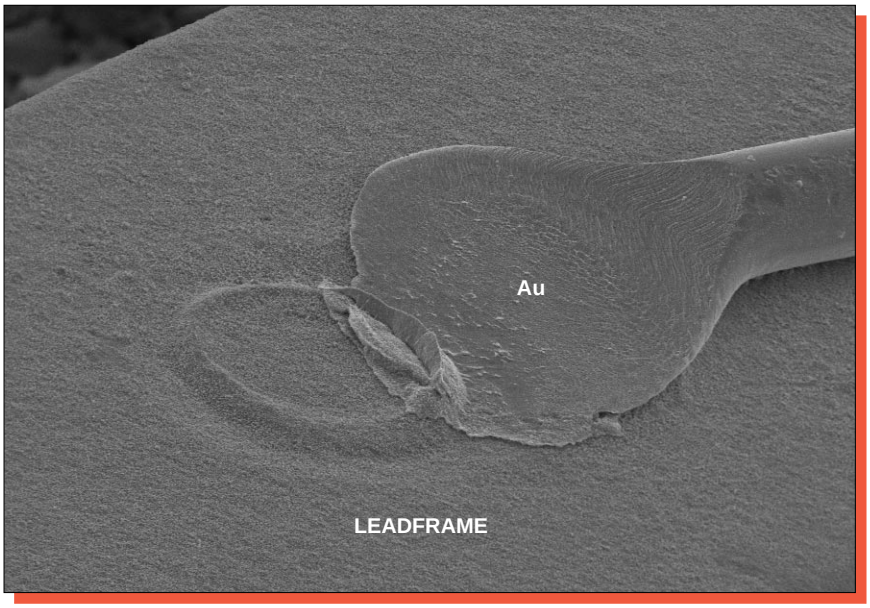


Mag. 3200x

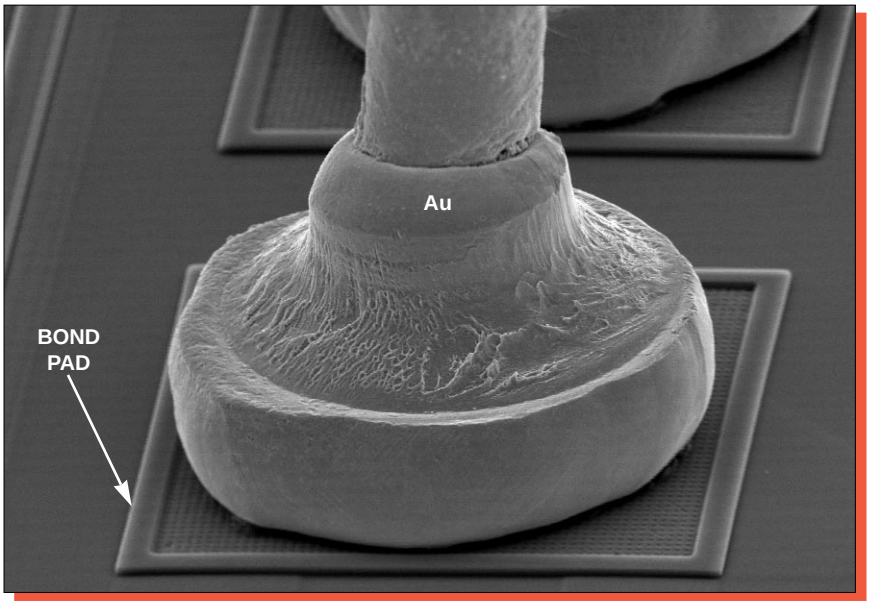


Mag. 13,000x

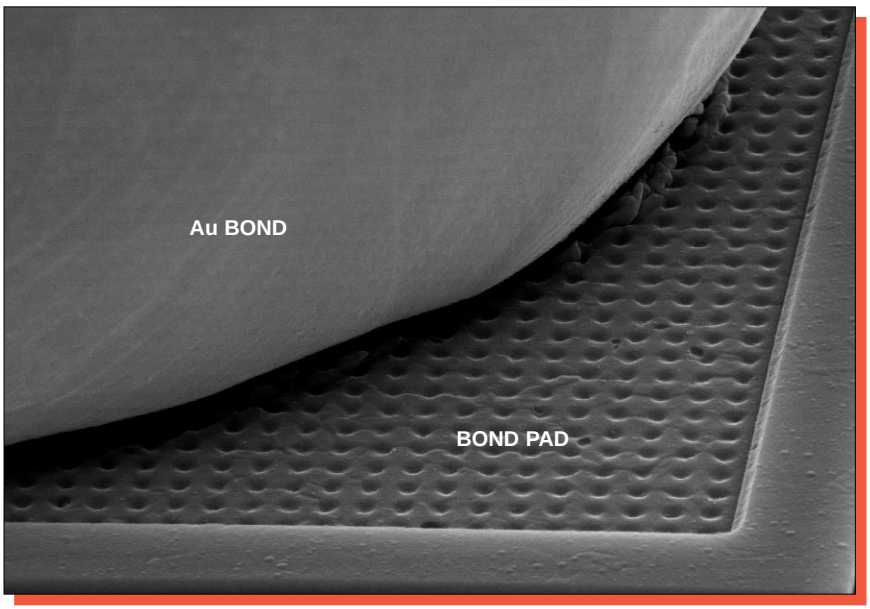
Figure 4. SEM section views of the edge seal.



Mag. 550x

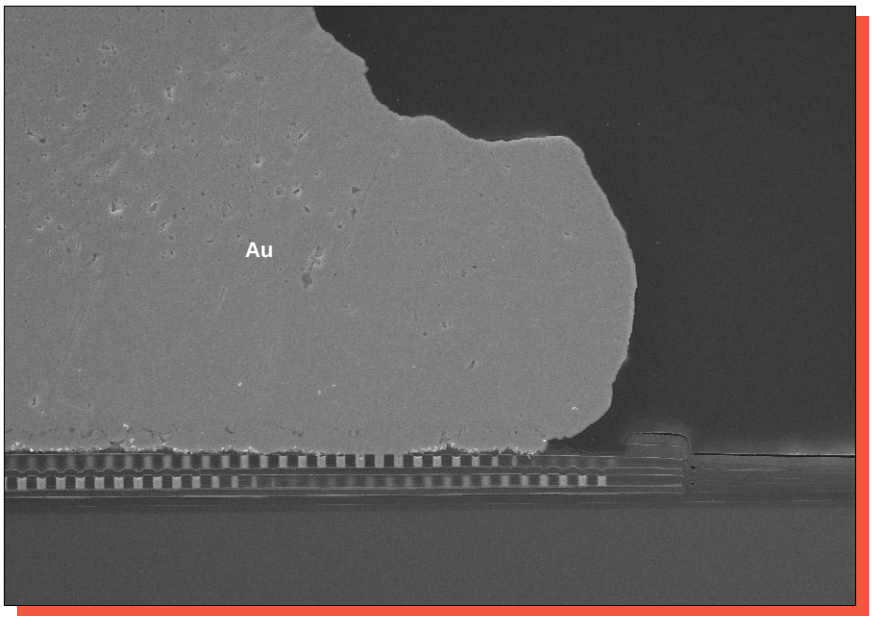


Mag. 775x

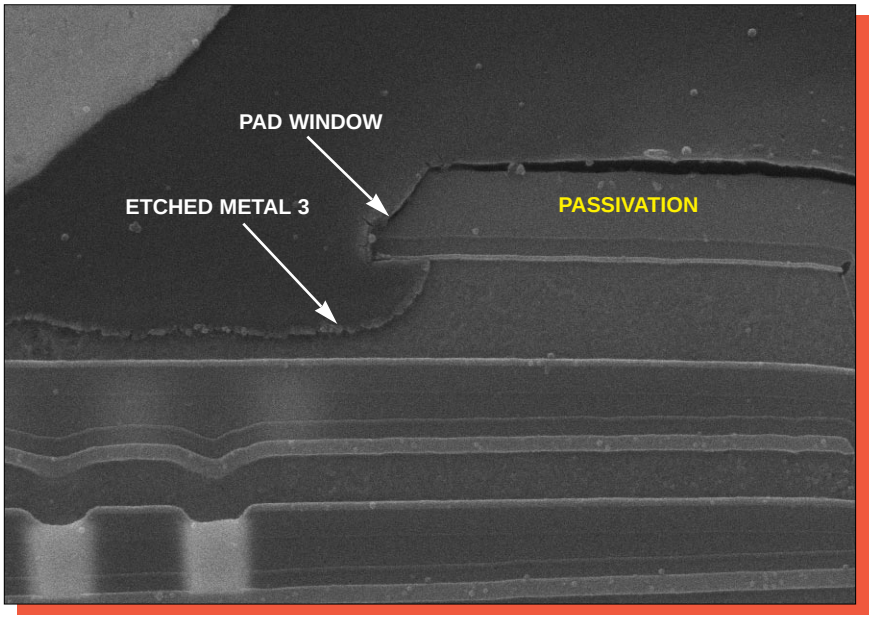


Mag. 3100x

Figure 5. SEM views of typical wirebonds. 60°.



Mag. 1600x



Mag. 13,000x

Figure 6. SEM section views of the bond pad structure.

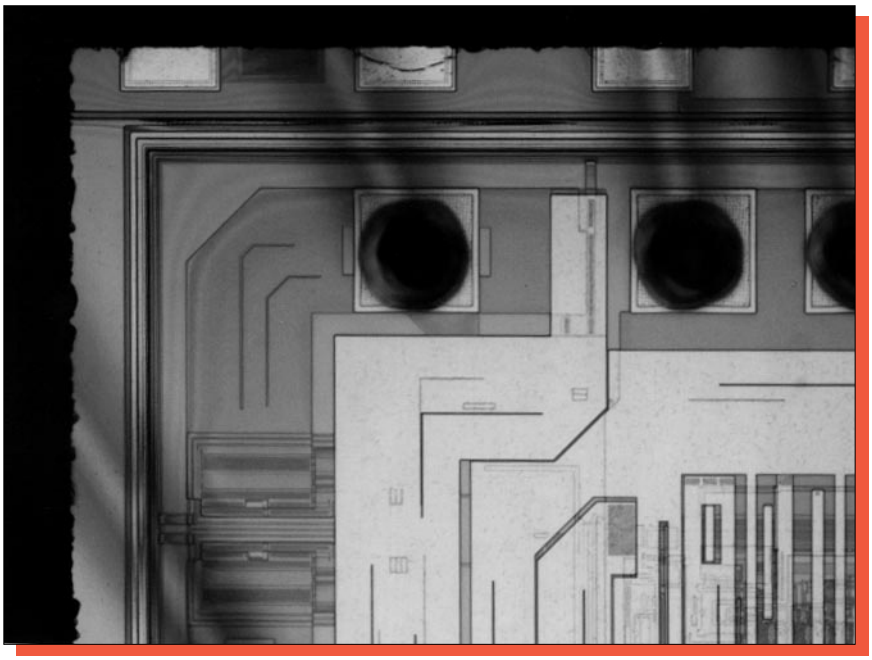
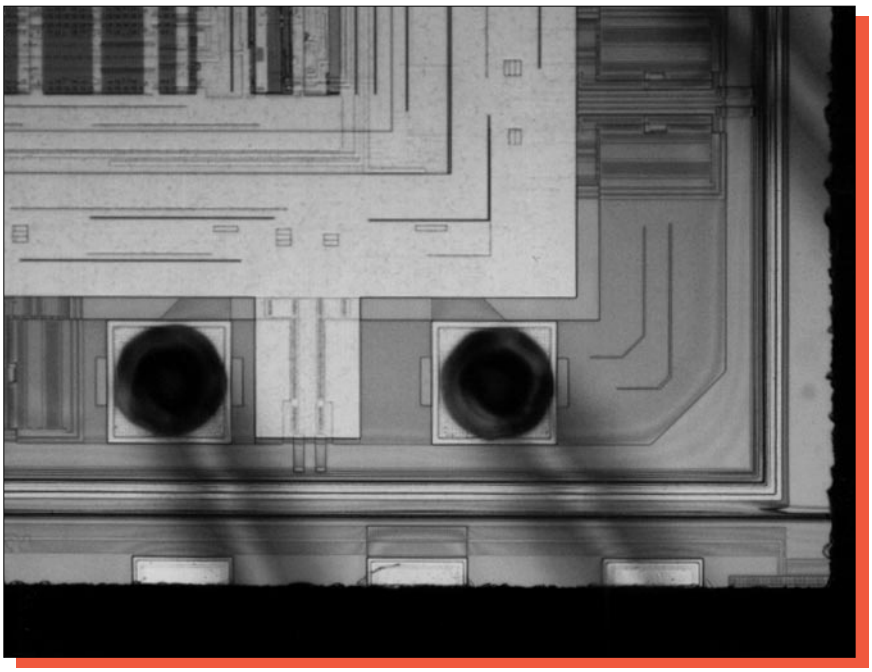


Figure 7. Optical views illustrating the scribe lane width. Mag. 160x.



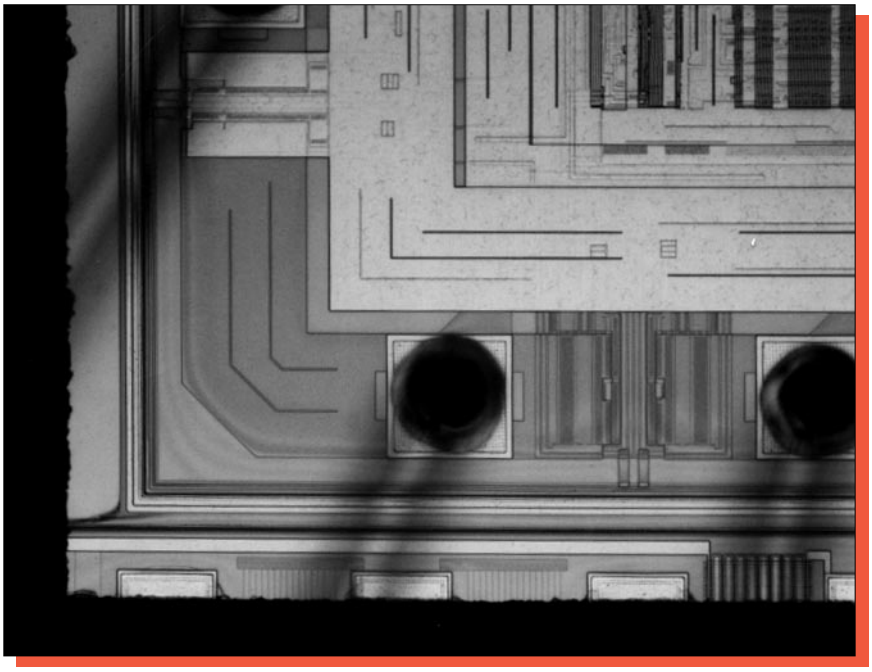


Figure 8. Optical views illustrating the scribe lane width. Mag. 160x.

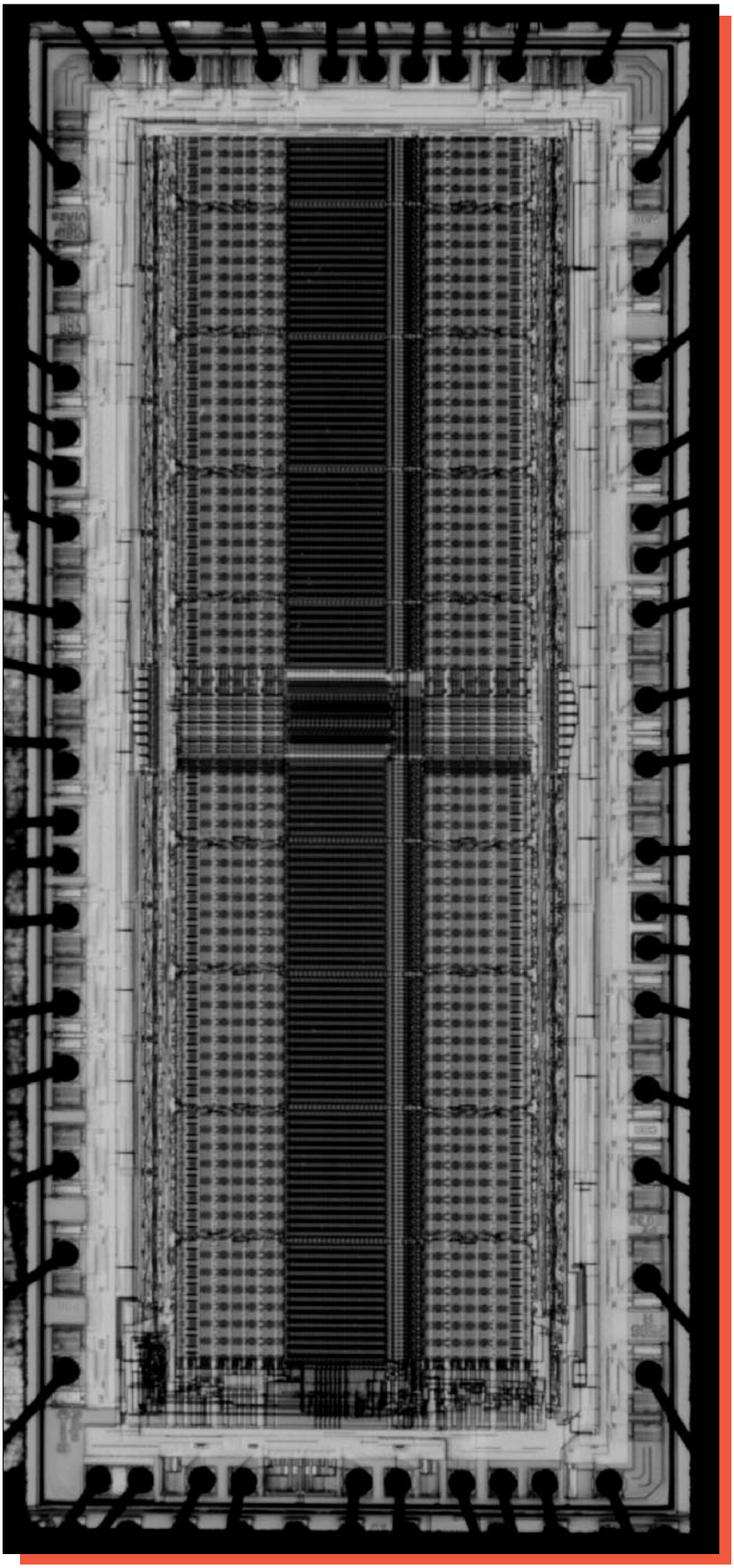
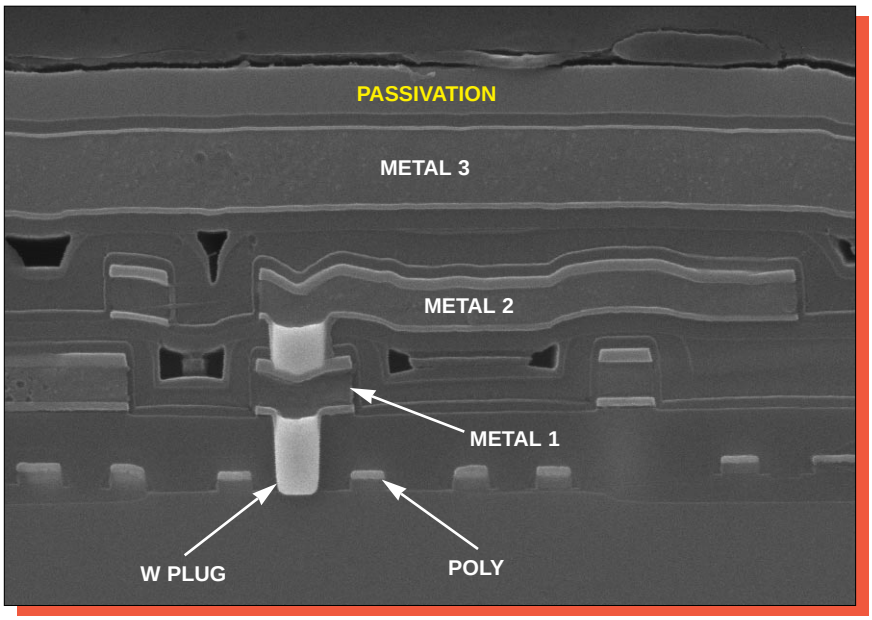


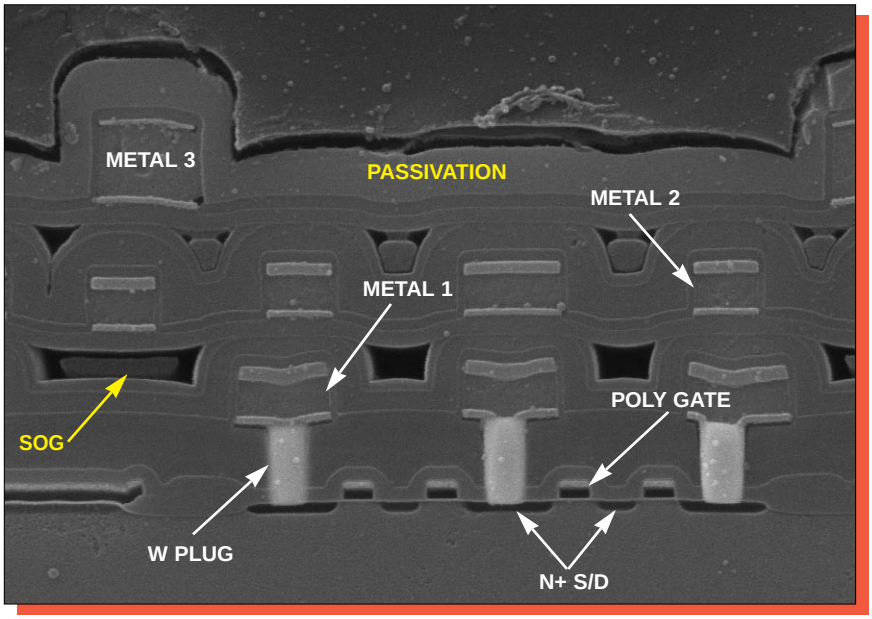
Figure 9. The Philips PZ5032 32 Macrocell CPLD. Mag. 44x.

Figure 10. Optical photographs of die identification markings. Mag. 500x.

Figure 11. Additional photographs of die markings. Mag. 500x.

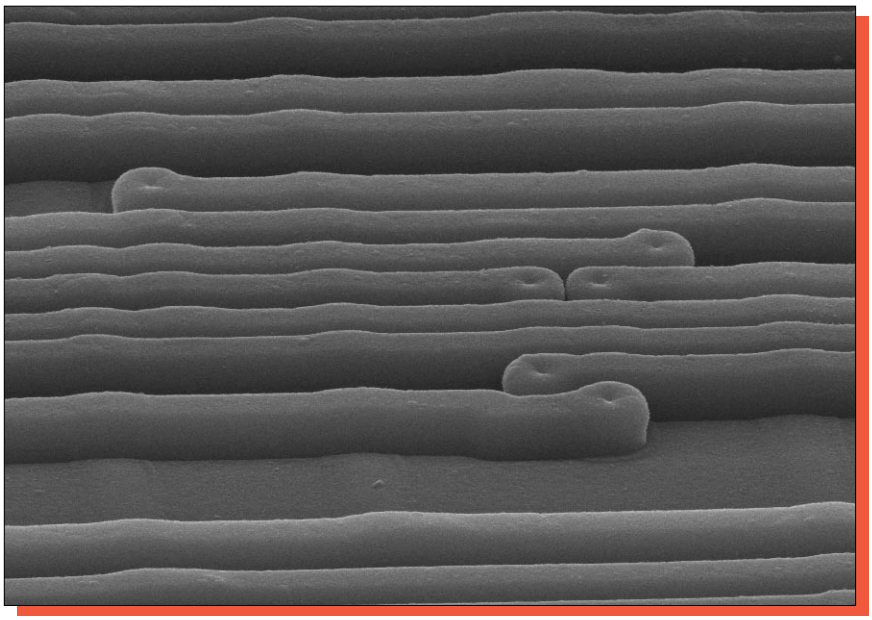


glass etch

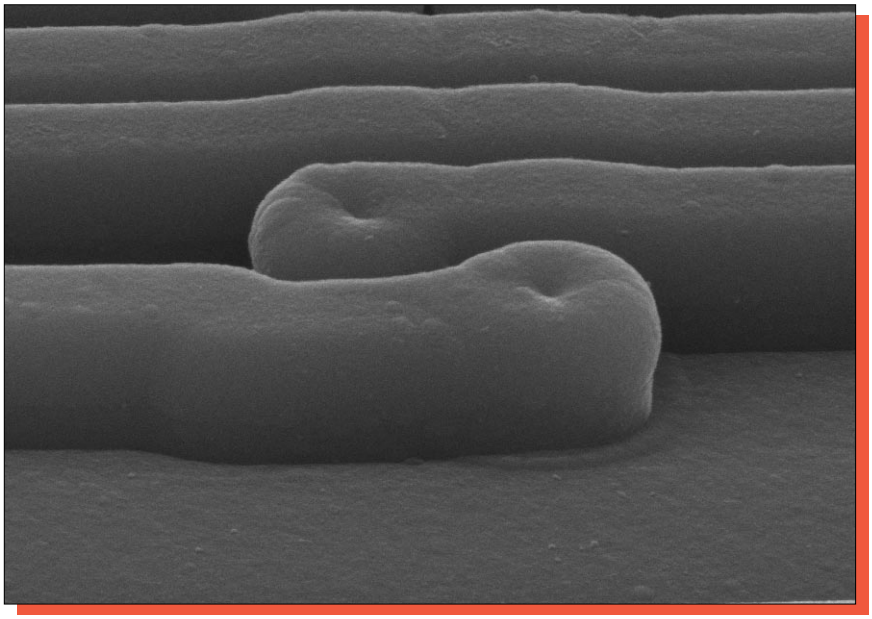


silicon etch

Figure 12. SEM section views illustrating general construction. Mag. 10,000x.

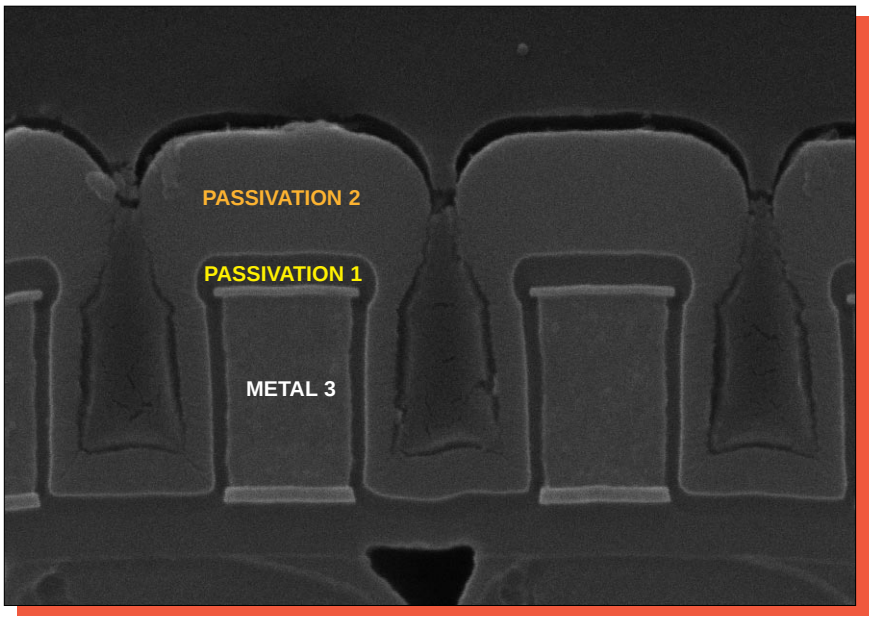


Mag. 5000x

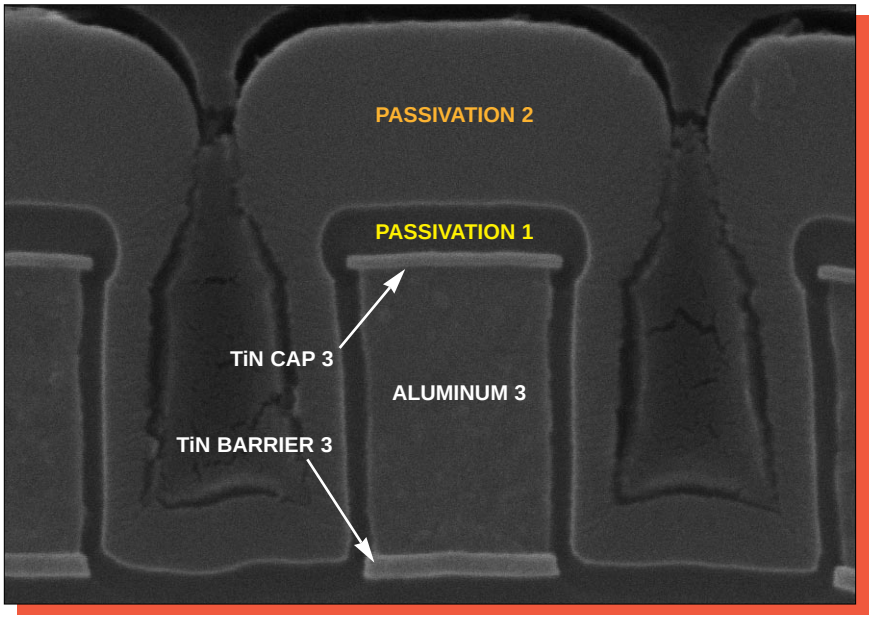


Mag. 13,000x

Figure 13. SEM views illustrating overlay passivation coverage. 60°.

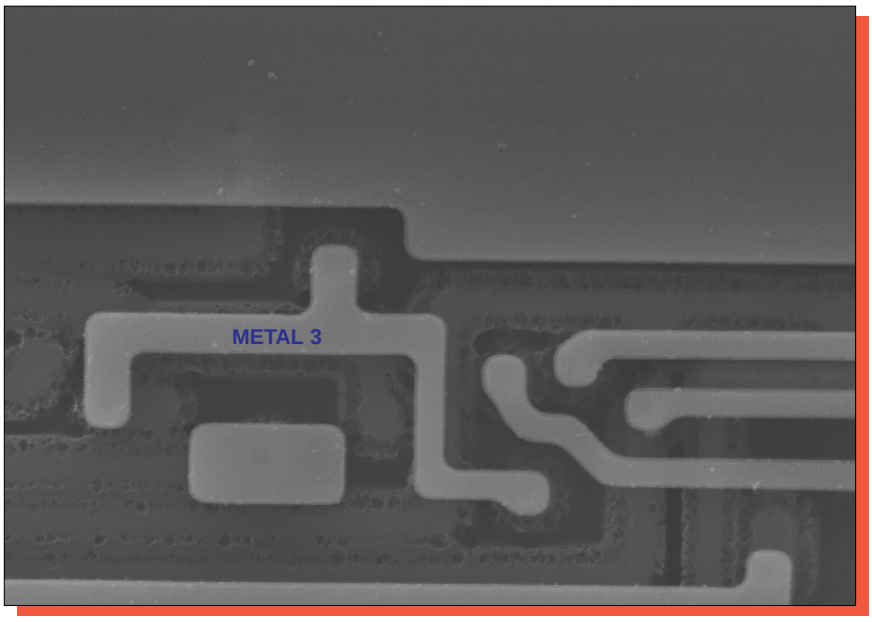


Mag. 26,000x



Mag. 40,000x

Figure 14. SEM section views illustrating metal 3 line profiles.



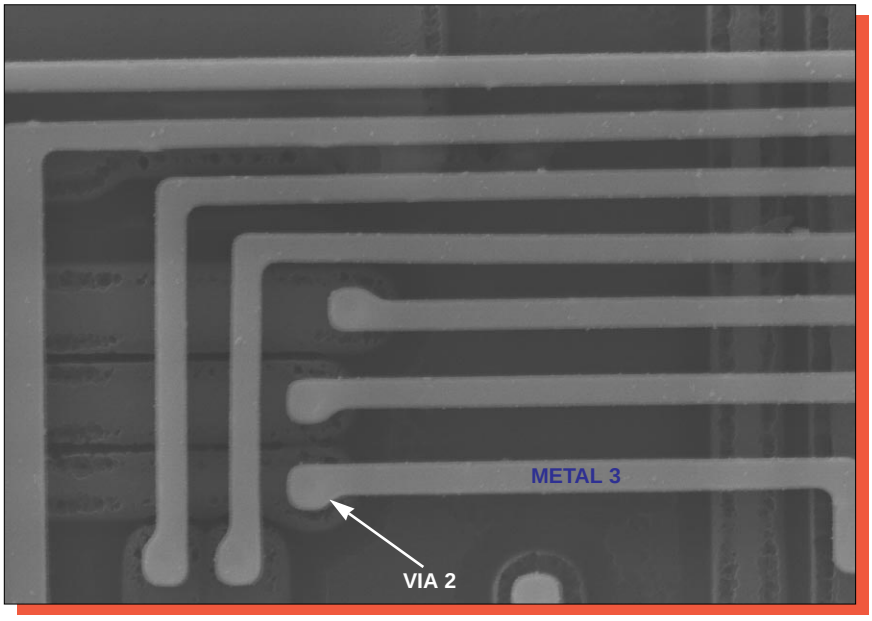
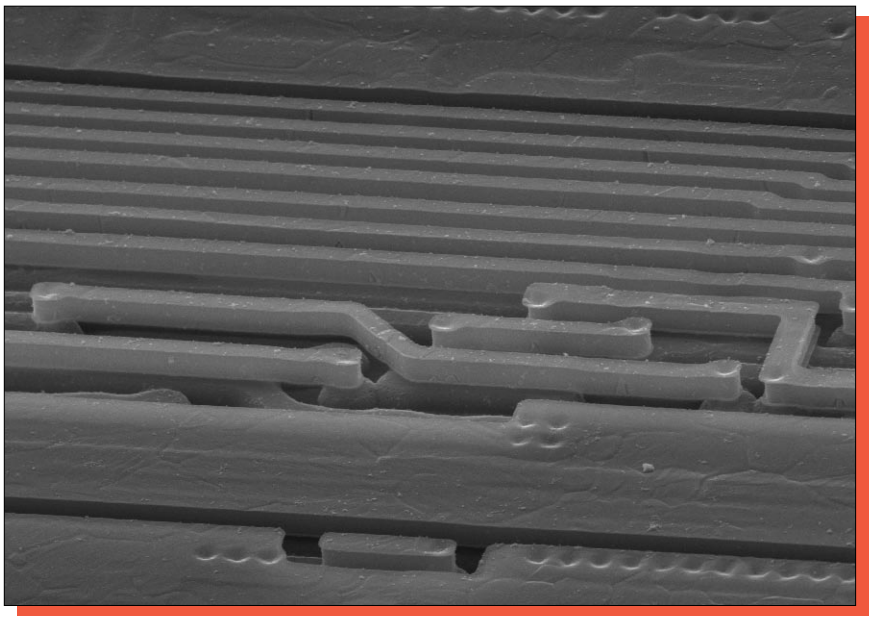
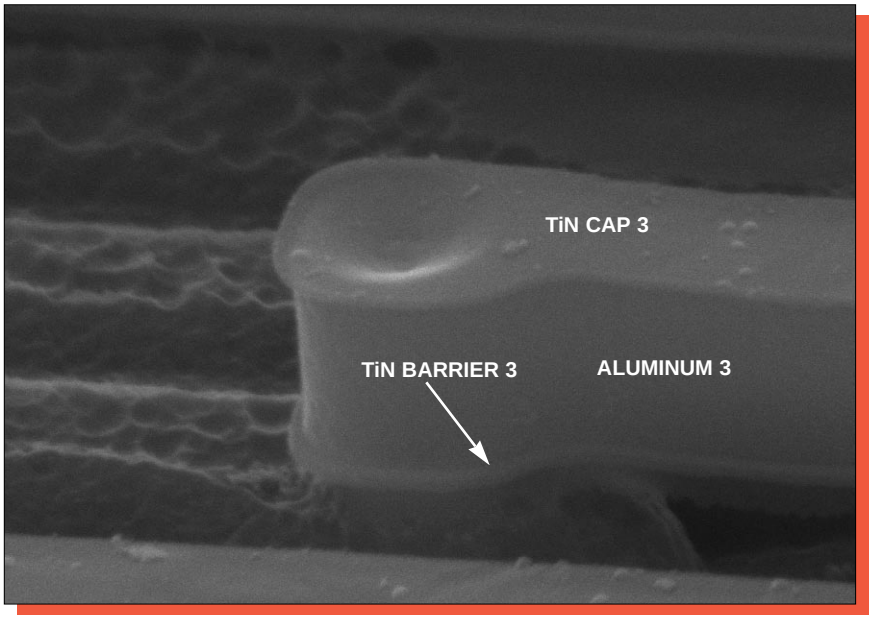


Figure 15. Topological SEM views of metal 3 patterning. Mag. 5000x, 0°.

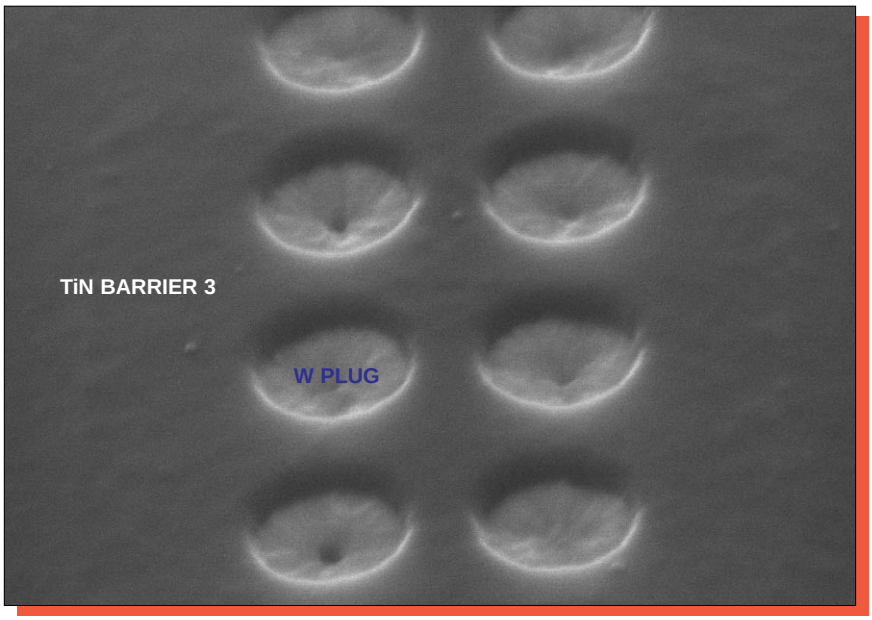


Mag. 3400x

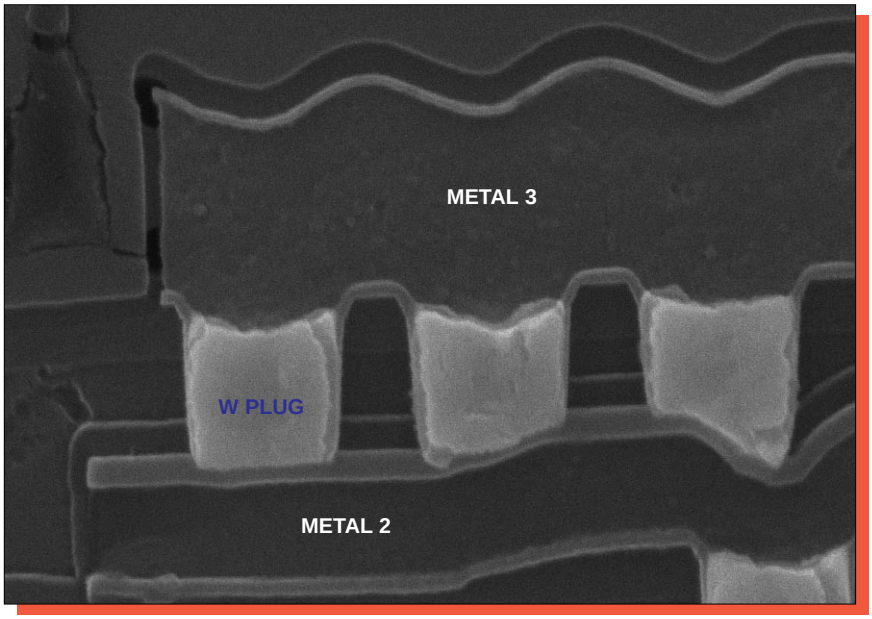


Mag. 27,000x

Figure 16. SEM views illustrating metal 3 coverage. 60°.

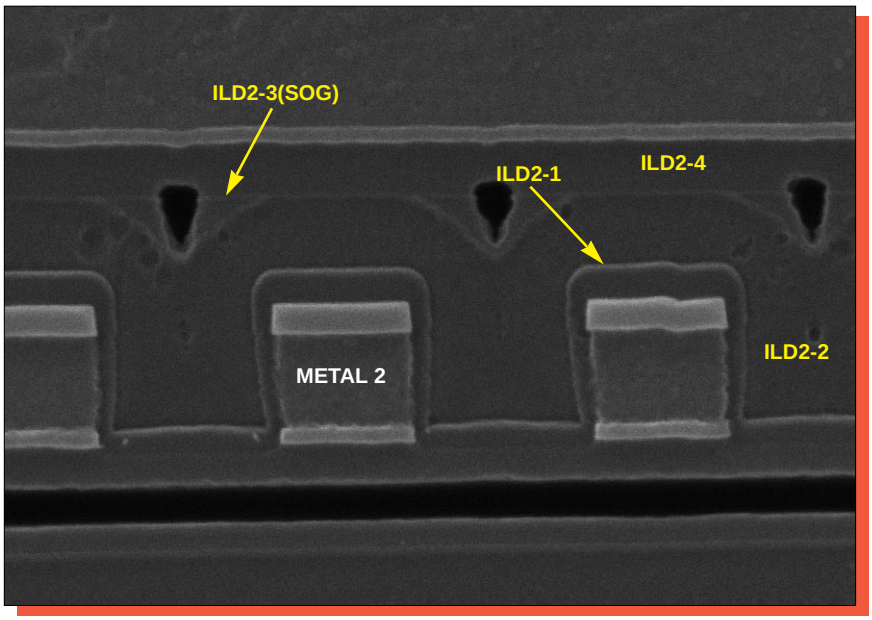


Mag. 25,000x, 45°

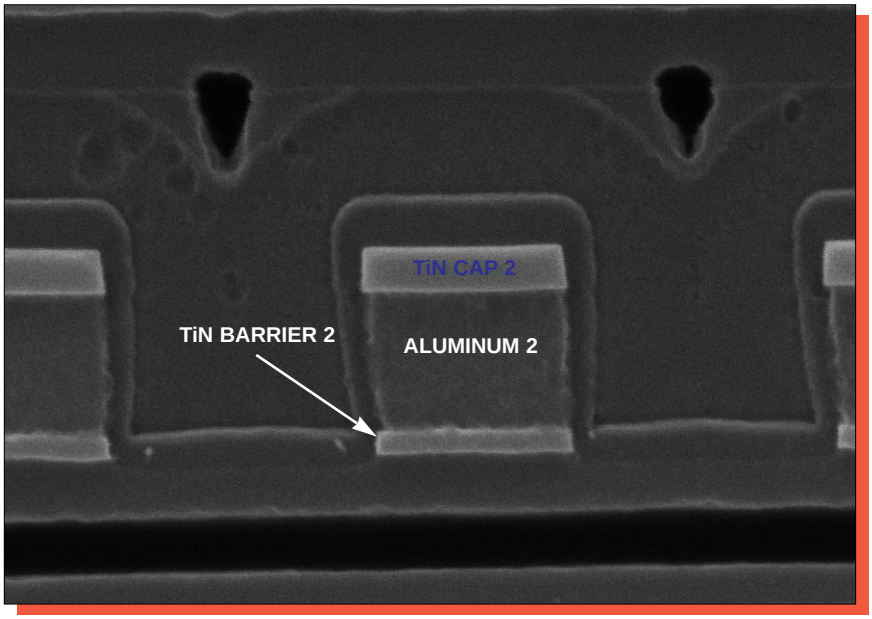


Mag. 26,000x

Figure 17. SEM views of metal 3-to-metal 2 vias.

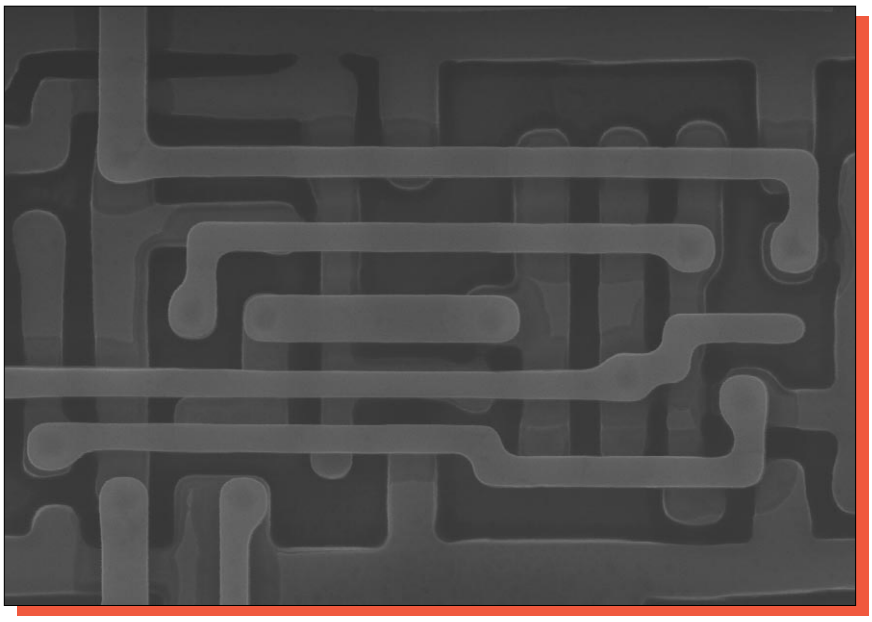


Mag. 26,000x



Mag. 40,000x

Figure 18. SEM section views of metal 2 line profiles.



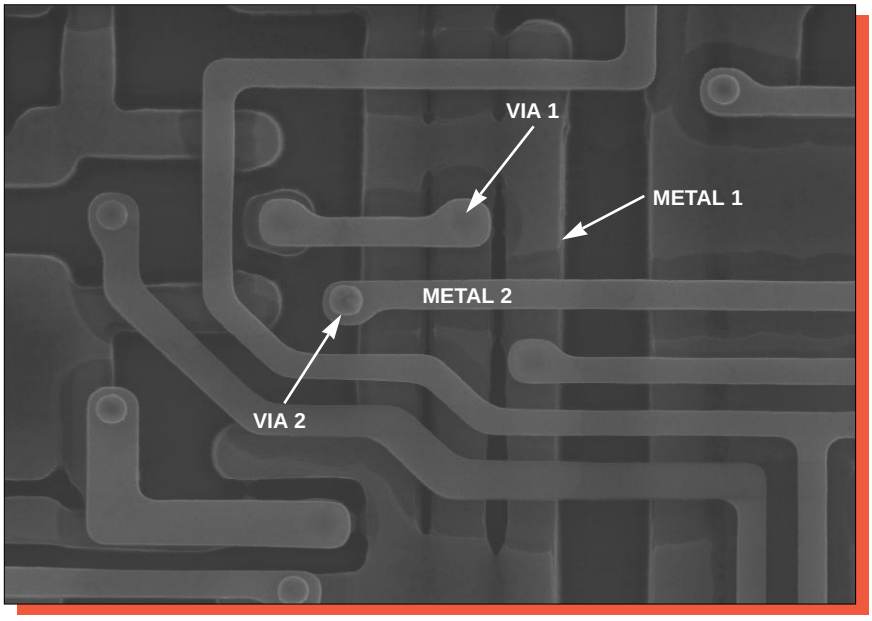
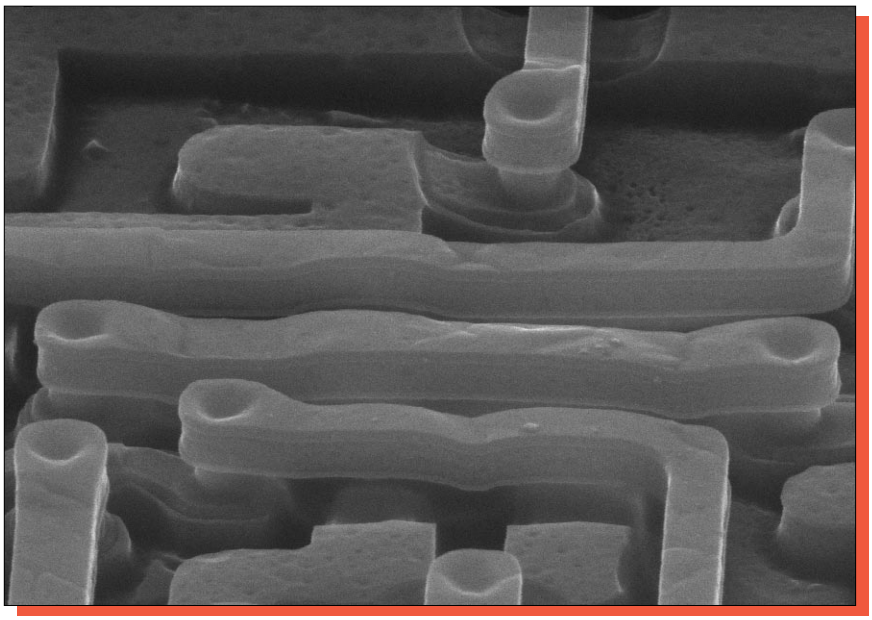
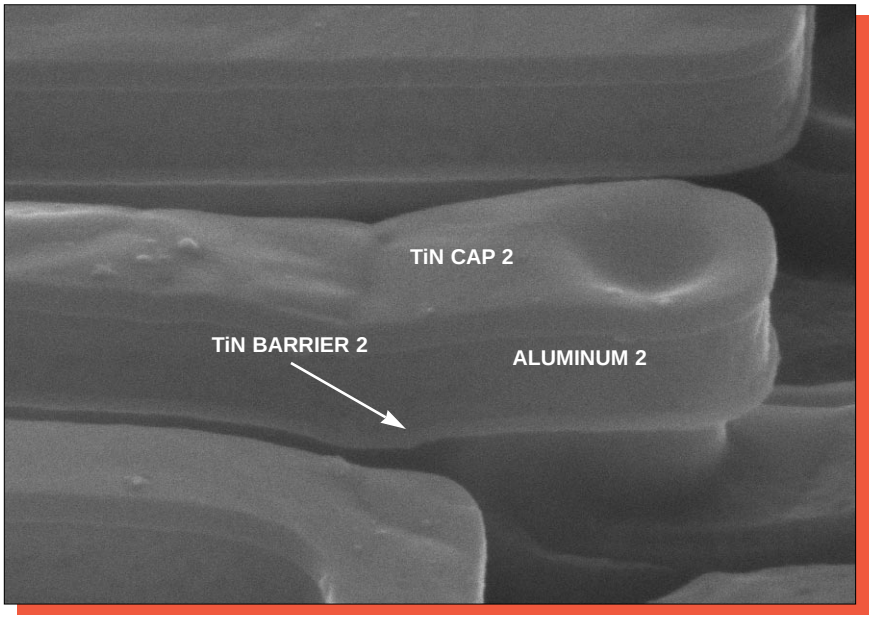


Figure 19. Topological SEM views of metal 2 patterning. Mag. 5000x, 0°.

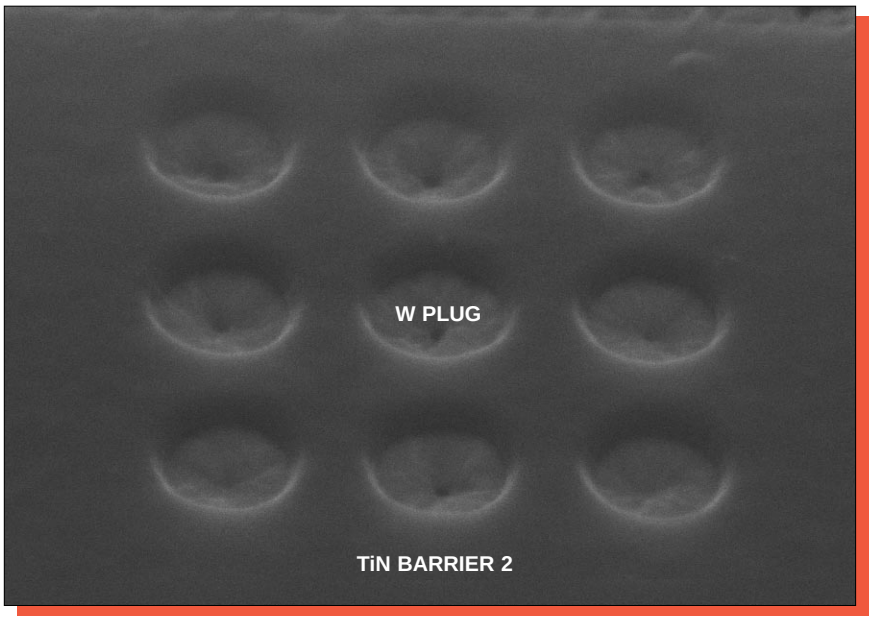


Mag. 10,000x

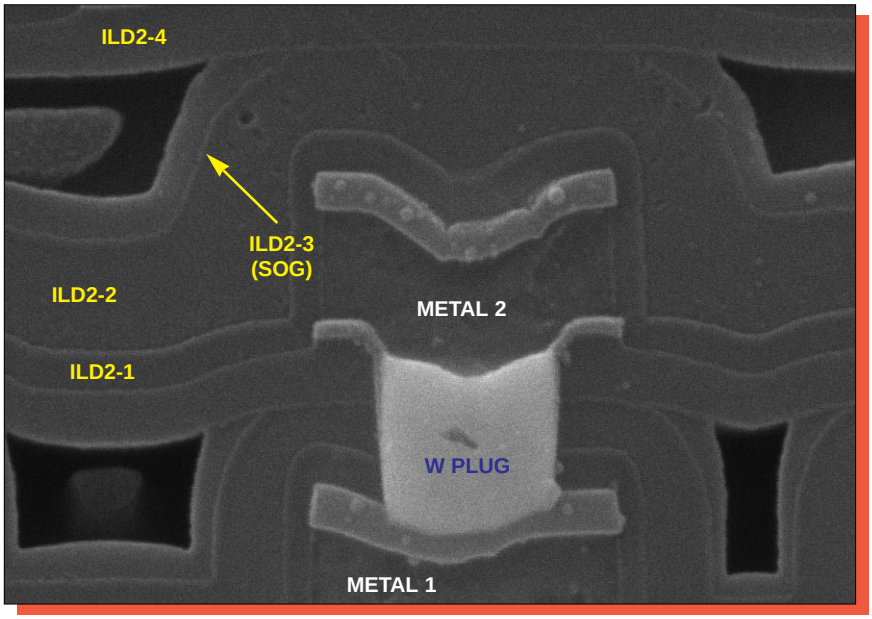


Mag. 27,000x

Figure 20. SEM views illustrating metal 2 coverage. 60°.

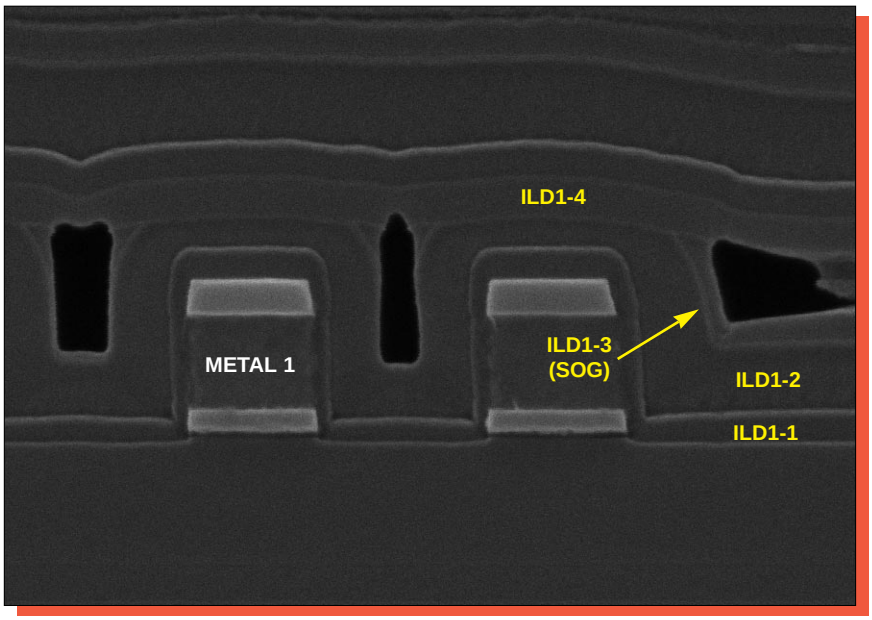


Mag. 25,000x, 45°

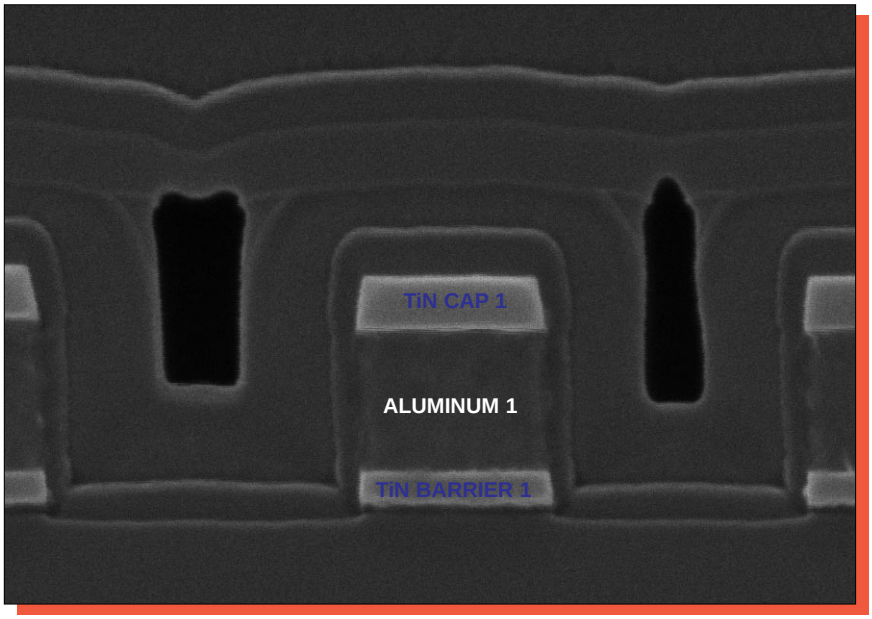


Mag. 33,500x

Figure 21. SEM views of metal 2-to-metal 1 vias.

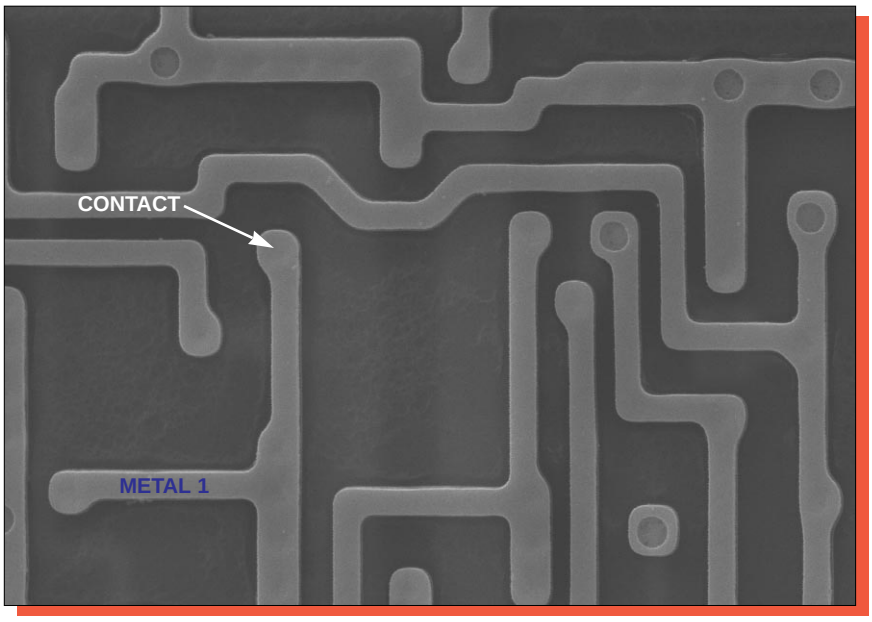


Mag. 26,000x



Mag. 40,000x

Figure 22. SEM section views of metal 1 line profiles.



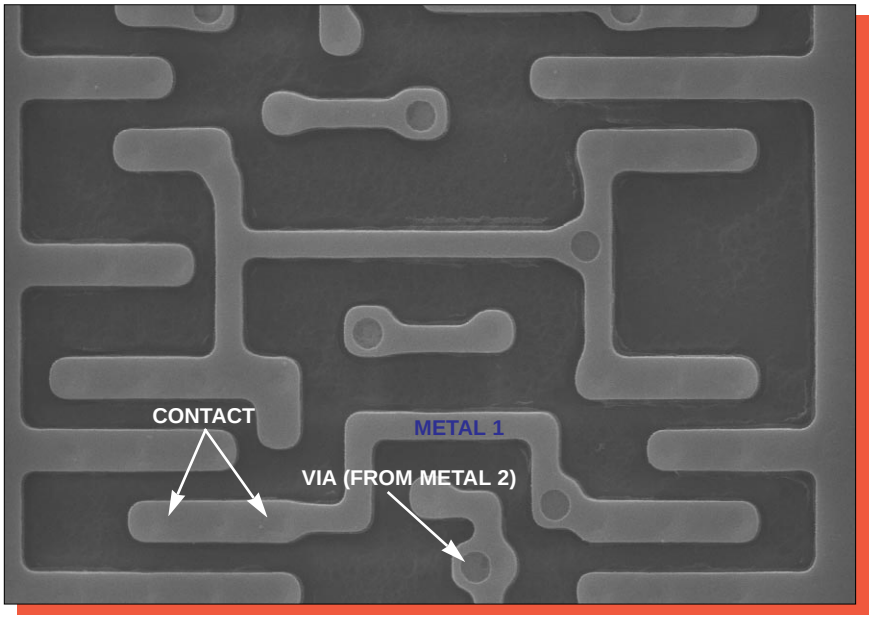
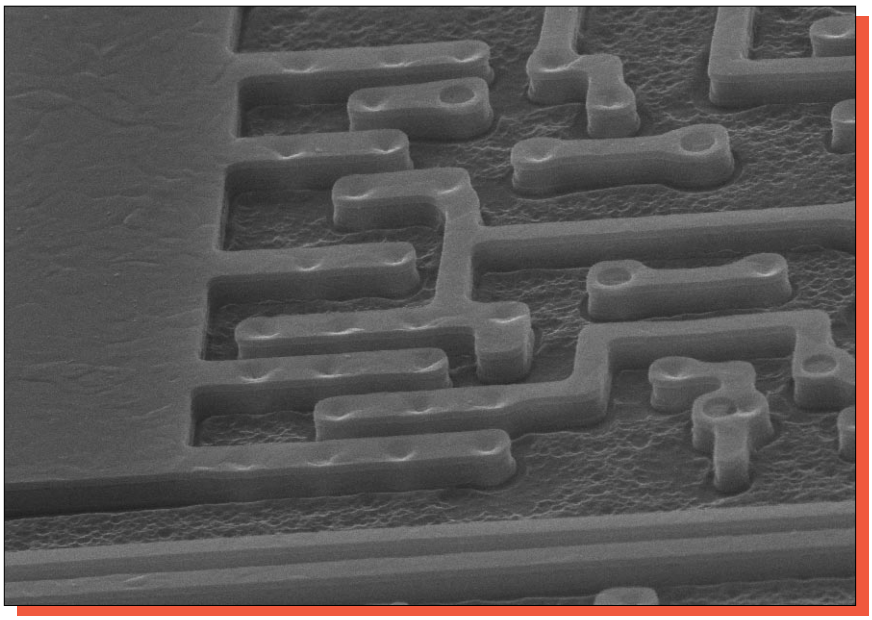
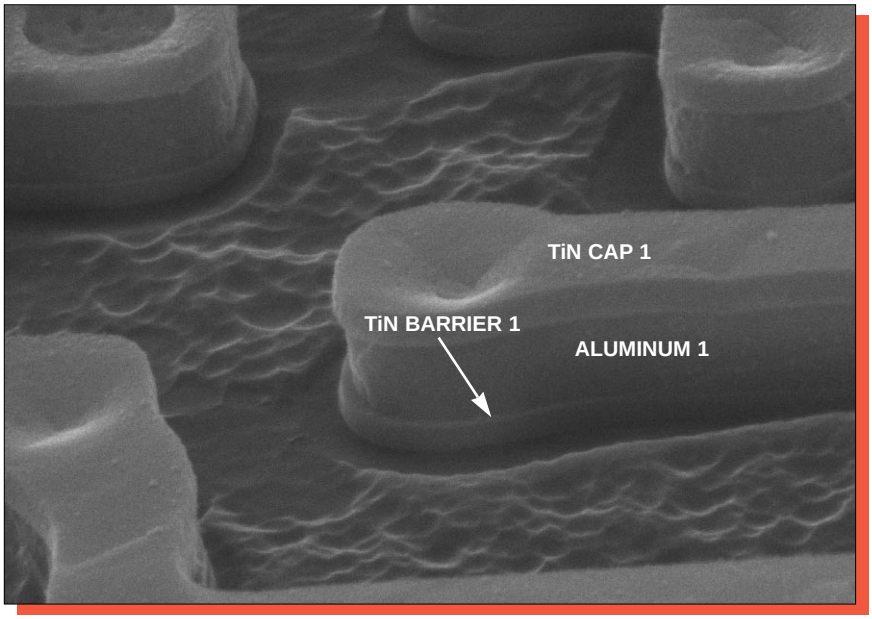


Figure 23. Topological SEM views of metal 1 patterning. Mag. 5000x, 0°.

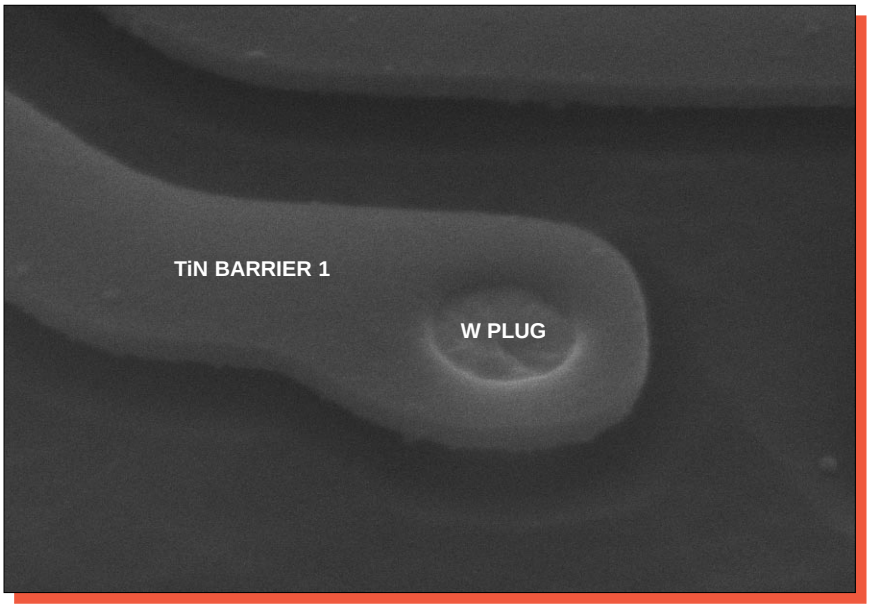


Mag. 6000x

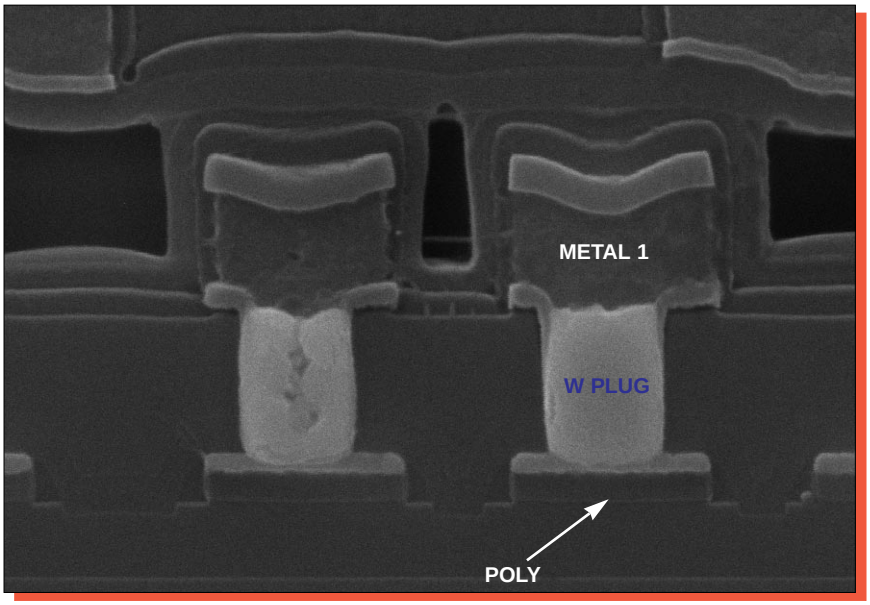


Mag. 25,000x

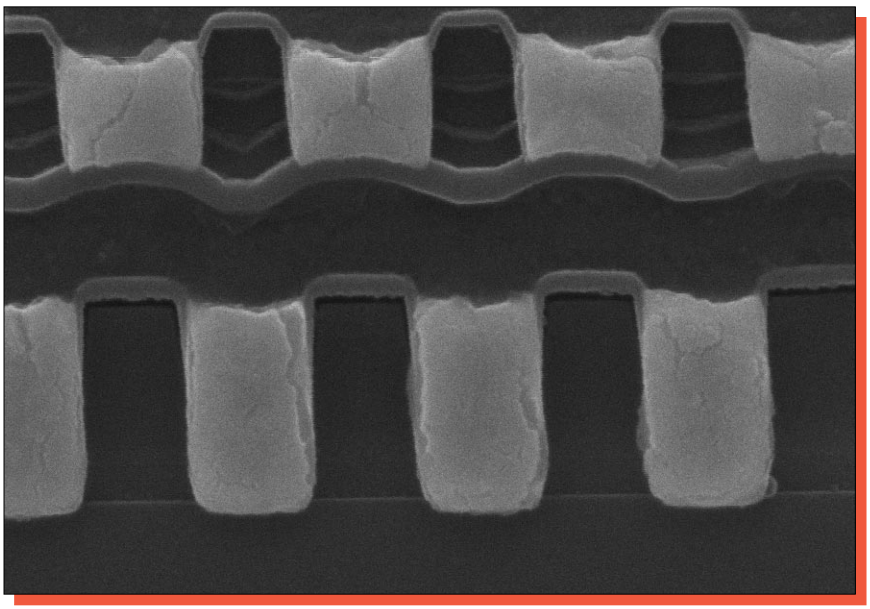
Figure 24. SEM views illustrating metal 1 coverage. 60°.



Mag. 40,000x, 45°

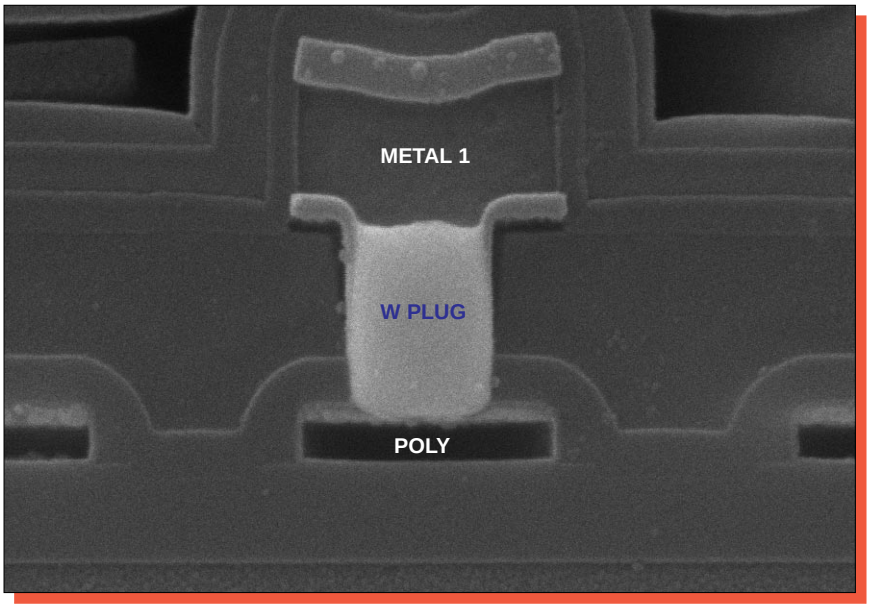


metal 1-to-poly,
glass etch,
Mag. 26,000x

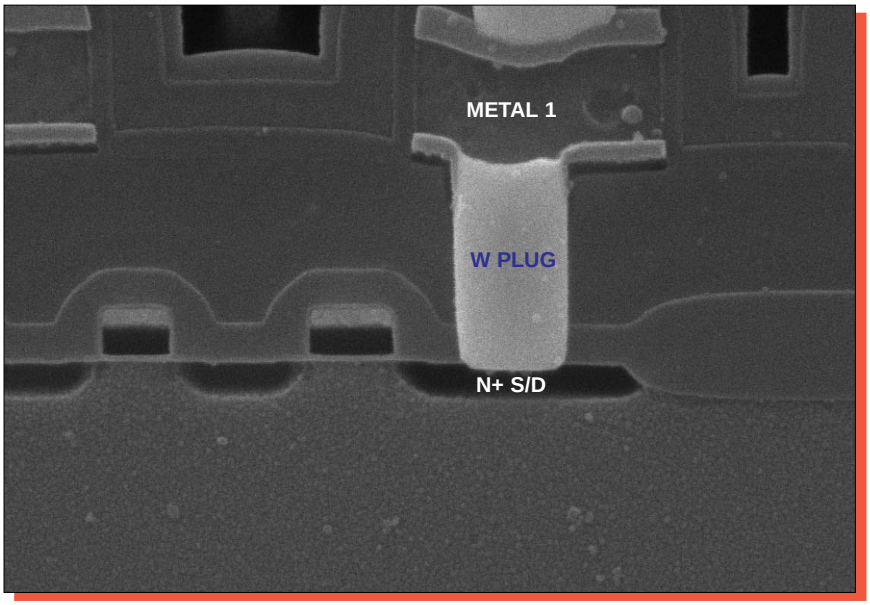


metal 1-to-diffusion,
glass etch,
Mag. 26,000x

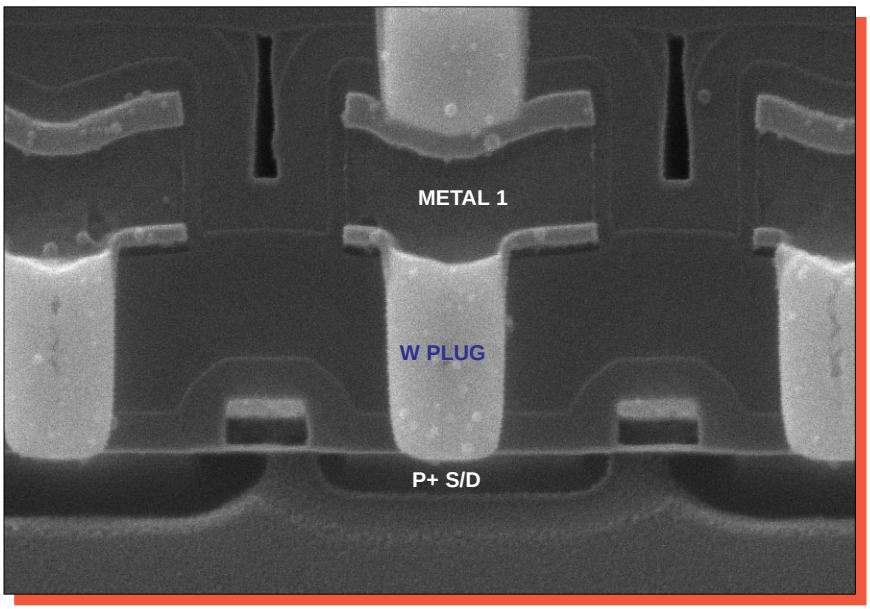
Figure 25. SEM views of typical metal 1 contacts.



metal 1-to-poly,
Mag. 33,500x

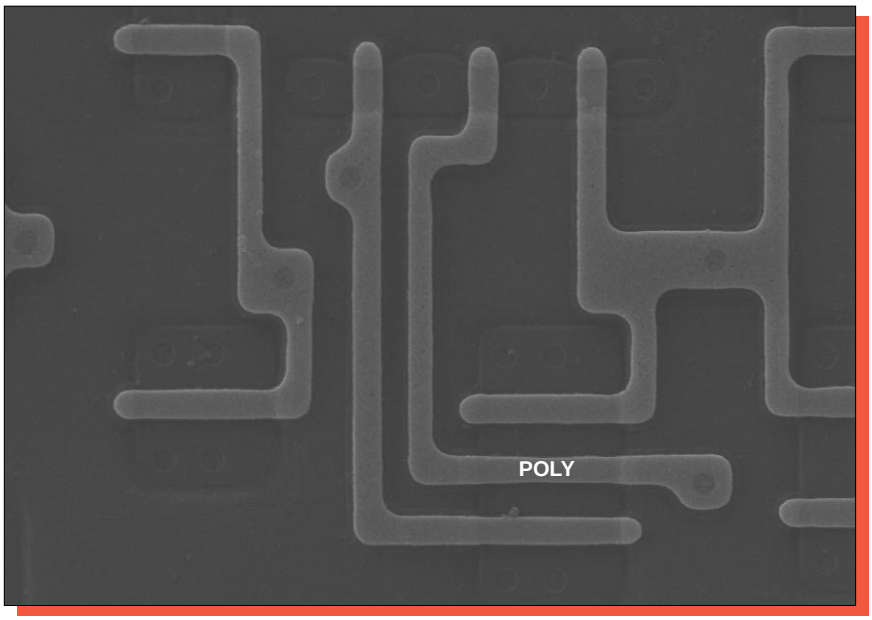


metal 1-to-N+,
Mag. 26,000x



metal 1-to-P+,
Mag. 26,000x

Figure 26. SEM section views of typical metal 1 contacts. Silicon etch.



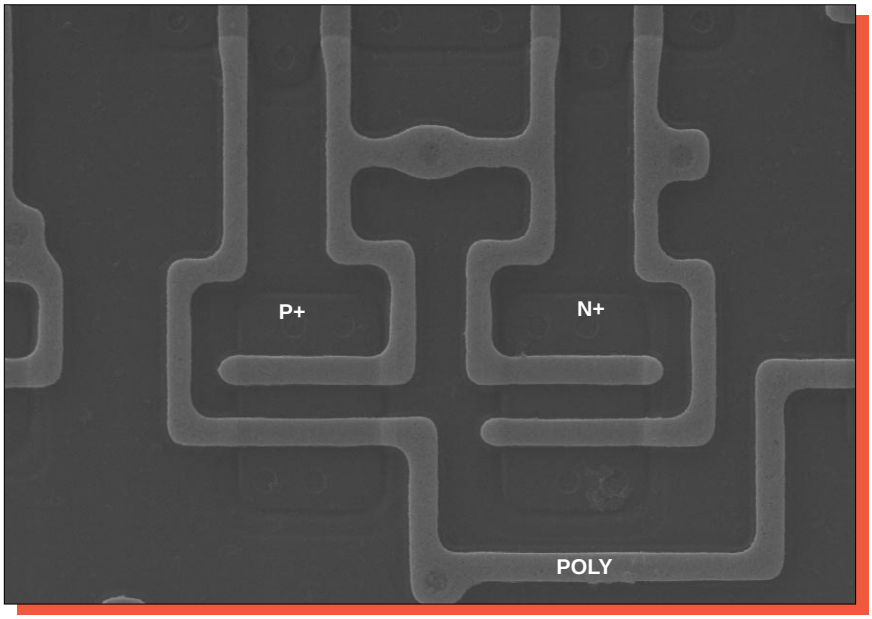
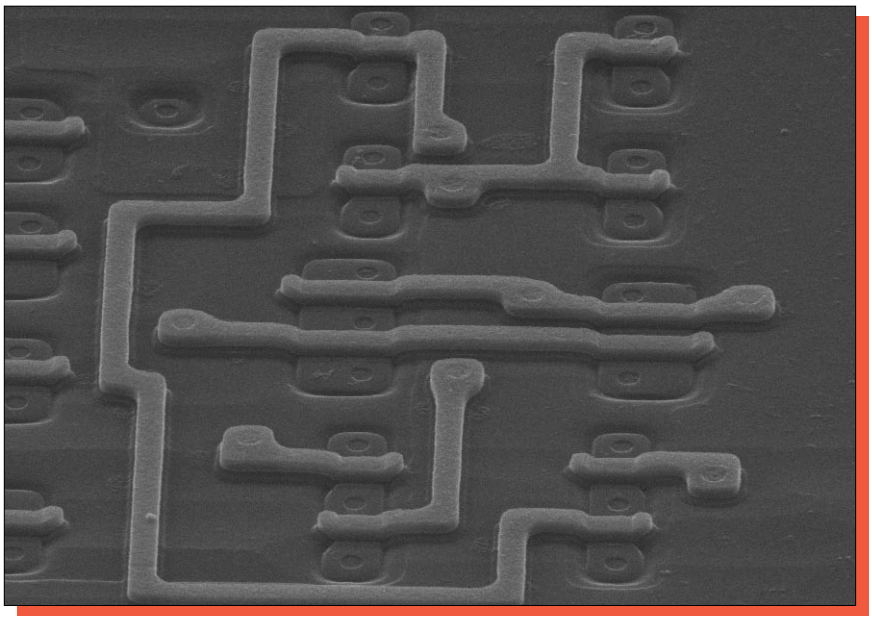
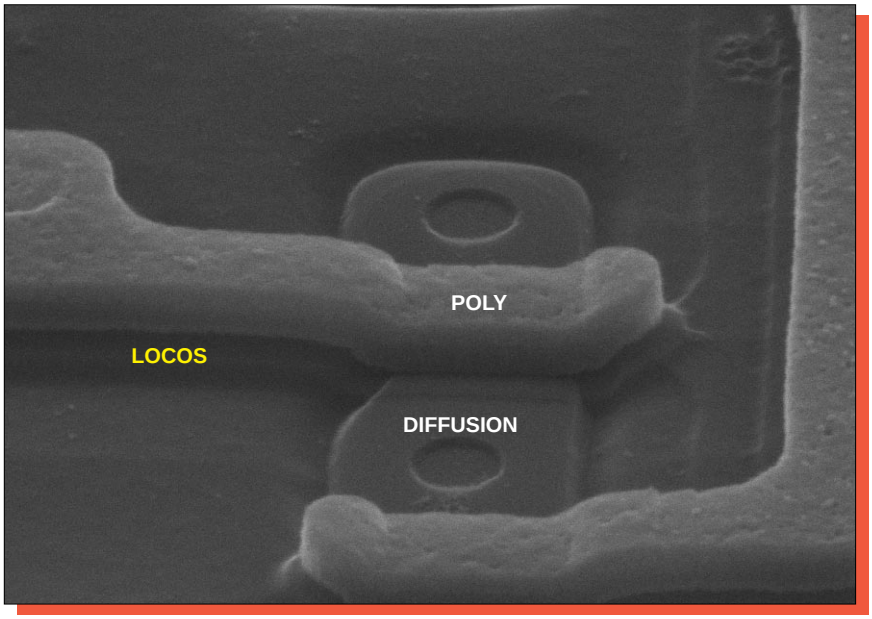


Figure 27. Topological SEM views of poly patterning. Mag. 6500x, 0°.

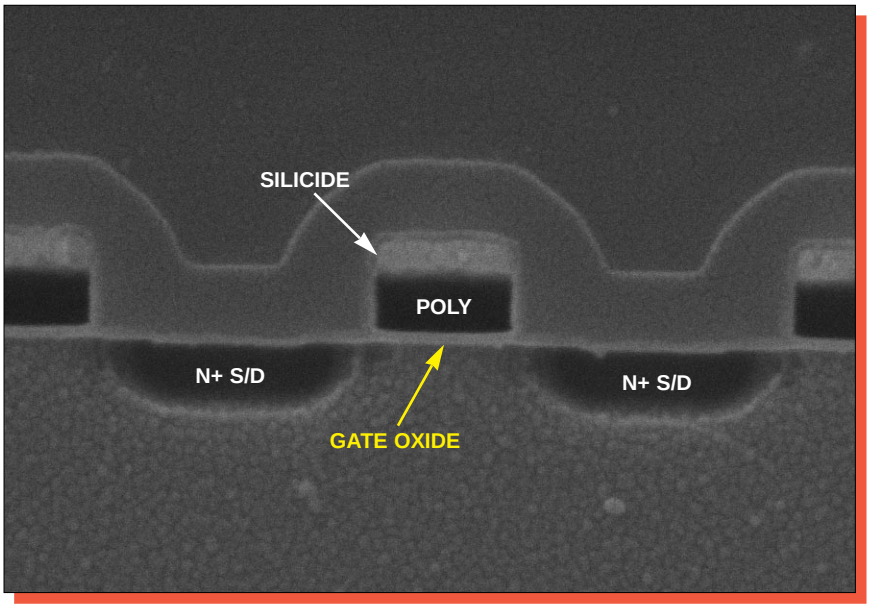


Mag. 6800x

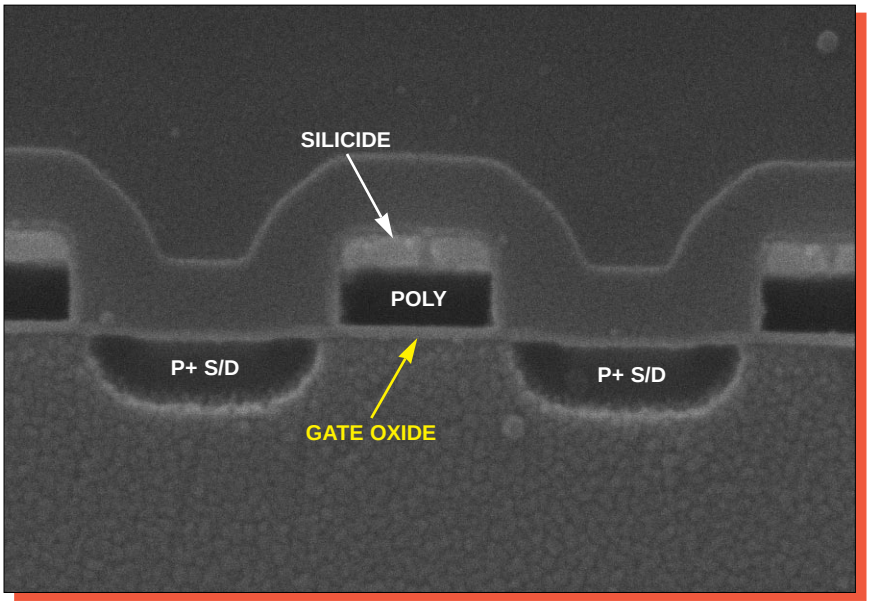


Mag. 30,000x

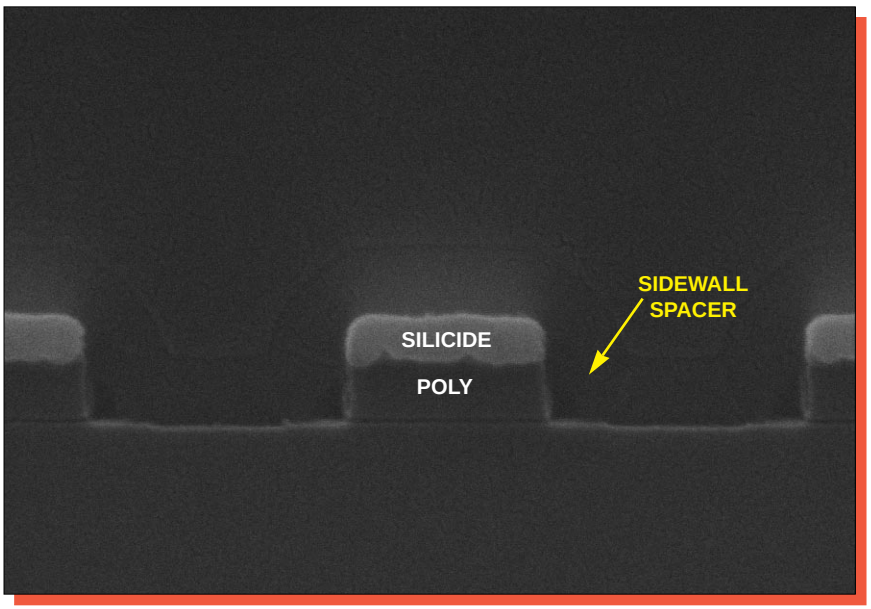
Figure 28. SEM views illustrating poly coverage. 60°.



N-channel



P-channel



glass etch

Figure 29. SEM section views of typical transistors. Mag. 52,000x.

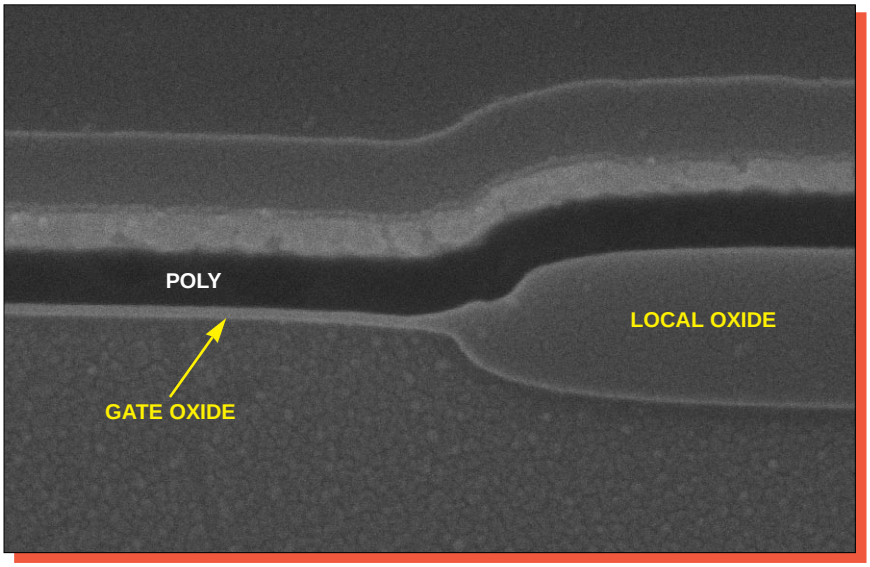
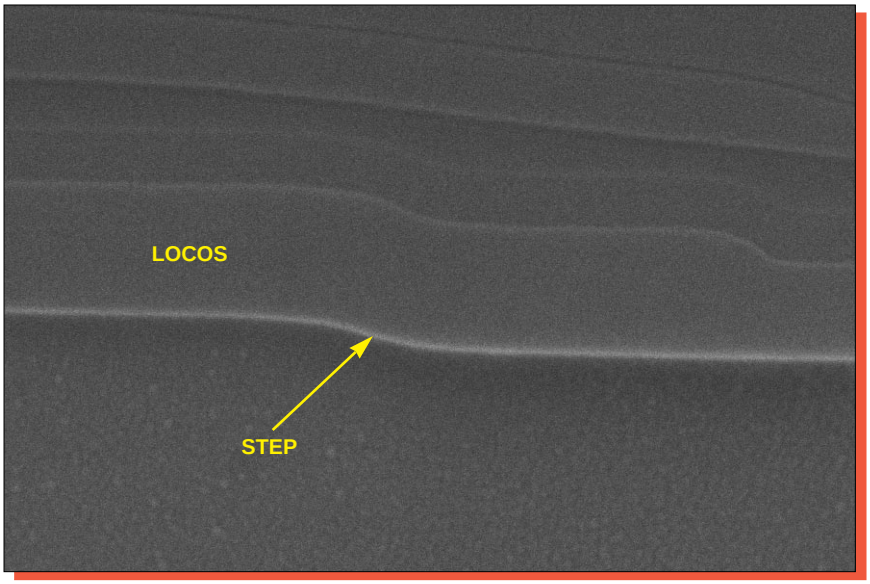
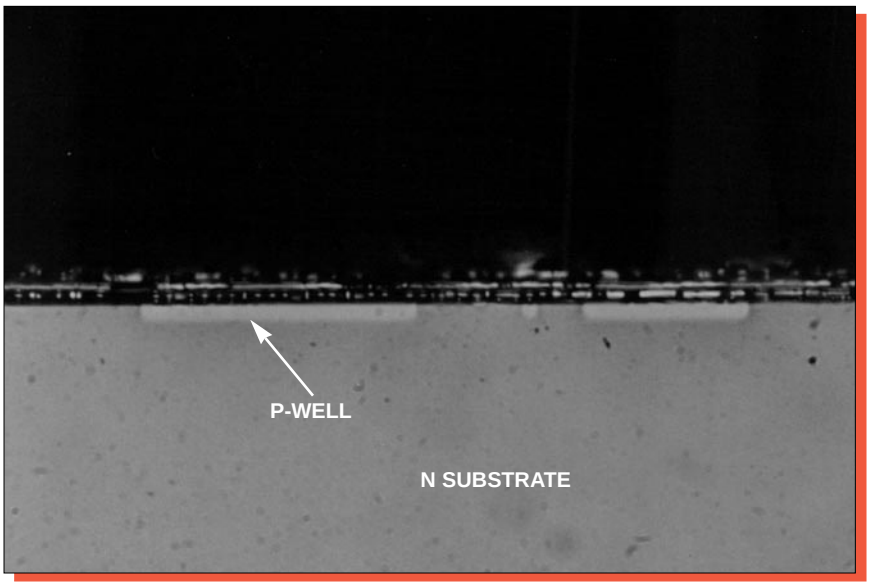


Figure 30. SEM section view of a local oxide birdsbeak. Mag. 52,000x.

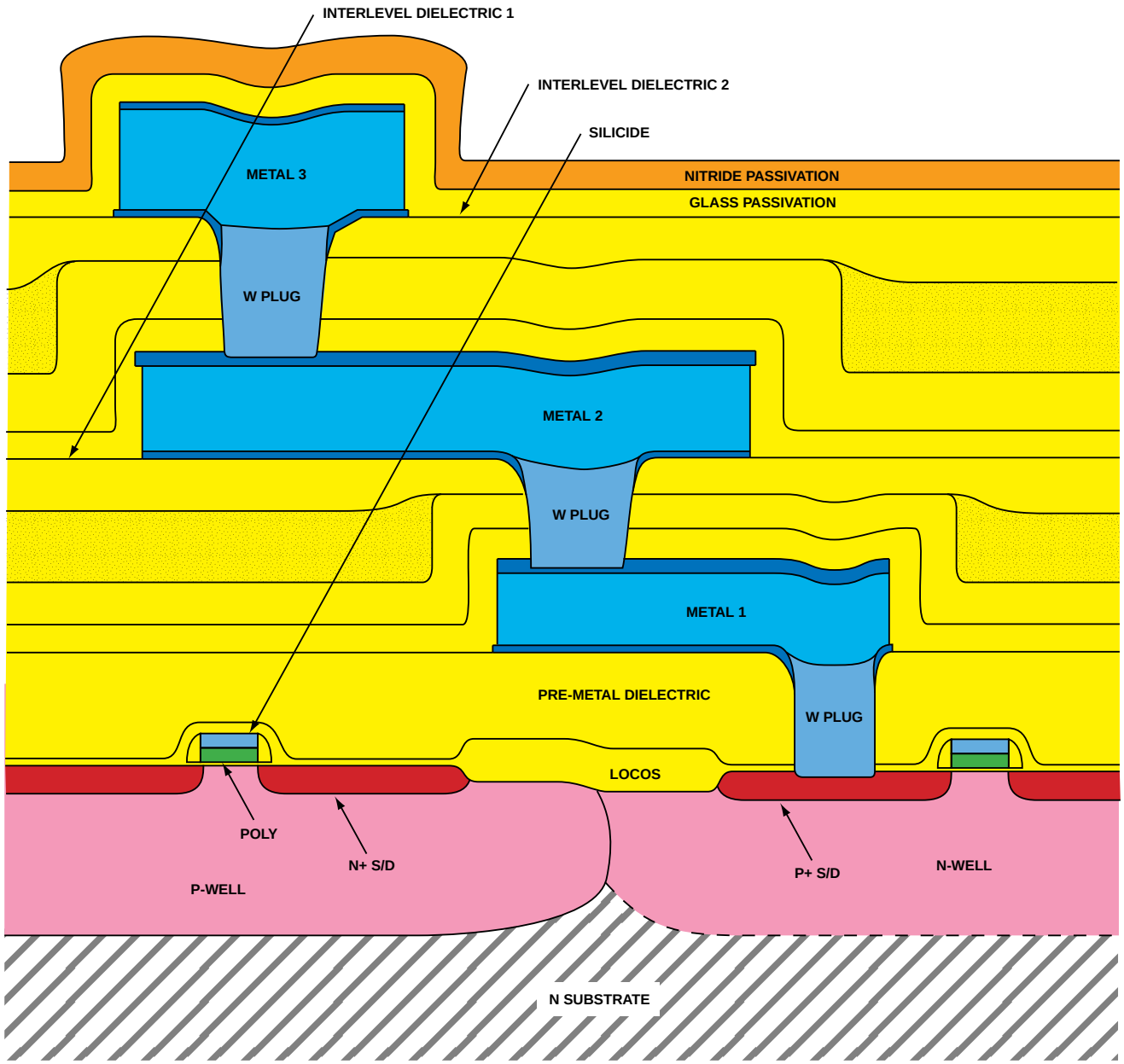


Mag. 52,000x



Mag. 800x

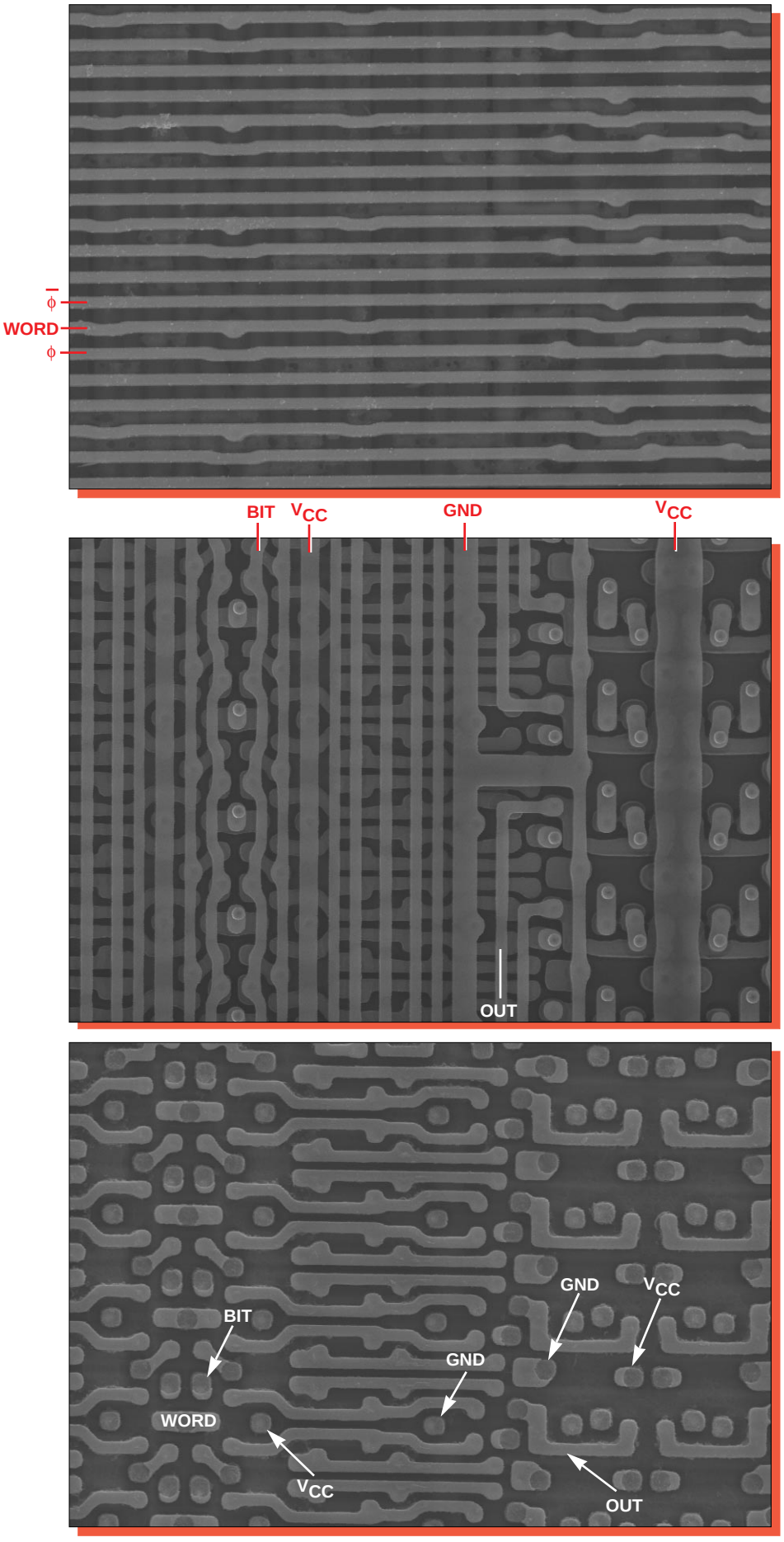
Figure 31. Section views of the well structure.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 31a. Color cross section drawing illustrating device structure.

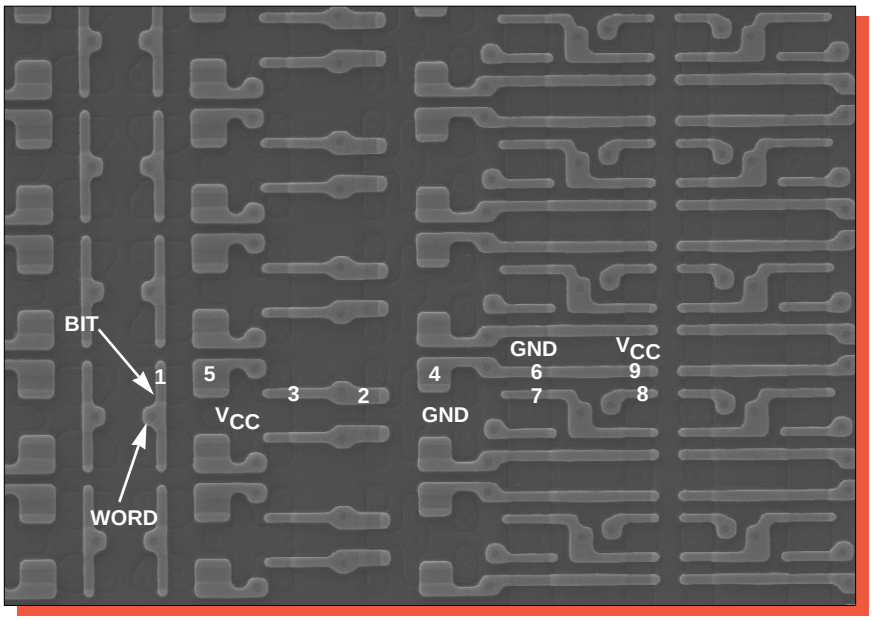


metal 3

metal 2

metal 1

Figure 32. Topological SEM views of the SRAM cell. Mag. 2500x, 0°.



unlayered

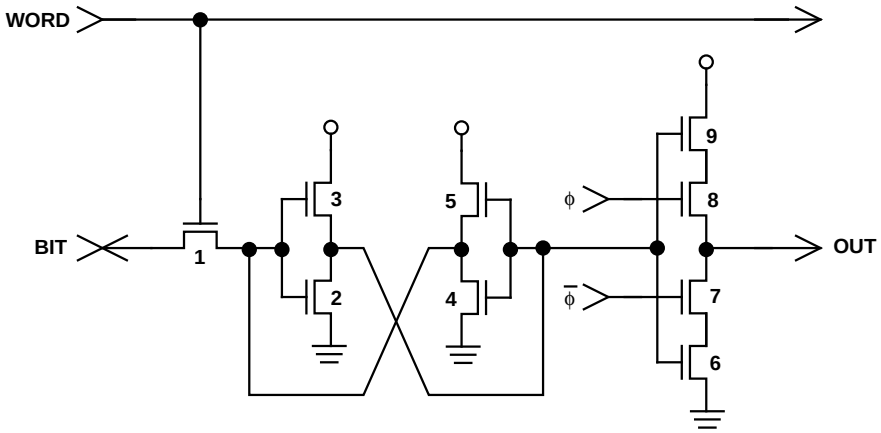
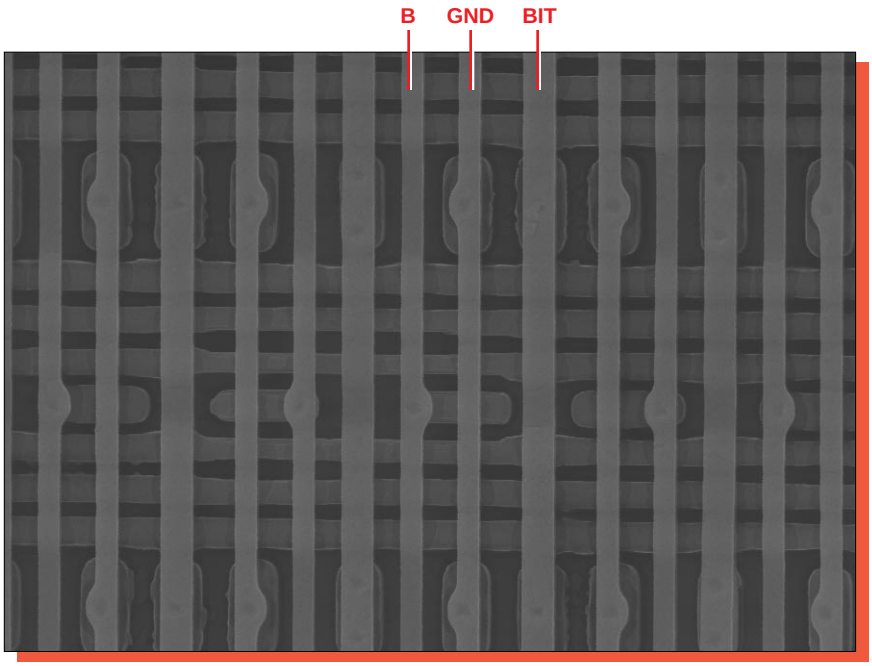
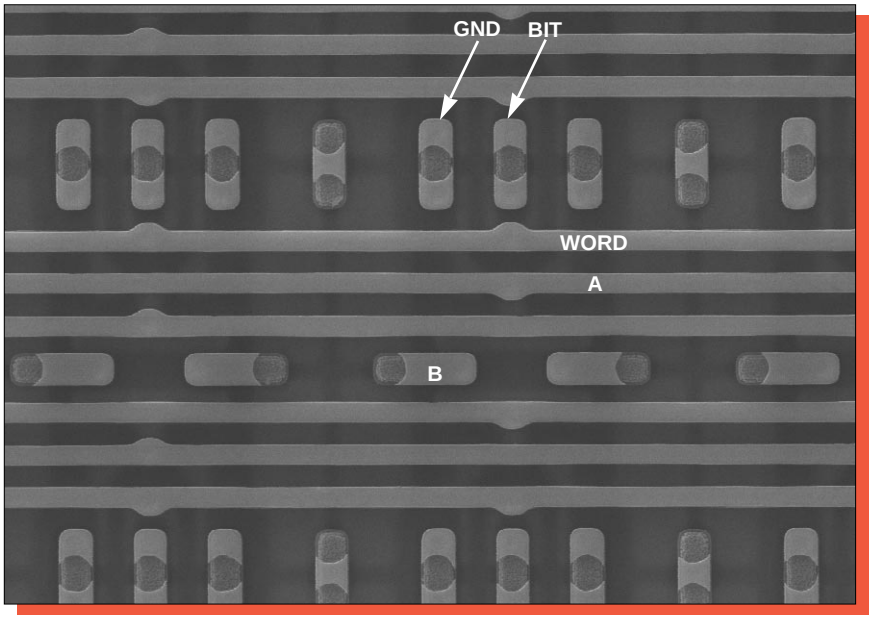


Figure 33. Topological SEM view and schematic of the SRAM cell. Mag. 2500x, 0°.

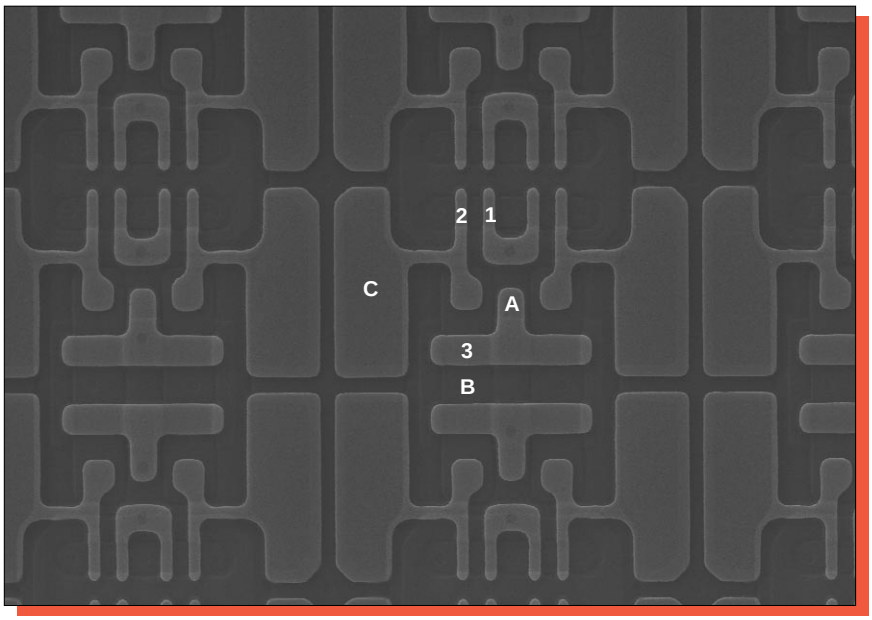


metal 2



metal 1

Figure 34. Topological SEM views of the EEPROM cell array. Mag. 3200x, 0°.



unlayered

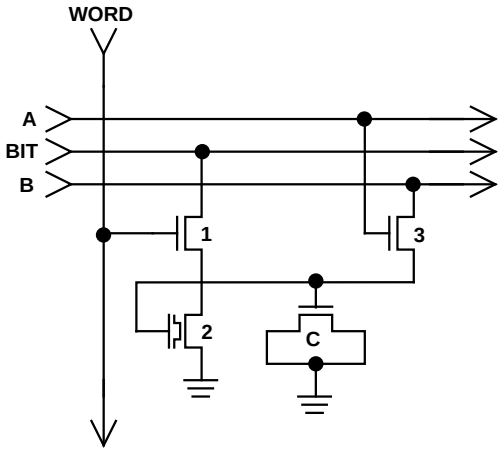
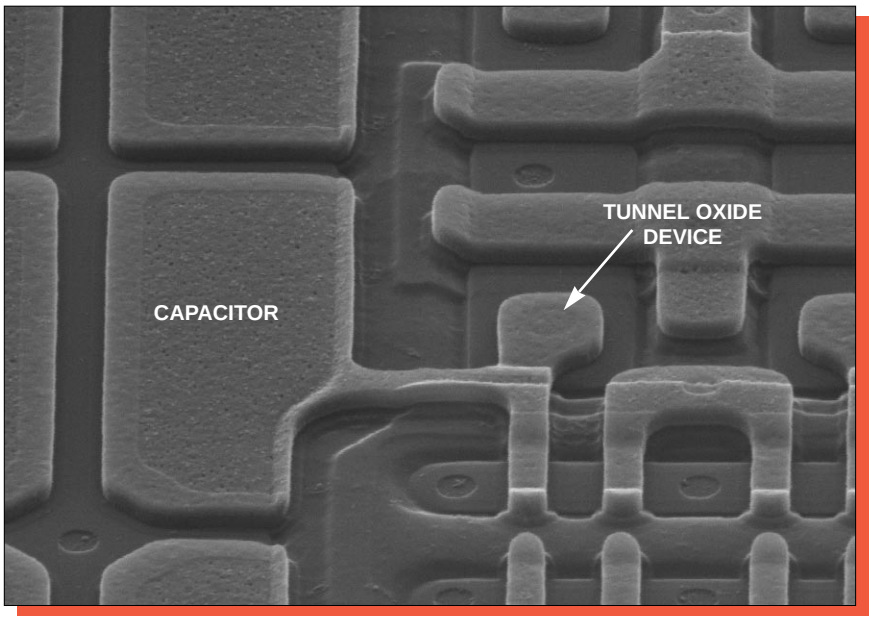
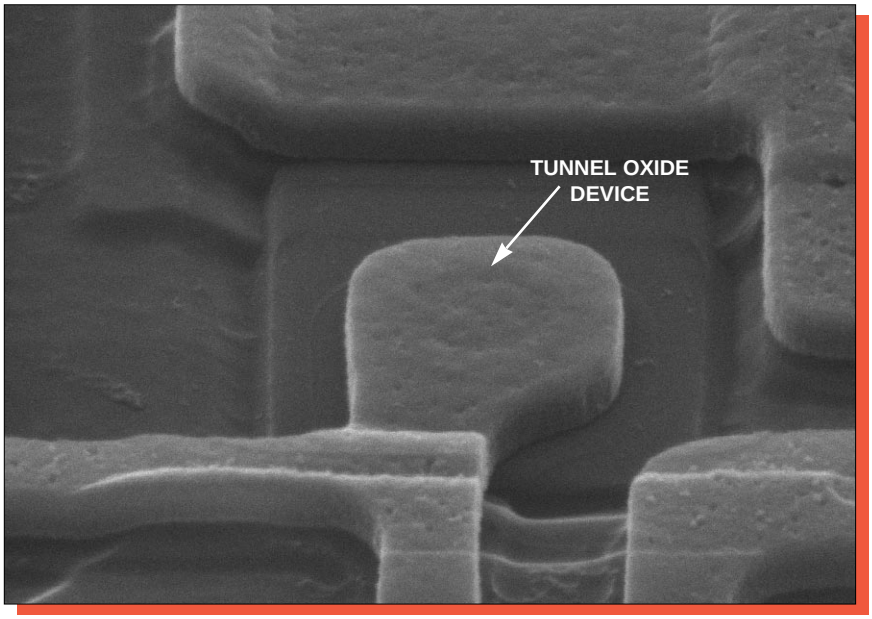


Figure 35. Topological SEM view and schematic of the EEPROM cell. Mag. 3200x,

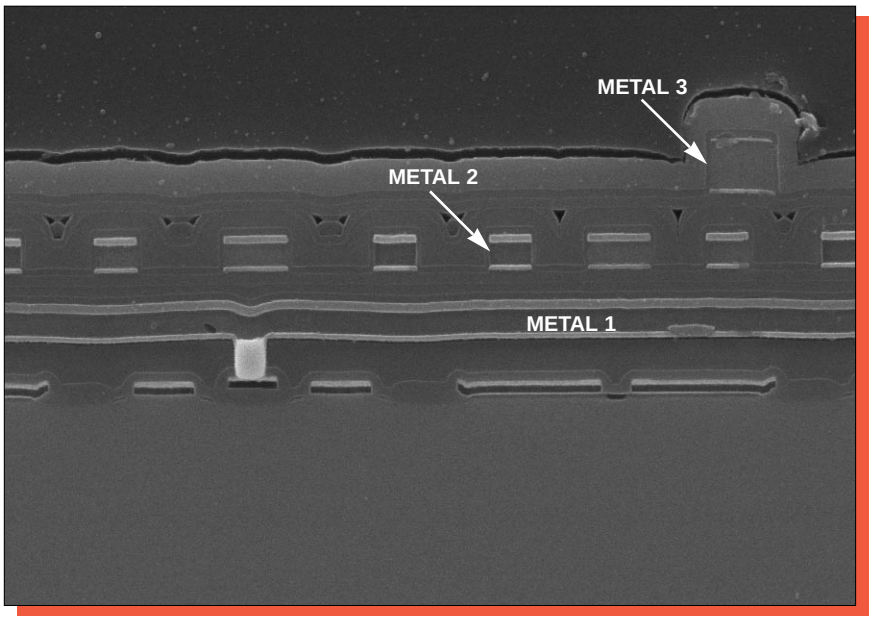


Mag. 1150x

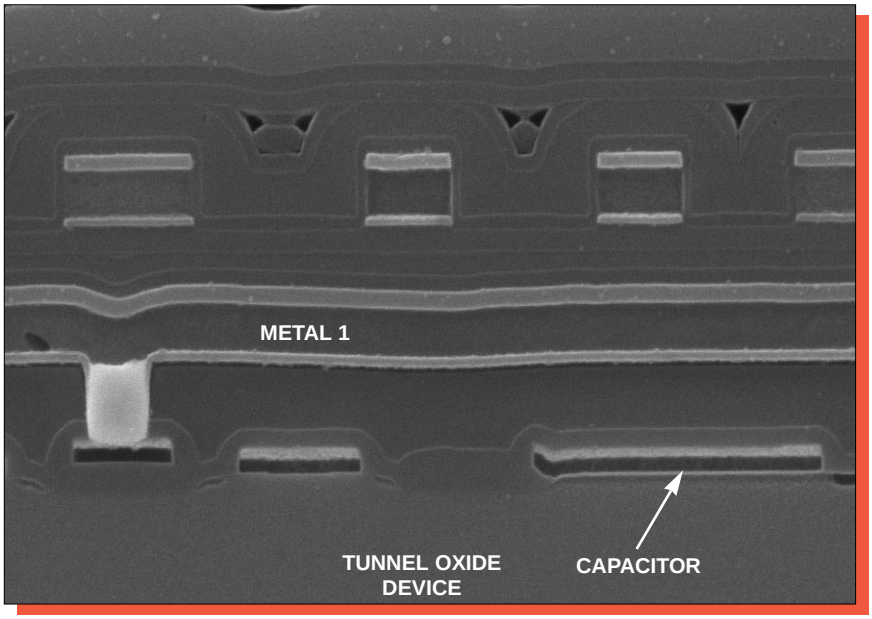


Mag. 31,000x

Figure 36. Detailed SEM views of the EEPROM cell. 60°.

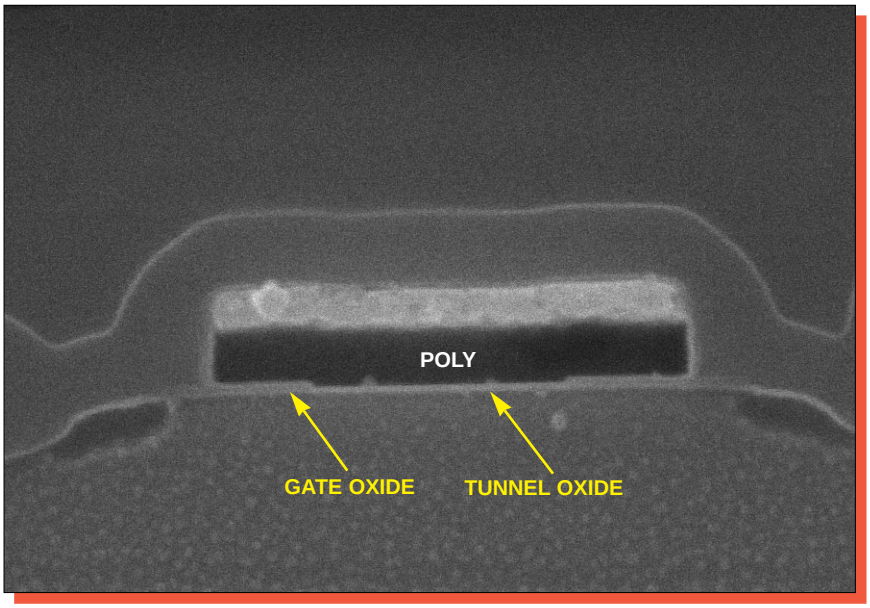


Mag. 6500x

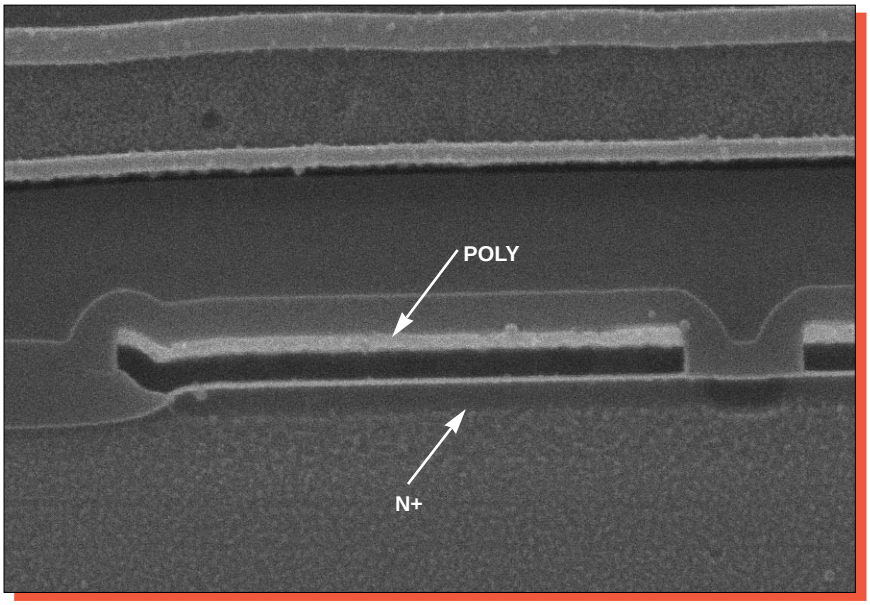


Mag. 13,000x

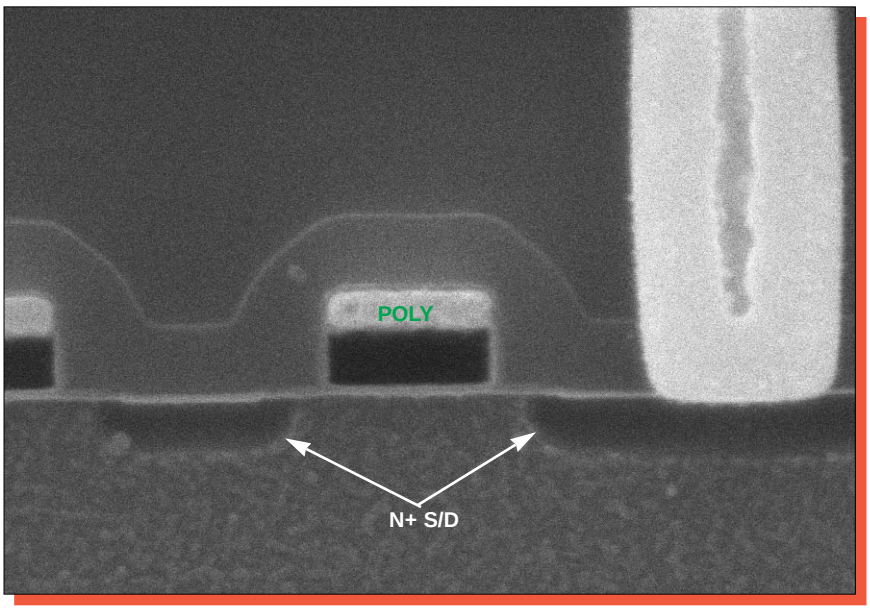
Figure 37. SEM section views of the EEPROM cell.



Mag. 52,000x

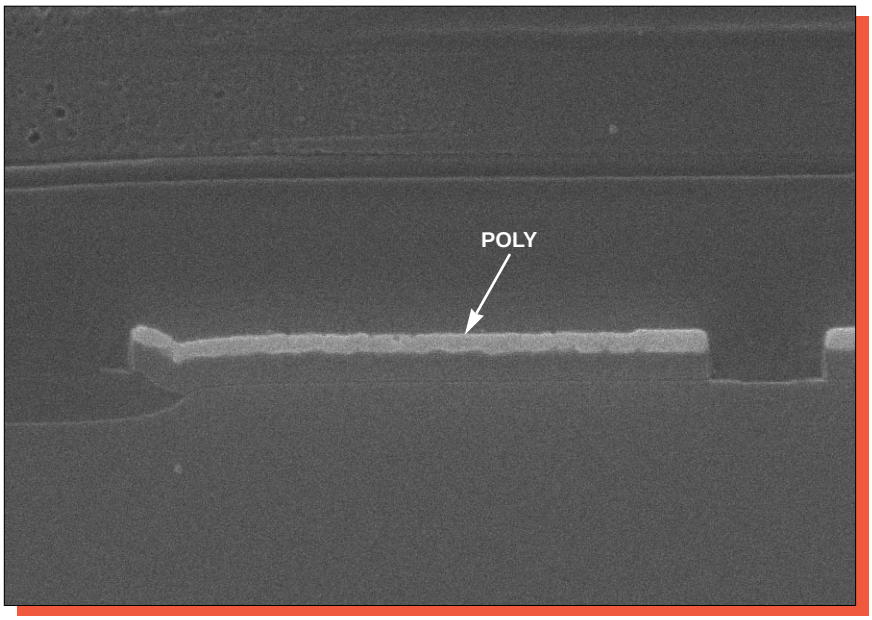


Mag. 26,000x

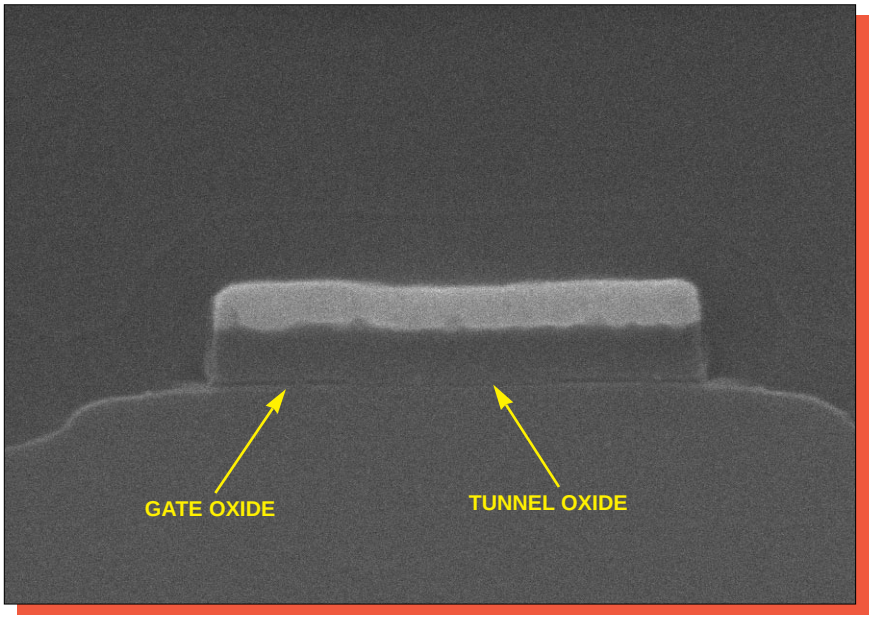


Mag. 52,000x

Figure 38. Detailed SEM section views of the EEPROM cell. Silicon etch.

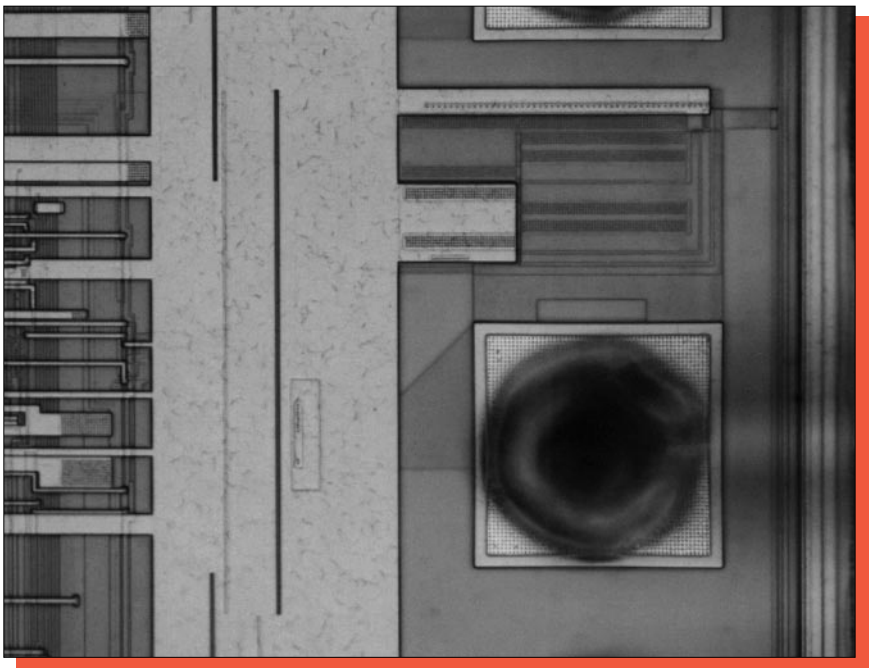


Mag. 26,000x

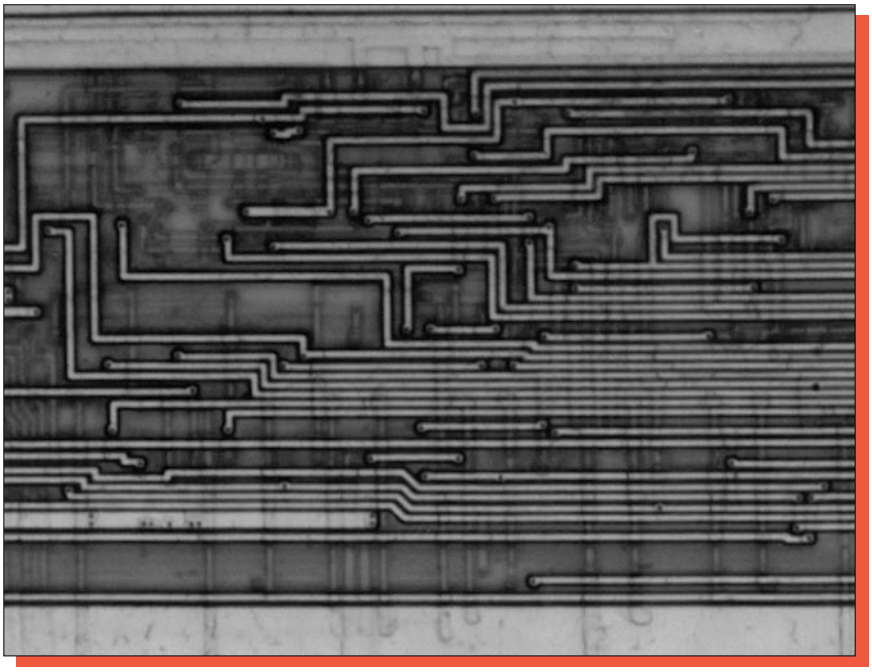


Mag. 52,000x

Figure 39. SEM section views of the EEPROM cell. Glass etch.



Mag. 320x



Mag. 800x

Figure 40. Optical views of an I/O structure and typical device circuitry.