Construction Analysis

UMC UM 613264F-7
2M-Bit SRAM

Report Number: SCA 9609-511

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the UMC UM613264F-7 2-megabit SRAM. Two devices packaged in a 100-pin Quad Flat Packs (QFPs) were received for the analysis. One device was mounted for package section and the other was used for cross section and delayering. The devices were date coded 9631.

MAJOR FINDINGS

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.3 micron N-channel, 0.4 micron P-channel).

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application*

TECHNOLOGY DESCRIPTION

Assembly:

- The device was packaged in a 100-pin Quad Flat Pack (QFP).
- External pins (gull-wing) were externally plated with tin-lead (SnPb) solder.
- The die was mounted to the header using silver-epoxy.
- Lead-locking provisions (anchors) were present at some pins.
- Die separation by sawn dicing (full depth).
- Wirebonding by the thermosonic ball bond method using 1.1 mil gold wire.
- Numerous pins were not connected.
- Multiple bonding wires were noted.

Die Process:

- Fabrication process: Selective oxidation CMOS process employing P-wells in an N substrate (no epi).
- Final passivation: Passivation consisted of a layer of nitride over a layer of silicon-dioxide.
- Metallization: Two levels of metal defined by dry-etch techniques. Metal 2 consisted of aluminum with a titanium-nitride cap and titanium barrier. Aluminum filled vias were used at this level. Metal 1 consisted of aluminum with titanium-nitride cap and barrier. A thin titanium adhesion layer was used under the metal 1 barrier. Metal 1 used tungsten plugs for contacts.
- Design features: No slotted bus lines were present and no bus lines had beveled corners.

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectric: Interlevel dielectric consisted of two layers of glass with a planarizing glass (SOG) layer in between. The filler glass was subjected to an etchback.

- Pre-metal dielectric: Consisted of reflow glass over various densified oxides. This layer was reflowed prior to contact cuts only.

- Poly: Two layers of poly were employed. Poly 1 (poly 1 and tungsten silicide) was used to form all gates, fuses, word lines and to distribute GND in the cell array. Poly 2 was used in the cell array to form the pull up resistors, bit line contact pads and to distribute Vcc.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place.

- Wells: P-well in an N substrate.

- Fuses: Poly 1 redundancy fuses were present on the device. No blown fuses were noted. Passivation and oxide cutouts were made over the fuses. Fuses were located along the column and row decode and in the periphery.

- Memory array: The memory cells consisted of a standard 4T NMOS SRAM cell design. Poly 1 formed the word lines, select gates, storage gates and distributed GND. Poly 2 formed the “pull up” resistors, bit line contact pads and distributed Vcc. Metal 1 formed the bit lines and Metal 2 was used to distribute GND.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 6**

Questionable Items:[1] None.

Special Features: None.

General Items:

- The device was packaged in a 100-pin QFP with gull-wing leads.
- Overall quality: Normal. No cracks or voids were noted on the external or internal portions of the package.
- Leadframe: The leadframe was constructed of copper and plated externally with tin-lead solder. Plating was complete and no voids were noted. No gaps were present at the lead exit.
- Dicing: Dicing was by the sawn method (full depth) and was of normal quality with no large chips or cracks.
- Die attach: Silver-epoxy of normal quality. No significant voiding was noted.
- Wirebonding: Thermosonic ball bond method using 1.1 mil gold wire. Bonds were well formed and were of good placement. Bond pull strengths were good with no bond lifts (see page 10).

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process: **Figures 7 - 36**

Questionable Items:[1] None.

Special Features:

- Sub-micron gate lengths (0.3 micron N-channel, 0.4 micron P-channel).

General Items:

- Fabrication process: Selective oxidation CMOS process employing P-wells in an N substrate (no epi). No significant problems were found in the process.

- Design implementation: Die layout was clean. Alignment was good at all levels. No slotted bus lines were present and no bus lines had beveled corners.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Final passivation: Passivation consisted of a layer of nitride over a layer of silicon-dioxide. Passivation integrity tests indicated defect-free passivation. Edge seal was good.

- Metallization: Two levels of metallization. Metal 2 consisted of aluminum with a titanium-nitride cap and titanium barrier. Metal 2 vias were aluminum filled. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier and tungsten filled plugs and a titanium-nitride cap and barrier. A thin titanium adhesion layer was present under the Metal 1 barrier.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal patterning: Both metal layers were defined by a dry etch of good quality. No problems were found.

- Metal defects: No notching or voiding of either metal layer was found. No silicon nodules were found following the removal of the metal layers.

- Metal step coverage: Virtually no metal thinning was noted at either metal layer due to Metal 2 filled vias and Metal 1 tungsten plugs.

- Interlevel dielectric: Interlevel dielectric consisted of two layers of glass with a planarizing glass (SOG) layer in between. The filler glass was subjected to an etchback. No problems were found with the dielectric layers.

- Pre-metal dielectric: Reflow glass over various densified oxides were used under Metal 1. Reflow was performed prior to contact cuts. No problems were found with any of these layers.

- Poly: Two layers of poly. Poly 1 (poly 1 and tungsten silicide) was used to form all gates and fuses on the die and the word and GND lines in the array. Poly 2 was used in the cell array to form bit line contact pads, "pull up" resistors and to distribute Vcc.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. No step was noted in the local oxide.

- Diffusions: Standard implanted N+ and P+ diffusions were used for sources and drains. An LDD process was used employing oxide sidewall spacers. The spacers were left in place. No problems were found in any of these areas.

- Wells: P-wells were used in an N substrate (no epi present). No problems were apparent.

- Buried contacts: Interpoly/buried contacts were used in the cell array. No problems were found.

ANALYSIS RESULTS II (continued)

- Fuses: All polycide 1 redundancy fuses had passivation and oxide cutouts over them. No blown fuses were present. Fuses were located along the column and row decodes and in the periphery.

- Memory array: The memory cells consisted of a standard 4T NMOS SRAM cell design. Poly 1 formed the word lines, select gates, storage gates and distributed GND. Poly 2 formed the "pull up" resistors, bit line contact pads, and distributed Vcc. Metal 1 formed the bit lines and Metal 2 was used to distribute GND. Cell pitch was 2.5 x 4.5 microns.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Package section

Decapsulate

Internal optical inspection

SEM inspection of assembly features and passivation

Wirepull test

Passivation integrity test

Delayer to Metal 2 and inspect

Aluminum removal (Metal 2) and inspect barrier

Delayer to Metal 1 and inspect

Aluminum removal (Metal 1) and inspect barrier

Delayer to poly/substrate and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	N
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	N
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire.

Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	G
Metal integrity	G
Metal registration	N
Contact coverage	N
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

(Logo) UMC
UM61L3264 F-7
9631S RM 6G53

WIREBOND STRENGTH

Wire material:	1.1 mil gold wire
Die pad material:	aluminum
Package lands:	silver

Sample #	**1**
# of wires pulled:	45
Bond lifts:	0
Force to break - high:	15.0g
- low:	7.5g
- avg.:	12.5g
- std. dev.:	1.6

PACKAGE MATERIAL ANALYSIS

Leadframe:	Copper (Cu)
Internal plating:	Silver (Ag)
External plating:	Tin-lead solder (SnPb)
Die attach:	Silver (Ag) epoxy

DIE MATERIAL ANALYSIS

Passivation:	Layer of nitride over a layer of silicon-dioxide.
Metal 2:	Aluminum with a titanium-nitride cap and titanium barrier.
Interlevel dielectric:	Two layers of silicon-dioxide with a spin-on-glass (SOG).
Metal 1:	Aluminum with titanium-nitride cap and barrier and titanium adhesion layer.
Pre-metal dielectric:	Reflow glass (probably BPSG) over various densified oxides.
Poly 2:	Poly.
Poly 1:	Poly with tungsten silicide.

HORIZONTAL DIMENSIONS

Die size:	6.1 x 6.7 mm (240 x 265 mils)
Die area:	41 mm^2 (63,600 $mils^2$)
Min pad size:	0.1 x 0.1 mm (4.2 x 4.2 mils)
Min pad window:	0.09 x 0.09 mm (3.9 x 3.9 mils)
Min pad space:	20 microns
Min metal 2 width:	0.6 micron
Min metal 2 space:	0.6 micron
Min metal 2 pitch:	1.2 micron
Min metal 1 width:	0.6 micron
Min metal 1 space:	0.6 micron
Min metal 1 pitch:	1.2 micron
Min via M2 - M1:	0.5 micron
Min contact:	0.5 micron
Min poly 1 width:	0.3 micron
Min poly 1 space:	0.5 micron
Min gate length* - (N-channel):	0.3 micron
- (P-channel):	0.4 micron
Cell size:	11.25 $microns^2$
Cell pitch:	2.5 x 4.5 microns

**Physical gate length.*

VERTICAL DIMENSIONS

Layers:

Passivation 2:	0.65 micron
Passivation 1:	0.4 micron
Metal 2 - cap:	0.05 micron (approx.)
- aluminum:	0.9 micron
- barrier:	0.08 micron (approx.)
Interlevel dielectric - glass 2:	0.4 micron
- glass 1:	0.8 micron (average)
Metal 1 - cap:	0.06 micron (approx.)
- aluminum:	0.5 micron
- barrier:	0.1 micron
- adhesion layer:	0.1 micron
Pre-metal dielectric:	0.65 micron (average)
Poly 2:	0.05 micron (approx.)
Interpoly oxide:	0.2 micron
Poly 1 - silicide:	0.12 micron
- poly 1:	0.17 micron
Local oxide:	0.3 micron
N+ S/D diffusion:	0.14 micron
P+ S/D diffusion:	0.25 micron
P- well:	3.5 microns

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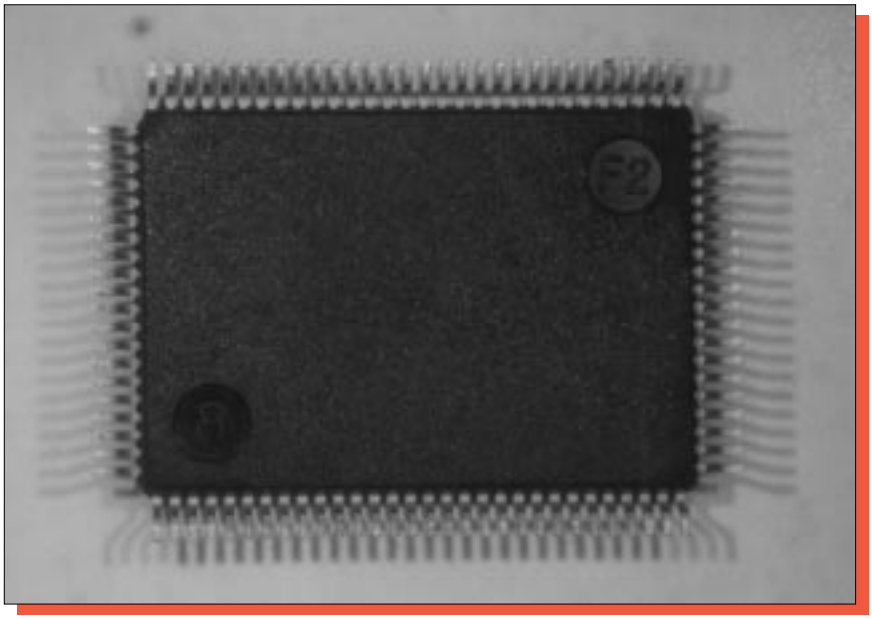
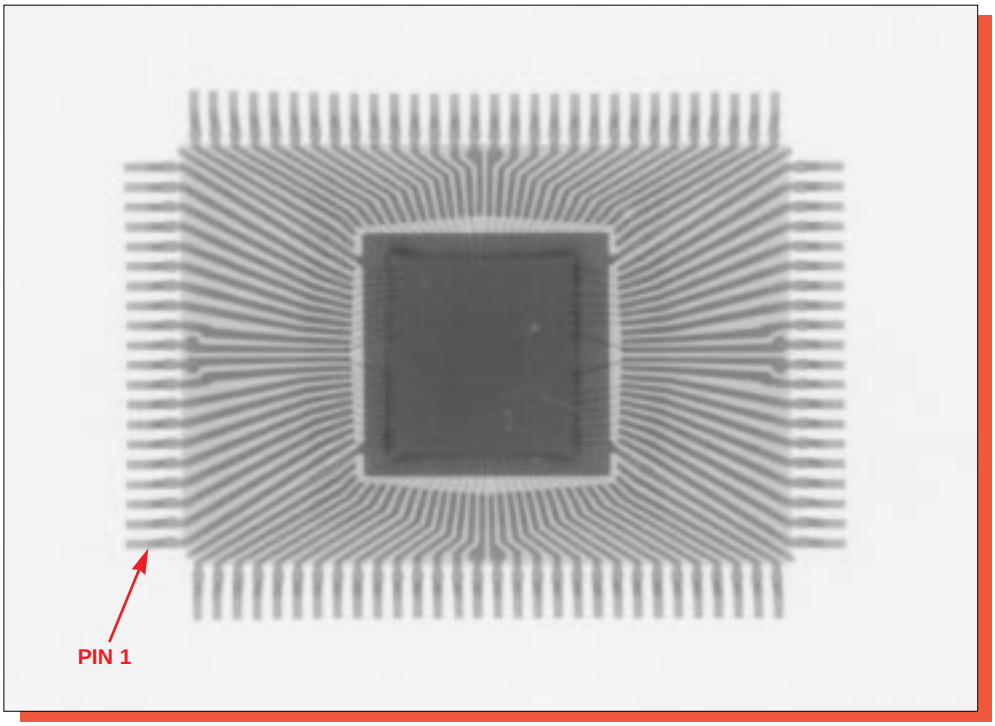


bottom

Figure 1. Package photographs of the UMC UM613264F-7. Mag. 4x.



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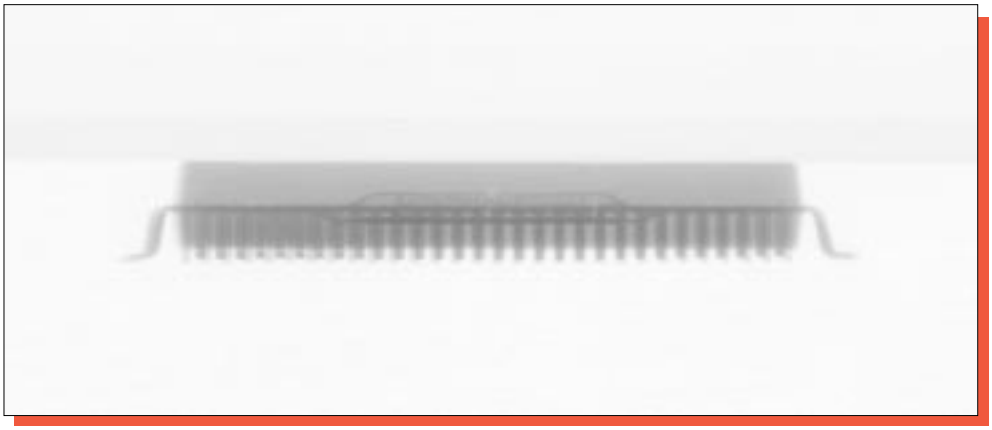
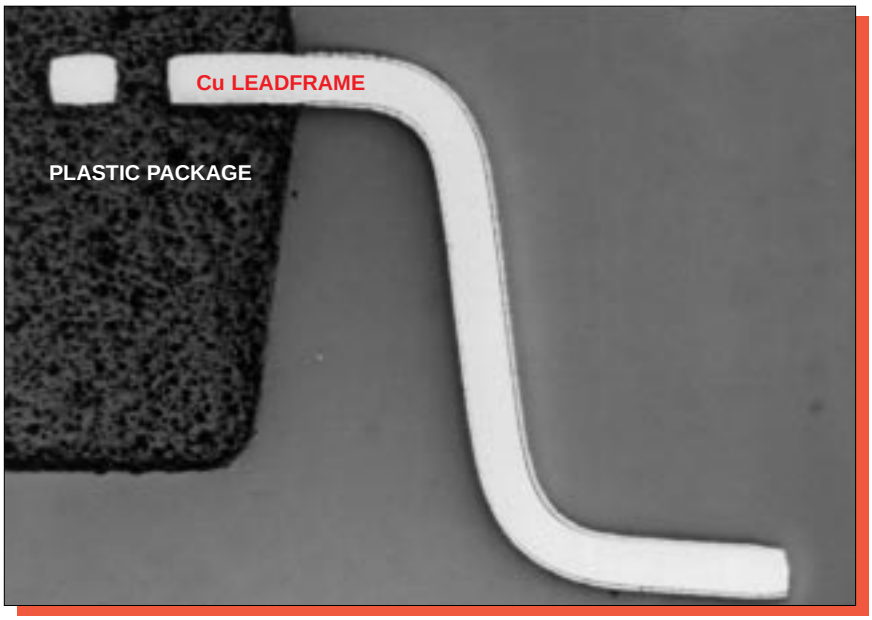


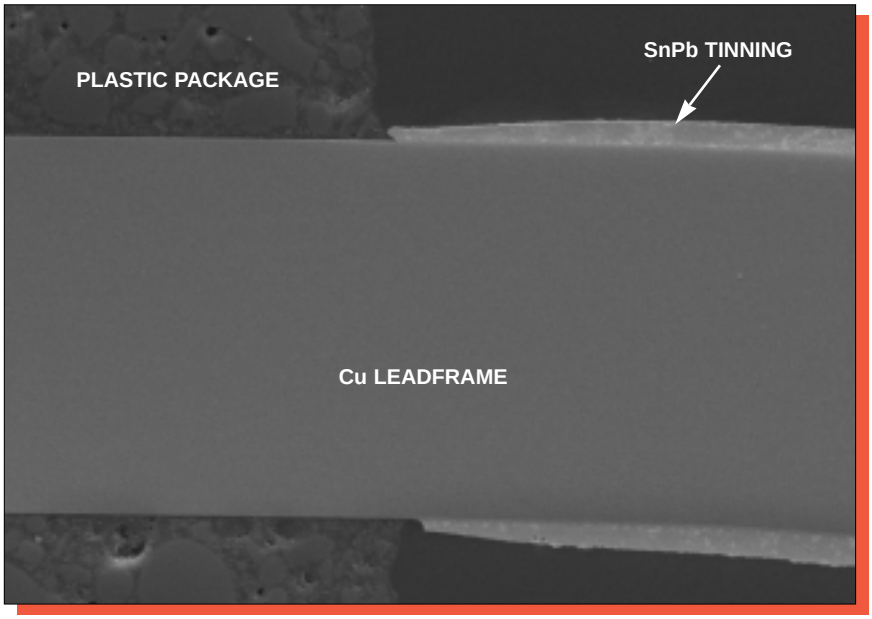
side

Figure 2. X-ray views of the package. Mag. 3.8x.

Figure 3. Package section view of general construction Mag. 13x.

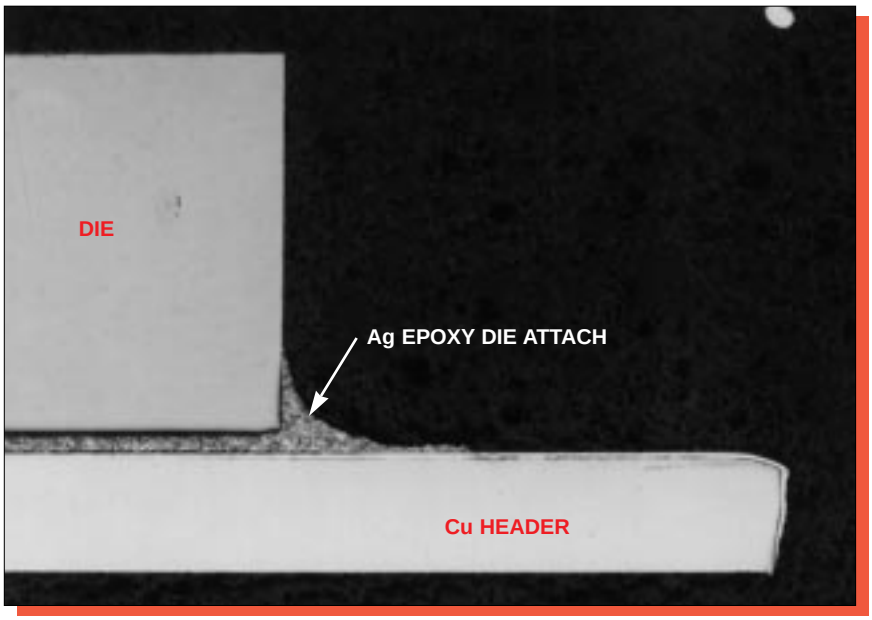


Mag. 40x

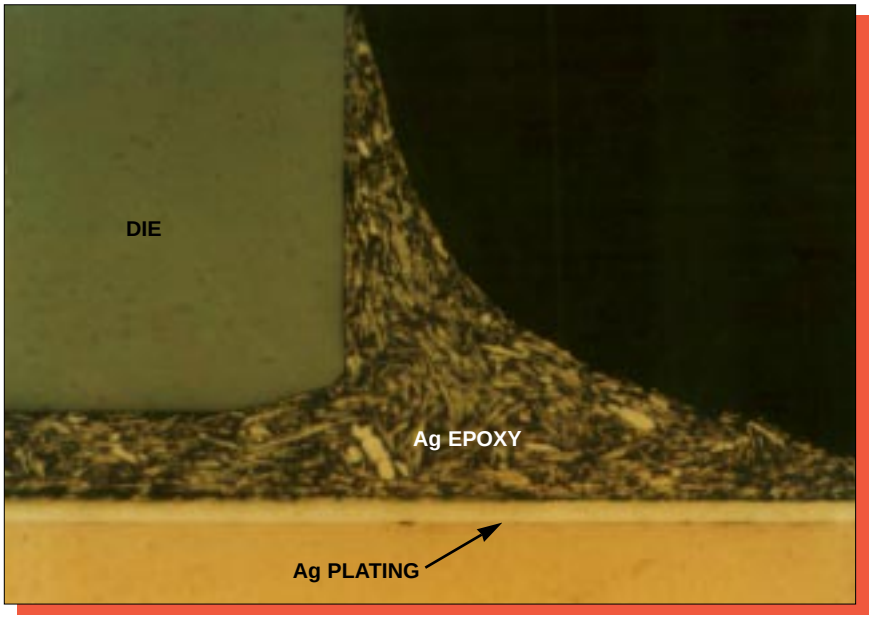


Mag. 340x

Figure 4. Package section views illustrating lead forming and lead exit.

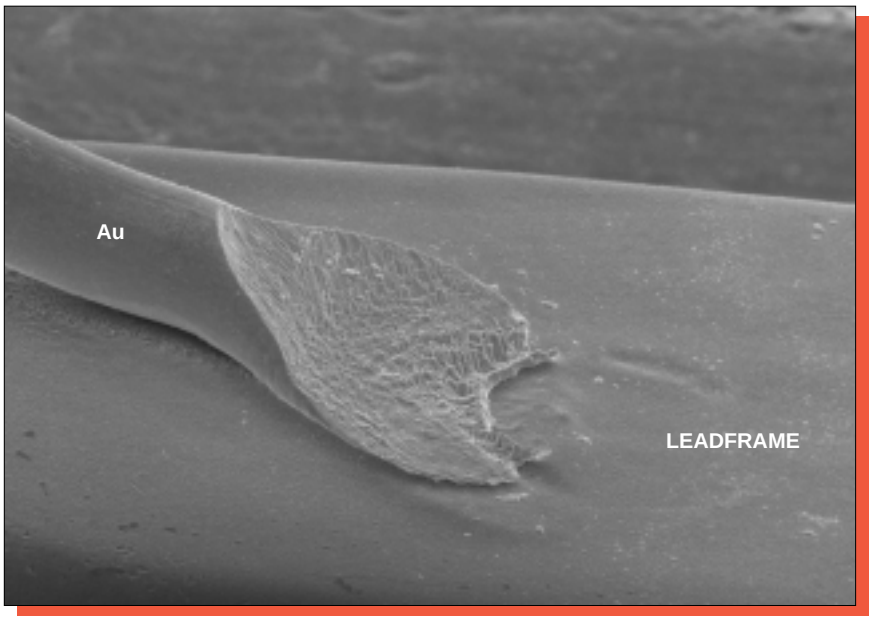


Mag. 100x

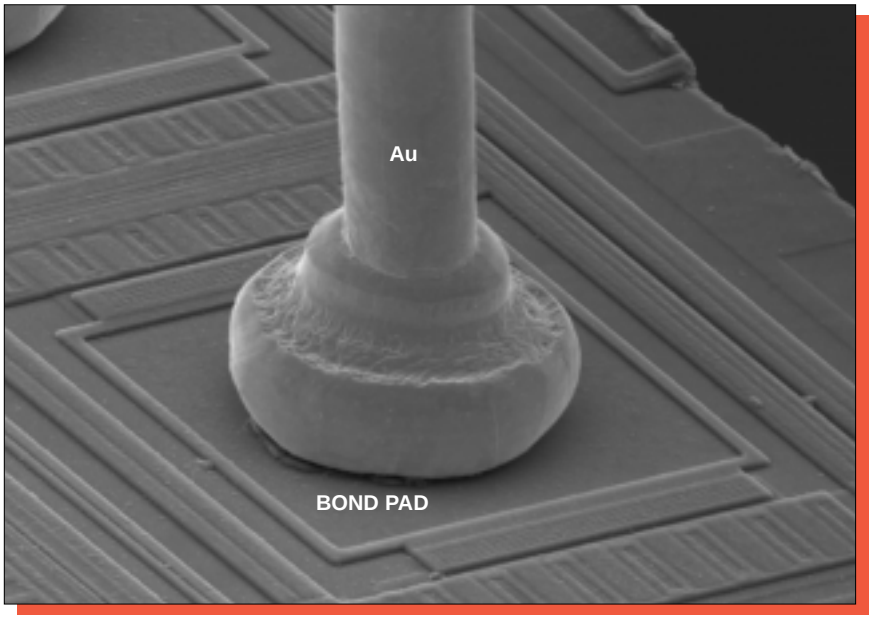


Mag. 500x

Figure 5. Package section views illustrating dicing and die attach.



Mag. 625x



Mag. 660x

Figure 6. SEM views of typical wirebonding. 60°.

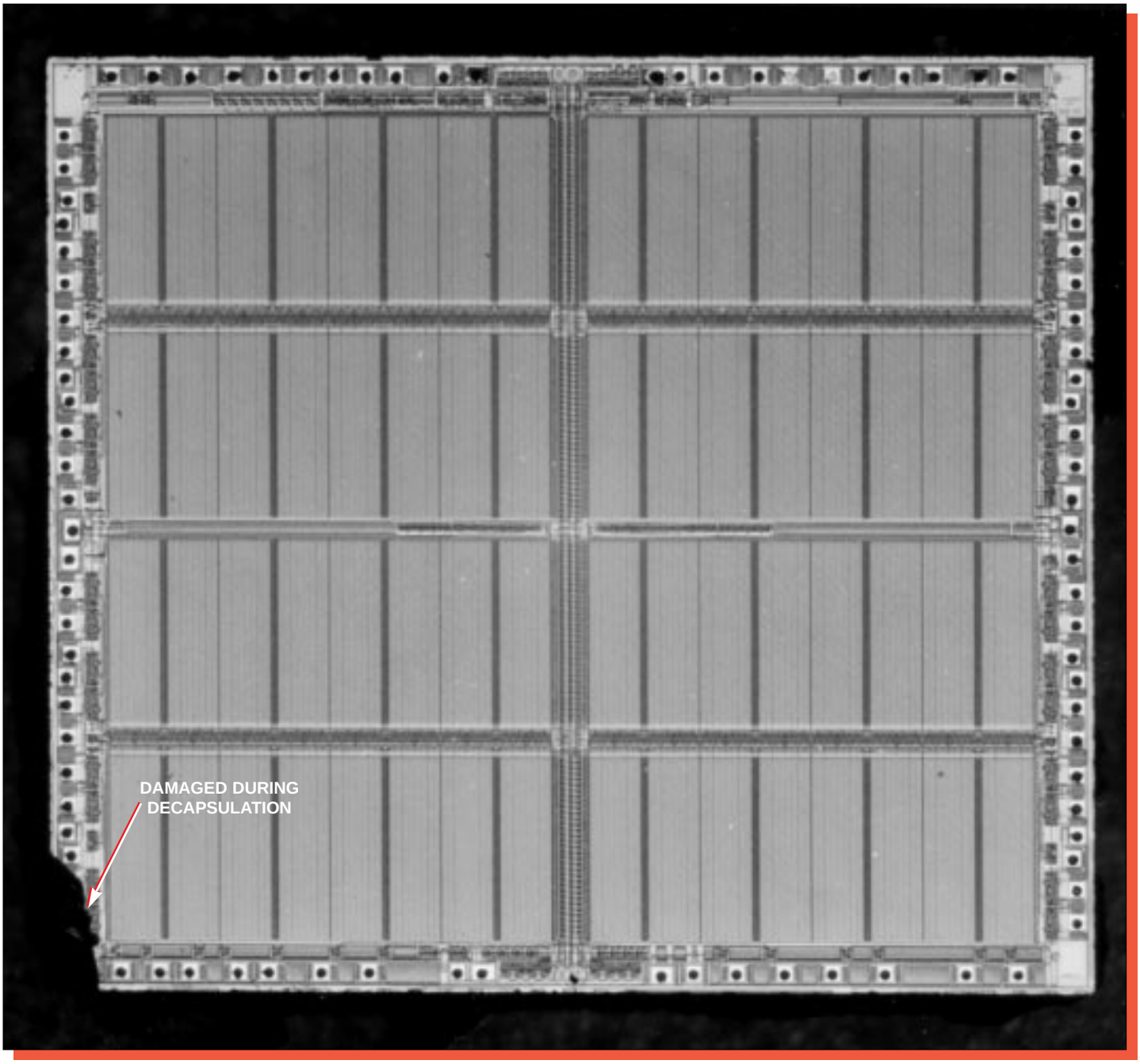
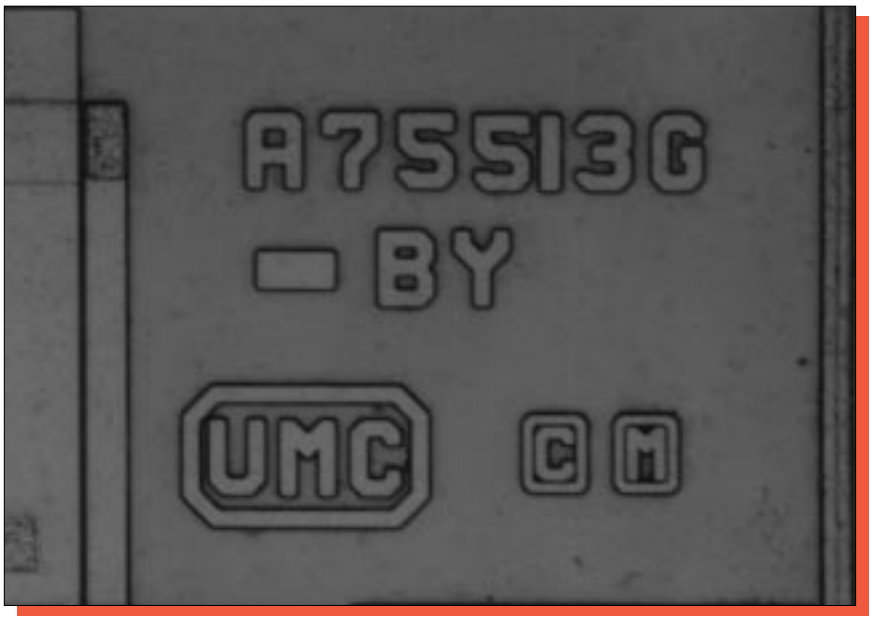


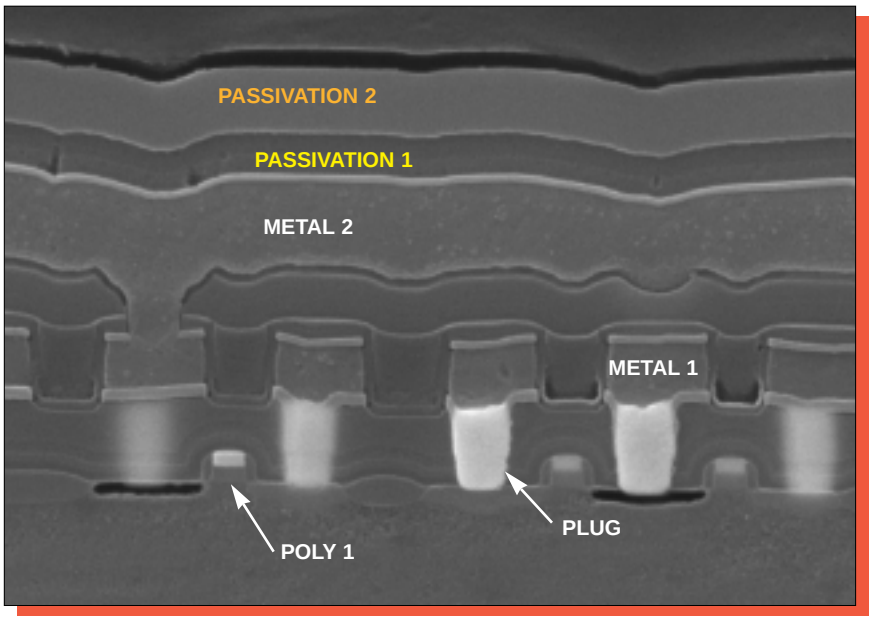
Figure 7. Whole die photograph of the UMC UM613264F-7. Mag. 13x.



Mag. 200x

Mag. 500x

Figure 8. Optical views of markings on the die surface.



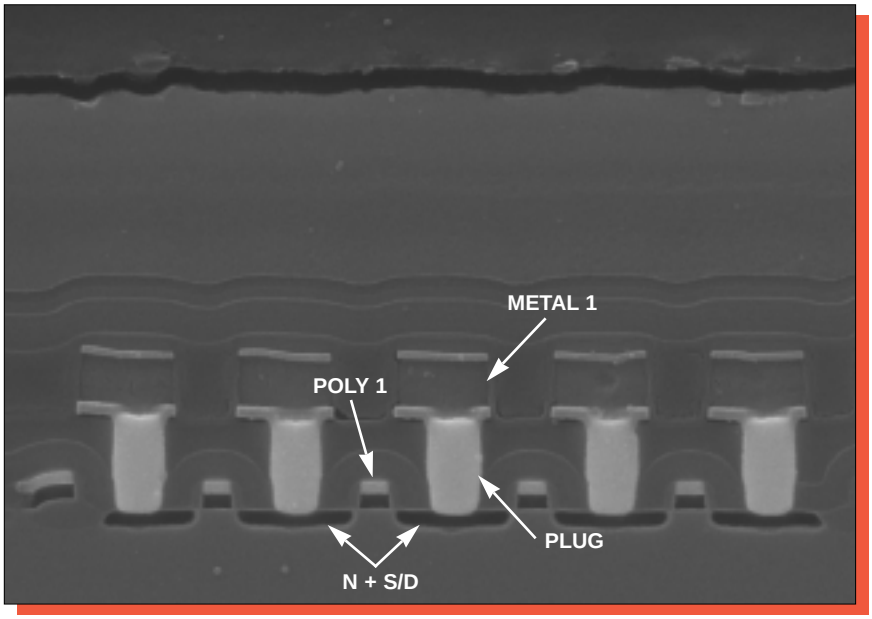
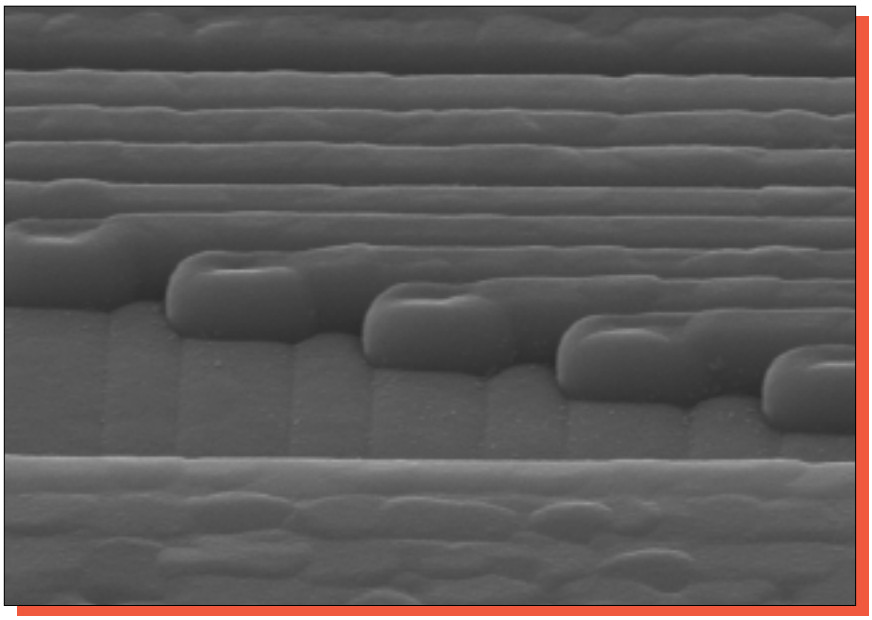
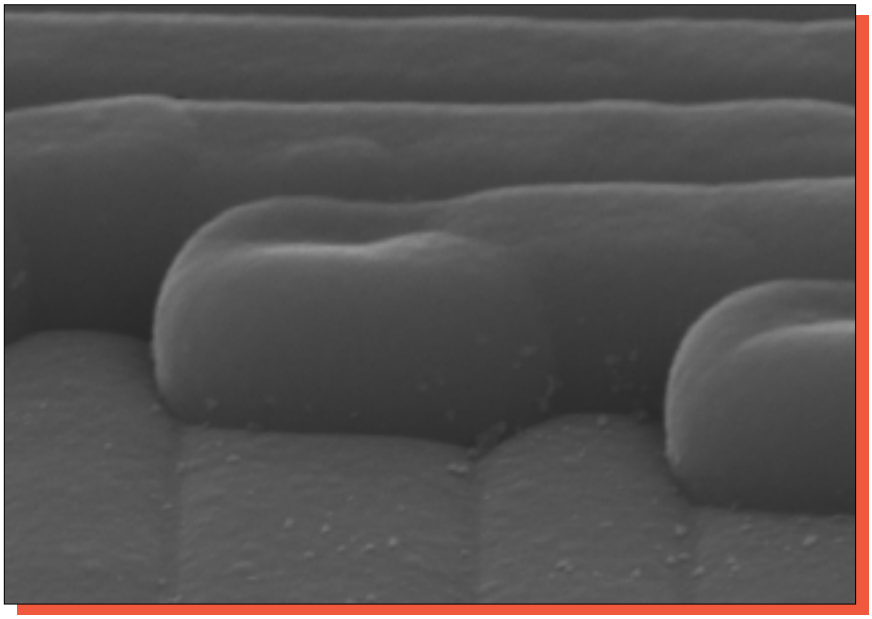


Figure 9. SEM section views illustrating general structure. Mag. 13,000x.

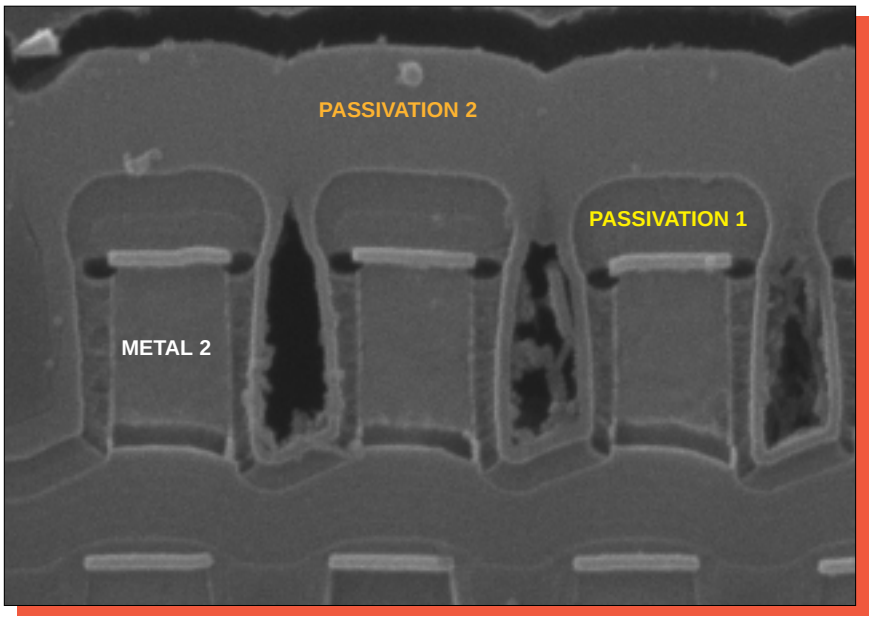


Mag. 5700x

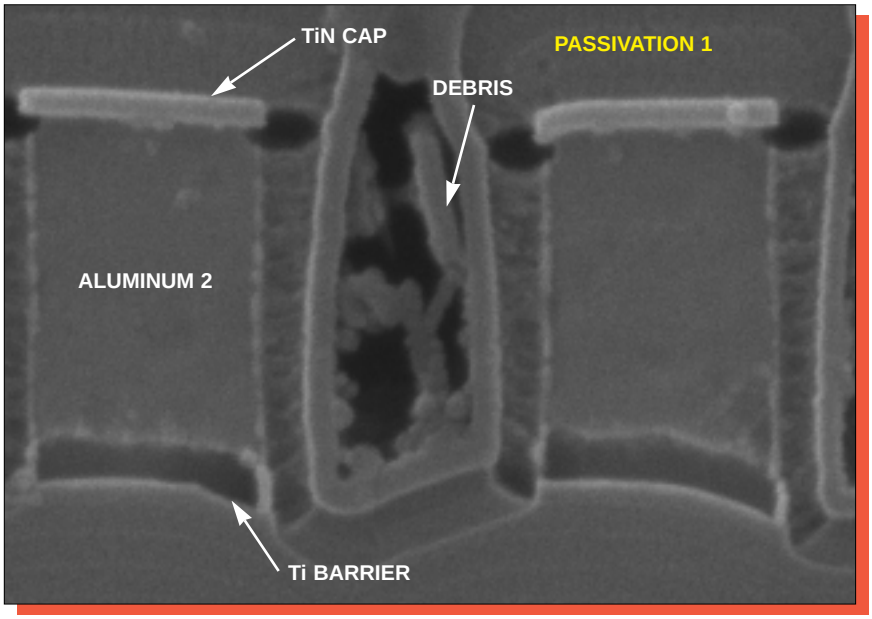


Mag. 15,000x

Figure 10. Perspective SEM views of overlay passivation coverage. 60°.

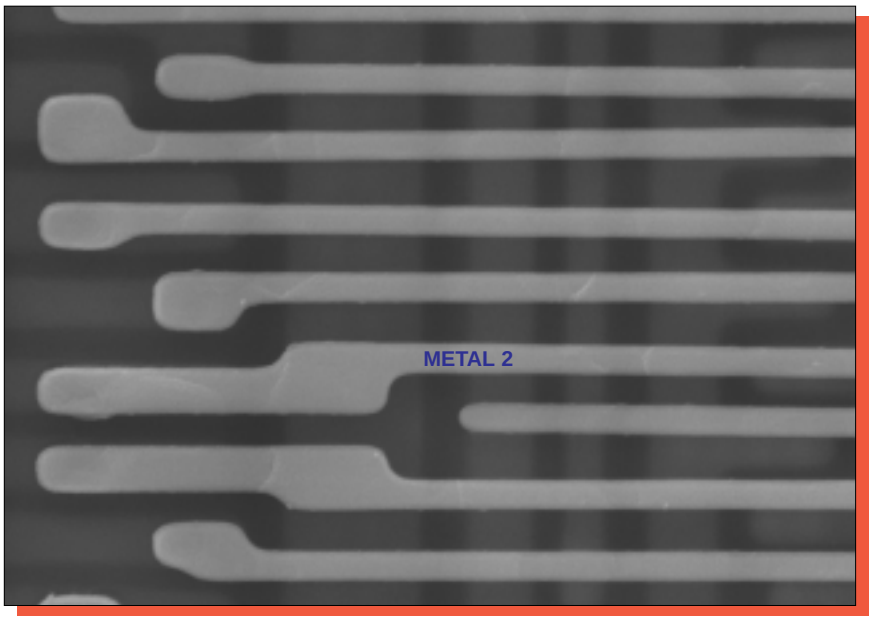


Mag. 26,000x

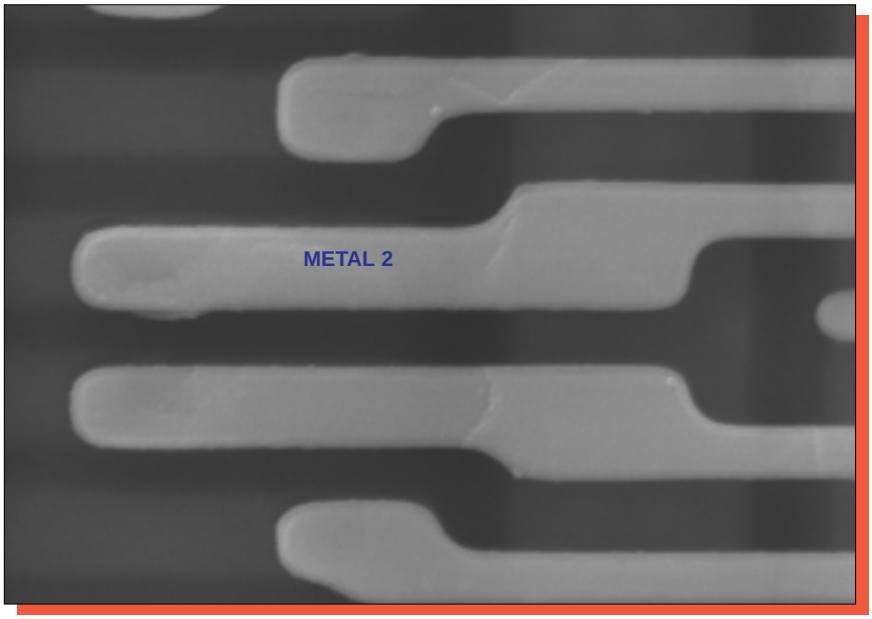


Mag. 52,000x

Figure 11. SEM section views of metal 2 line profiles.

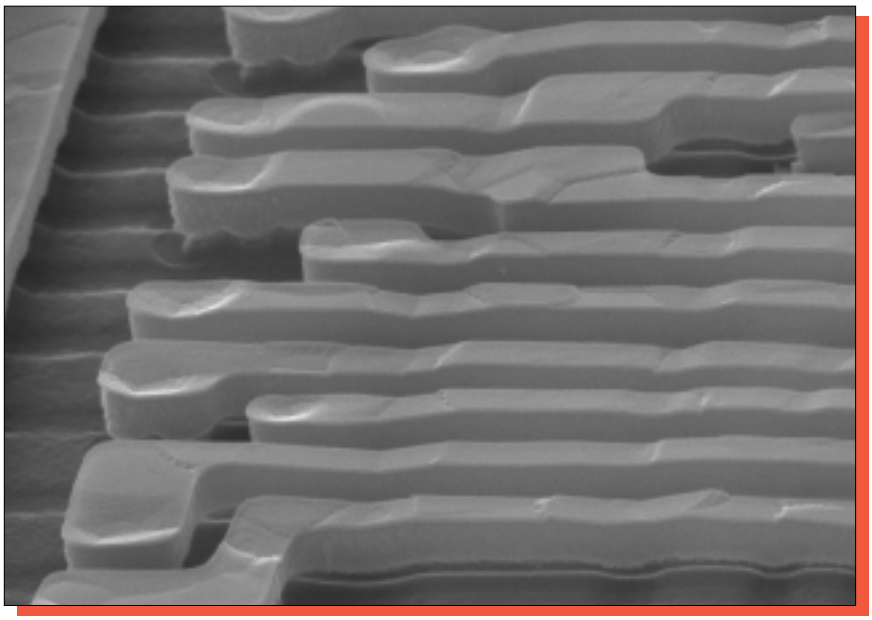


Mag. 6000x

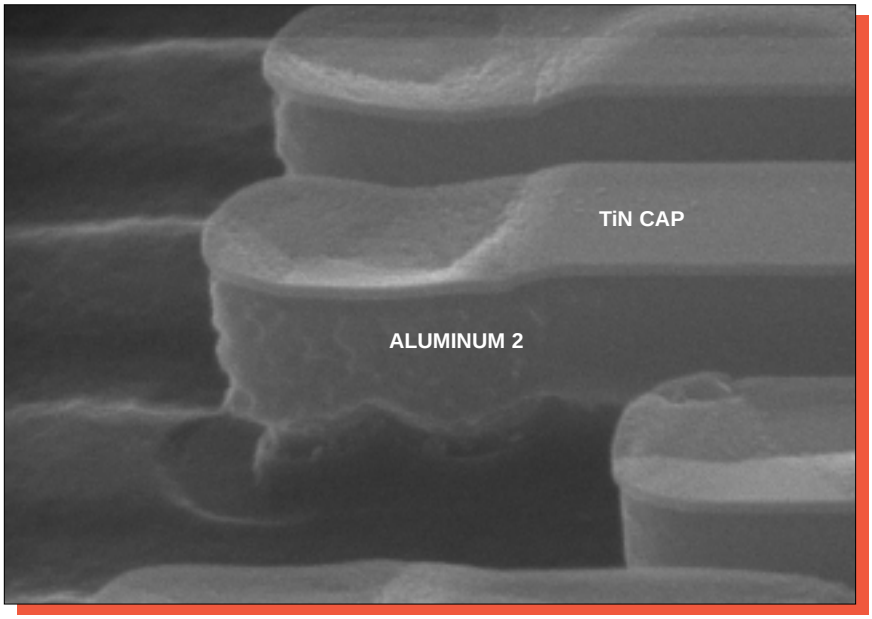


Mag. 10,000x

Figure 12. Topological SEM views of metal 2 patterning. 0°.

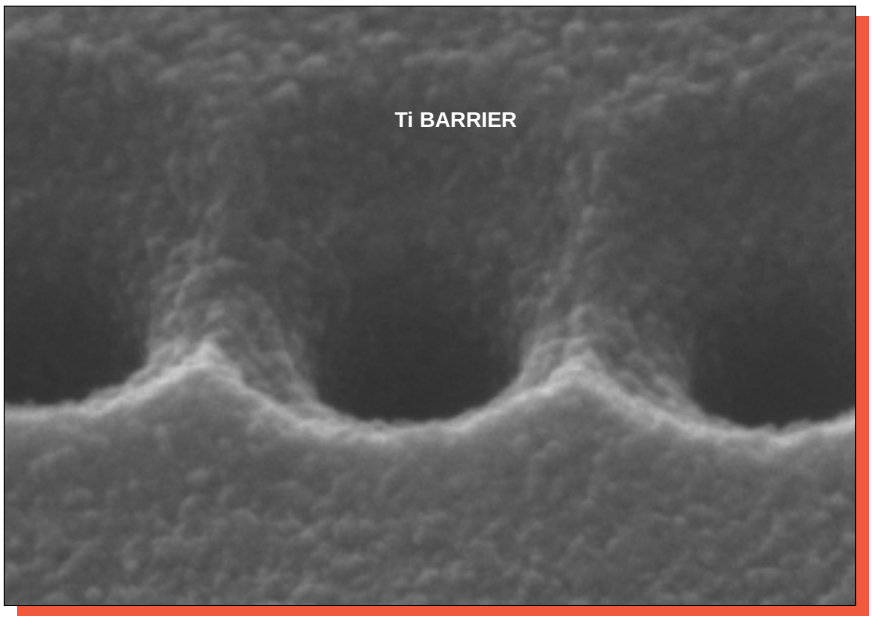


Mag. 8400x

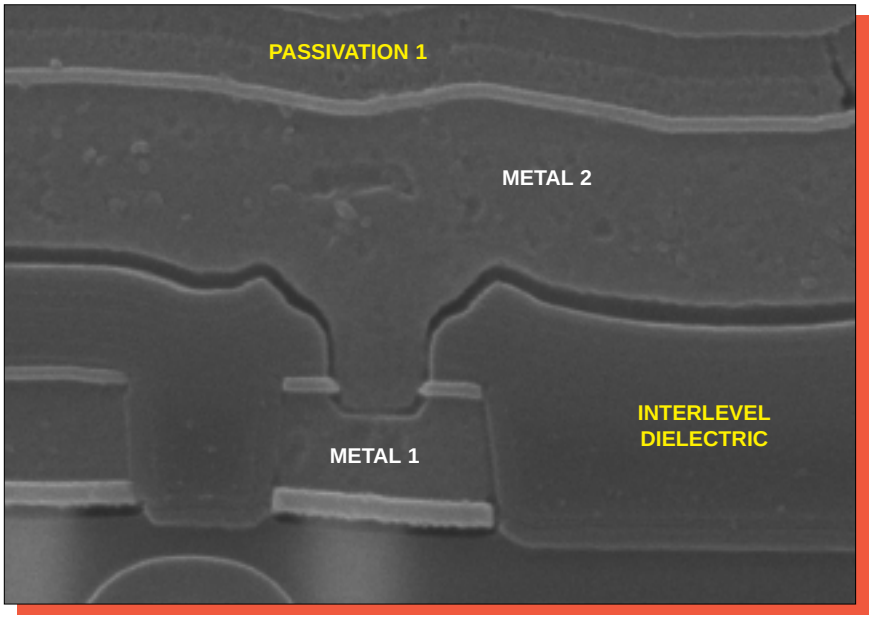


Mag. 26,000x

Figure 13. Perspective SEM views of metal 2 coverage. 60°.

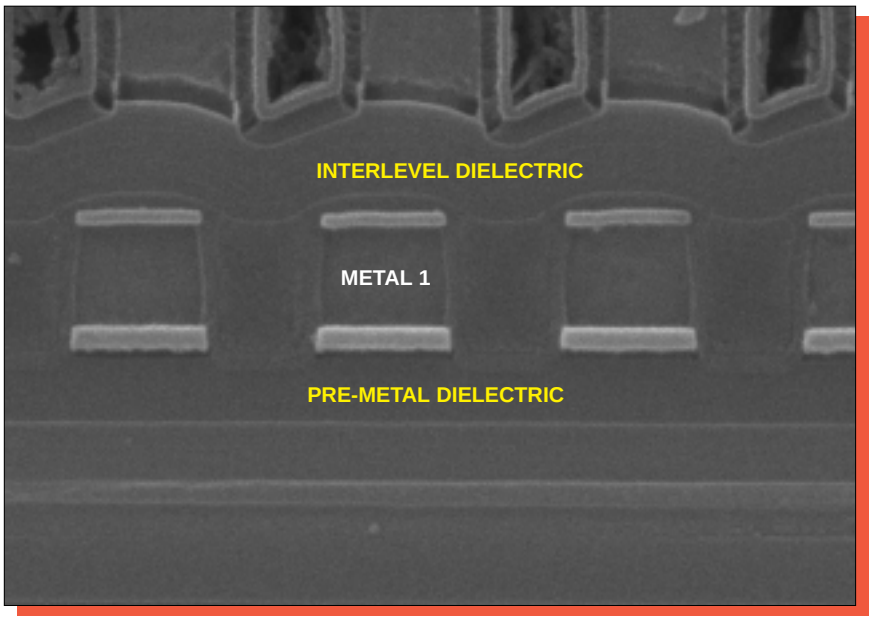


Mag. 52,000x, 45°

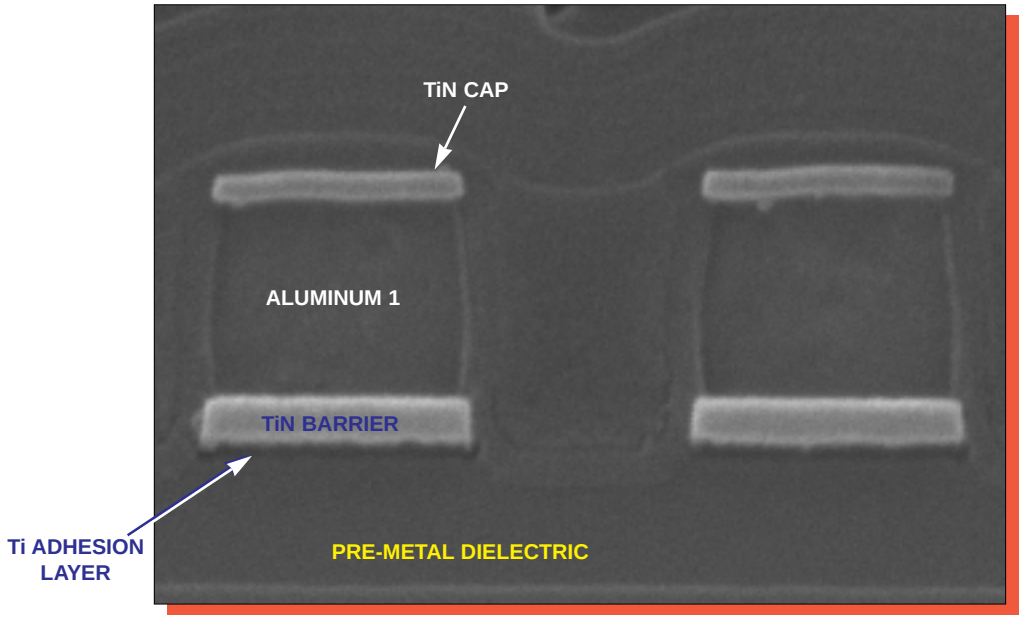


Mag. 26,000x

Figure 14. SEM views of barrier coverage and metal 2-to-metal 1 via.

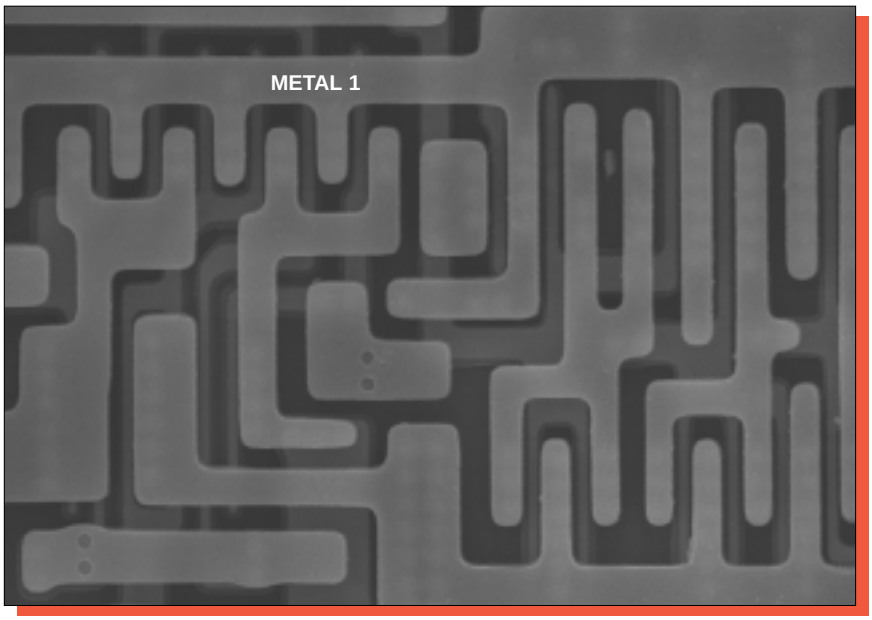


Mag. 26,000x

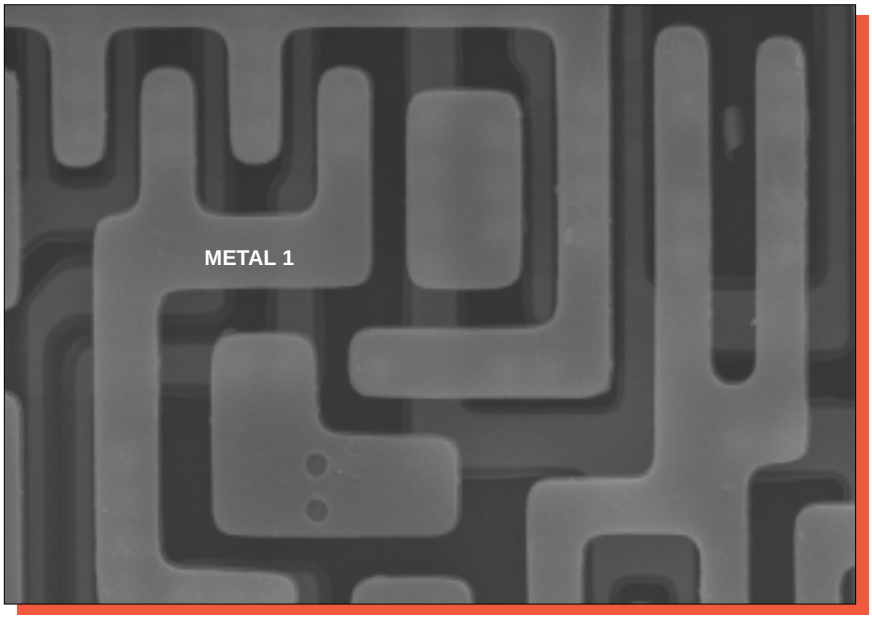


Mag. 52,000x

Figure 15. SEM section view of metal 1 line profiles.

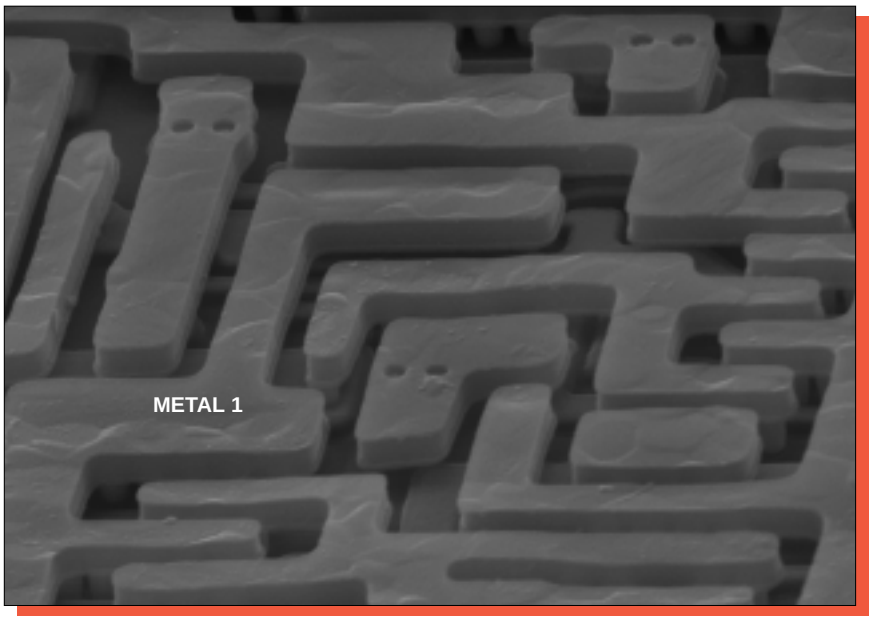


Mag. 4000x

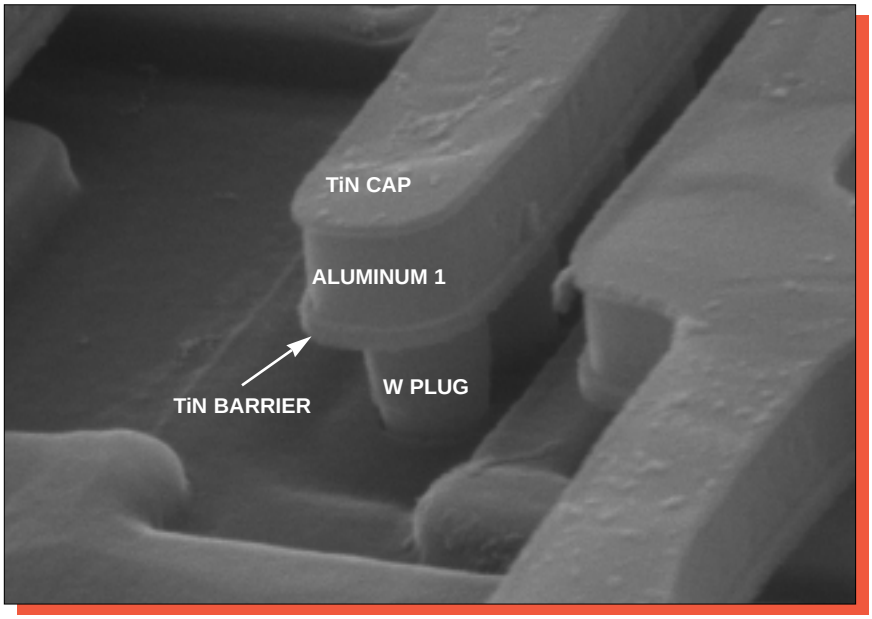


Mag. 7400x

Figure 16. Topological SEM views of metal 1 patterning. 0°.

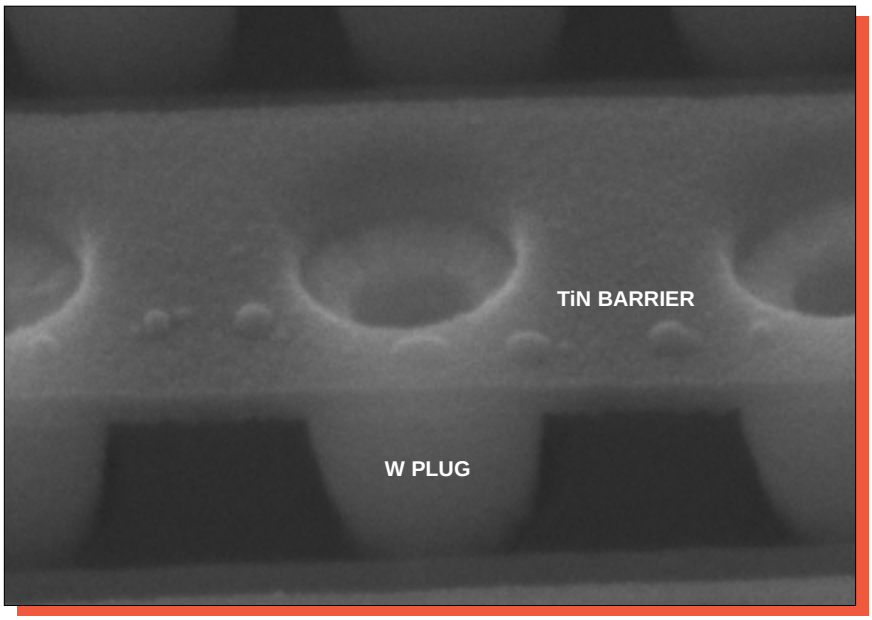


Mag. 6500x

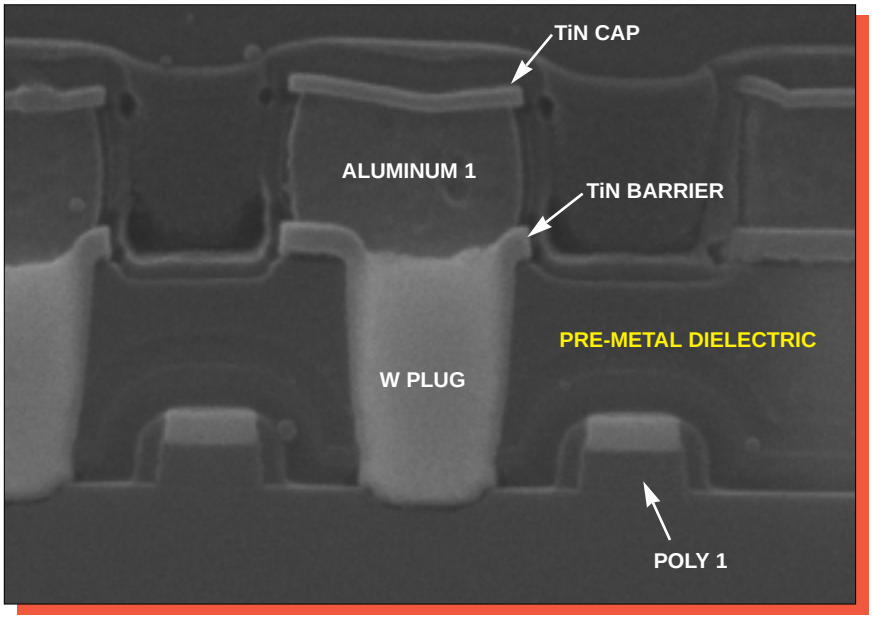


Mag. 26,000x

Figure 17. Perspective SEM views of metal 1 step coverage. 60°.



Mag. 52,000x



glass etch, Mag. 35,000x

Figure 18. SEM views of barrier coverage and metal 1 contact.

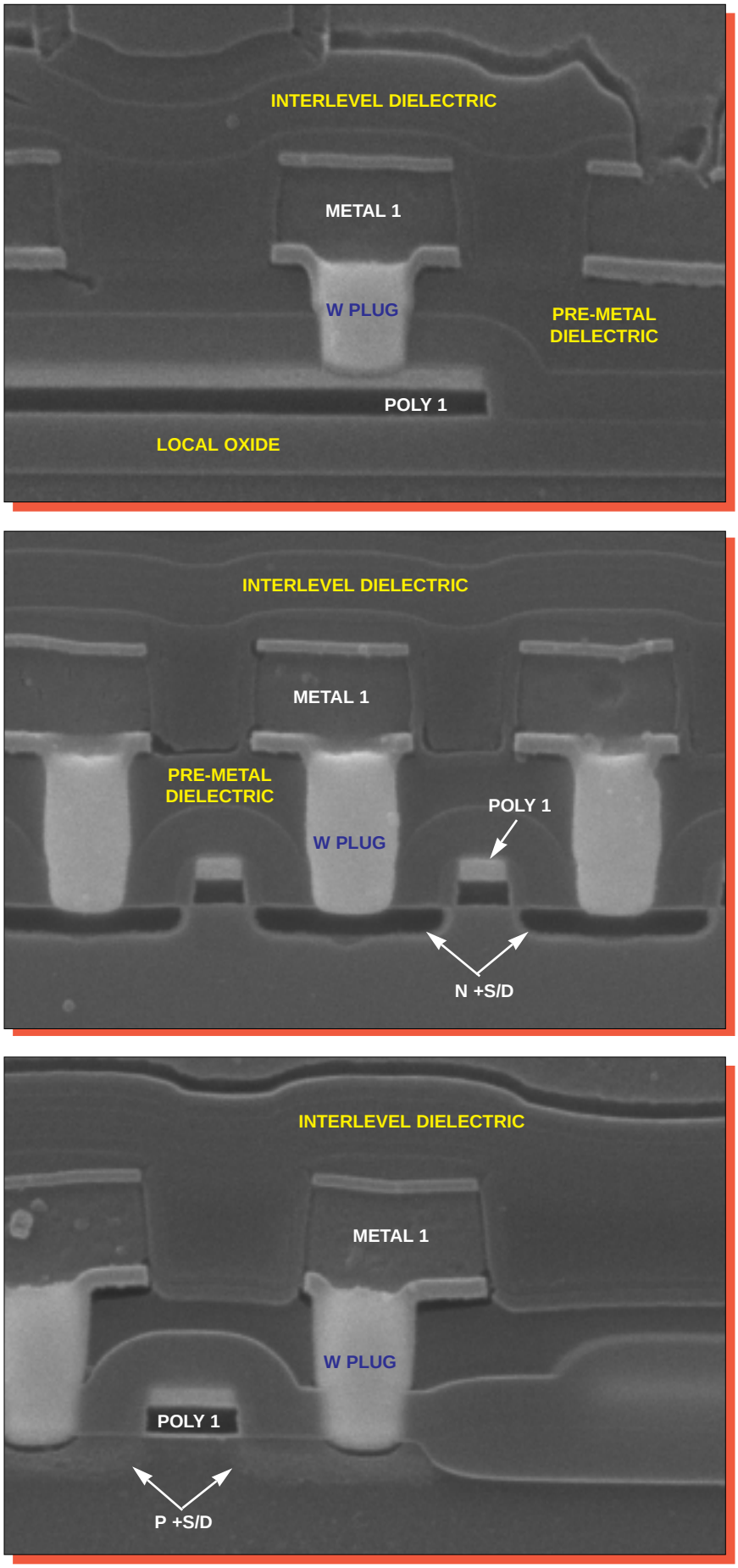
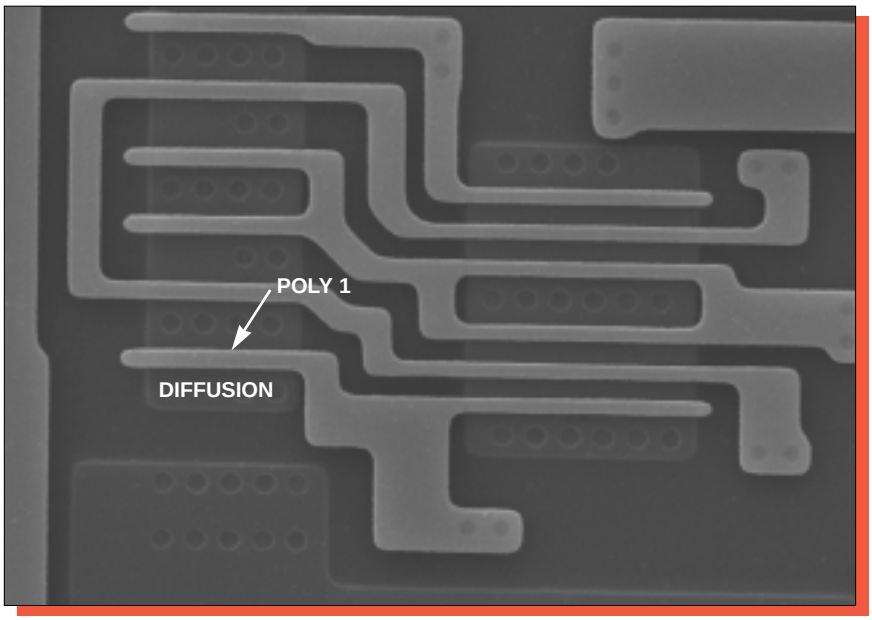
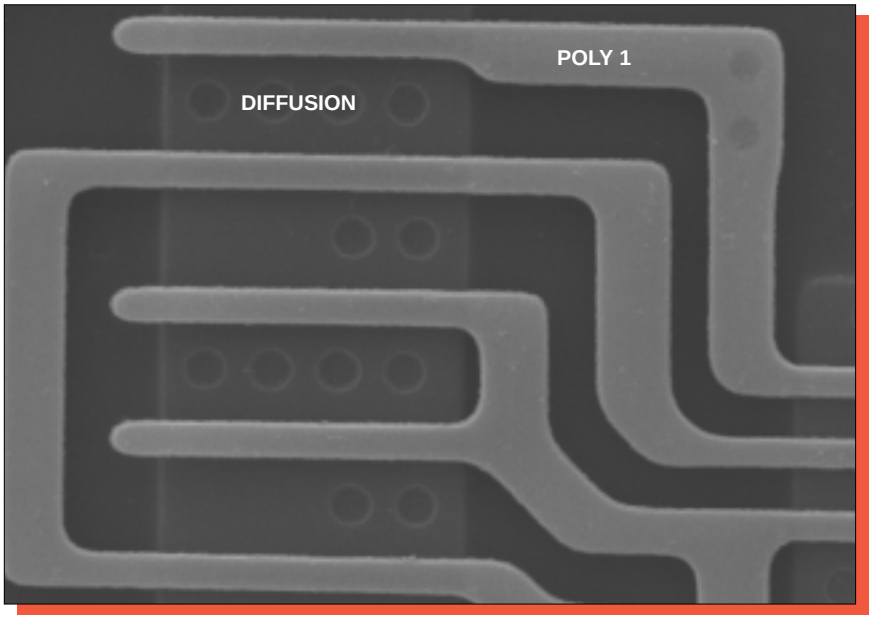


Figure 19. SEM section views of metal 1 contacts. Silicon etch, Mag. 26,000x.

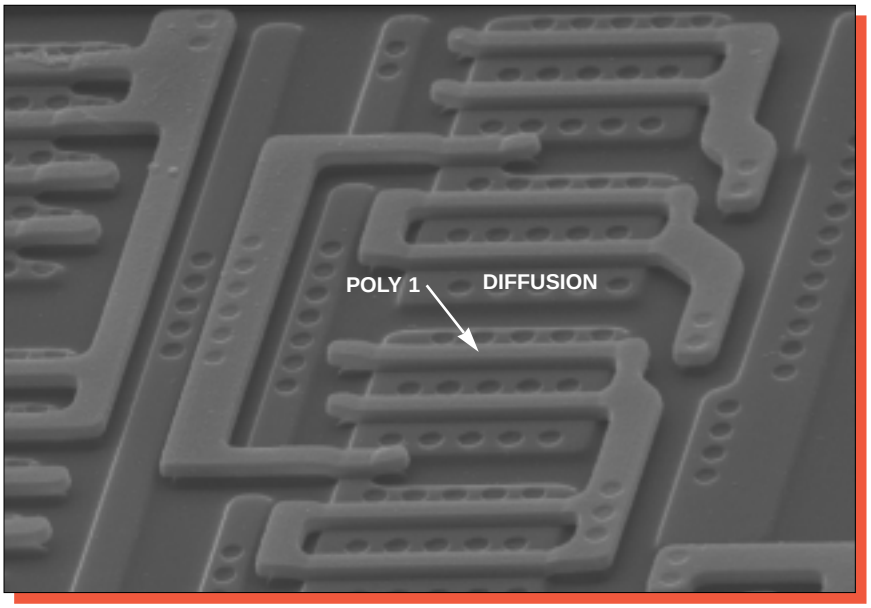


Mag. 5500x

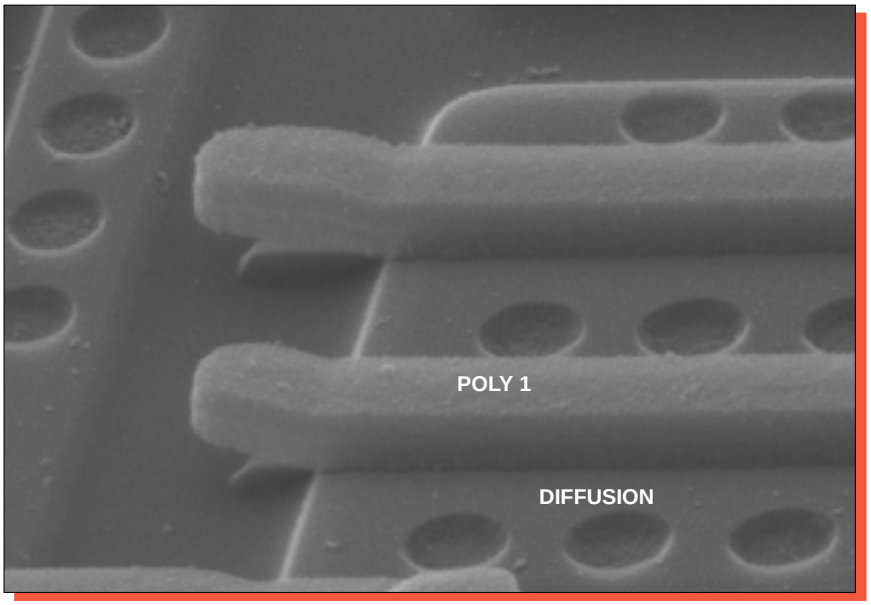


Mag. 11,000x

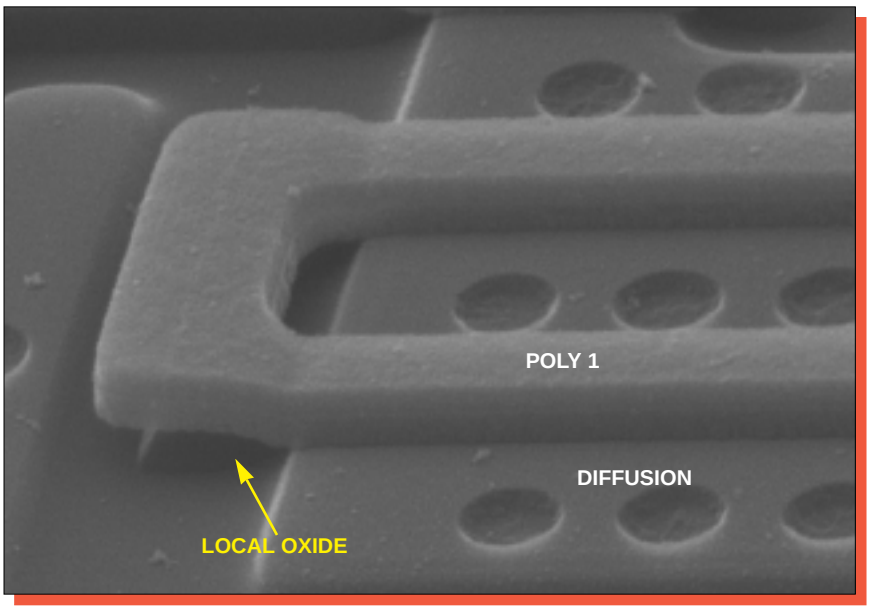
Figure 20. Topological SEM views of poly patterning. 0°.



Mag. 6500x

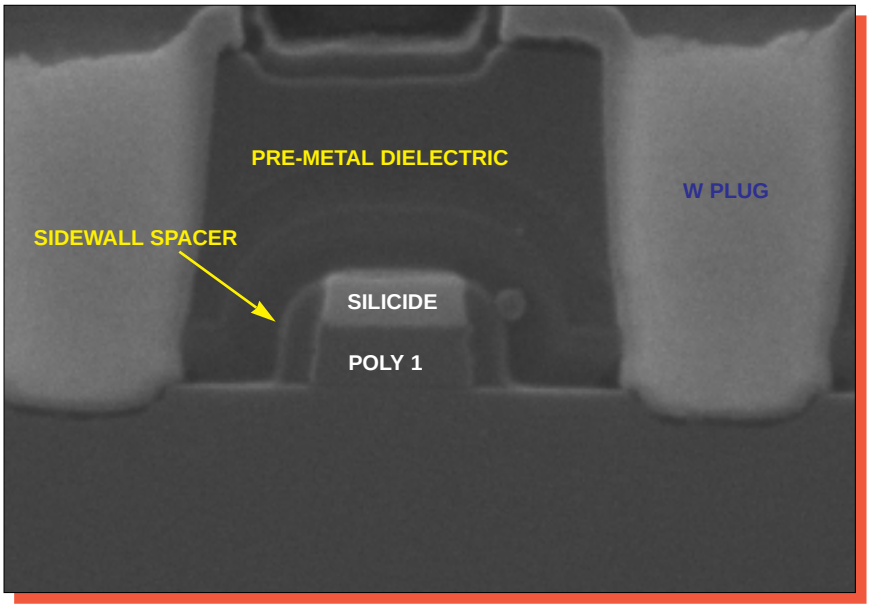


Mag. 26,000x

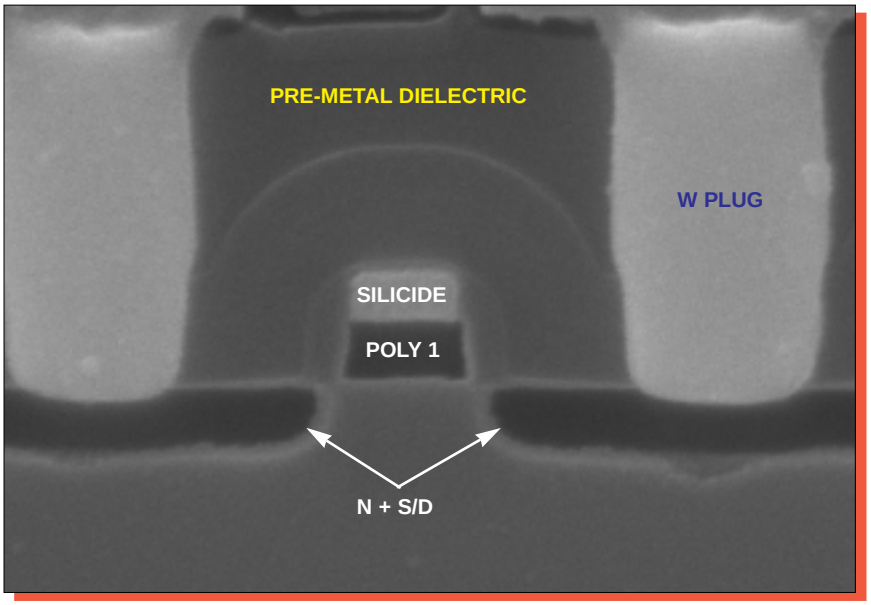


Mag. 26,000x

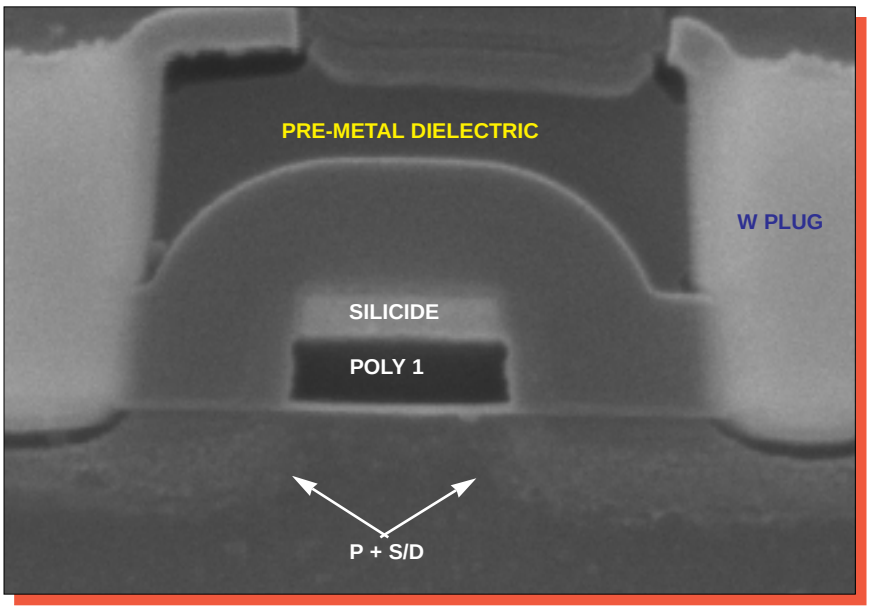
Figure 21. Perspective SEM views of poly 1 coverage. 60°.



glass etch



N-channel



P-channel

Figure 22. SEM section views of typical transistors. Mag. 52,000x.

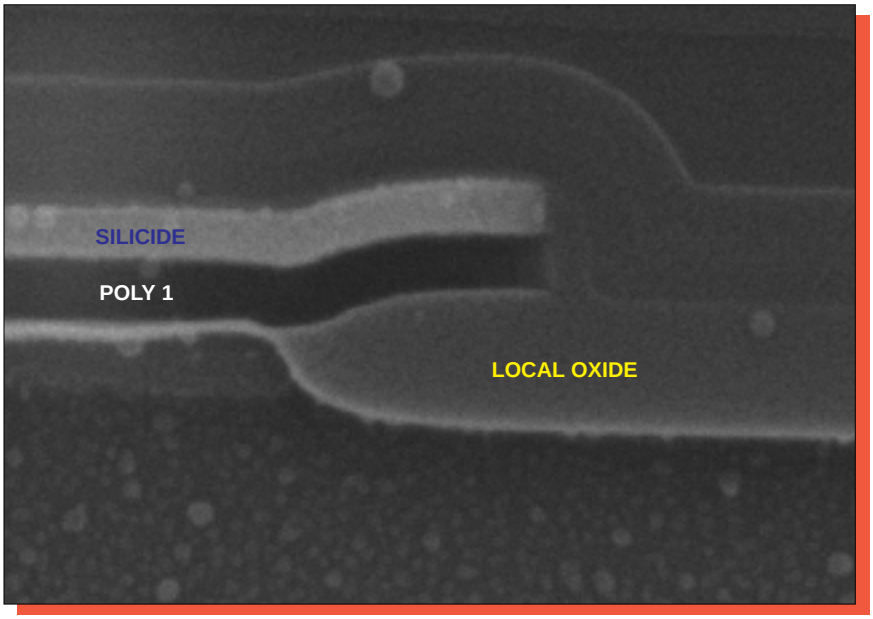


Figure 23. SEM section view of a typical local oxide birdsbeak. Mag. 52,000x.

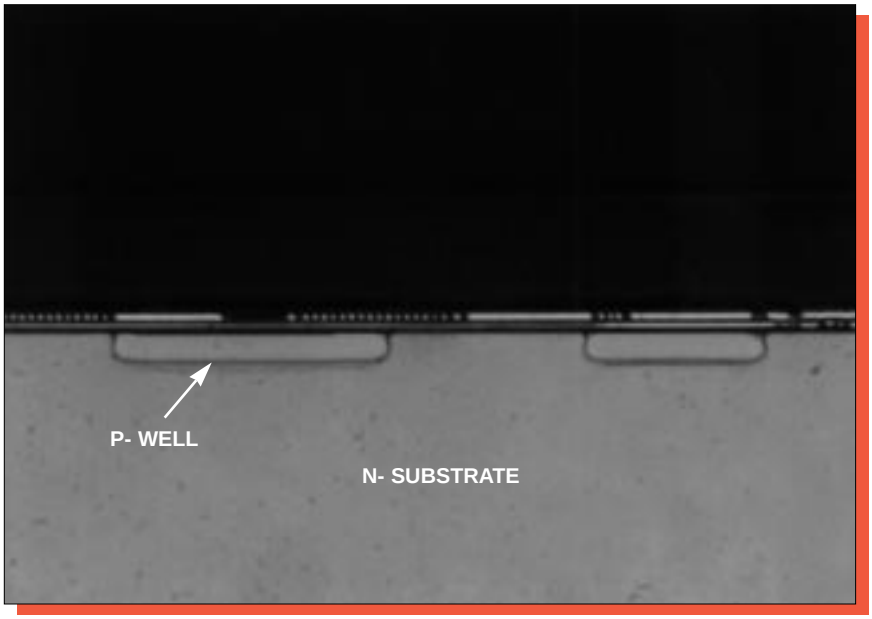
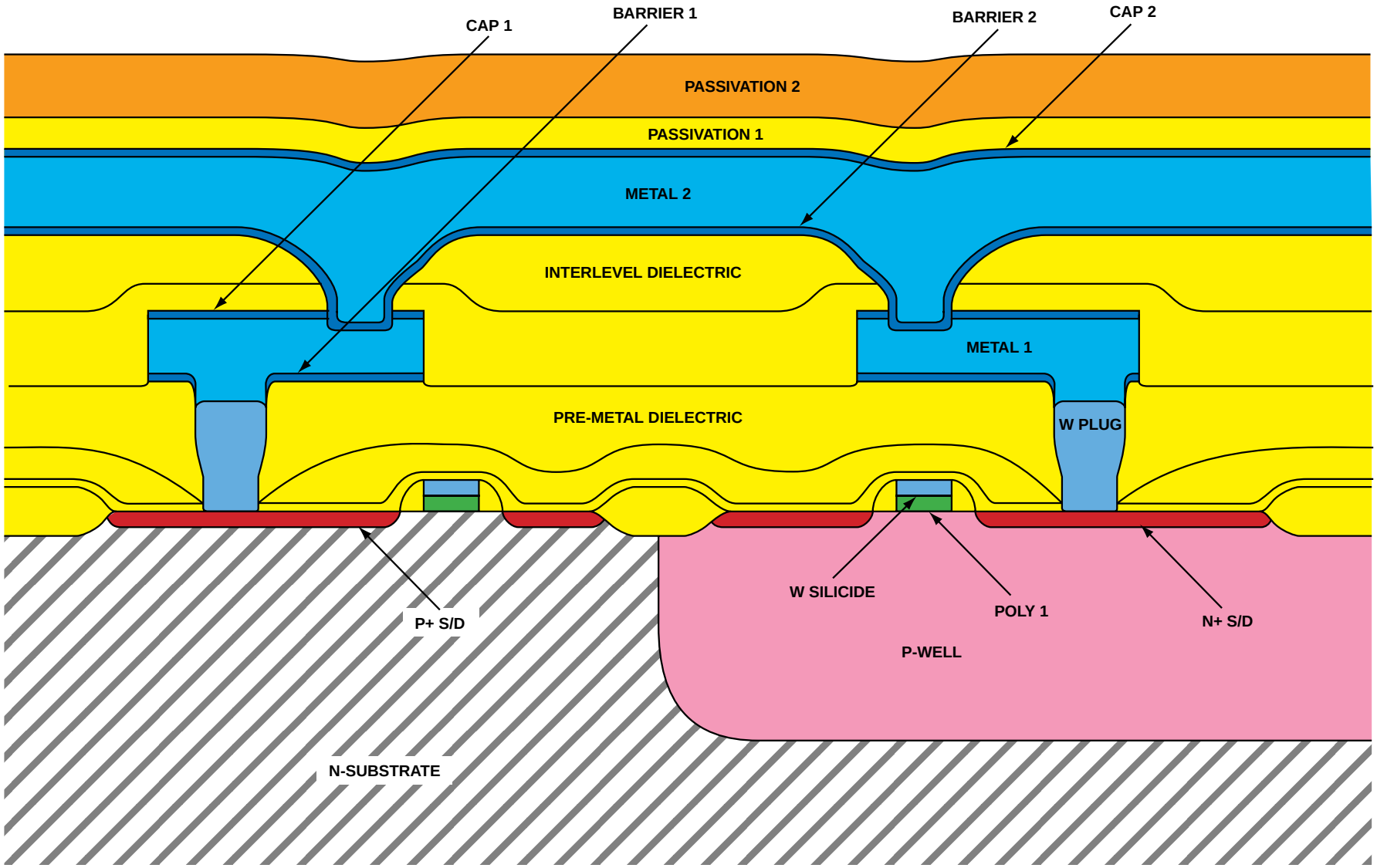


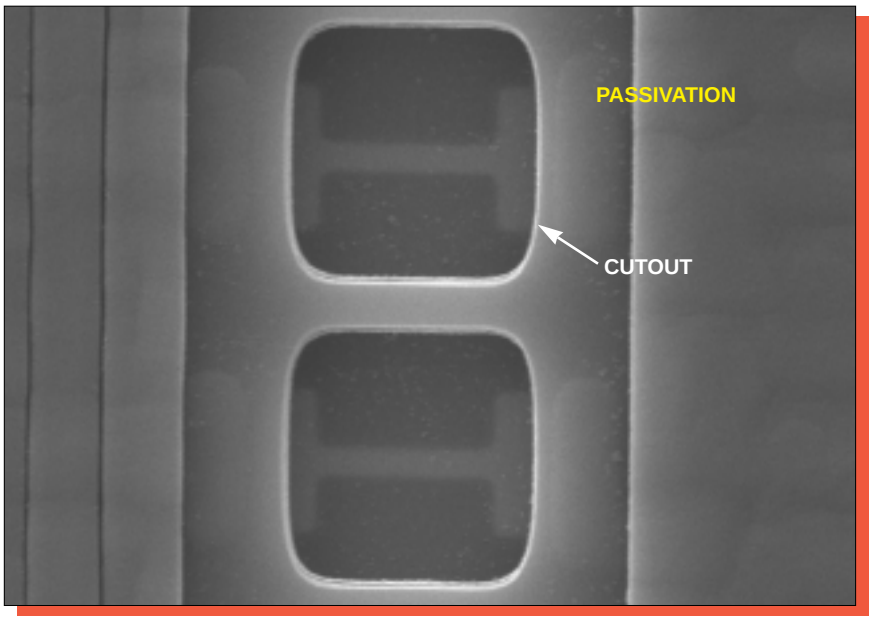
Figure 24. Optical section view of the well structure. Mag. 800x.



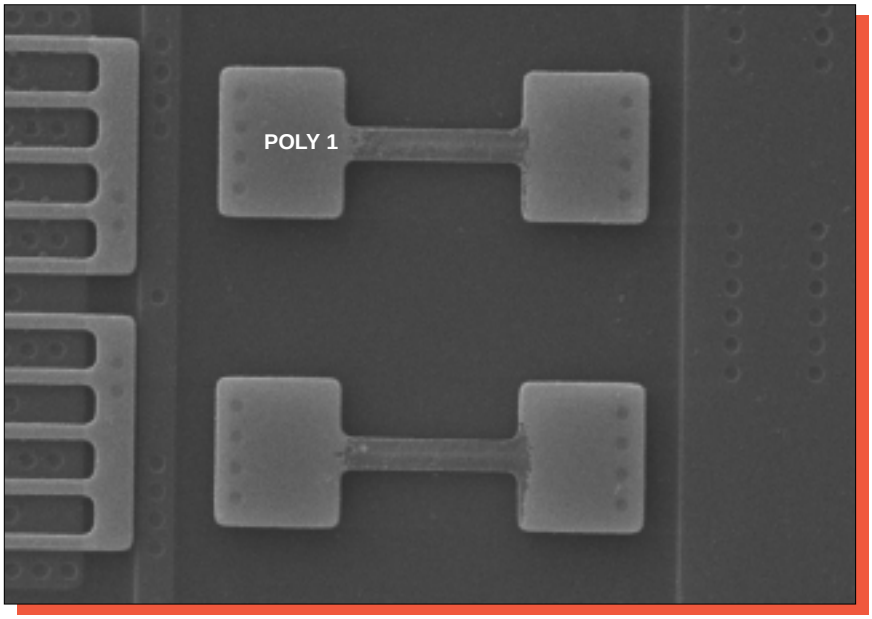
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 25. Color cross section drawing illustrating device structure.

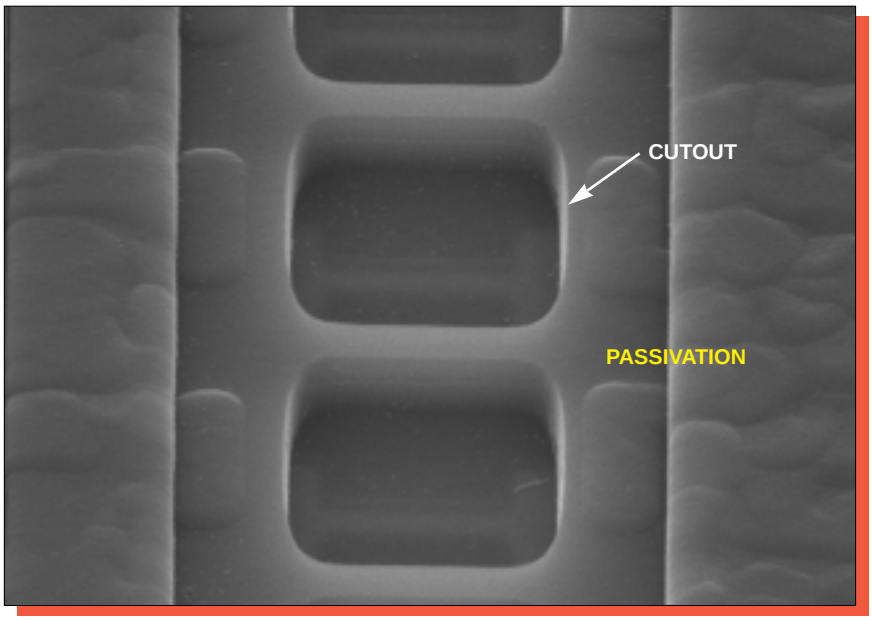


intact

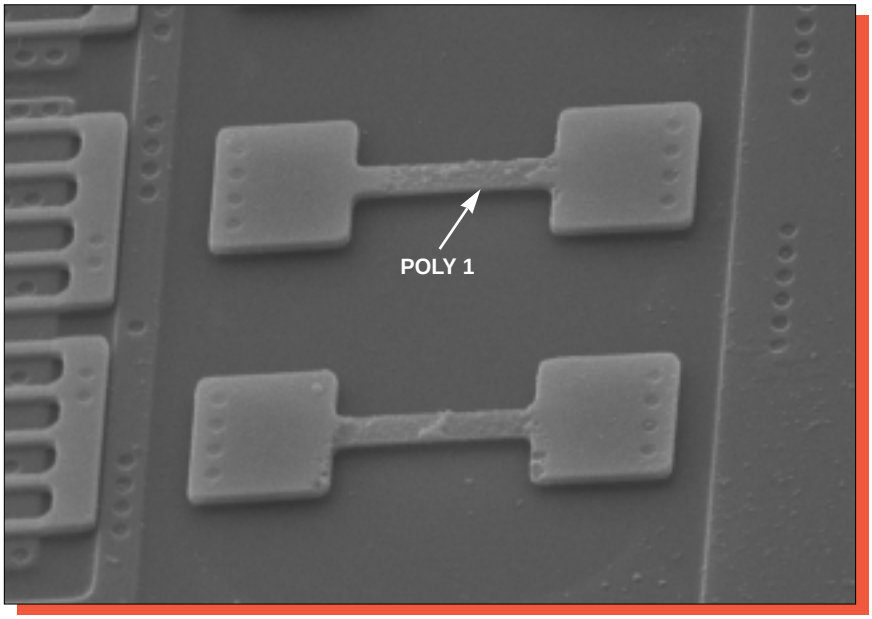


delayered

Figure 26. Topological SEM views of fuses. Mag. 4400x, 0°.



intact



delayered

Figure 27. Perspective SEM views of fuses. Mag. 5000x, 45°.

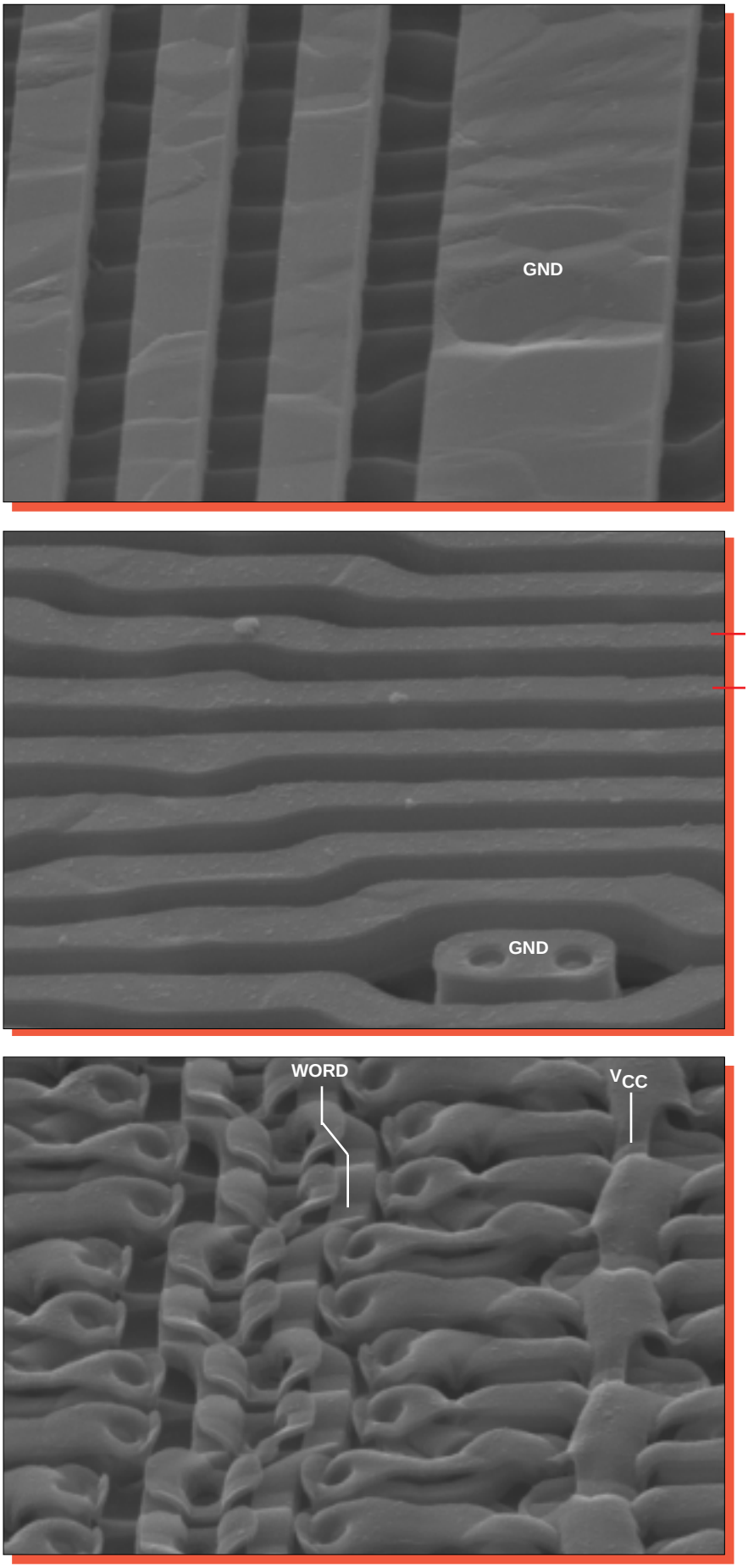
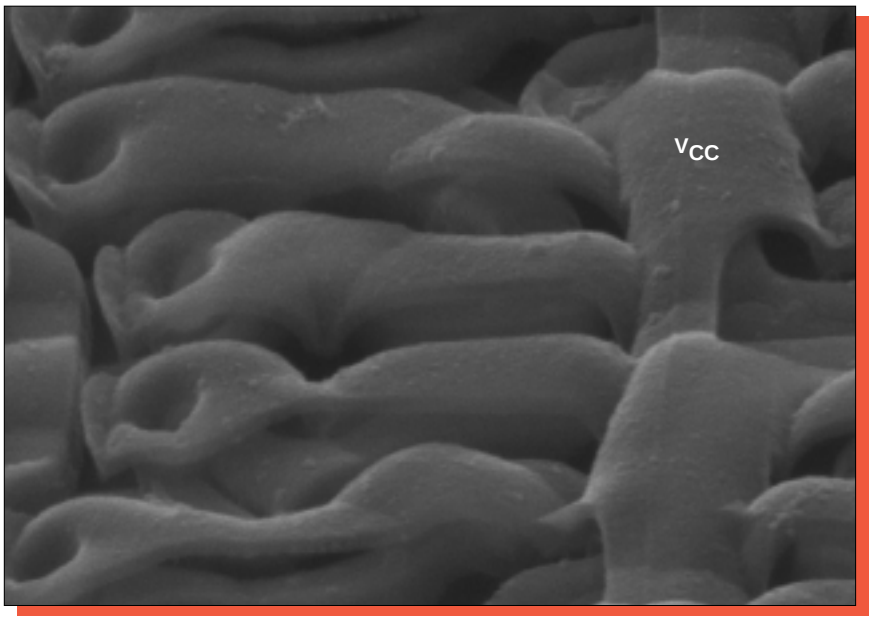
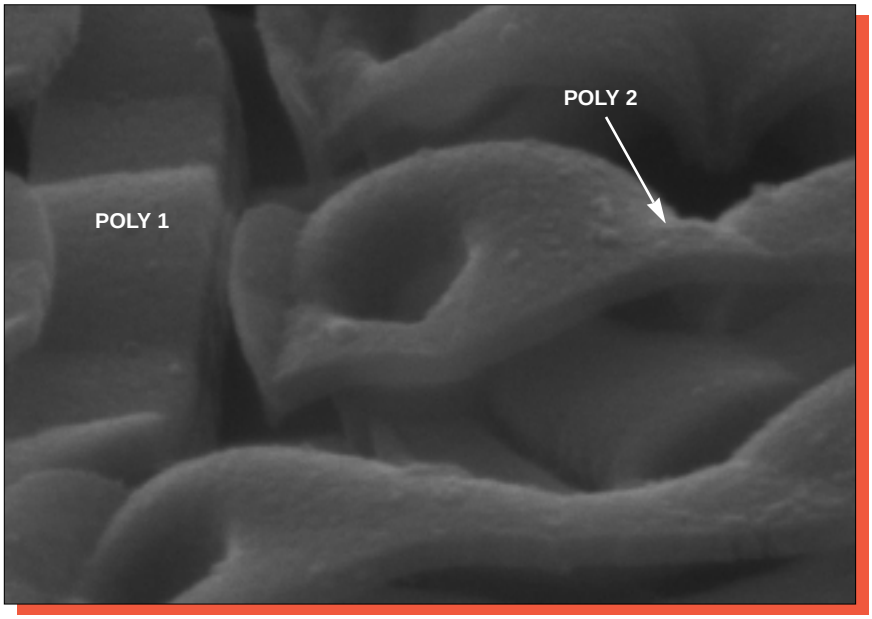


Figure 28. Perspective SEM views of a SRAM cell array. Mag. 13,000x, 60°.

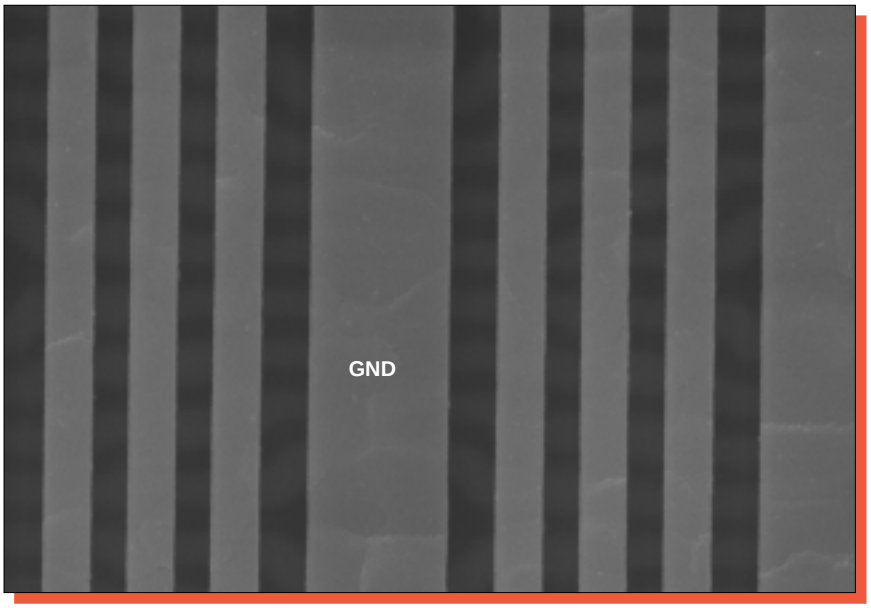


Mag. 26,000x

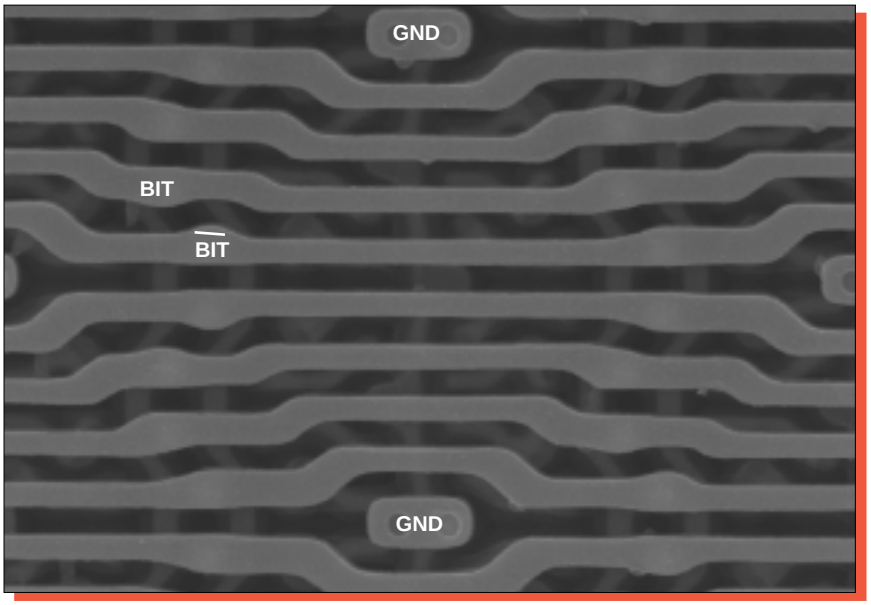


Mag. 52,000x

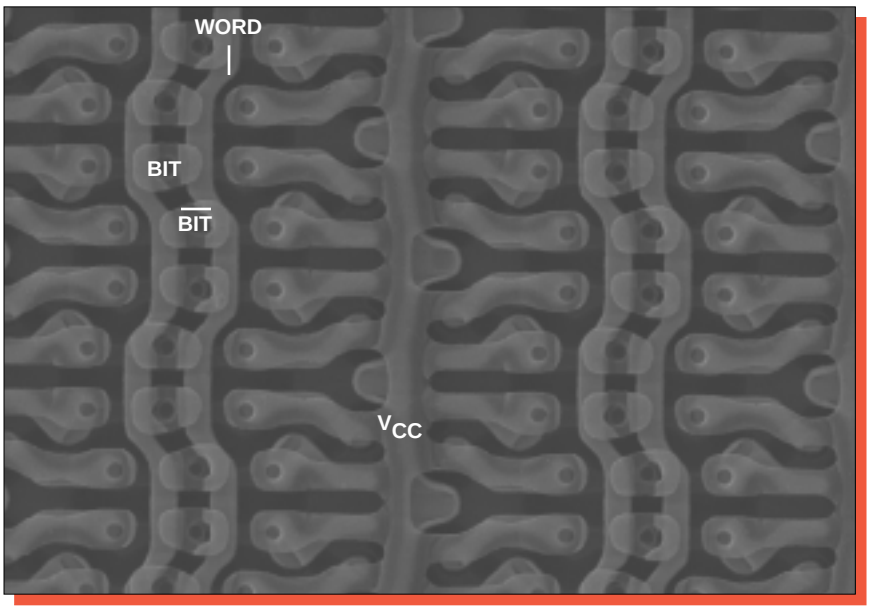
Figure 29. Detailed SEM views of the SRAM cell array. 60°.



metal 2

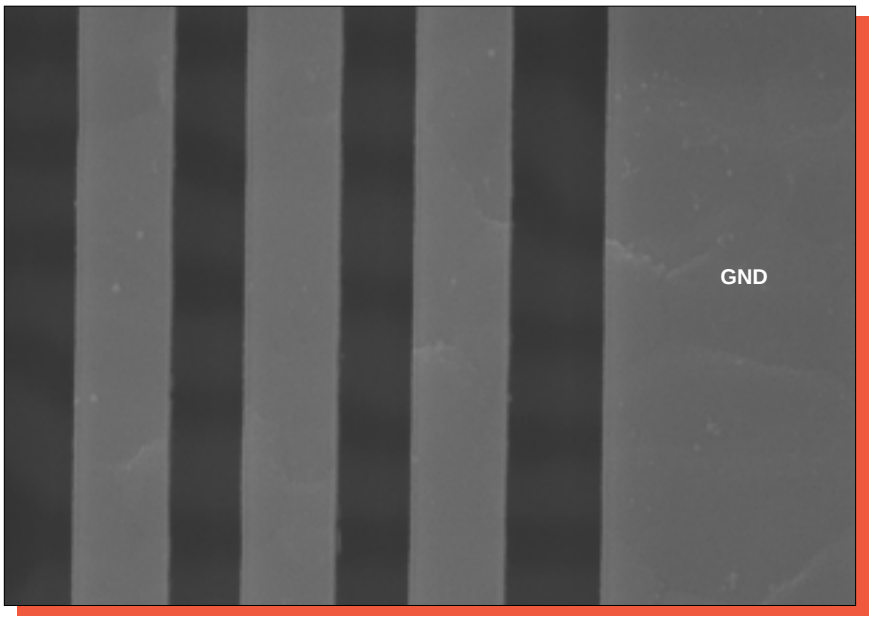


metal 1

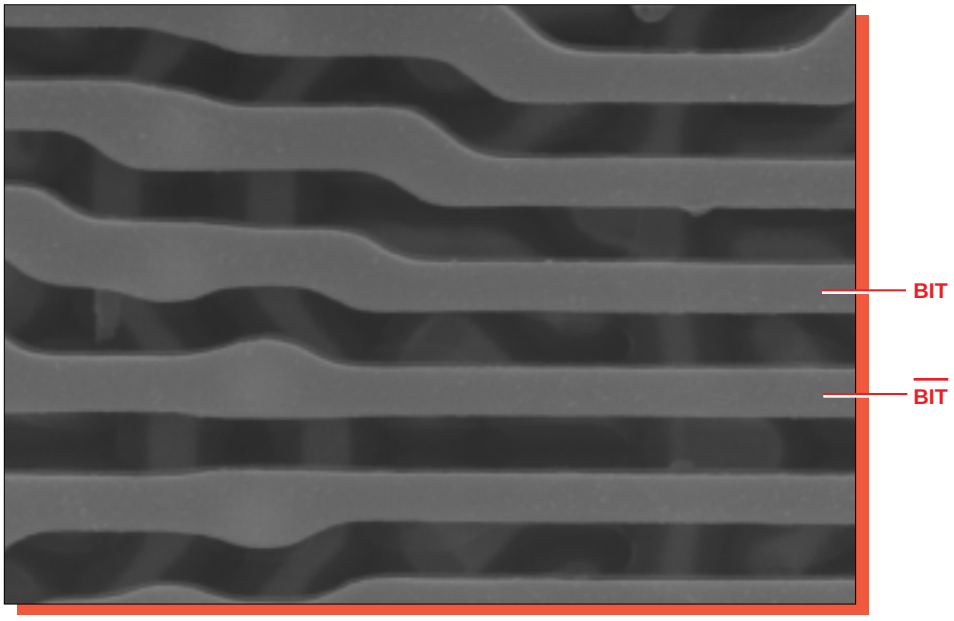


unlayered

Figure 30. Topological SEM views of the SRAM cell array. Mag. 6500x.

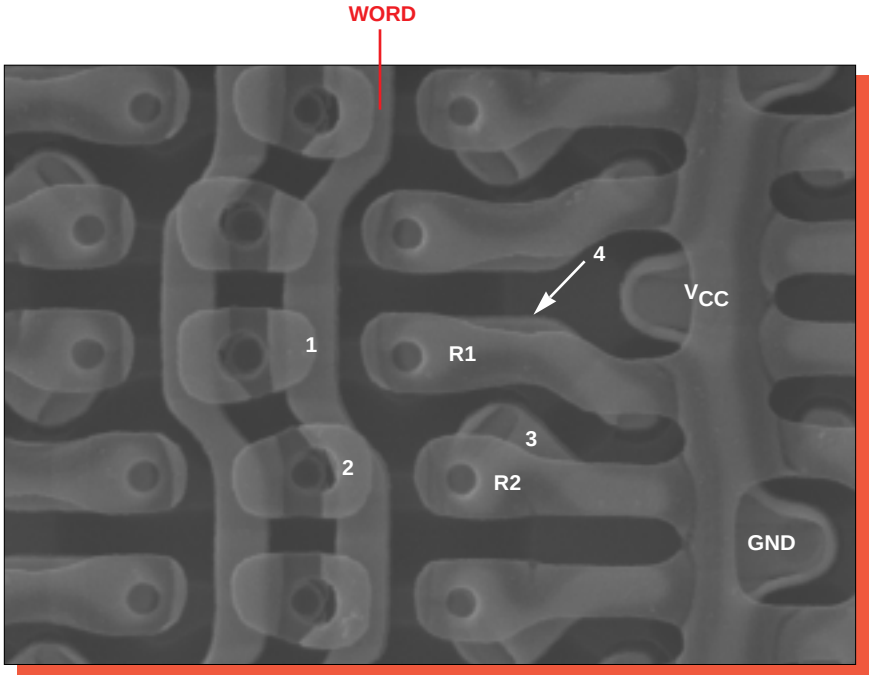


metal 2



metal 1

Figure 31. Topological SEM views of the SRAM cell array. Mag. 13,000x.



unlayered

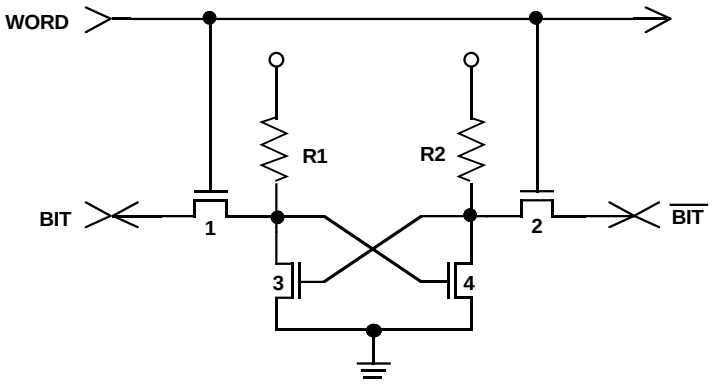
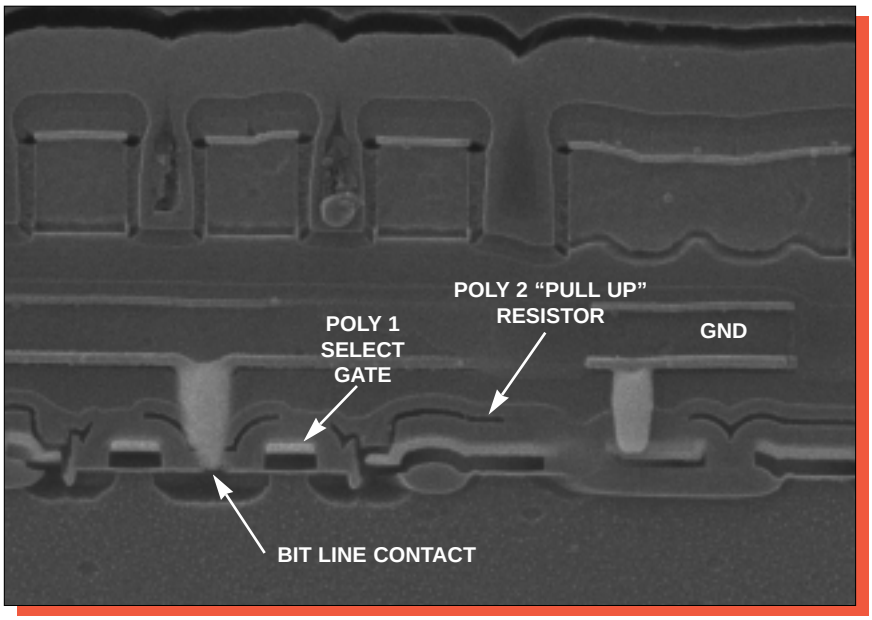
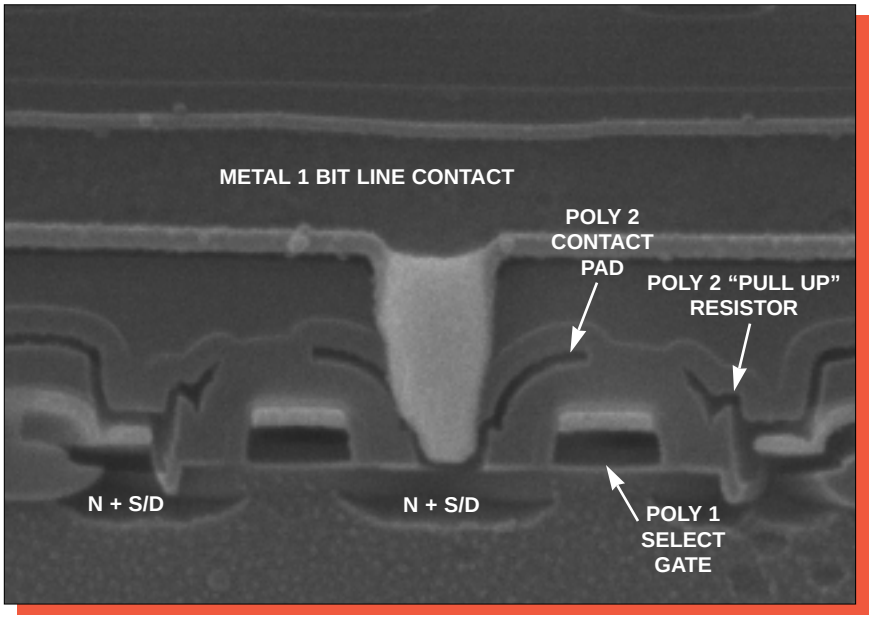


Figure 32. Topological SEM views and schematic of the SRAM cell array. Mag. 13,000x.

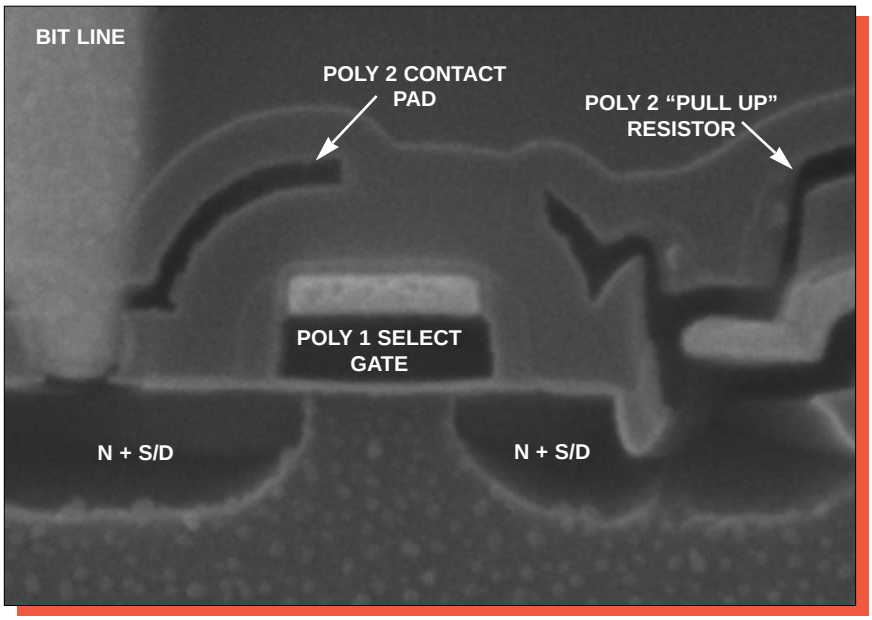


Mag. 13,000x



Mag. 26,000x

Figure 33. SEM section views of SRAM cell array.



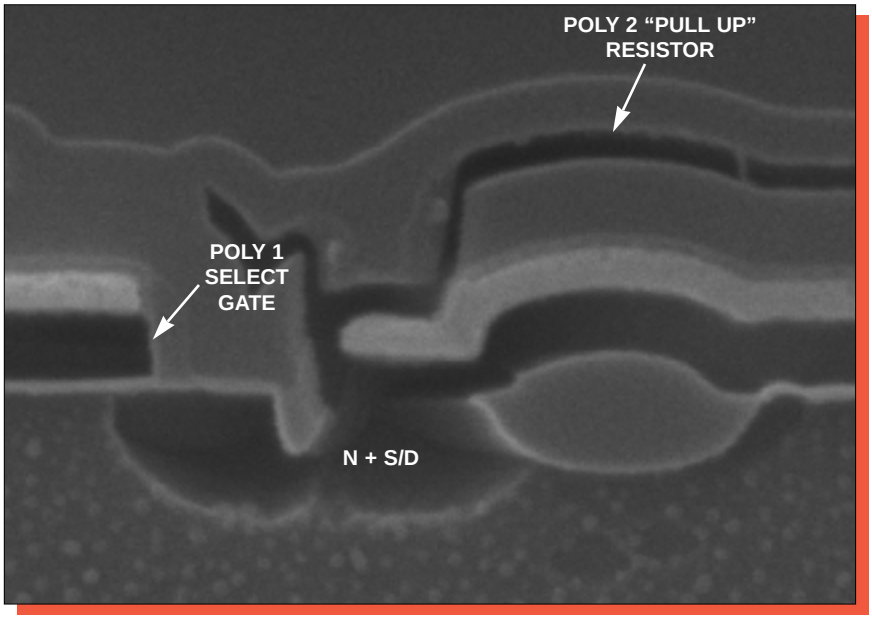
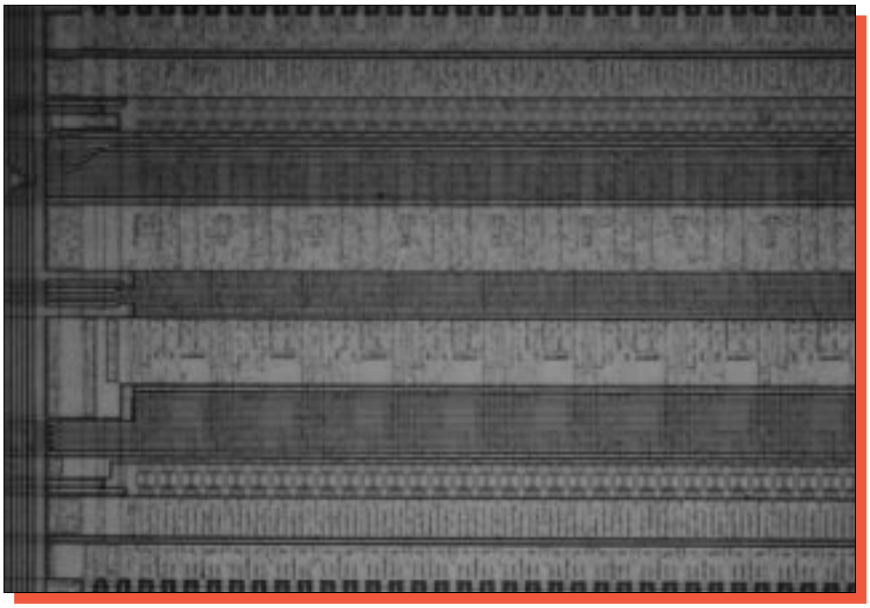
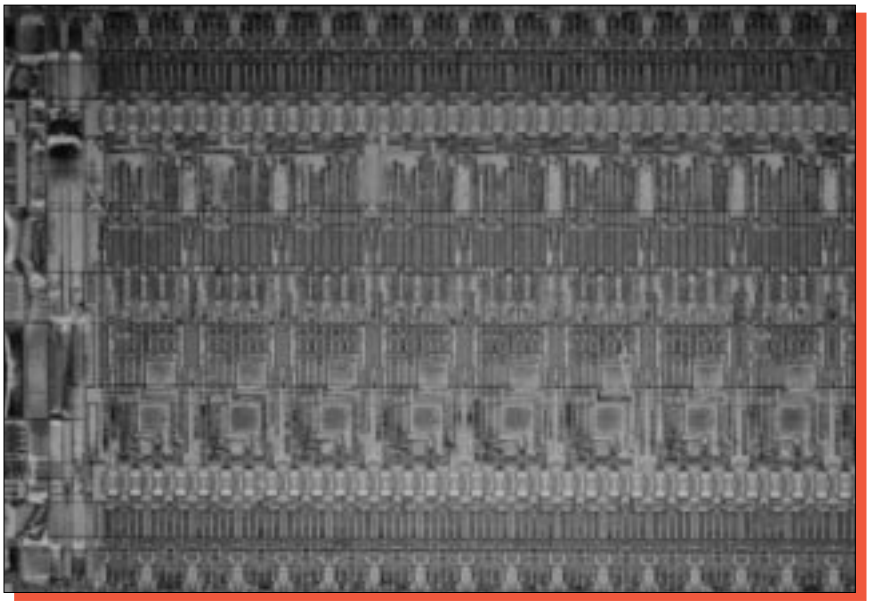


Figure 34. Detailed SEM views of SRAM cell array. Mag. 52,000x.



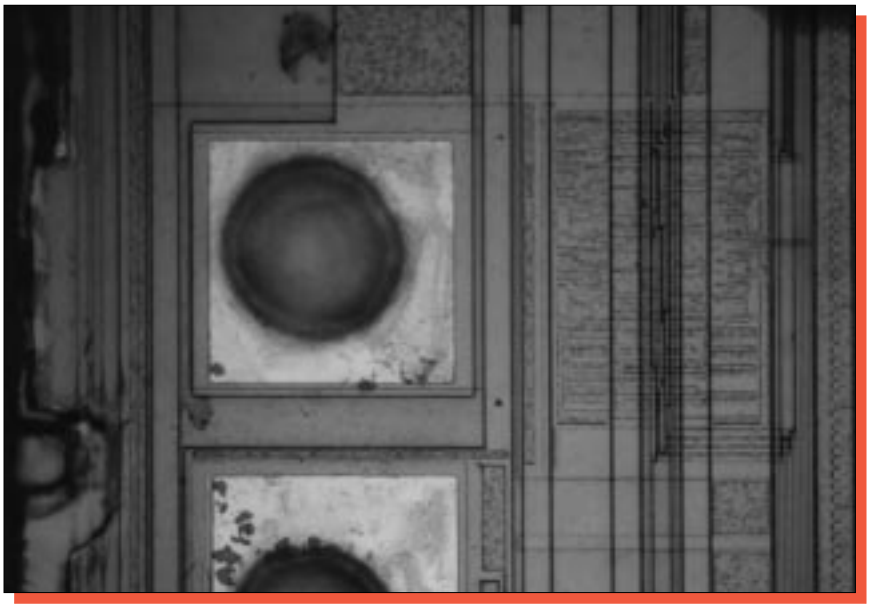
intact



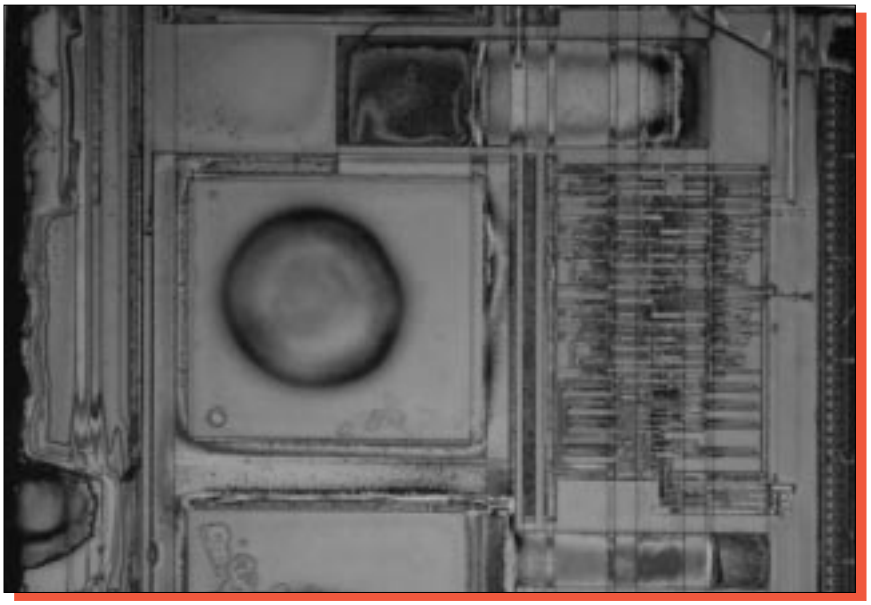
metal 1

unlayered

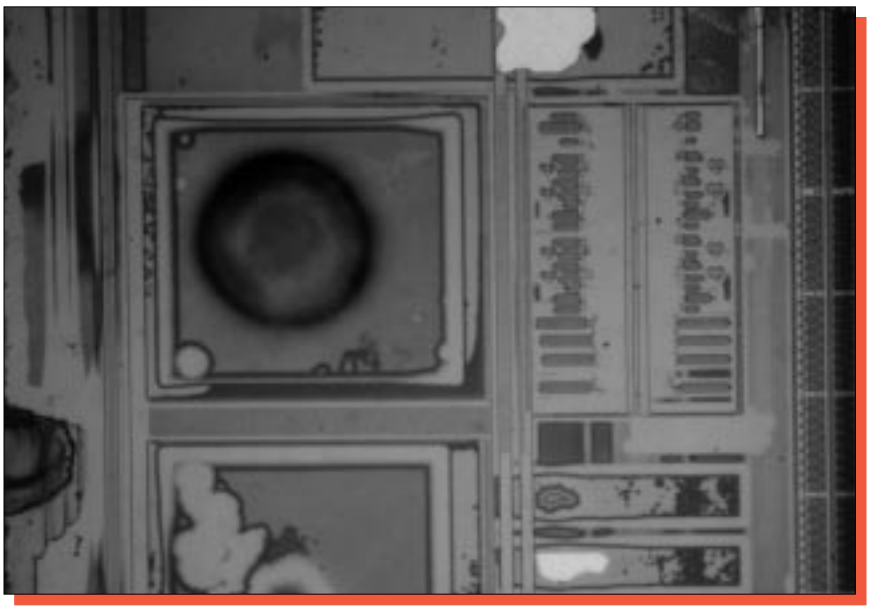
Figure 35. Optical views of general circuitry. Mag. 320x.



intact



metal 1



unlayered

Figure 36. Optical views of I/O structure. Mag. 320x.