Construction Analysis

Motorola XC56002PV80 Digital Signal Processor

Report Number: SCA 9608-509

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INTEGRATED CIRCUIT ENGINEERING

15022 N. 75th Street
Scottsdale, AZ 85260-2476
Phone: 602-998-9780
Fax: 602-948-1925
e-mail: ice@primenet.com
Internet: http://www.ice-corp.com/ice

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INTRODUCTION

This report describes a construction analysis of the Motorola XC56002PV80 Digital Signal Processor. Five devices packaged in 144-pin Square Quad Flat Packs (SQFPs) were received for the analysis. Devices were date coded 9552. An analysis of the assembly is also included.

MAJOR FINDINGS

Questionable Items:[1]

- Metal 2 aluminum thinning up to 90 percent[2] at metal 2-to-metal 1 vias (Figure 18).

- Metal 1 aluminum thinning up to 85 percent[2] at metal 1 contacts (Figure 23).

Special Features:

- Sub-micron gate lengths (0.6 micron N-channel and 0.7 micron P-channel).

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were packaged in 144-pin Square Quad Flat Packs (SQFPs) for surface mount applications (cavity down).

- The leadframe was constructed of copper and plated externally with tin-lead solder. Internal plating consisted of silver and was present on the internal portion of the leadframe and the sides of the header. The silver plating was not present on top of the header. A dimpled header was added for package strength.

- Die separation was by sawing (full depth). Silver-filled epoxy was used to attach the die to the header.

- Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire.

- Numerous pins were not connected. No multiple bonding was noted.

Die Process:

- Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

- No die coat was present.

- Passivation consisted of a layer of silicon-nitride over a layer of silicon-dioxide.

- Metallization consisted of two layers of metal. Metal 2 consisted of aluminum with titanium-nitride cap and no barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Standard contacts and vias were used at both levels (no plugs).

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectric (between metals) consisted of two layers of silicon-dioxide.

- Pre-metal dielectric consisted of borophosphosilicate glass (BPSG) over various densified oxides. The glass was reflowed prior to contact cuts only.

- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with nitride sidewall spacers left in place.

- Local oxide (LOCOS) isolation. A step was present in the oxide at the well boundary, which indicates a twin-well process was used.

- The memory cell array utilized a 6T SRAM cell design. Metal 2 was used to form the bit lines and distribute GND (via Metal 1). Metal 1 was used to form "piggyback" word lines, provide cell interconnect and distribute Vcc. Poly was used to form word lines and all gates.

- Redundancy fuses were not present.

ANALYSIS RESULTS I

Package and Assembly: **Figures 1 - 9**

Questionable Items:[1] None.

General Items:

- Devices were packaged in 144-pin Square Quad Flat Packs (SQFPs) for surface mount applications (cavity down).

- Overall package quality: Good. No significant defects were noted on the external or internal portions of the package. The package was subjected to a dye penetrant test. No dye penetrant was noted at leadframe exits, header or die.

- Leadframe: The leadframe was constructed of copper (Cu) and plated externally with tin-lead (SnPb) solder. Internal plating consisted of silver and was present on the internal portion of the leadframe and the sides of the header. The silver plating was not present on top of the header. No problems were noted. A dimpled header was added for package strength. No gaps were noted at lead exits.

- Die dicing: Die separation was by sawing (full depth) of normal quality. No large cracks or chips were present.

- Die attach: A silver-filled epoxy was used to attach the die to the header. No voids were noted.

- Wirebonding: Wirebonding was by the thermosonic ball bond method using 1.0 mil O.D. gold wire. Some incomplete intermetallic formation was noted; however, bond pull strengths were normal (see page 10) and no bond lifts occurred. Ball bonds were overcompressed slightly; however, no problems are foreseen.

- Numerous pins were not connected. No multiple bonding was noted.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II

Die Process: **Figures 10 - 34**

Questionable Items:[1]

- Metal 2 aluminum thinning up to 90 percent[2] at metal 2-to-metal 1 vias (Figure 18).

- Metal 1 aluminum thinning up to 85 percent[2] at metal 1 contacts (Figure 23).

Special Features:

- Sub-micron gate lengths (0.6 micron N-channel and 0.7 micron P-channel).

General Items:

- Fabrication process: Devices were fabricated using a selective oxidation, twin-well CMOS process in a P substrate. No epi was used.

- Process implementation: Die layout was clean and efficient. Alignment was good at all levels. No damage or contamination was found. Slots and beveled corners were present in Metal 1 and Metal 2 bus lines.

- Die coat: No die coat was present.

- Overlay passivation: Consisted of a layer of nitride over a layer of silicon-dioxide. Overlay integrity test indicated defect-free passivation. Edge seal was good as the passivation extended into the scribe lane.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metallization: Two layers of metal. Metal 2 consisted of aluminum with a titanium-nitride cap and no barrier. Metal 1 consisted of aluminum with a titanium-nitride cap and barrier. Standard contacts and vias were used at both levels (no plugs were used).

- Metal patterning: Both metal layers were patterned by a dry etch of normal quality. Both metal were widened around vias and contacts.

- Metal defects: No voiding, notching, or neckdown was noted in either of the metal layers. All contacts and vias were completely surrounded by metal. No silicon nodules were noted following the removal of either metal layer.

- Metal step coverage: Metal 2 aluminum thinned up to 90 percent at via edges. Total Metal 2 thinning was reduced to 85 percent with the addition of the cap metal. Metal 1 aluminum thinned up to 85 percent at contact edges. Total Metal 1 thinning was reduced to 75 percent with the addition of the cap and barrier metals.

- Interlevel dielectric: Interlevel dielectric consisted of two layers of silicon-dioxide. The first layer (Glass 1) had been backetched to aid in planarization. No problems were found in any of these layers (the apparent voids shown in the photos are delineation artifacts).

- Pre-metal dielectric: Borophosphosilicate glass (BPSG) over various densified oxides was used under Metal 1. Reflow was performed prior to contact cuts only. No problems were found.

- Contact defects: Via and contact cuts appeared to be defined by a two step process. No over-etching of the contacts or vias was noted.

<u>ANALYSIS RESULTS II</u> (continued)

- A single layer of poly (no silicide) was used to form all gates on the die. Direct poly-to-diffusion (buried) contacts were not used. Definition was by dry-etch of normal quality.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. An LDD process was used with nitride sidewall spacers left in place. No problems were found.

- Local oxide (LOCOS) isolation was used. The step present at the well boundary indicates a twin-well process was employed.

- The memory cell array utilized a 6T SRAM cell. Metal 2 was used to form the bit lines and distribute GND (via Metal 1). Metal 1 was used to form “piggyback” word lines, provide cell interconnect, and distribute Vcc. Poly was used to form word lines and all gates. Cell pitch was 9.5 x 13 microns.

- Redundancy fuses were not present on the die.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Package section and EDX

Decapsulate

Internal optical inspection

SEM of passivation and assembly features

Passivation integrity test

Wirepull test

Passivation removal

Delayer to metal 2 and inspect

Metal 2 removal and inspect barrier

Delayer to metal 1 and inspect

Metal 1 removal and inspect barrier

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

******Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal/Poor

DETAIL OF EVALUATION

Package integrity	N
Package markings	N
Die placement	N
Wirebond placement	N
Wire spacing	N
Wirebond quality	N
Die attach quality	N
Dicing quality	N
Die attach method	Silver-epoxy
Dicing method	Sawn (full depth)
Wirebond method	Thermosonic ball bonds using 1.0 mil gold wire.

Die surface integrity:

Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity	P[1]
Metal registration	N
Contact coverage	N
Contact registration	N

[1]*Metal 2 aluminum thinning up to 90 percent, Metal 1 aluminum thinning up to 85 percent.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS (TOP)

XC56002PV80
1F87L
HEA09552

(BOTTOM)

HONG KONG

WIREBOND STRENGTH

Wire material: 1.0 mil O.D. gold

Die pad material: aluminum

Sample #	**1**	**2**
# of wires pulled:	31	31
Bond lifts:	0	0
Force to break - high:	9g	10g
- low:	5g	4g
- avg.:	6.8g	5.7g
- std. dev.:	1.1	1.3

PACKAGE MATERIAL ANALYSIS (EDX)

Leadframe:	Copper (Cu)
Internal plating:	Silver (Ag)
External plating:	Tin-lead (SnPb) solder
Die attach:	Silver (Ag) epoxy

DIE MATERIAL ANALYSIS

Overlay passivation:	A layer of silicon-nitride over a layer of silicon-dioxide.
Metallization 2:	Aluminum (Al) with a titanium-nitride (TiN) cap with no barrier.
Interlevel dielectric:	Two layers of silicon.
Metallization 1:	Aluminum (Al) with a titanium-nitride (TiN) cap and barrier.
Pre-metal dielectric:	BPSG containing 6.7 wt. % phosphorus and 2.6 wt. % boron.

HORIZONTAL DIMENSIONS

Die size:	6.5 x 6.5 mm (254 x 254 mils)
Die area:	42.3 mm^2 (64,515 $mils^2$)
Min pad size:	0.12 x 0.15 mm (4.7 x 5.9 mils)
Min pad window:	0.11 x 0.11 mm (4.2 x 4.2 mils)
Min pad space:	45 microns
Min metal 2 width:	1.1 micron
Min metal 2 space:	0.9 micron
Min metal 2 pitch:	2.0 microns
Min metal 1 width:	0.7 micron
Min metal 1 space:	0.7 micron
Min metal 1 pitch:	1.4 micron
Min via (M2 - M1):	1.1 micron (diameter)
Min contact:	0.9 micron
Min poly width:	0.6 micron
Min poly space:	0.6 micron
Min gate length - (N-channel):*	0.6 micron
- (P-channel):	0.7 micron
Cell pitch:	9.5 x 13 microns
Cell size:	124 microns

*****_Physical gate length_

VERTICAL DIMENSIONS

Die thickness:	0.35 mm (13.8 mils)

Layers:

Passivation 2:	0.6 micron
Passivation 1:	0.4 micron
Metal 2 - cap:	0.06 micron (approximate)
- aluminum:	1.0 micron
Interlevel dielectric - glass 2:	0.25 micron
- glass 1:	0.25 - 0.65 micron
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.7 micron
- barrier:	0.1 micron
Pre-metal dielectric:	0.2 - 0.55 micron
Oxide on poly:	0.15 micron
Poly:	0.25 micron
Local oxide:	0.5 micron
N+ S/D:	0.3 micron
P + S/D:	0.4 micron
N-well:	5.5 microns (approximate)
P-well:	Could not delineate

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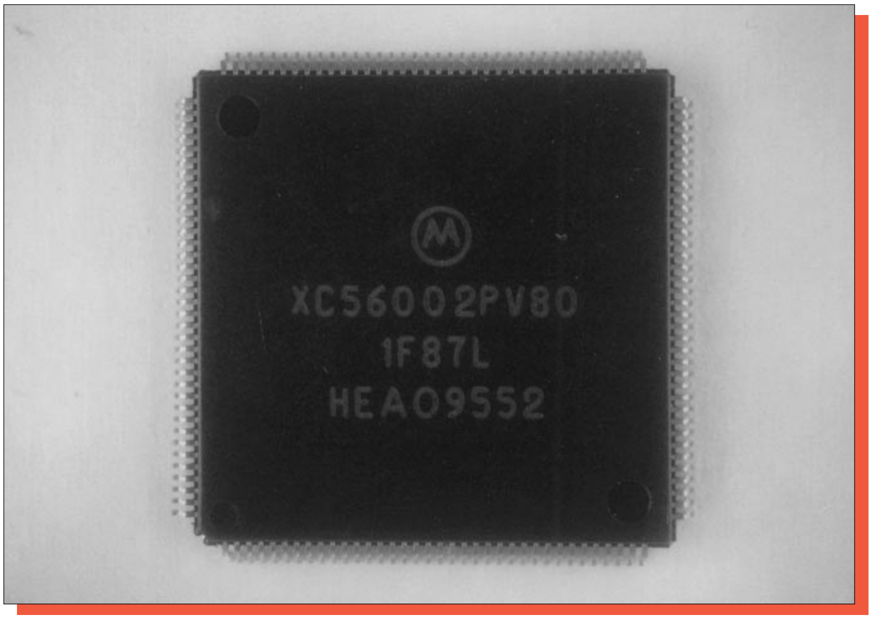
GENERAL CIRCUITRY	Figure 33
I/O STRUCTURE	Figure 34



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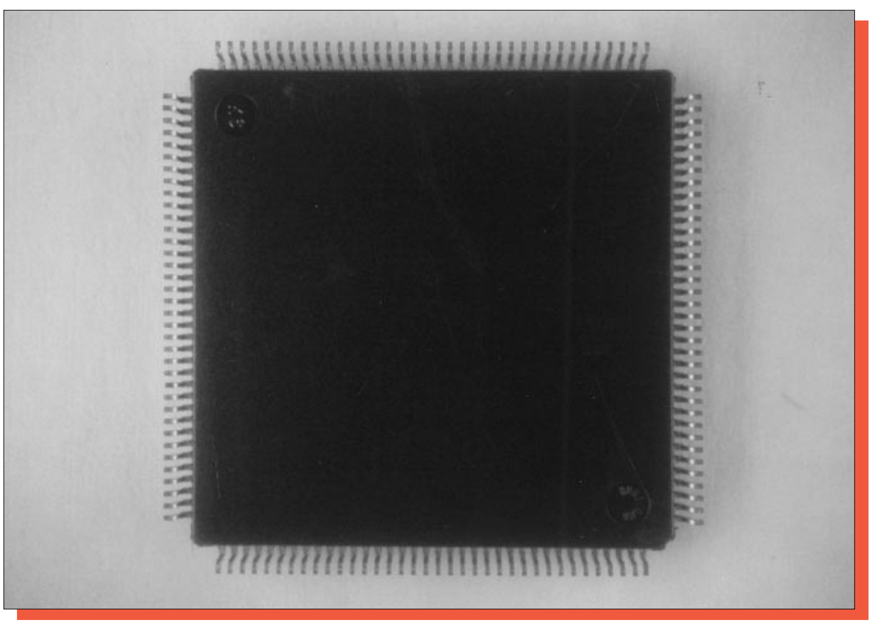

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Figure 1. Package photographs of the Motorola XC56002PV80. Mag. 3.2x

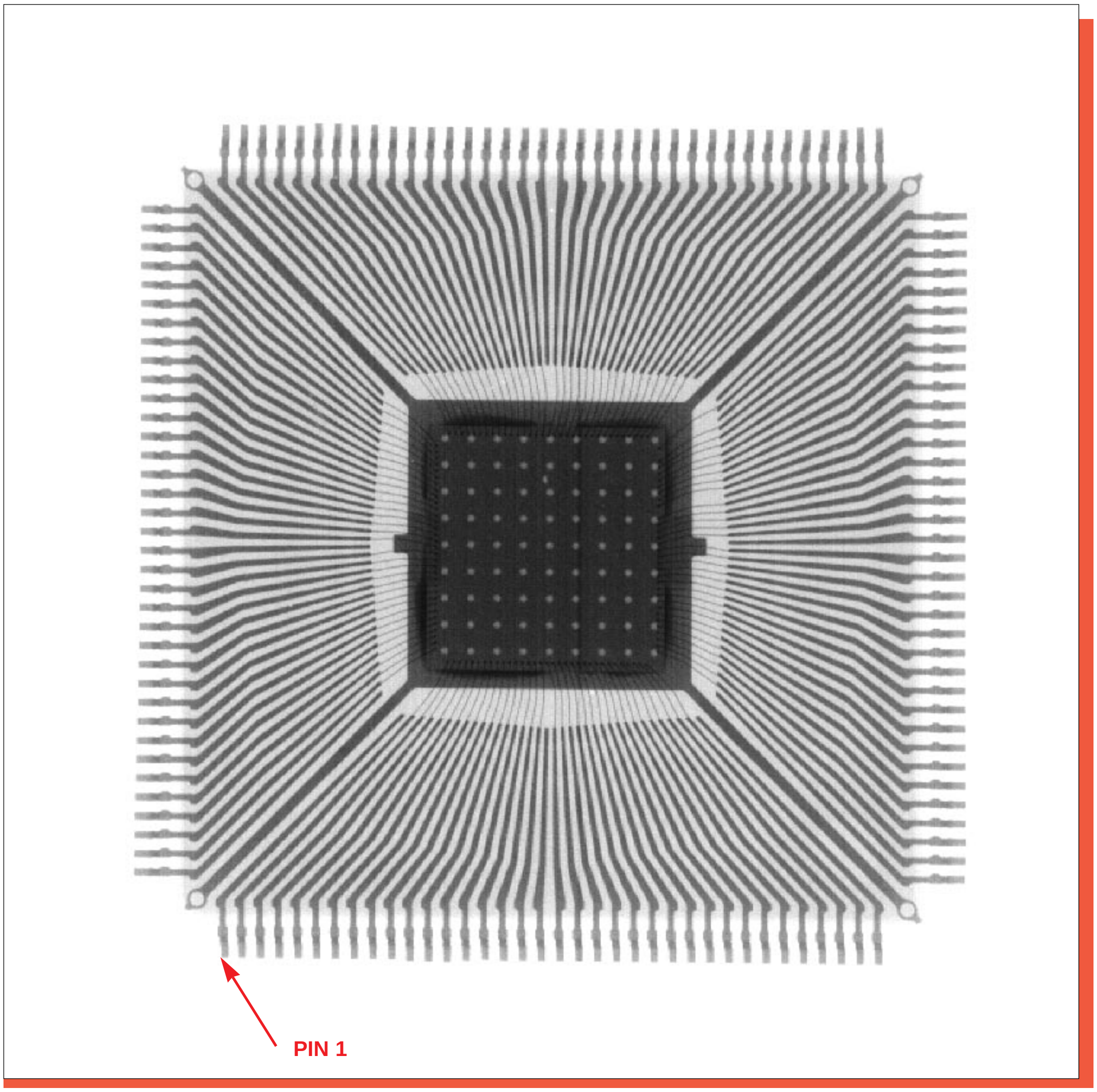


Figure 2. X-ray view of the package. Mag. 5x.

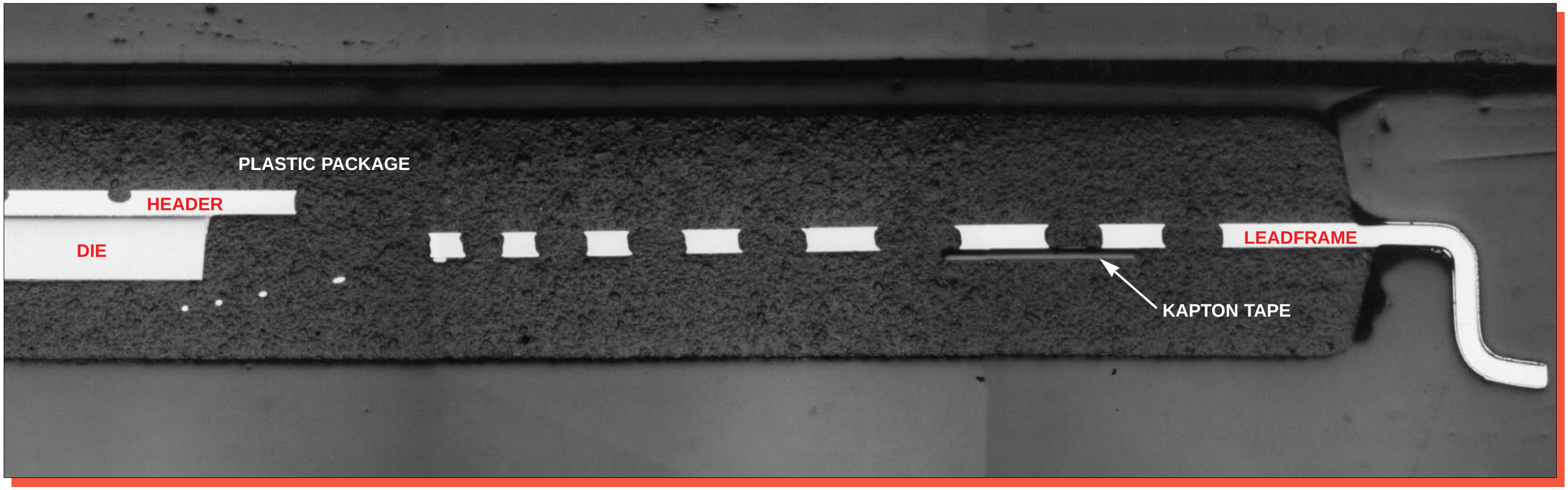
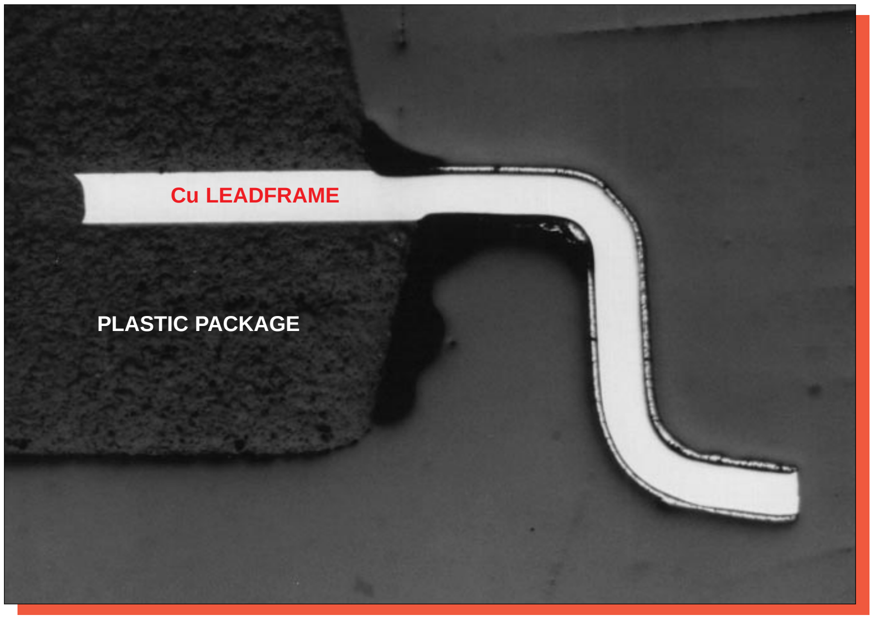
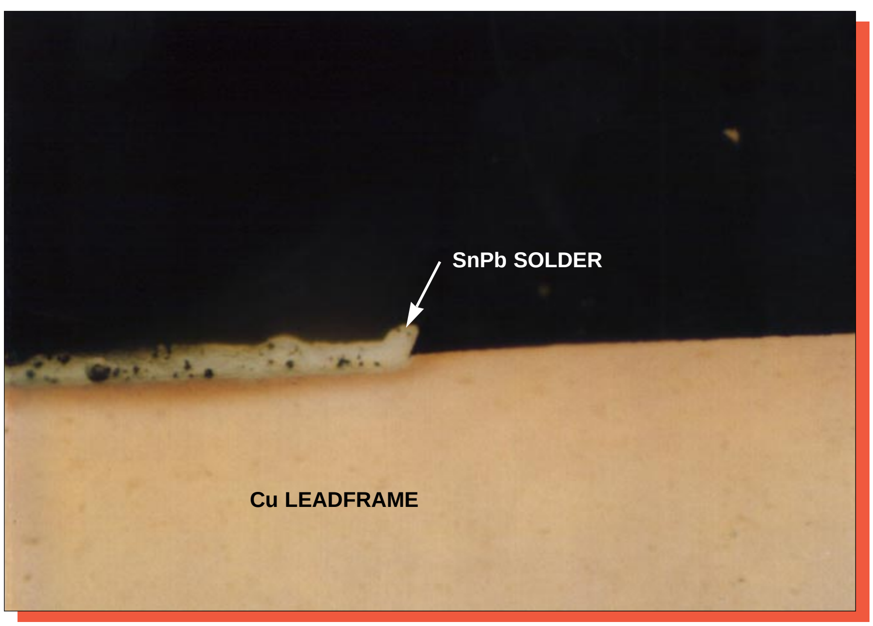


Figure 3. Optical package section view of general construction. Mag. 26x.

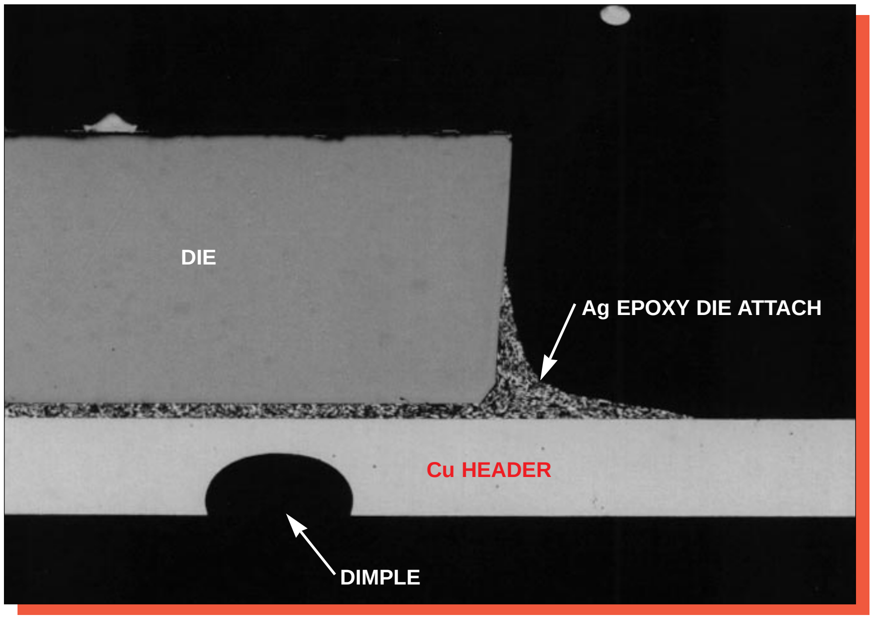


Mag. 50x

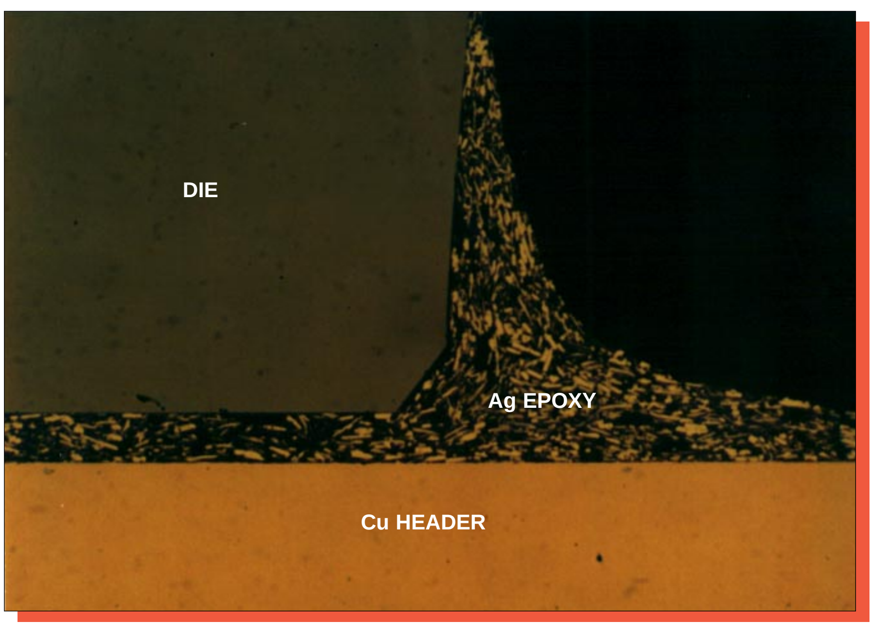


Mag. 500x

Figure 4. Section views illustrating lead forming and lead exit.

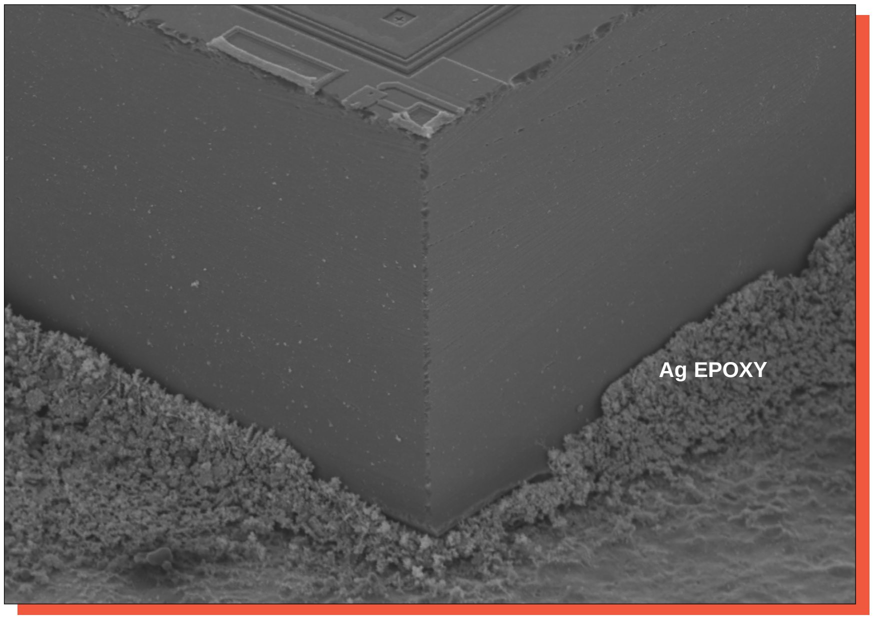


Mag. 100x

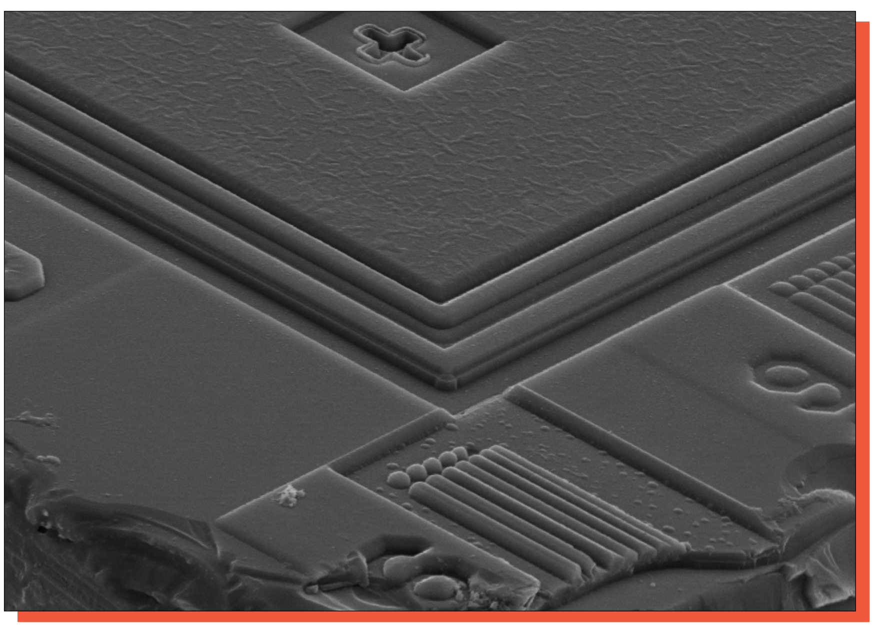


Mag. 320x

Figure 5. Section views illustrating dicing and die attach.

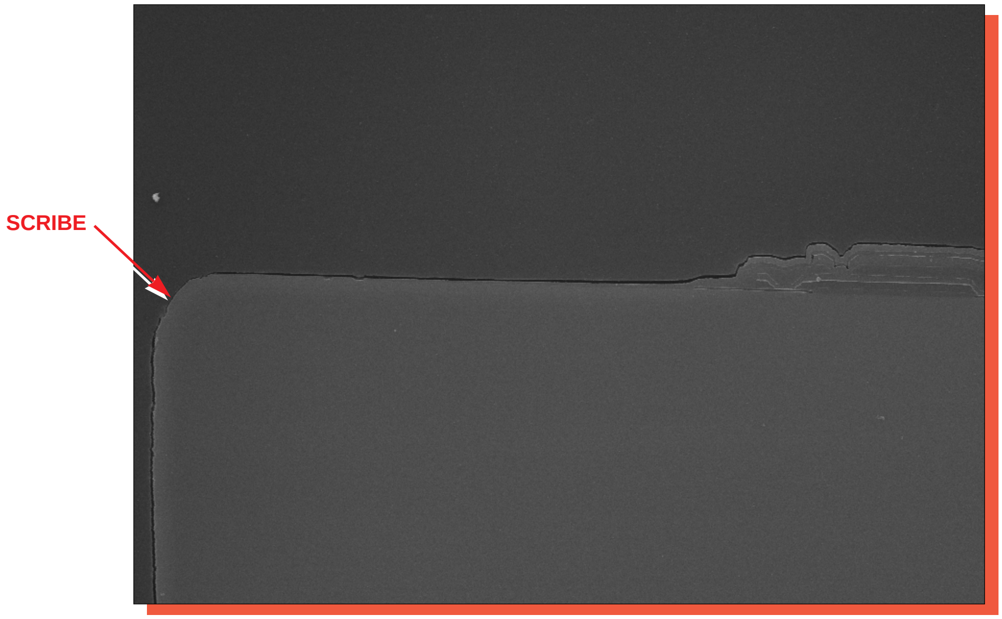


Mag. 180x

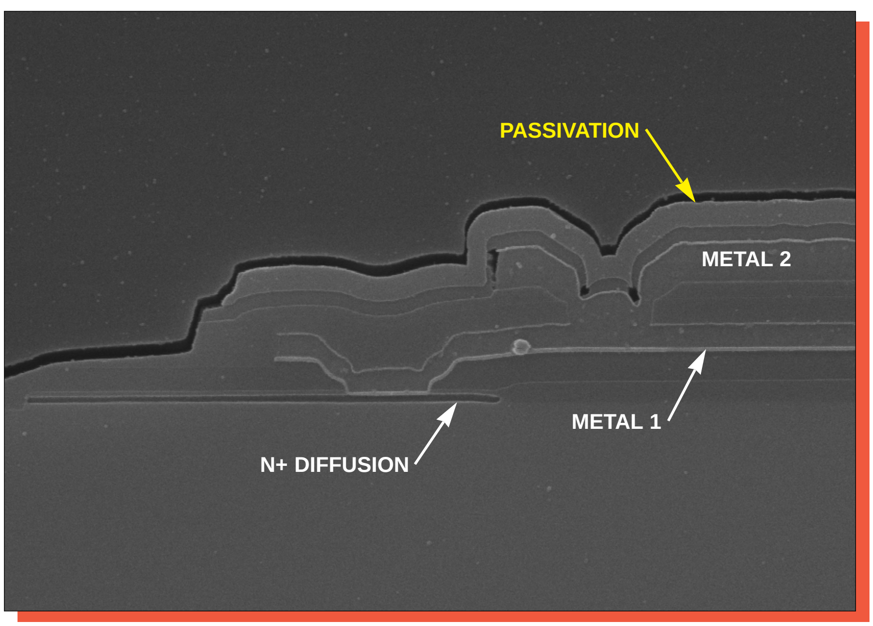


Mag. 1200x

Figure 6. Perspective SEM views of dicing and edge seal. 60°.

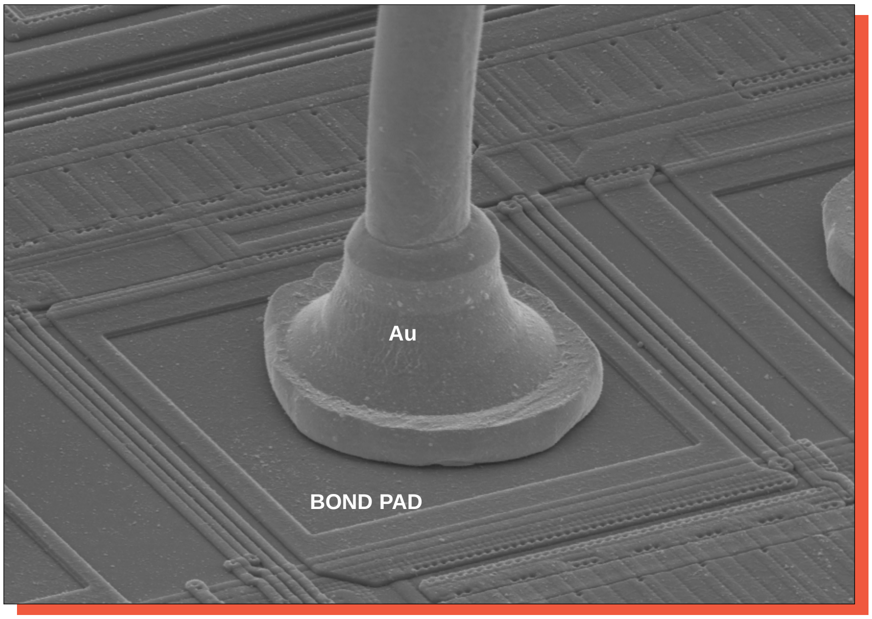


Mag. 1300x

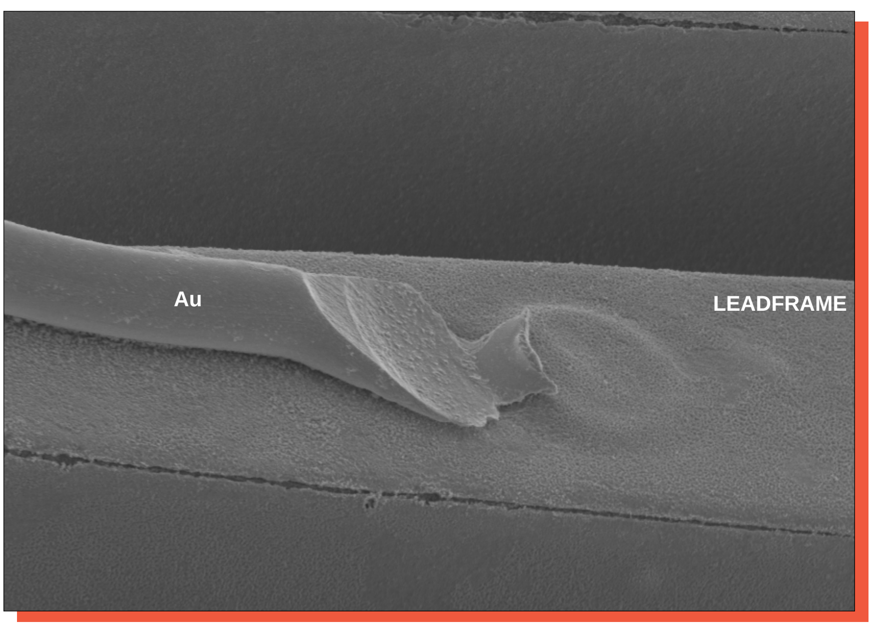


Mag. 5000x

Figure 7. SEM section views of edge seal.

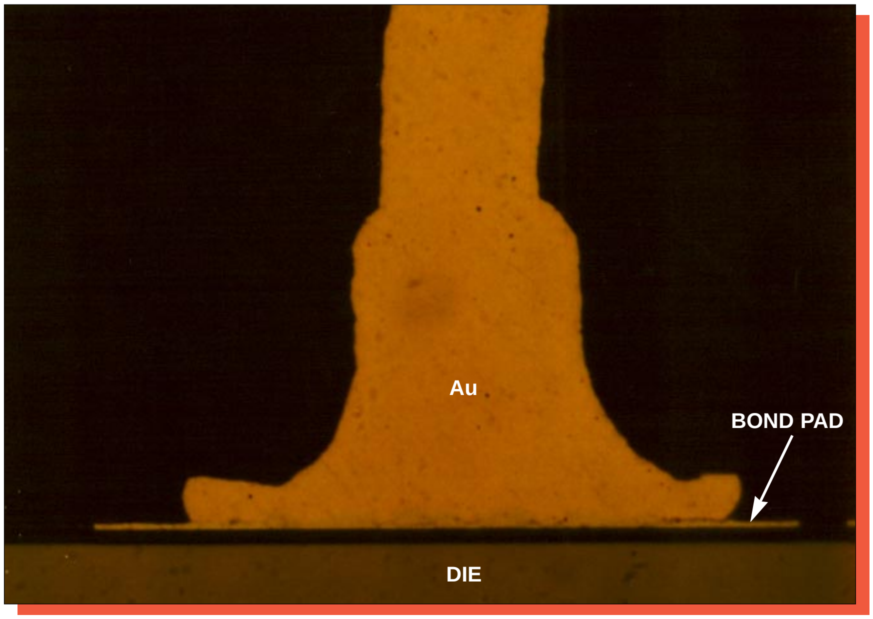


Mag. 550x

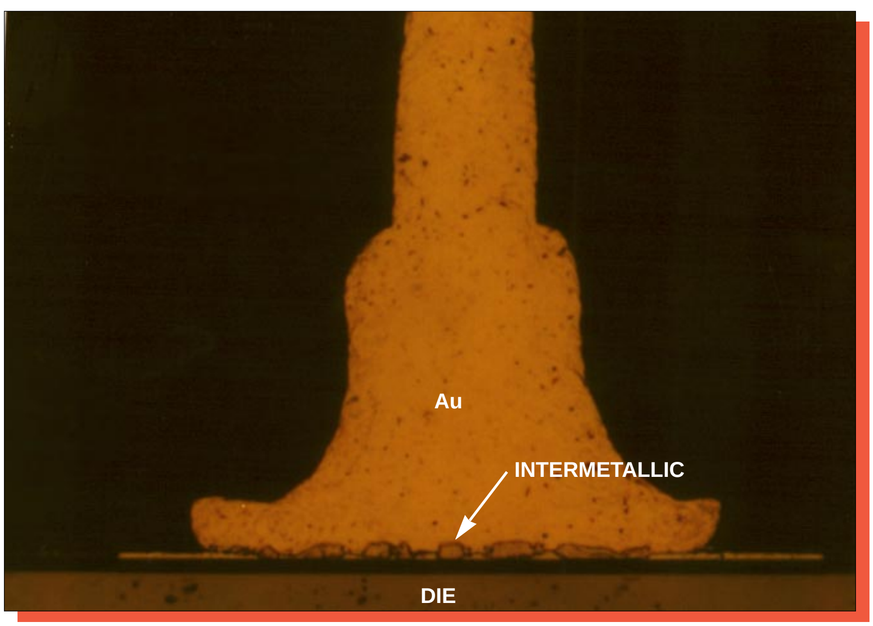


Mag. 460x

Figure 8. Perspective SEM views of typical bonds. 60°.



as polished



intermetallic delineation

Figure 9. Section views of a typical ball bond. Mag. 800x.

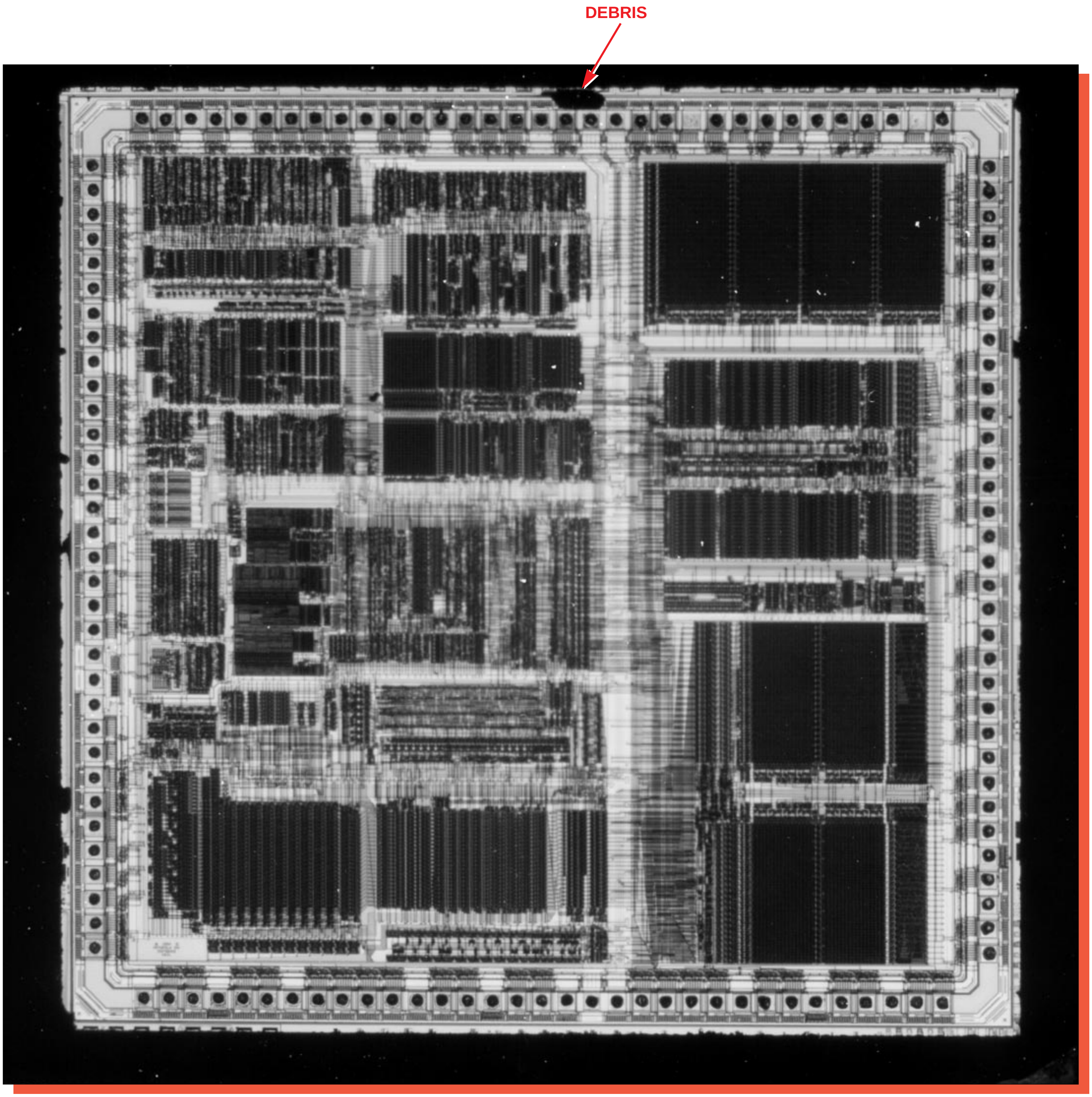
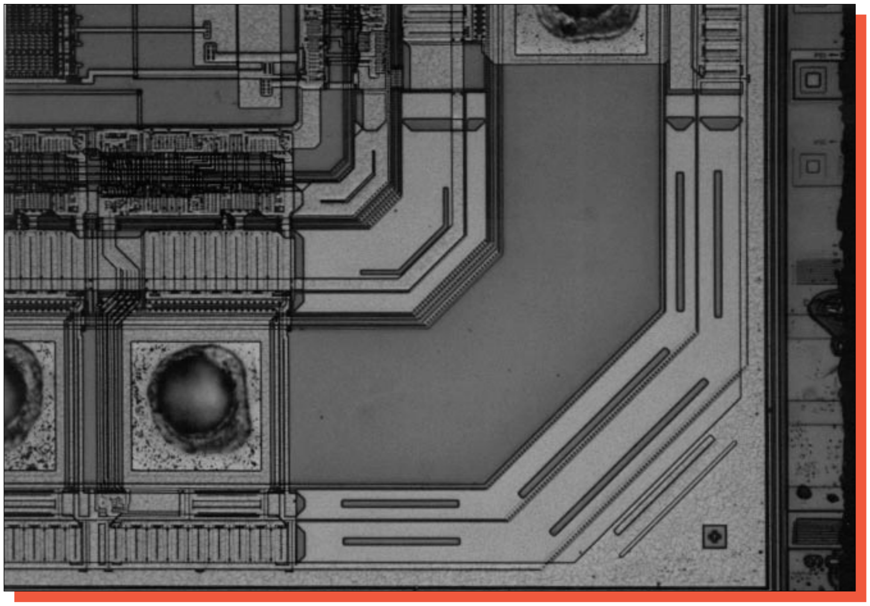
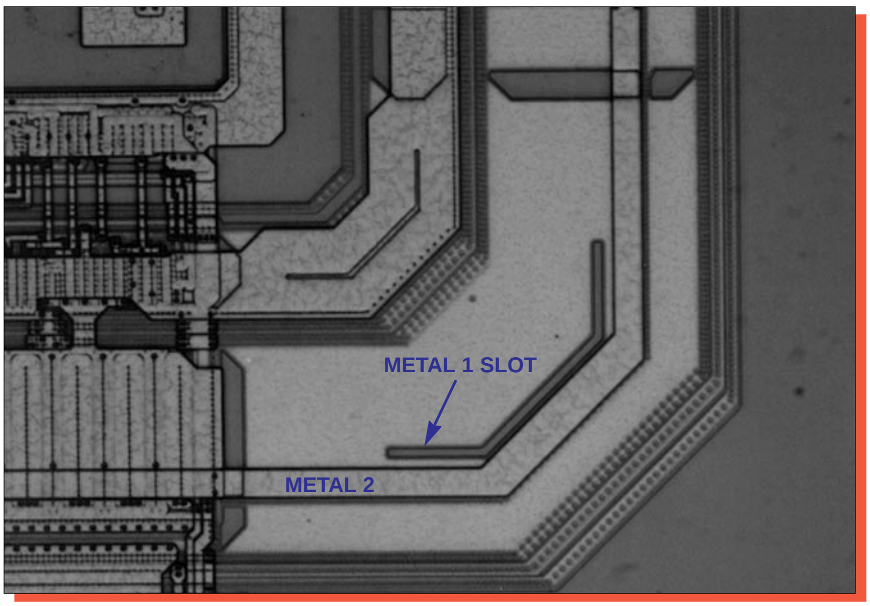


Figure 10. Whole die photograph of the Motorola XC56002PV80. Mag. 26x.

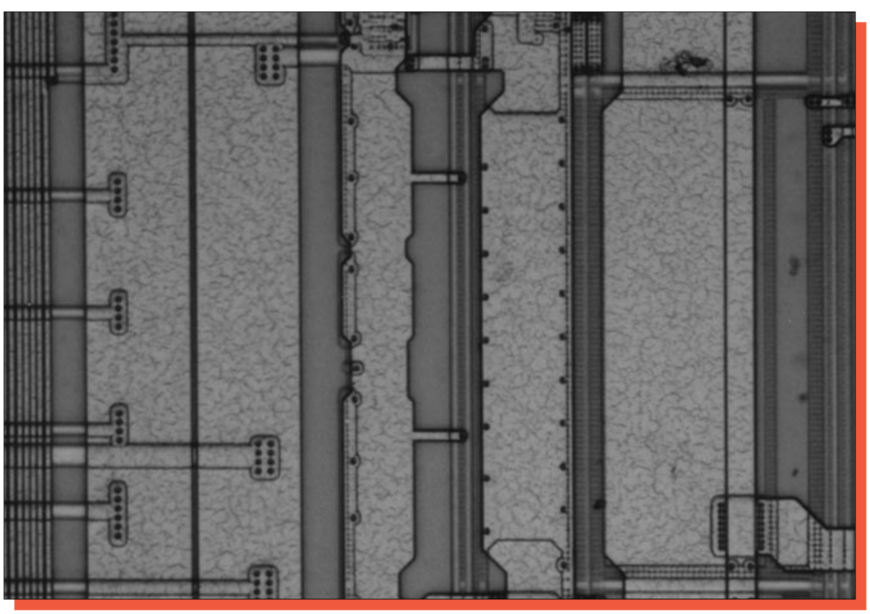
Figure 11. Optical view of marking on the die surface. Mag. 400x.



Mag. 160x

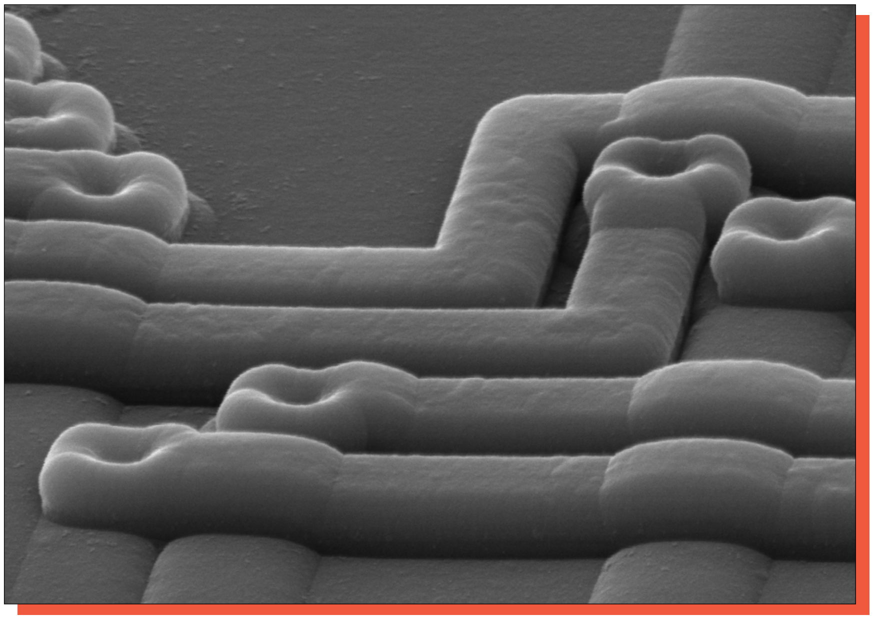


Mag. 400x

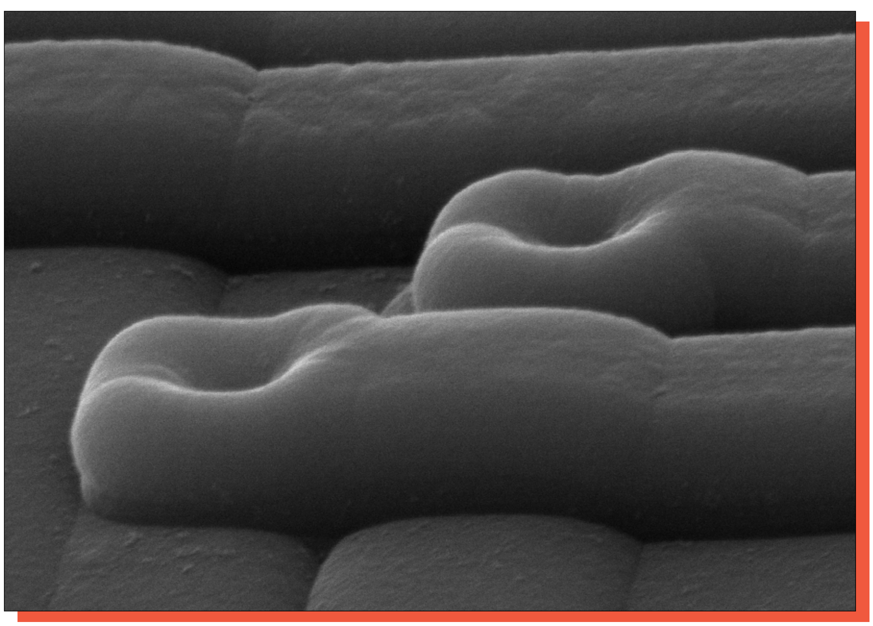


Mag. 400x

Figure 12. Optical views of slotted and beveled metal 2 bus lines.

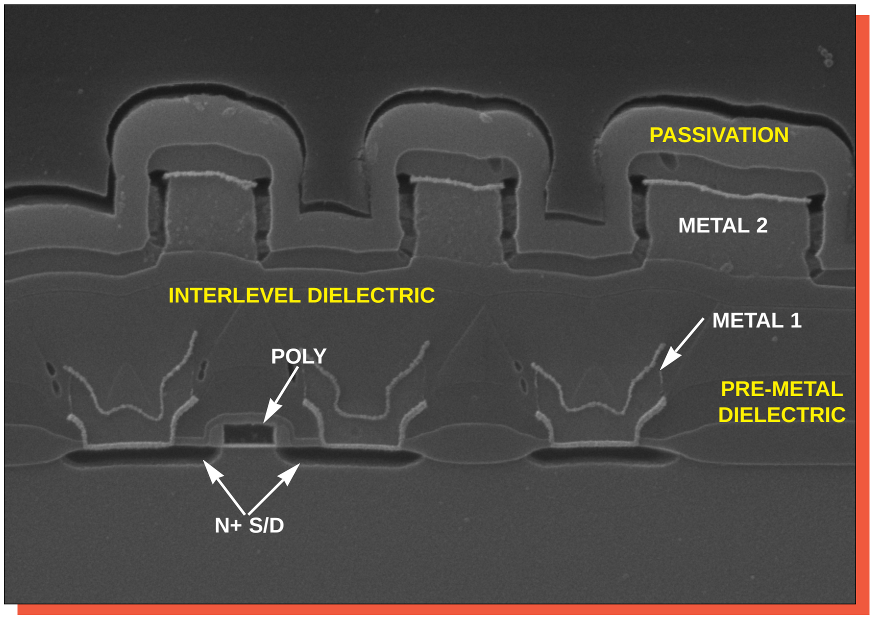


Mag. 6000x



Mag. 12,000x

Figure 13. Perspective SEM views illustrating general overlay passivation coverage. 60°.



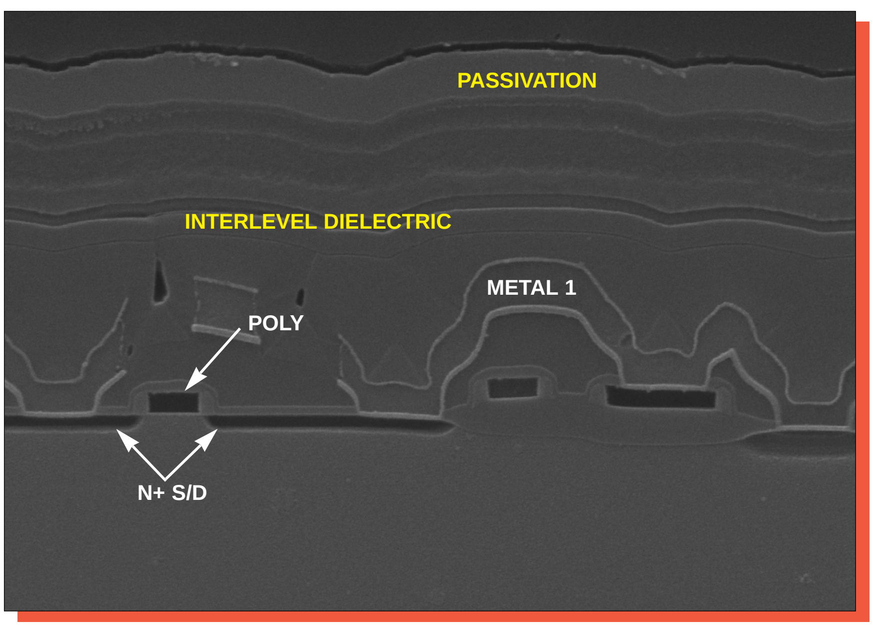
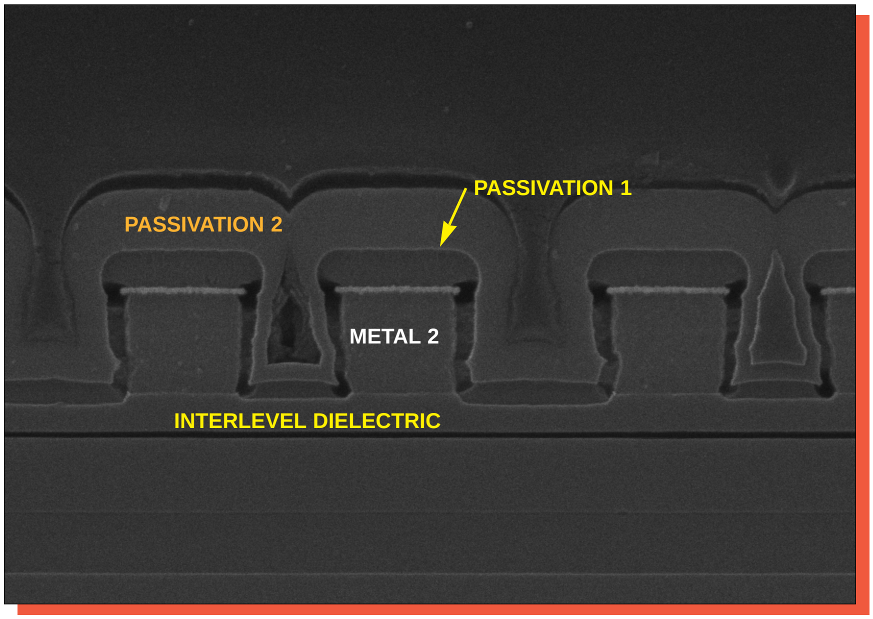
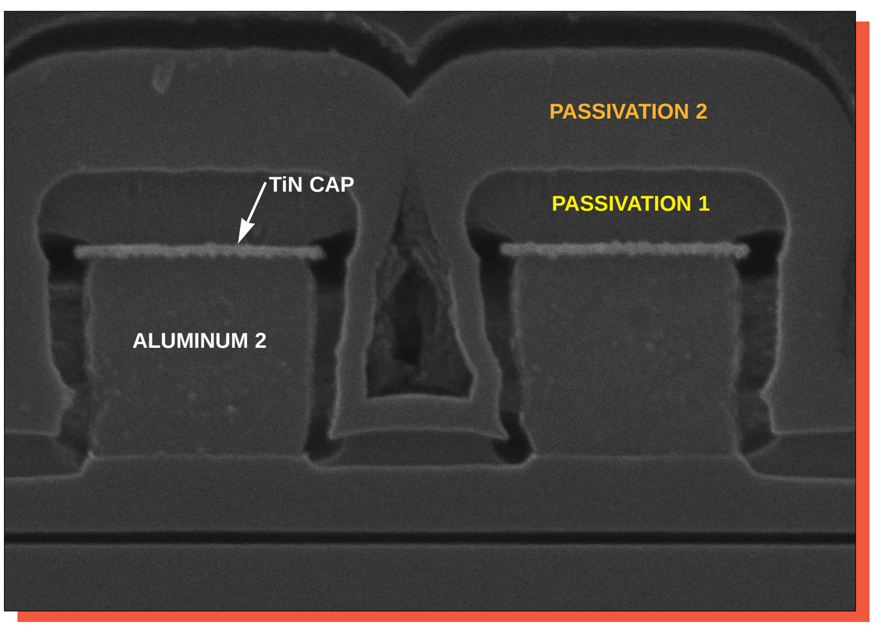


Figure 14. SEM section views illustrating general device structure. Mag. 10,000x.

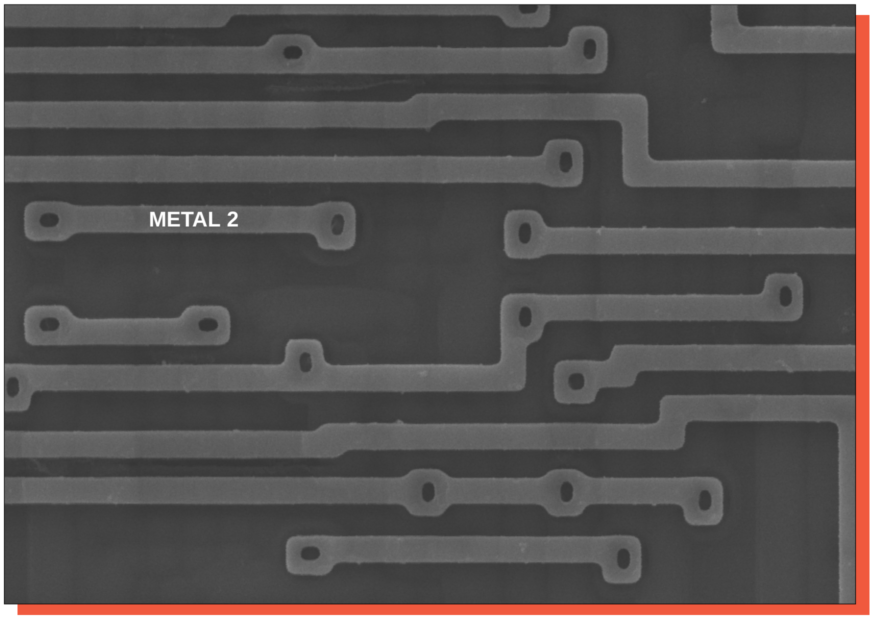


Mag. 13,000x

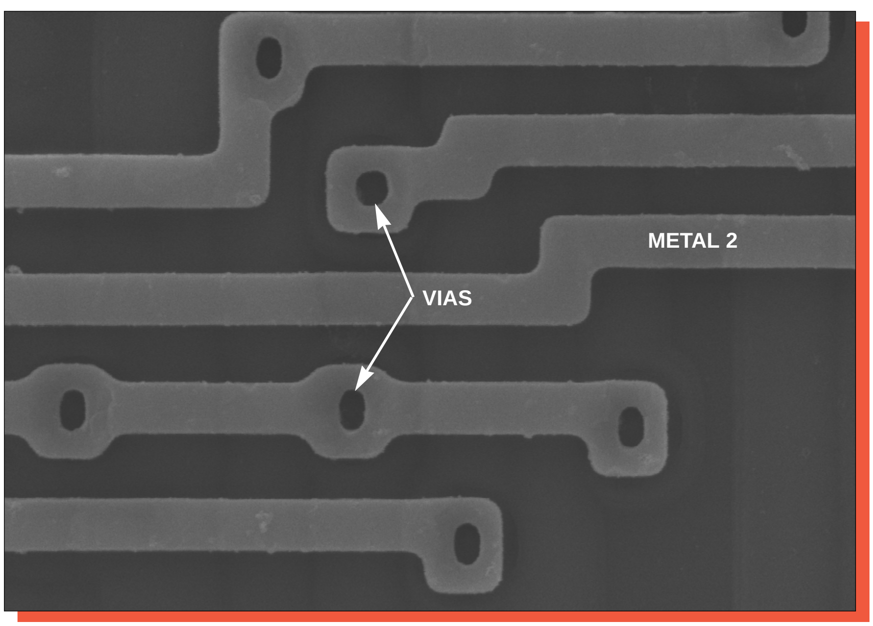


Mag. 26,000x

Figure 15. SEM section views of metal 2 line profiles.

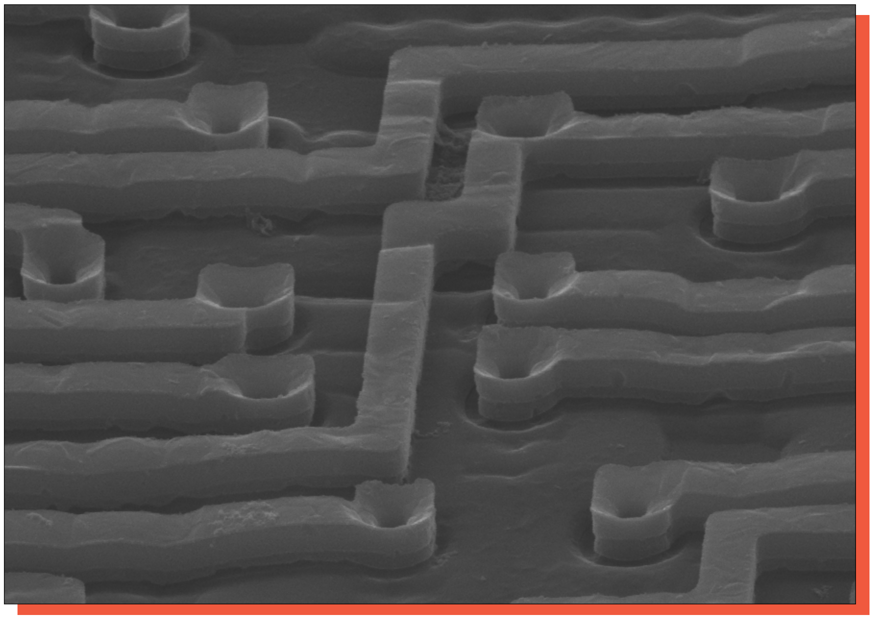


Mag. 2700x

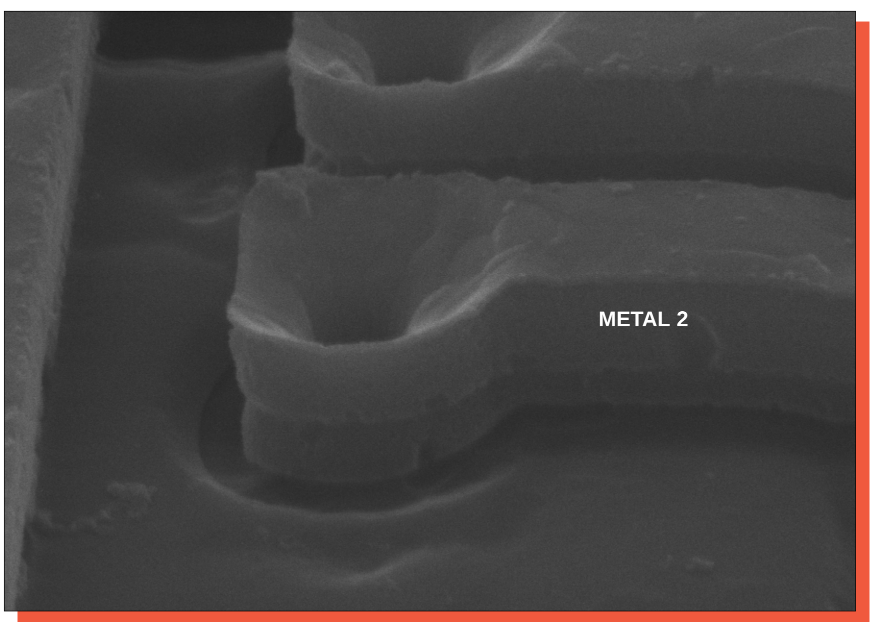


Mag. 5500x

Figure 16. Topological SEM views illustrating metal 2 patterning. 0°.

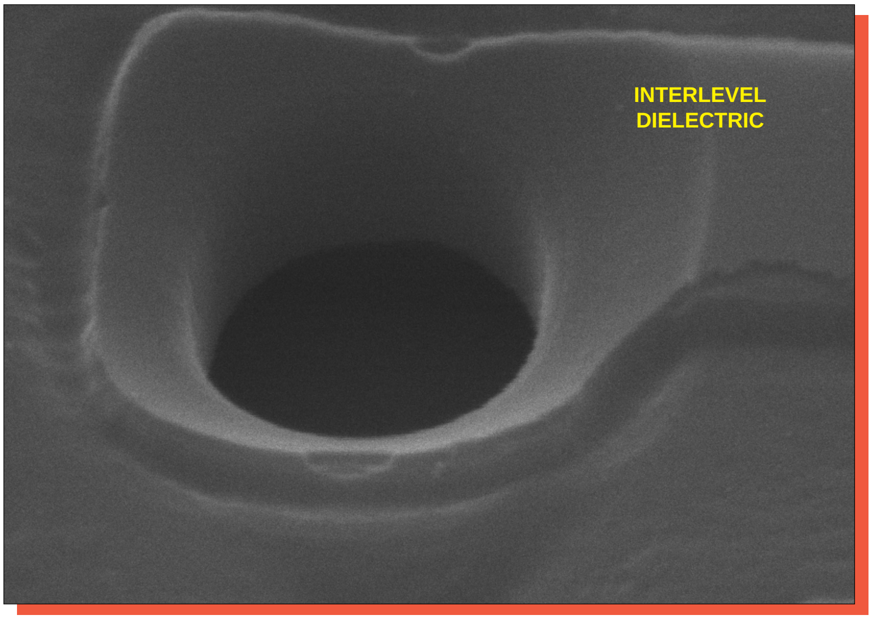


Mag. 6000x

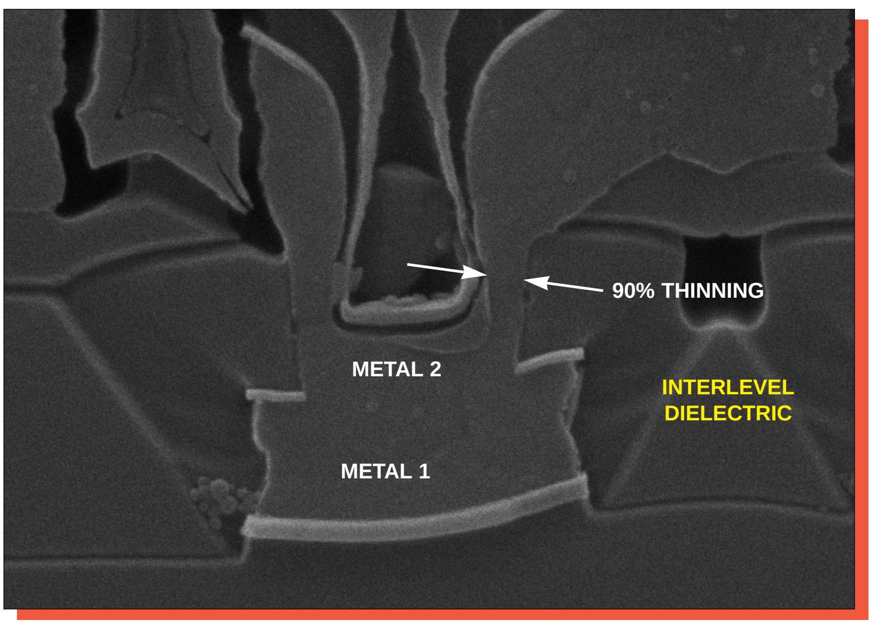


Mag. 20,000x

Figure 17. Perspective SEM views illustrating metal 2 step coverage. 60°.

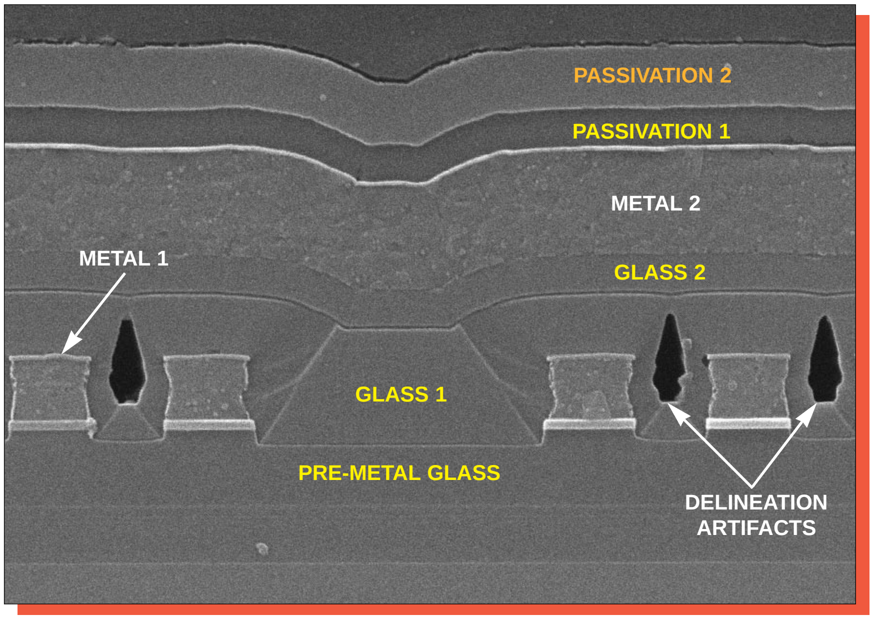


Mag. 37,000x, 45°

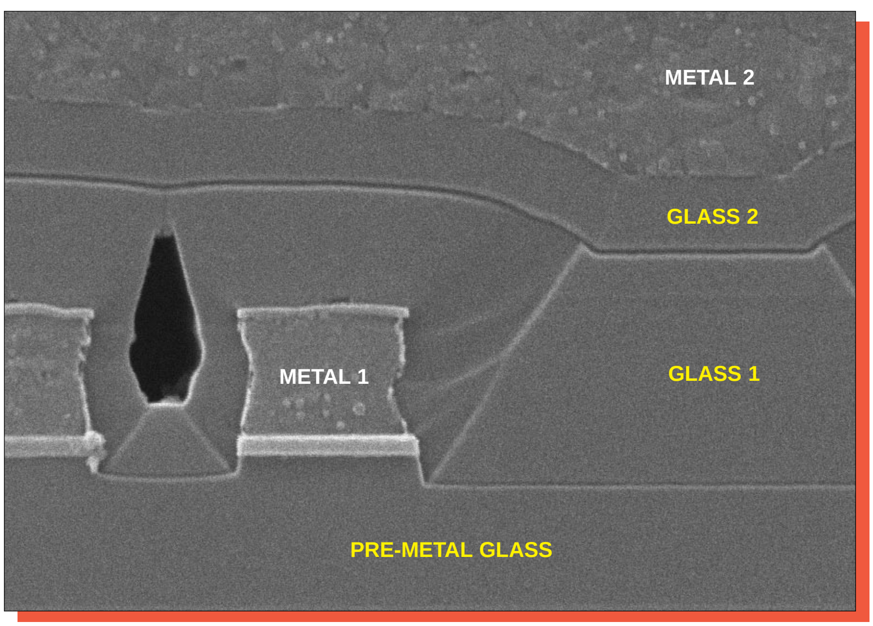


Mag. 26,000x

Figure 18. SEM views illustrating metal 2-to-metal 1 vias.

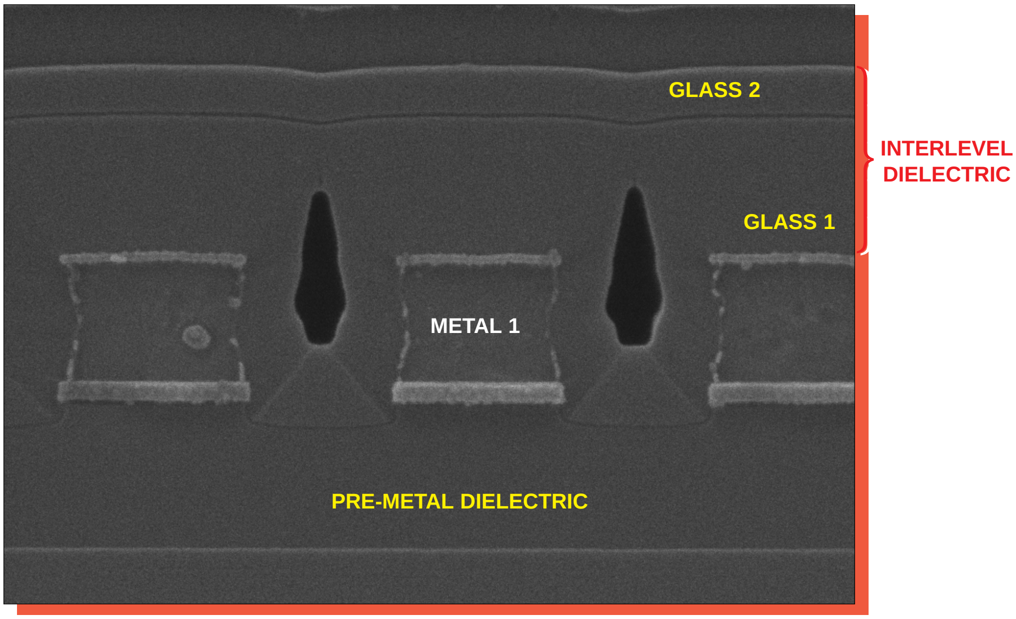


Mag. 13,000x

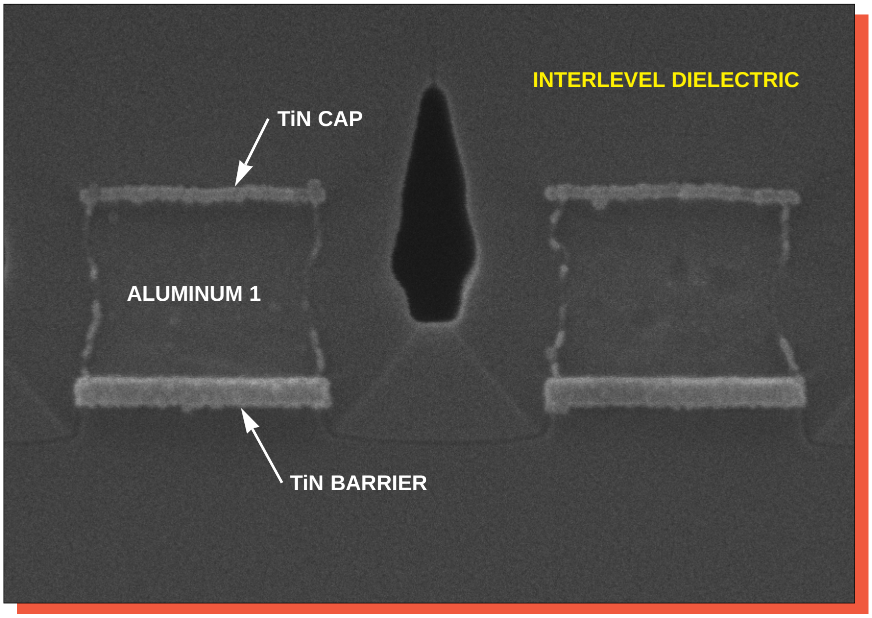


Mag. 26,000x

Figure 19. Detailed views of interlevel dielectric structure. Glass etch delineation.

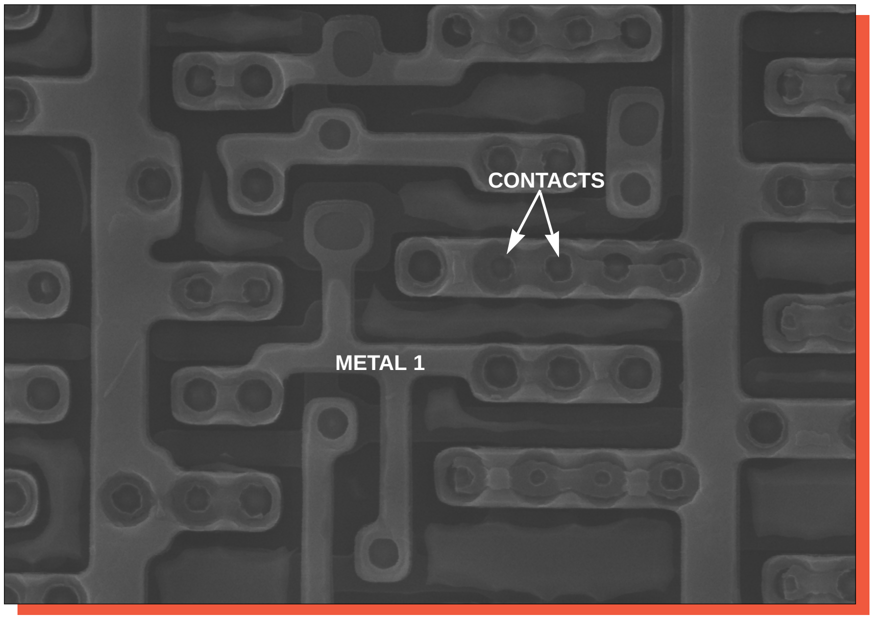


Mag. 26,000x

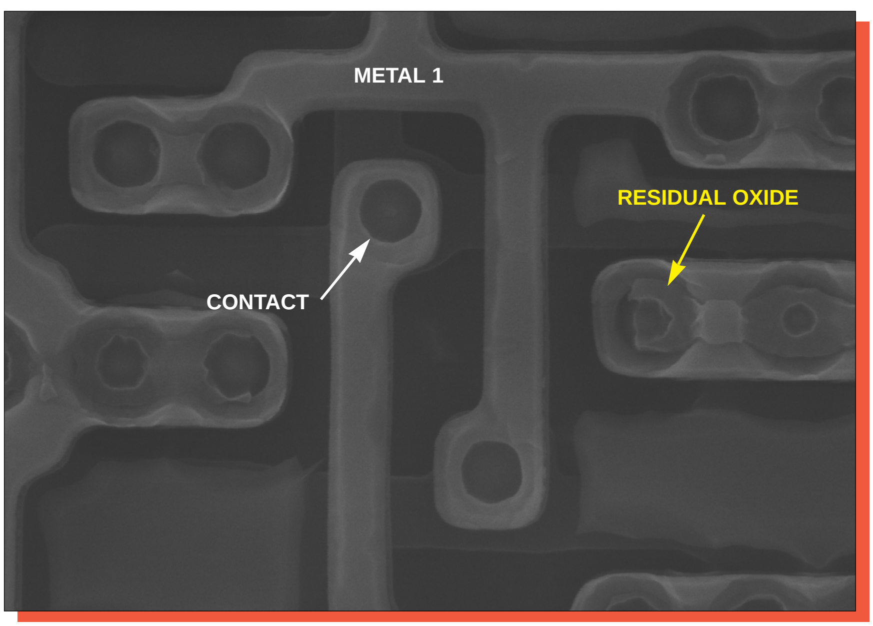


Mag. 40,000x

Figure 19a. SEM section views of metal 1 line profiles.

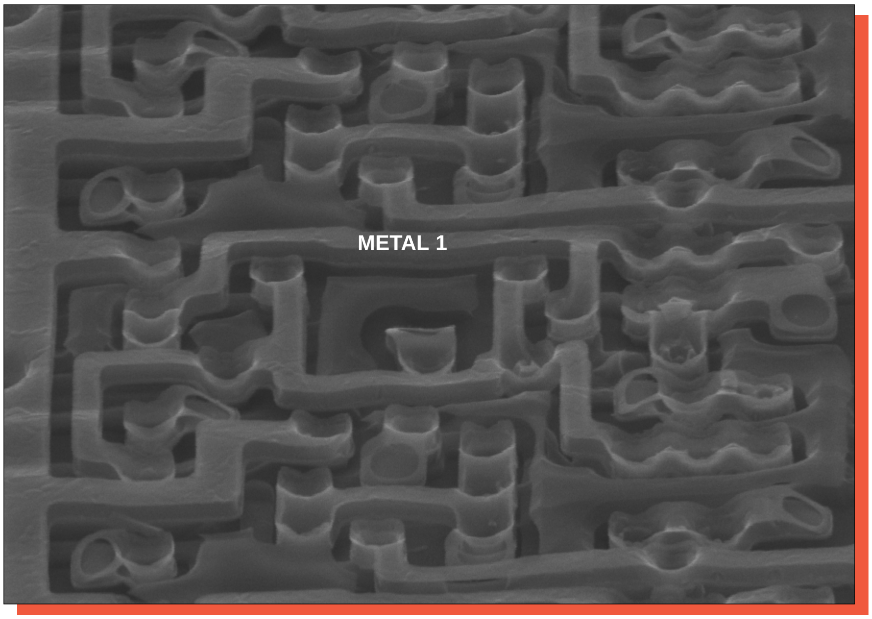


Mag. 4200x

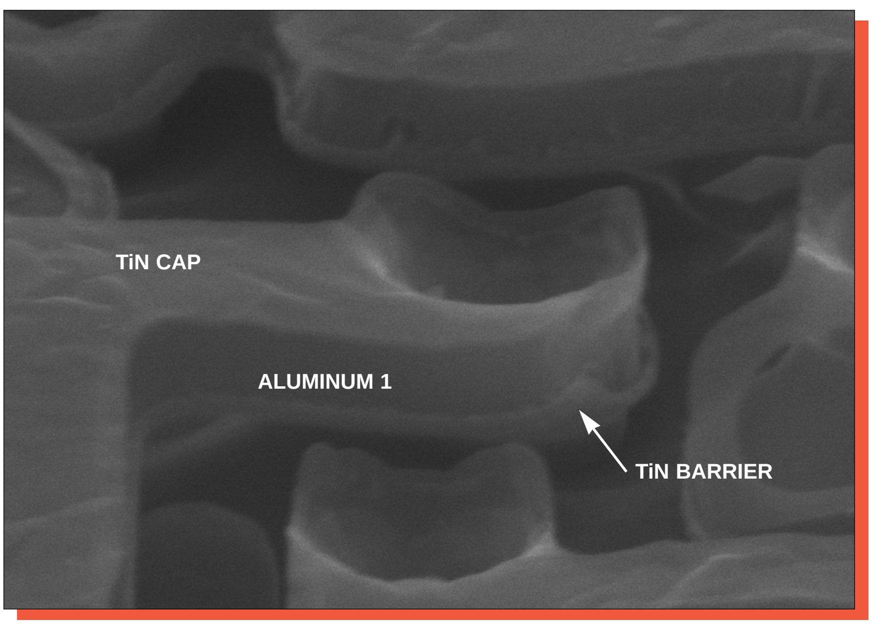


Mag. 8400x

Figure 20. Topological SEM views of metal 1 patterning. 0°.

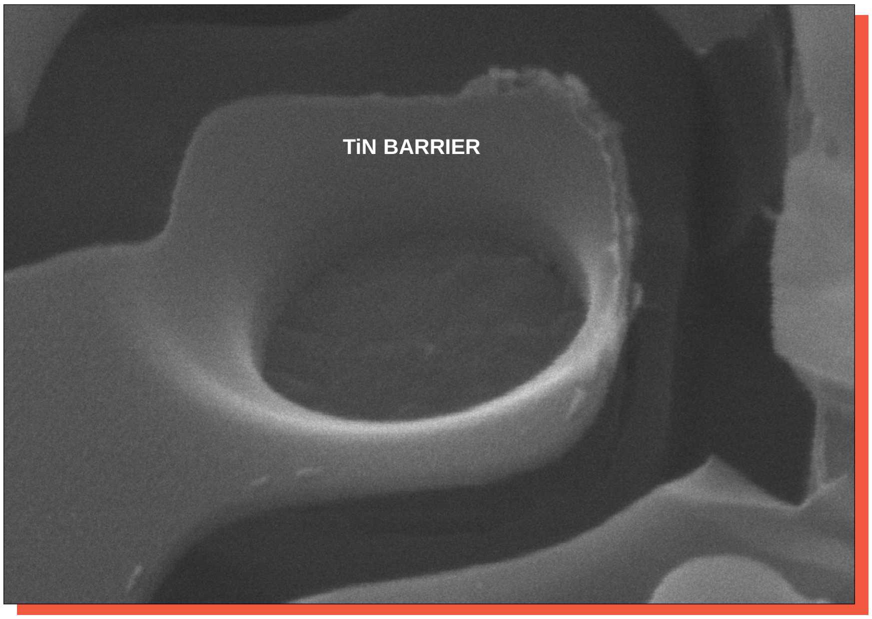


Mag. 4200x

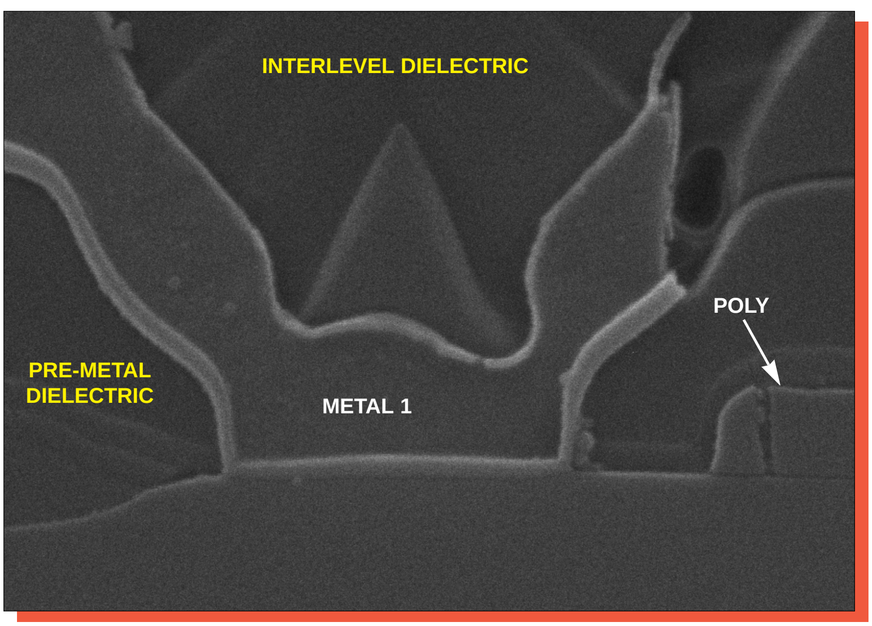


Mag. 20,000x

Figure 21. Perspective SEM views illustrating metal 1 step coverage. 60°.

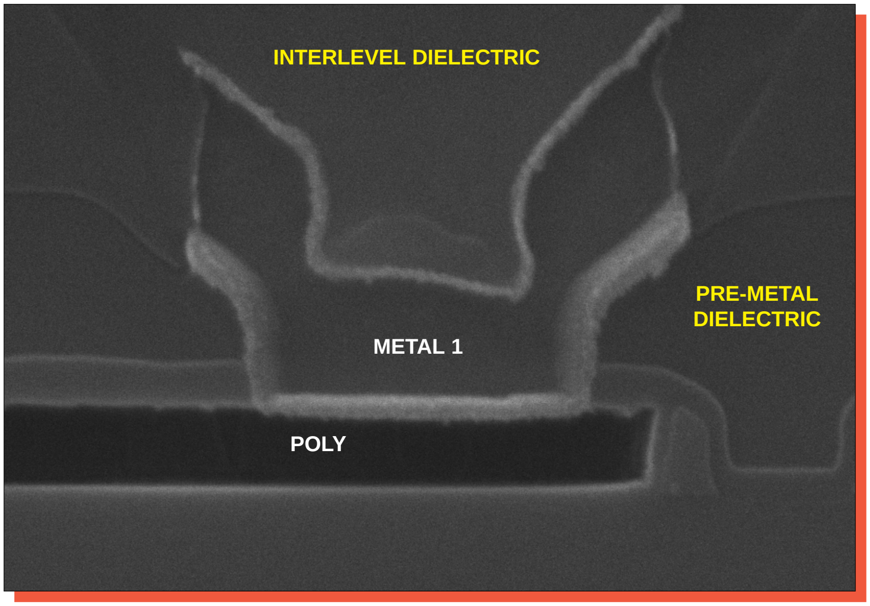


Mag. 37,000x, 45°

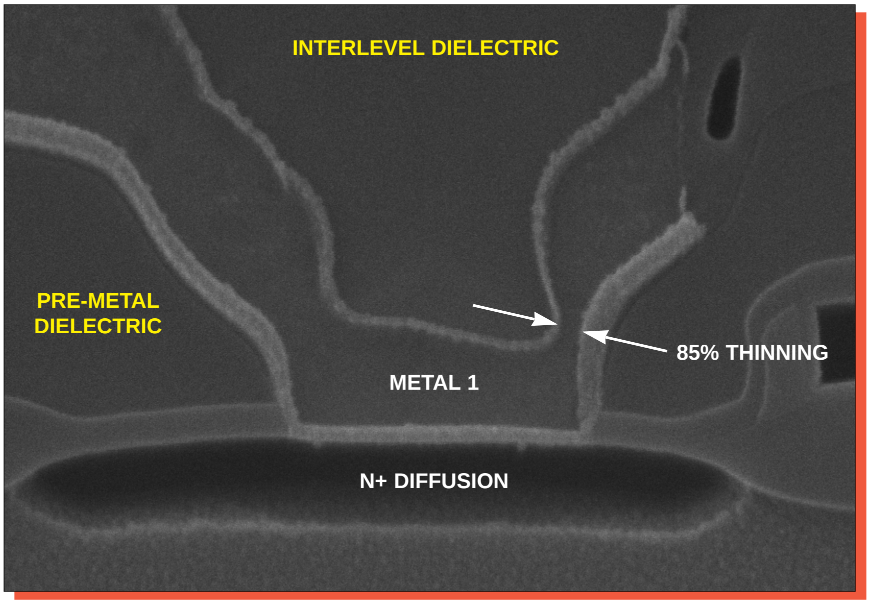


Glass etch, Mag. 40,000x

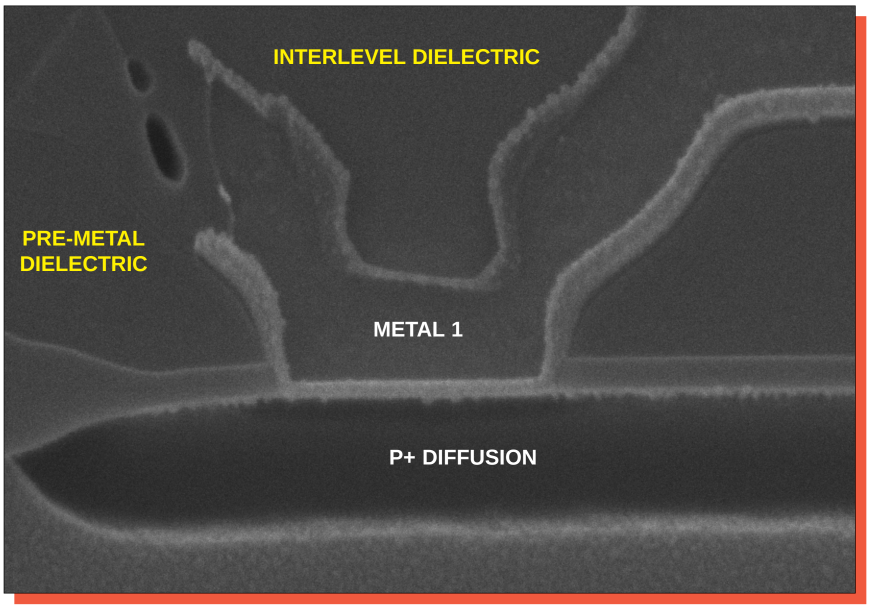
Figure 22. SEM views of barrier coverage and a metal 1 contact.



metal 1-to-poly

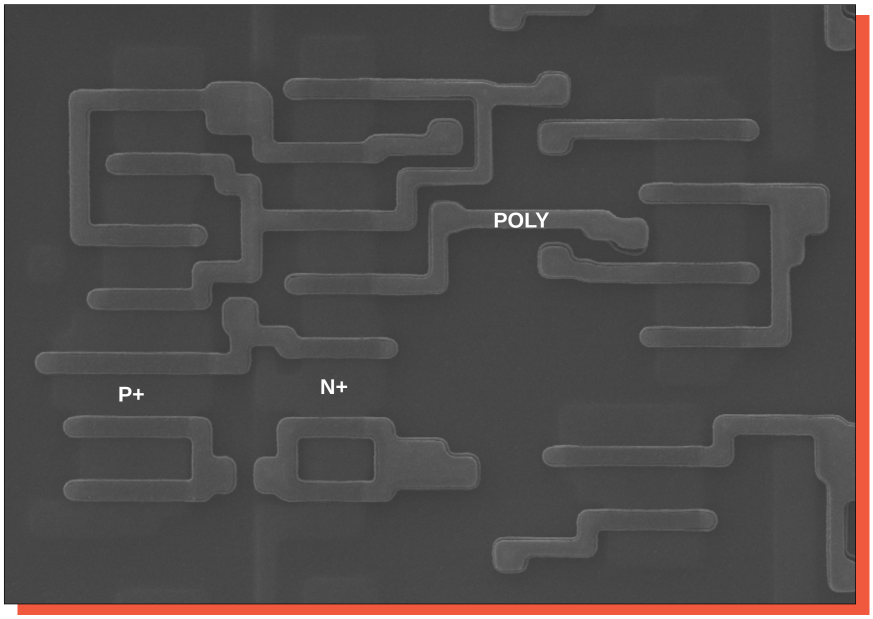


metal 1-to-N+

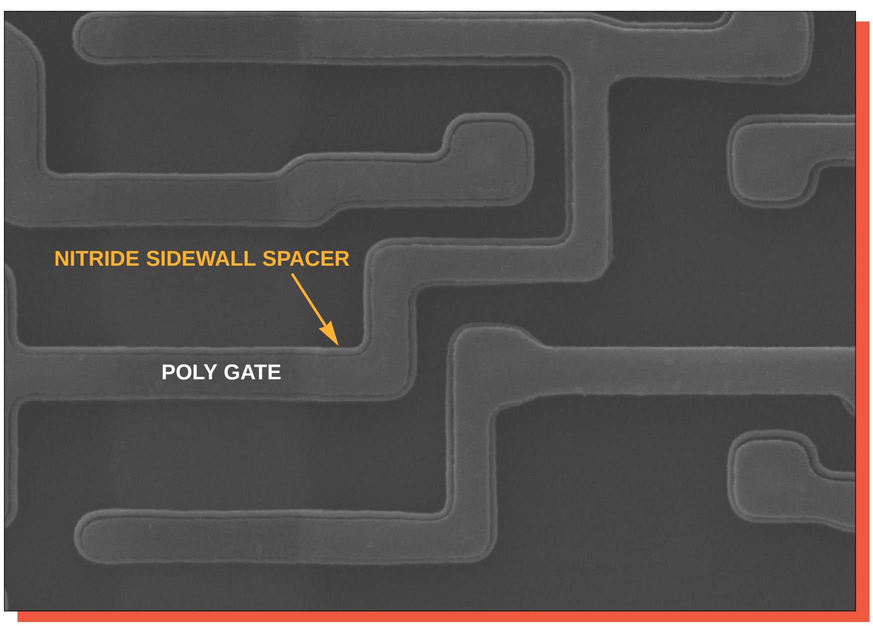


metal 1-to-P+

Figure 23. SEM section views of metal 1 contacts (silicon etch). Mag. 40,000x.

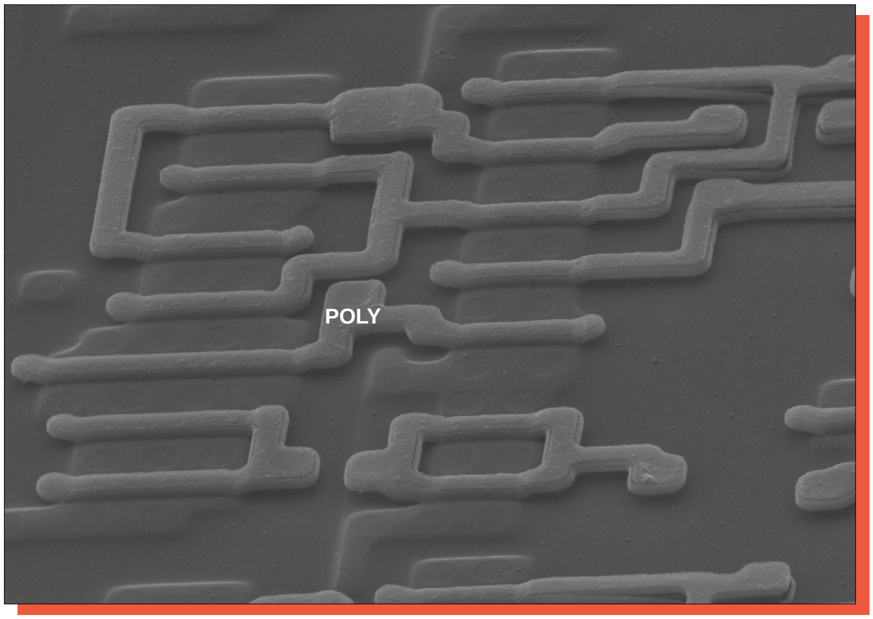


Mag. 2600x

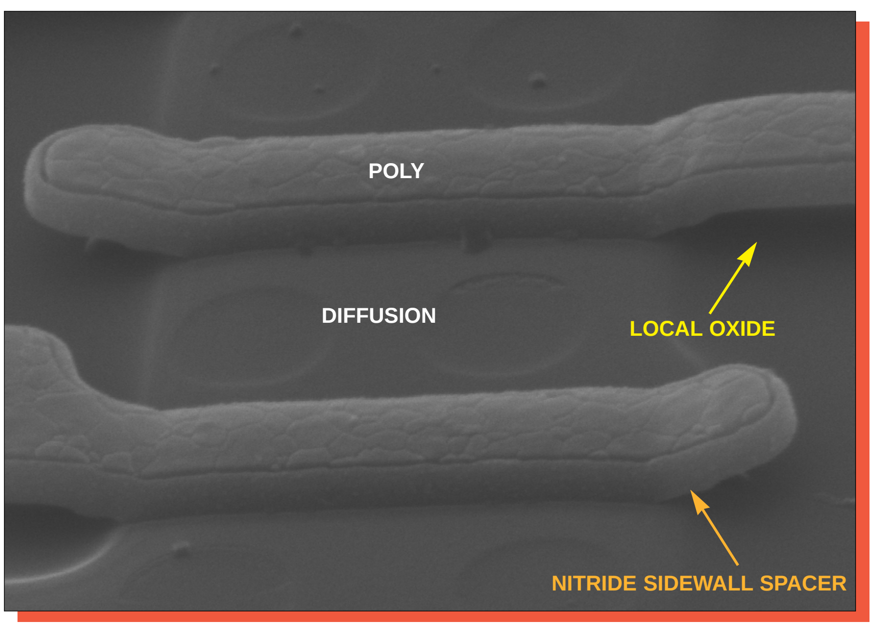


Mag. 6500x

Figure 24. Topological SEM views of poly patterning. 0°.

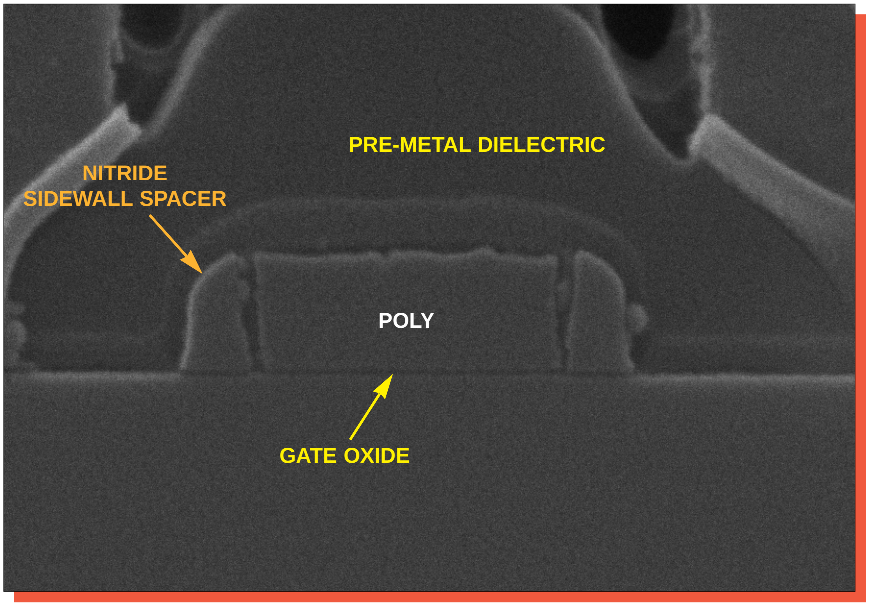


Mag. 4200x

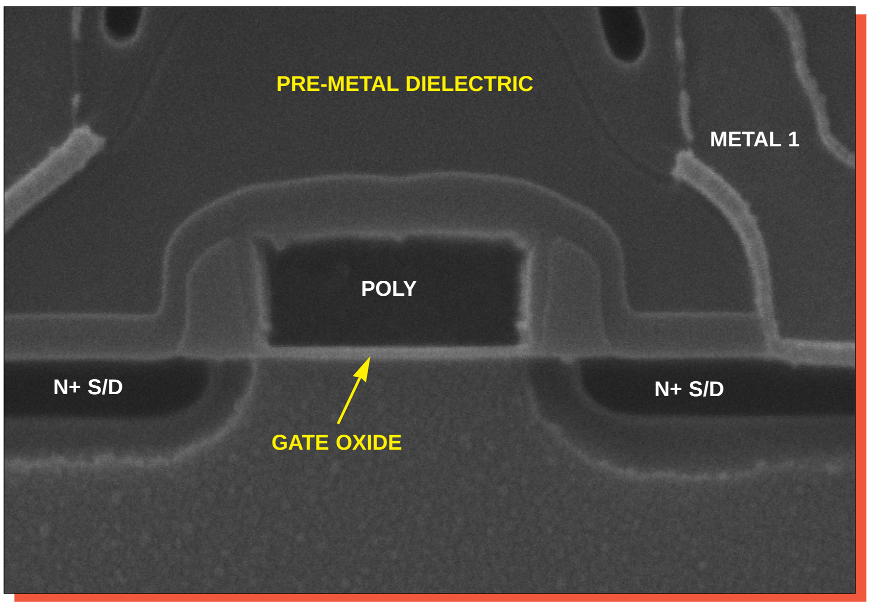


Mag. 18,000x

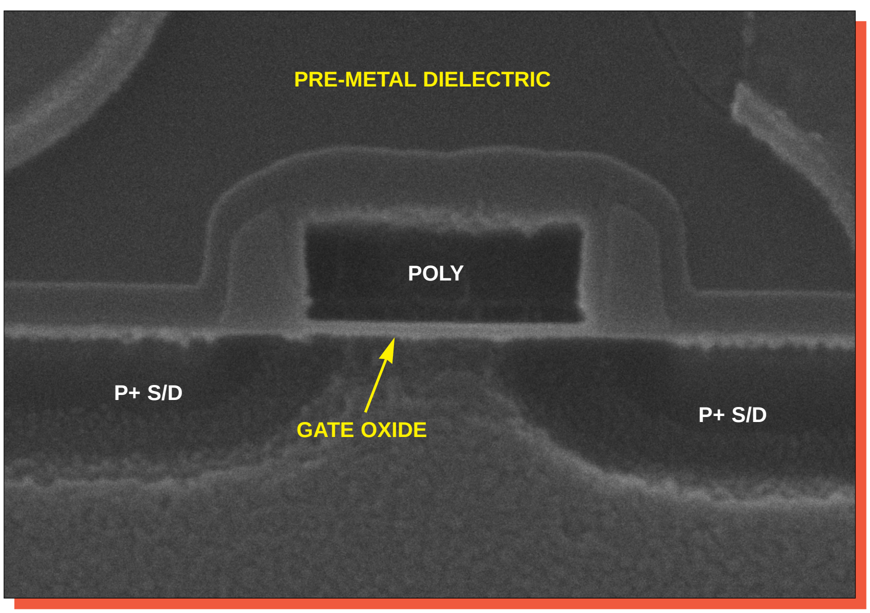
Figure 25. Perspective SEM views of poly coverage. 60°.



glass etch



N-channel



P-channel

Figure 26. SEM section views of typical transistors. Mag. 52,000x.

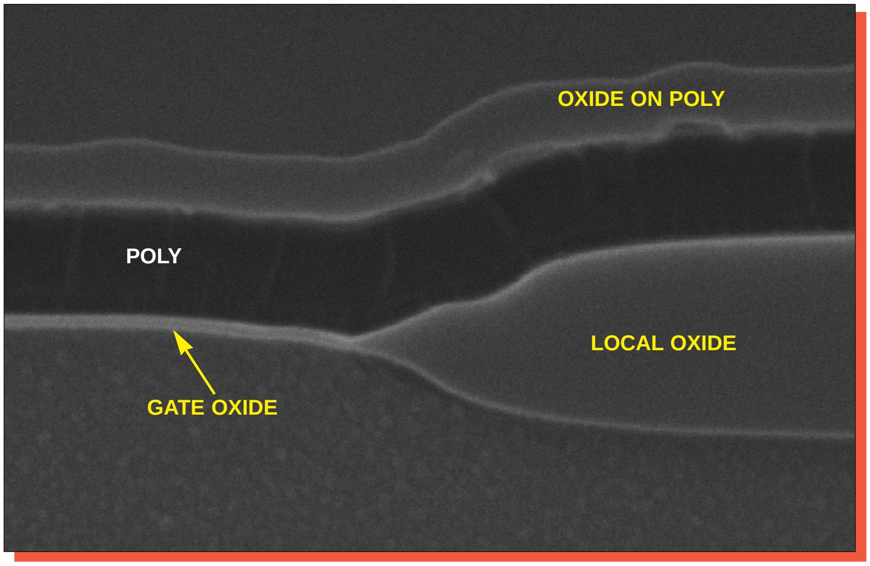
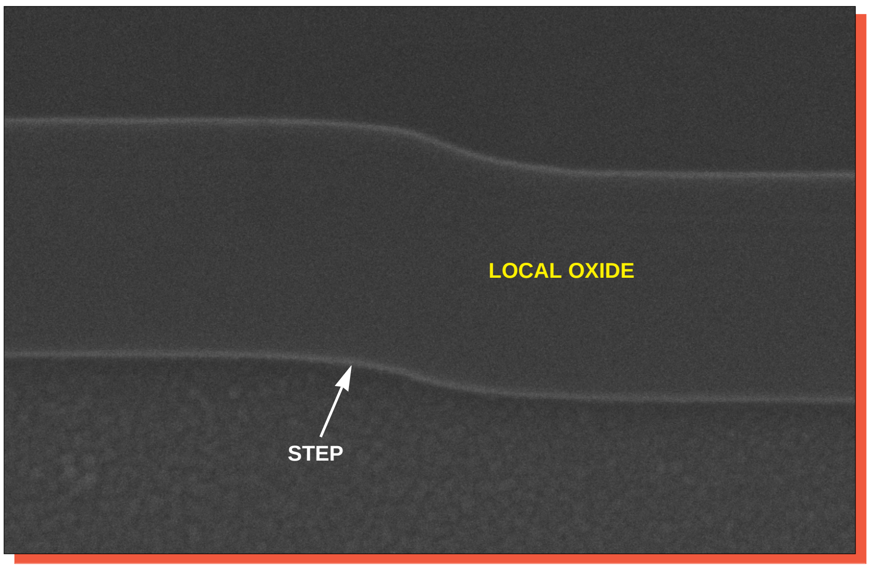
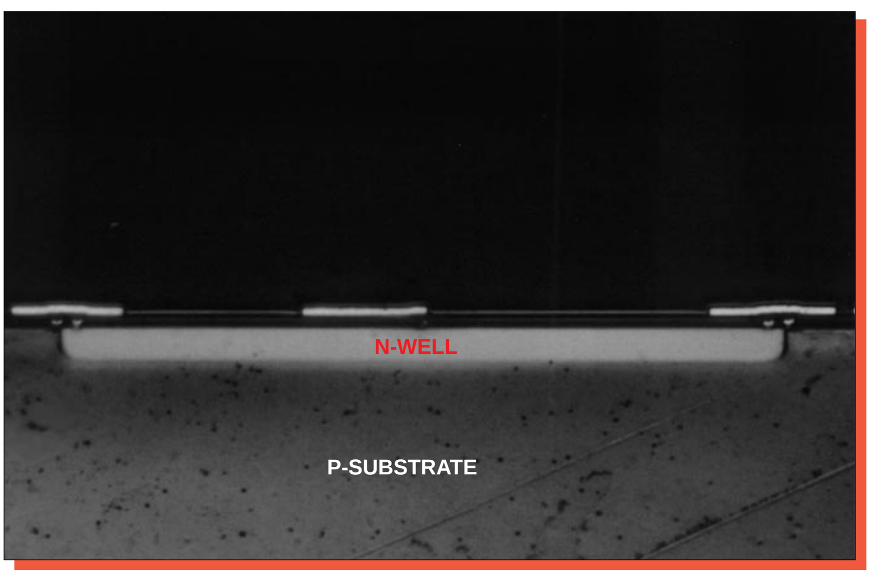


Figure 27. SEM section view of a typical local oxide birdsbeak. Mag. 52,000x.

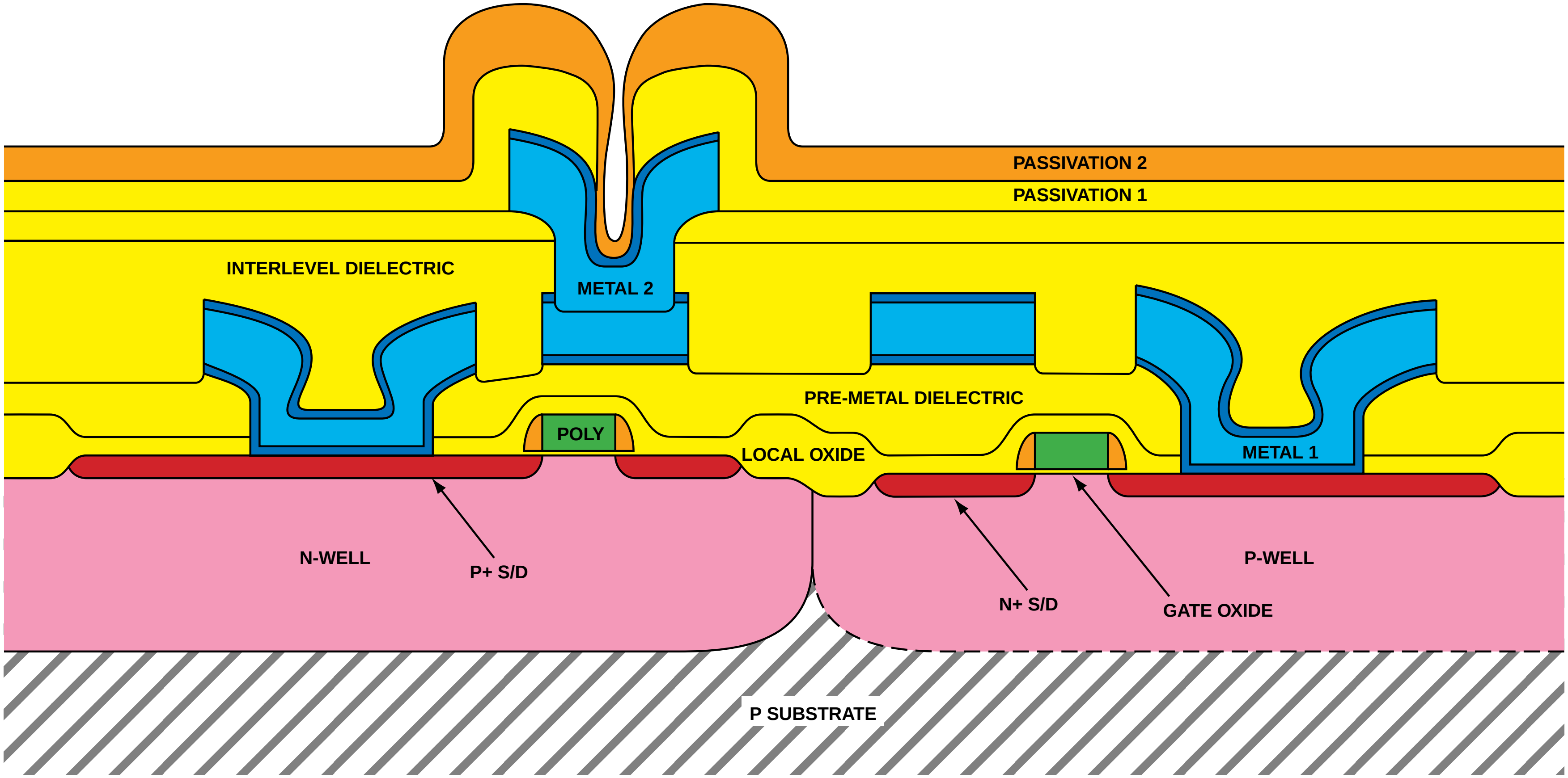


Mag. 52,000x



Mag. 800x

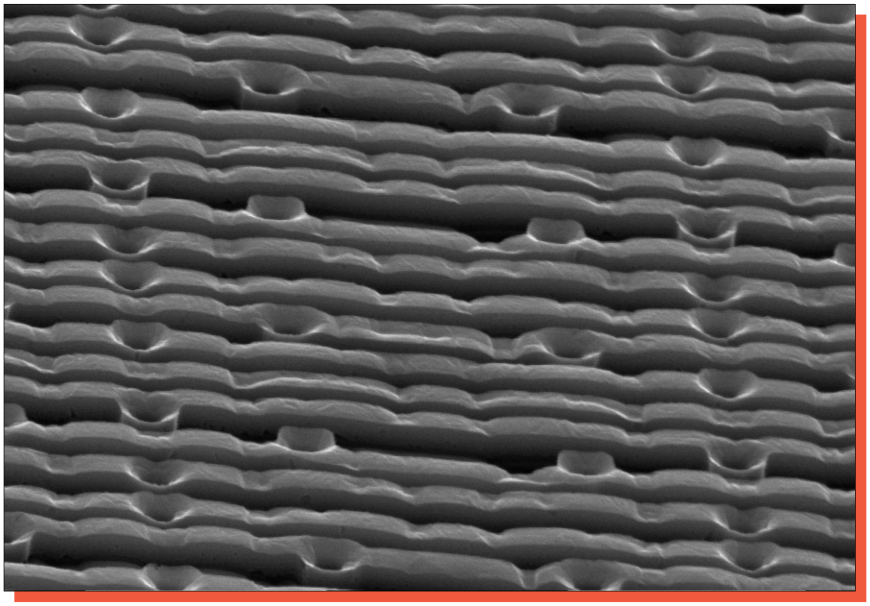
Figure 28. Section views illustrating the well structure.



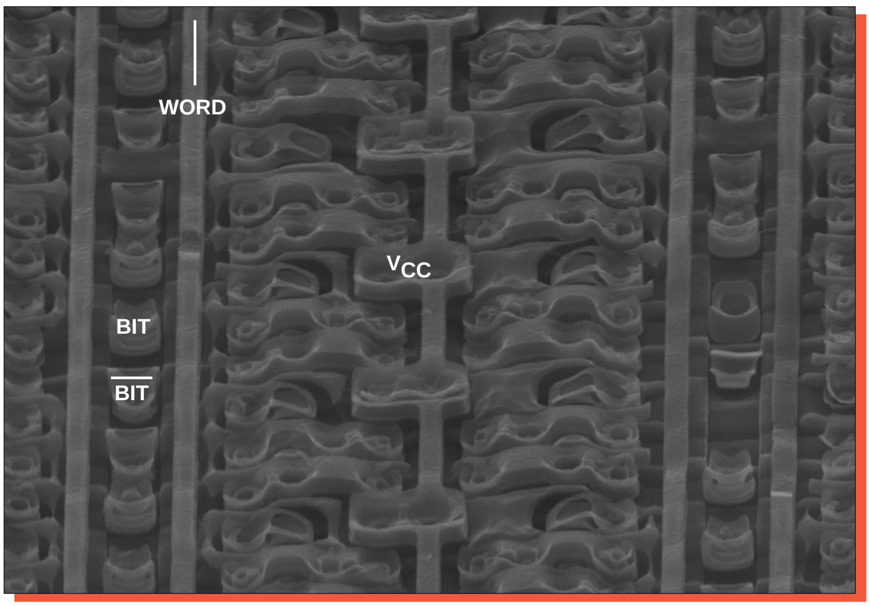
Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

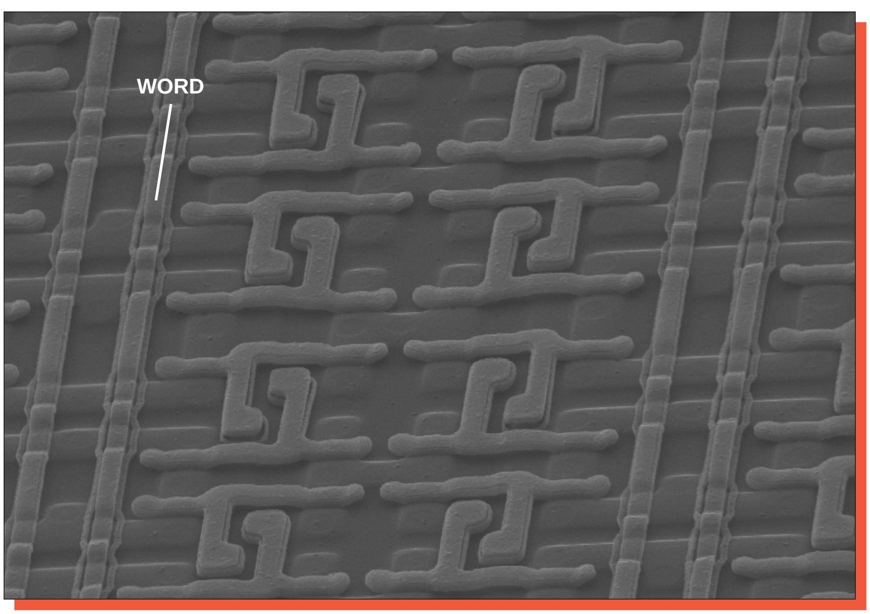
Figure 29. Color cross section drawing illustrating device structure.



metal 2

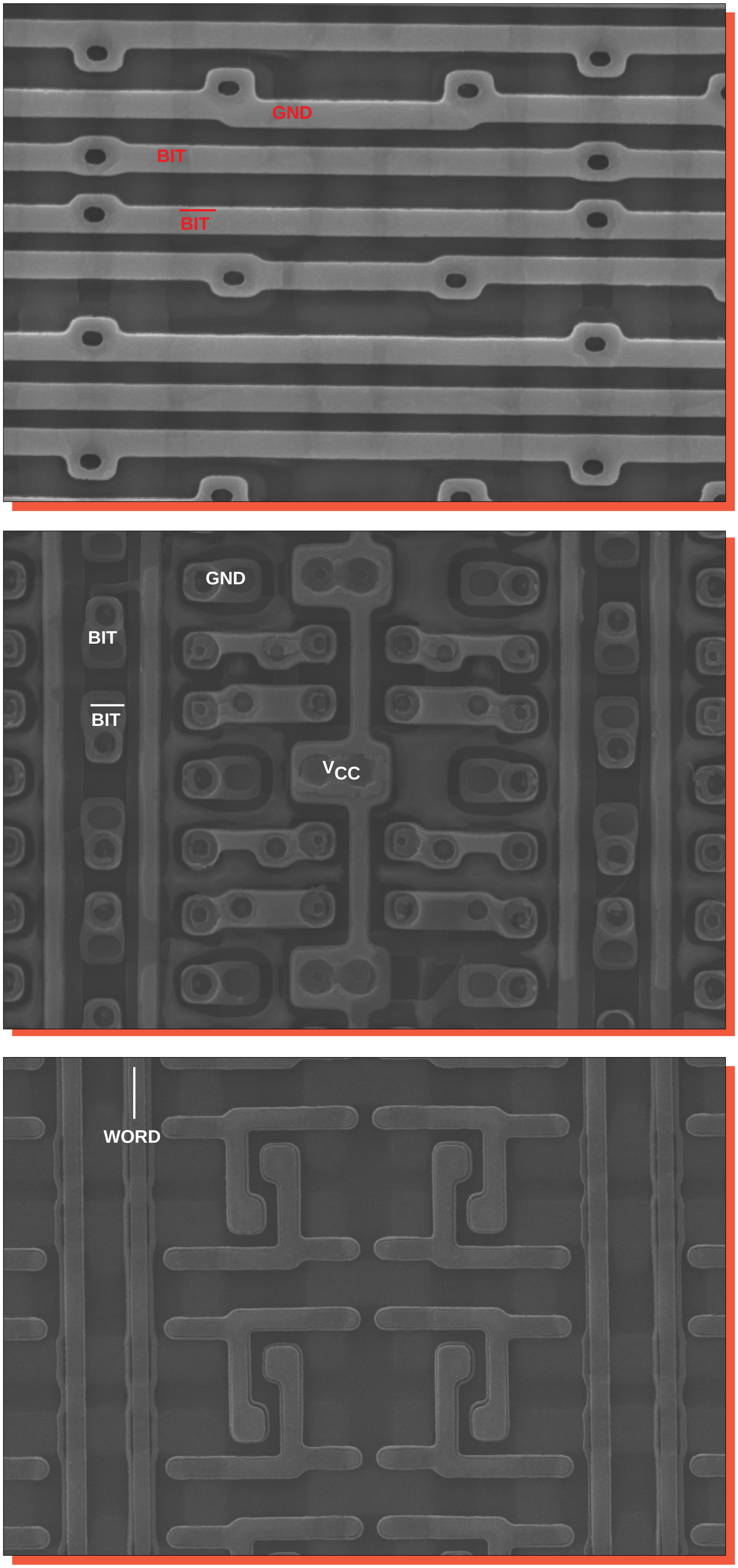


metal 1



poly

Figure 30. Perspective SEM views of SRAM cell array. Mag. 3200x, 60°.



metal 2

metal 1

poly

Figure 31. Topological SEM views of the SRAM cell array. Mag. 3200x.

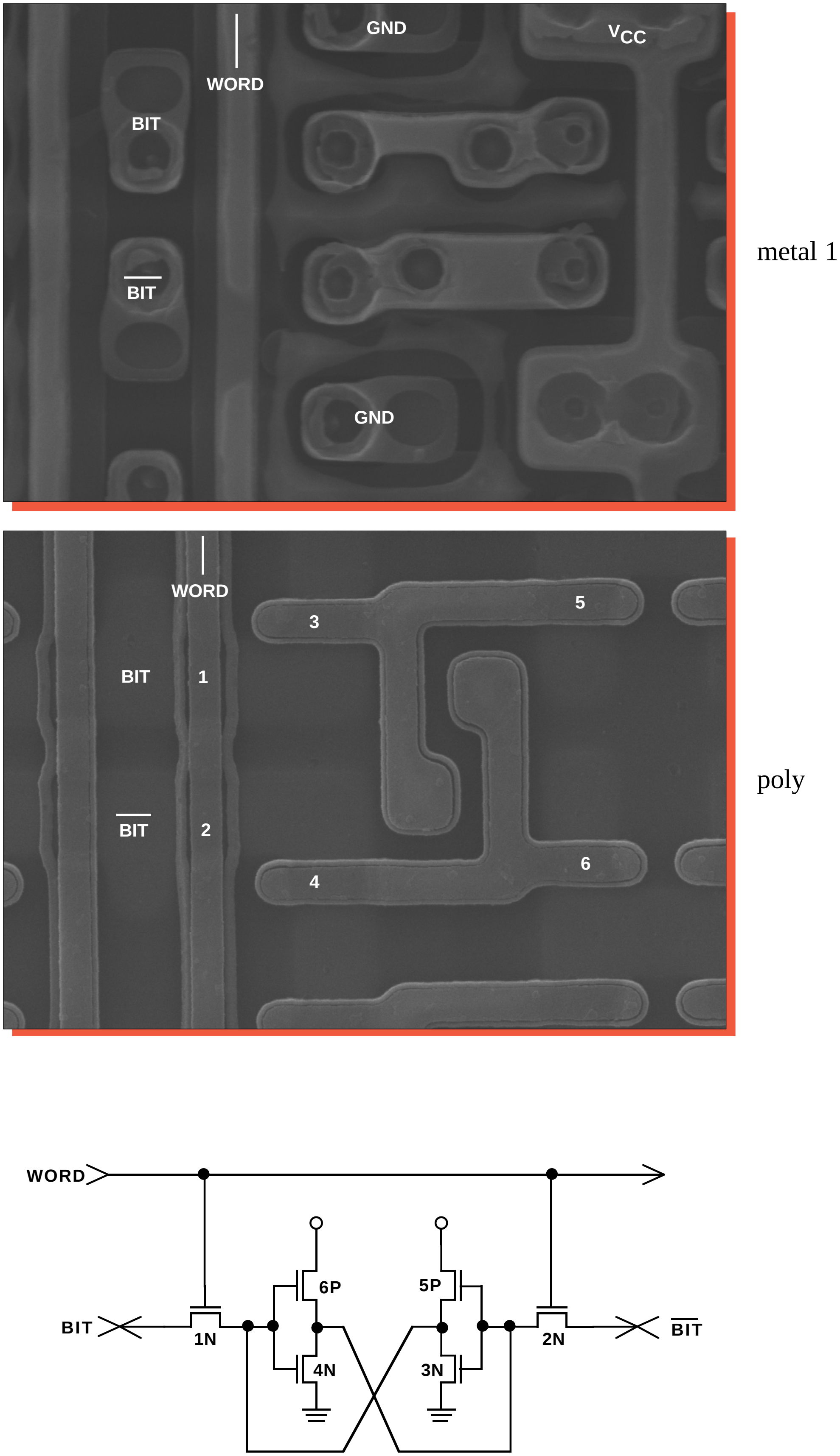
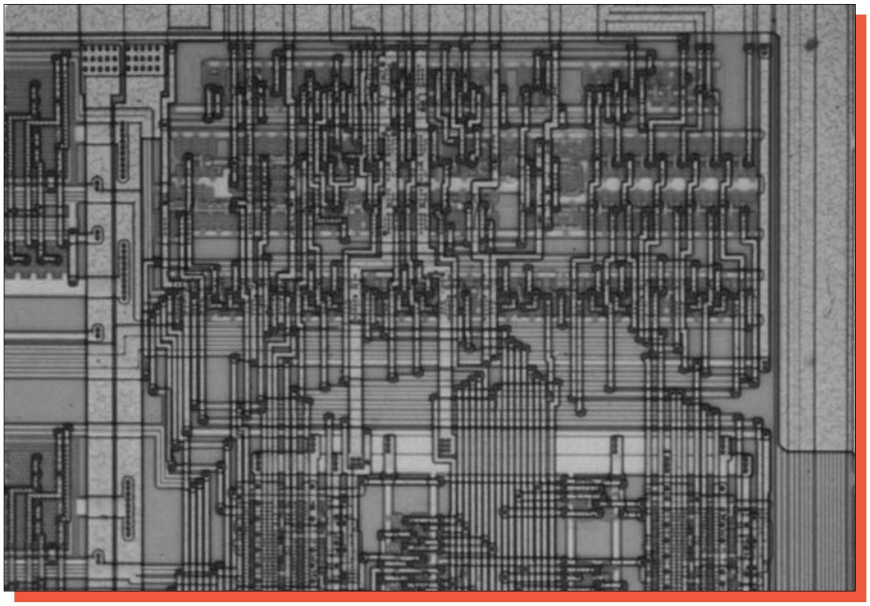
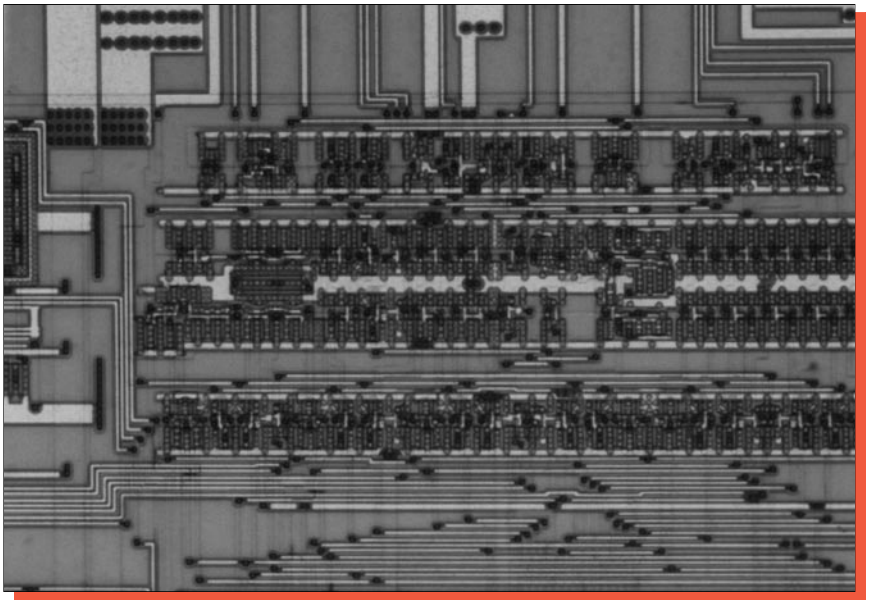


Figure 32. Topological SEM views and schematic of the SRAM cell array. Mag. 6500x.



metal 2



metal 1

unlayered

Figure 33. Optical views of general circuitry. Mag. 400x.

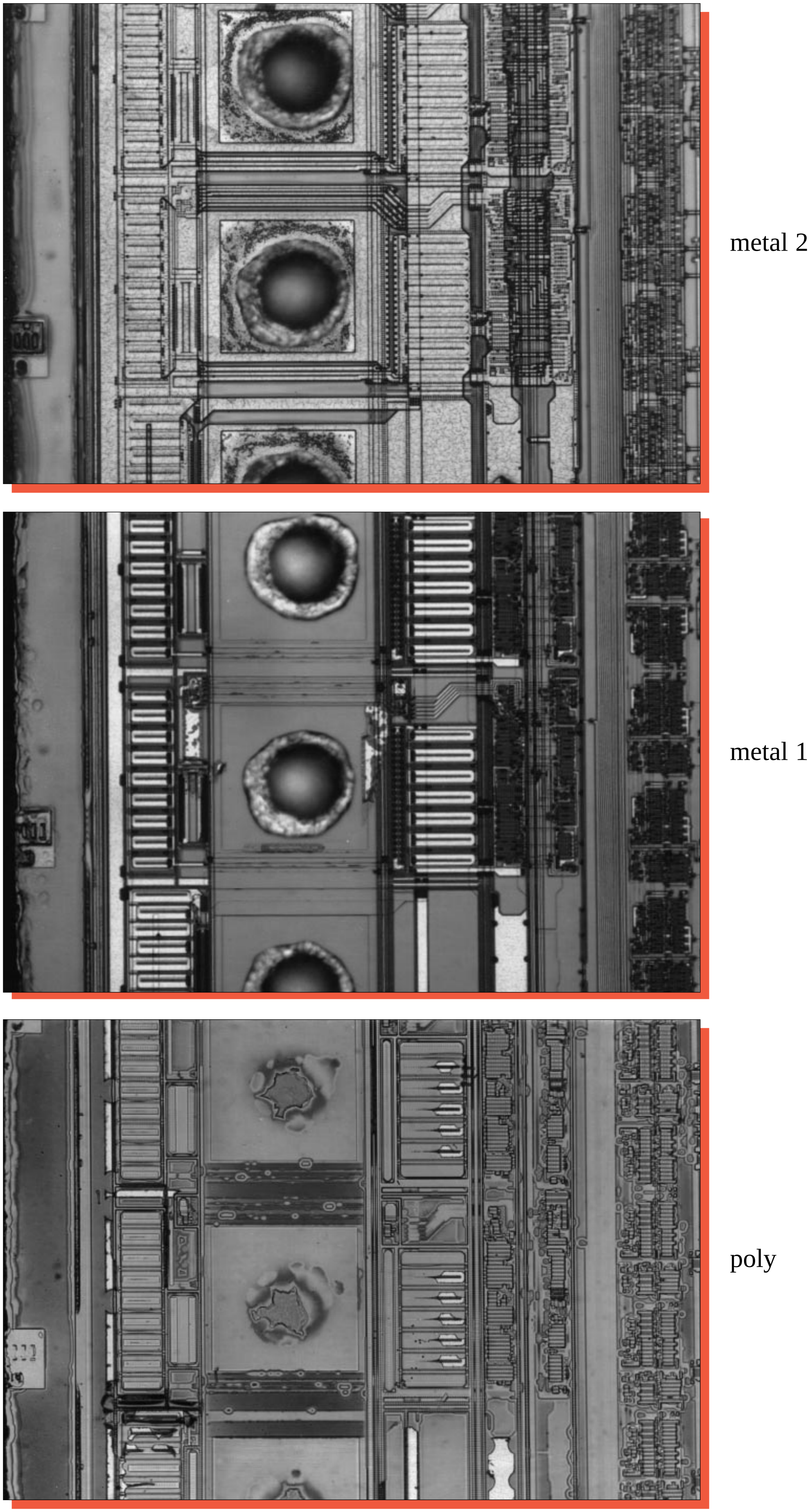


Figure 34. Optical views of a I/O structure. Mag. 200x.