Construction Analysis

Chip Express QYH530
Laser Programmable Gate Array

Report Number: SCA 9608-508

INTEGRATED CIRCUIT ENGINEERING

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INTRODUCTION

This report describes a construction analysis of the Chip Express QYH 530 LPGA (Laser Personalized Gate Array). Four devices were supplied for the analysis. They were encapsulated in 160-pin Plastic Quad Flat Packs (PQFP) for surface mount applications. All samples were date coded 9621.

MAJOR FINDINGS

Questionable Items:[1]

- Large silicon nodules occupied up to at least 65 percent[2] of the metal 1 line widths and 100 percent of the metal thickness. This will increase susceptibility to electromigration.

- Laser programming of metal 1 blasted holes into the silicon substrate. This was not passivated particularly well in some cases.

- Many of the polycide gates had "worm holes" beside the sidewall spacers. Reliability effects are unknown but contaminants may be trapped in these locations.

Special Features:

- These devices are designed to provide very fast turnaround customized IC products, by laser patterning of photoresist to define metal 2 interconnect and direct laser vaporization of metal 1 "programmable links" (fuses). A highly unusual appearance (but not necessarily unreliable structure) results.

- Metal 2 was chemically etched (very roughly) for personalization purposes.

- Metal 1 links were laser blown for the same purposes.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- 160-pin Plastic Quad Flat Pack (PQFP) with gull wing leads for surface mount applications.
- Leadframe and header/paddle constructed of copper (Cu). A dimpled header was employed for additional package strength.
- Kapton tape was employed to stabilize the leadframe leads.
- Externally leads were plated with tin-lead (SnPb) and internally spot plated with silver (Ag).
- A silver-epoxy die attach was employed.
- Die did not employ a backside plating.
- A patterned polyimide die coat was employed.
- Thermosonic wirebonding using 1.3 mil O.D. gold wire.
- Wafer dicing was by sawing (full depth).

Die Process and Design

- Fabrication process: Selective oxidation CMOS process employing twin wells in a P substrate. No epi was used.
- Final passivation: A single layer of silicon-nitride, (under the polyimide die coat).
- Metallization: Two quite different levels of aluminum. Whereas metal 2 used no cap metal, had apparent normal to light level silicon doping, and a very thin titanium adhesion layer, metal 1 used both tungsten cap and barrier and appeared significantly over-doped with silicon.

TECHNOLOGY DESCRIPTION (continued)

- Both metal layers were patterned into standard (pre-customizing) interconnect design using dry etching. Metal 2 was then apparently patterned into its custom design using (laser exposed?) photoresist and a dry etch. Metal 1 was customized by laser vaporization of selected program sites.

- Interlevel dielectric: Two layers of deposited glass; the second of which may have been a spin-on-glass (SOG) for planarization purposes.

- Pre-metal dielectric: A layer of deposited glass over a layer of BPSG reflow glass over densified oxide. The reflow glass was reflowed prior to contact cuts only.

- Polysilicon: A single layer of silicided polysilicon (poly and tungsten silicide) was used to form all gates on the die.

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place.

- Wells: Twin wells in a P substrate. No epi was present.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 8**

Questionable Items:[1] None.

General Items:

- The devices were encapsulated in a 160-pin Plastic Quad Flat Packs (PQFP) with gull wing leads for surface mount applications.

- Overall package quality: Good. No defects were found on the external portions of the package. External pins were well formed and tinning of the leads was complete.

- One package was subjected to a dye penetrant test which revealed that no gaps were present at lead exits.

- Leadframe: Copper (Cu) leadframe externally tinned with tin-lead (SnPb) solder and spot plated internally with silver (Ag). A dimpled header/paddle was employed for additional package strength. No problems were found.

- Kapton tape was employed on the internal leadframe to help stabilize the lead spacing.

- Die attach: A patterned silver-epoxy die attach was used. Minor voids were noted; however, they are not severe enough to be a reliability concern.

- Die backside plating was not employed.

- Die dicing: Die separation was by sawing (full depth) with normal quality and workmanship.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS I (continued)

- Wirebonding: Thermosonic ball bond method using 1.3 mil O.D. gold wire. Wirebond placement was good. Wire clearance and spacing were normal. Bond pull strengths were good (see page 11) and no bond lifts occurred. All pins were connected.

- A thin patterned polyimide die coat was employed.

ANALYSIS RESULTS II

Die Process and Design: **Figures 9 - 41**

Questionable Items:[1]

- Large silicon nodules occupied up to at least 65 percent[2] of the metal line widths and 100 percent of the metal thickness. This will cause increased susceptibility to metal migration and possible early failure. It is of particular concern at metal steps into contacts where metal thins as well.

- Laser programming of metal 1 blasted holes into the silicon substrate. This was not passivated really well in some cases.

- Many of the polycide gates had "worm holes" beside the sidewall spacers. Contaminants may be trapped in these.

Special Features:

- These devices are designed to provide very fast turnaround customized IC products, by laser patterning of photoresist to define metal 2 interconnect and direct laser blowing of metal 1 "programmable links." A highly unusual appearance (but not necessarily unreliable structure) results.

- Metal 2 was chemically etched (very roughly) for personalization purposes.

- Metal 1 links were laser blown for the same purposes.

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate. No epi was present. Basic process implementation appeared to be of good quality except for metal 1 composition and "worm hole" formation at gate edges.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2]*Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Design implementation: Die layout was clean. Alignment was good at all levels.

- Surface defects: No toolmarks, masking defects, or contamination areas were found.

- Final passivation: A single layer of silicon-nitride was employed. Passivation integrity tests indicated defect-free passivation. Edge seal was also good. Passivation quality is especially important since it must also seal the laser programmed metal 1 links and this process creates holes that penetrate into the silicon substrate.

- Metallization: Two layers of silicon-doped aluminum. Only metal 1 employed a tungsten cap and barrier. Metal 2 used a very thin adhesion layer of titanium.

- Metal design: Both metal layers employed slotted bus lines for stress relief. Apparently a standard interconnect pattern (masterslice type design) using normal photolithography and dry etch techniques is employed for the basic die design. No problems were found in this area.

- Custom metal patterning: Both metal layers were selectively patterned for personalization purposes prior to final passivation. As mentioned, apparently metal 2 is customized by direct laser exposure of photoresist followed by a dry etch. Although this leaves very rough looking metal edges there was no visible indication of any problems in this process step nor do we foresee any potential cause for concern. Metal 1 is also customized, either before or after metal 2 patterning. It is programmed by direct laser blowing of specific sites where interlevel dielectric and metal 1 cap layer have been removed. A laser pulse is used to vaporize this metal and in almost all cases the laser power used is enough to also vaporize the pre-metal dielectric and substrate silicon (to a depth of 0.3 micron). It is presumed that the apparent excessive power is required to ensure clearing of the tungsten barrier metal. The holes created due to this are of some concern because of their location in some places (Figure 28) and because the nitride passivation does not always appear to seal these areas as well as might be desirable, leaving visible knit lines (Figure 23).

ANALYSIS RESULTS II (continued)

- Metal defects: No notching or voiding was found but metal 1 silicon nodules occupied up to 100 percent of the line thickness and up to at least 65 percent of the line widths (Figure 24). Silicon nodules >50 percent of the line widths can cause an unacceptable increase in the aluminum's susceptibility to electromigration, but this is entirely dependent on the die design.

- Metal step coverage: Metal 2 aluminum thinned up to 50 percent at some vias (Figure 16). Total metal 1 thinning was up to 75 percent, while metal 1 aluminum thinning up to 80 percent occurred at some contacts (Figure 25). The concern that exists is for the combined effect of the thinning and silicon nodule density. For reference MIL-STD-883D allows up to 70 percent metal thinning for vias and contacts of this size.

- Contact etch: No overetching of contacts were noted. No problems are foreseen.

- Interlevel dielectric: Two layers of deposited glass; the second of which may have been a spin-on-glass (SOG) for planarization purposes. No problems were found.

- Pre-metal dielectric: A layer of deposited glass over a layer of BPSG reflow glass over densified oxide. The reflow glass was reflowed prior to contact cuts only. Here also no problems were found.

- Polysilicon: The single layer of silicided polysilicon (poly and tungsten silicide) was used to form all gates on the die. Definition was good and no problems were found in this area.

- Sidewall spacers: Oxide sidewall spacers were used (and left in place) to provide the LDD spacing. The reflow glass deposited after S/D implant did not fill the corners left by the outside edges of the spacers. There is some concern that this was caused by inadequate cleaning prior to reflow glass deposition, or poor glass/deposition controls. The effects on product performance or reliability are unknown.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was present in the local oxide at the well boundaries indicating the presence of a twin-well process.

ANALYSIS RESULTS II (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of MOS transistors. No anomalies were found.

- Wells: Twin-wells were used in a P substrate. The P-wells could not be delineated; however, the step in the local oxide at the well boundary indicates a twin-well process. No problems were found.

- Buried contacts: Direct poly-to-diffusion contacts were not employed.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Dye penetrant test

Decapsulation

Internal optical inspection

SEM of assembly features

Wirepull test

Passivation integrity test

Passivation removal and inspect metal 2

Aluminum 2 removal and inspect

Delayer to metal 1 and inspect

Aluminum 1 removal and inspect

Delayer to poly/substrate and inspect

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

PACKAGE MARKINGS

TOP

CONFIDENTIAL CLIENT ID AND
"M022477-23, 24
9621 USA"

WIREBOND STRENGTH

Wire material:	1.3 mil diameter gold
Die pad material:	aluminum
Material at package post:	silver

Sample #

# of wires tested:	40
Bond lifts:	0
Force to break - high:	12.0g
- low:	7.0g
- avg.:	9.8g
- std. dev.:	1.5

CONTACT MATRIX

	Metal 2	**Metal 1**	**Polycide**	**N+**	**P+**
Metal 2:		X			
Metal 1:	X		X	X	X
Polycide:		X			

Note: *X = direct connection.*

DIE MATERIALS

Passivation:	Silicon-nitride.
Metal 2 - aluminum:	Aluminum doped with silicon (no copper was detected).*
- adhesion layer:	Titanium.
Metal 1 - cap:	Tungsten.
- aluminum:	Aluminum doped with silicon (no copper was detected).*
- barrier:	Tungsten.
Reflow glass:	Borophosphosilicate glass (BPSG) containing 3.0 wt. percent boron and 5.0 wt. percent phosphorus.
Polycide:	Tungsten (W) silicide.

**There is no known method for determining the exact amount of silicon or copper in the aluminum on a finished die.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal to Poor

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Lead conformity	G
Lead plating quality	G
Die placement	G
Die attach quality	N
Wire spacing	N
Wirebond placement	G
Wirebond quality	G
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.3 mil gold wire
Die attach method	Silver-filled epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	N
Process defects (absence)	N
General workmanship	N
Passivation integrity	N
Metal definition	N
Metal integrity	NP*
Metal registration	G
Contact coverage	G
Contact registration	G

**Large silicon nodules and thinning at steps (M1).*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

HORIZONTAL DIMENSIONS

Die size:	9.5 x 9.5 mm (375 x 375 mils)
Die area:	91 mm^2 (140,625 $mils^2$)
Min pad size:	0.10 x 0.12 mm (4.3 x 4.8 mils)
Min pad window:	0.10 x 0.10 mm (3.9 x 3.9 mils)
Min pad spacing:	5 microns
Min pad-to-metal:	10 microns
Min metal 2 width:	1.6 micron
Min metal 2 space:	0.9 micron
Metal 2 pitch:	3.3 microns
Min via:	1.3 micron (round)
Metal 2 etch pattern:	2.35 x 3.9 microns (oval)
Min metal 1 width:	0.9 micron
Min metal 1 space:	1.0 micron
Metal 1 pitch:	2.4 microns
Min contact:	1.0 micron (round)
Min contact-to-gate:	0.9 micron
Metal 1 cap removed at fuse:	1.5 micron
Metal 1 fuse window:	1.5 x 2.35 microns (oval)
Min polycide width:	0.75 micron
Min polycide space:	2.1 microns
Min gate length* - (N-channel):	0.8 micron
- (P-channel):	0.75 micron

**Physical gate length.*

VERTICAL DIMENSIONS

Die thickness:	0.6 mm (24 mils)

Layers

Die coat:	2.5 microns
Passivation:	0.8 micron
Metal 2:	1.0 micron
Metal 2 overetch depth:	0.2 micron
Interlevel glass:	0.7 micron (average)
Metal 1 - cap:	0.08 micron (approx.)
- aluminum:	0.4 micron
- barrier:	0.08 micron (approx.)
Holes created by M1 programming:	0.9 micron
Vaporized (by laser zap) substrate:	0.3 micron
Pre-metal glass:	0.6 micron (average)
Polycide - silicide:	0.2 micron
- poly:	0.15 micron
Local oxide:	0.4 micron
N+ S/D diffusion:	0.15 micron
P+ S/D diffusion:	0.15 micron
N- well:	4.5 microns
P- well:	Could not delineate

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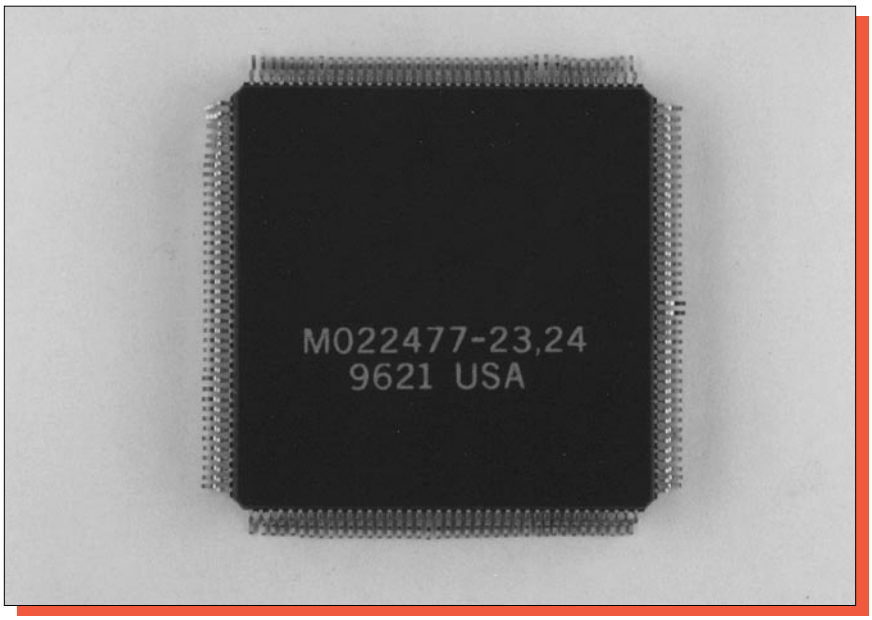


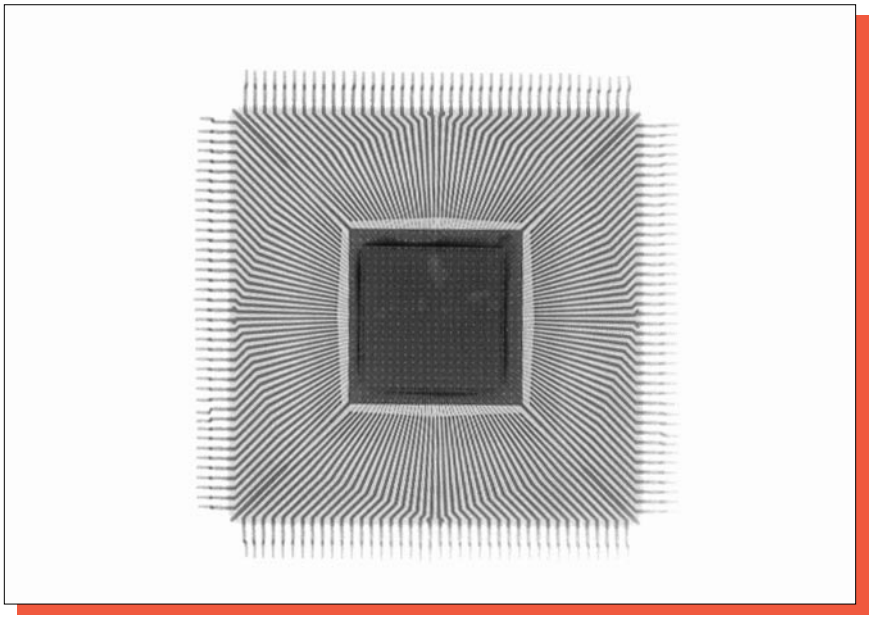


Figure 1. Package photograph and x-ray of the Otis Elevator AAA616QG1. Mag. 2x.

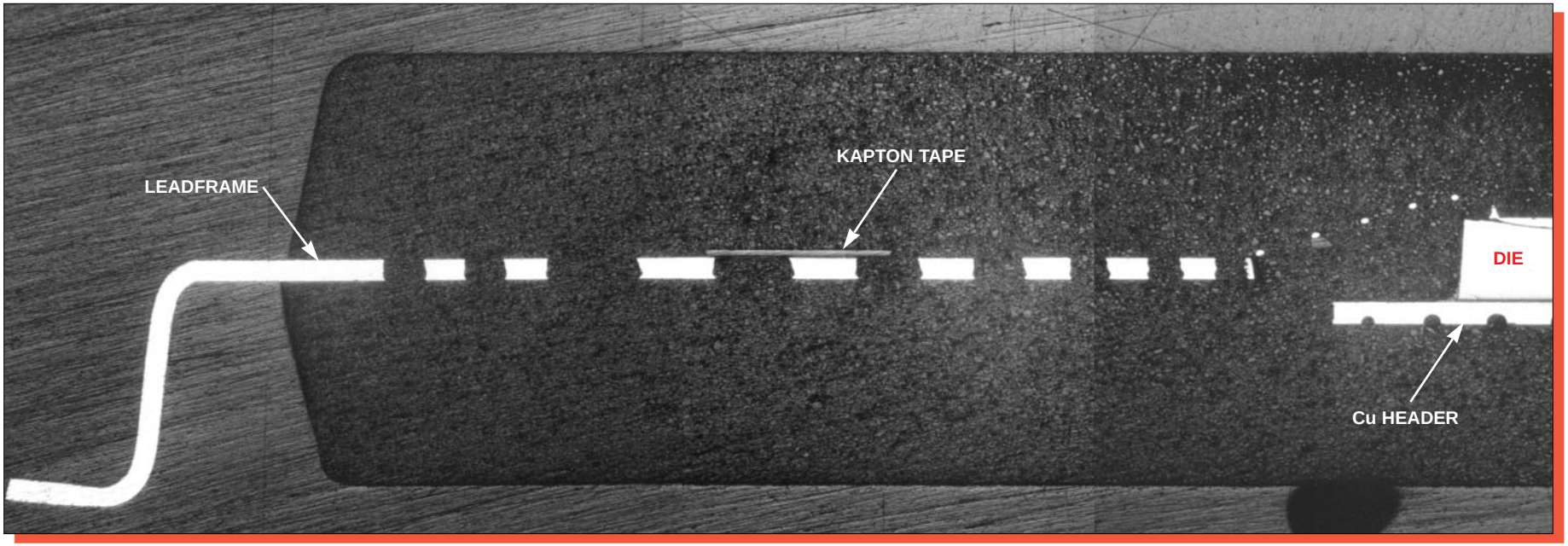
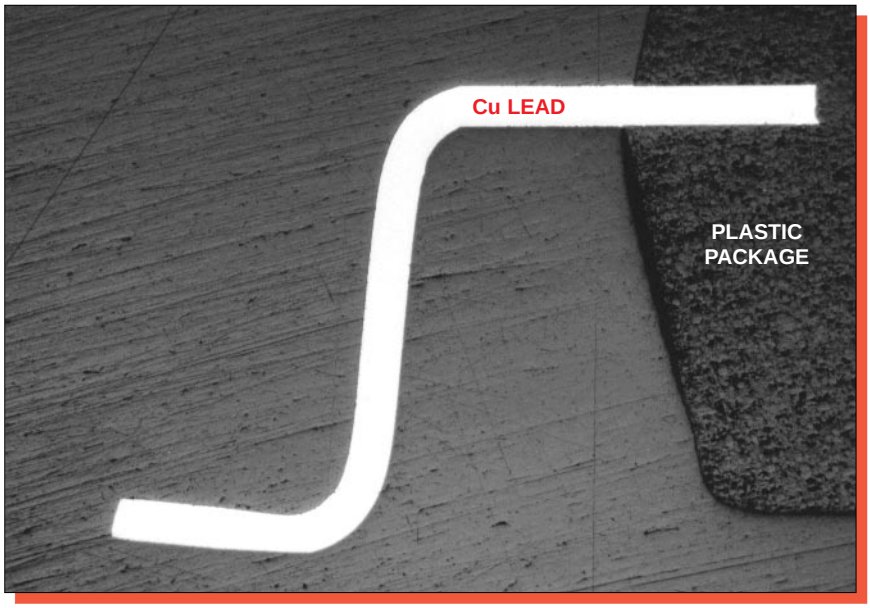
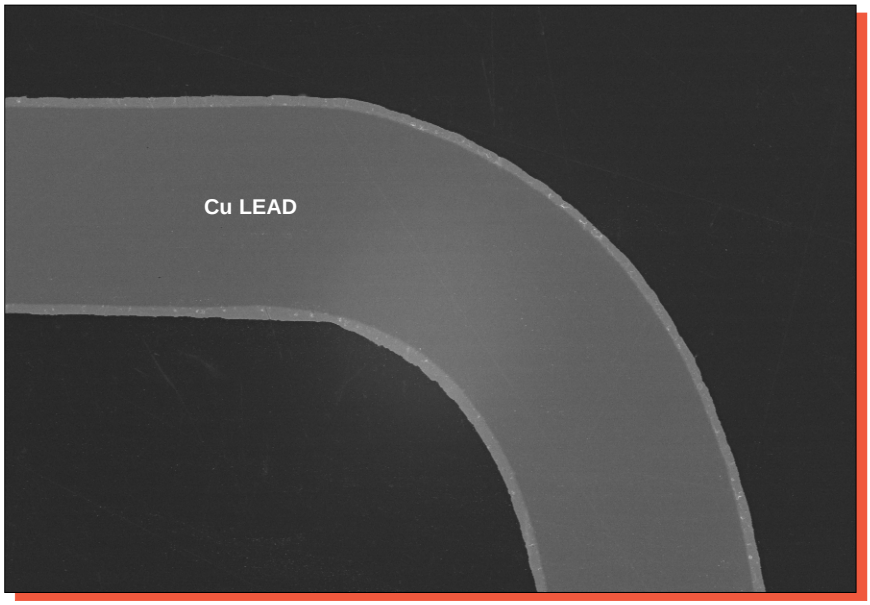


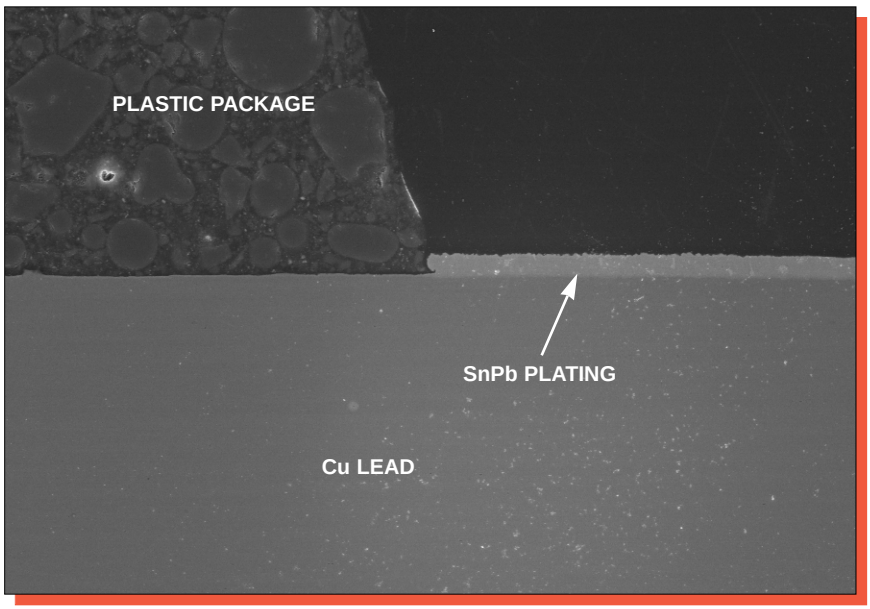
Figure 2. Portion of the package section illustrating general construction. Mag. 20x.



Mag. 30x

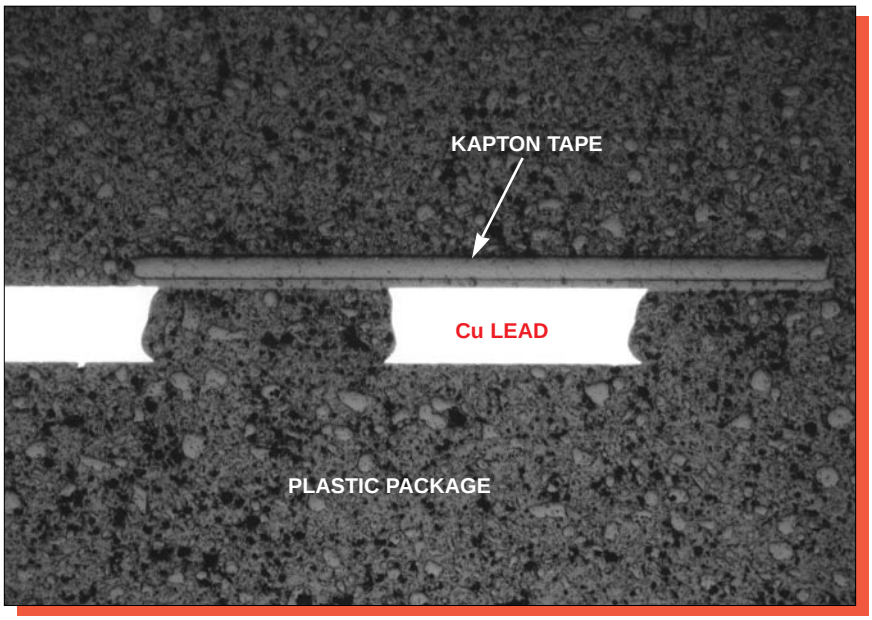


Mag. 180x

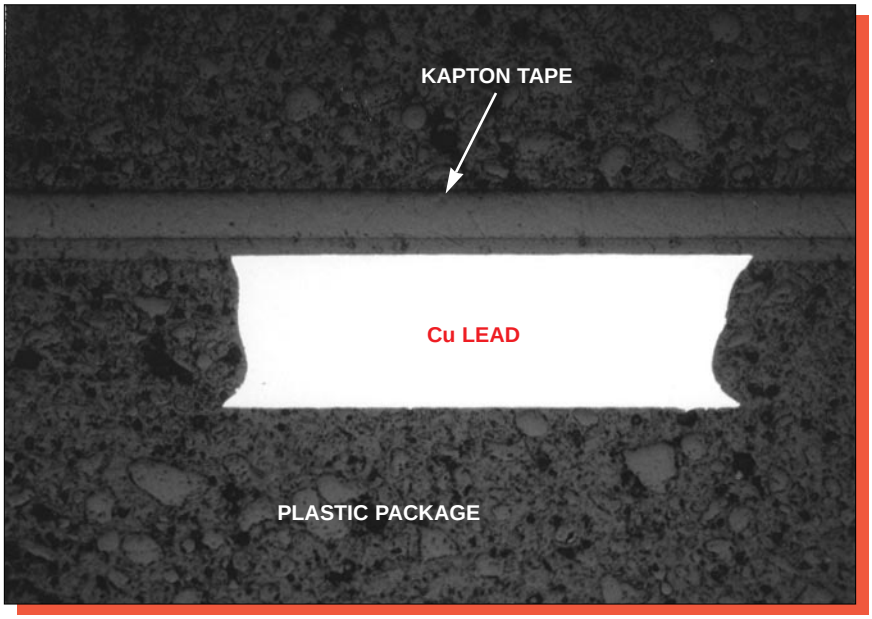


Mag. 360x

Figure 3. Package section views illustrating lead exit.



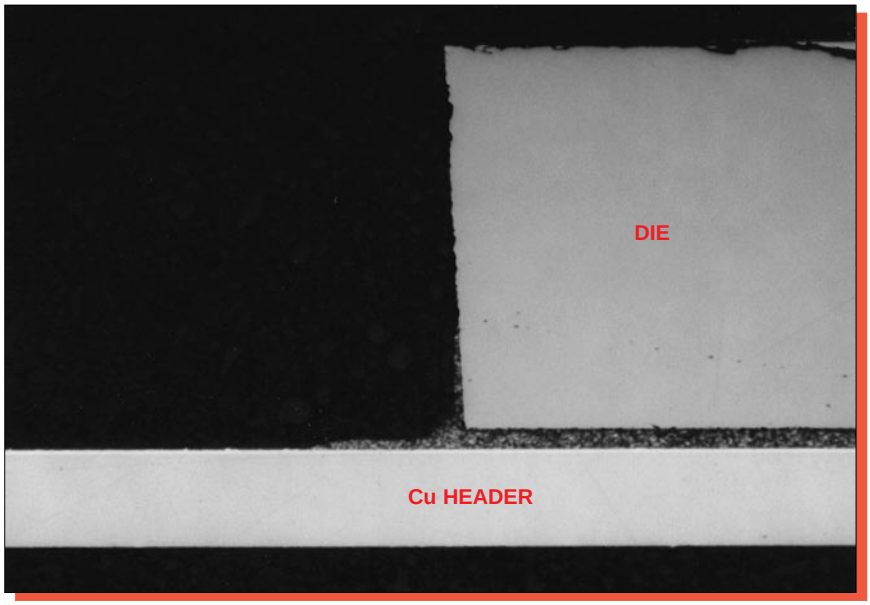
Mag. 65x



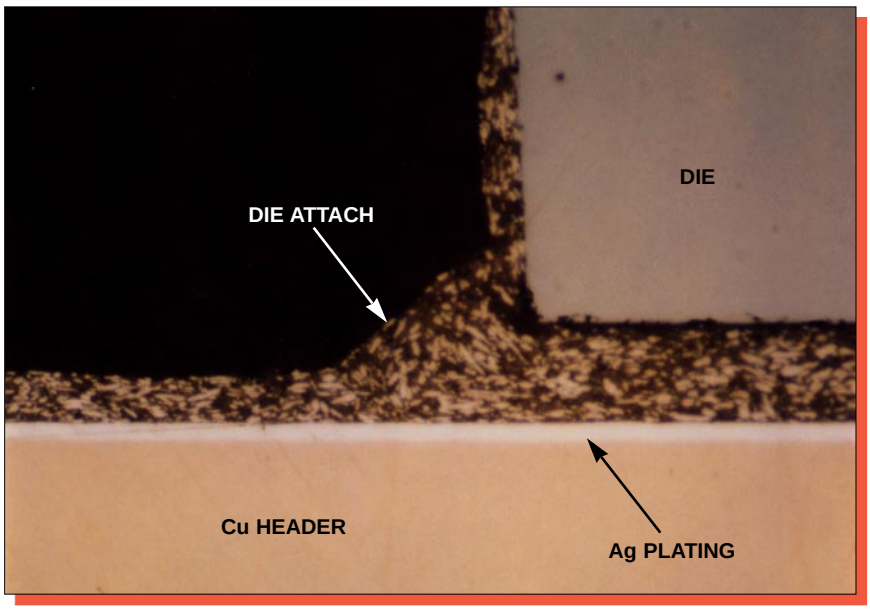
Mag. 130x

Figure 3a. Optical package section views illustrating Kapton tape.

Mag. 50x



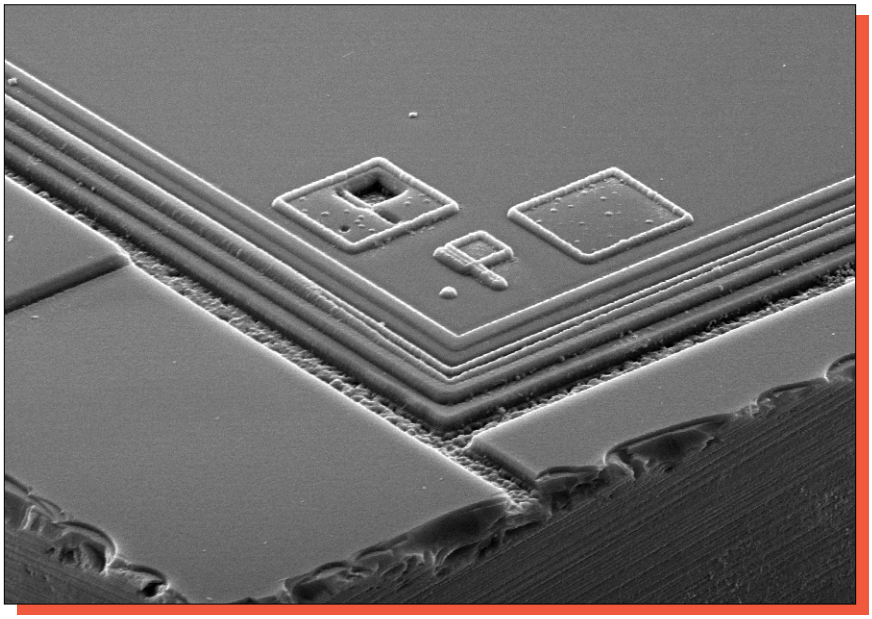
Mag. 80x



Mag. 400x

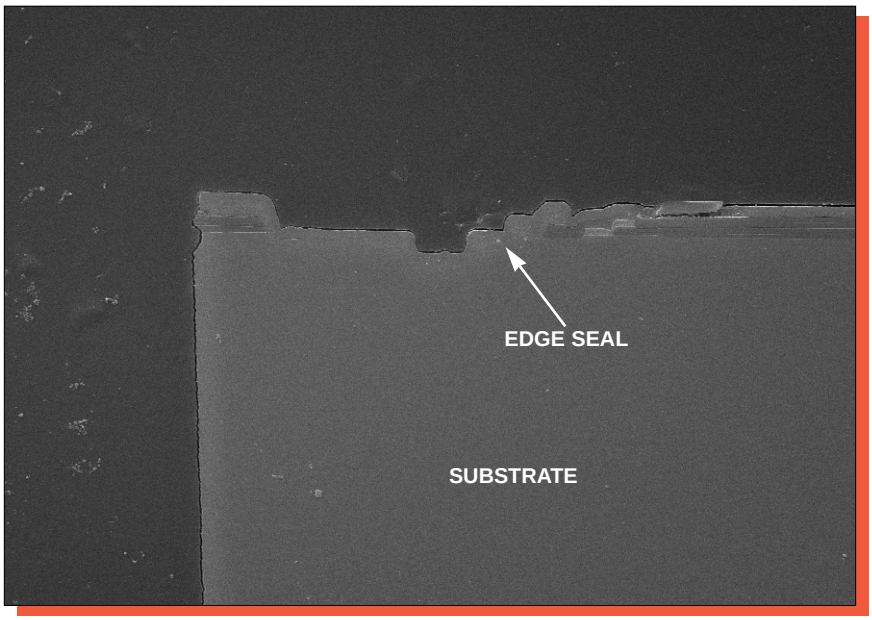
Figure 4. Optical package section views illustrating dicing and die attach.

Mag. 930x

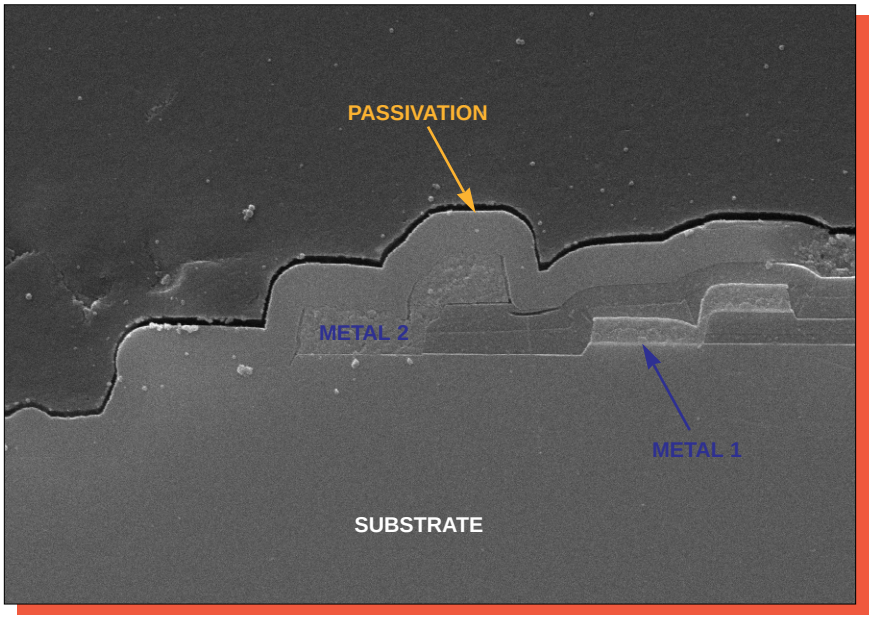


Mag. 1000x

Figure 5. SEM views illustrating die corner and edge seal.



Mag. 1600x



Mag. 6500x

Figure 6. SEM section views illustrating edge seal.

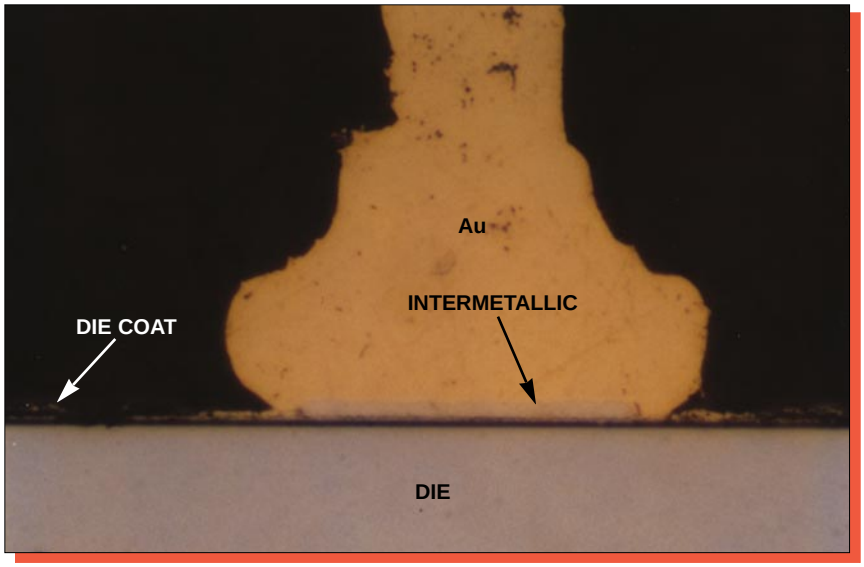
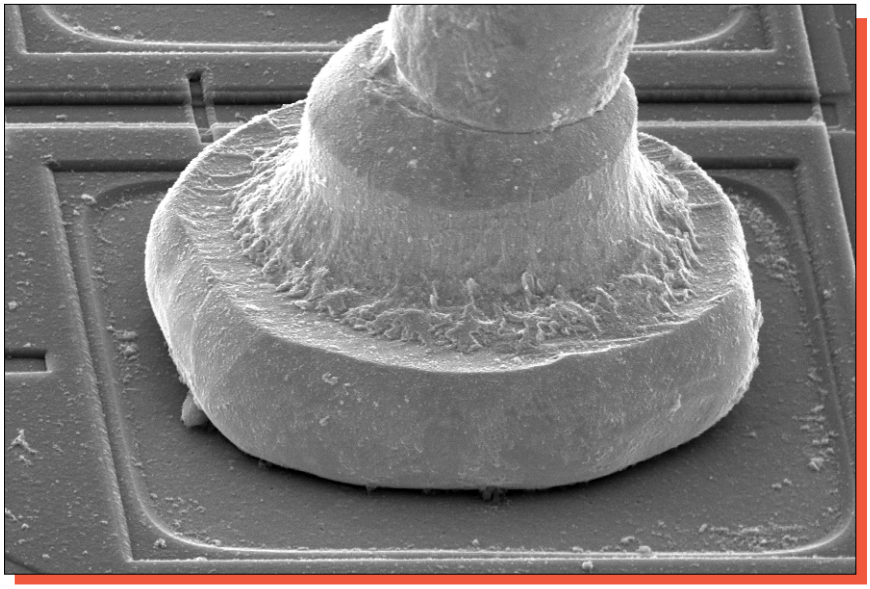
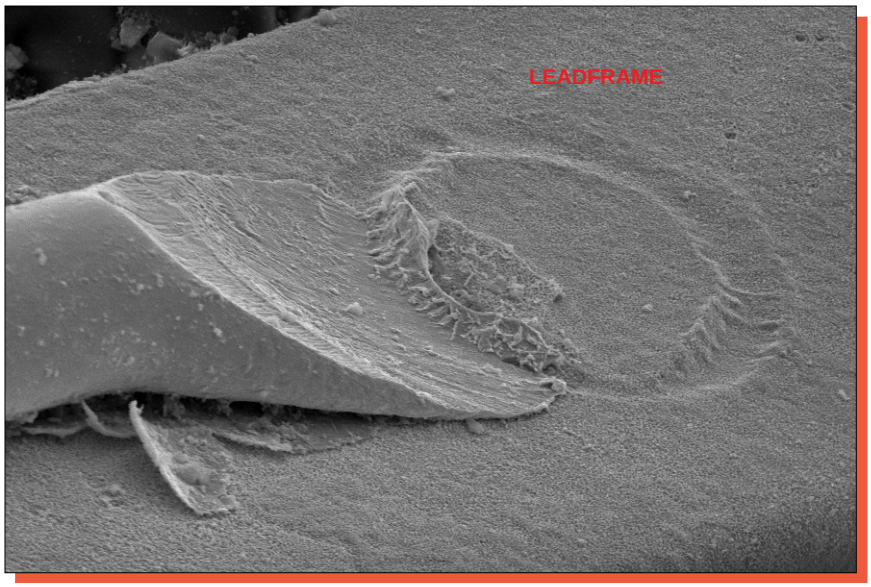


Figure 7. Optical section view illustrating a typical ball bond. Mag. 800x



Mag. 1000x



Mag. 800x

Figure 8. SEM views illustrating typical wirebonds.

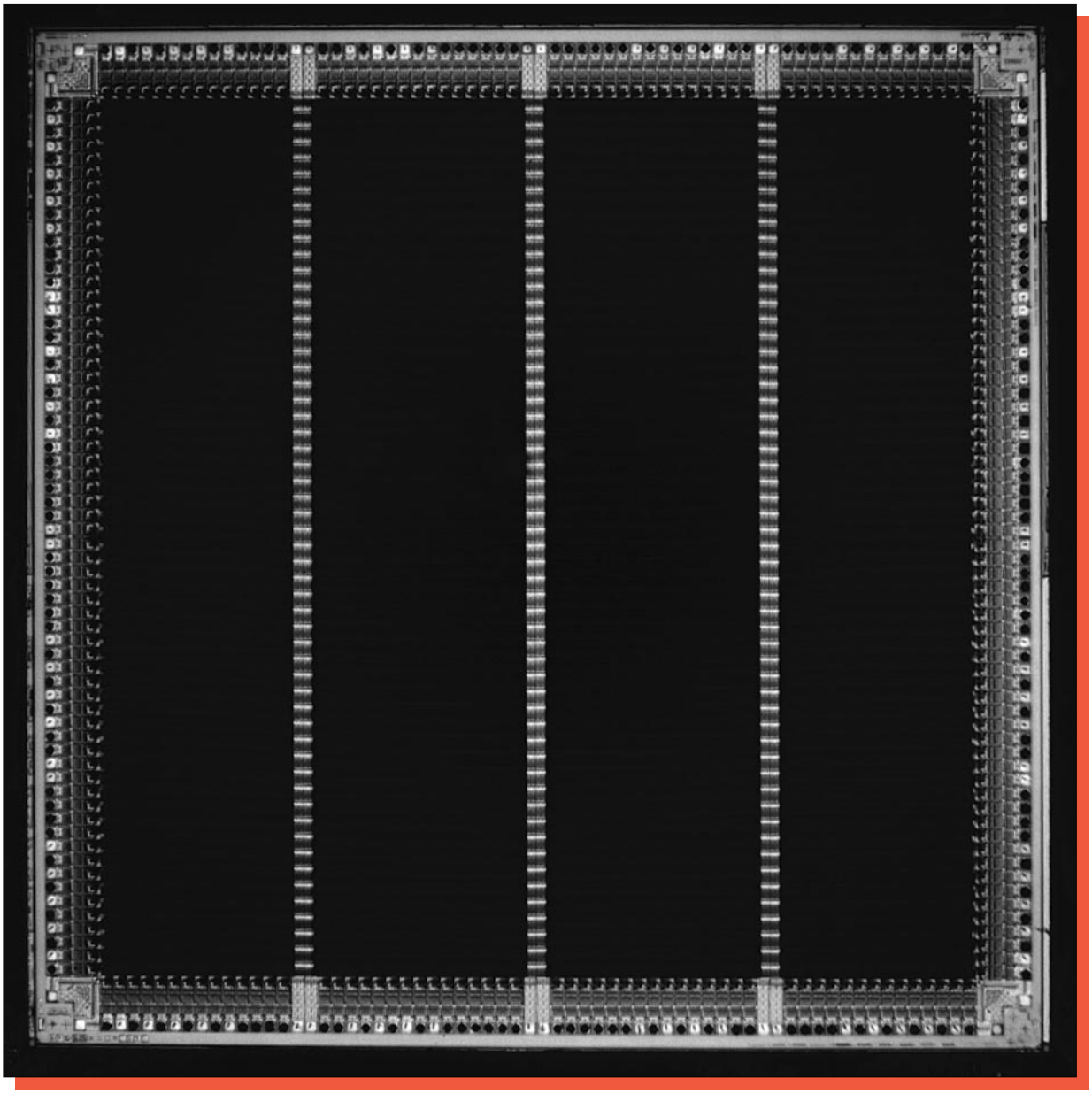
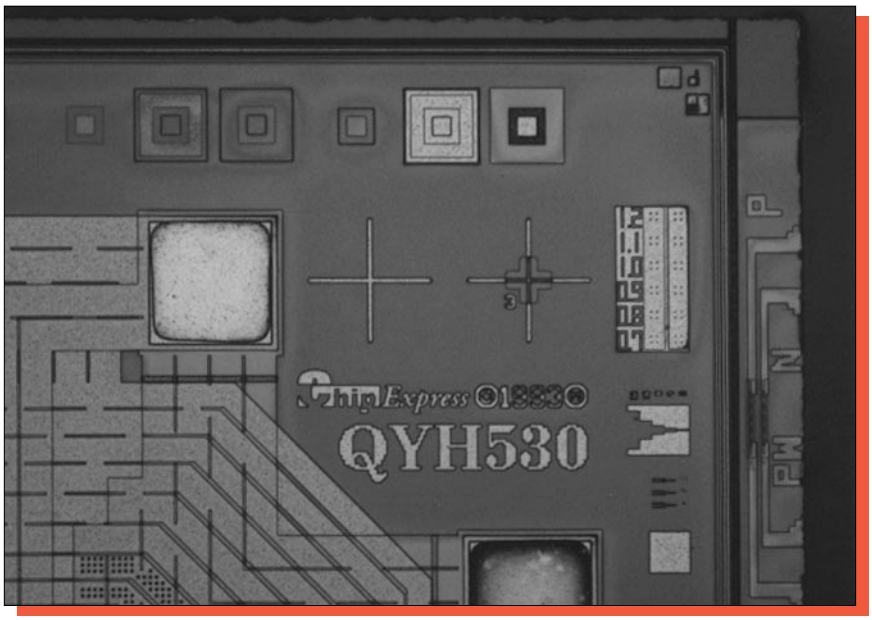
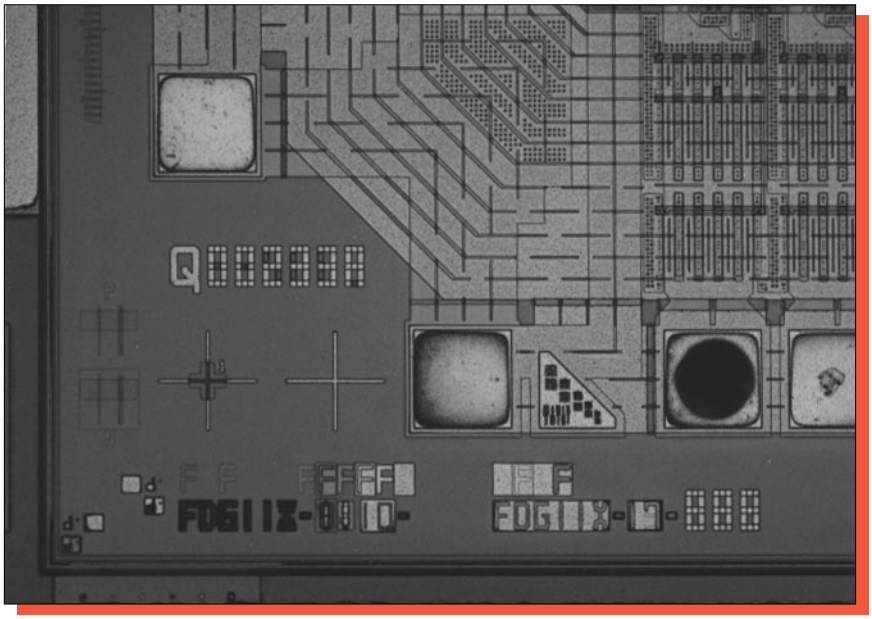


Figure 9. The Otis Elevator AAA616QG1 intact circuit die. Mag. 16x.

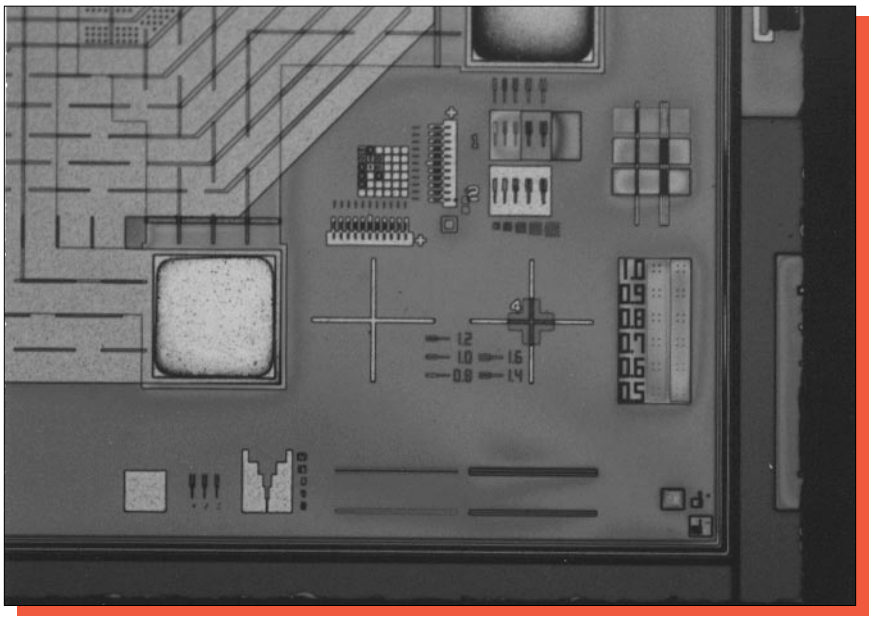


Mag. 160x



Mag. 130x

Figure 10. Optical views of die markings.



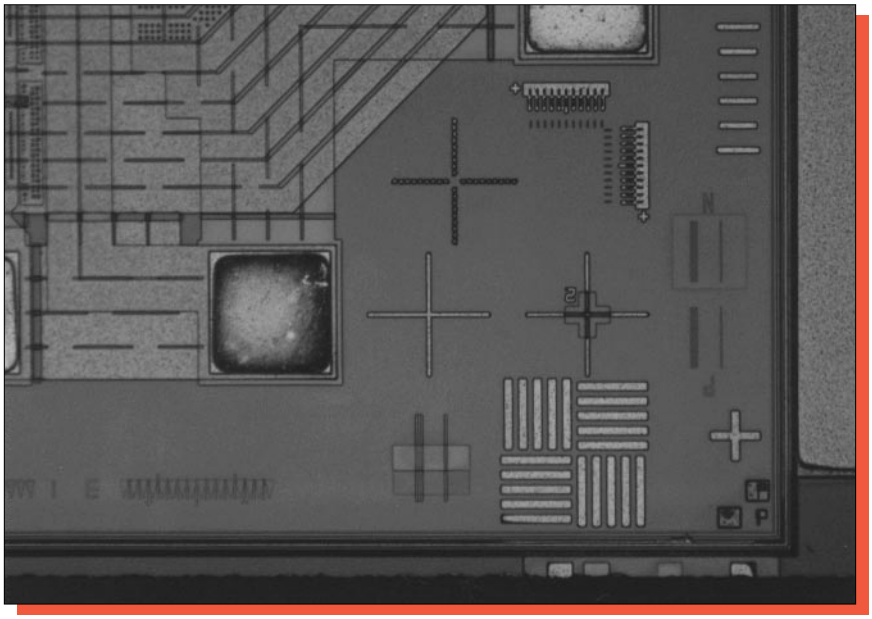
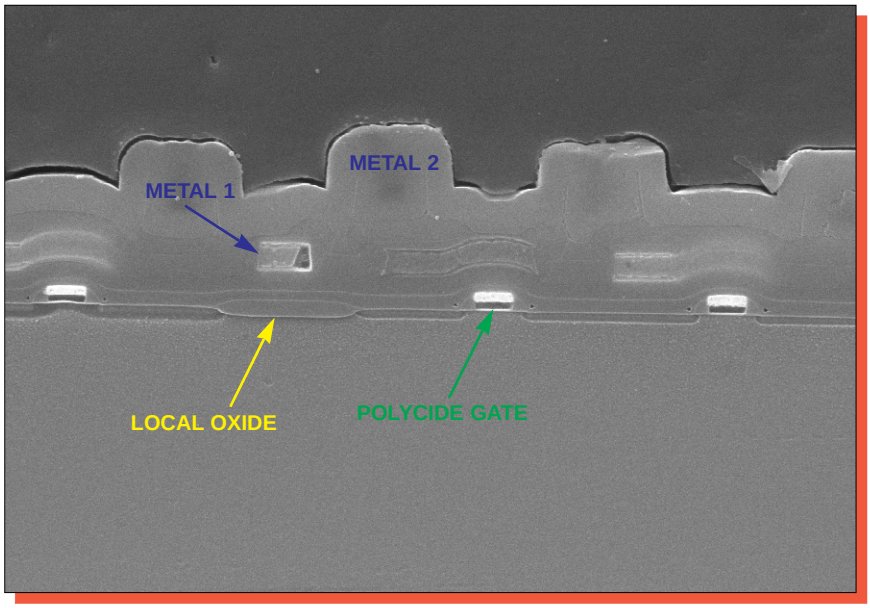
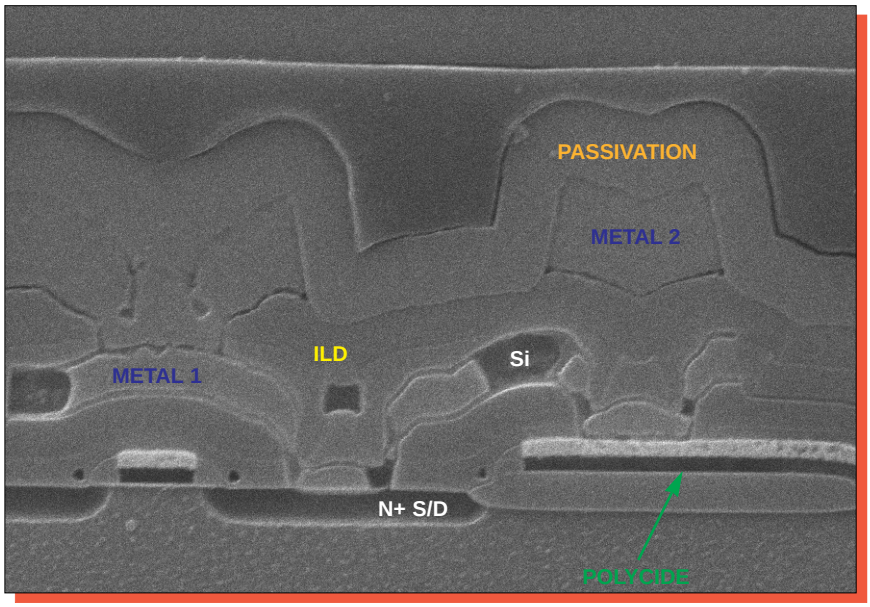


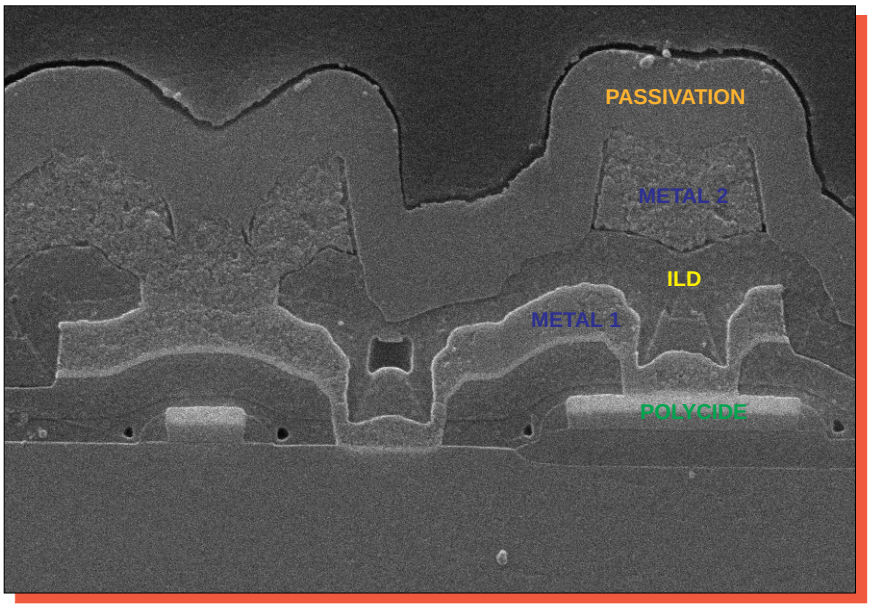
Figure 10a. Optical views of die markings. Mag. 160x.



Mag. 6500x

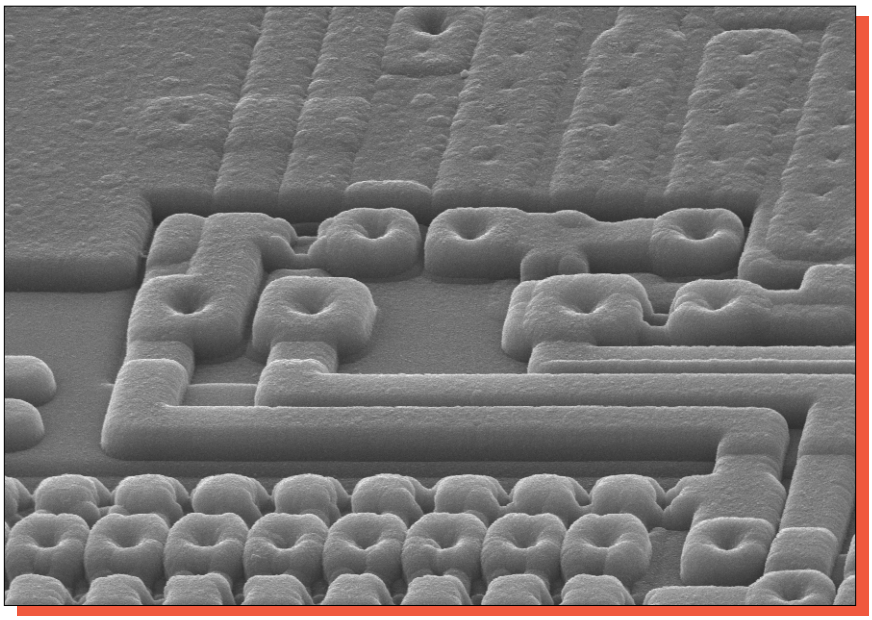


silicon etch,
Mag. 13,000x

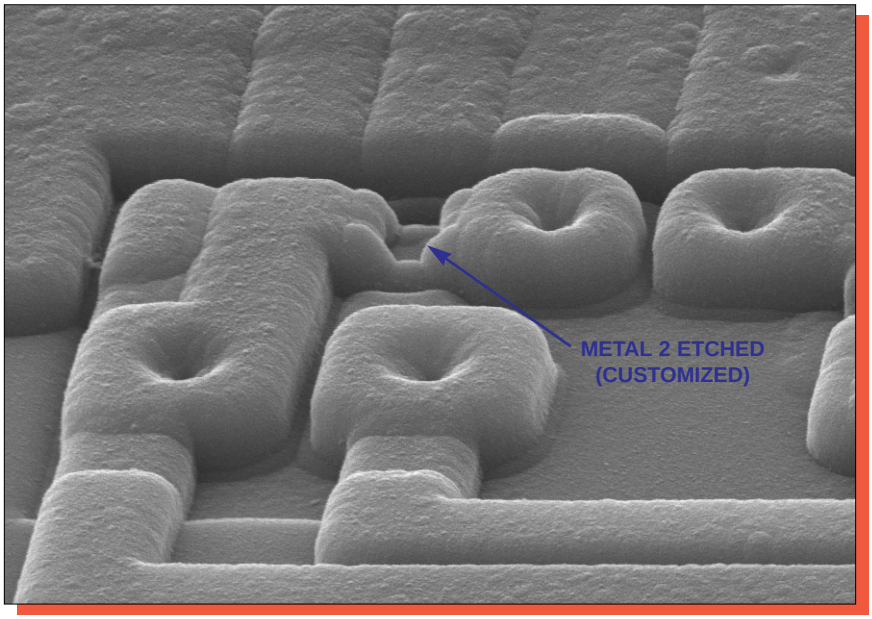


glass etch,
Mag. 13,000x

Figure 11. SEM section views illustrating general structure. Mag. 13,000x.

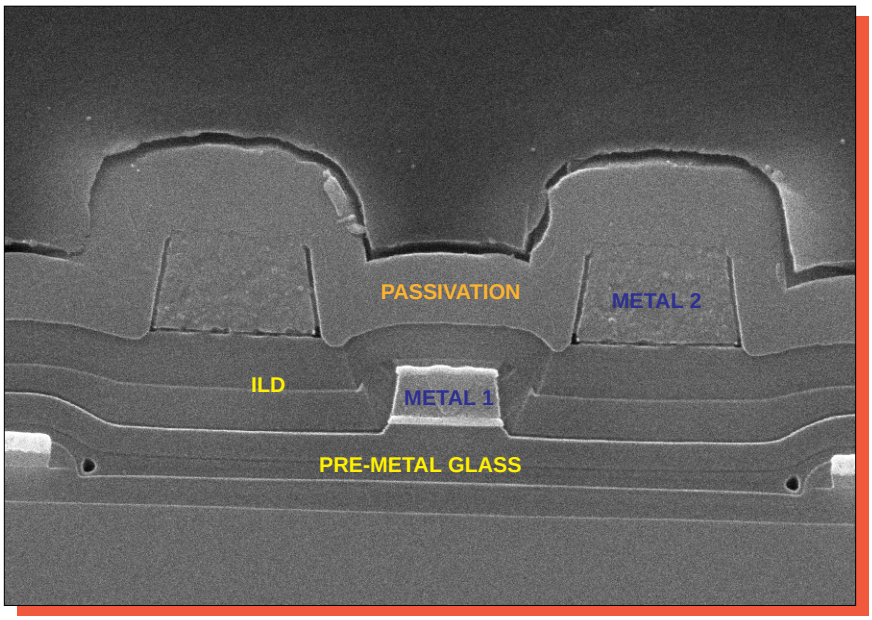


Mag. 3000x

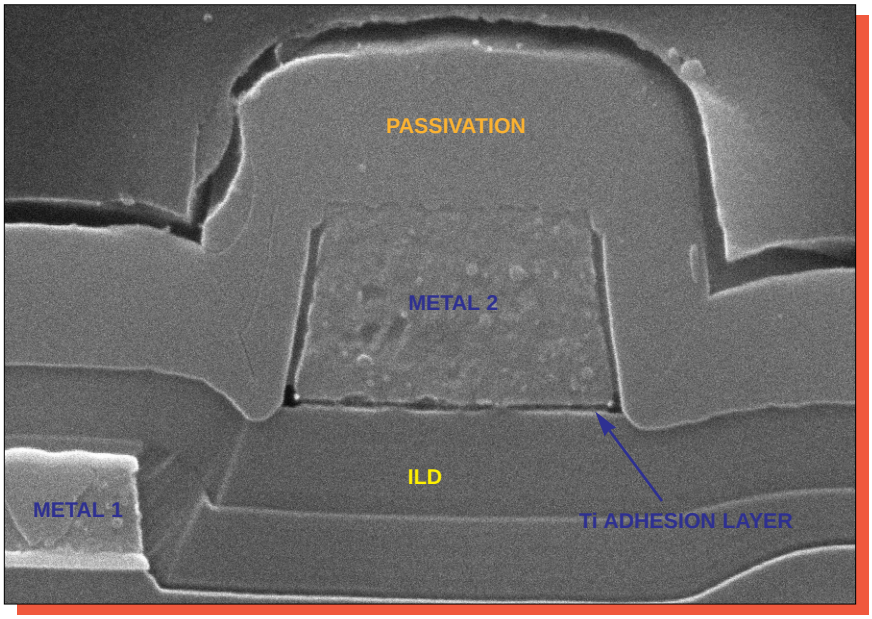


Mag. 6000x

Figure 12. SEM views illustrating passivation coverage. 60°.

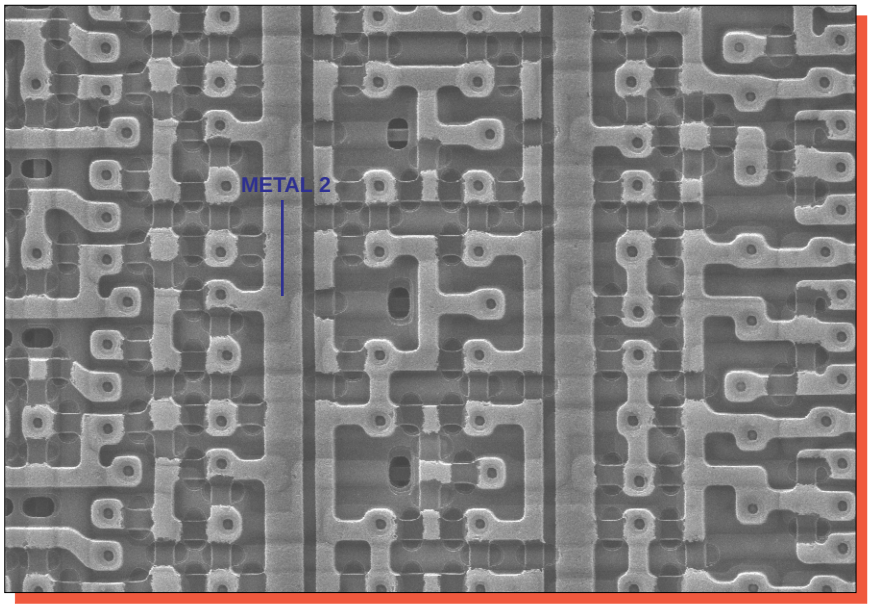


Mag. 13,000x

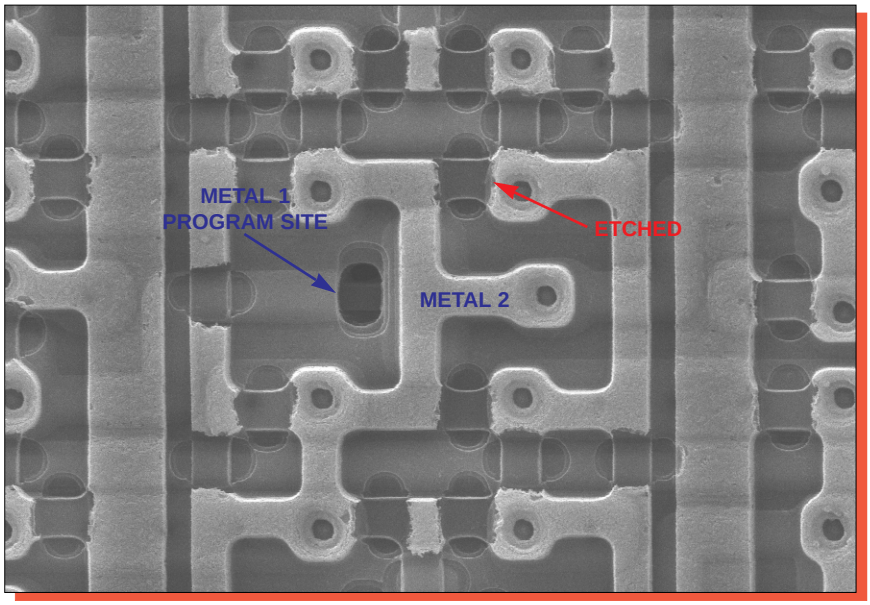


Mag. 26,000x

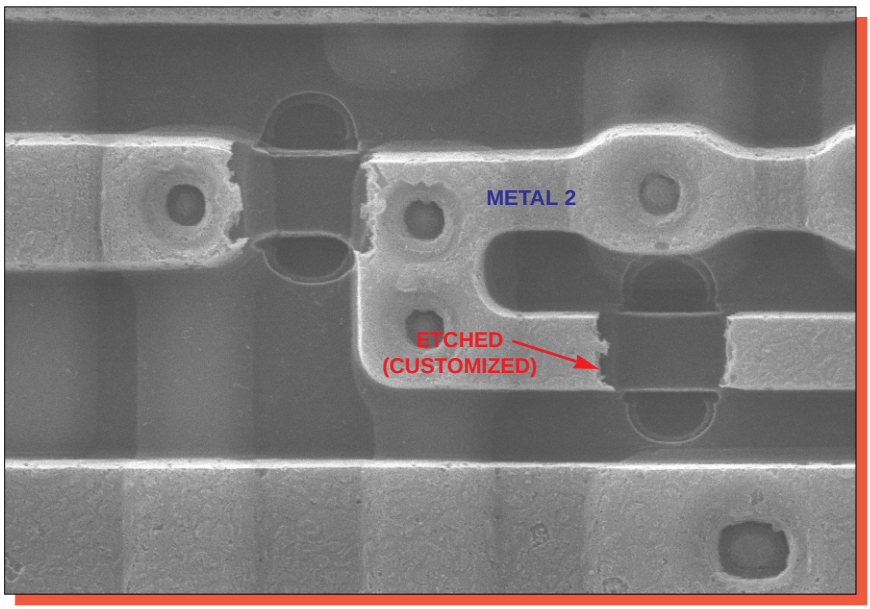
Figure 13. SEM section views illustrating metal 2 line profiles. Glass etch.



Mag. 1600x

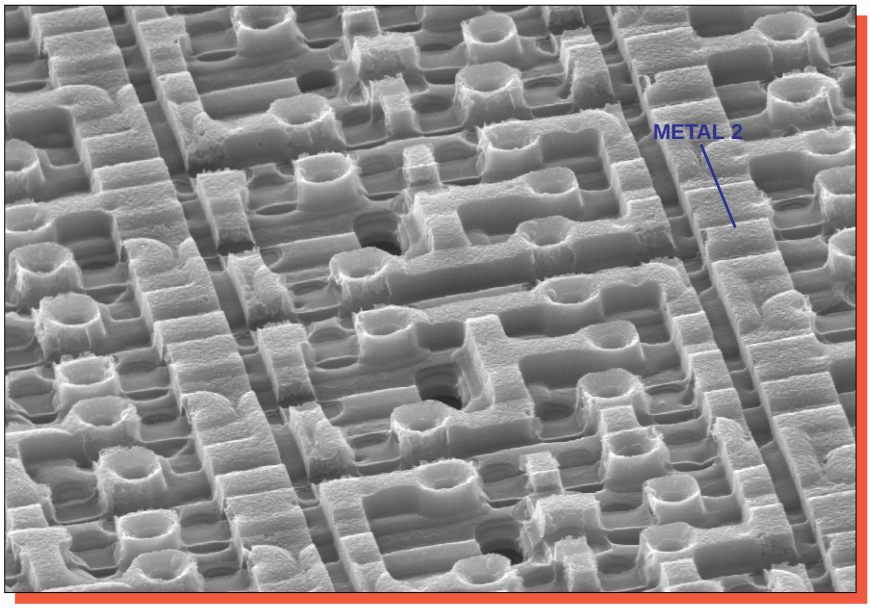


Mag. 3250x

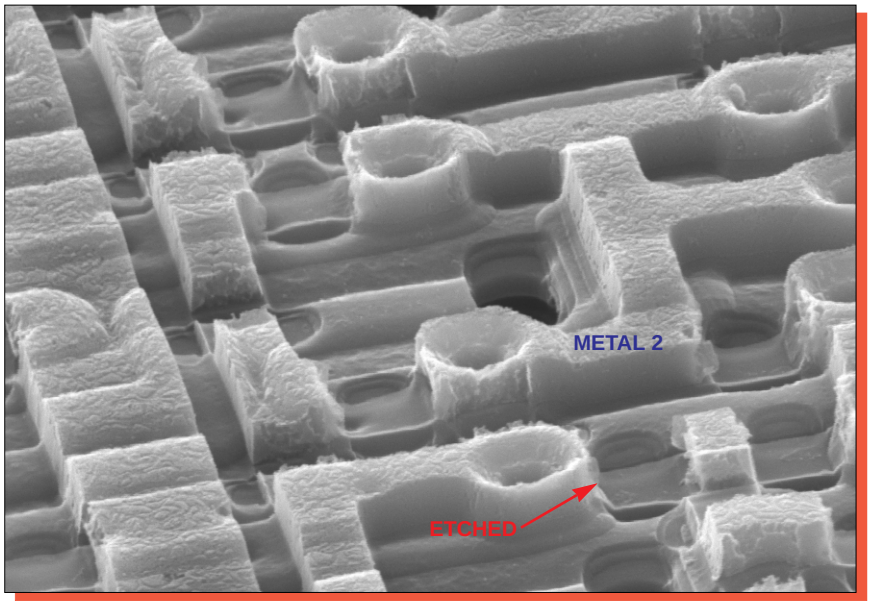


Mag. 6500x

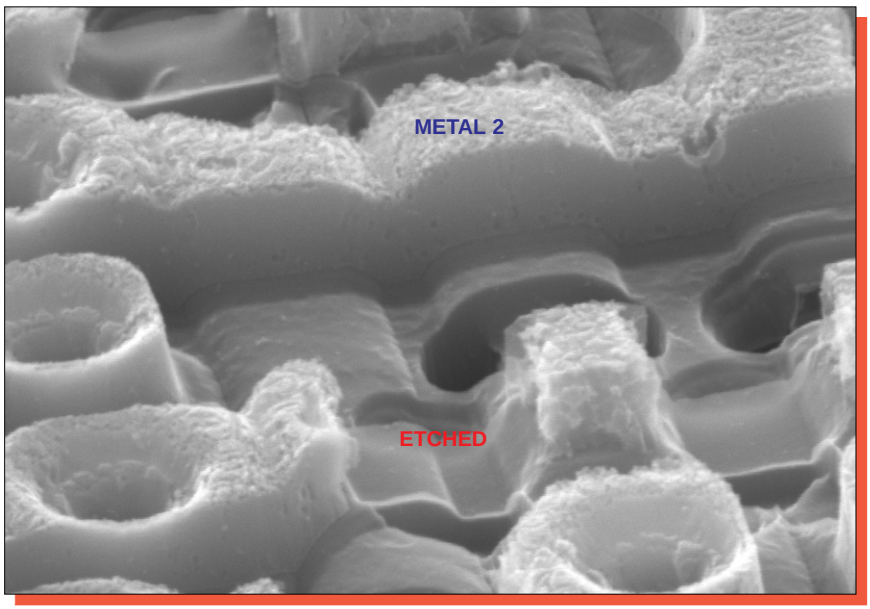
Figure 14. Topological SEM views illustrating metal 2 patterning. 0°.



Mag. 3000x

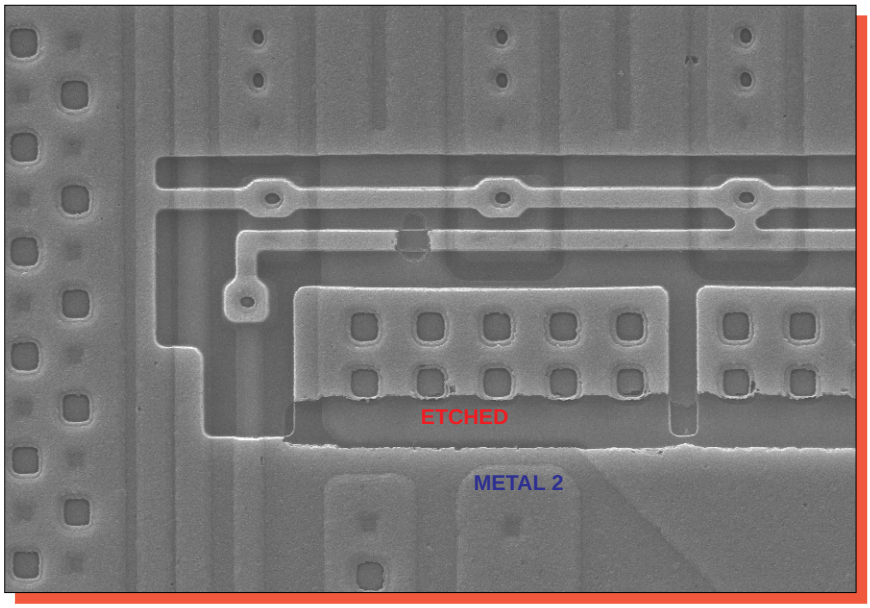


Mag. 6000x

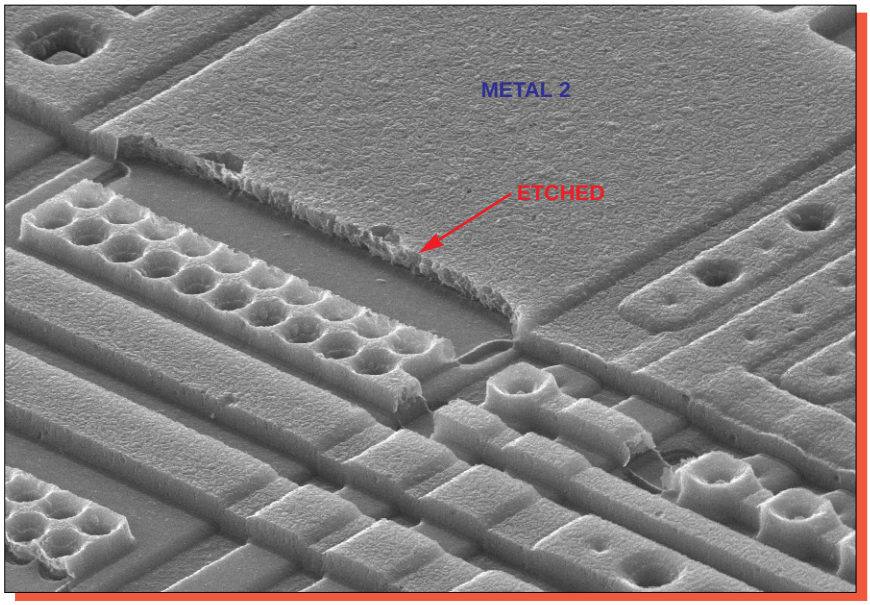


Mag. 12,000x

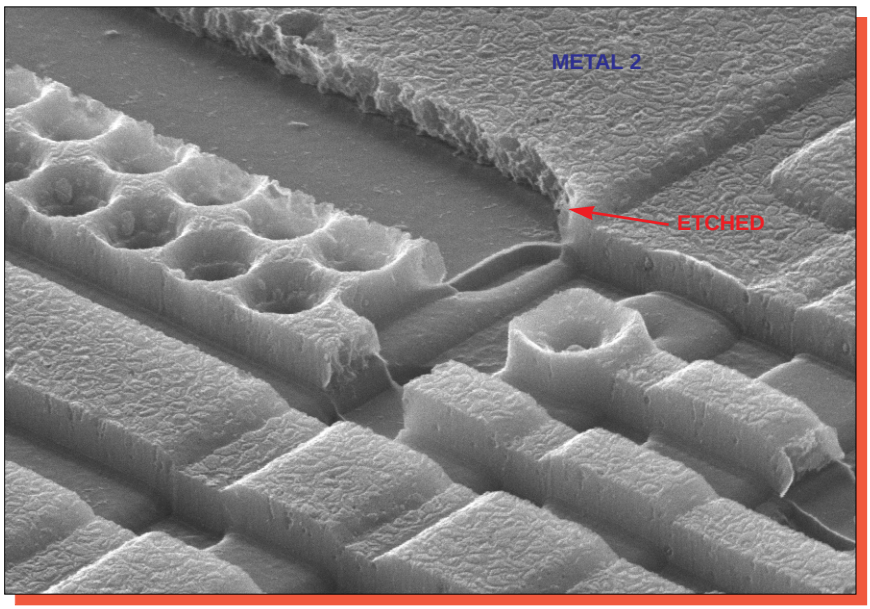
Figure 15. SEM views of metal 2 step coverage. 60°.



Mag. 1600x, 0°

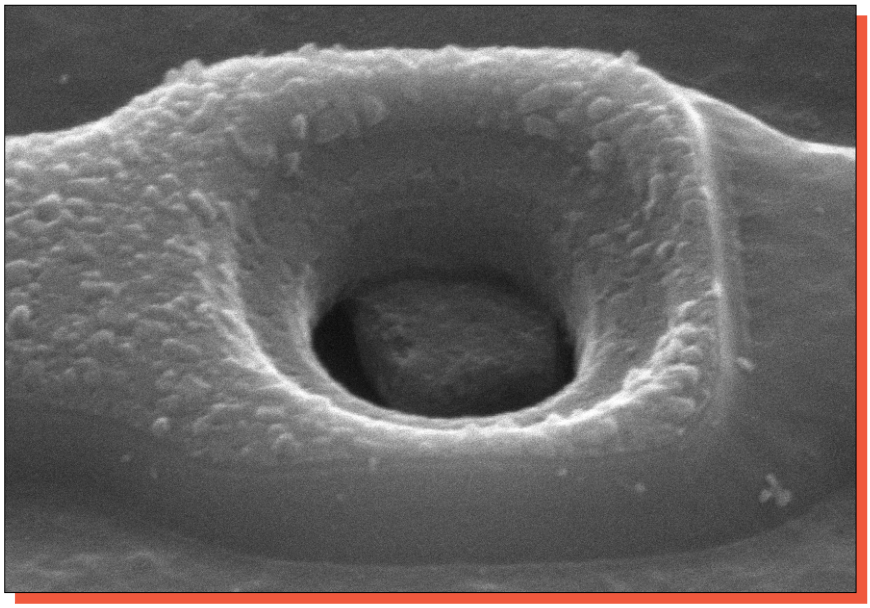


Mag. 3000x, 60°

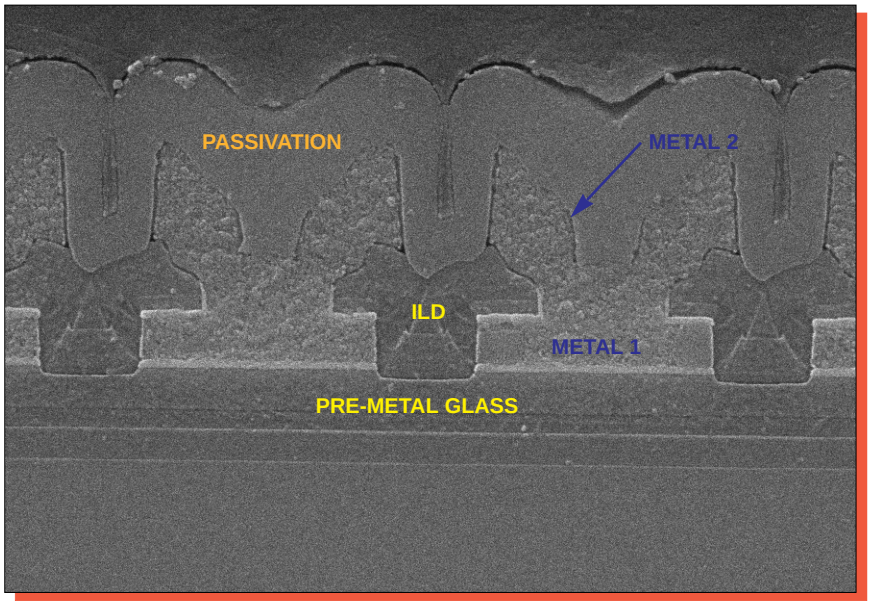


Mag. 6000x, 60°

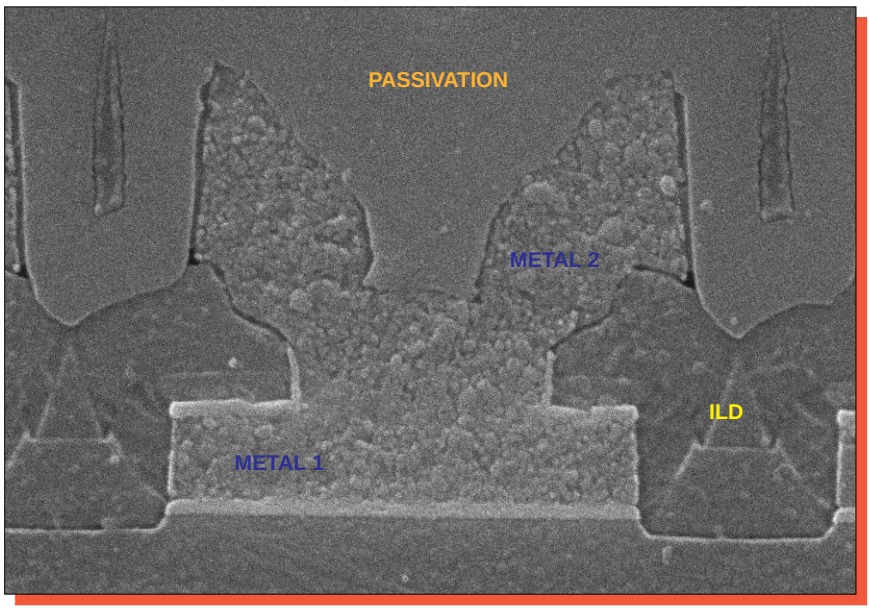
Figure 15a. SEM views illustrating metal 2 patterning in periphery.



aluminum removed,
Mag. 30,000x, 45°

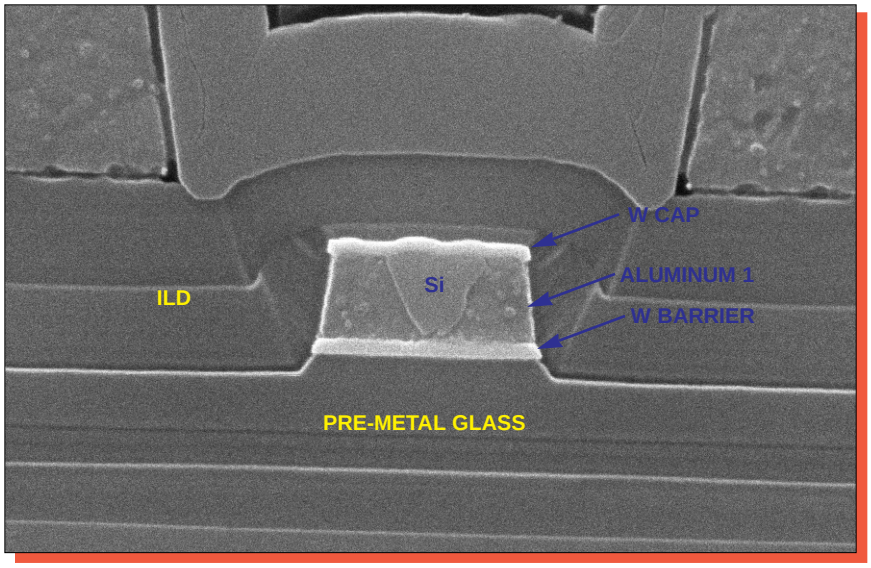


glass etch,
Mag. 13,000x

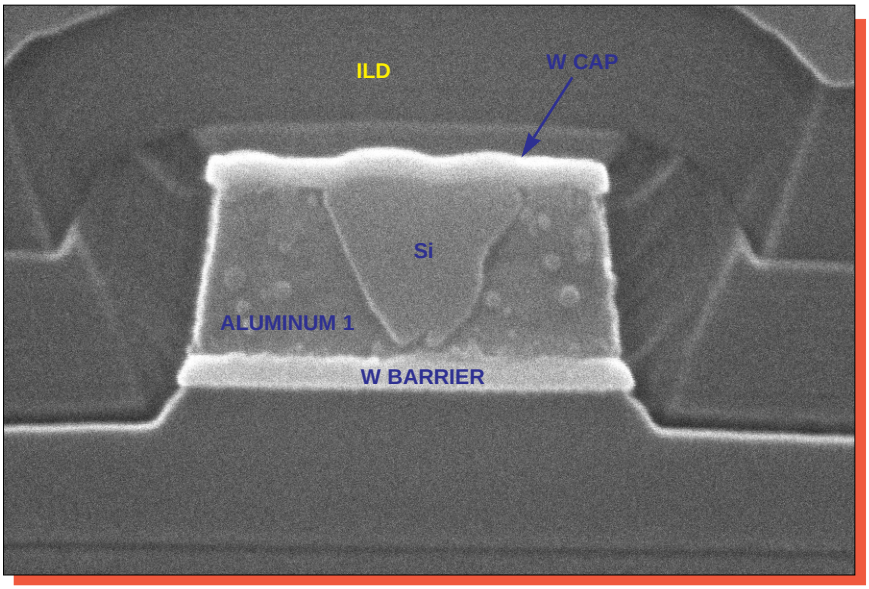


glass etch,
Mag. 26,000x

Figure 16. SEM views illustrating metal 2-to-metal 1 vias.



Mag. 26,000x



Mag. 52,000x

Figure 17. SEM section views illustrating metal 1 line profile. Glass etch.

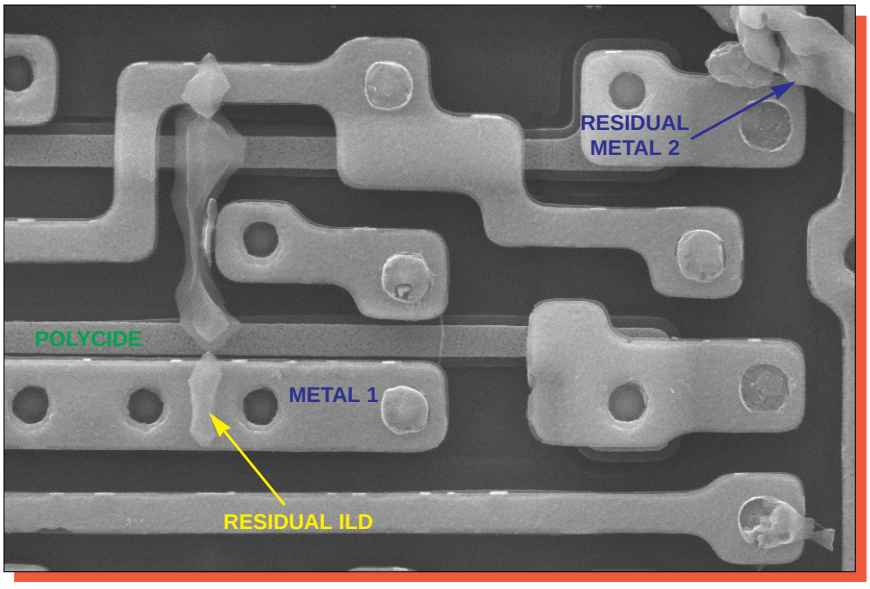
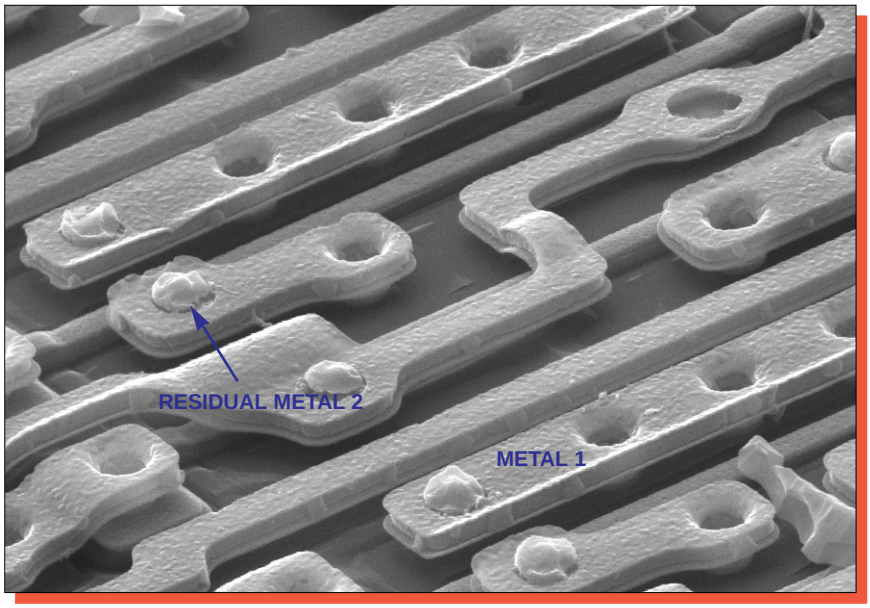
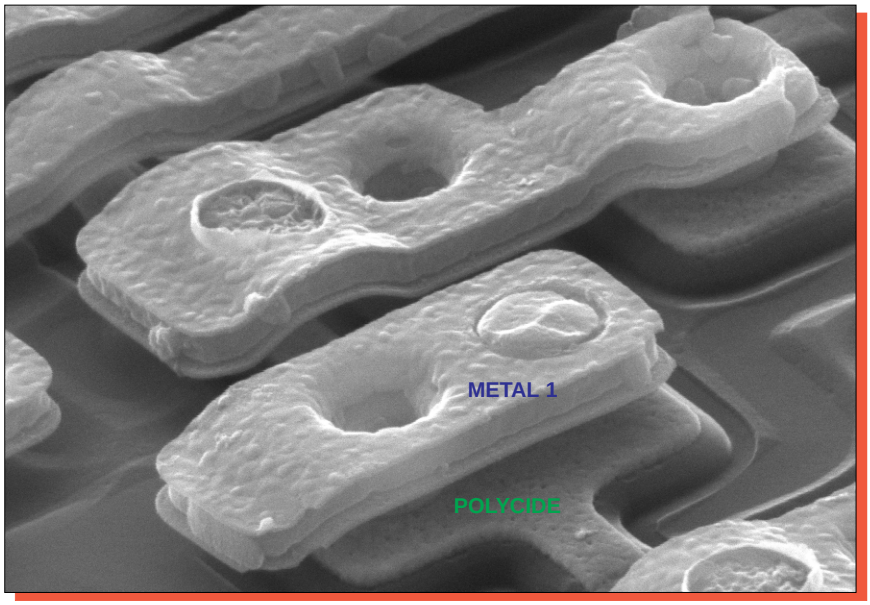


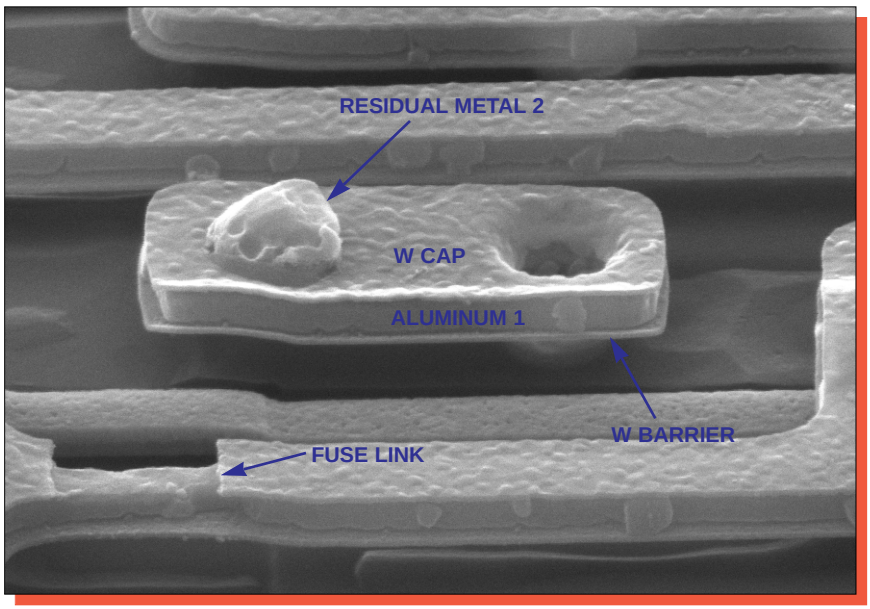
Figure 18. Topological SEM view of metal 1 patterning. Mag. 5000x, 0°.



Mag. 6500x

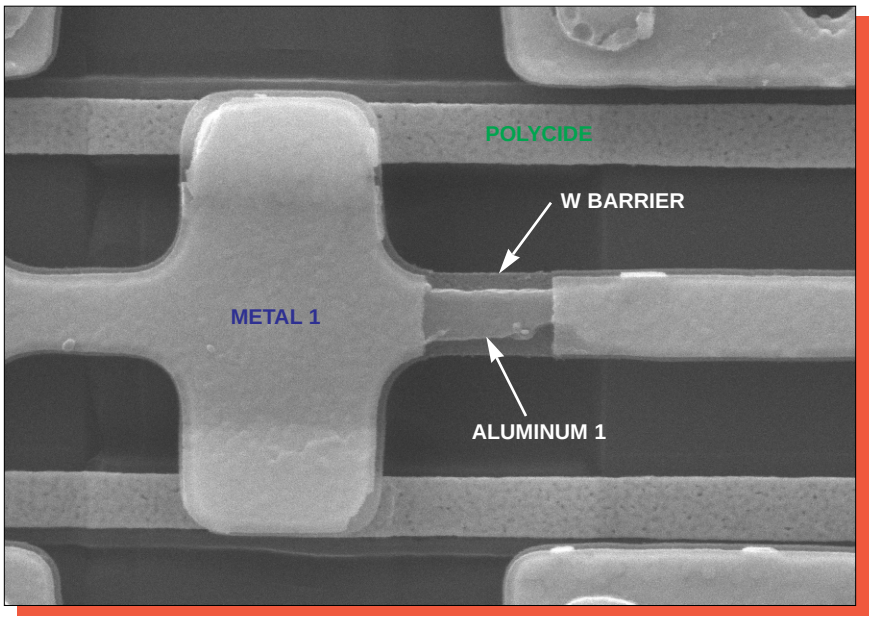


Mag. 13,000x

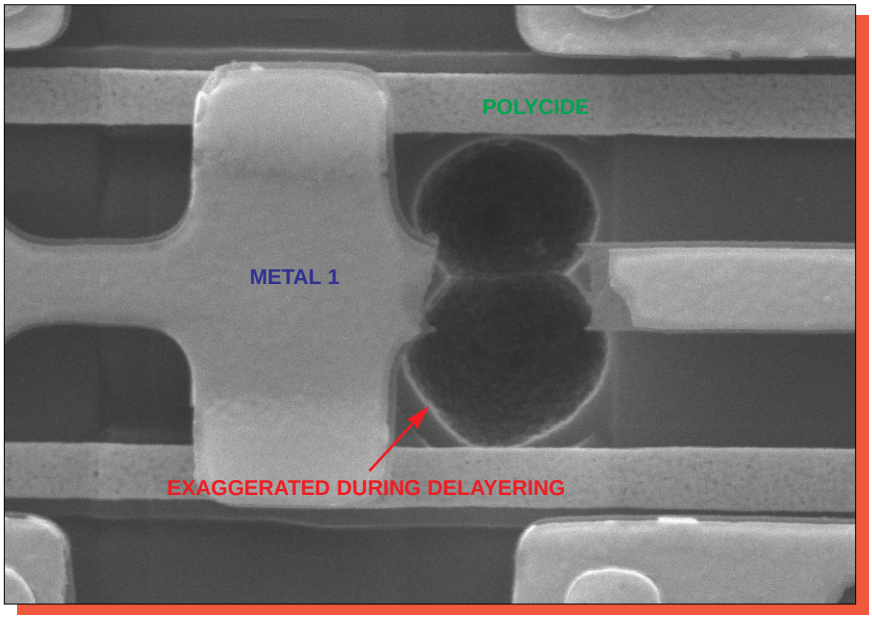


Mag. 13,000x

Figure 19. SEM views illustrating metal 1 step coverage. 60°.

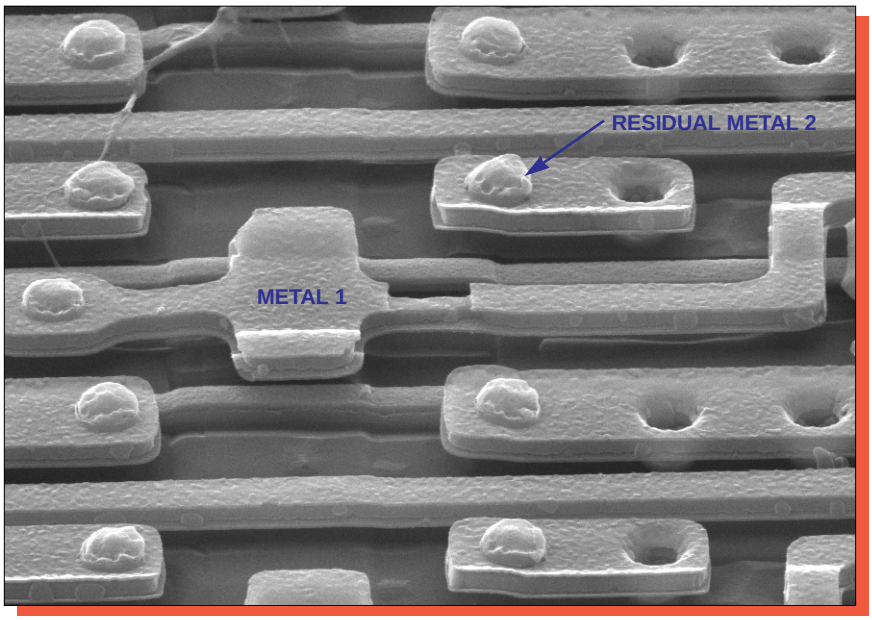


intact

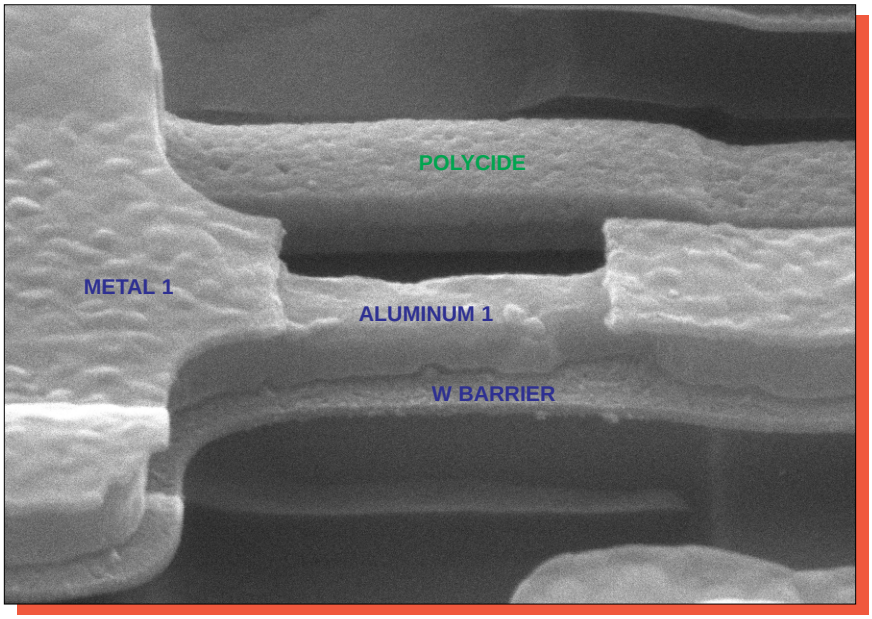


blown

Figure 20. Topological SEM views of metal 1 fuse links. Mag. 10,000x, 0°.

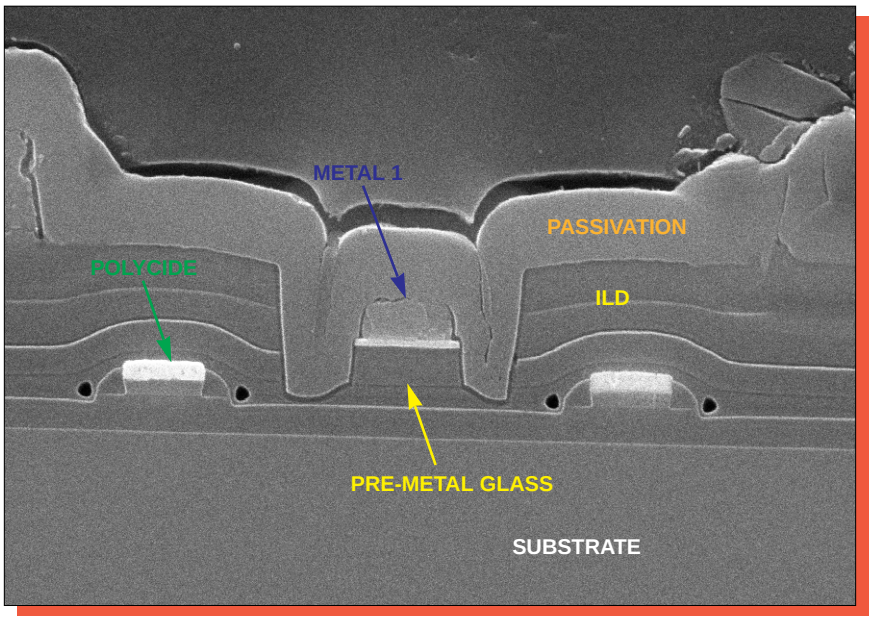


Mag. 6500x

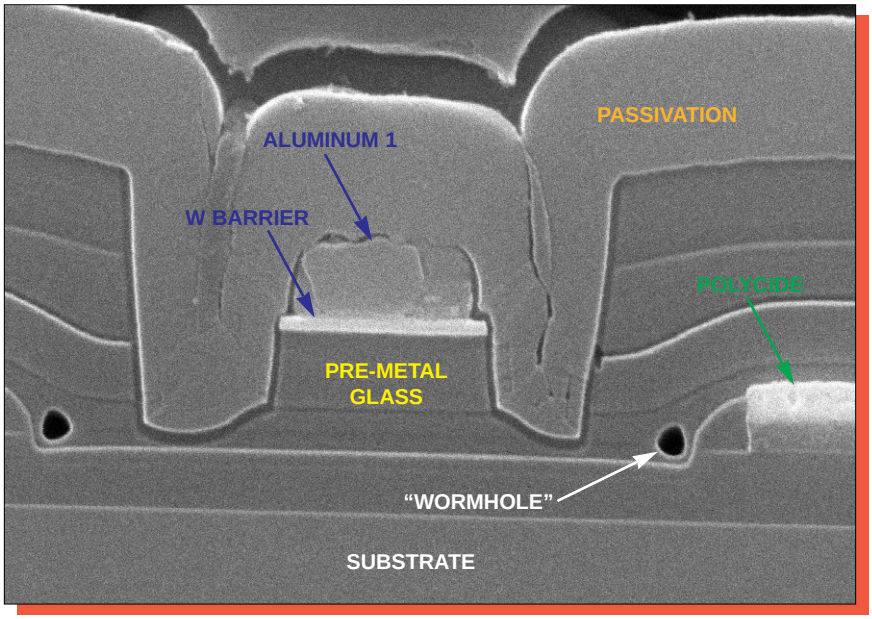


Mag. 26,000x

Figure 21. SEM views illustrating metal 1 fuse links. 60°.

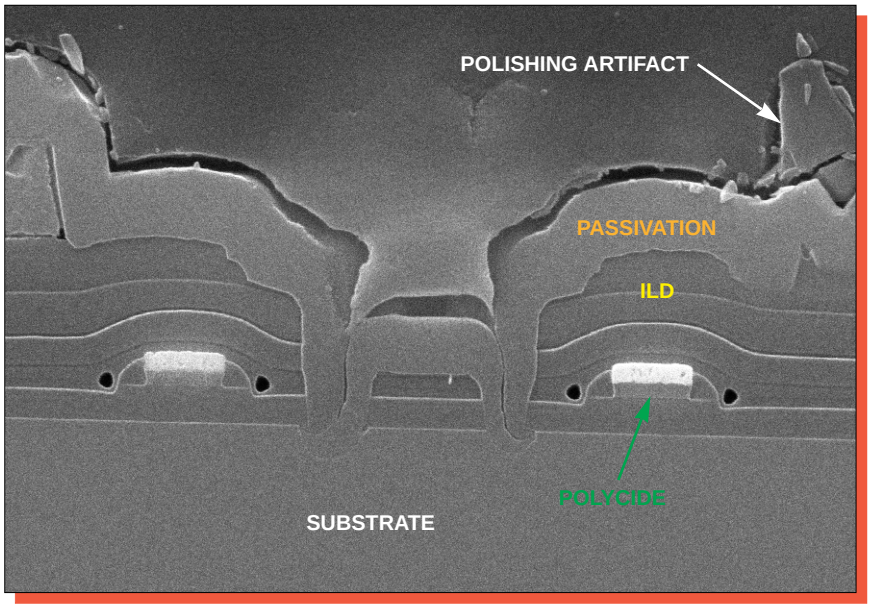


Mag. 13,000x

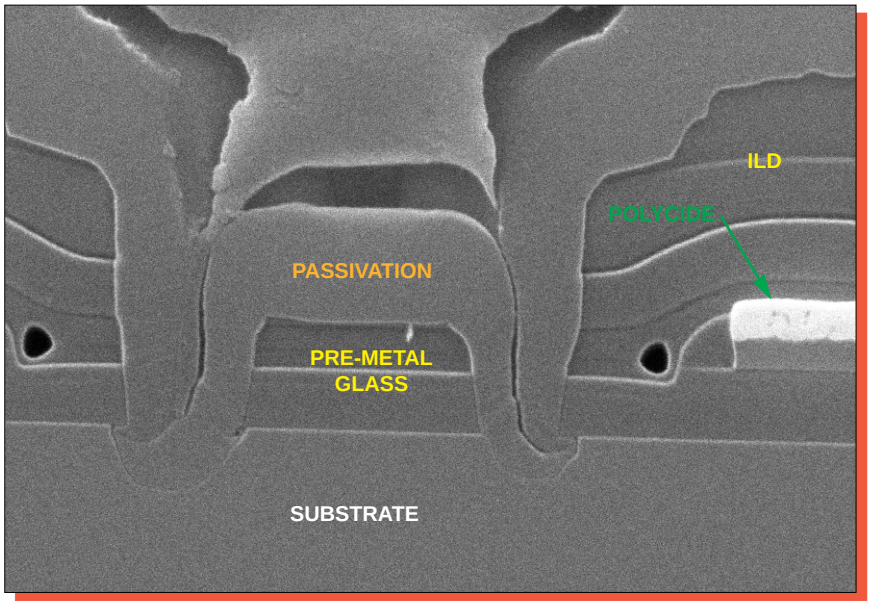


Mag. 26,000x

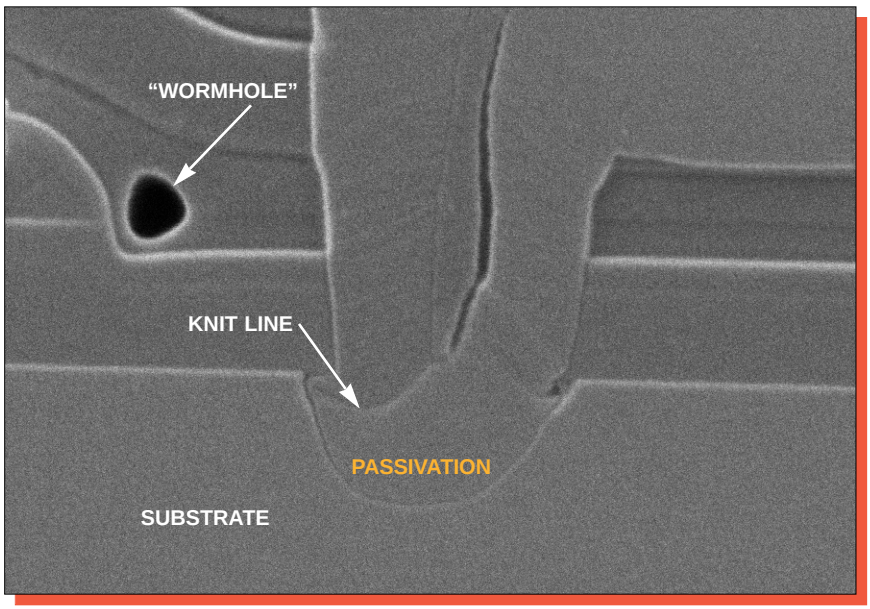
Figure 22. SEM section views of an intact metal 1 fuse link. Glass etch.



Mag. 13,000x

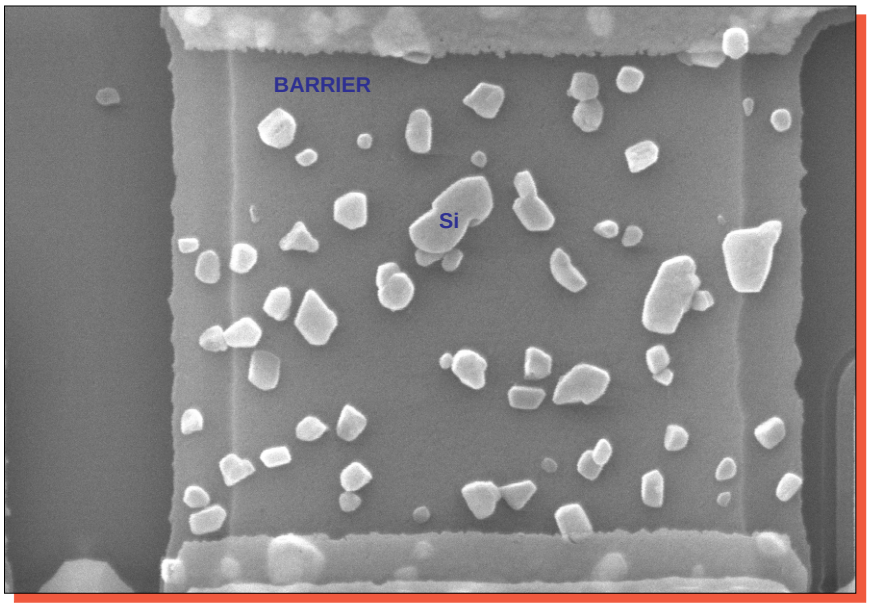


Mag. 26,000x

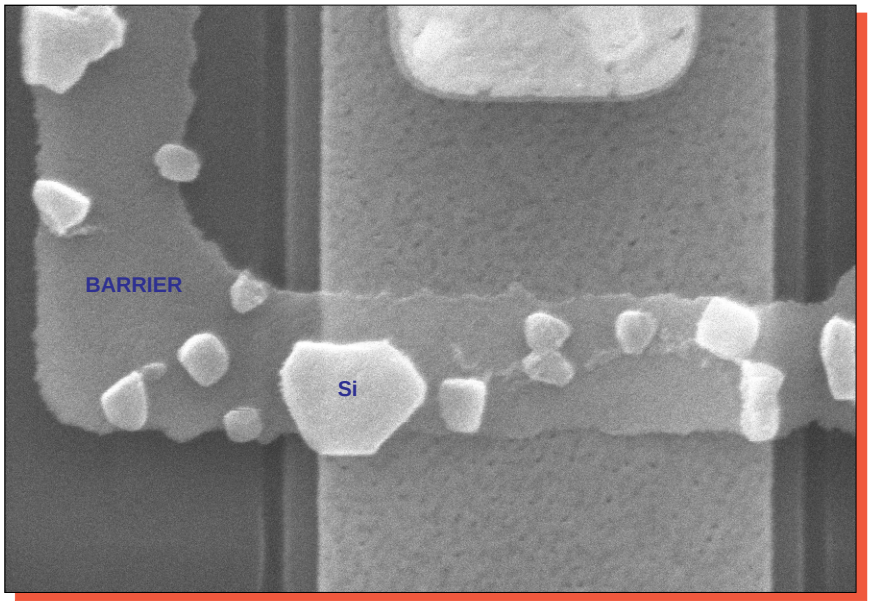


Mag. 52,000x

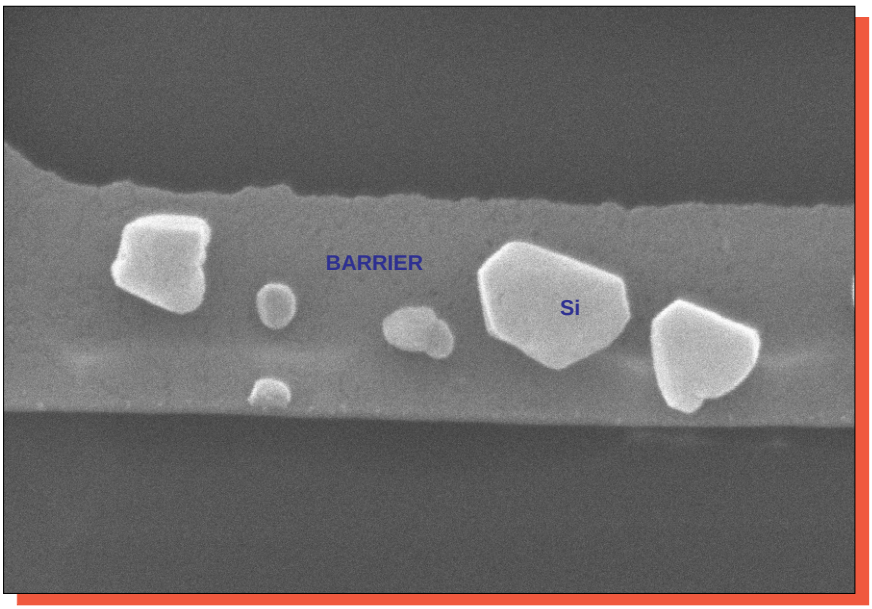
Figure 23. SEM section views of a blown metal 1 link. Glass etch.



Mag. 8000x

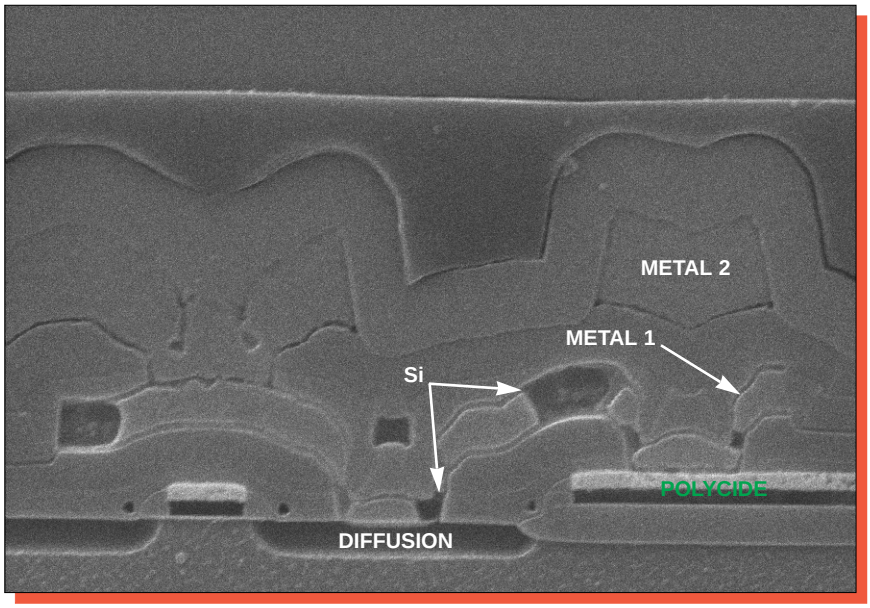


Mag. 15,000x

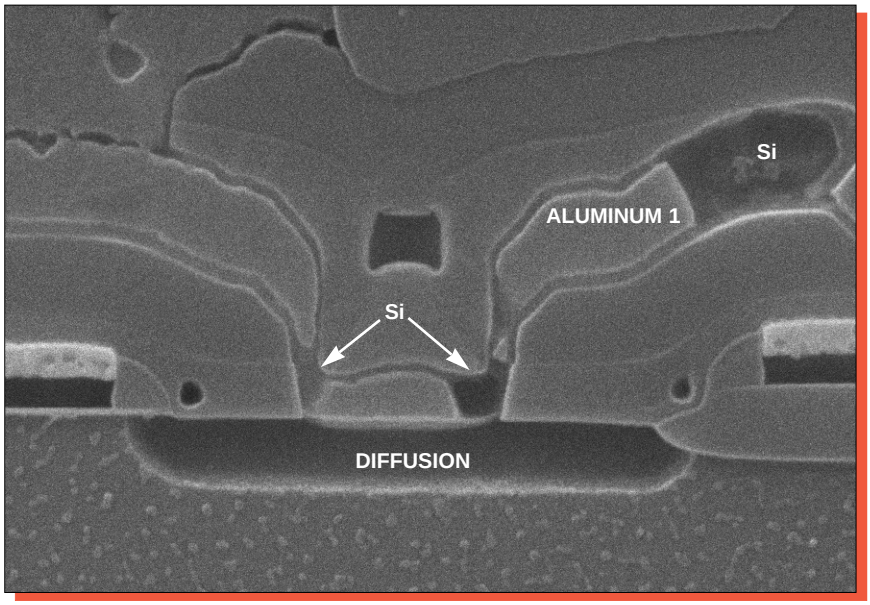


Mag. 19,000x

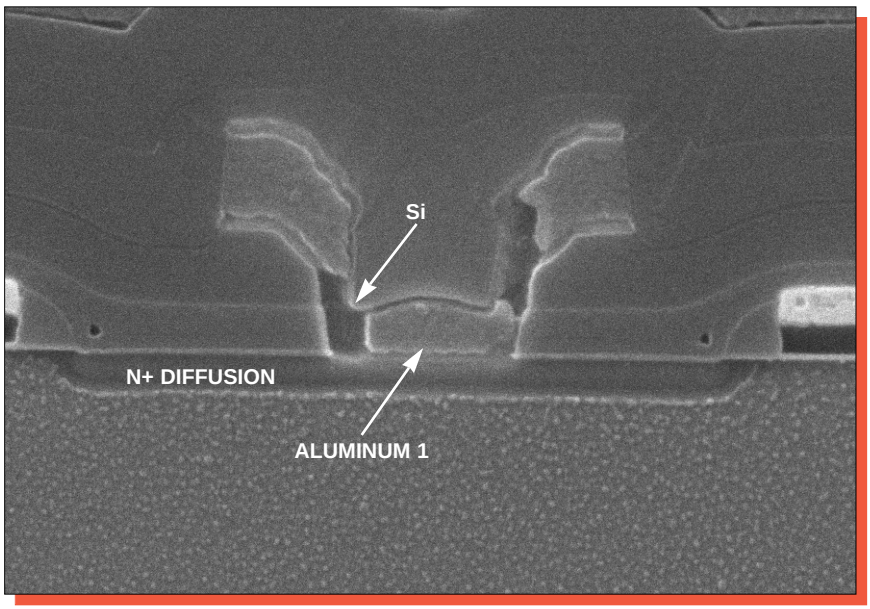
Figure 24. Topological SEM views illustrating metal 1 silicon nodules. 0°.



Mag. 13,000x

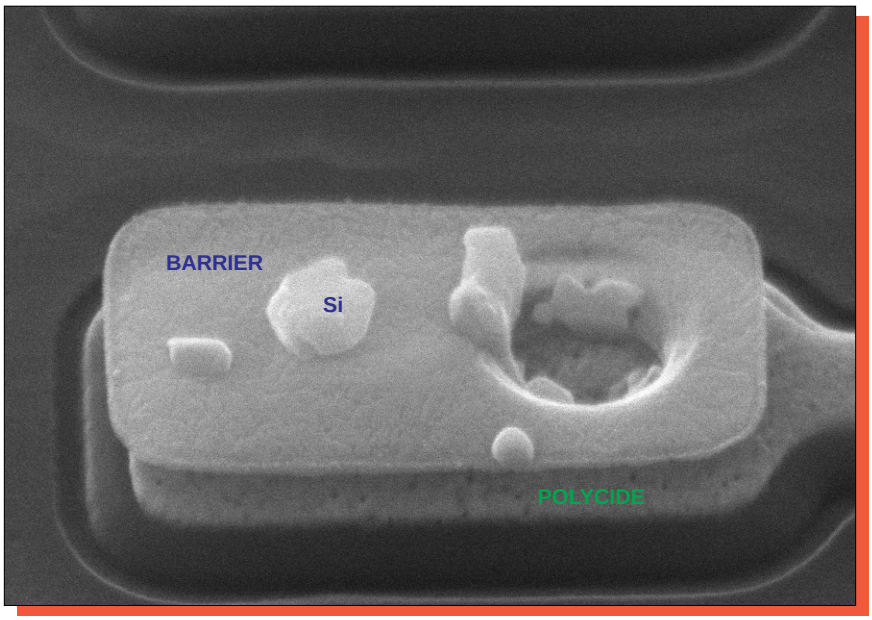


Mag. 26,000x

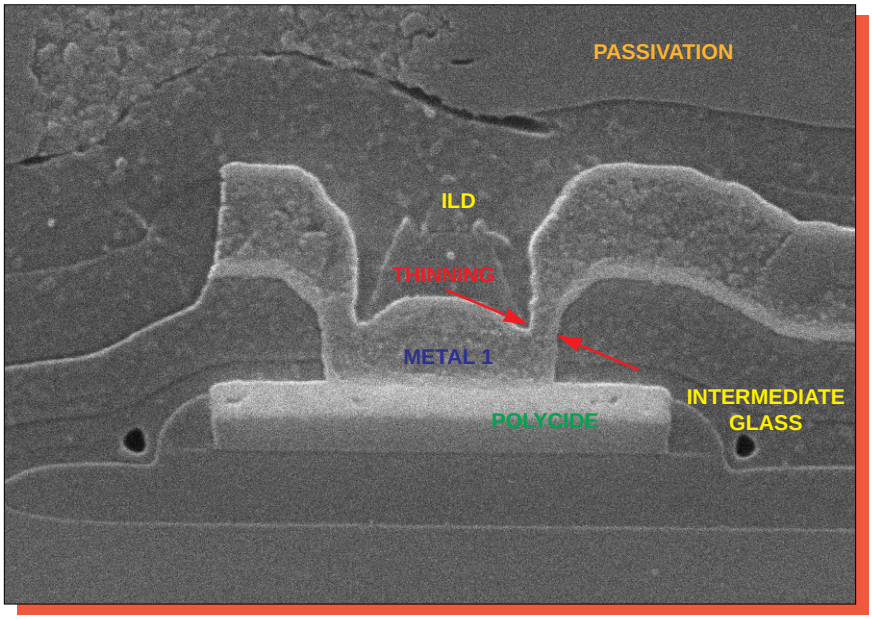


Mag. 26,000x

Figure 24a. Section views illustrating silicon nodules at contacts. Silicon etch.

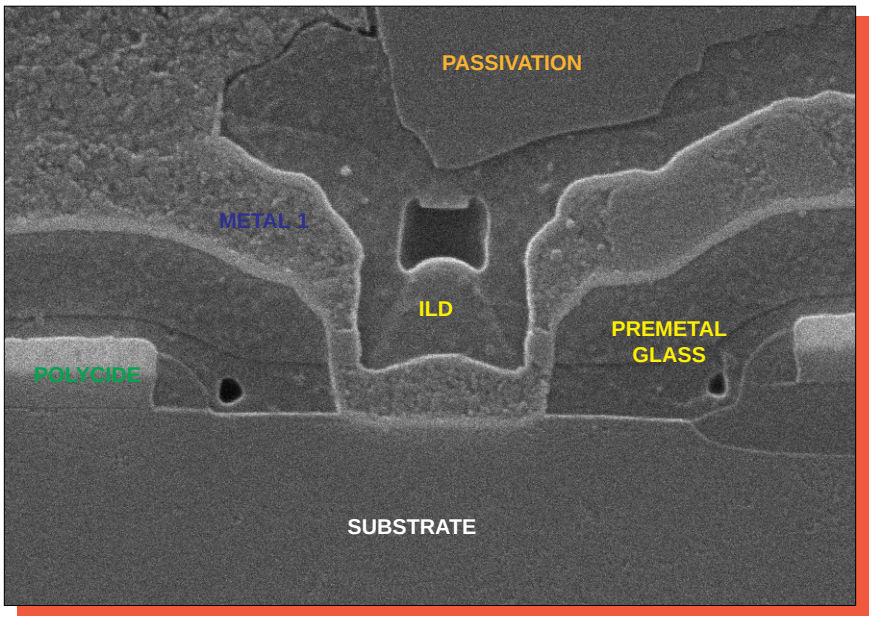


Mag. 20,000x, 45°



glass etch, Mag. 26,000x

Figure 25. SEM views illustrating typical contact cuts.



glass etch

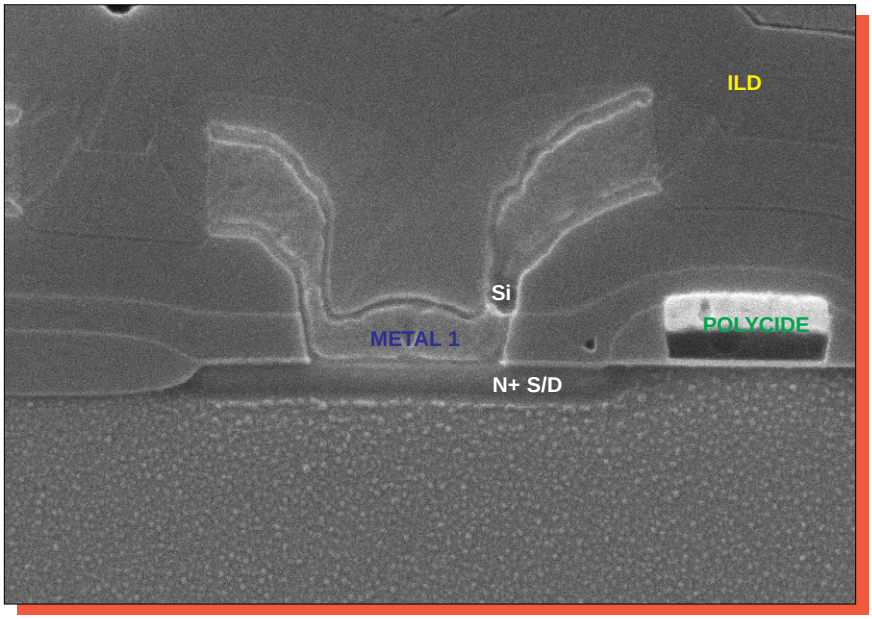
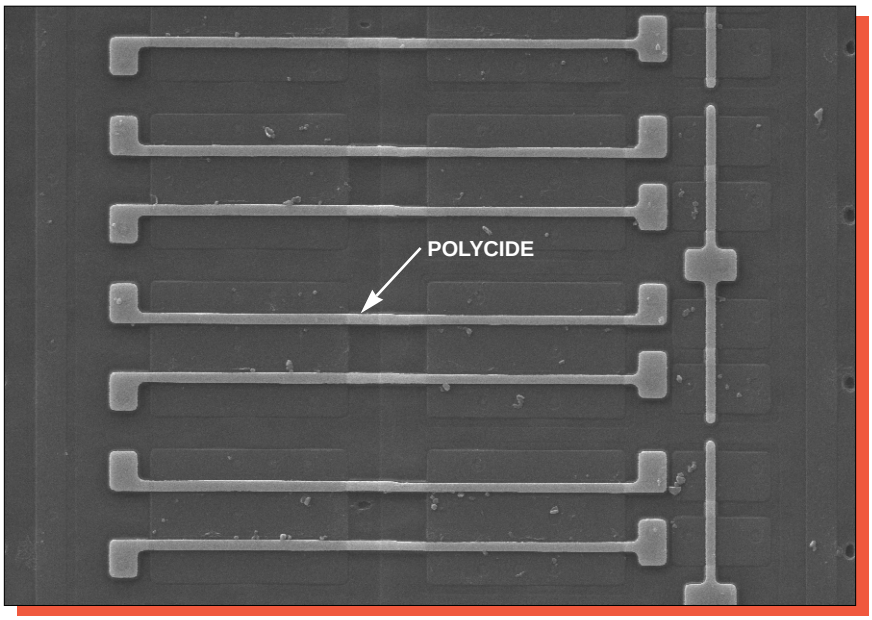
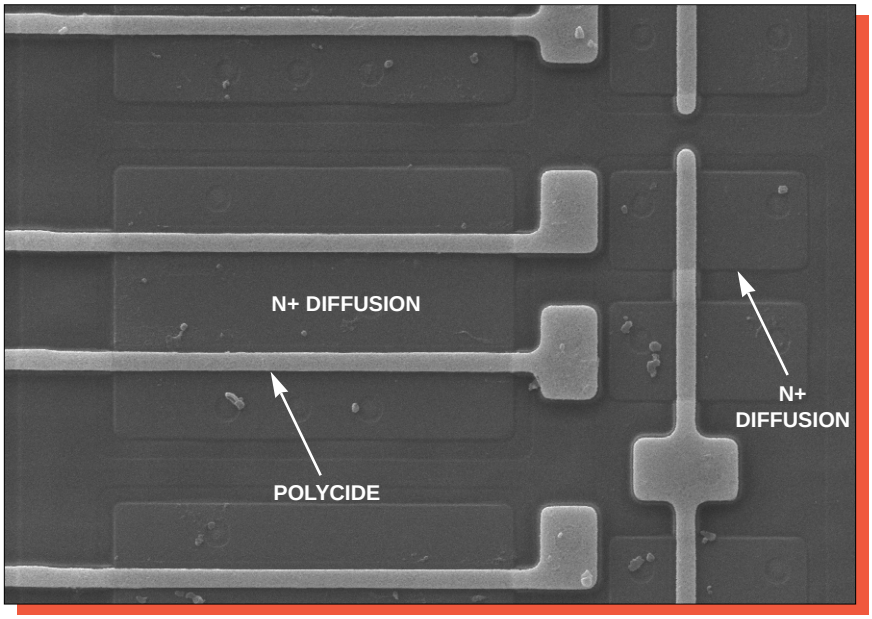


Figure 26. SEM section views illustrating typical contacts. Mag. 26,000x.

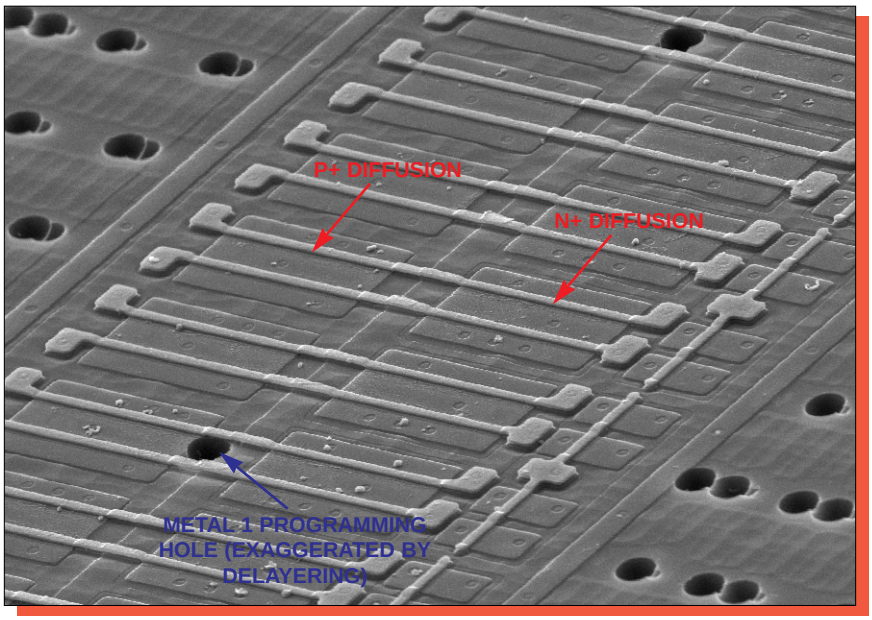


Mag. 1500x

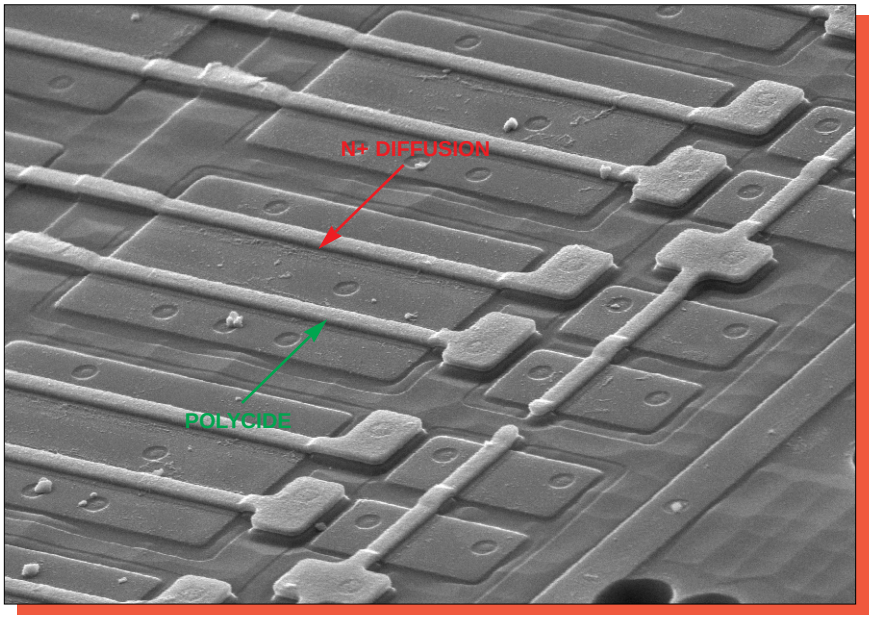


Mag. 3000x

Figure 27. Topological SEM views of polycide patterning. 0°.

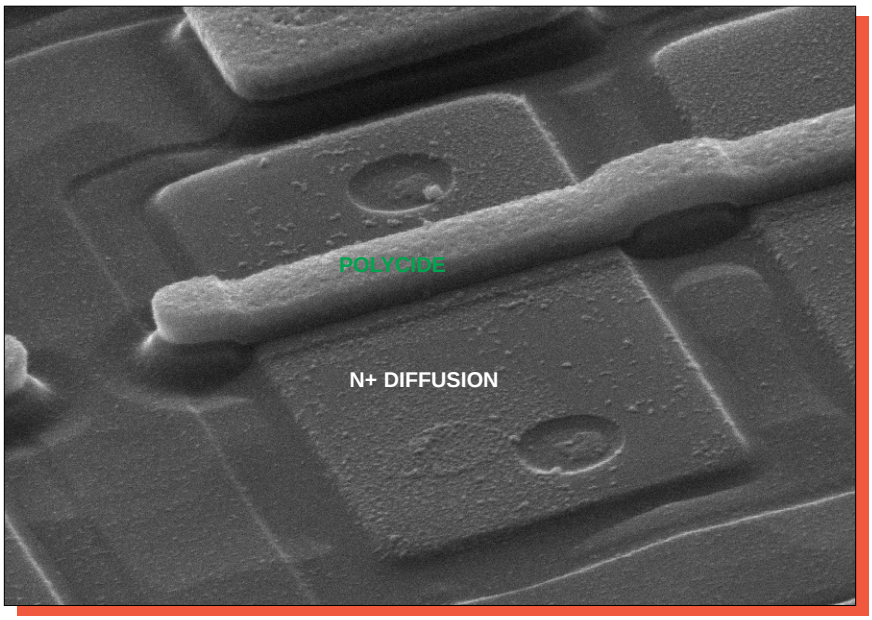


Mag. 1600x

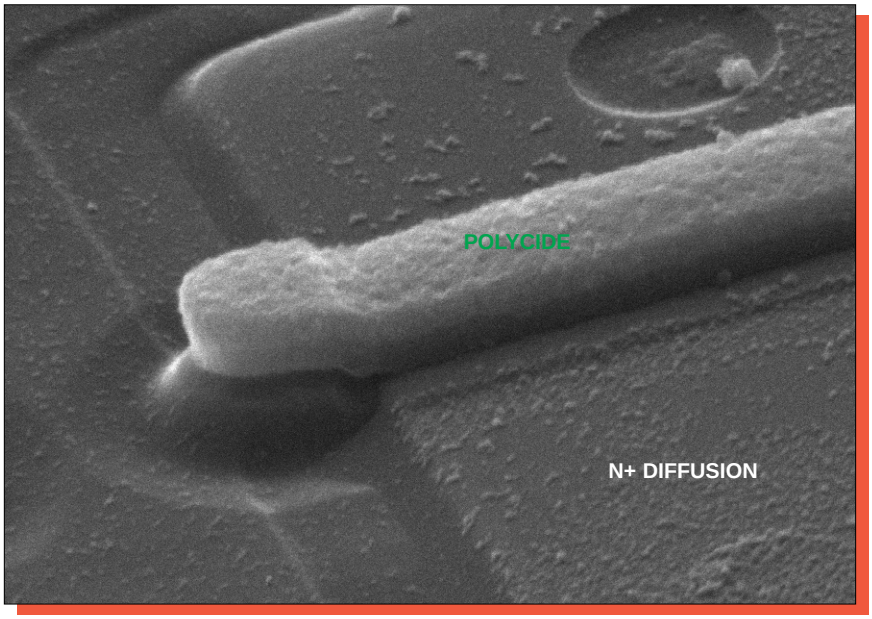


Mag. 3250x

Figure 28. SEM views of polycide step coverage. 60°.

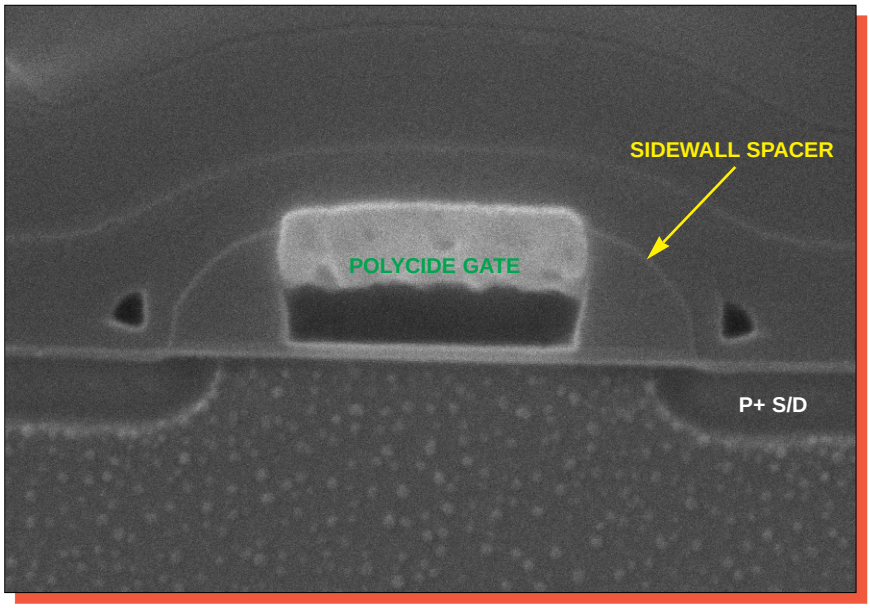


Mag. 13,000x

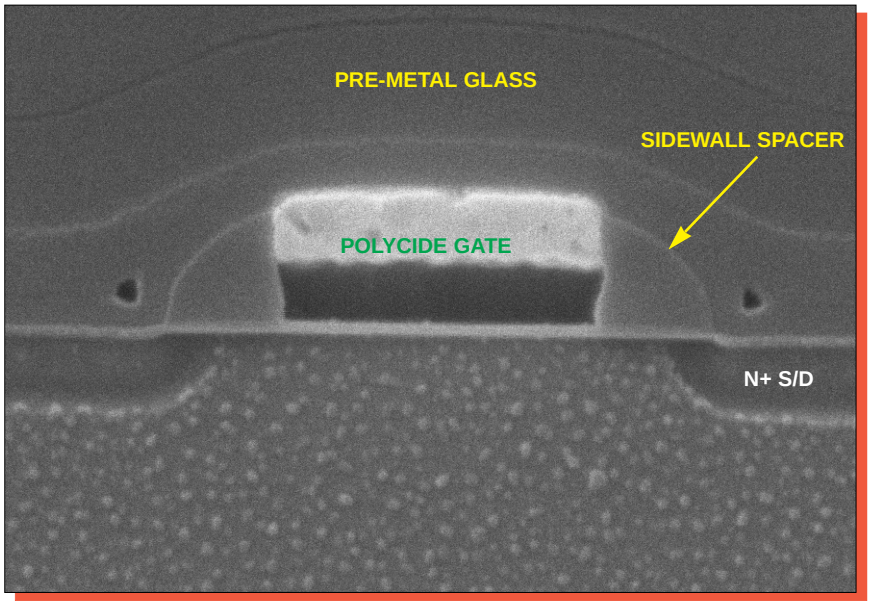


Mag. 26,000x

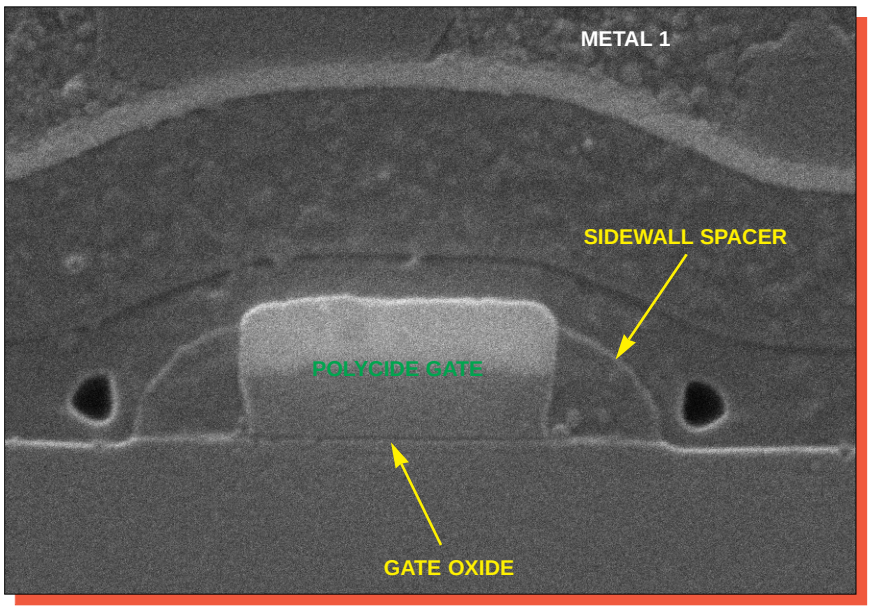
Figure 29. Detailed SEM views of polycide step coverage. 60°.



P-channel

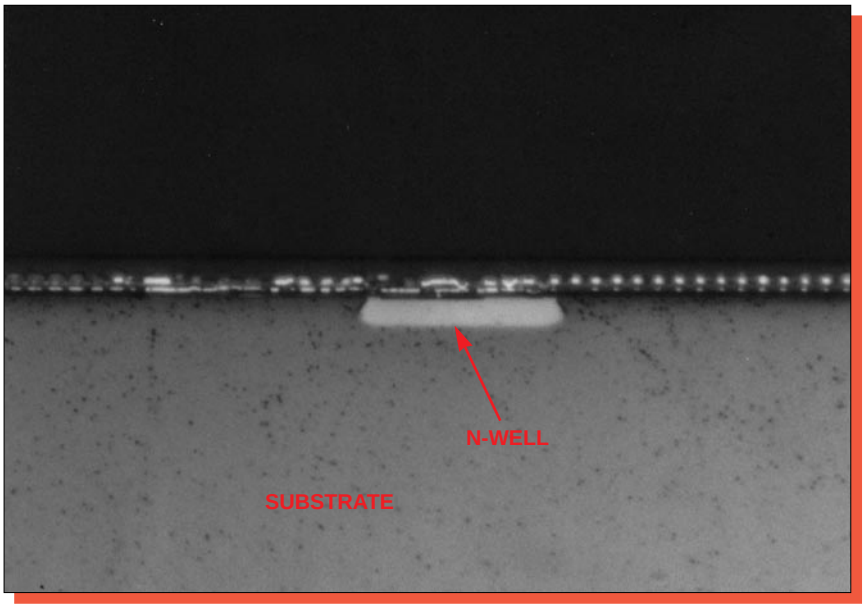


N-channel

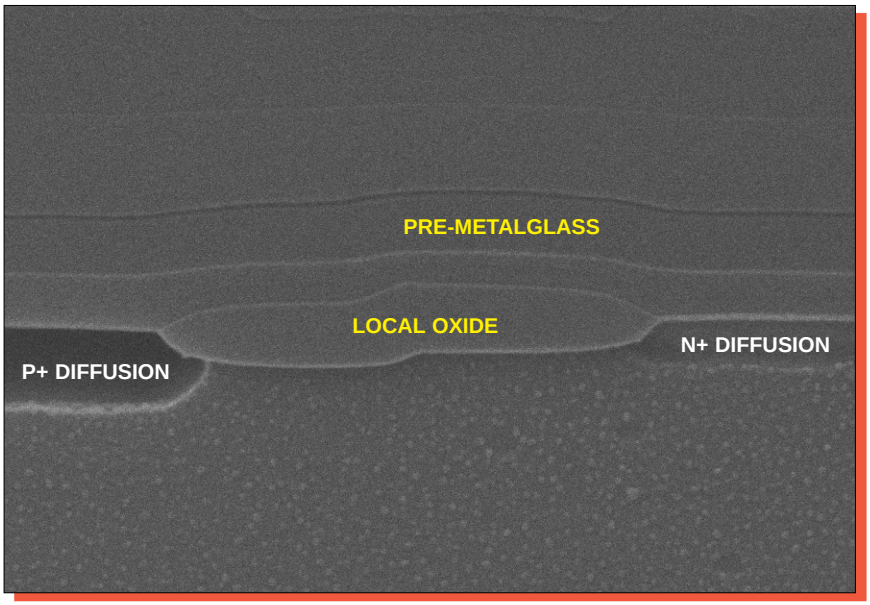


glass etch

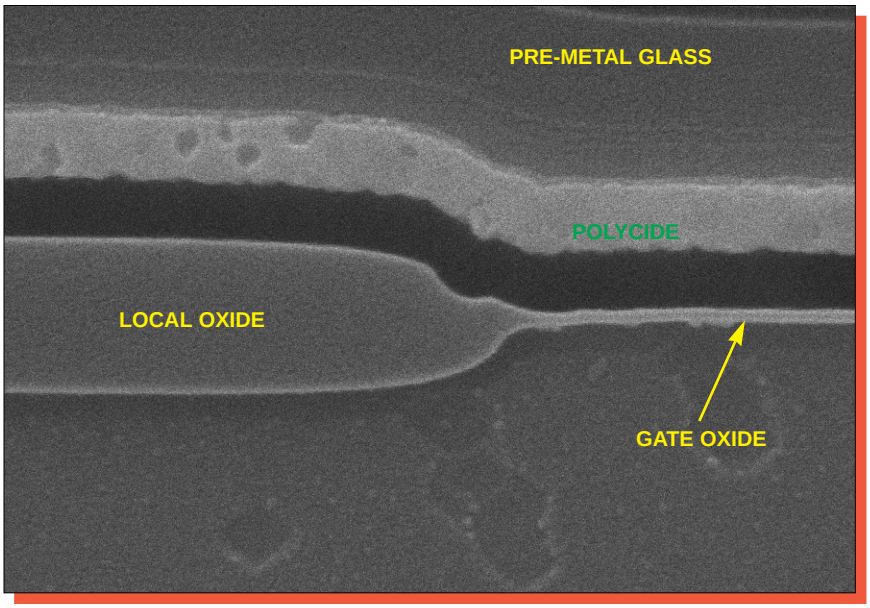
Figure 30. SEM section views of typical gates. Mag. 52,000x.



Mag. 800x



Mag. 26,000x



Mag. 52,000x

Figure 31. SEM section views illustrating well structure, step at well boundary, and a birdsbeak.

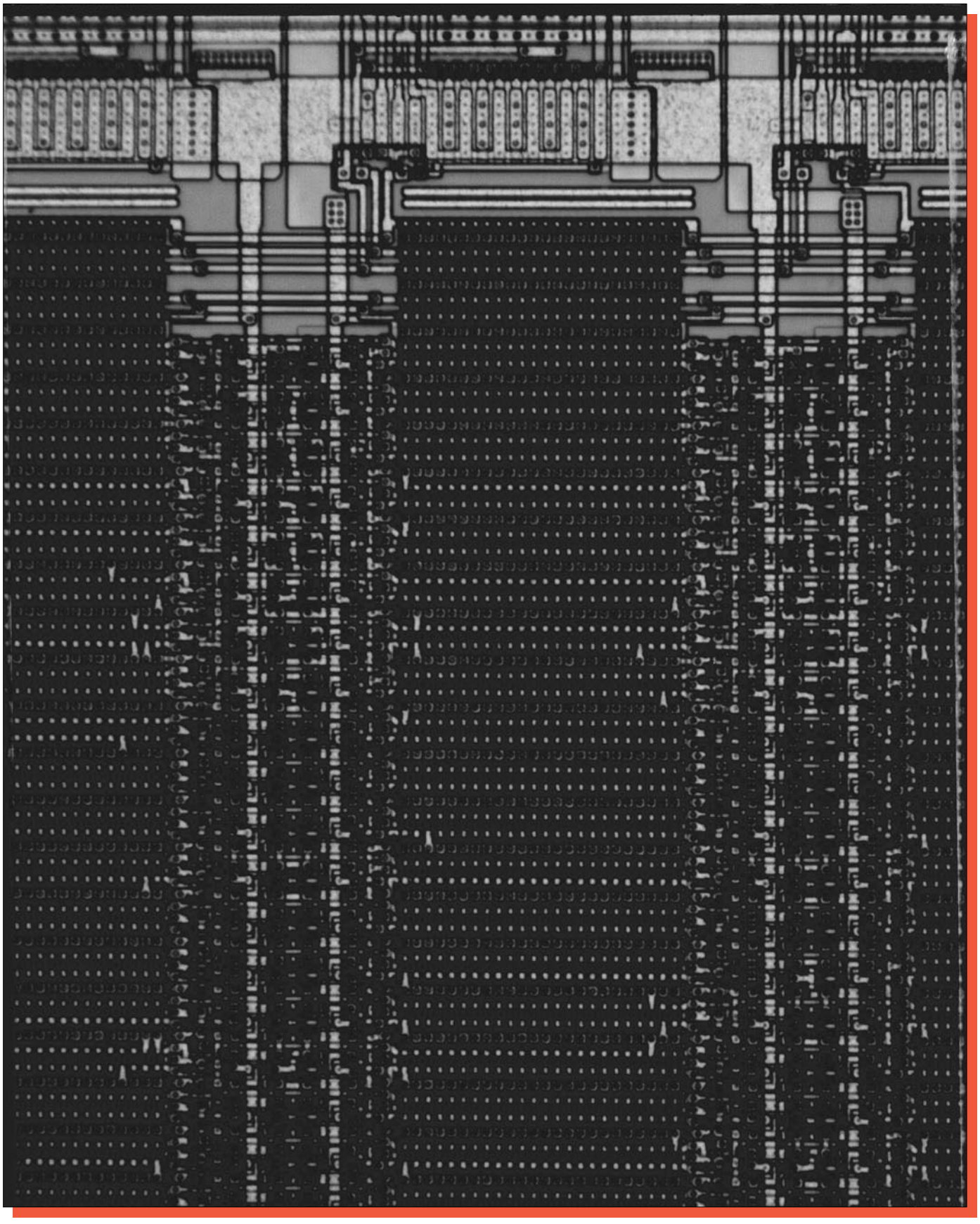
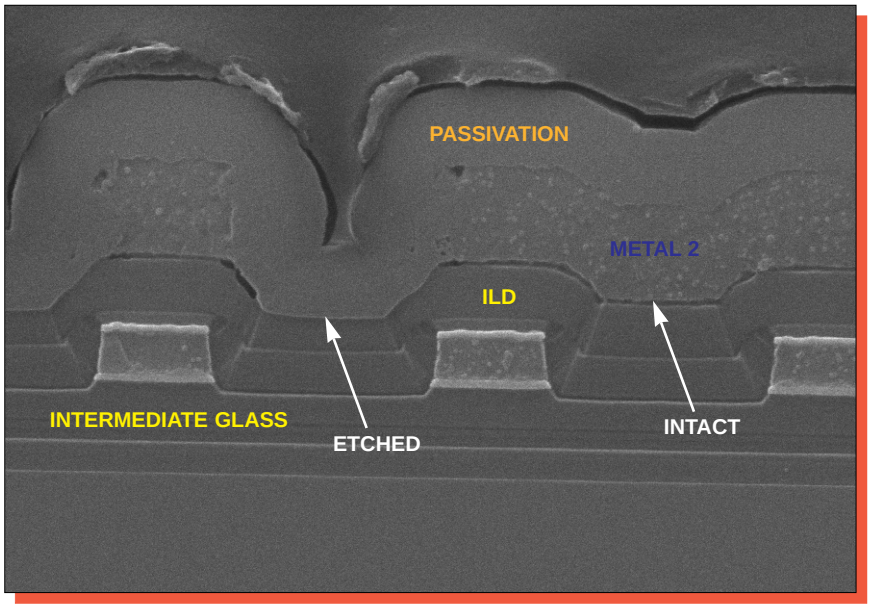
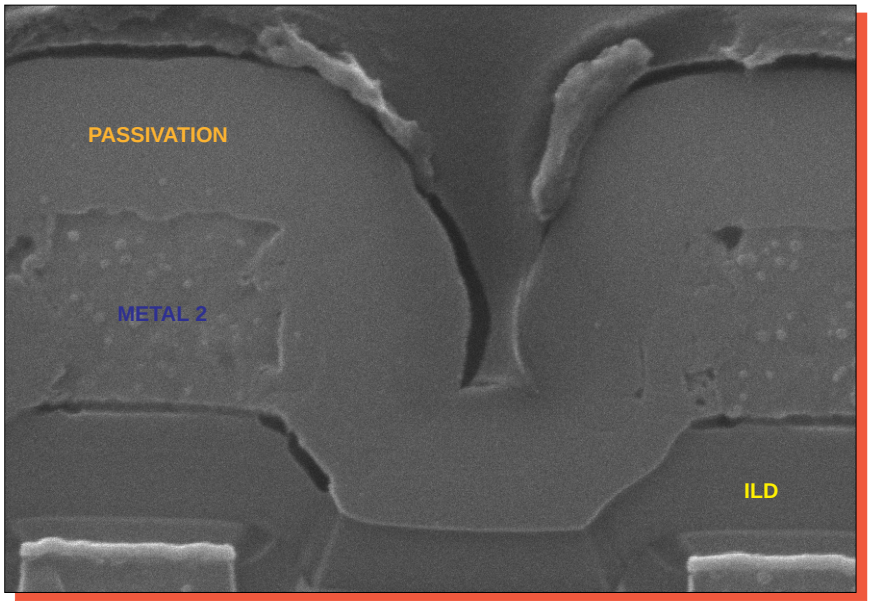


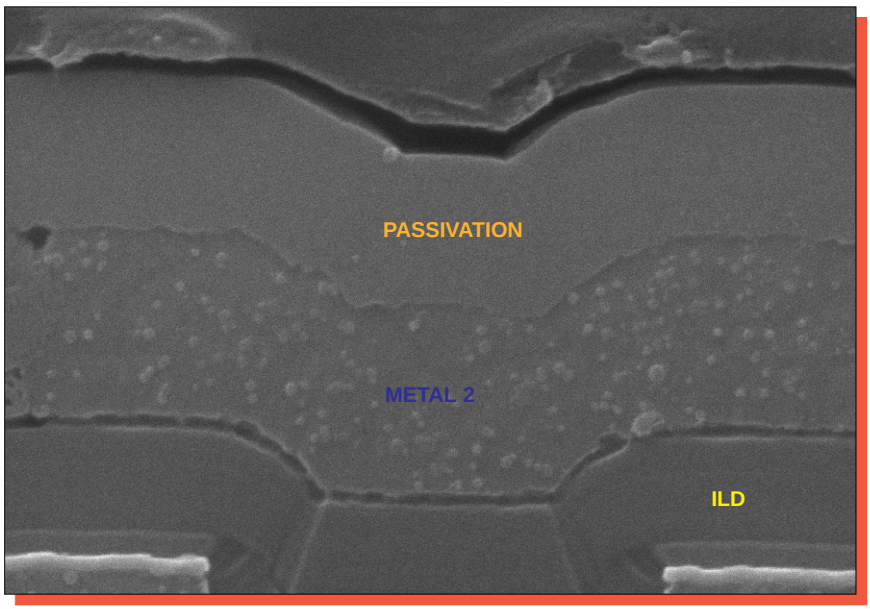
Figure 32. Optical view of programmable array. Mag. 640x.



Mag. 13,000x

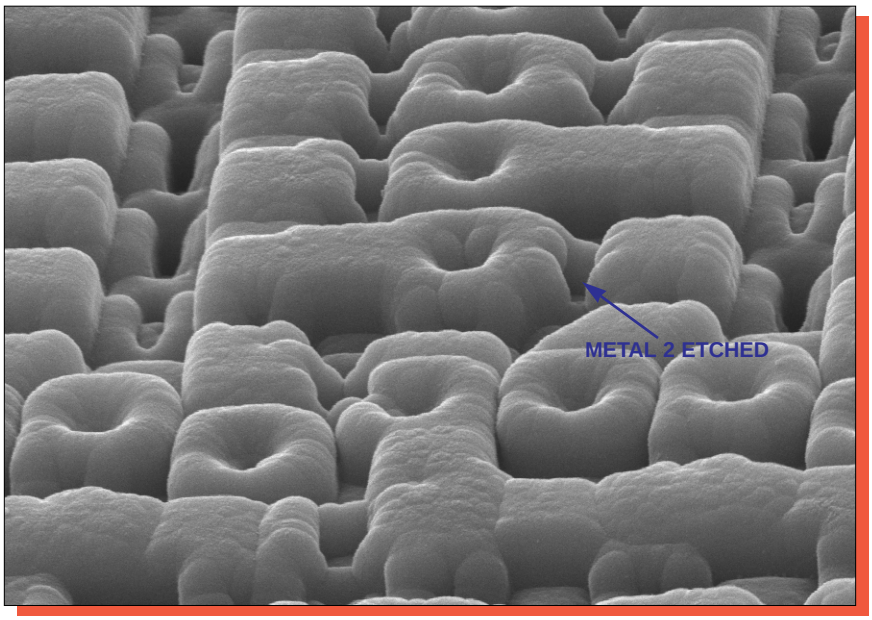


Mag. 26,000x

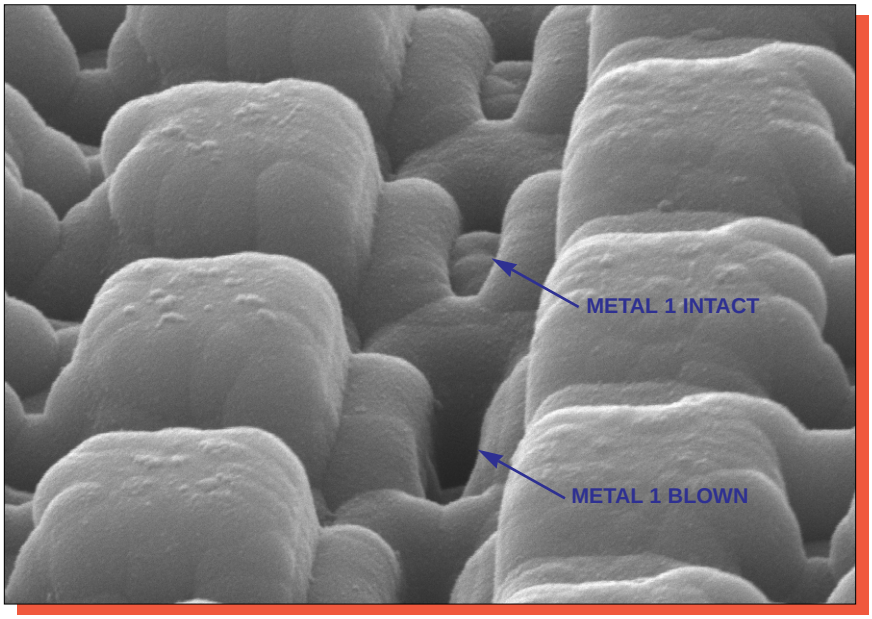


Mag. 26,000x

Figure 33. SEM section views illustrating (custom) mask etching of metal 2. Glass etch.

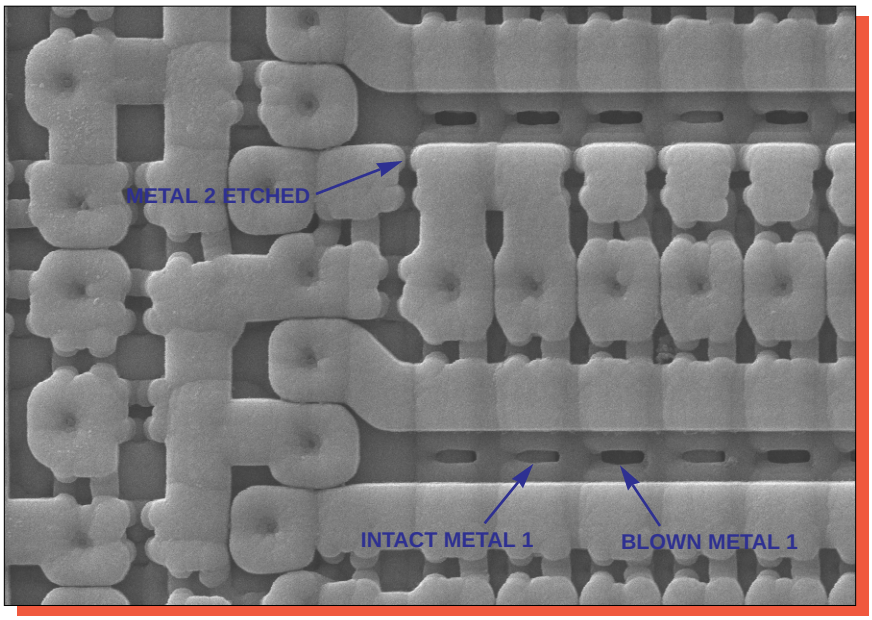


Mag. 6000x

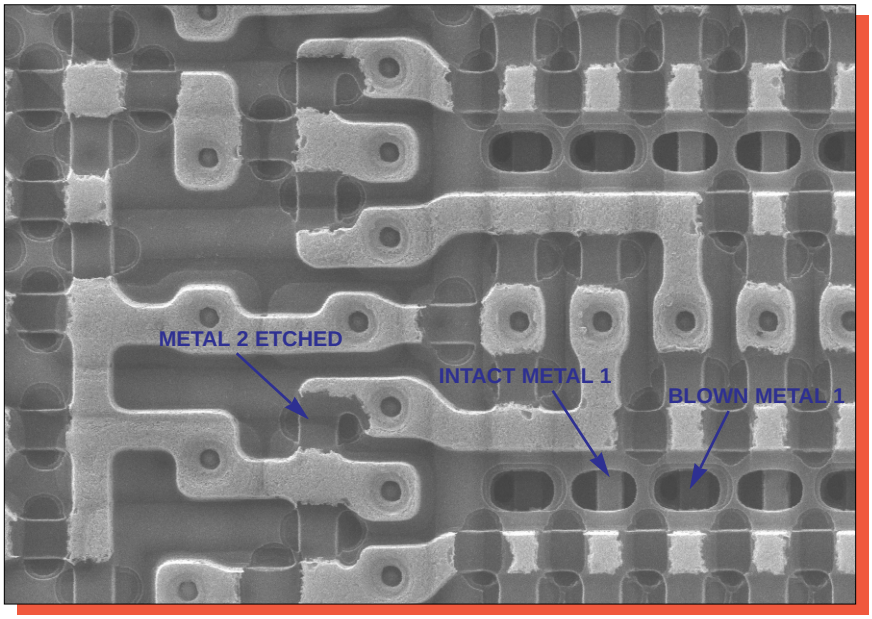


Mag. 12,000x

Figure 33a. SEM views of passivation coverage. 60°.

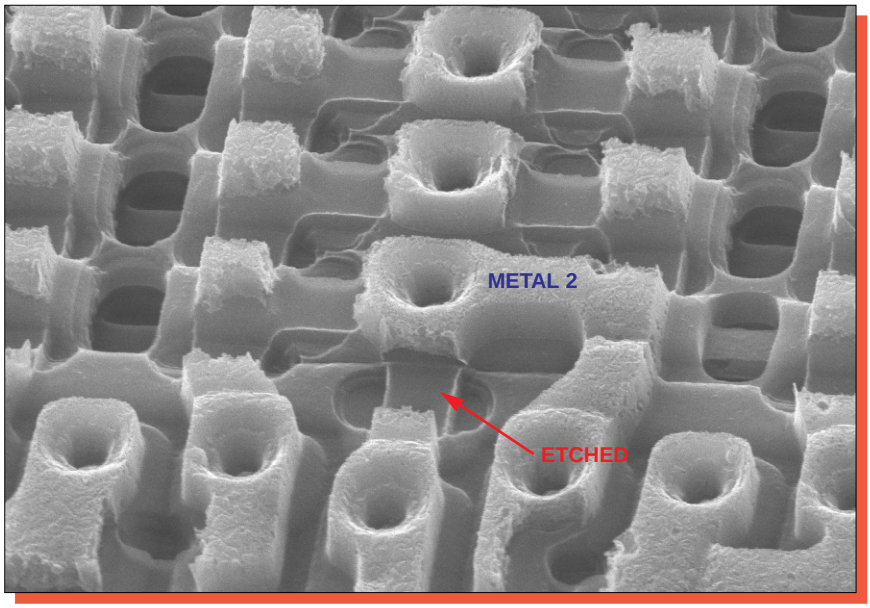


intact

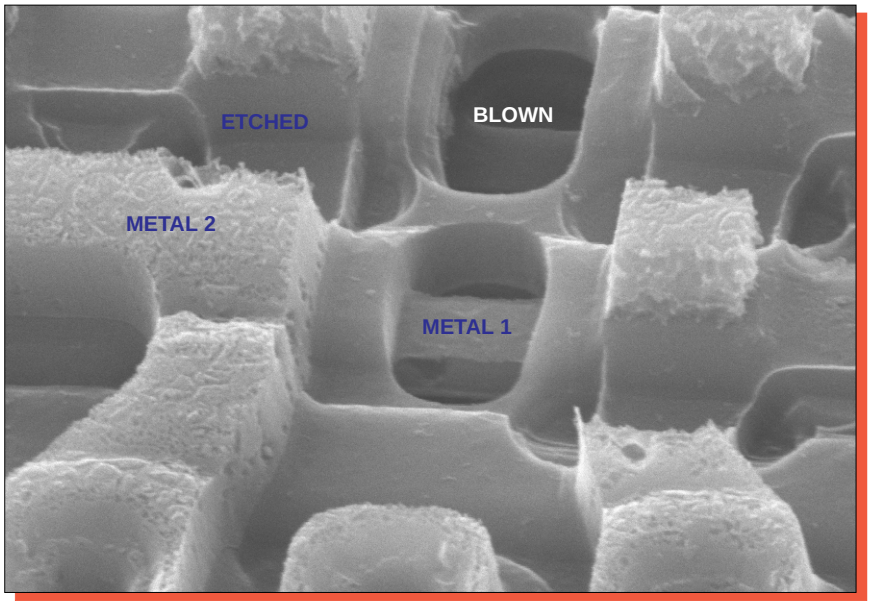


passivation removed

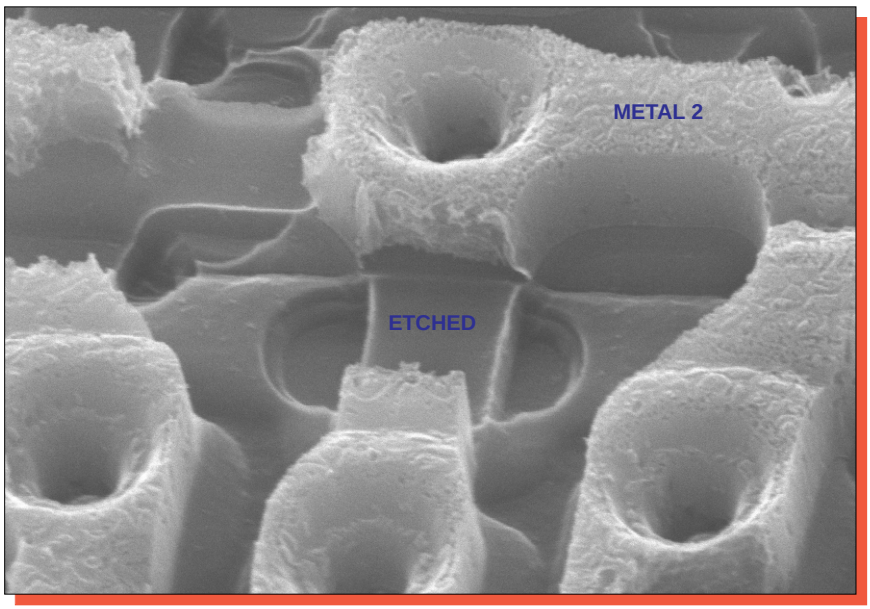
Figure 34. Topological SEM views of programmable array. Mag. 3250x.



Mag. 6000x

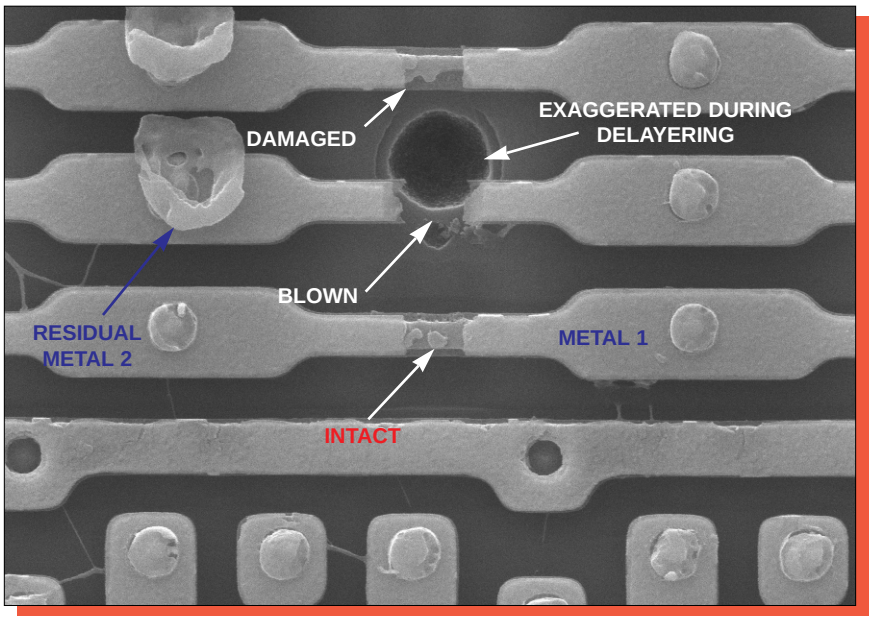


Mag. 12,000x

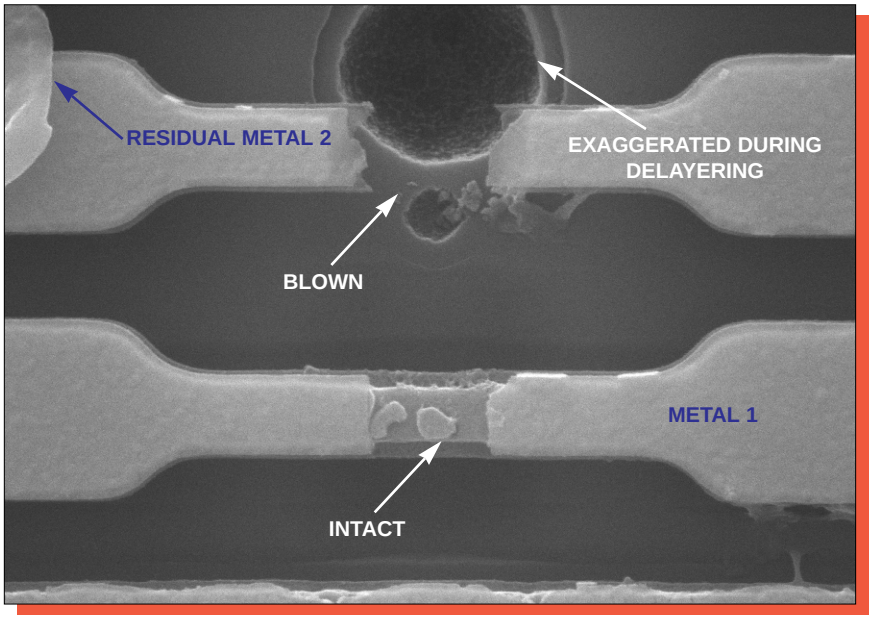


Mag. 12,000x

Figure 35. SEM views illustrating programmable array topology. 60°.

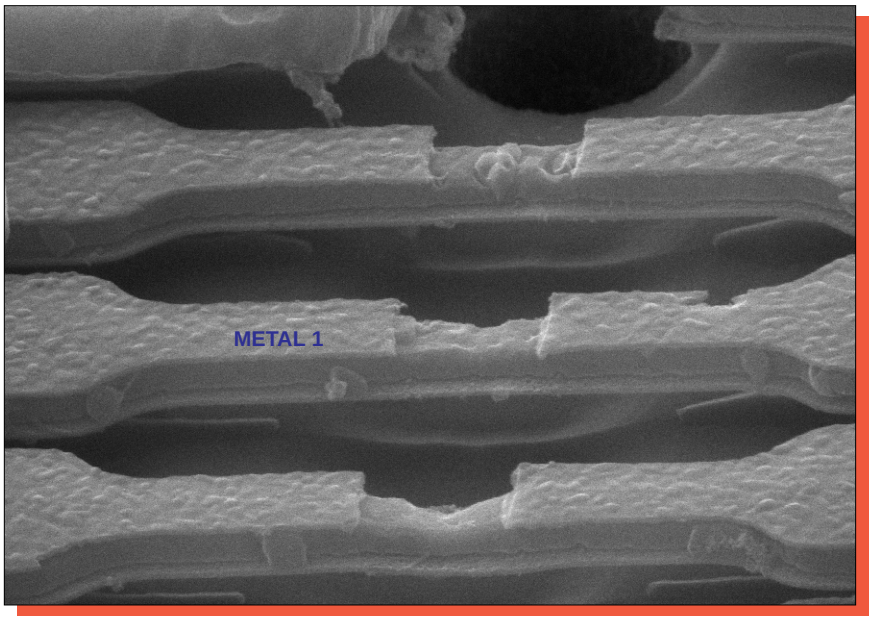


Mag. 5000x

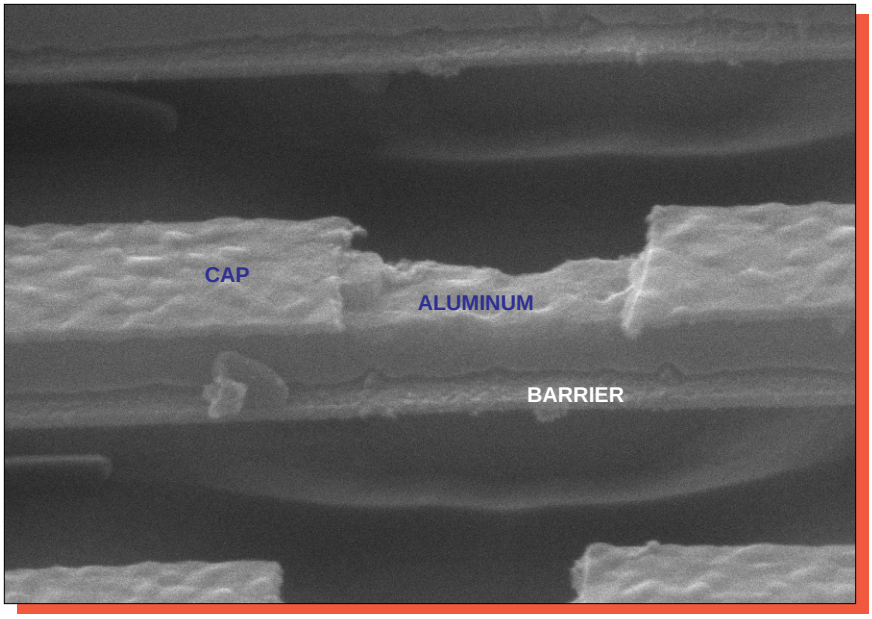


Mag. 10,000x

Figure 36. Topological views of metal 1 in programmable array. 0°.

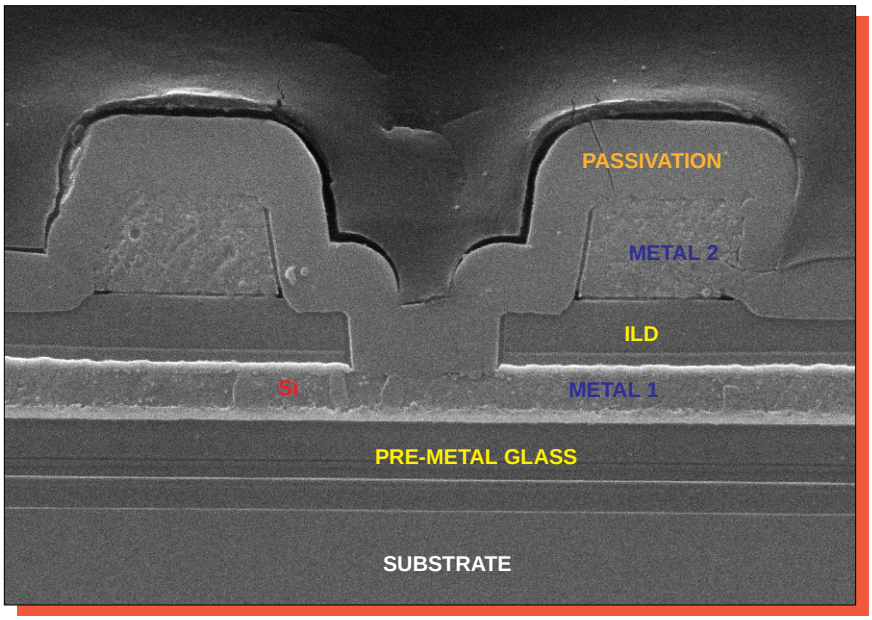


Mag. 13,000x

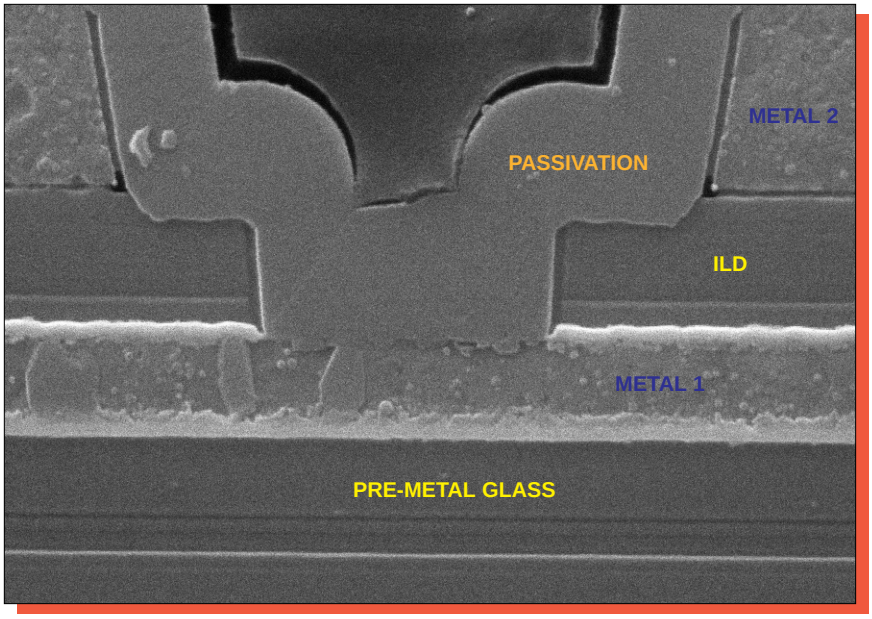


Mag. 26,000x

Figure 37. SEM views illustrating intact metal 1 programmable fuse links in programmable array. 60°.

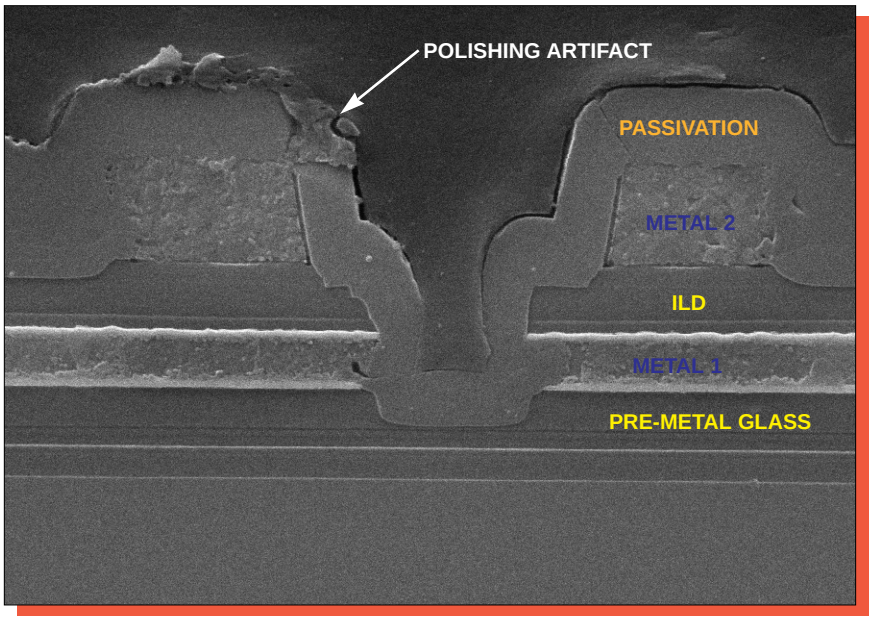


Mag. 13,000x

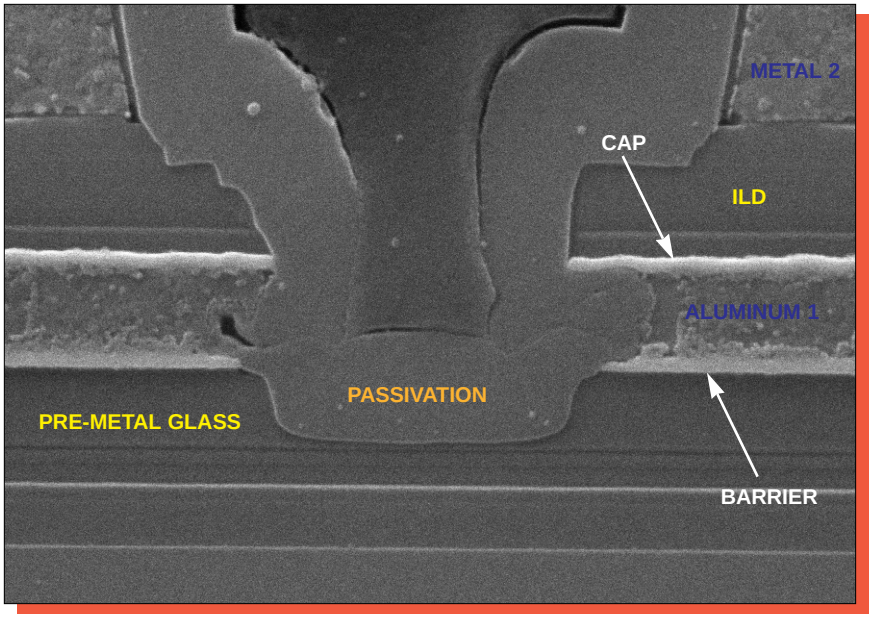


Mag. 26,000x

Figure 38. SEM section views illustrating intact metal 1 fuse link in programmable array. Glass etch.

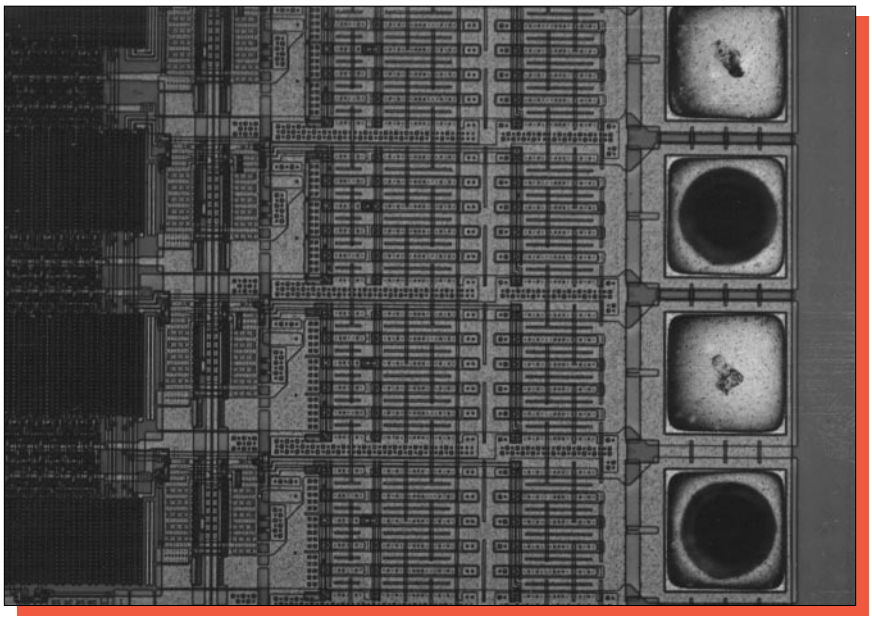


Mag. 13,000x

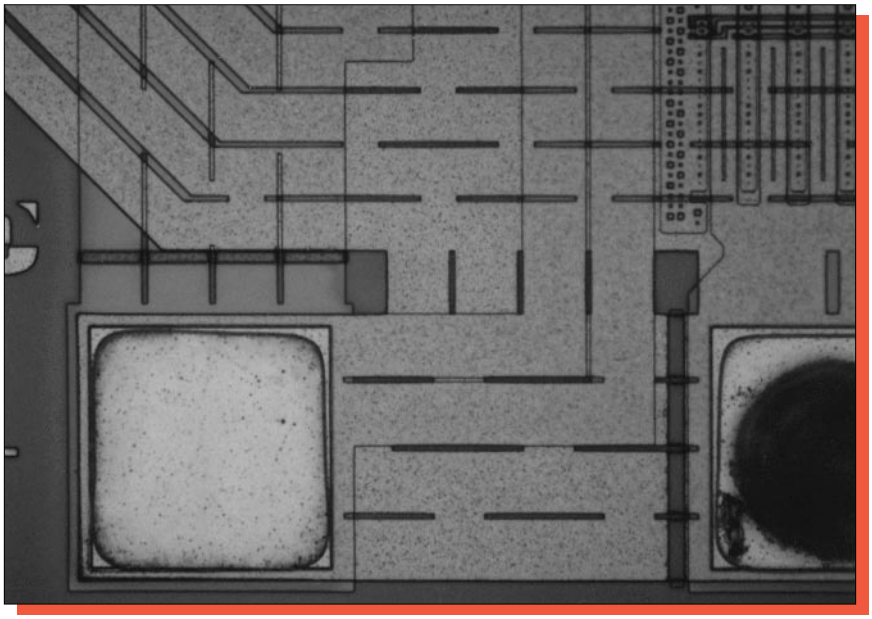


Mag. 26,000x

Figure 39. SEM section views illustrating a blown fuse link in the programmable array. Glass etch.

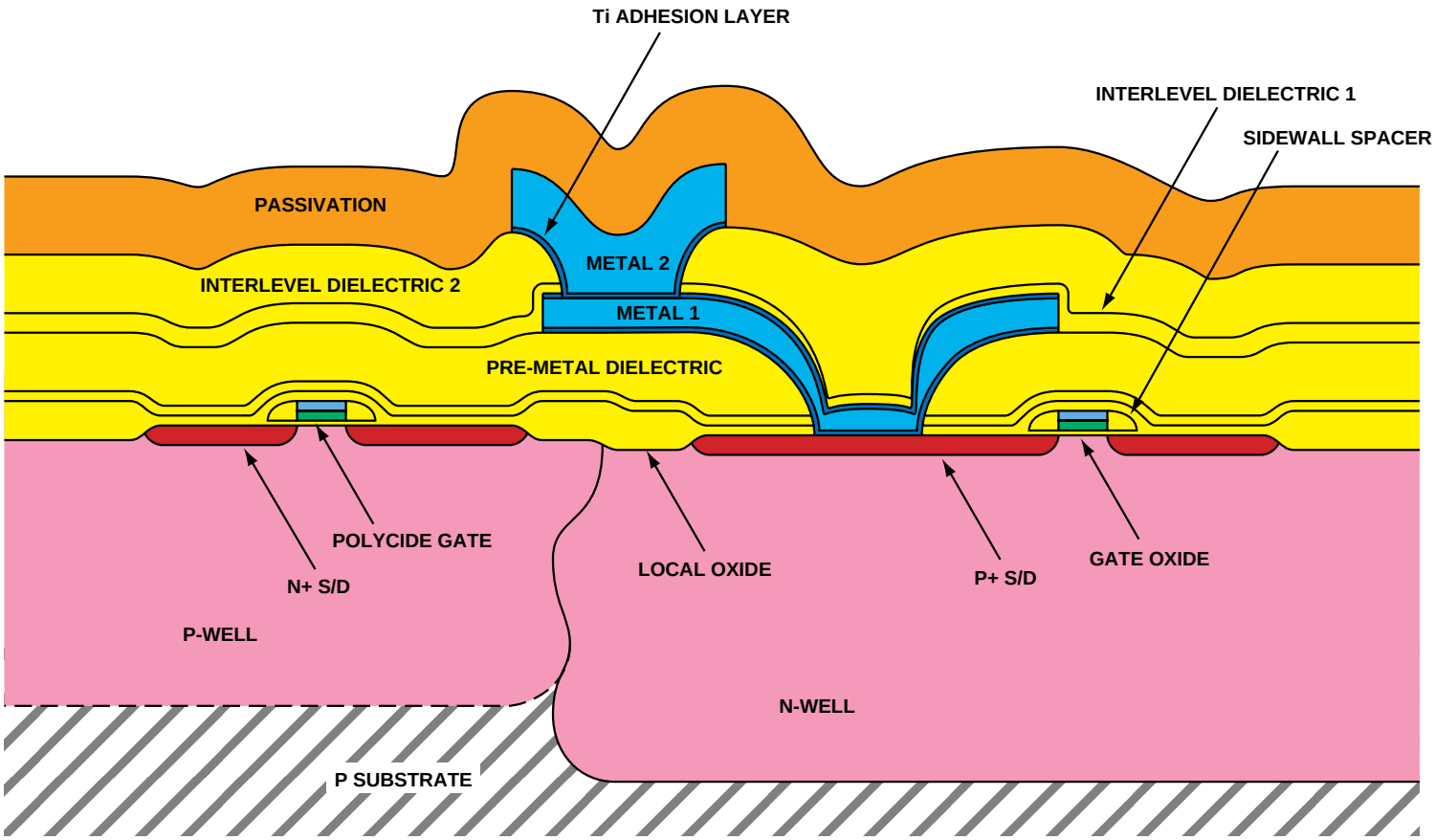


Mag. 160x



Mag. 320x

Figure 40. Optical views illustrating typical I/O structure and bus metal layout.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 41. Color cross section drawing illustrating device structure.