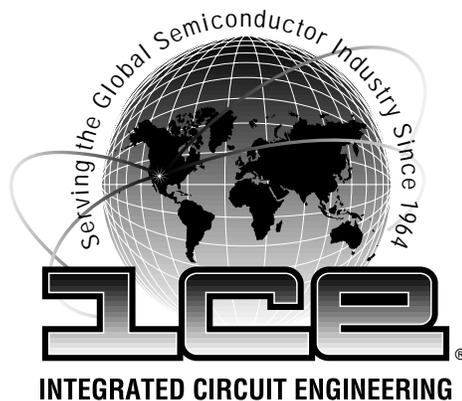


## Construction Analysis

# QLogic ISP1000 SCSI Processor

Report Number: SCA 9512-444



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## **INTRODUCTION**

This report describes a construction analysis of the Qlogic ISP1000 SCSI Processor. Four devices, which were packaged in 208-pin Square Quad Flat Packs (SQFP), were supplied for the analysis. The devices were date coded 9523.

## **MAJOR FINDINGS**

### **Questionable Items:<sup>1</sup>**

- Metal 2 aluminum thinned up to 95 percent<sup>2</sup> at vias (Figure 21). The barrier helped maintain continuity.
- Metal 1 aluminum thinned up to 85 percent<sup>2</sup> at poly contacts (Figure 27). This thinning was a result of "folds" in the metal at contact edges.

**Special Features:** None.

### **Design Features:**

- Slotted and beveled metal 2 bus lines, array of vias and contacts. Various size vias and contacts (Figure 13).

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## **TECHNOLOGY DESCRIPTION**

### **Assembly:**

- 208-pin plastic Square Quad Flat Pack (SQFP) with gull-wing leads.
- Leadframe and header/paddle constructed of copper.
- External leads plated with tin-lead and internally spot plated with silver.
- A silver-epoxy die attach was employed.
- Lead-locking provisions (anchors) were present at all pins.
- Pins 101 and 122 were not connected.
- Thermosonic wirebonding using 1.1 mil O.D. gold wire.
- Dicing was by sawing (full depth).

### **Die Process and Design:**

- The device was fabricated by an N-well CMOS process which utilized selective oxidation. No epi was present on the P substrate.
- A patterned, spun-on, polyimide die coat was present over the entire die.
- Overlay passivation consisted of a layer of silicon-nitride over a layer of glass.
- Two levels of silicon-doped aluminum interconnect were defined by dry-etch techniques. Metal 2 employed a titanium-nitride barrier and metal 1 employed a titanium-nitride cap and barrier. Standard vias and contacts were used (no plugs).
- Interlevel dielectric consisted of two depositions of silicon-dioxide (glass). The first layer was subjected to an etchback. No spin-on-glass (SOG) was used.

## **TECHNOLOGY DESCRIPTION (continued)**

- Intermediate glass consisted of a BPSG reflow glass over densified oxides.
- A single layer of dry-etched polysilicon was used to form all gates. No silicide was employed on the poly.
- Standard implanted N+ and P+ source/drain diffusions were used. Only the slightest evidence of LDD sidewall spacers was visible. The minimum gate lengths indicate that an LDD process was employed.
- No buried contacts (poly-to-diffusion) were employed.
- No redundancy fuses were noted.
- Numerous small cell arrays were present on the device. The largest array was delayered for documentation. It appeared to be a FIFO type cell layout which employed ten transistors per cell. Cell size was 17.8 X 17.8 microns.
- Design features: Beveled and slotted metal 2 bus lines (short and long slots), array of vias and contacts. Various size and shape vias and contacts. Some elongated contacts were employed with metal 1.

## ANALYSIS RESULTS I

### Assembly:

### Figures 1 - 10

#### **Questionable Items:<sup>1</sup>**

- Small cracks radiated from the corners of the header/paddle and a gap was present underneath (Figure 6).

#### **General Items:**

- The devices were encapsulated in 208-pin plastic Square Quad Flat Pack (SQFP).
- Overall package quality: No defects were found on the external portions of the package. External pins were well formed and tinning of the leads was complete. No significant gaps were present at lead exits. Internally small cracks radiated from the corners of the header and a gap was present underneath the header. The cracks and gap reduce overall package strength and integrity.
- Leadframe: Copper (Cu) leadframe externally tinned with tin-lead (SnPb) solder and plated internally with silver (Ag).
- Die attach: A silver-epoxy die attach of normal quality. Die attach coverage was incomplete due to use of a screened on dot deposition method.
- Die dicing: Die separation was by sawing (full depth) with normal quality and workmanship.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## **ANALYSIS RESULTS I (continued)**

- Wirebonding: Thermosonic ball bond method using 1.1 mil O.D. gold wire. Wirebond placement was good. Bond pad pitch was tight with a pad spacing of only 11 microns; however, wire spacing was normal and no problems were seen. Ball bonds were well formed and intermetallic formation was complete. Bond pull strengths were good (see page 11) with no bond lifts.
- Die coat: A spun-on, patterned, polyimide die coat was present over the die surface. Coverage was good.

## ANALYSIS RESULTS II

### Die Process:

Figures 11 - 38

### **Questionable Items:<sup>1</sup>**

- Metal 2 aluminum thinned up to 95 percent<sup>2</sup> at vias (Figure 21). The barrier helped maintain continuity.
- Metal 1 aluminum thinned up to 85 percent<sup>2</sup> at poly contacts (Figure 27). This thinning was a result of "folds" in the metal at contact edges.

**Special Features:** None.

### **General Items:**

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P substrate. No epi was used.
- Process implementation: Die layout was clean and efficient. Alignment was good at all levels and no damage, process defects, or contamination was found.
- Design features: Beveled and slotted metal 2 bus lines (short and long slots), array of vias and contacts. Various size and shape vias and contacts. Some elongated contacts were employed with metal 1.
- Overlay passivation: A layer of silicon-nitride over a layer of glass. Overlay integrity tests indicated defect-free passivation. Edge seal was also good as the passivation extended past the metal at the die edge. A cutout was present in the passivation around the die perimeter to prevent cracking of the passivation from dicing.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

*<sup>2</sup>Seriousness depends on design margins.*

## **ANALYSIS RESULTS II (continued)**

- Metallization: Two levels of metallization, each consisting of silicon-doped aluminum. Metal 2 employed a titanium-nitride barrier and metal 1 employed a titanium-nitride cap and barrier.
- Metal patterning: Both metal levels were defined by a dry etch of good quality.
- Metal step coverage: Metal 2 aluminum thinned up to 95 percent at vias. The barrier helped maintain continuity. Thinning was worse at one side of the via; although, thinning of 80 percent still occurred on the other side. Metal 1 aluminum thinned up to 85 percent at poly contacts. Again, the barrier helped maintain continuity. The severe thinning at these contacts was due to folds in the metal coverage rather than the typical thinning seen. Folds were also noted in the metal at diffusion contacts; however, the folds were not as wide but just as deep in some cases (similar to micro cracks). MIL-STD-883D, Method 2018.3 allows up to 70 percent thinning for contacts of this size.
- Metal defects: No voiding, notching or neckdown of the metals was found. Metal lines were widened at vias and contacts and vias and contacts were completely surrounded by metal. Virtually no silicon nodules were present following metal 2 removal; however, silicon nodules occupied up to 50 percent of metal 1 line widths. Silicon nodules which occupy >50 percent of the line widths, increase the metal's susceptibility to electromigration.
- Contact defects: None. Via and contact cuts appeared to be defined by a two step etch. Standard vias and contacts (no plugs) were used. No significant overetching of the vias or contacts was found.
- Interlevel dielectric: Two depositions of silicon-dioxide were employed. No spin on glass (SOG) was used. The first layer of silicon dioxide was subjected to an etchback for planarization. No problems were found.
- Intermediate glass: A BPSG reflow glass over densified oxide. The BPSG was reflowed prior to contact cuts. No problems were found in this layer.

## **ANALYSIS RESULTS II (continued)**

- Polysilicon: A single layer of dry-etched polysilicon (no silicide) was used to form all gates on the die. Definition of the poly layer was normal-to-poor. The width varied slightly over gate oxide and local oxide regions.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere.
- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of the transistors. As mentioned, the sidewall spacers were removed so almost no evidence of an LDD process was left; however, the minimum gate lengths on this device require an LDD process. No problems were found.
- No buried contacts were used on the device.
- No redundancy fuses were present.
- Wells: N-wells were used in a P substrate. No epi layer was used. Definition of the wells was normal.
- Numerous small cell arrays were present on the device. The largest array was delayed for documentation. It appeared to be a FIFO type cell layout which employed ten transistors per cell. Cell size was 17.8 x 17.8 microns.
- ESD test: One device was subjected to an ESD test. All pins passed pulses of  $\pm 4000V$ .

## **PROCEDURE**

The devices were subjected to the following analysis procedures:

External inspection

ESD test

X-ray

Package section

Decapsulation

Internal optical inspection

SEM of assembly features

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Removal aluminum 2 and inspect

Delayer to metal 1

SEM inspection of metal 1

Remove aluminum 1 and inspect

Delayer to polysilicon and inspect

Die sectioning (90° for SEM)\*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal/Poor

**DETAIL OF EVALUATION**

Package integrity	NP (cracks and gap at header)
Package markings	G
Lead conformity	G
Lead plating quality	G
Die placement	G
Die attach quality	N
Wire spacing	N
Wirebond placement	G
Wirebond quality	N
Dicing quality	N
Wirebond method	Thermosonic ball bonds using 1.1 mil gold wire
Die attach method	Silver-filled epoxy
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	N
Passivation integrity	G
Metal definition	G
Metal integrity	P <sup>1</sup>
Metal registration	N
Contact coverage	G
Contact registration	G

<sup>1</sup>Metal 2 aluminum thinning up to 95 percent at vias and metal 1 aluminum thinning up to 85 percent at poly contacts.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

**PACKAGE MARKINGS**

**TOP**

q logic™ corp.  
ISP10002405034  
JA T9N43B  
US PAT# 5,276.807 9523EAI

**WIREBOND STRENGTH**

Wire material: 1.1 mil diameter gold  
Die pad material: aluminum  
Material at package post: silver

**Sample #**

# of wires tested: 31  
Bond lifts: 0  
Force to break - high: 8.0g  
- low: 6.0g  
- avg.: 6.9g  
- std. dev.: 0.7

**CONTACT MATRIX**

	<b>Metal 2</b>	<b>Metal 1</b>	<b>Poly</b>	<b>N+</b>	<b>P+</b>
Metal 2:		X			
Metal 1:	X		X	X	X

## DIE MATERIAL ANALYSIS

Passivation:	Silicon-nitride over glass.
Metal 2:*	Silicon-doped aluminum with a titanium-nitride barrier.
Interlevel dielectric:	Two depositions of silicon-dioxide.
Metal 1:*	Silicon-doped aluminum employing a titanium-nitride cap and barrier.
Intermediate oxide:	BPSG reflow glass containing 3.8 wt. percent boron and 6.4 wt. percent phosphorus.

*\* There is no known method for determining the exact amount of silicon and copper in the aluminum on a finished die.*



## VERTICAL DIMENSIONS

Die thickness: (0.3 mm) 11.5 mils

Die coat: 6 microns

### Layers:

Passivation 2: 0.6 micron

Passivation 1: 0.4 micron

Metal 2 - aluminum: 1.0 micron

- barrier: 0.07 micron (approximate)

Interlevel dielectric - glass 2: 0.45 micron

- glass 1: 0.2 - 1.1 micron

Metal 1 - cap: 0.04 micron (approximate)

- aluminum: 0.55 micron

- barrier: 0.1 micron

Intermediate glass: 0.6 micron (average)

Poly: 0.3 micron

Local oxide: 0.45 micron

N+ source/drain: 0.25 micron

P+ source/drain: 0.3 micron

N- well: 4 microns

## INDEX TO FIGURES

ASSEMBLY	Figures 1 - 10
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PHYSICAL DIE STRUCTURES	Figures 14 - 34
COLOR PROCESS DRAWING	Figure 35
EXAMPLE CELL LAYOUT	Figure 36 and 37
TYPICAL I/O BUFFER CIRCUIT LAYOUT	Figure 38

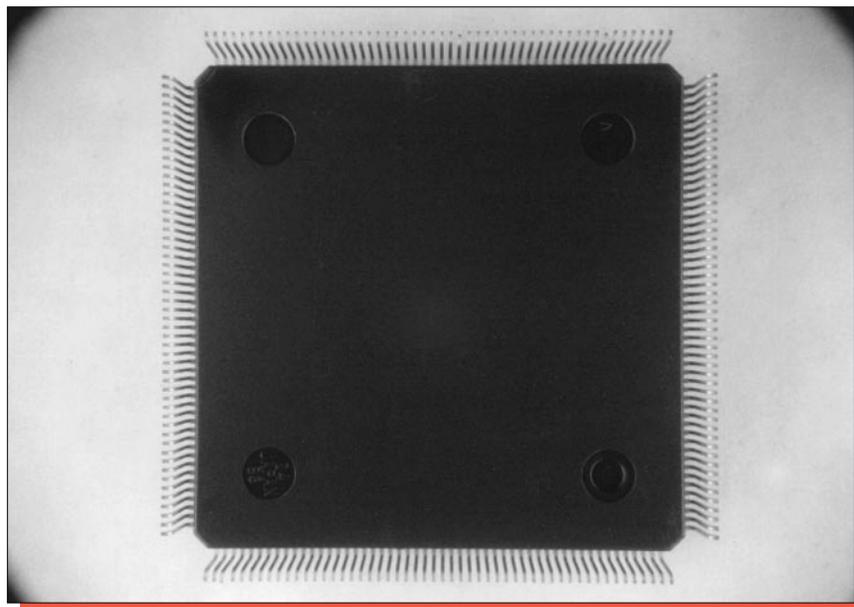


Figure 1. Package photographs of the QLogic ISP1000. Mag. 2.5x.

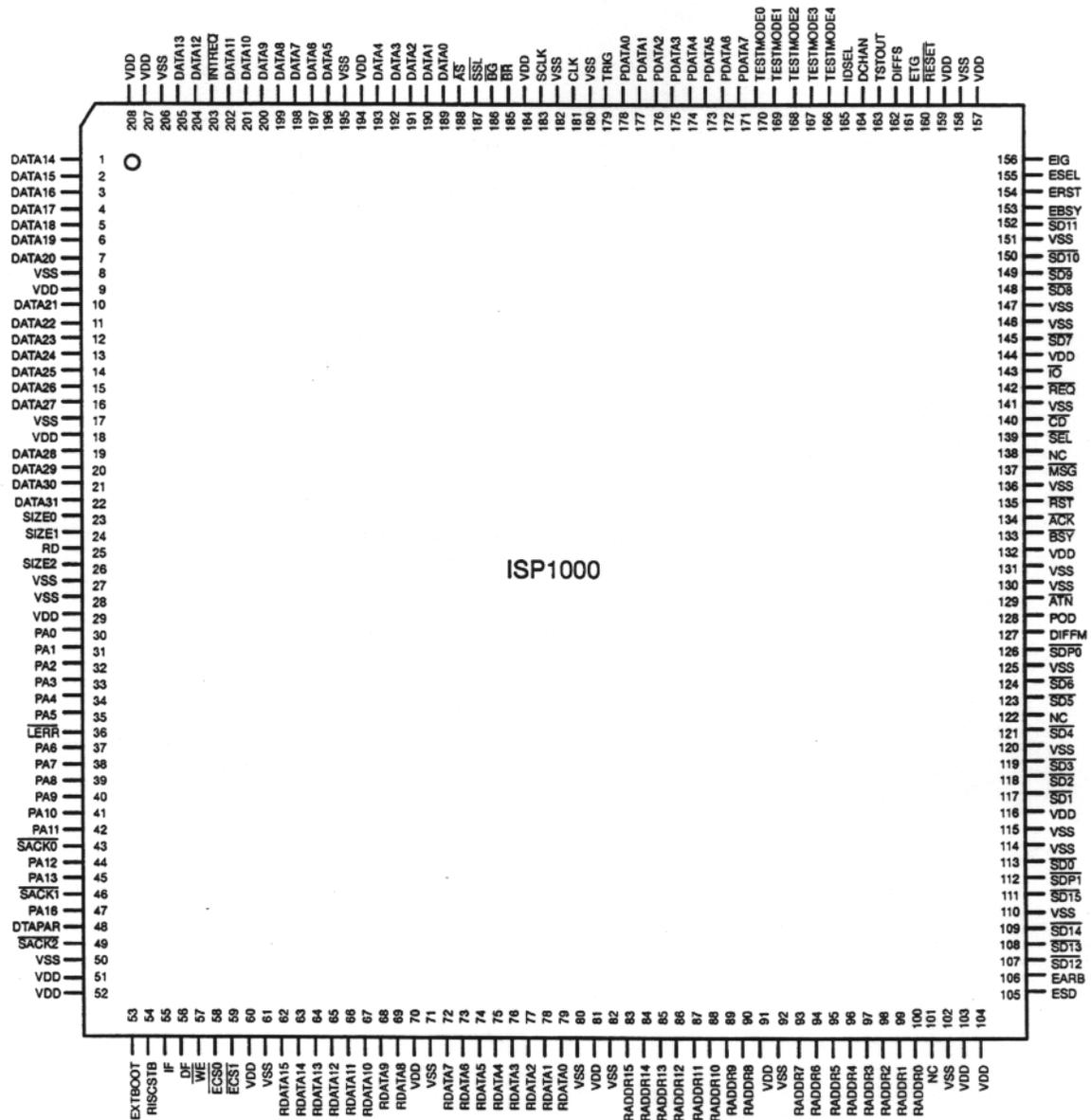


Figure 1a. Pinout diagram of the QLogic ISP1000.

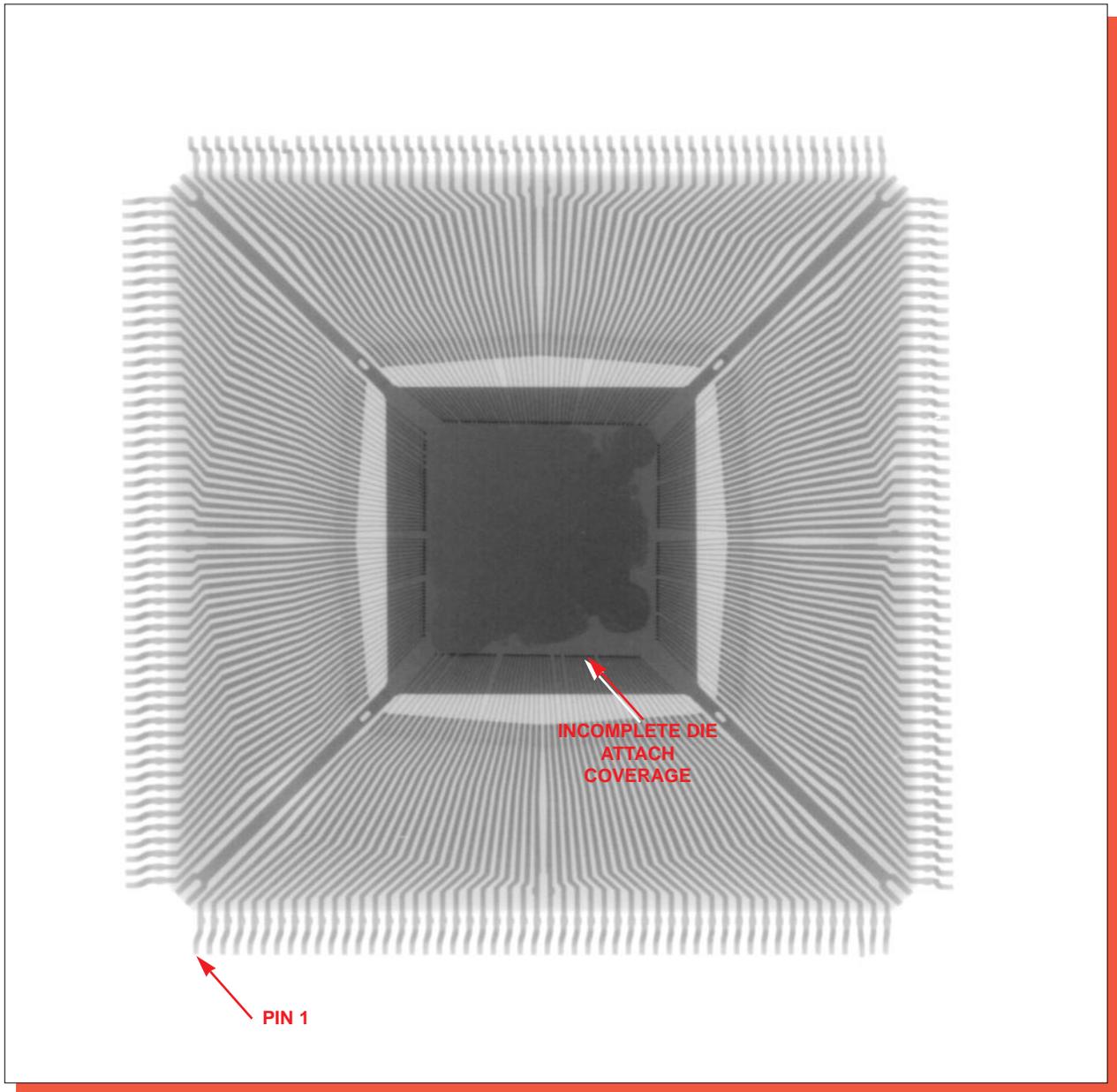


Figure 2. Topological x-ray view of the package. Mag. 4x.

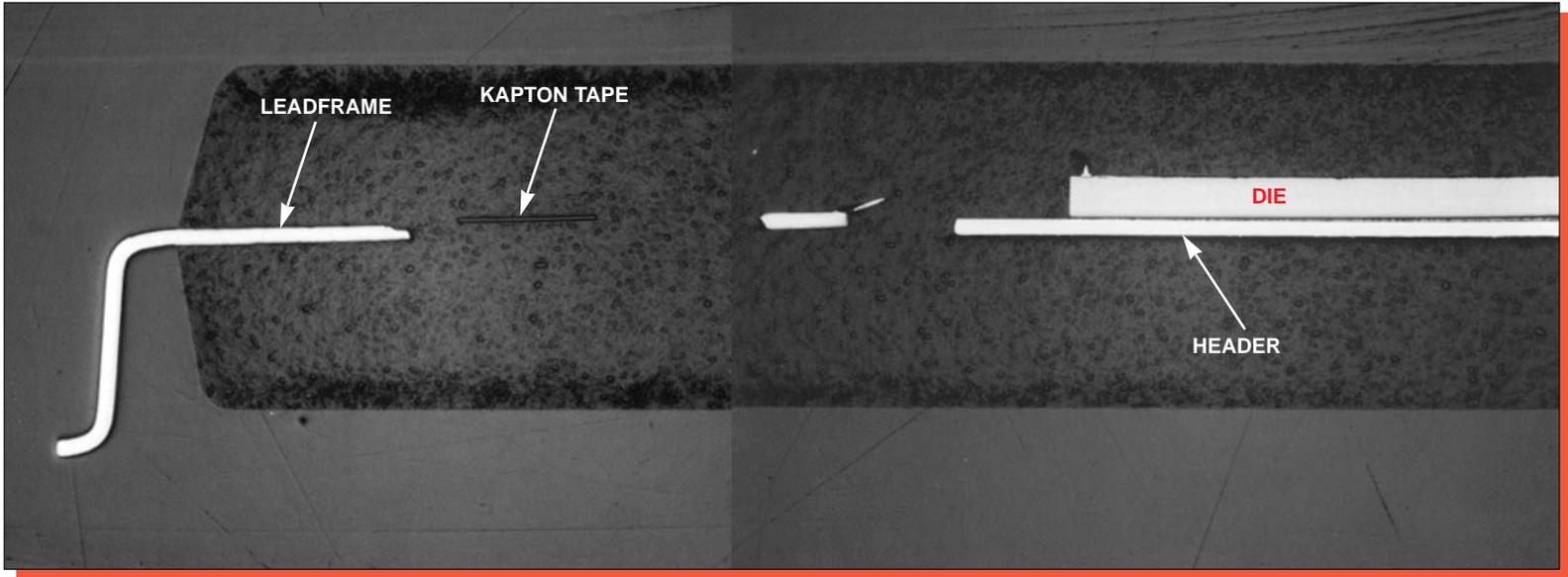
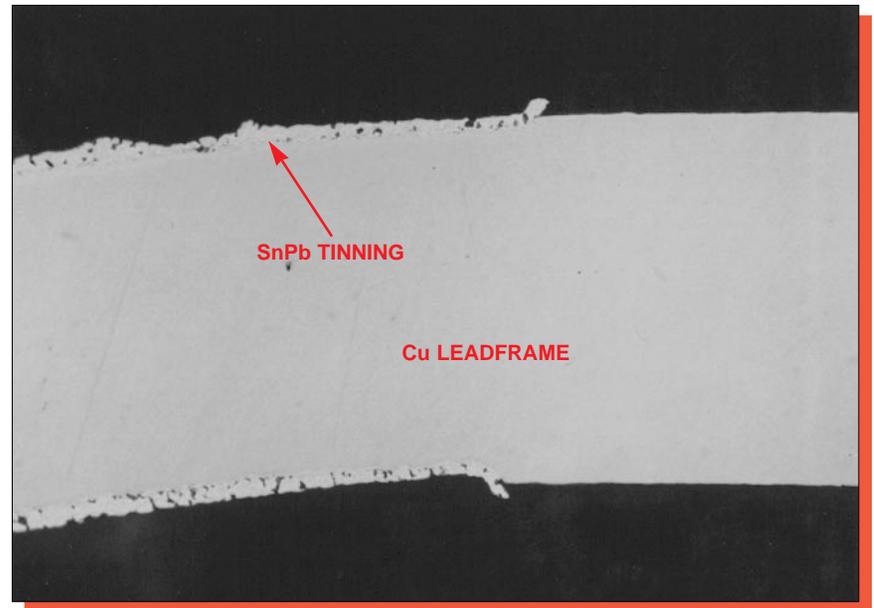


Figure 3. Section view of the package illustrating general construction. Mag. 13x.

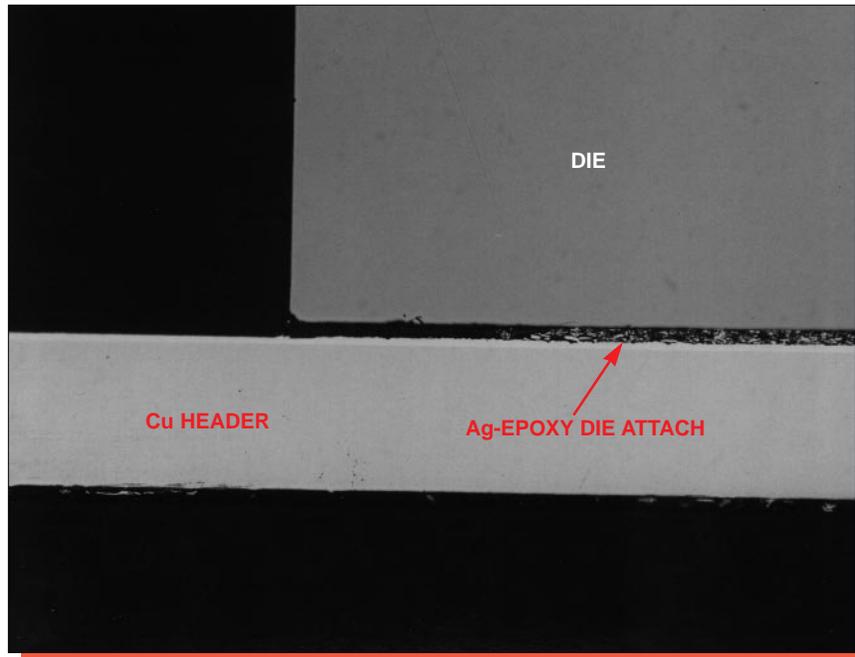


Mag. 80x

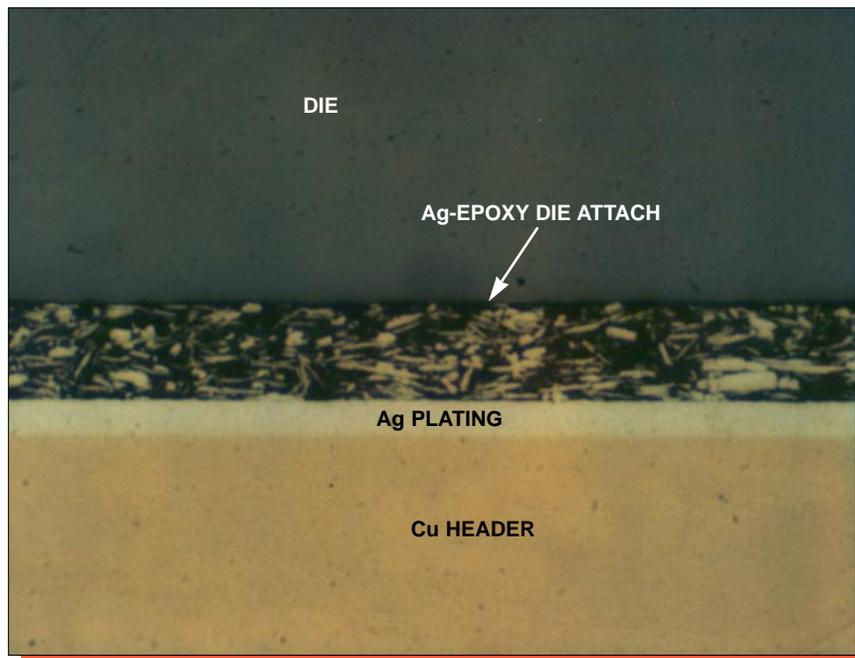


Mag. 320x

Figure 4. Section views illustrating lead forming and lead exit.



Mag. 130x



Mag. 800x

Figure 5. Section views illustrating dicing and die attach quality.

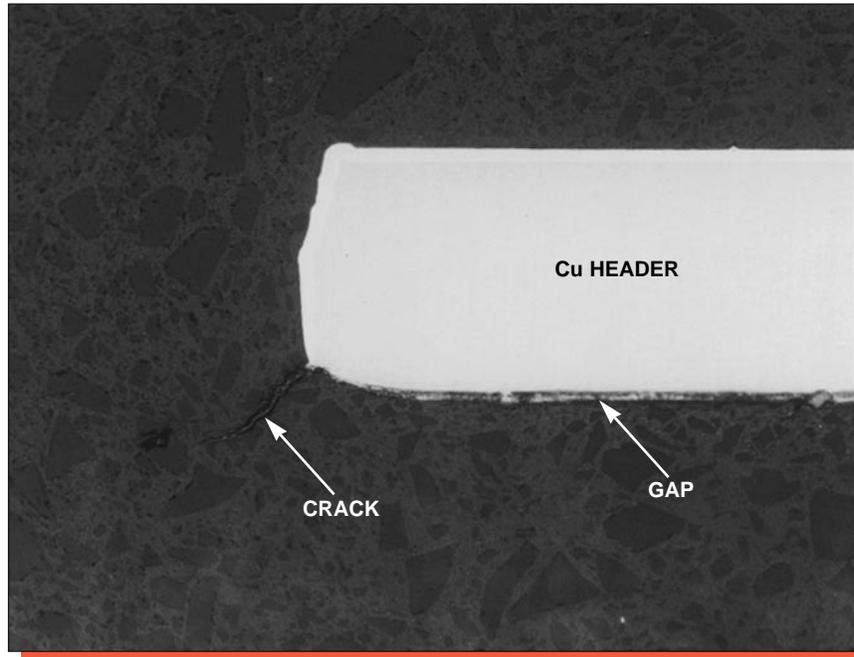


Figure 6. Section view of a crack in the plastic package. Mag. 200x.

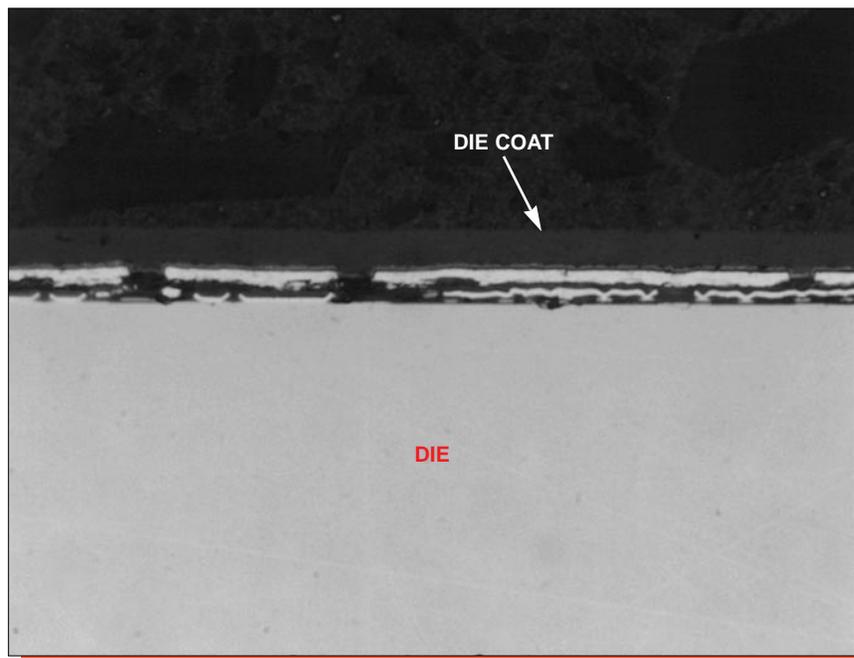
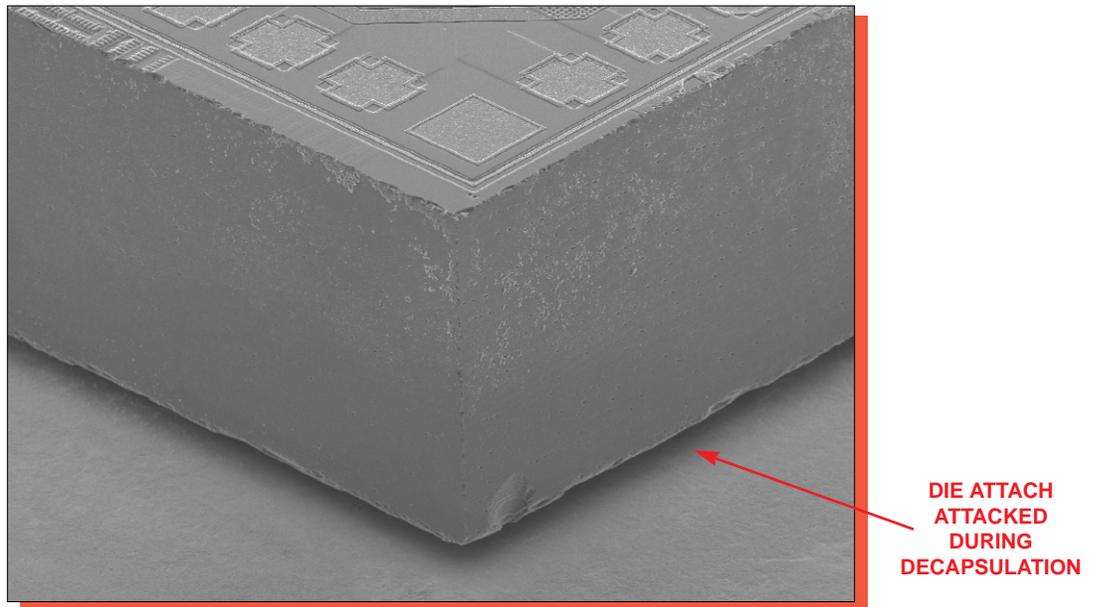
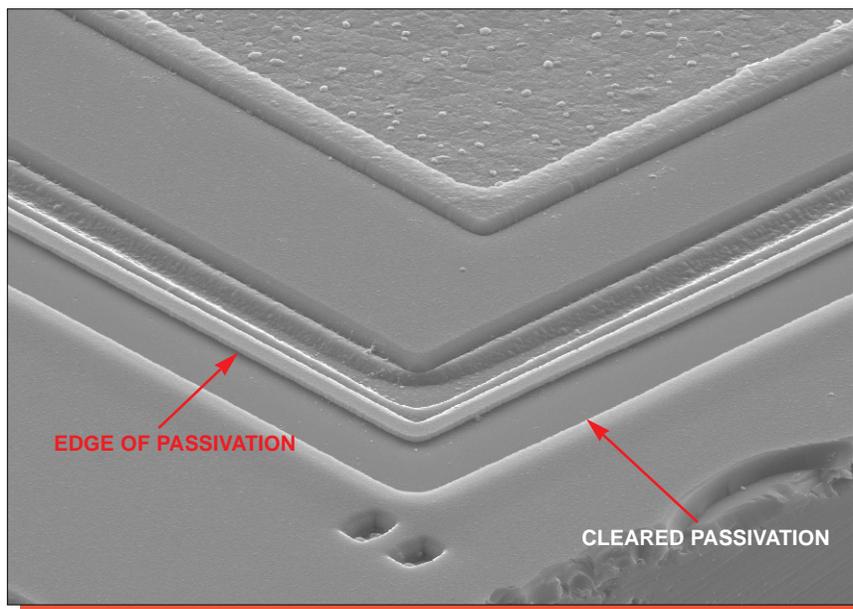


Figure 7. Section view of the die coat. Mag. 800x.

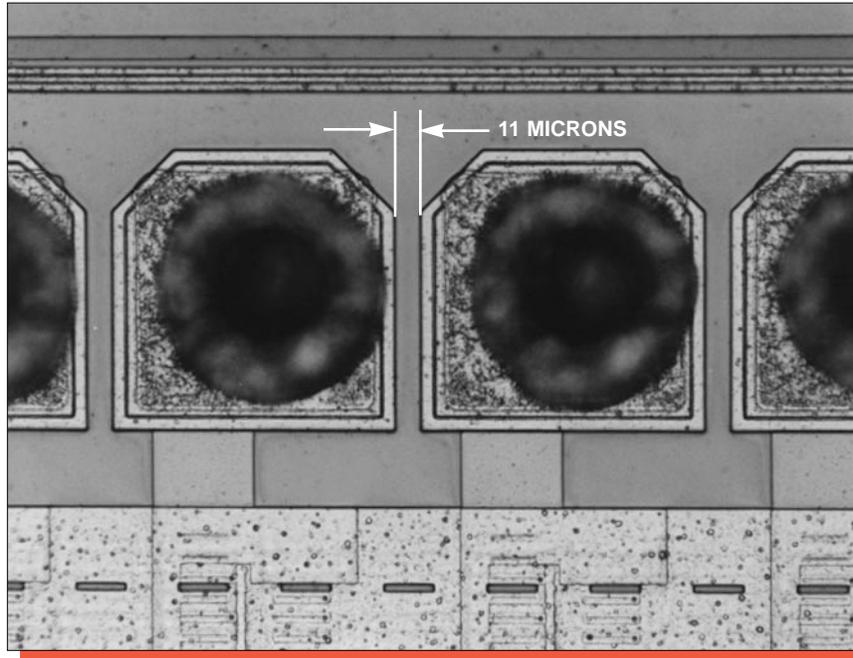


Mag. 120x

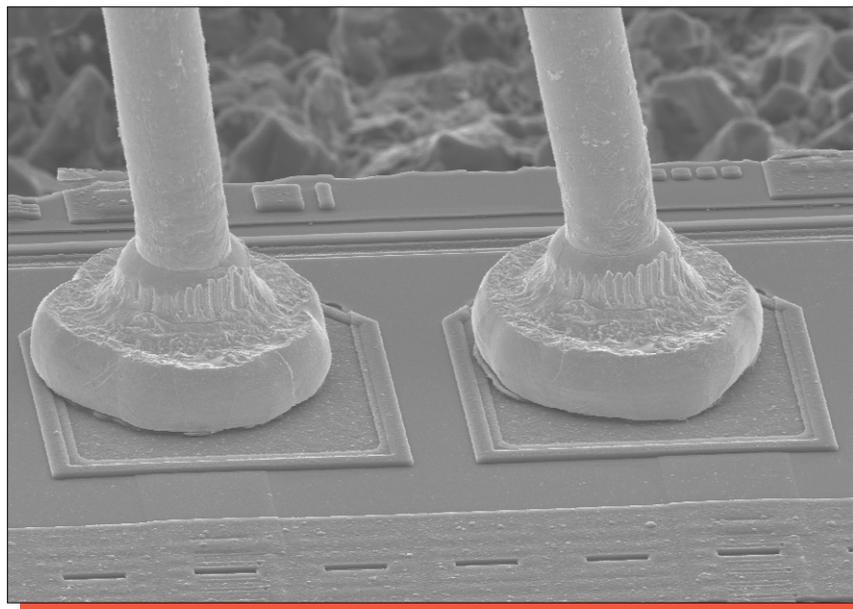


Mag. 1200x

Figure 8. SEM views of a die corner and edge seal. 60°.

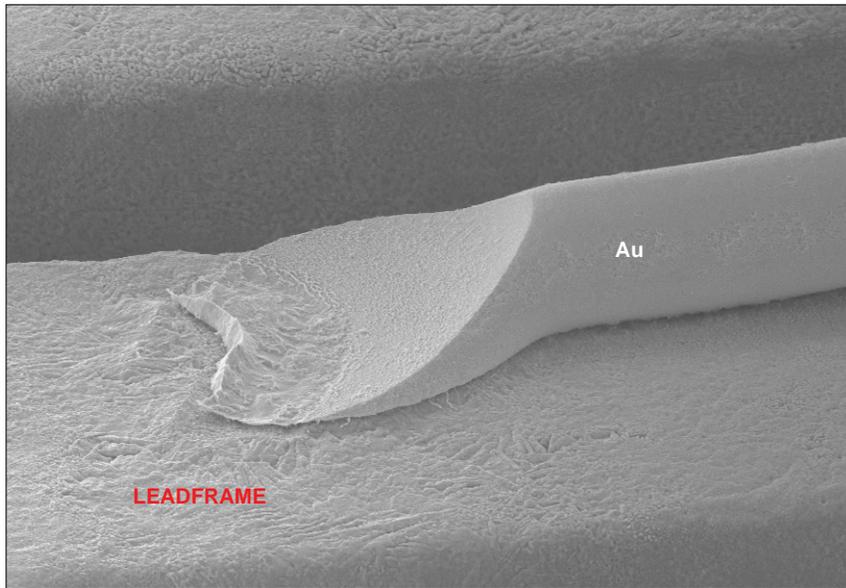


Mag. 320x

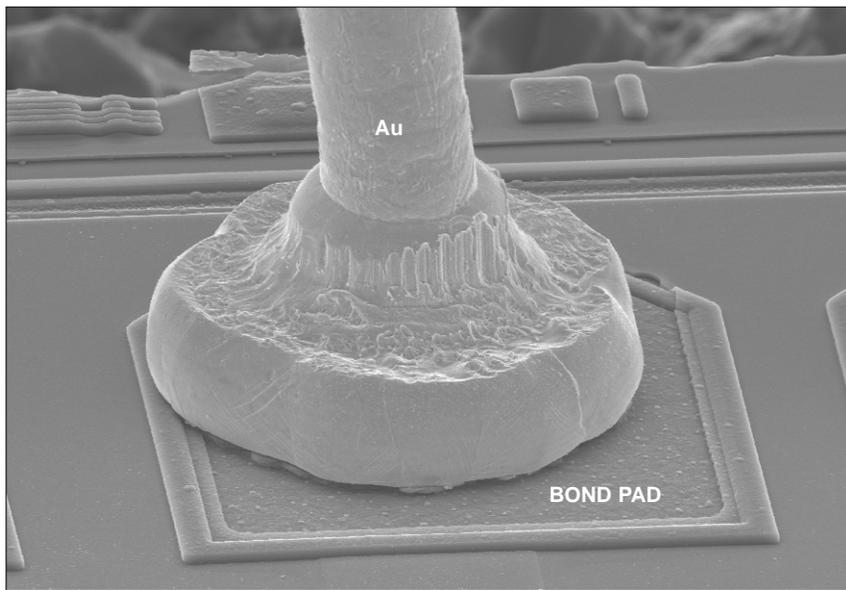


Mag. 440x, 60°

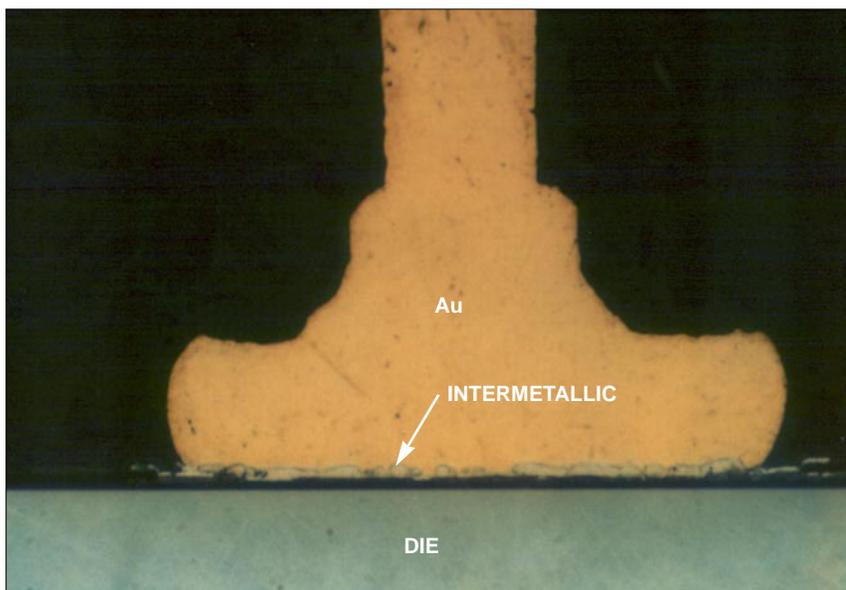
Figure 9. Optical and SEM views illustrating minimum bond pad spacing and pitch.



Mag. 650x, 60°



Mag. 750x, 60°



intermetallic delineated,  
Mag. 800x

Figure 10. SEM and section views of typical wirebonds.

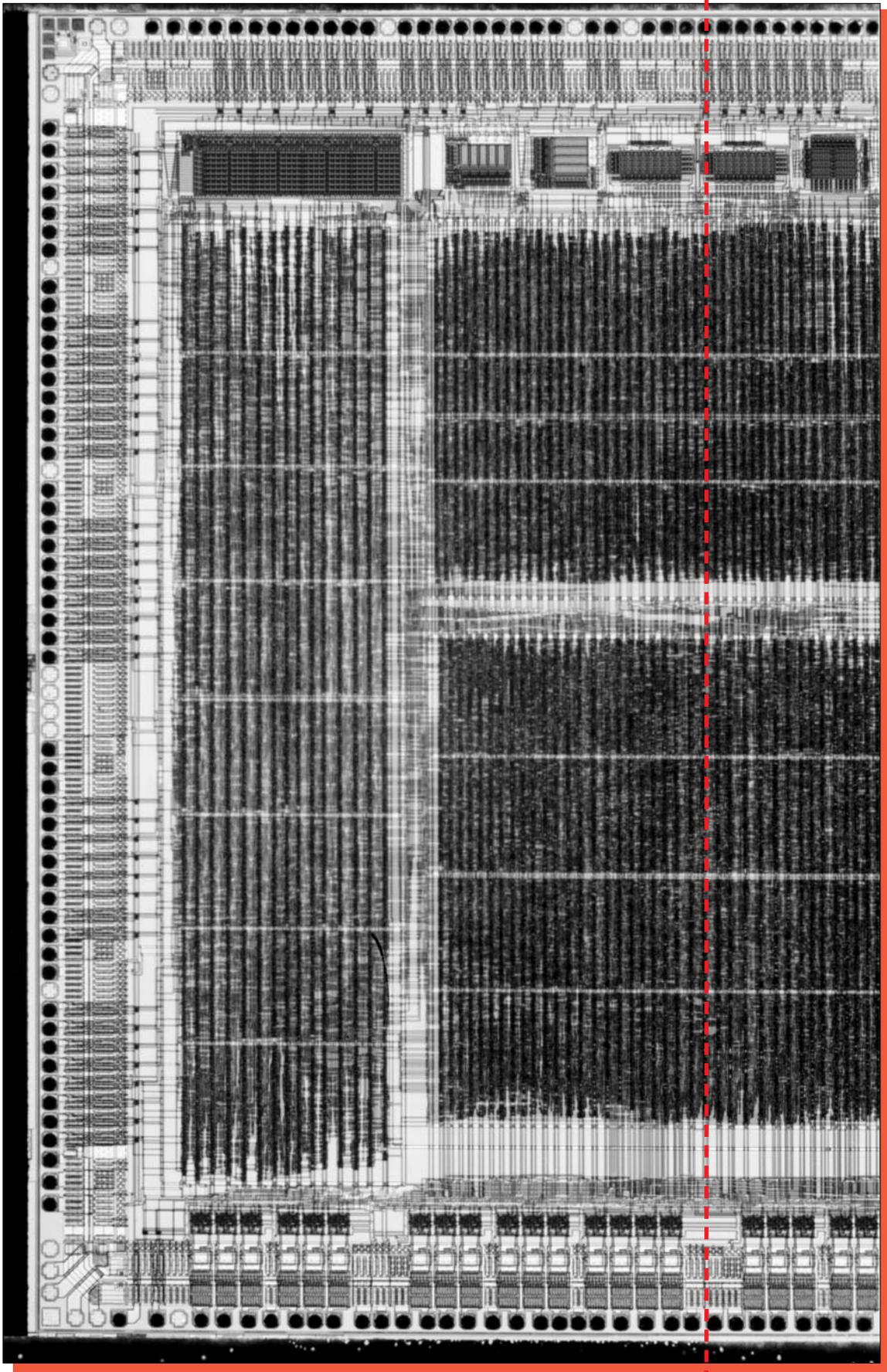


Figure 11. Portion of the QLogic ISP1000 die photograph. Mag. 26x.

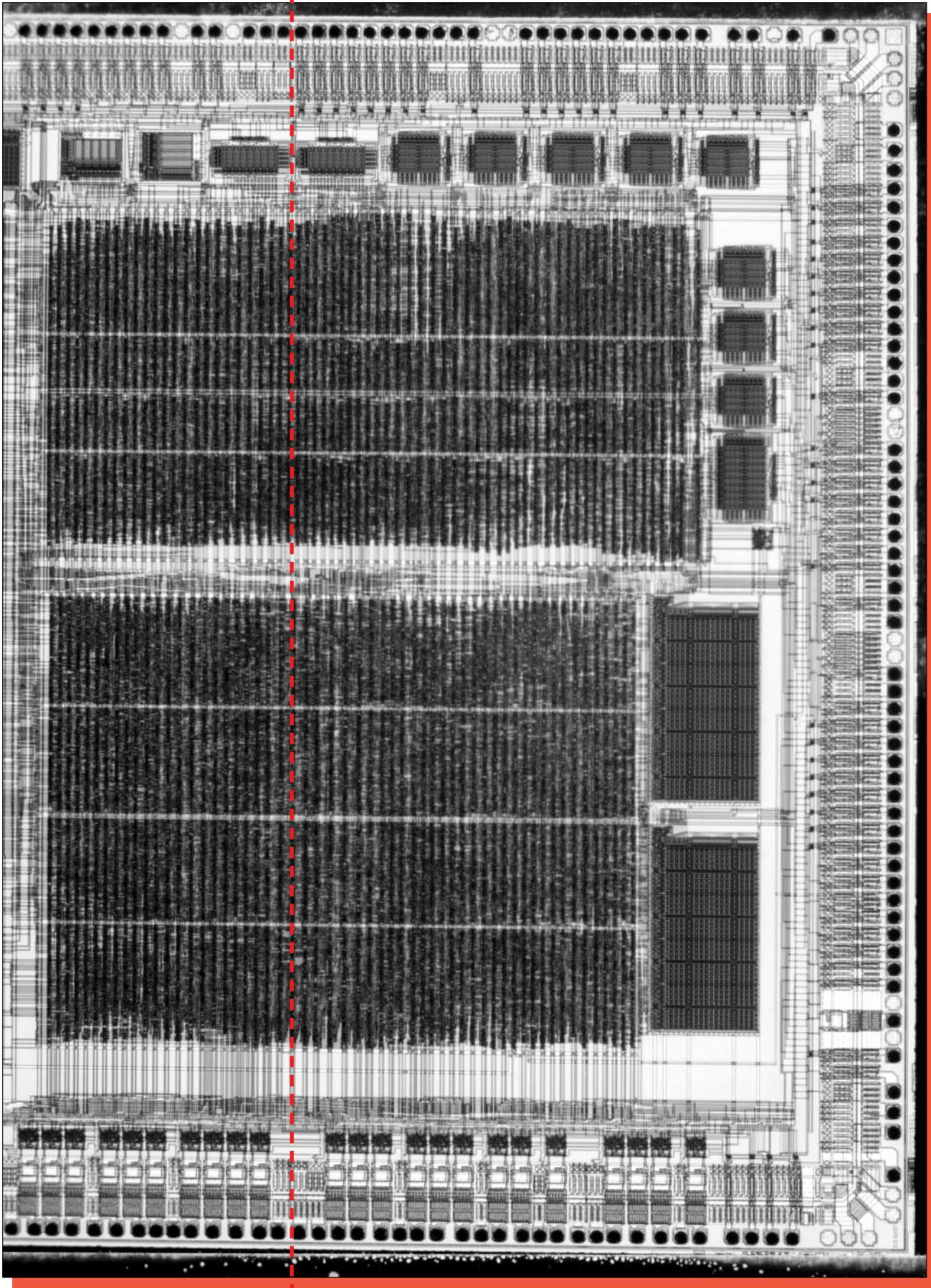


Figure 11a. Remaining portion of the QLogic ISP1000 die photograph. Mag. 26x.

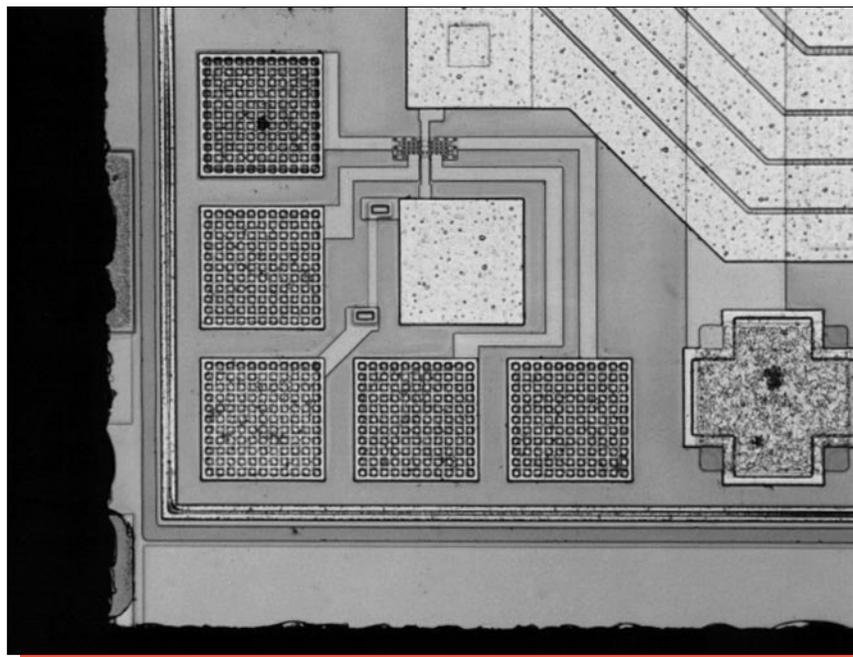
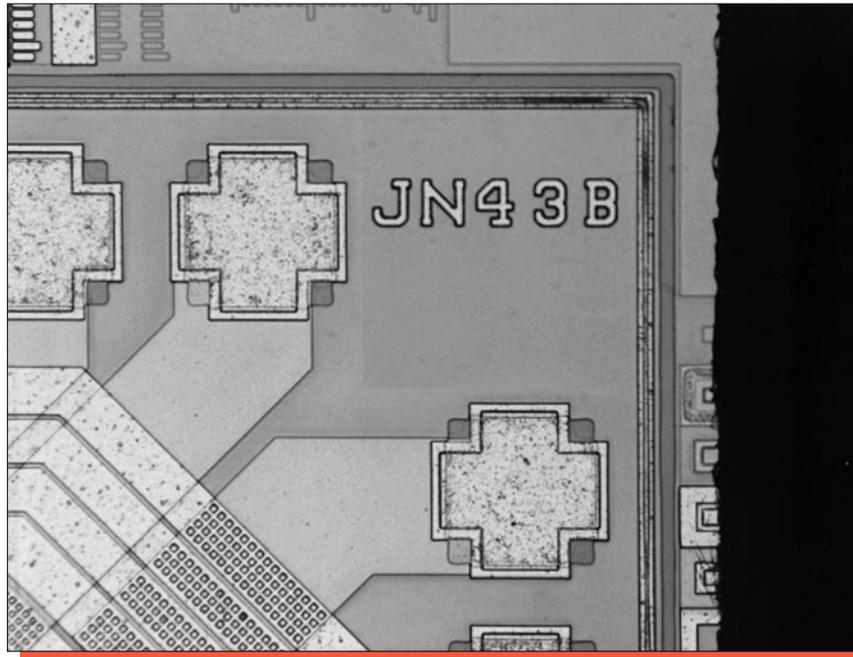
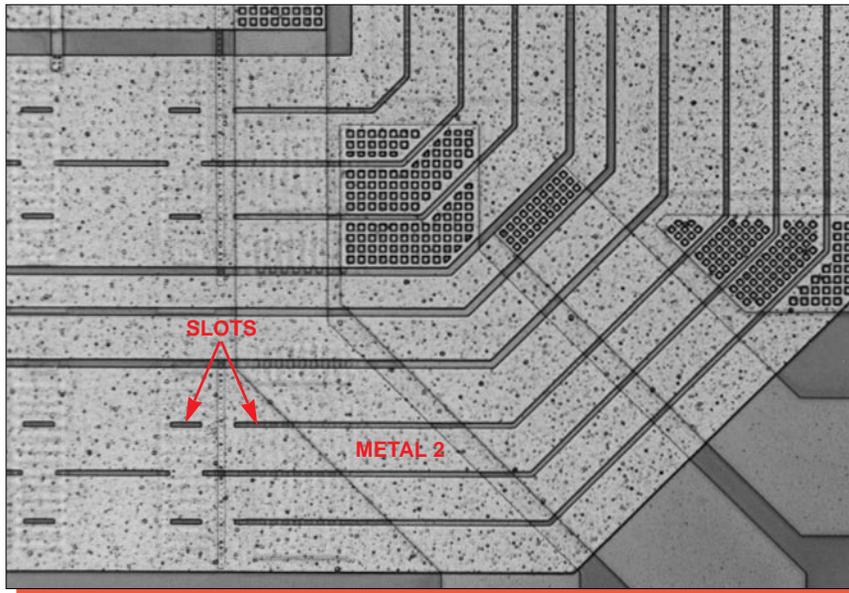
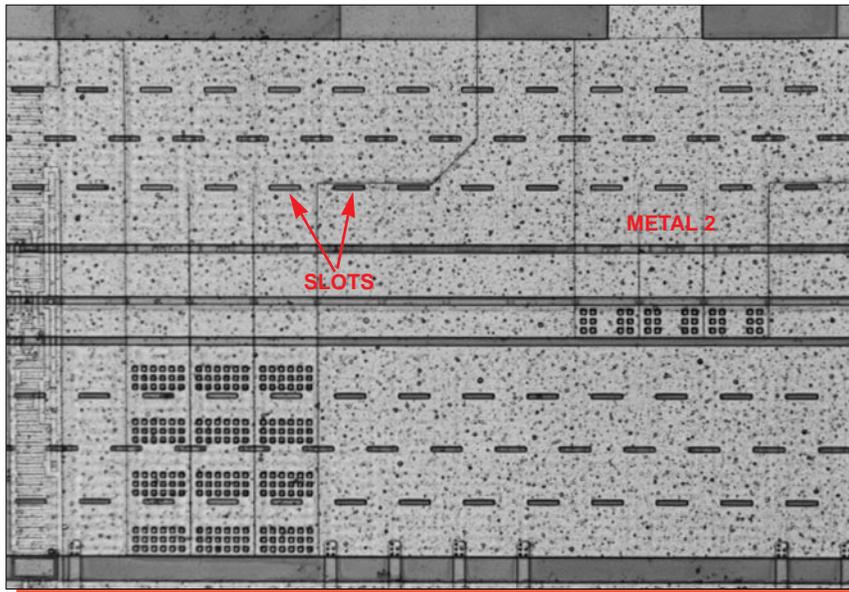


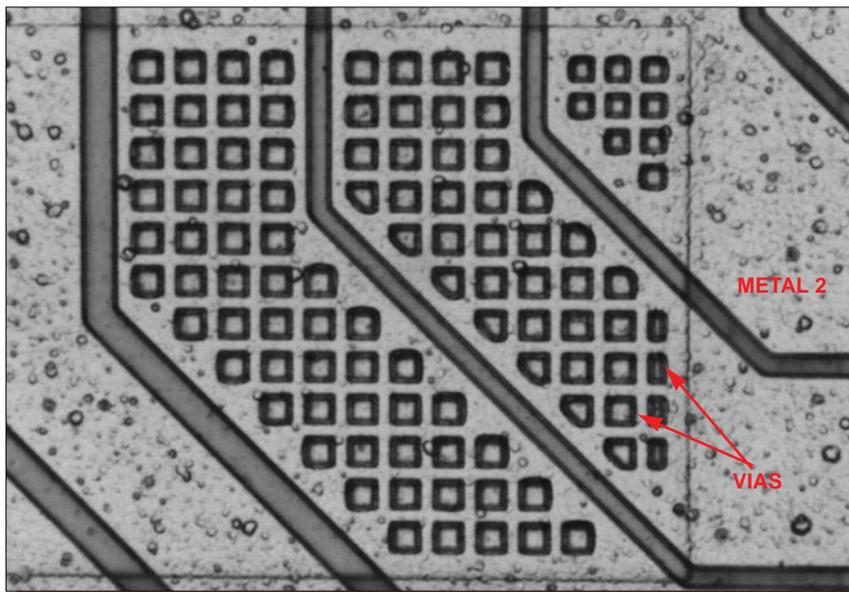
Figure 12. Die identification markings and test devices. Mag. 200x.



Mag. 200x



Mag. 200x



Mag. 800x

Figure 13. Optical views illustrating slotted/beveled bus line and arrays of vias.

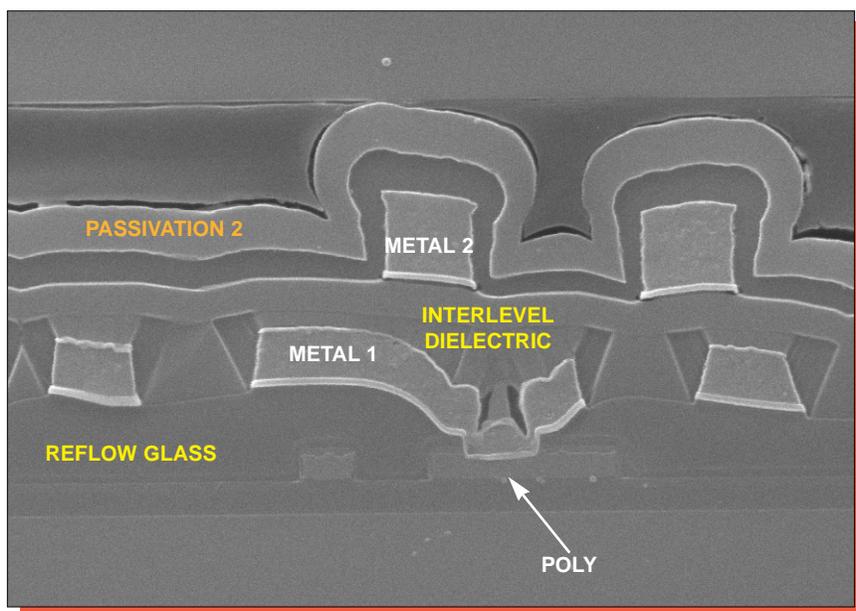
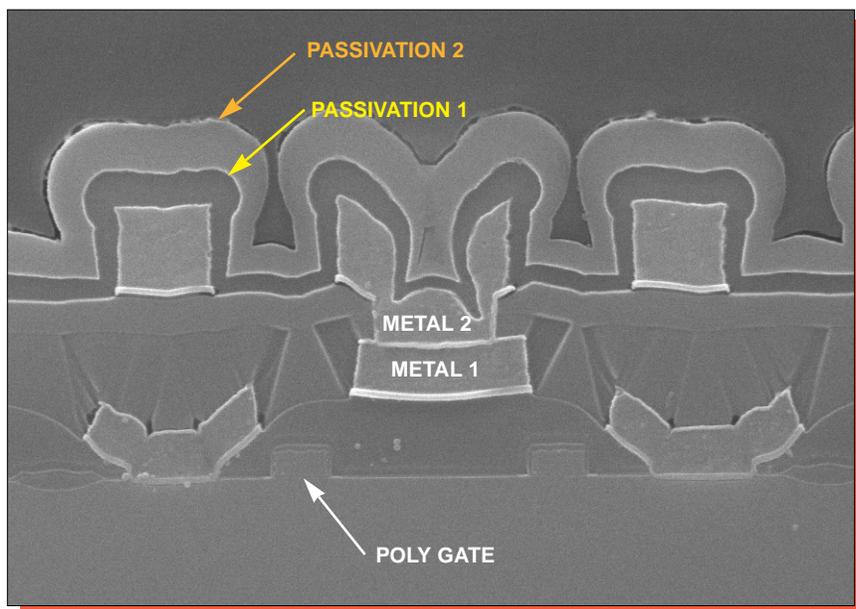


Figure 14. Glass etch section views illustrating general device structure. Mag. 11,000x.

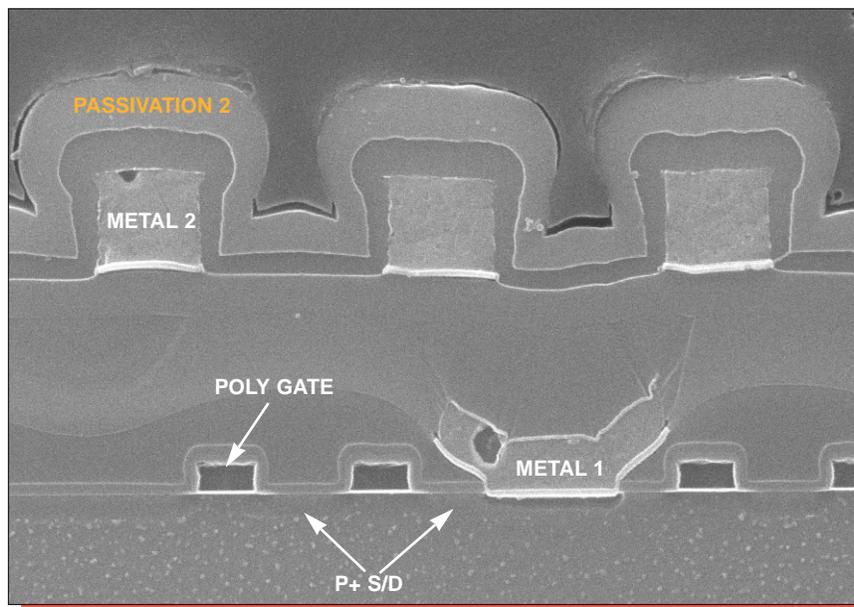
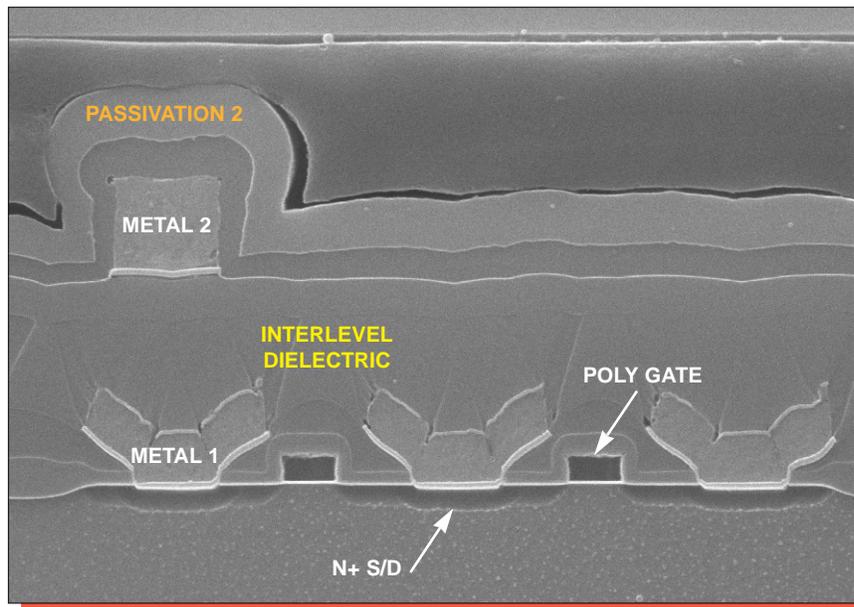
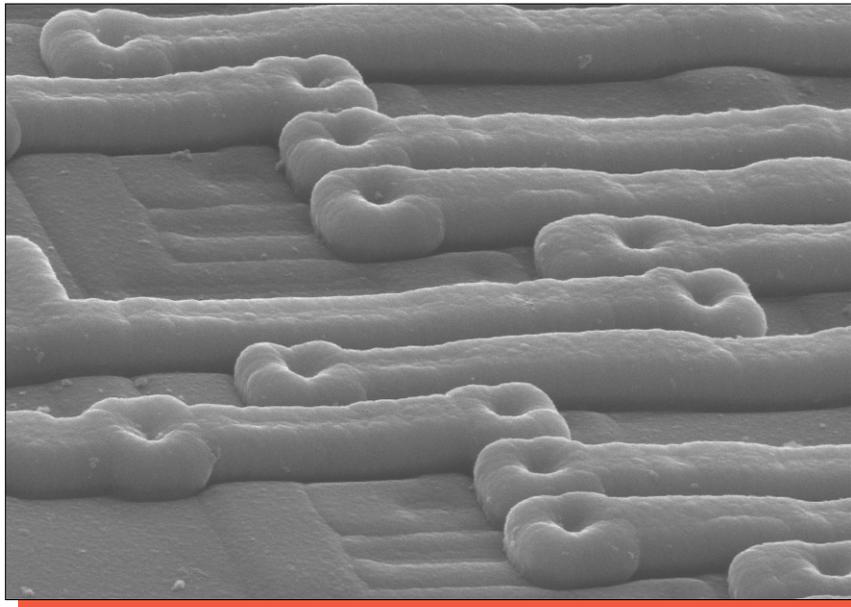
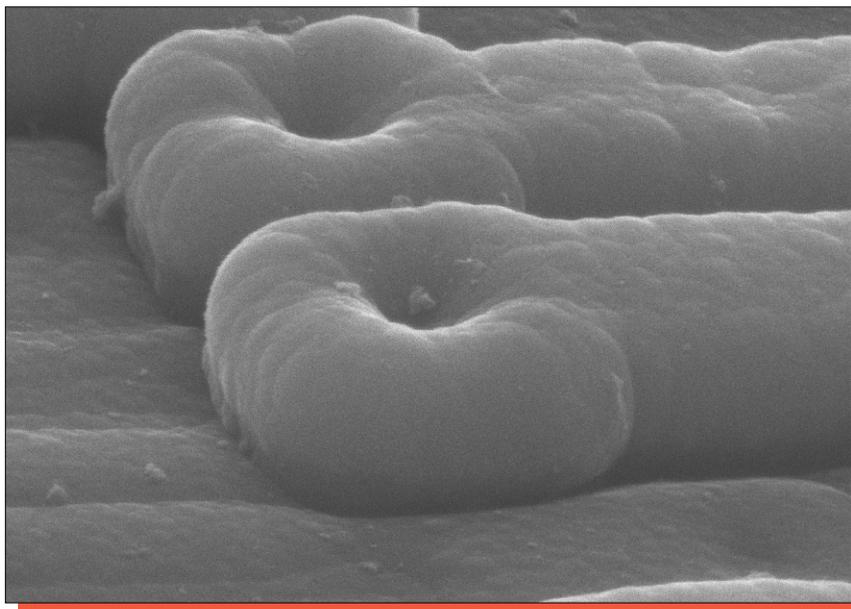


Figure 15. Silicon etch section views illustrating general device structure.  
Mag. 12,000x.

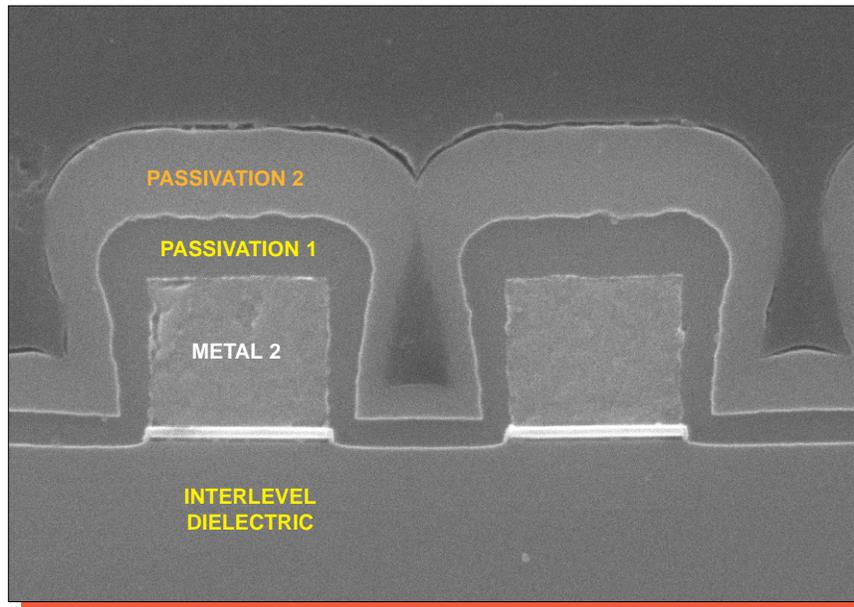


Mag. 4400x

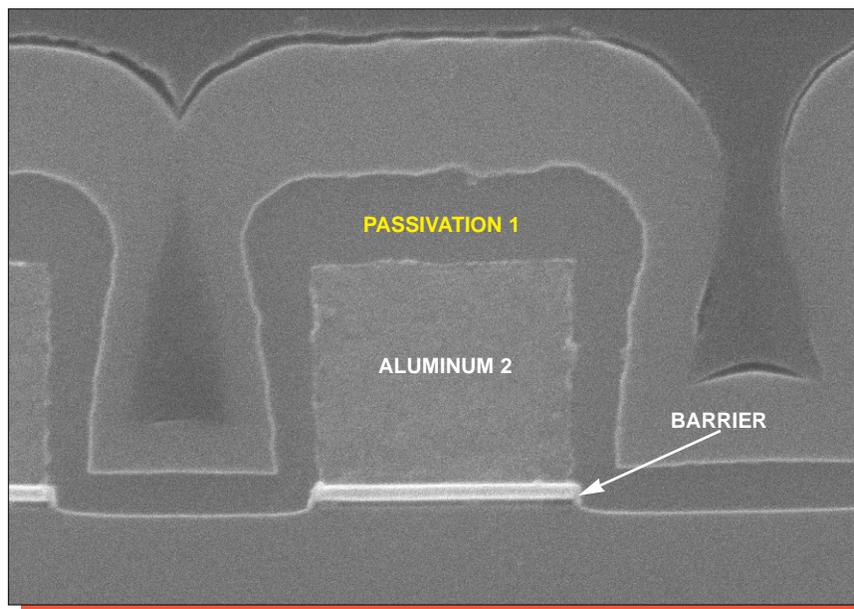


Mag. 13,500x

Figure 16. SEM views of general overlay passivation coverage. 60°.

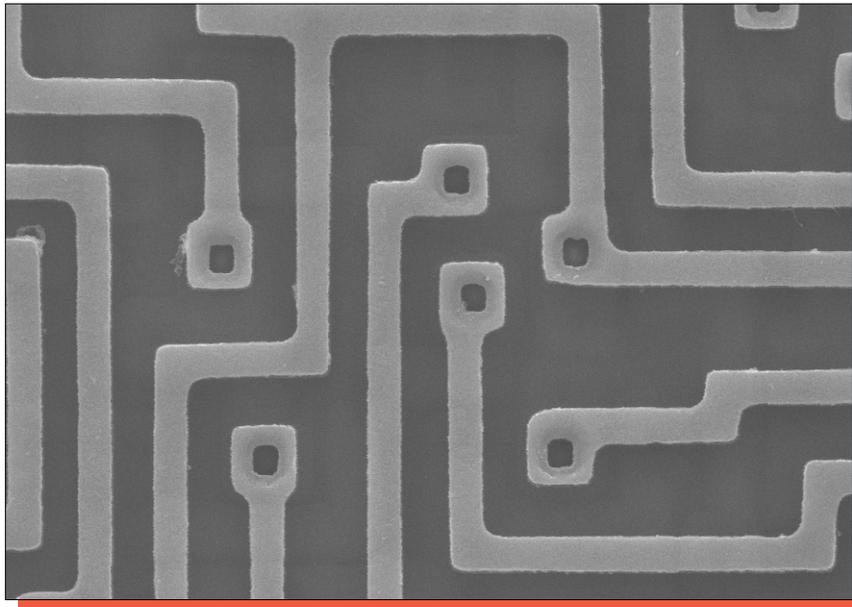


Mag. 20,000x

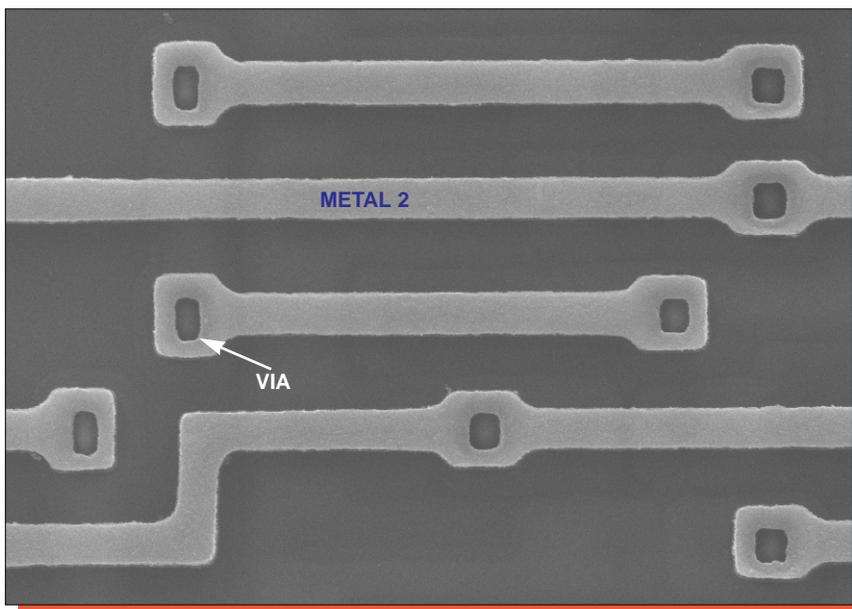


Mag. 30,000x

Figure 17. SEM section views of metal 2 line profiles.

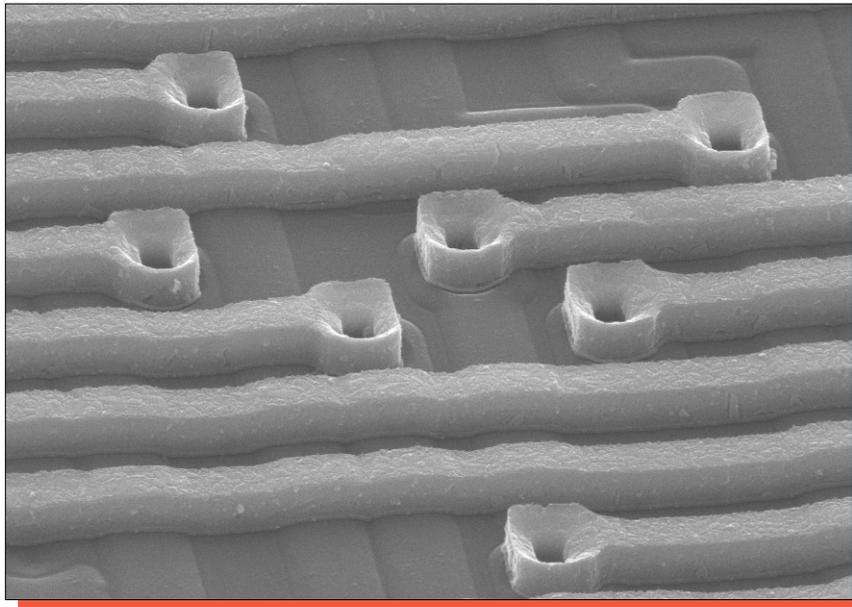


Mag. 4000x

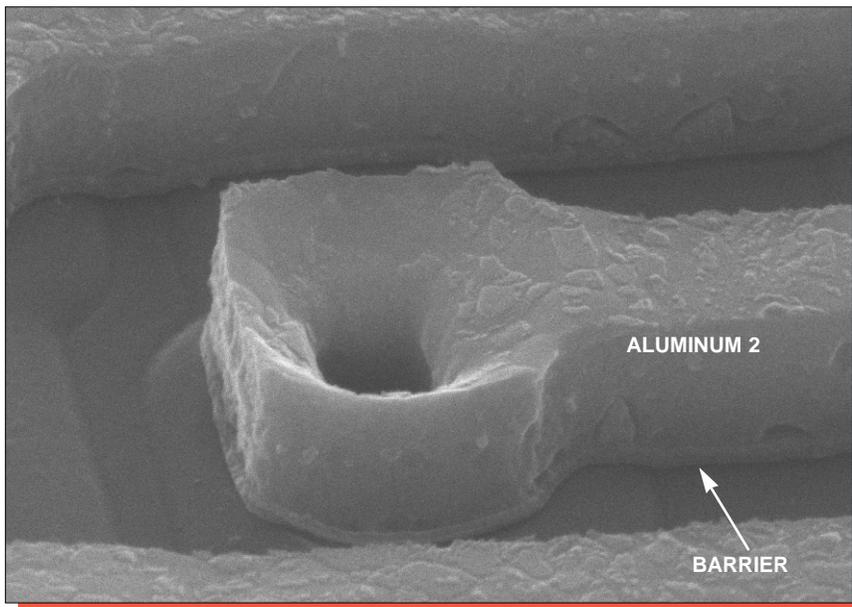


Mag. 5000x

Figure 18. Topological SEM views of metal 2 patterning. 0°.

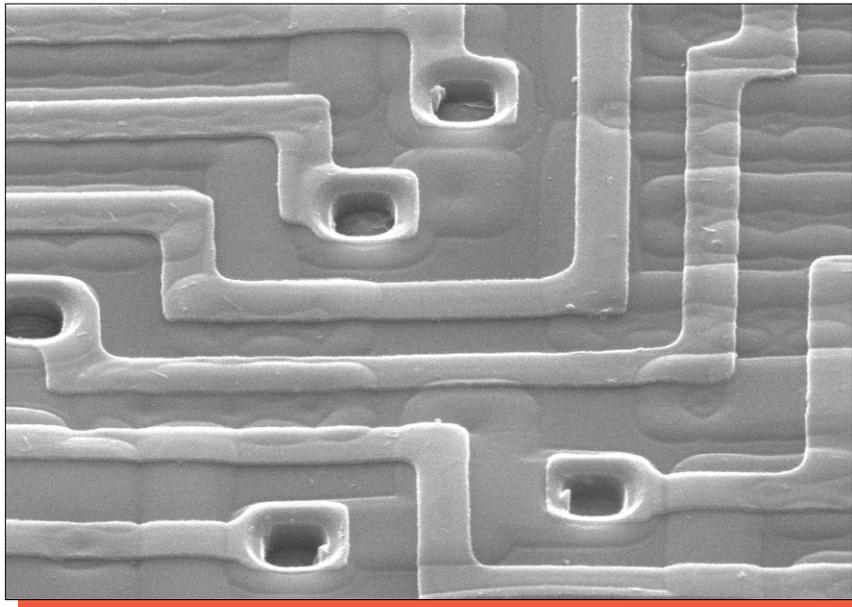


Mag. 5500x

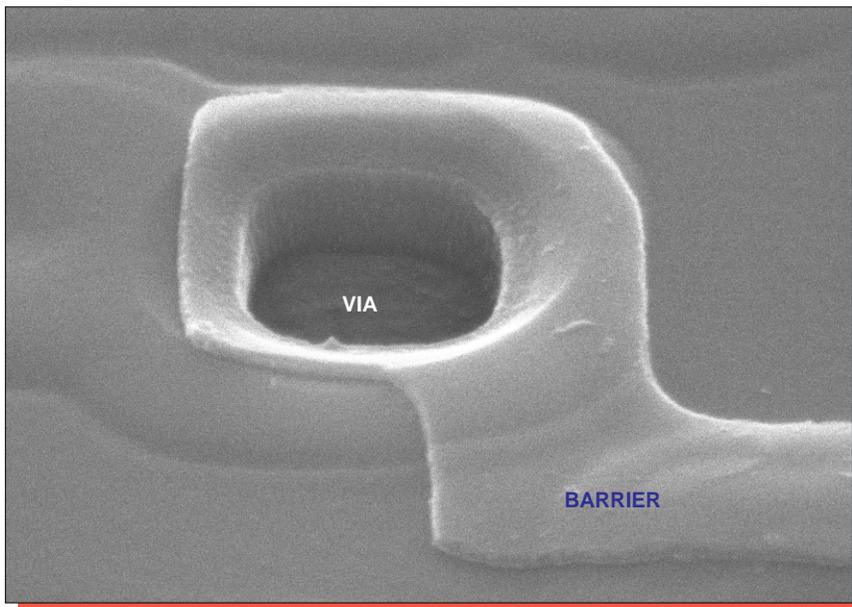


Mag. 20,000x

Figure 19. SEM views of general metal 2 integrity. 60°.

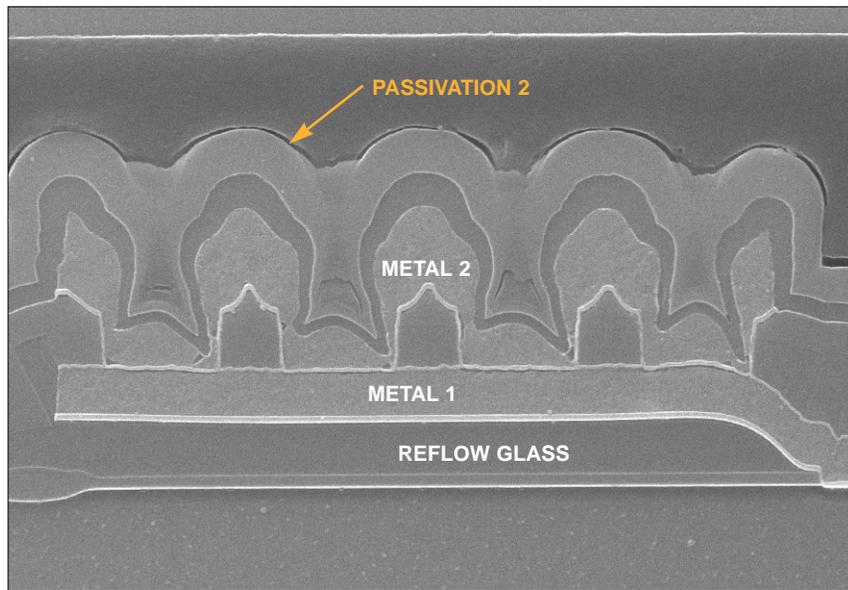


Mag. 5000x

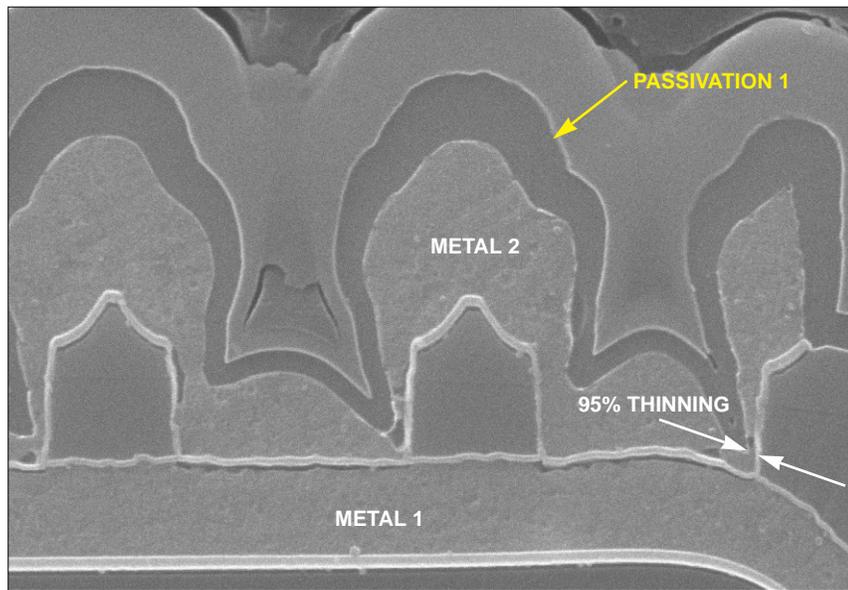


Mag. 20,000x

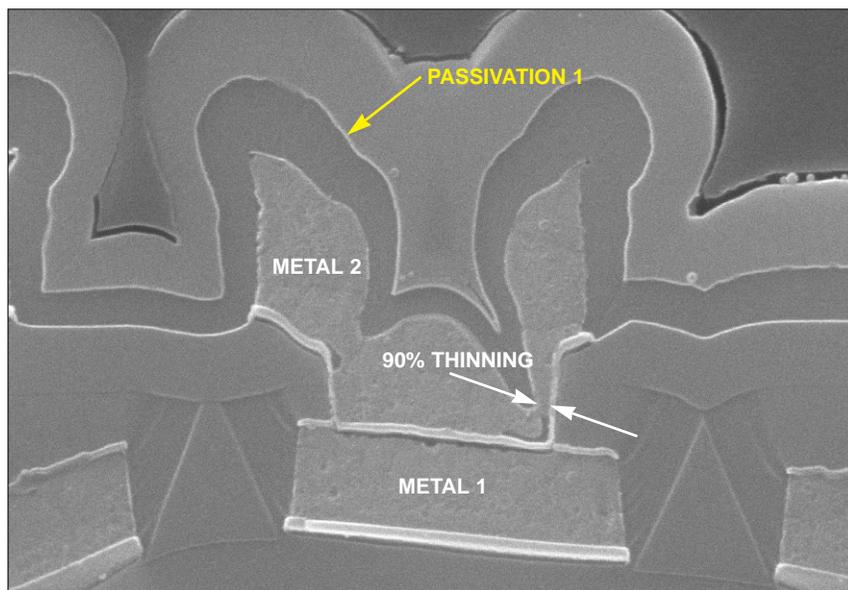
Figure 20. SEM views of metal 2 barrier coverage. 45°.



Mag. 10,000x

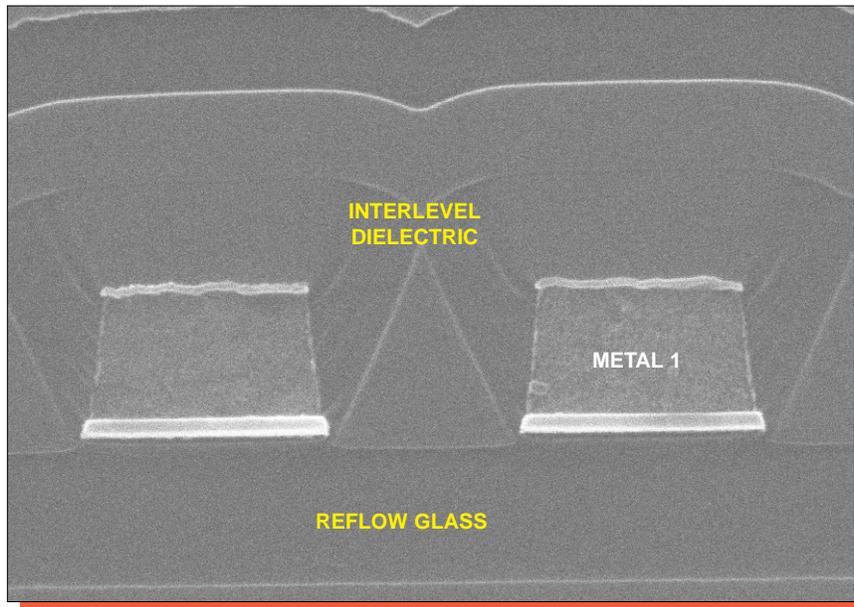


Mag. 20,000x

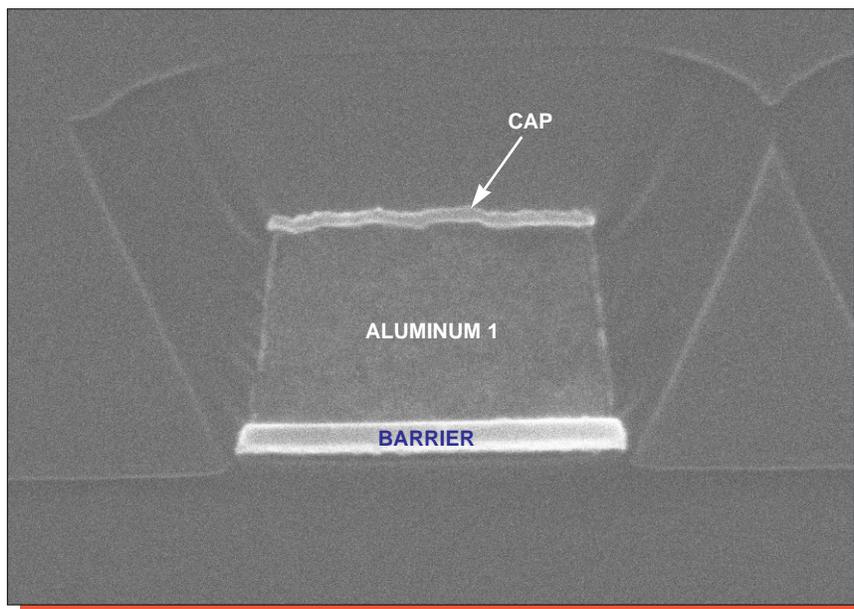


Mag. 20,000x

Figure 21. SEM section views of typical vias.

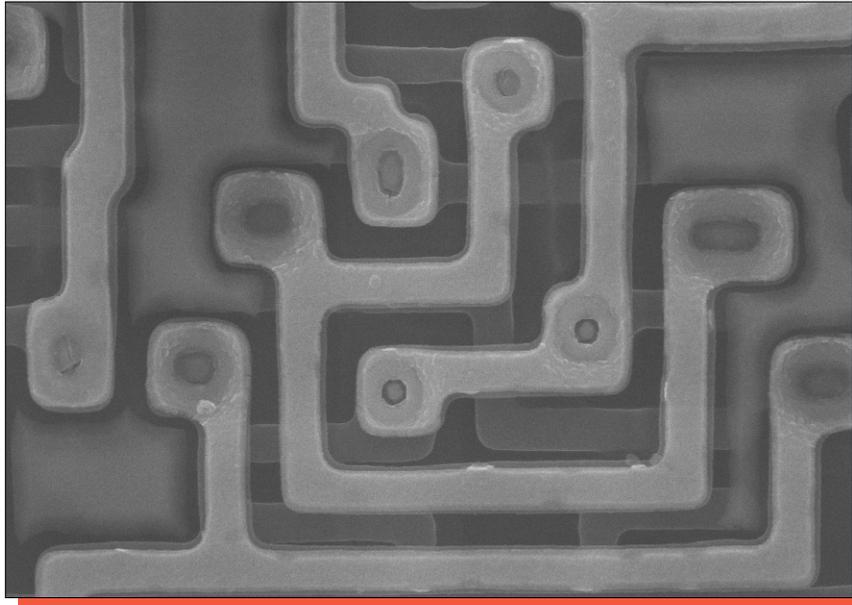


Mag. 30,000x

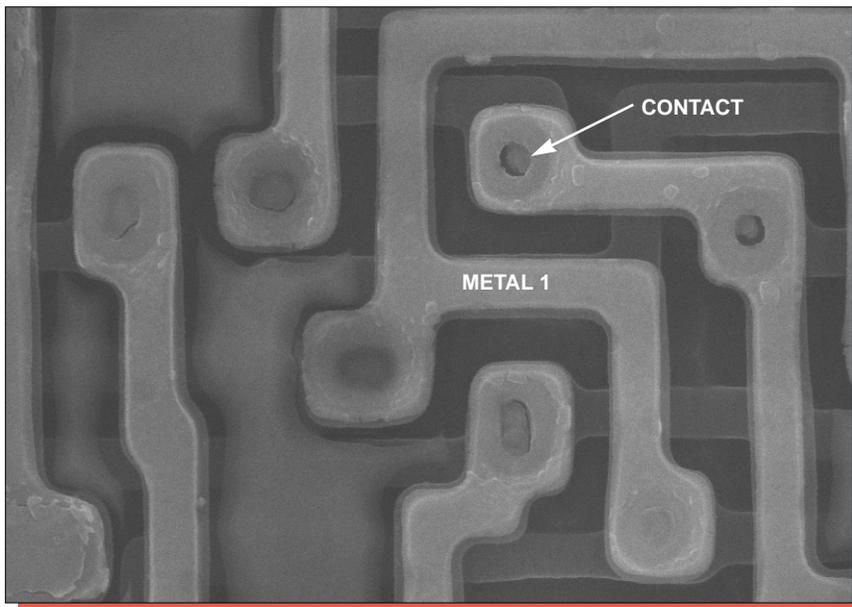


Mag. 45,000x

Figure 22. SEM section views of metal 1 line profiles.

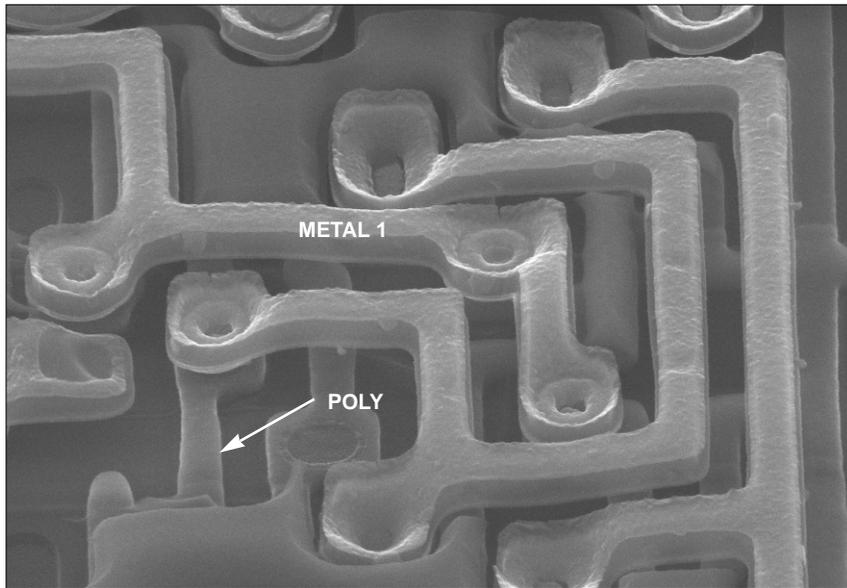


Mag. 6000x

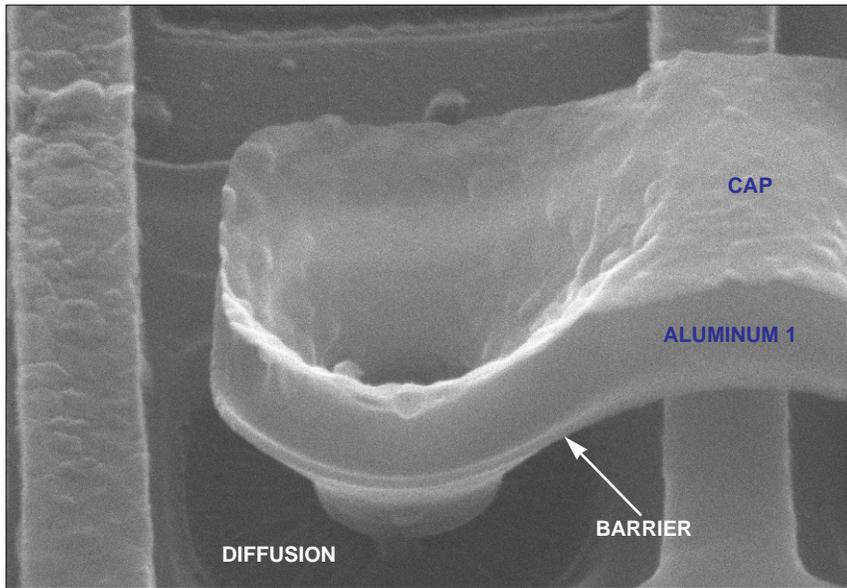


Mag. 7400x

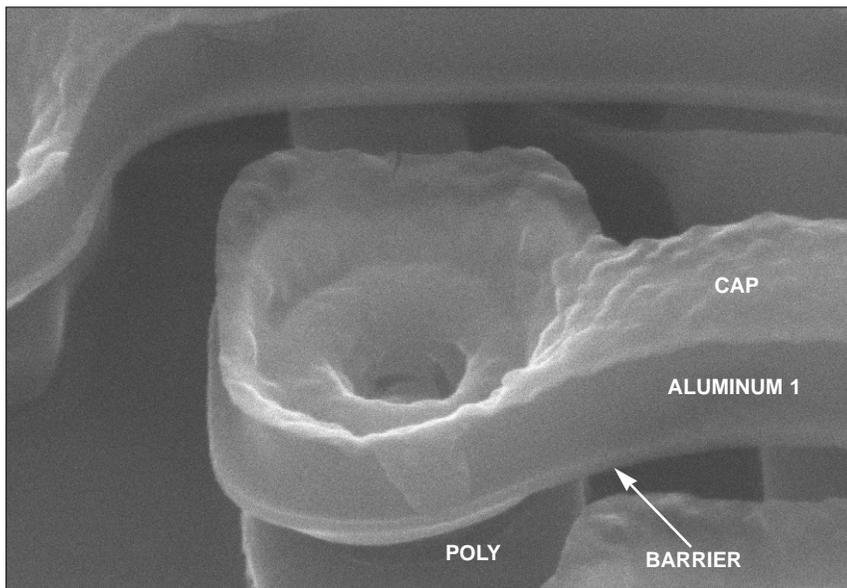
Figure 23. Topological SEM views of metal 1 patterning. 0°.



Mag. 6500x

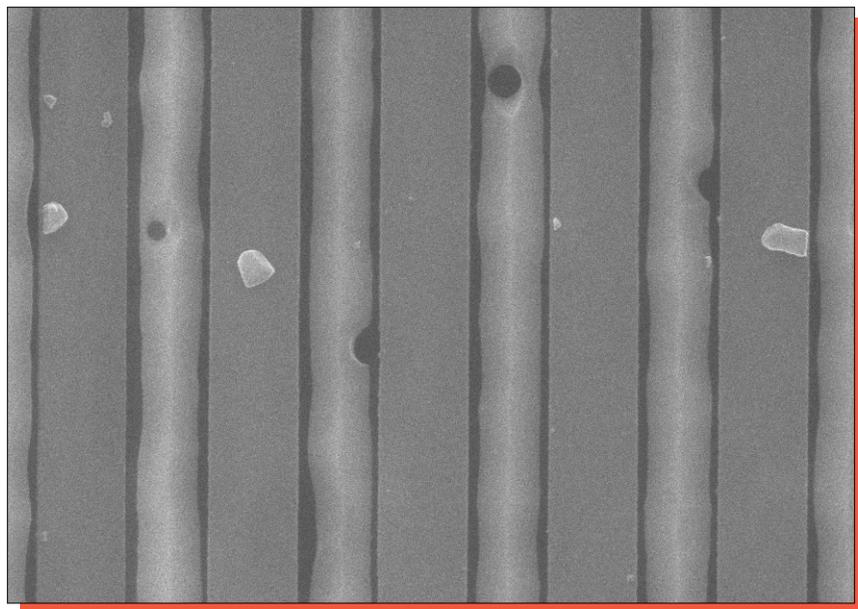


Mag. 25,000x

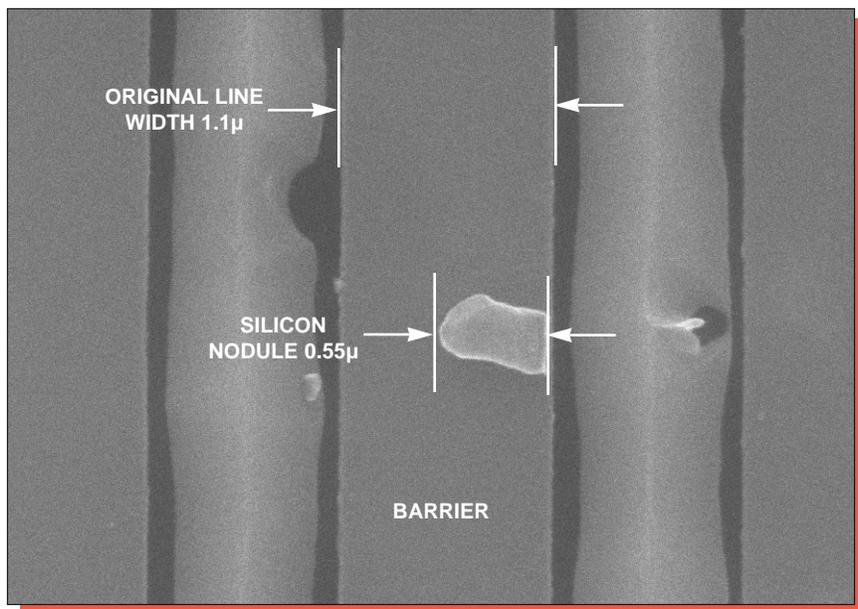


Mag. 25,000x

Figure 24. SEM views of general metal 1 integrity. 60°.



Mag. 10,000x



Mag. 25,000x

Figure 25. Topological SEM views of silicon nodules following aluminum 1 removal. 0°.

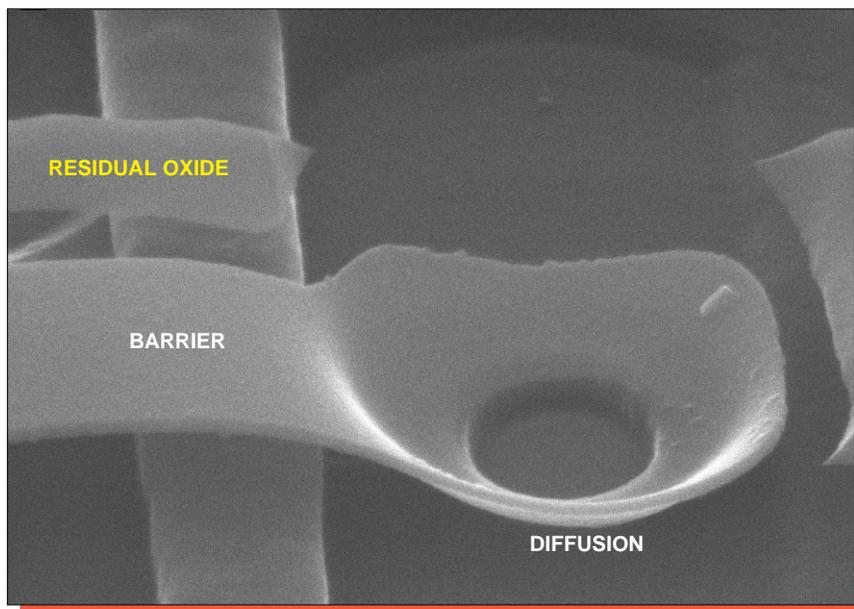
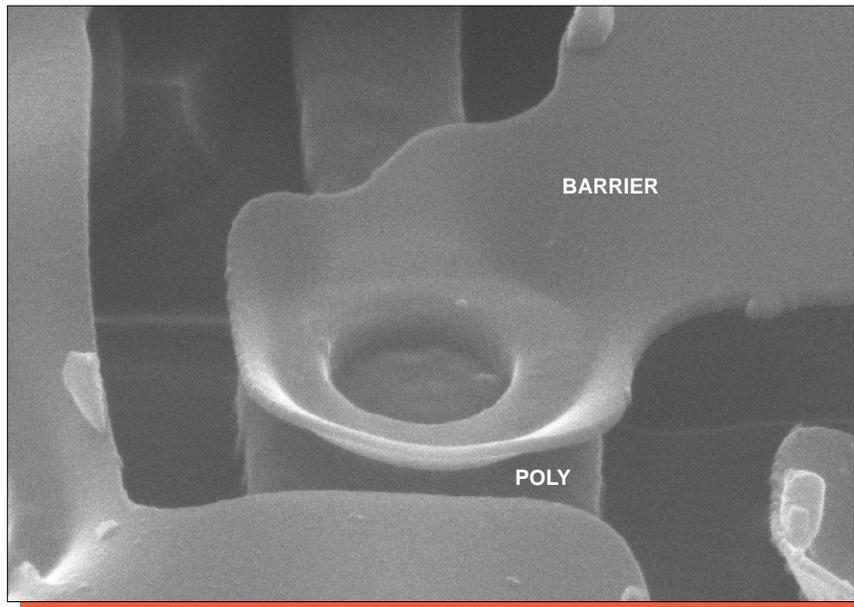


Figure 26. SEM views of metal 1 barrier coverage. Mag. 27,000x, 45°.

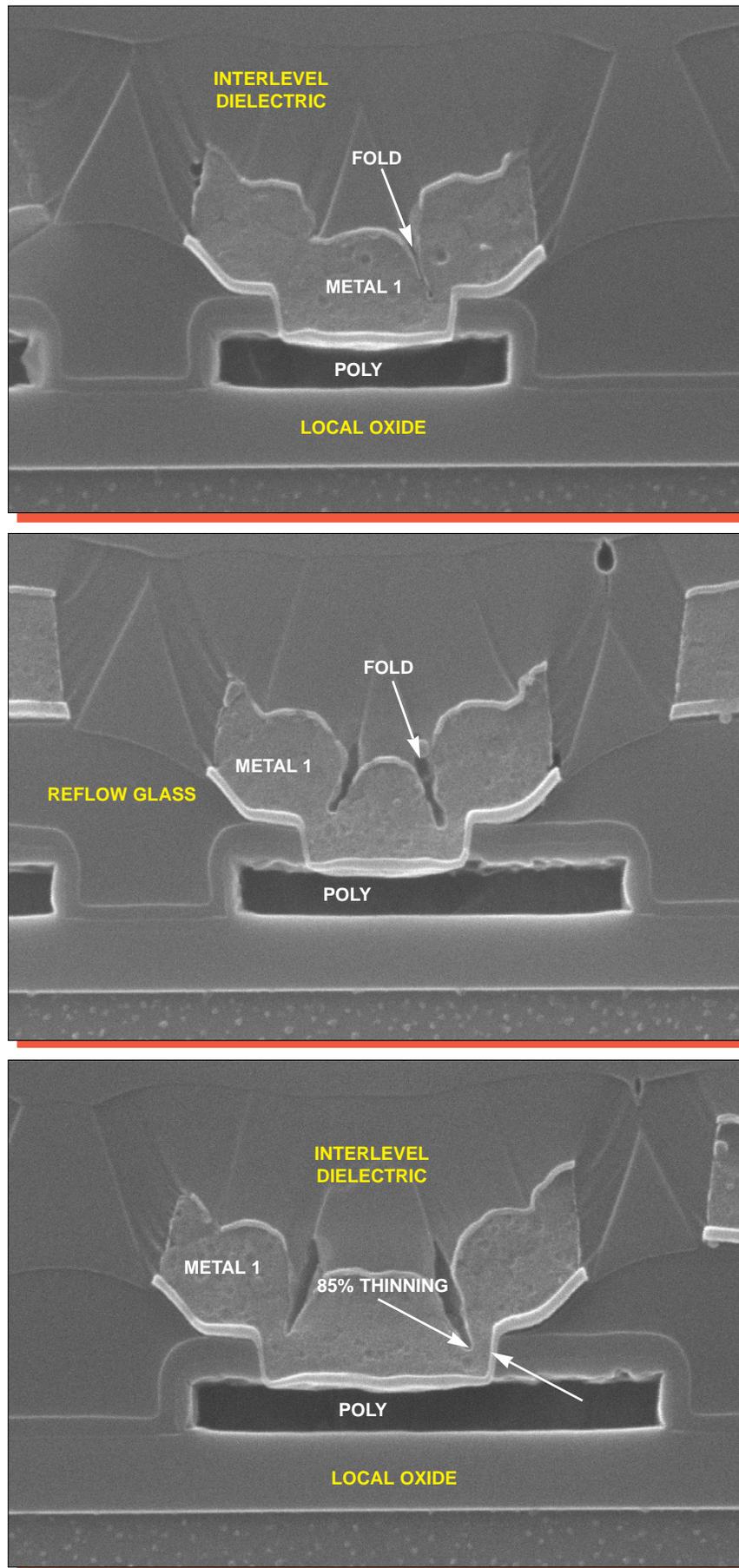
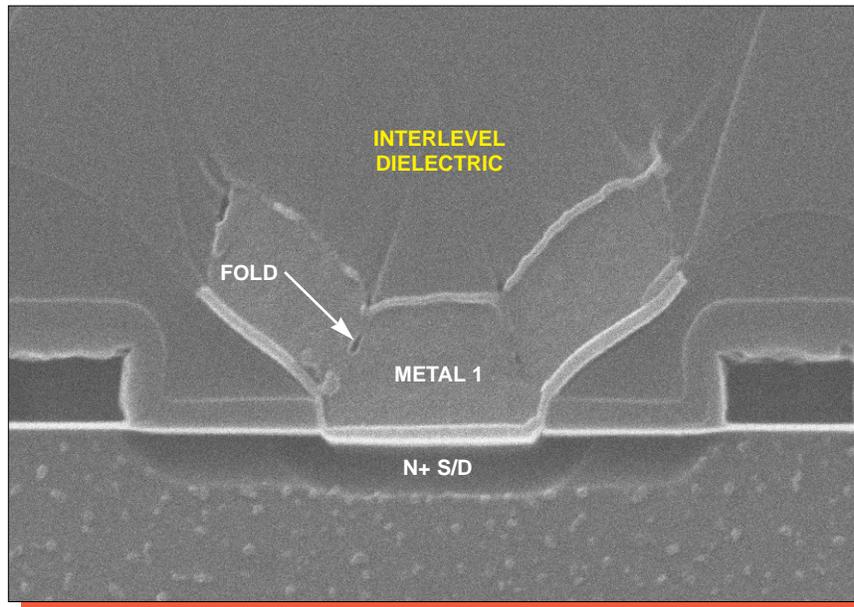
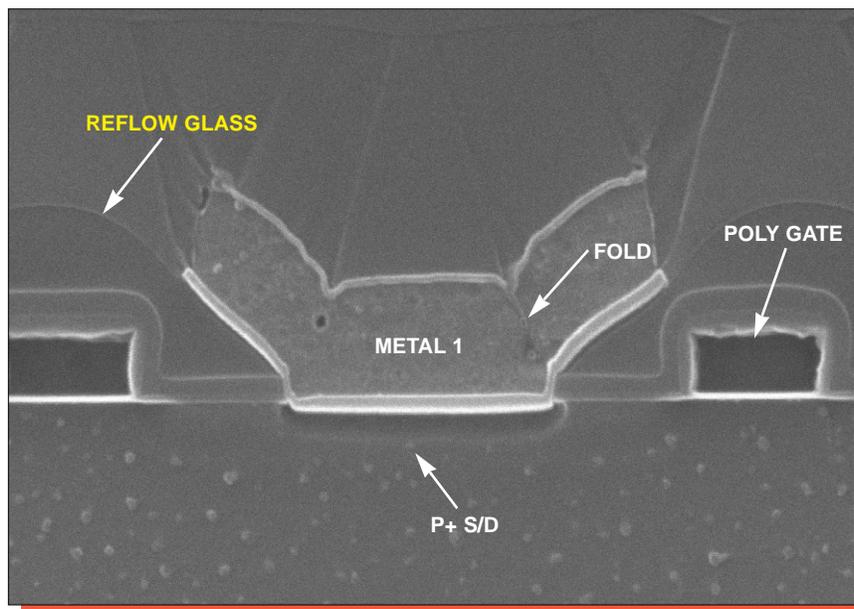


Figure 27. SEM section views of metal 1-to-poly contacts illustrating metal thinning.  
Mag. 27,000x.

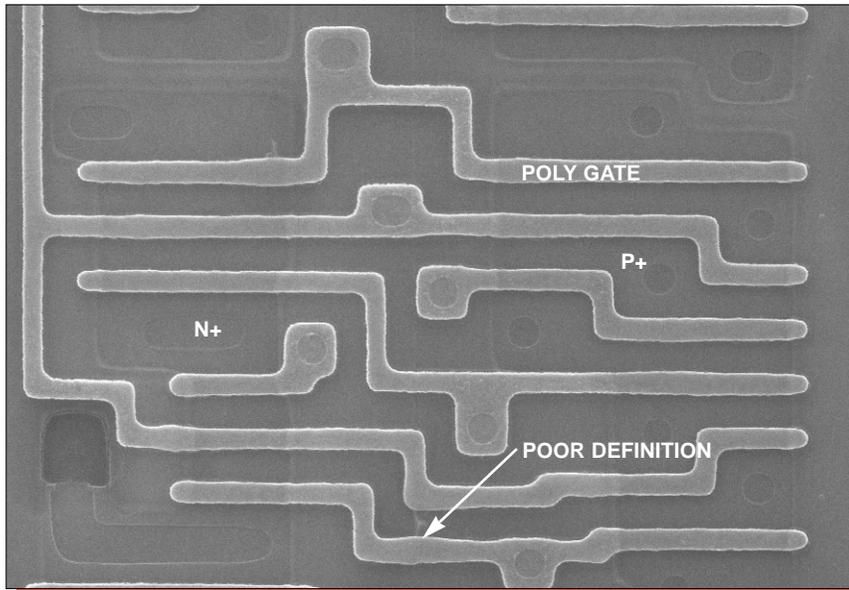


metal 1-to-N+, Mag. 30,000x

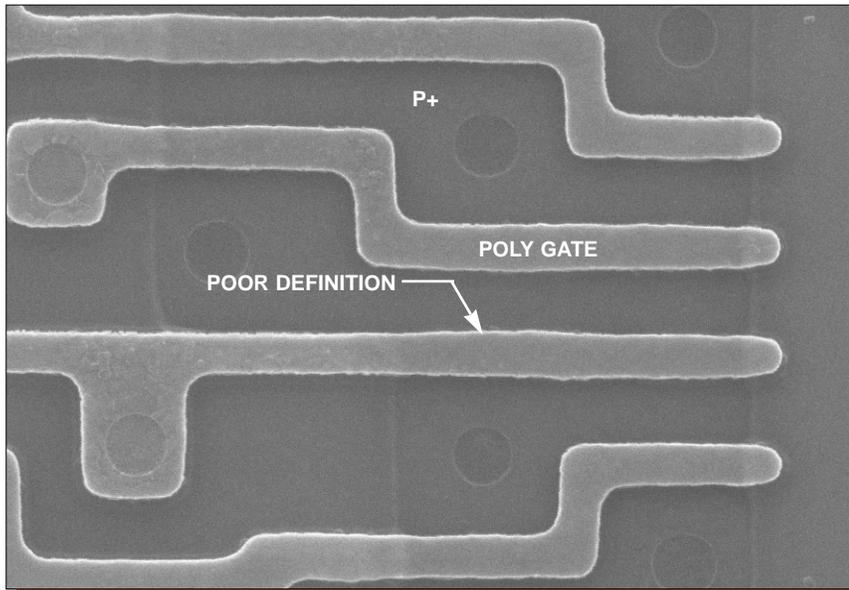


metal 1-to-P+, Mag. 27,000x

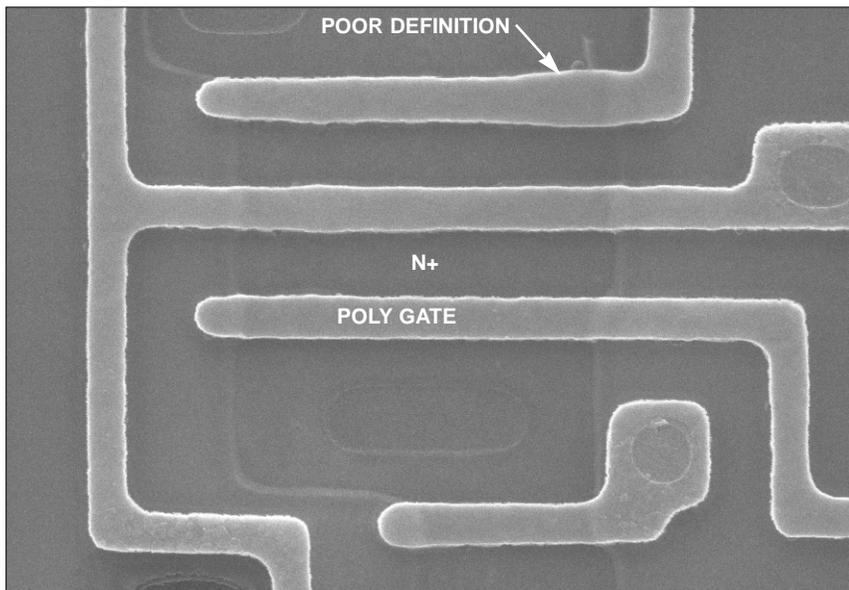
Figure 28. SEM section views of metal 1-to-diffusion contacts.



Mag. 4000x

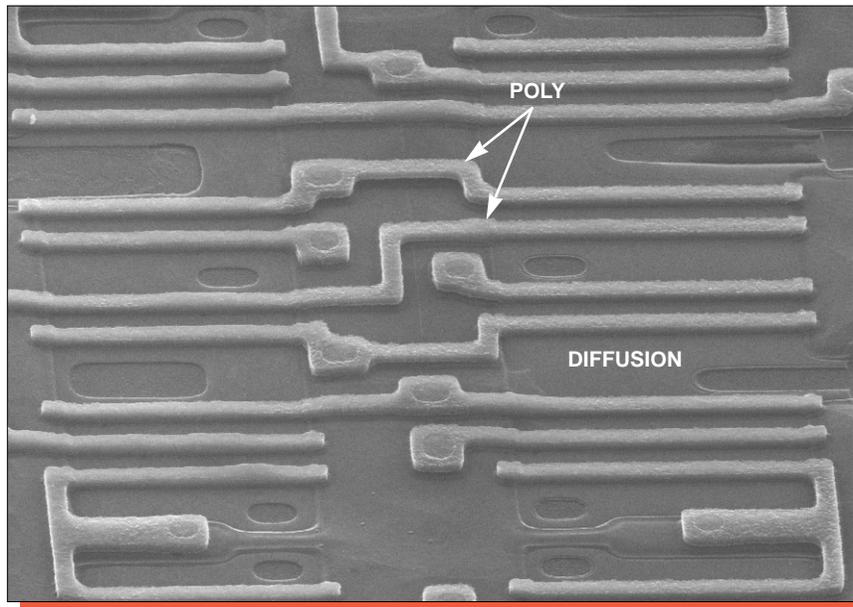


Mag. 8000x

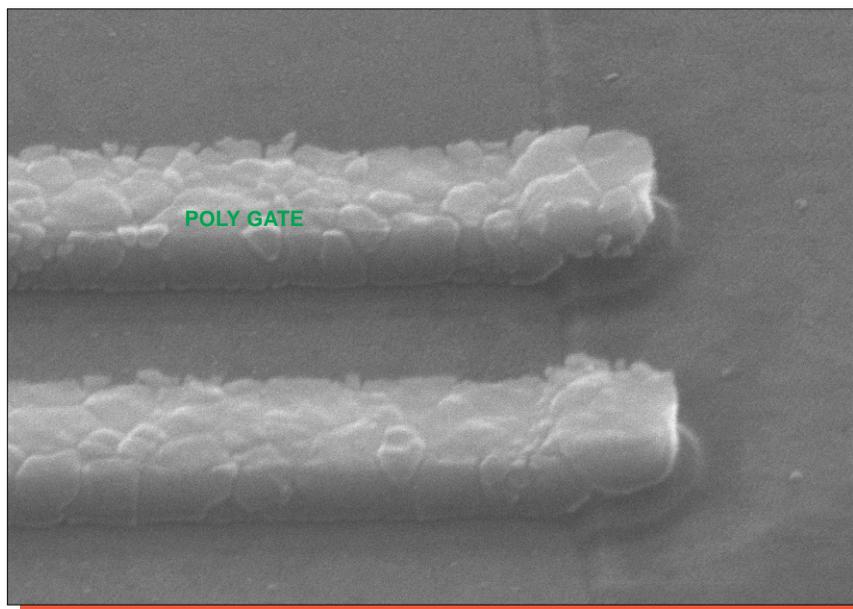


Mag. 8000x

Figure 29. Topological SEM views of poly patterning. 0°.

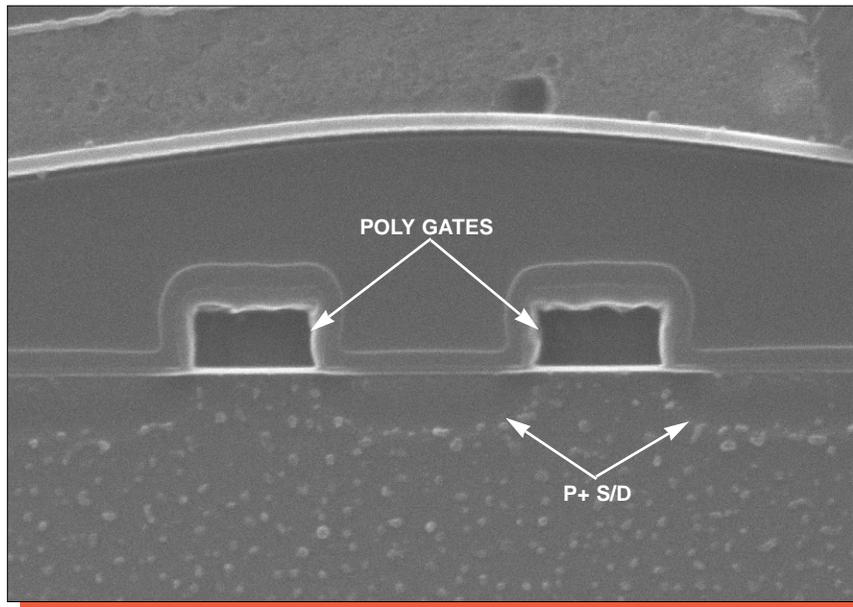


Mag. 4200x

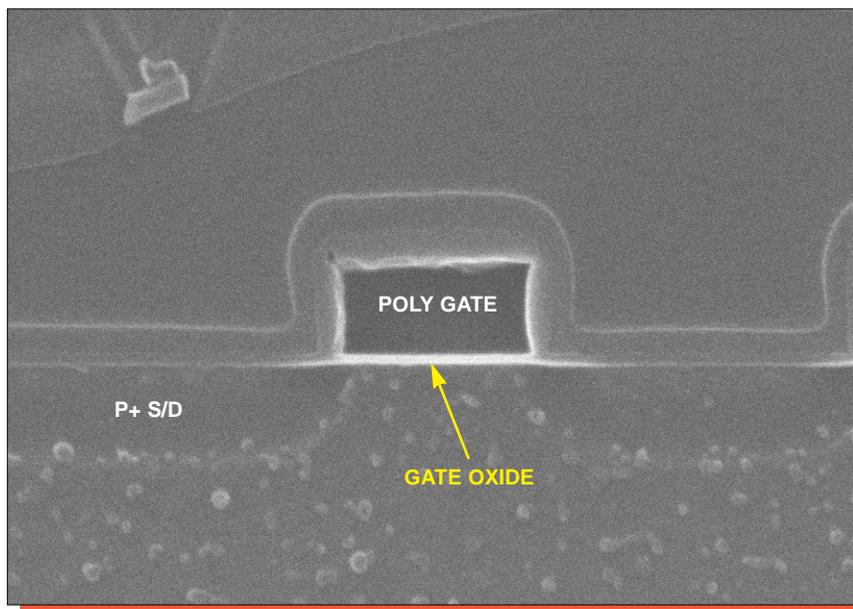


Mag. 30,000x

Figure 30. SEM views of poly coverage. 60°.

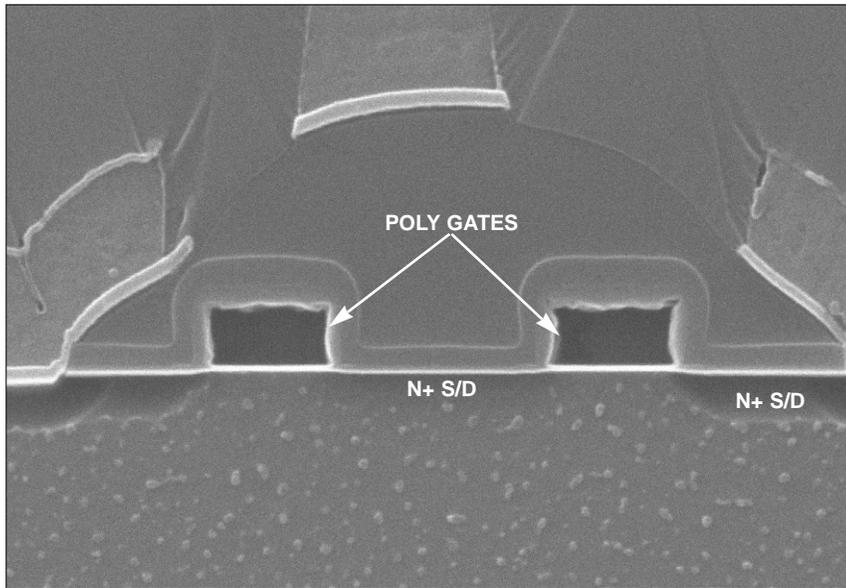


Mag. 26,000x

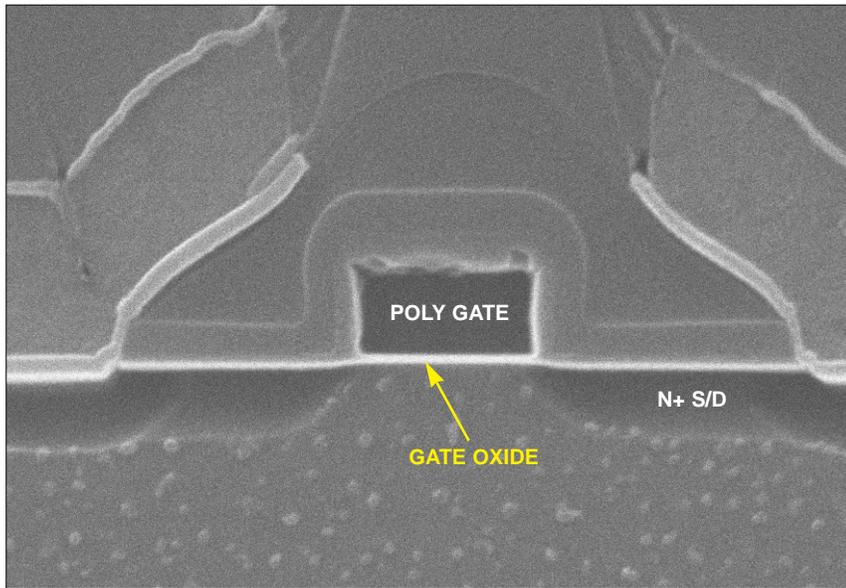


Mag. 40,000x

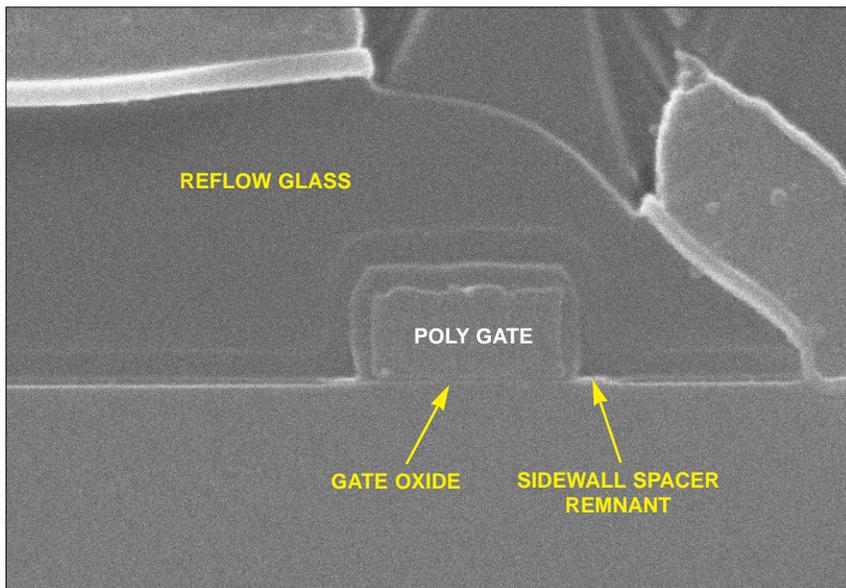
Figure 31. SEM section views of typical P-channel transistors.



Mag. 26,000x



Mag. 40,000x



glass etch,  
Mag. 40,000x

Figure 32. SEM section views of typical N-channel transistors.

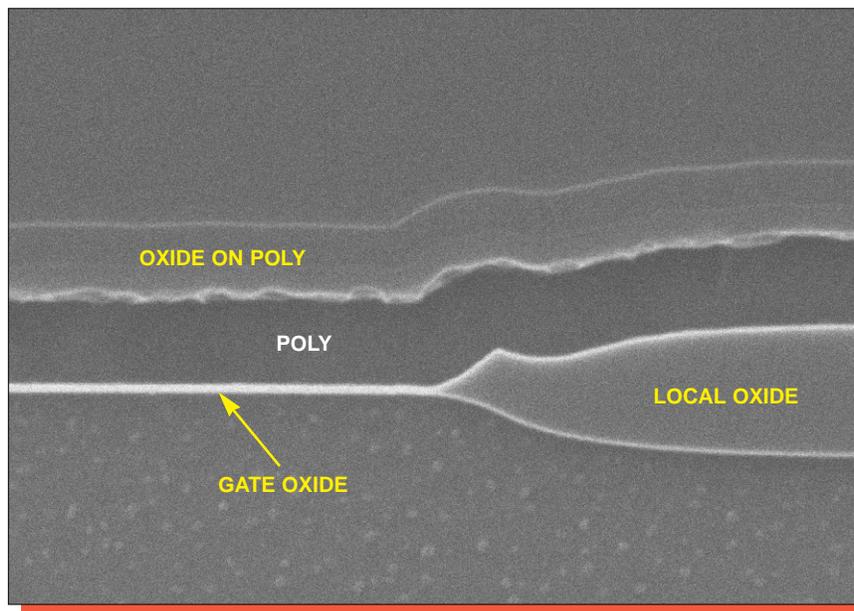


Figure 33. SEM section view of a local oxide birdsbeak. Mag. 40,000x.

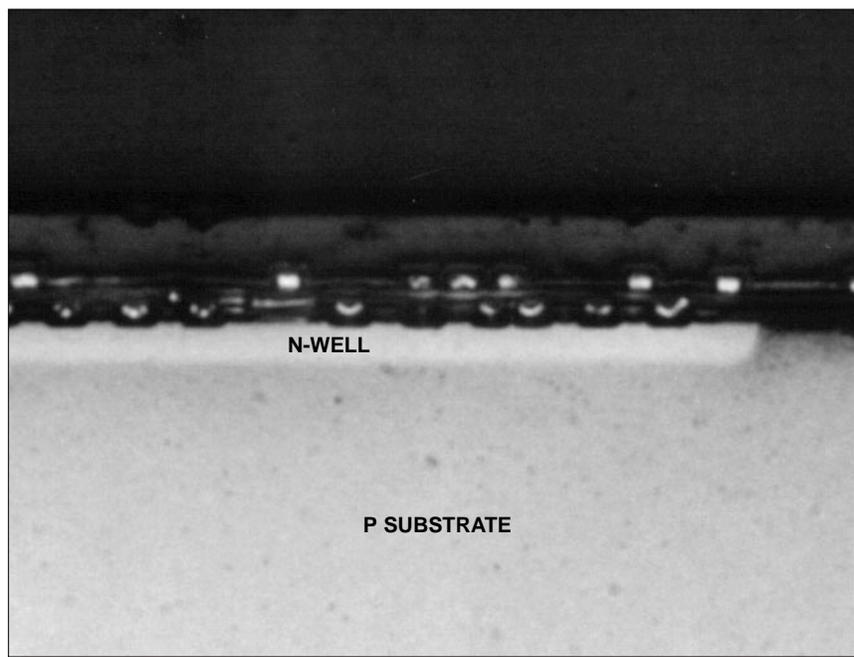
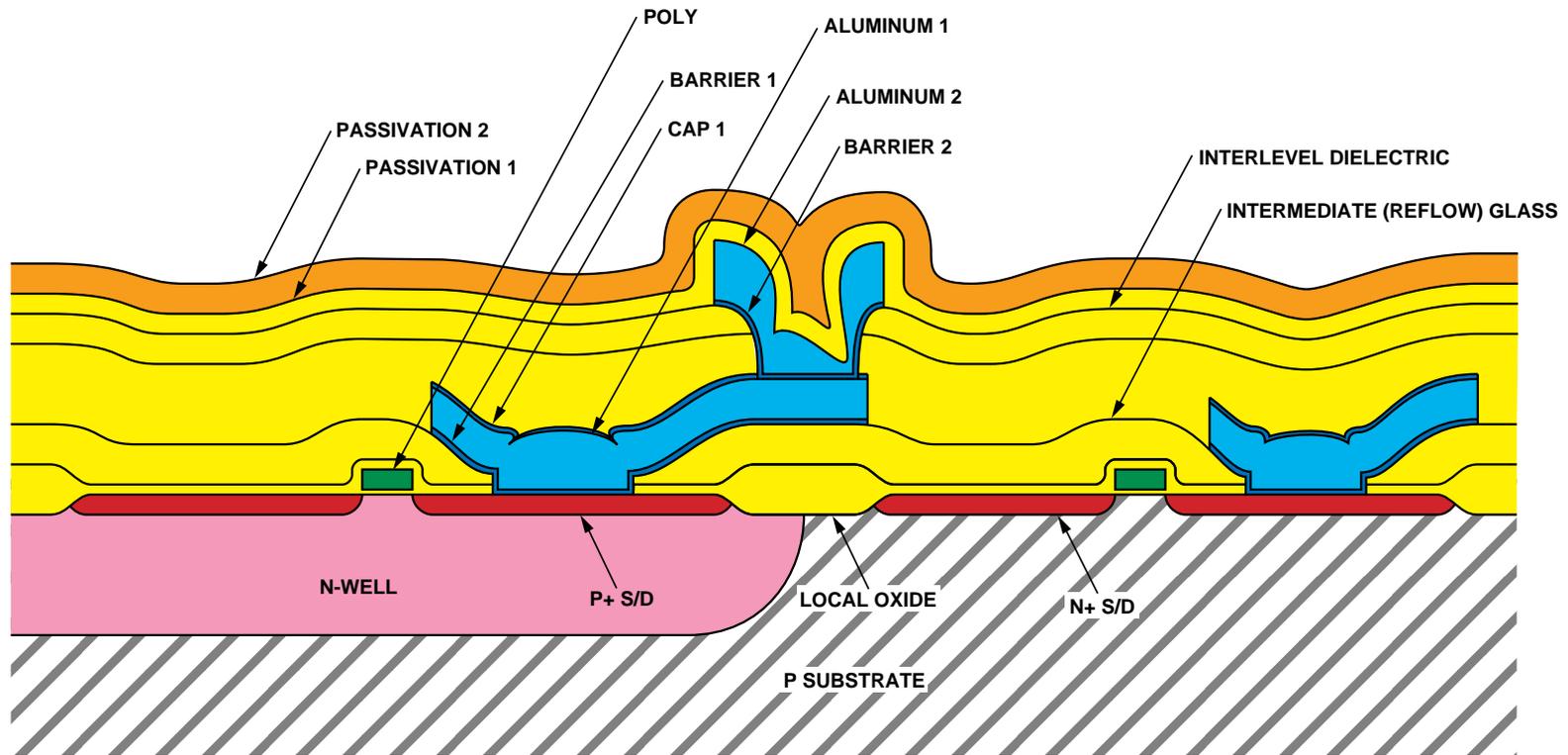
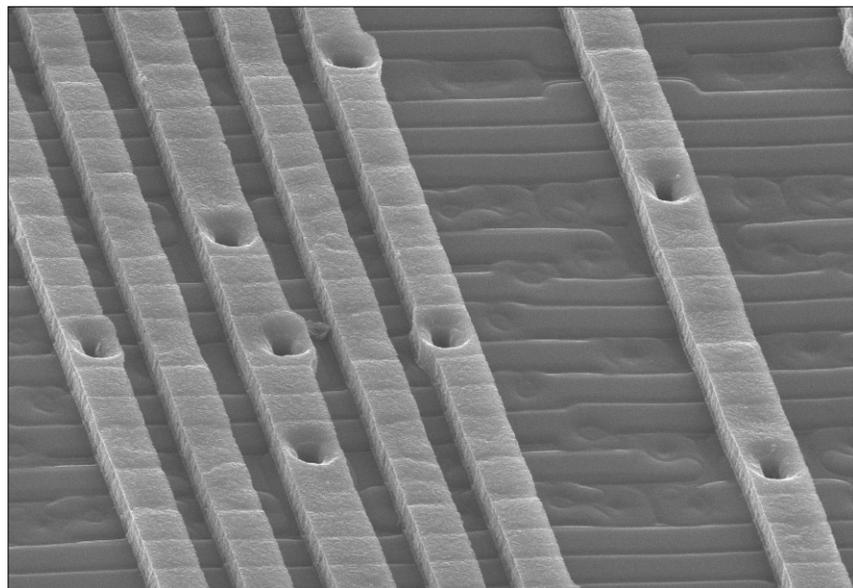


Figure 34. Optical section view illustrating well structure. Mag. 1600x.

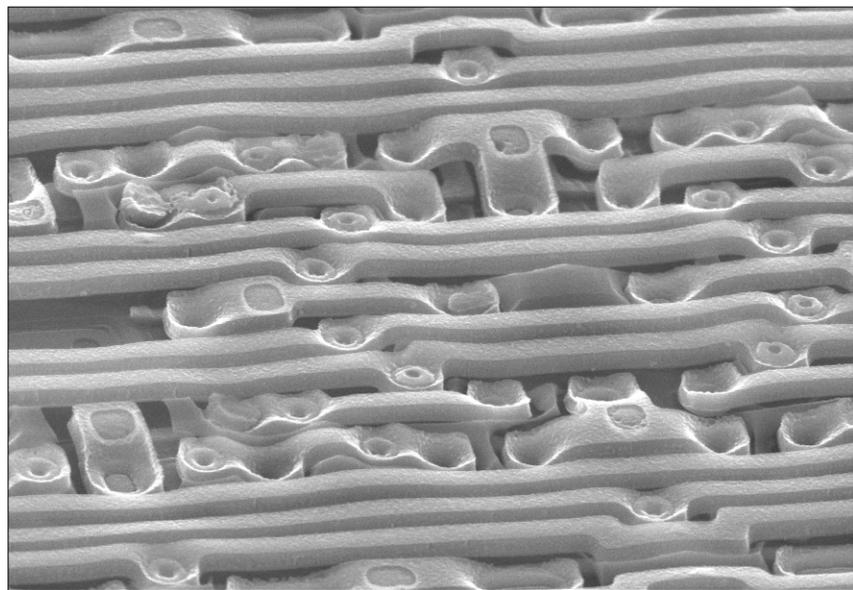


Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
 Red = Diffusion, and Gray = Substrate

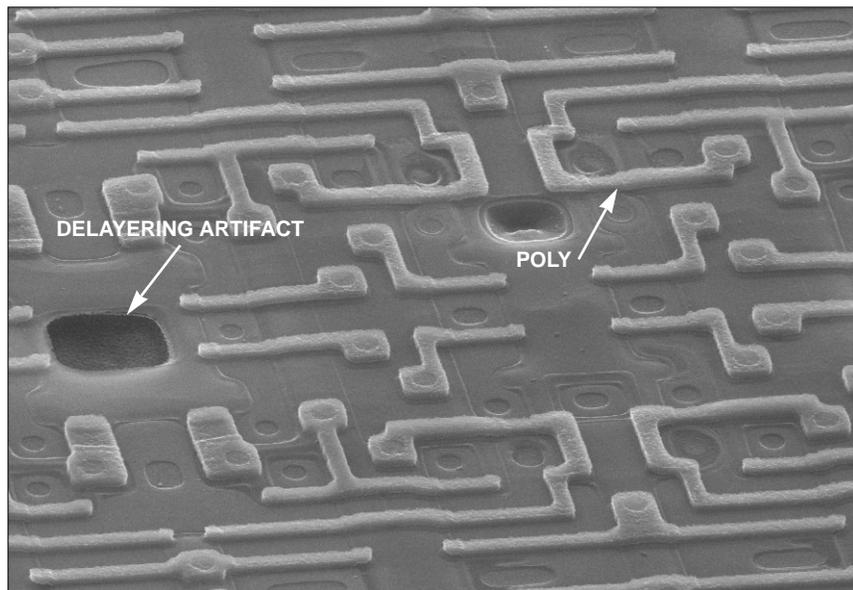
Figure 35. Color cross section drawing illustrating device structure.



metal 2

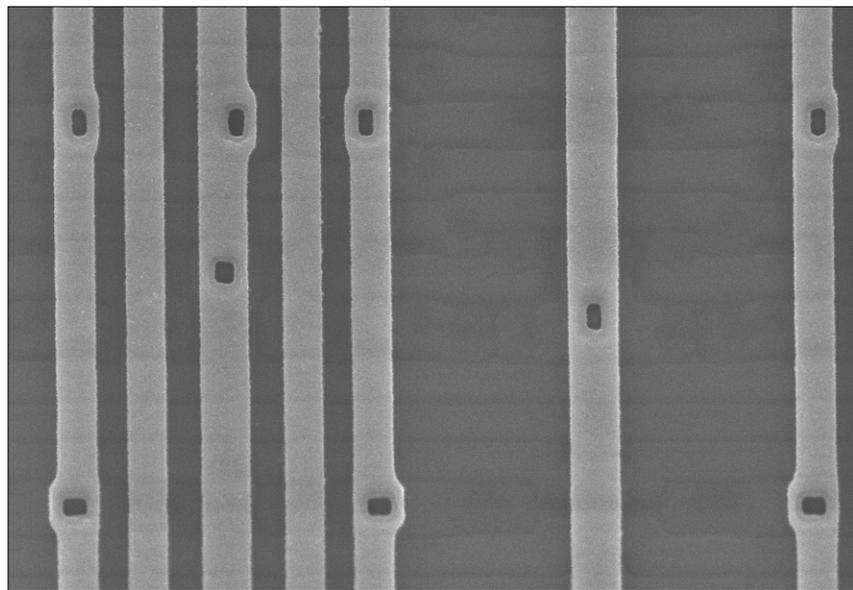


metal 1

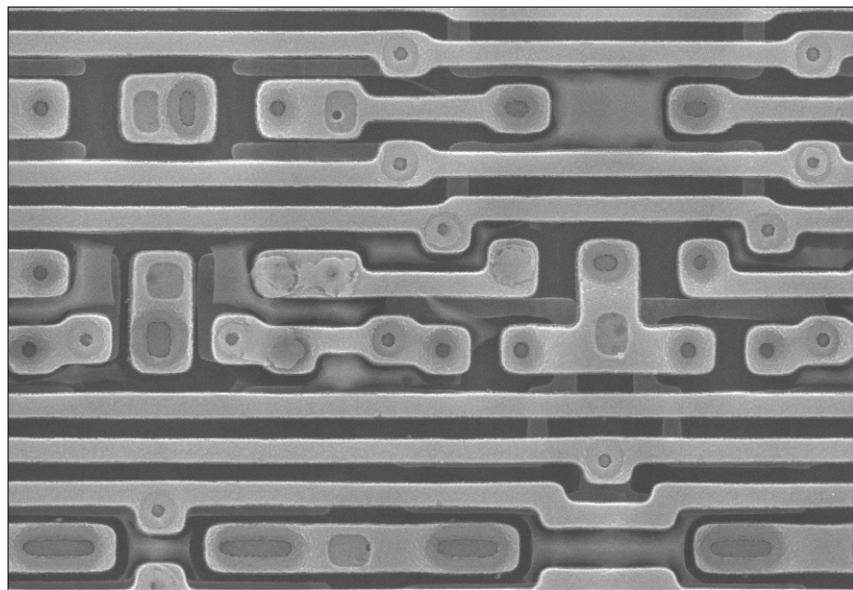


unlayered

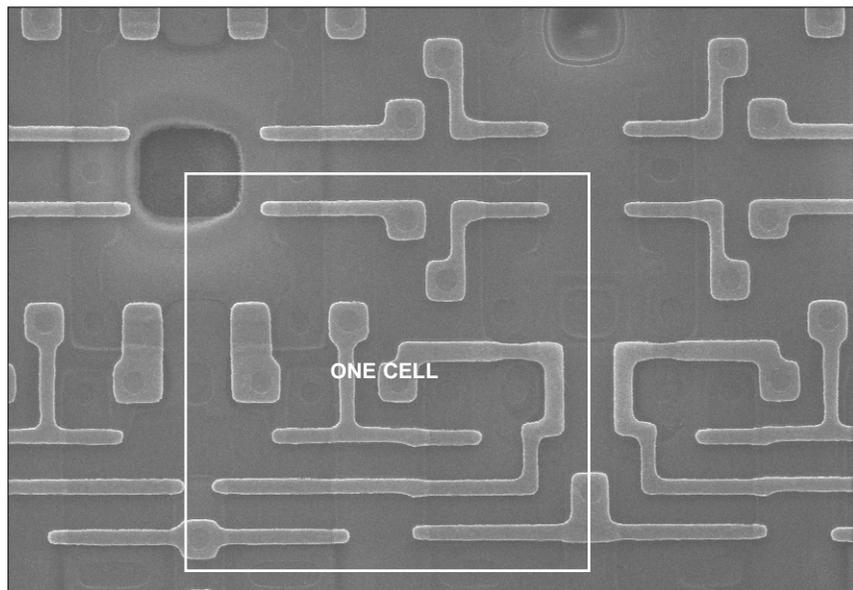
Figure 36. Perspective SEM views of a cell array. Mag. 3500x, 60°.



metal 2

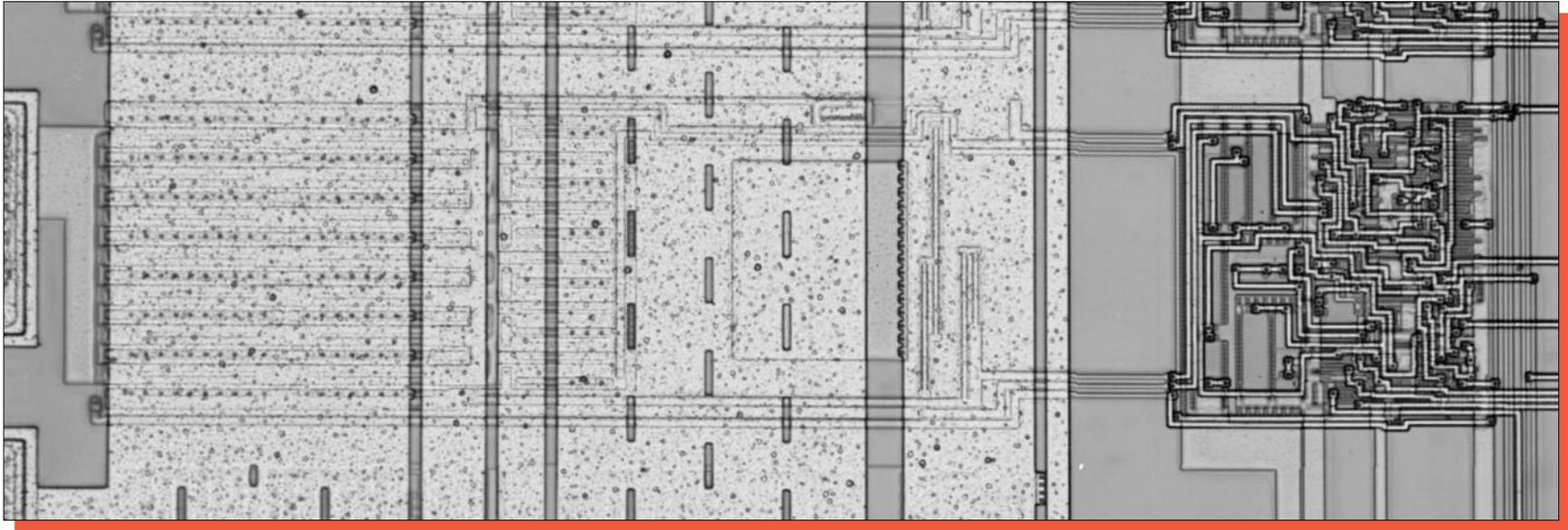


metal 1

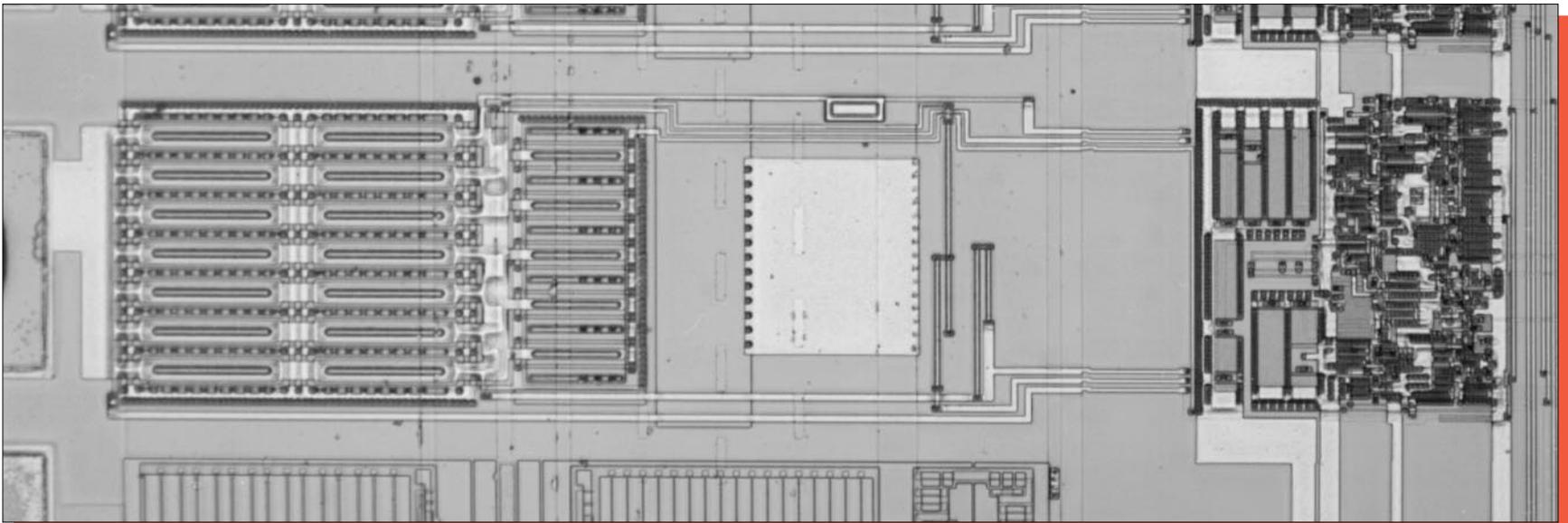


unlayered

Figure 37. Topological SEM views of a cell array. Mag. 3000x, 0°.



metal 2



metal 1

Figure 38. Optical views of I/O Buffer circuitry. Mag. 320x.