Construction Analysis

National Semiconductor 24C16EN 16 Kbit Serial EEPROM

Report Number: SCA 9512-442

INTEGRATED CIRCUIT ENGINEERING
17350 N. Hartford Drive
Scottsdale, AZ 85255
Phone: 602-515-9780
Fax: 602-515-9781
e-mail: ice@ice-corp.com
Internet: http://www.ice-corp.com

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INTRODUCTION

This report describes a construction analysis of the National Semiconductor 24C16EN 16K Serial EEPROM. Ten devices encapsulated in 8-pin Dual In-line Packages (DIP) were supplied for the analysis. No identifiable date code was present.

MAJOR FINDINGS

Questionable Items:[1]

- Poor metal 2 definition.
- Neckdown of the metal 2 was noted over metal 1 lines (Figure 14a). This narrowed the line widths by up to 45 percent[2].
- Silicon mound growth occupied up to 70 percent[2] of P+ contacts (Figure 20a).

Special Features:

- Manufacturer pinout indicates pin 1 connected; however, on all parts inspected this pin was not connected.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 8-pin DIPs.
- Thermosonic ball bond method employing 1.0 mil O.D. gold wire.
- Pins 1 and 7 were not connected.
- Lead-locking provisions (anchors and holes) at all pins.
- Sawn dicing (full depth).
- Silver-filled polyimide die attach.

Die Process and Design

- Fabrication process: Selective oxidation N-well CMOS process using a P-epi on a P substrate.
- Overlay passivation: A layer of nitride over a layer of silicon-dioxide.
- Metallization: Metal consisted of a two layers of aluminum doped with silicon. The metallization layers were defined by a dry-etch technique. No cap or barrier metals were employed.
- Interlevel dielectric: A single layer of silicon-dioxide.
- Intermediate glass: A borophosphosilicate glass (BPSG) over various densified oxides. This layer was reflowed prior to contact cuts.
- Polysilicon: One layer of dry-etched polysilicon (no silicide). Poly was used to form word lines, capacitors and gates in the array and all gates in the periphery.

TECHNOLOGY DESCRIPTION (continued)

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. No deep N+ contact diffusions were employed. No sidewall spacers (LDD process) were used.

- An N+ implant before poly deposition was present under the capacitors in the memory array.

- Wells: N-wells in a P-epi on a P substrate.

- Memory cells: The memory cell design consisted of poly word lines and select gates. Metal 1 formed the bit lines and distributed GND. Programming is achieved through an ultra-thin tunnel oxide.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 7**

Questionable Items: None.

Special Items:

- Pin 1 was not connected although data indicates it is.

General Items:

- Devices were packages in 8-pin DIPs.
- Overall package quality: Normal. No significant defects were found on the external or internal portions of the packages. Deflash quality was good. No gaps were noted at the lead exits.
- The header was offset in the package. The leadframe consisted of copper (Cu) with a trace of iron (Fe) and was externally tinned with tin-lead (SnPb) solder. Coverage was good.
- The leadframe was internally spot plated with silver.
- Lead-locking provisions (holes and anchors) were present at all leads.
- Wirebonding: Thermosonic ball bond method using 1.0 mil O.D. gold wire. Wirebond placement and formation was good. Intermetallic formation was complete. No bond lifts occurred and bond pull strengths were good. Wire spacing was normal.
- Die attach: Silver-filled polyimide of normal quality. Some small voids were noted in the die attach; however, no problems are foreseen.
- Die dicing: Die separation was by full depth sawing with good quality workmanship.

ANALYSIS RESULTS II

Die Process and Design: **Figures 8 - 34**

Questionable Items:[1]

- Poor metal 2 definition.
- Neckdown of the metal 2 over metal 1 lines (Figure 14a). This narrowed the line widths by up to 45 percent [2].
- Silicon mound growth occupied up to 70 percent[2] of P+ contacts (Figure 20a).

Special Features: None.

General Items:

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P-epi on a P substrate.
- Design and layout: Die layout was clean and efficient. Alignment of the layers was good.
- Die surface defects: None. No contamination, toolmarks or processing defects were noted.
- Overlay passivation: A layer of nitride over a layer of silicon-dioxide. Overlay integrity tests indicated defect-free passivation. Edge seal was good.
- Metallization: Two levels of metallization. Metals consisted of aluminum doped with silicon. No cap or barrier metals were employed.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

[2] *Seriousness depends on design margins.*

ANALYSIS RESULTS II (continued)

- Metal patterning: Metal 2 was defined by a dry etch of poor quality. Metal 2 patterning was rough and necked down over metal 1 steps. Some overetching of the metal 2 was noted along bottom half of sidewalls. This indicates poor processing control; however, no reliability concerns are foreseen. No problems were noted with the metal 1 patterning.

- Metal defects: There were no significant (>50 percent of line width) silicon nodules found following the removal of the metal layers.

- Metal step coverage: Metal 2 thinning of up to 45 percent was noted at vias and metal 1 thinning up to 40 percent at contacts. Virtually no metal thinning was noted outside of vias and contacts.

- Contacts: Via and contact cuts appeared to be slope etched. Some overetching of the contacts was noted; however, no problems are foreseen. Some significant silicon mound growth was noted at metal-to-P+ contacts. These silicon mounds occupied up to 70 percent of contact areas. These areas increase contact resistance. Some overetching of the contacts was present; however, no problems are foreseen.

- Interlevel dielectric: The interlevel dielectric consisted of a layer of silicon-dioxide (PECVD?). No problems were found with this layer. No SOG was used.

- Intermediate glass: A layer of borophosphosilicate glass (BPSG) over various densified oxides. This layer was reflowed prior to contact cuts. No problems were found.

- Polysilicon: One layer of dry-etched polysilicon (no silicide). Poly was used to form word lines, capacitors and gates in the array and all gates in the periphery.

- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. No step was noted in the local oxide at the well boundaries.

ANALYSIS RESULTS II (continued)

- Diffusions: Standard implanted N+ and P+ diffusions were used for sources and drains. No problems were found. No deep N+ contact diffusions were employed. Sidewall spacers were not present (no LDD process).

- As mentioned, a separate N type implant, done before poly deposition was present under some of the poly in the cell array.

- It appears that at least three types of thin oxide are present.

- Wells: N-wells in a P-epi on a P substrate.

- Memory cells: The EEPROM memory cell design consisted of poly word lines, select gates and capacitor plates. Metal 1 formed the bit lines and distributed GND. Programming is achieved through and ultra-thin tunnel oxide. Cell size was 20 x 20 microns.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

X-ray

Package section

Decapsulation

Internal optical inspection

SEM inspection of assembly features and passivation

Passivation integrity test

Wirepull test

Passivation removal

Delayer to metal 2 and inspect

Metal 2 removal and inspect vias and silicon nodules

Delayer to metal 1 and inspect

Metal 1 removal and inspect contacts and silicon nodules

Delayer to poly and inspect poly structures and die surface

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

Die material analysis

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	G
Dicing quality	G
Wirebond method	Thermosonic ball bonds using 1.0 mil gold wire.
Die attach method	Silver-filled polyimide
Dicing method:	Sawn (full depth)
Die surface integrity:	
Tool marks (absence):	G
Particles (absence):	G
Contamination (absence):	G
Process defects (absence):	N
General workmanship	N
Passivation integrity	G
Metal definition	NP[1]
Metal integrity	N
Contact coverage	G
Contact registration	G
Contact defects	N

[1] Poor *metal 2 patterning.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

Top	Bottom
(LOGO) B43AG 24C16EN	THAILAND

WIREBOND STRENGTH

Wire material:	1.0 mil diameter gold
Die pad material:	aluminum
Material at package post:	silver
# of wires tested:	6
Bond lifts:	0
Force to break - high:	11.0g
- low:	8.0g
- avg.:	9.5g
- std. dev.:	1.1

PACKAGE MATERIAL ANALYSIS (EDX)

Leadframe:	Copper (Cu) with iron (Fe)
Internal plating:	Silver (Ag)
External plating:	Tin-lead (SnPb)
Die attach:	Silver- (Ag) filled polyimide

DIE MATERIAL ANALYSIS

Passivation:	Silicon-nitride over glass.
Metallization:	Silicon-doped aluminum. No copper was detected.
Interlevel dielectric:	Silicon-dioxide.
Intermediate glass:	Borophosphosilicate glass (BPSG) containing 4.5 wt. percent boron and 5.1 wt. percent phosphorus.

HORIZONTAL DIMENSIONS

Die size:	3.3 x 3.3 mm (129 x 129 mils)
Die area:	10.7 mm^2 (16,641 $mils^2$)
Min pad size:	0.12 x 0.11 mm (4.7 x 4.3 mils)
Min pad window:	0.11 x 0.1 mm (4.4 x 4.0 mils)
Min pad space:	0.6 mm (25 mils)
Min metal 2 width:	2.0 microns
Min metal 2 space:	2.0 microns
Min metal 1 width:	2.0 microns
Min metal 1 space:	1.8 micron
Min via:	2.0 microns
Min contact:	1.4 micron
Min poly width:	2.1 microns
Min poly space:	1.5 micron
Min gate length - (N-channel):	2.1 microns
- (P-channel):	2.1 microns
Cell pitch:	20 x 20 microns
Cell size:	400 $micron^2$

VERTICAL DIMENSIONS

Die thickness:	0.35 mm (13.5 mils)

Layers

Passivation 2:	1.2 micron
Passivation 1:	0.25 micron
Metallization 2:	1.25 micron
Interlevel dielectric:	0.9 micron (average)
Metallization 1:	1.0 micron
Intermediate glass:	0.8 micron (average)
Poly:	0.5 micron
Local oxide:	1.2 micron
Oxide over N+:	0.2 micron
Oxide over P+:	0.13 micron
N+ S/D diffusion:	0.35 micron
N+ under poly implant:	0.2 micron
P+ diffusion:	0.4 micron
N - well:	8.0 microns
P - epi:	23 microns

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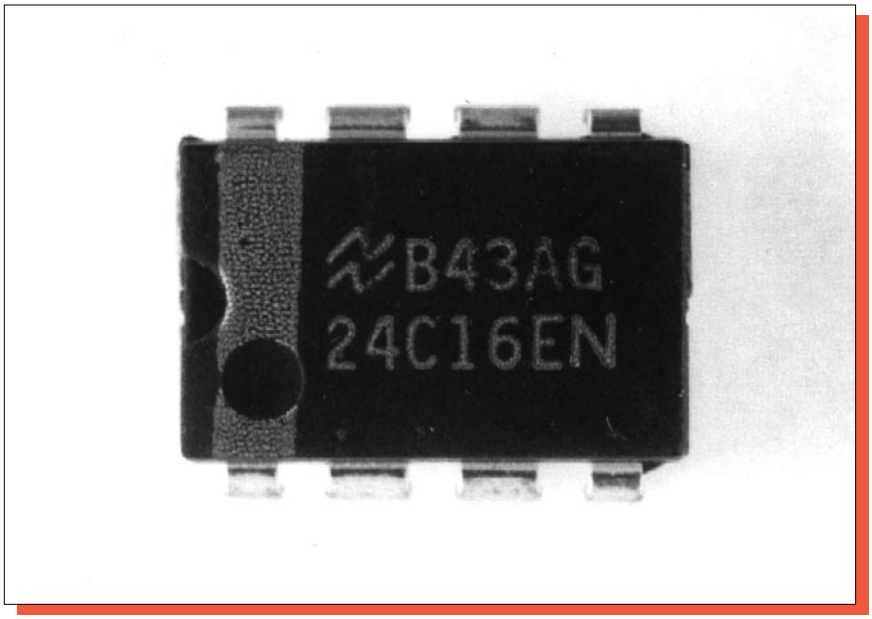


top

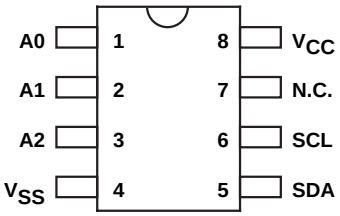
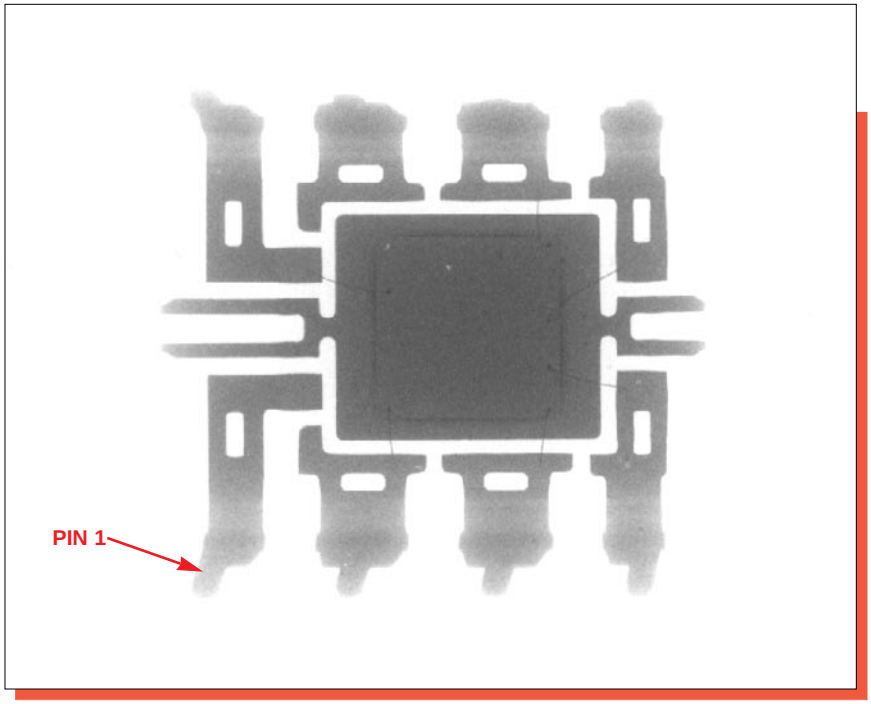


Figure 1. Package photograph and pinout of the National Semiconductor 16K Serial EEPROM. Mag. 7x.



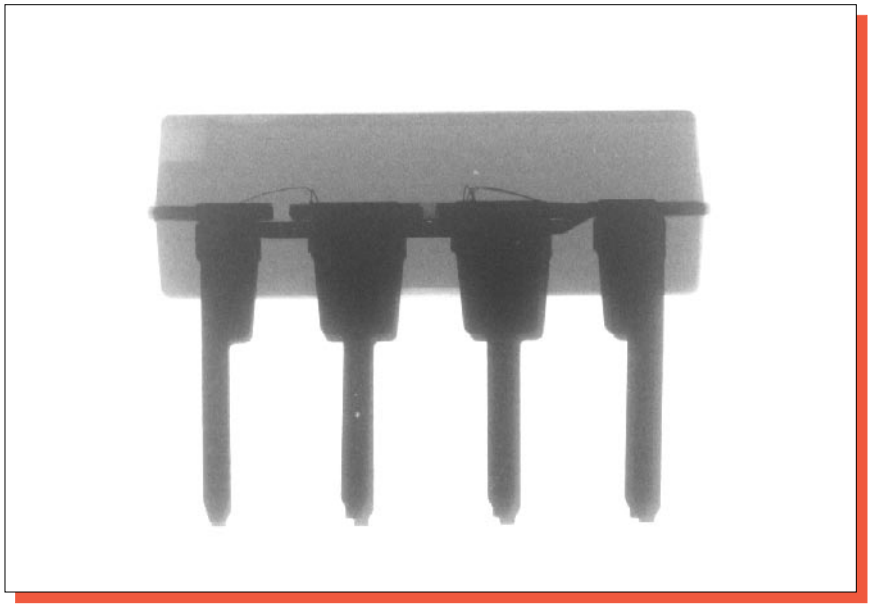
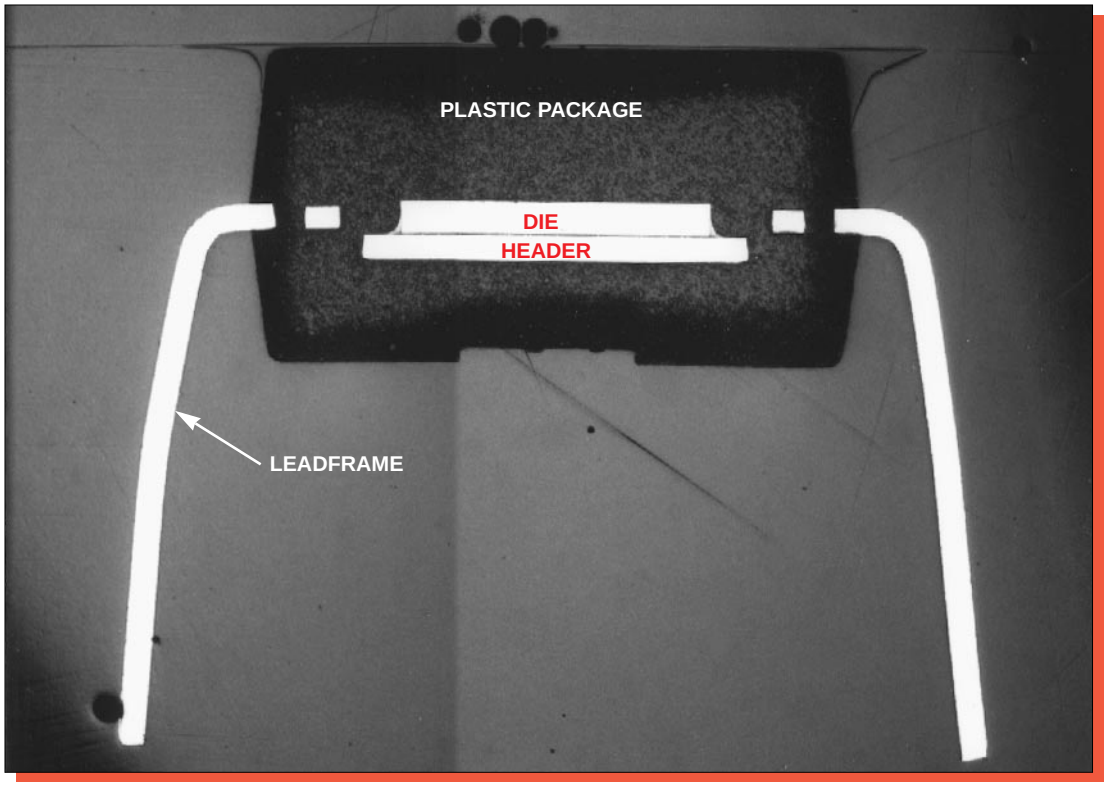
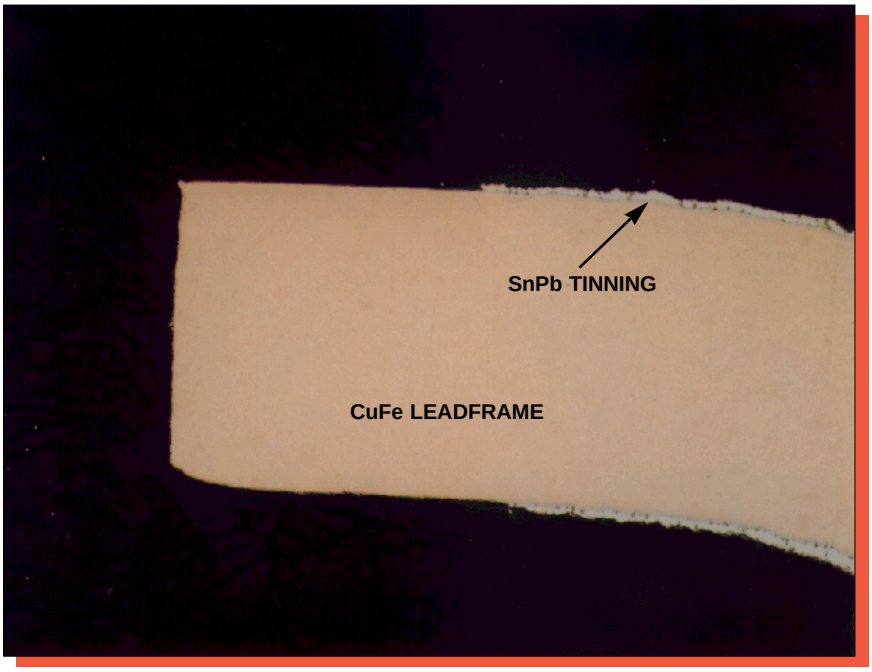


Figure 2. X-ray views of the package. Mag. 7x.

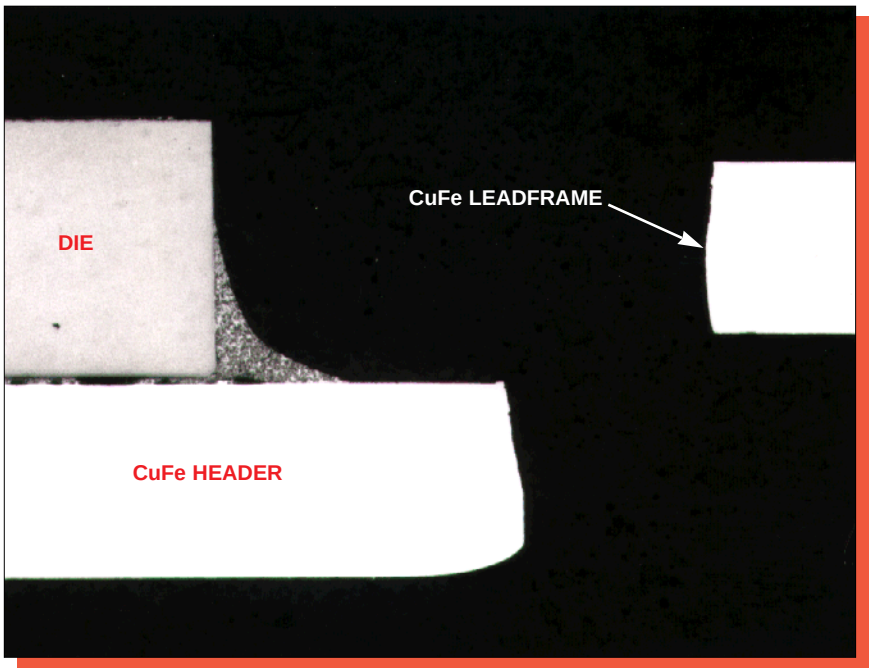


Mag. 13x

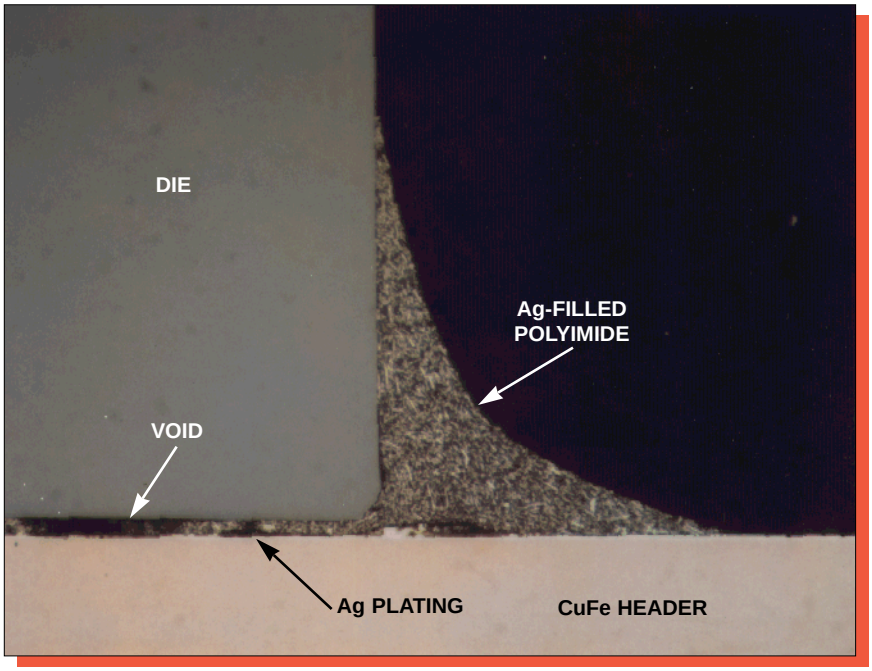


Mag. 160x

Figure 3. Package section views of general package construction and lead exit and plating.

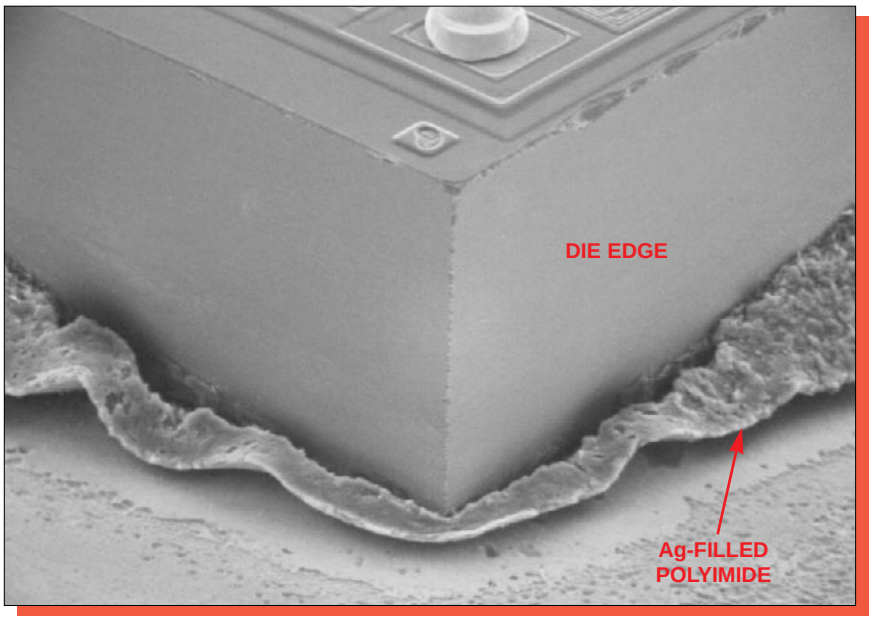


Mag. 100x

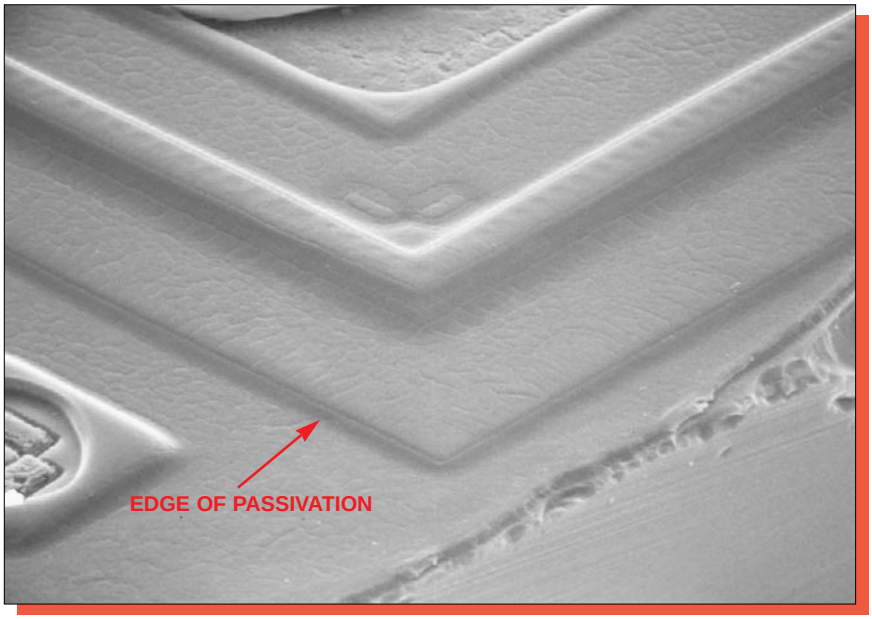


Mag. 260x

Figure 4. Package section views of dicing and die attach.

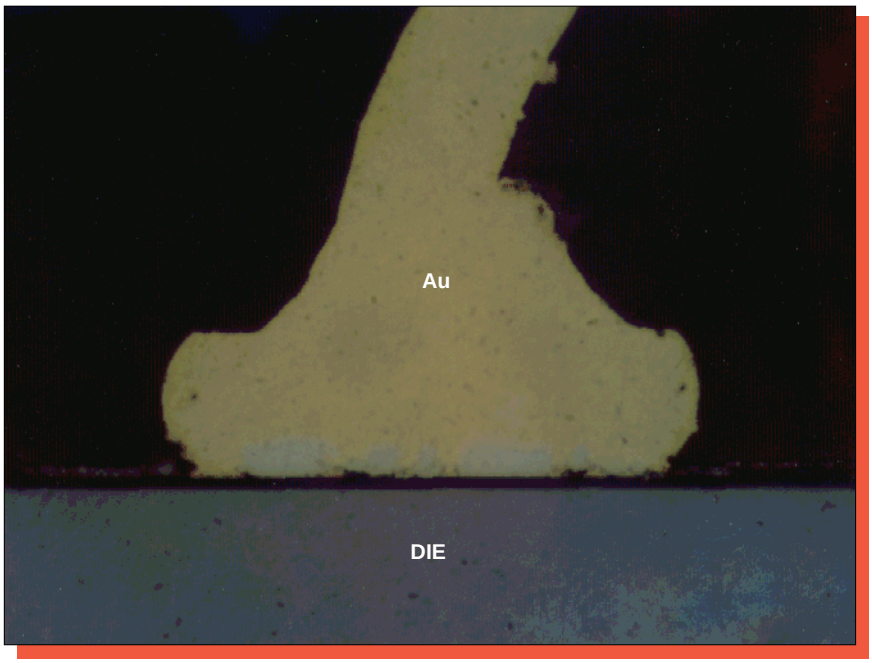


Mag. 150x

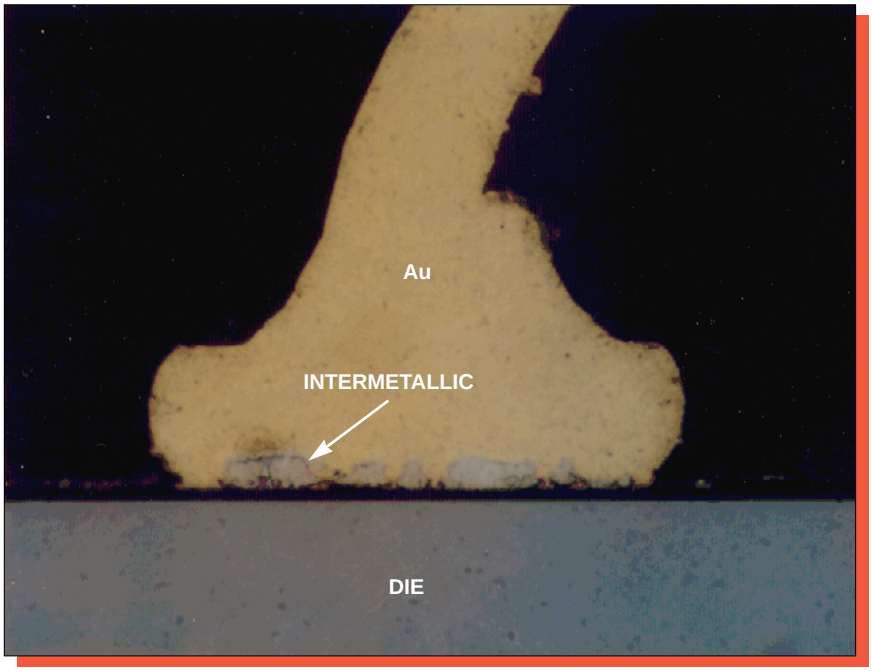


Mag. 800x

Figure 5. SEM views of die corner, die attach and edge seal. 60°.

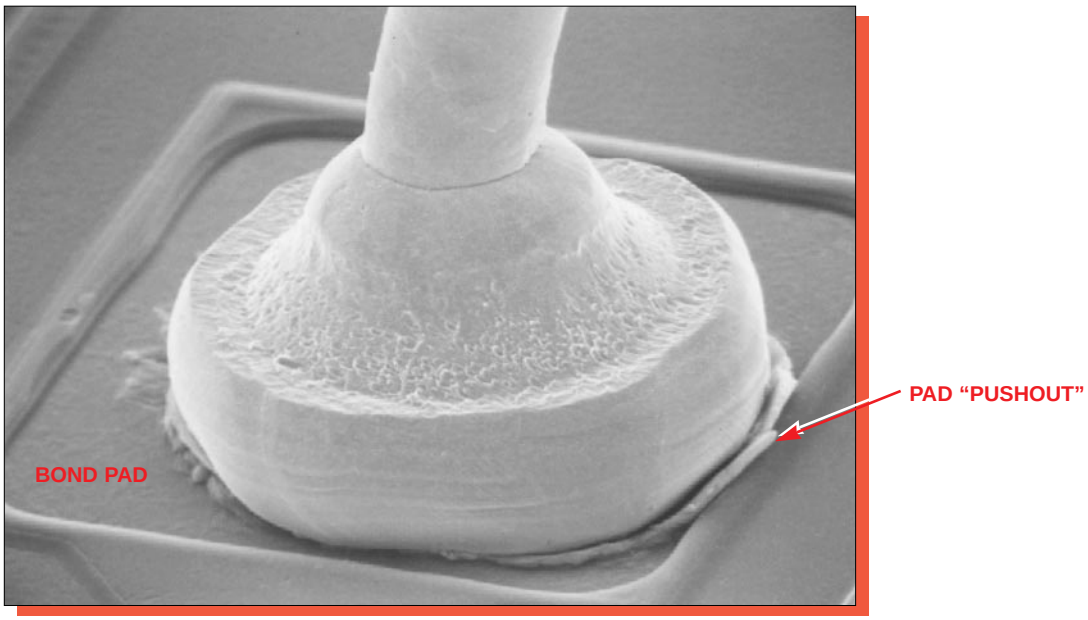


as polished

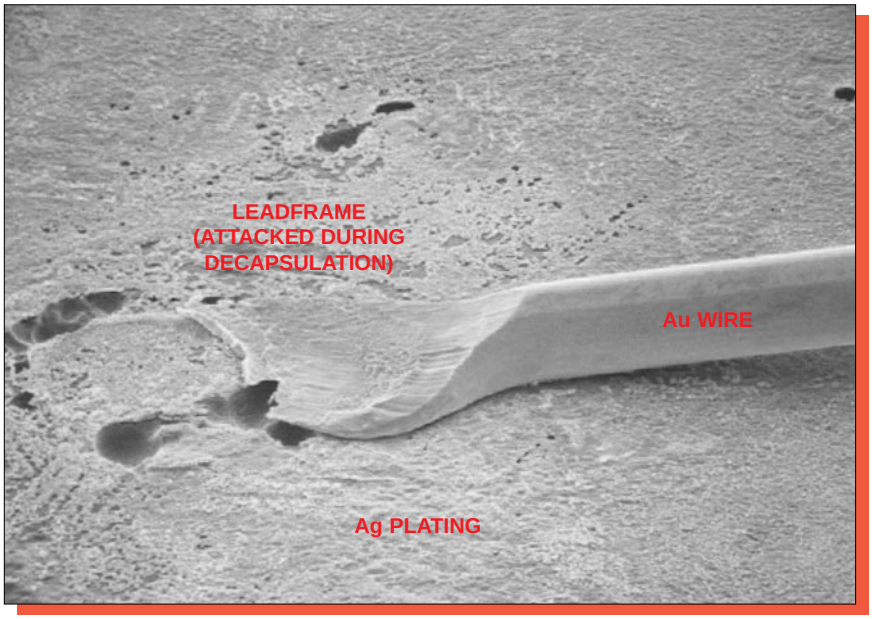


intermetallic delineated

Figure 6. Package section views of a typical ball bond. Mag. 800x.



Mag. 900x



Mag. 500x

Figure 7. SEM views of typical wirebonds. 60°.

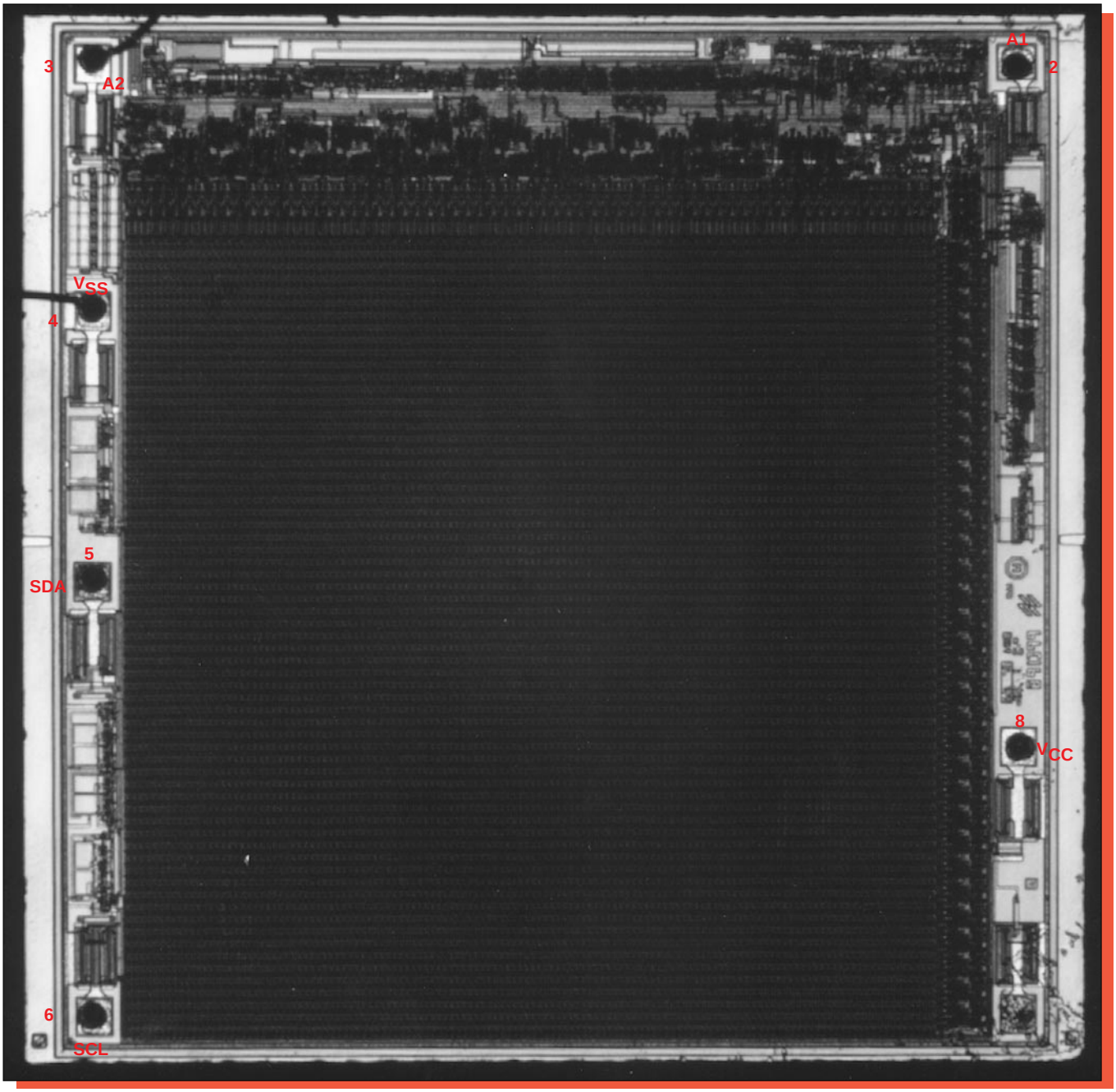
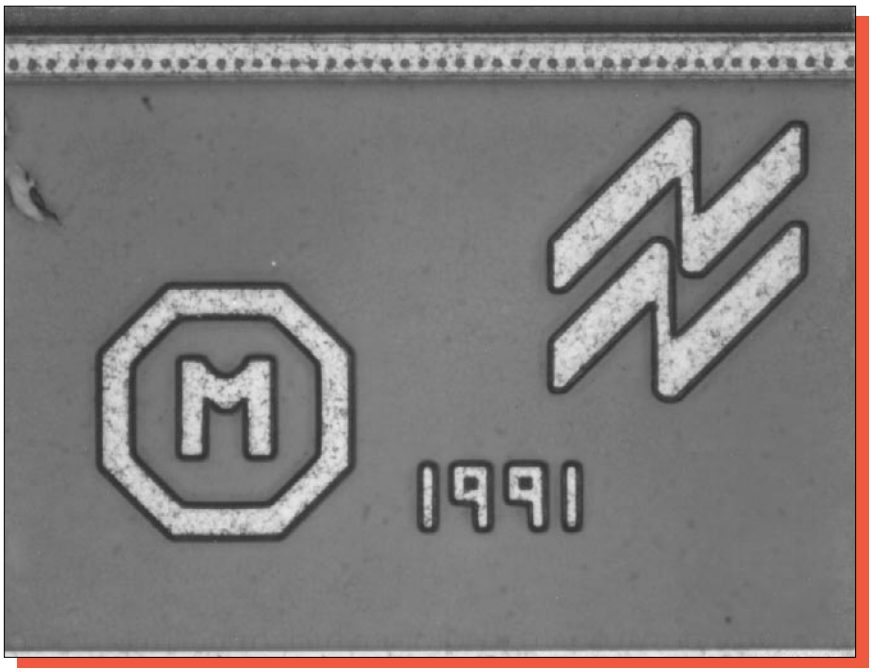
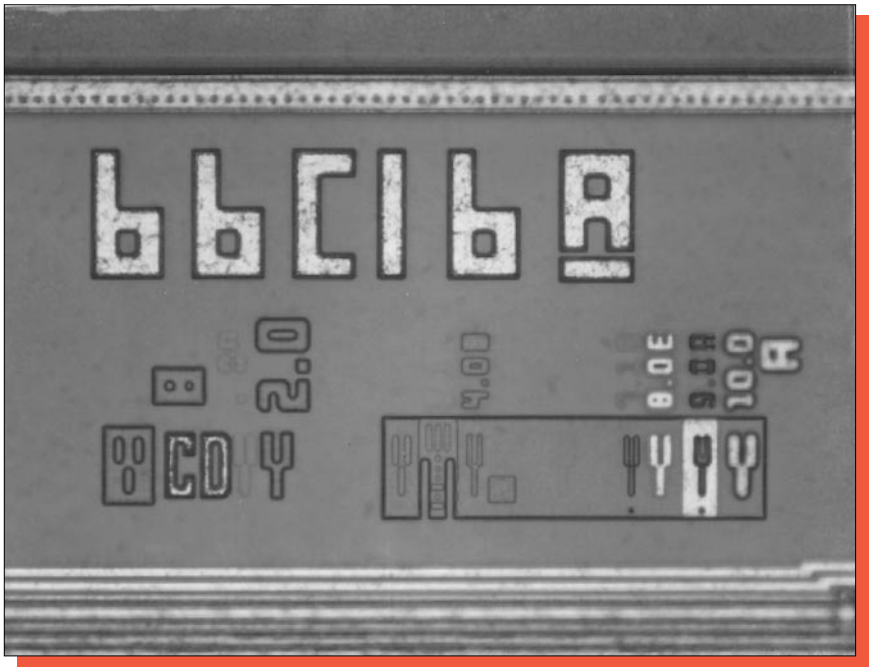


Figure 8. Whole die photograph of the National Semiconductor 16K Serial EEPROM.
Mag. 52x.

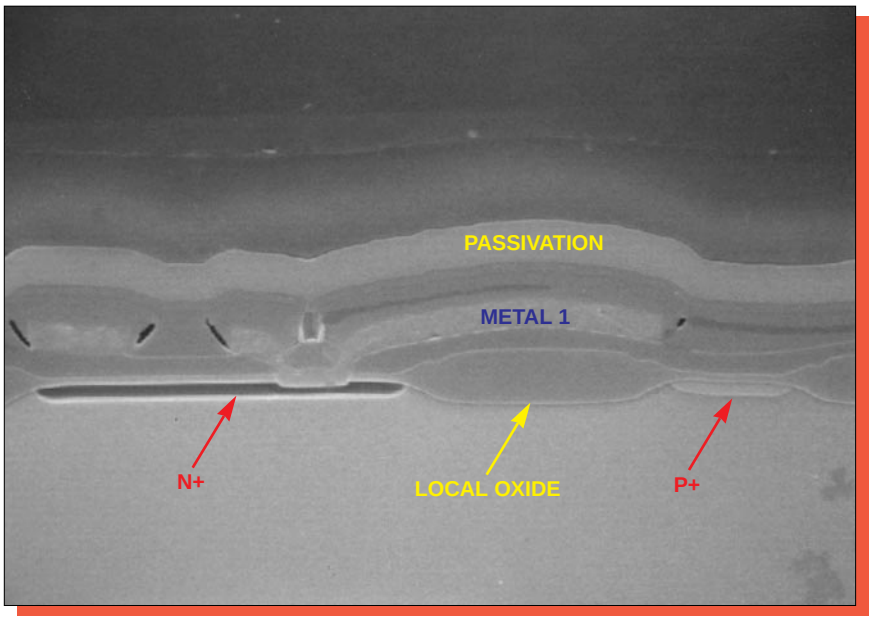


Mag. 500x



Mag. 400x

Figure 9. Die identification markings.



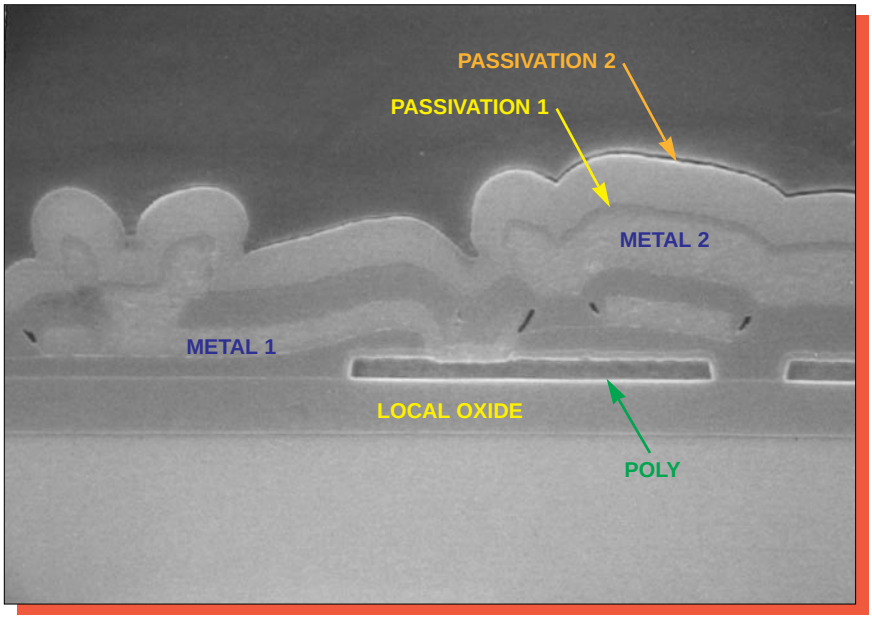
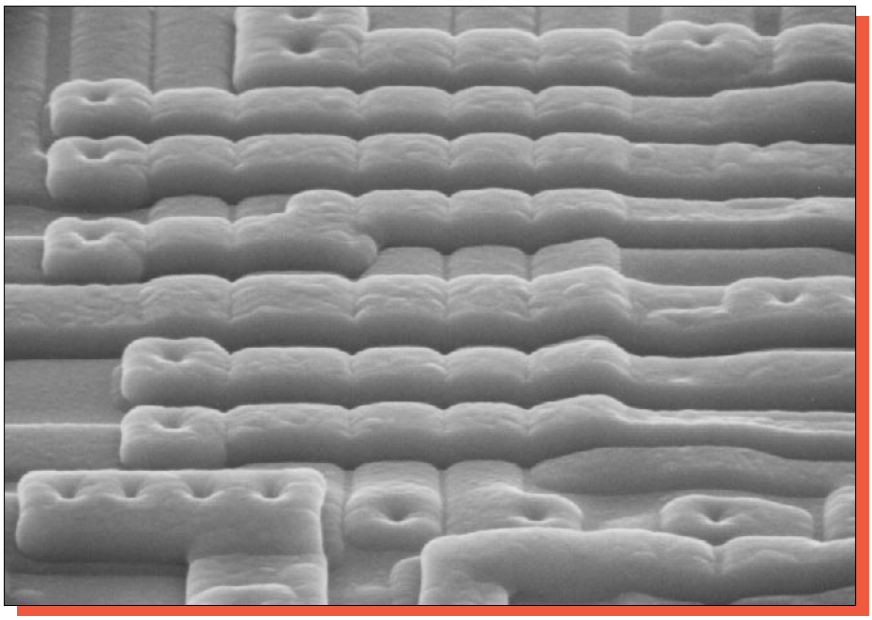
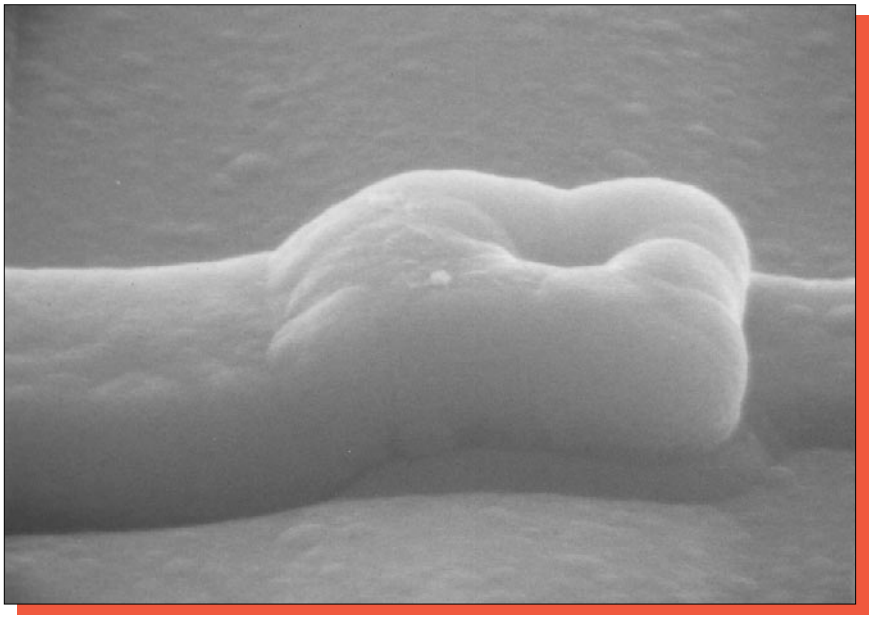


Figure 10. SEM section views illustrating general device structure. Mag. 5500x.

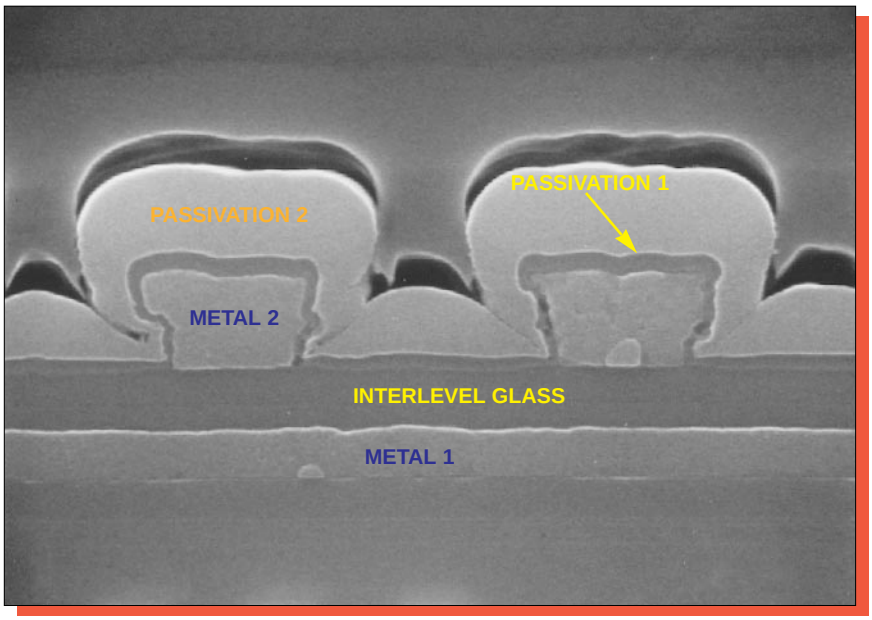


Mag. 2500x

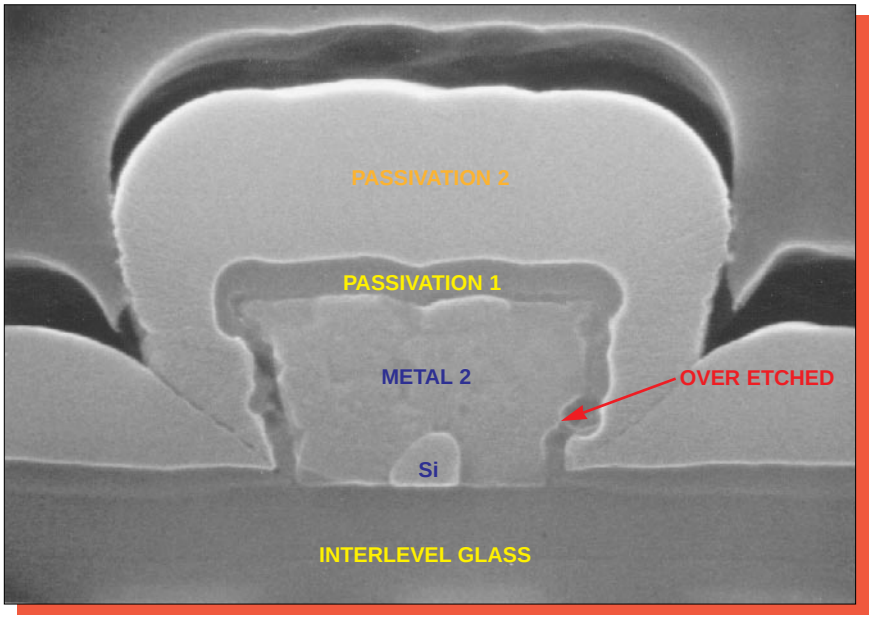


Mag. 10,000x

Figure 11. SEM views of general overlay passivation coverage. 60°.

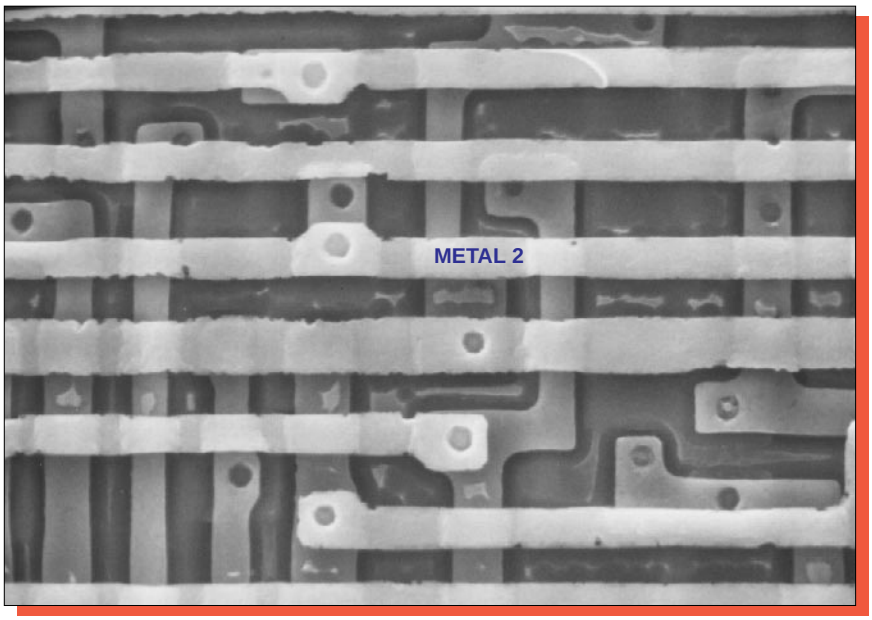


Mag. 10,000x

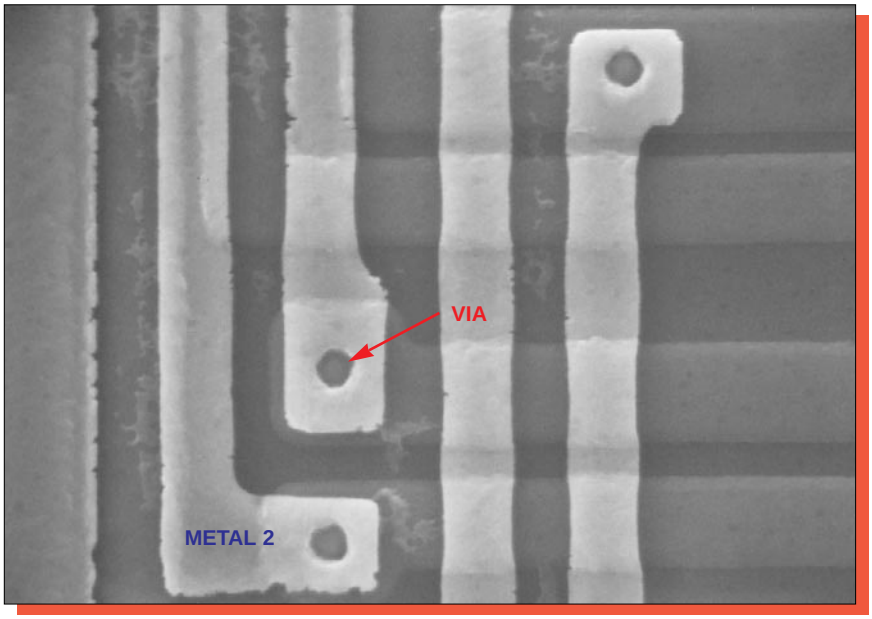


Mag. 20,000x

Figure 12. SEM section views of metal 2 line profiles.

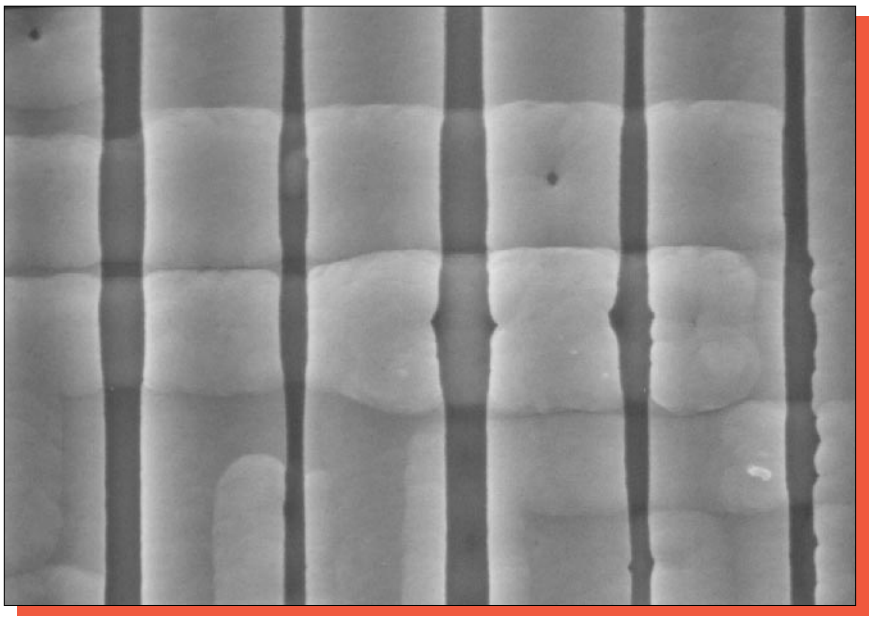


Mag. 2000x

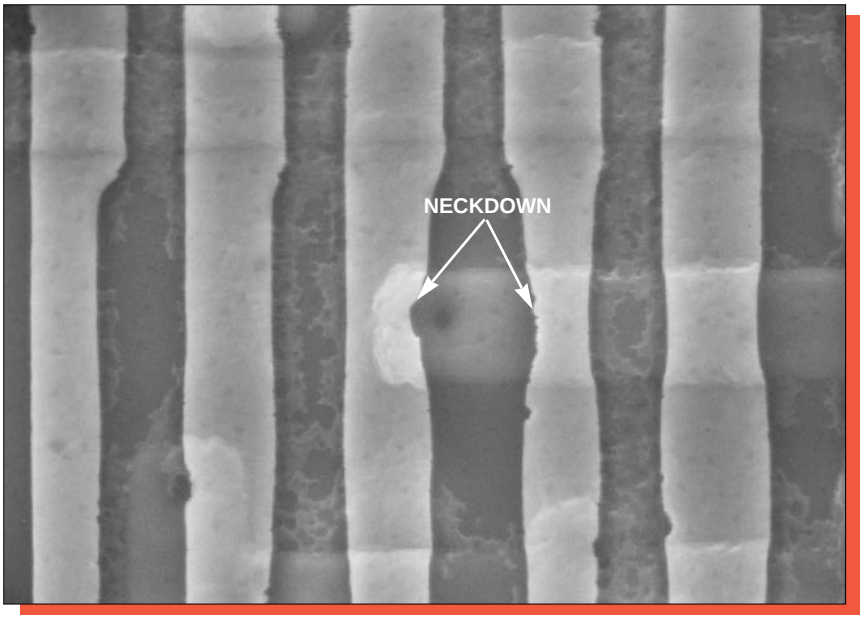


Mag. 3200x

Figure 13. Topological SEM views of metal 2 patterning. 0°.

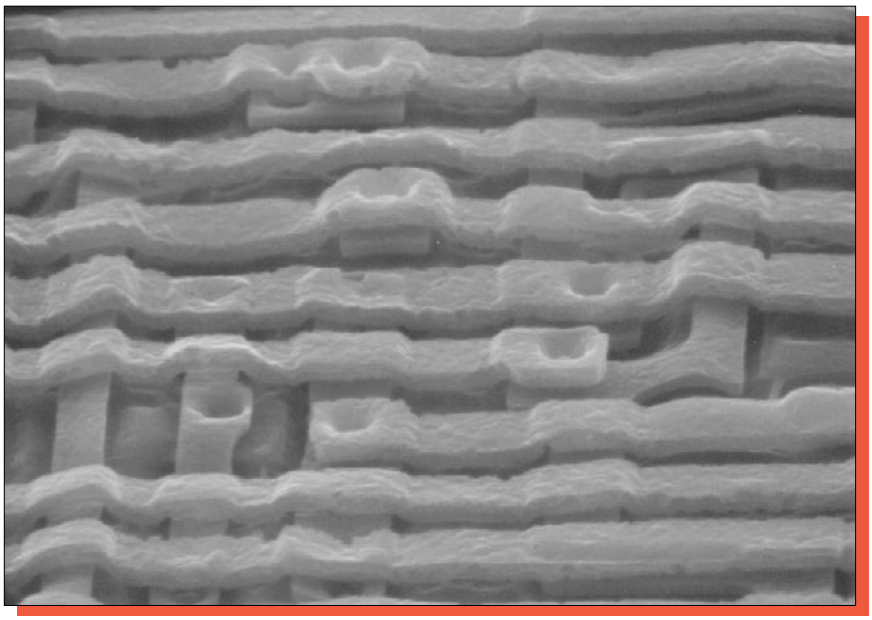


passivation intact

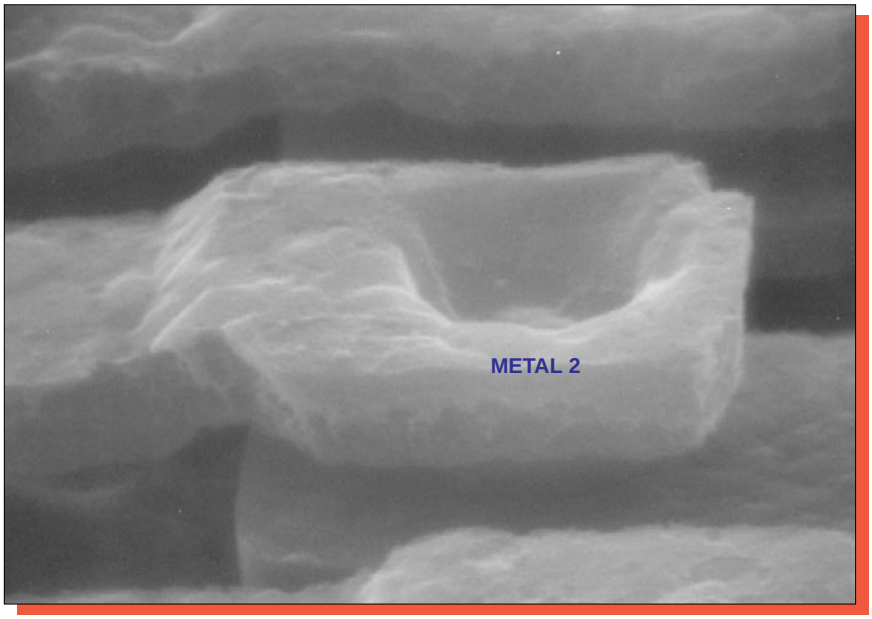


passivation removed

Figure 14. Topological SEM views illustrating “neckdown” in metal 2. Mag. 3250x,0°.

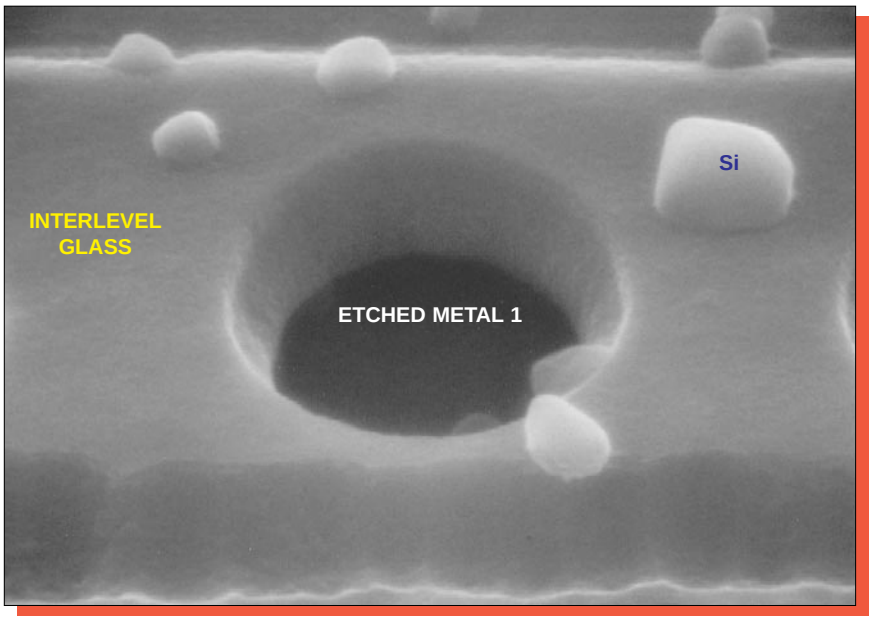


Mag. 3000x

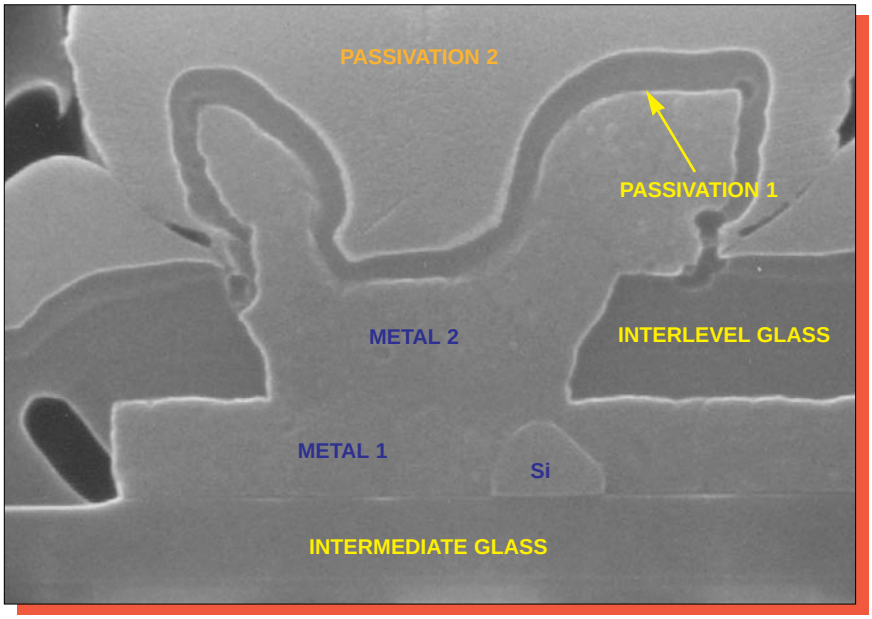


Mag. 15,000x

Figure 15. Perspective SEM views of general metal 2 integrity. 60°.

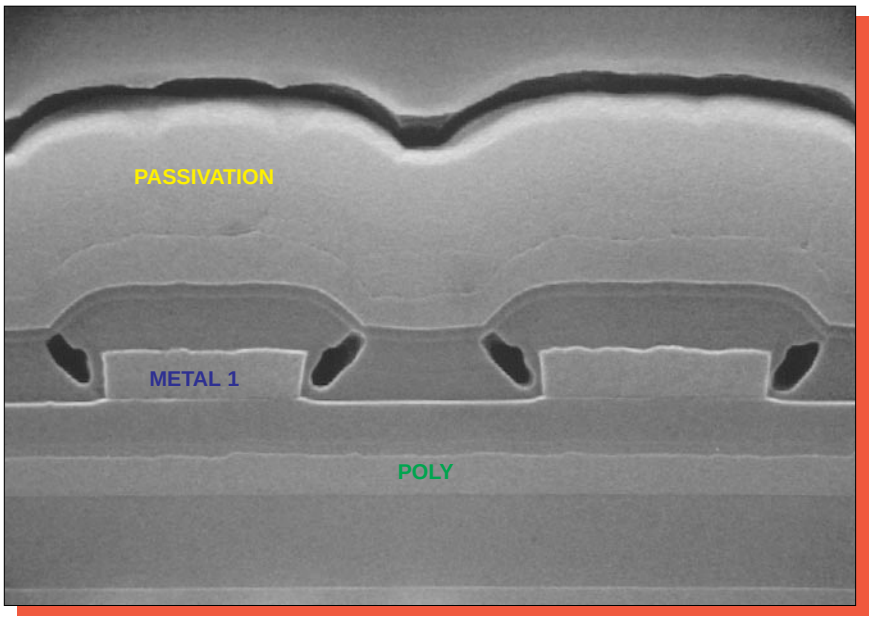


45°

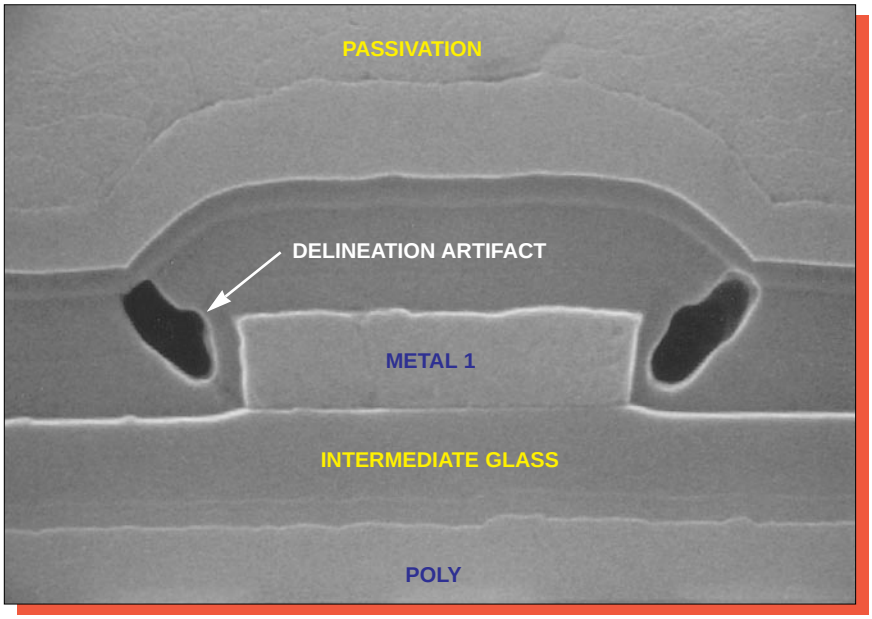


90°

Figure 16. SEM views of metal 2-to-metal 1 vias. Mag. 20,000x.

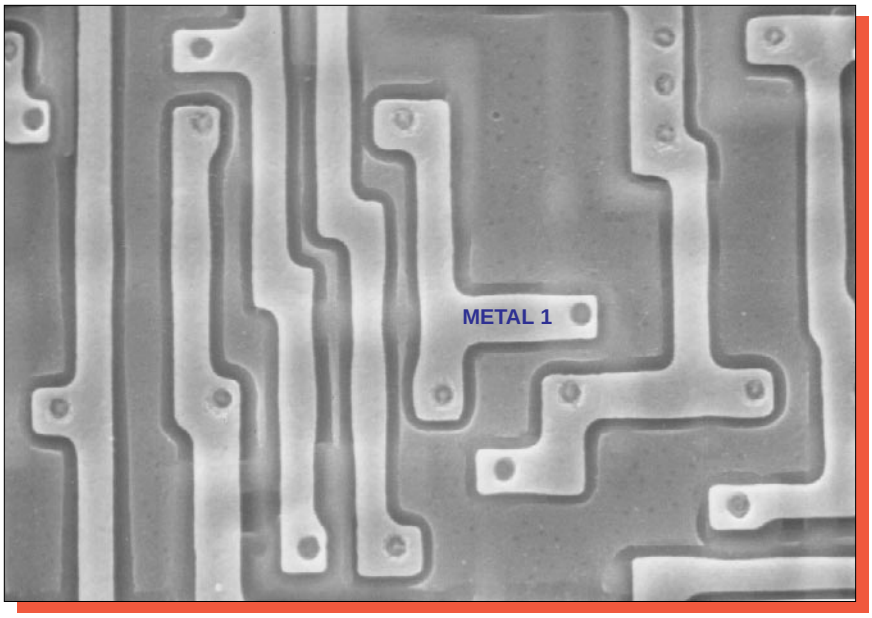


Mag. 10,000x

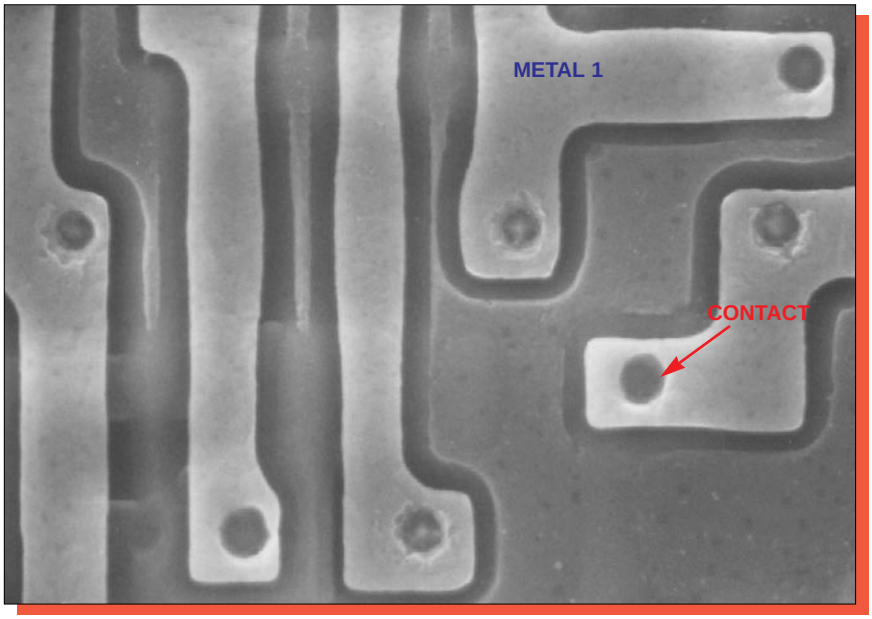


Mag. 20,000x

Figure 17. SEM section views of metal 1 line profiles.

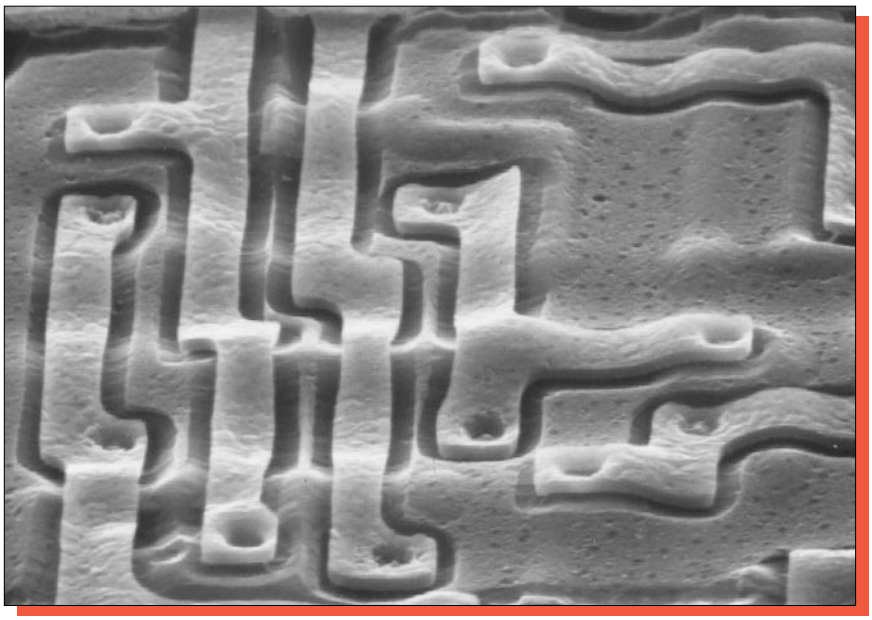


Mag. 2000x

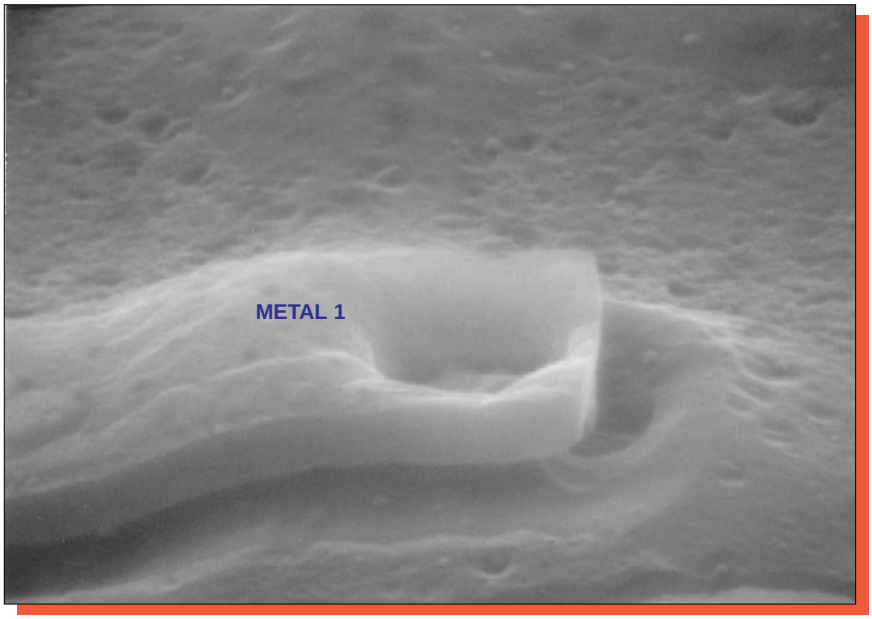


Mag. 4000x

Figure 18. Topological SEM views of metal 1 patterning. 0°.

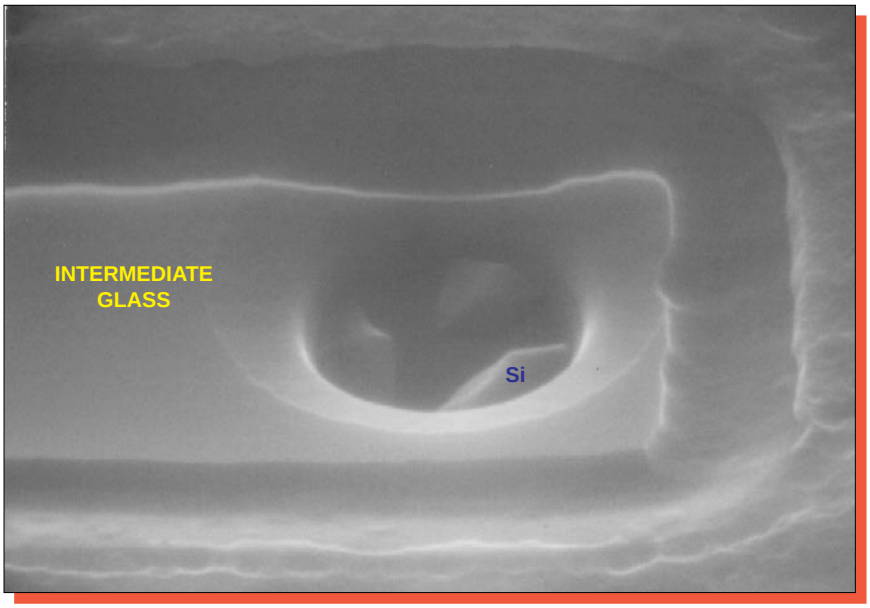


Mag. 3300x

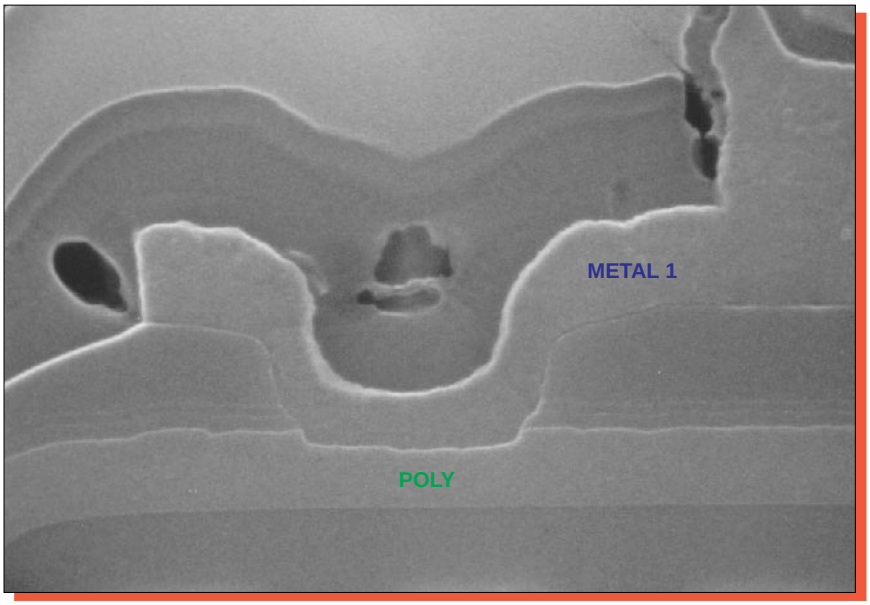


Mag. 15,000x

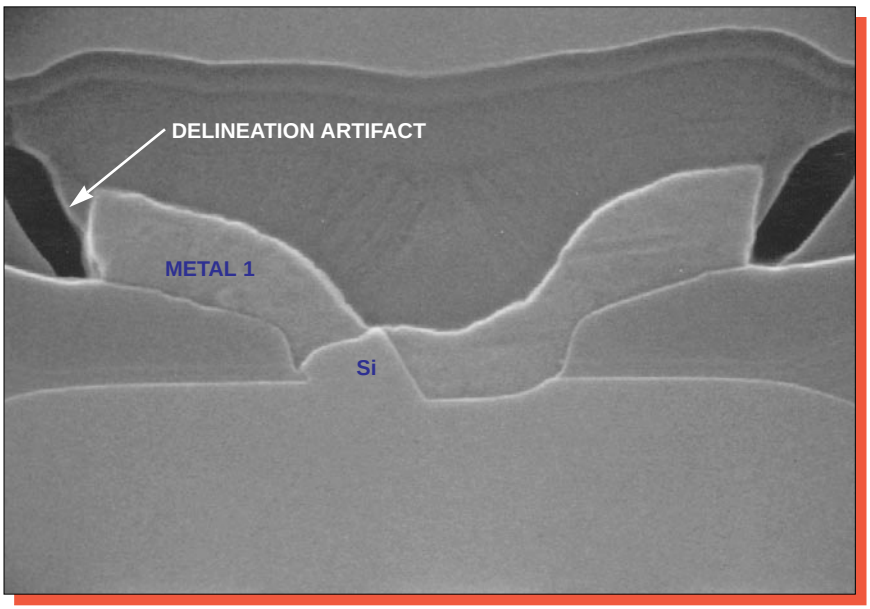
Figure 19. Perspective SEM views of general metal 1 integrity. 60°.



45°

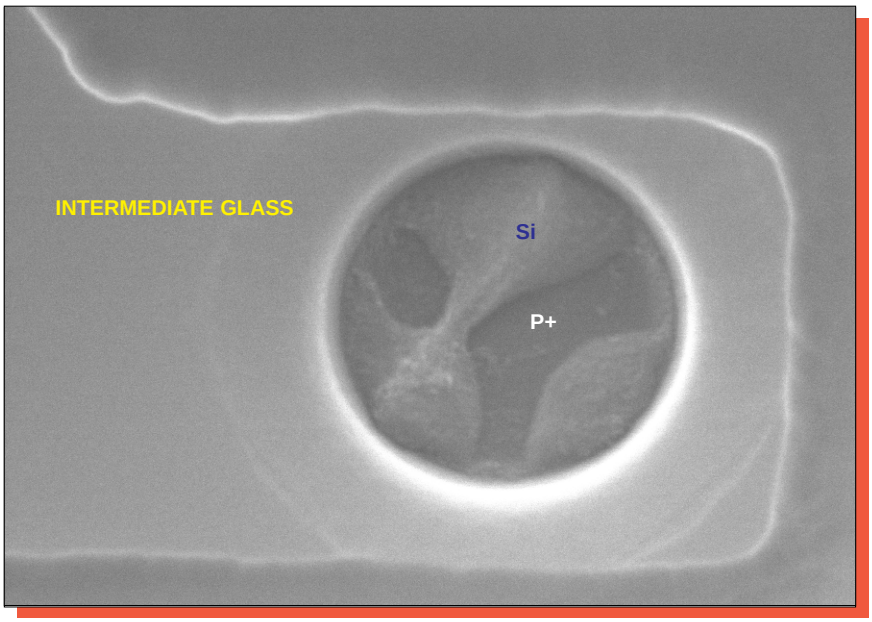


glass etch,
metal 1-to-poly



glass etch,
metal 1-to-diffusion

Figure 20. SEM surface and section views of typical metal 1 contacts. Mag. 20,000x



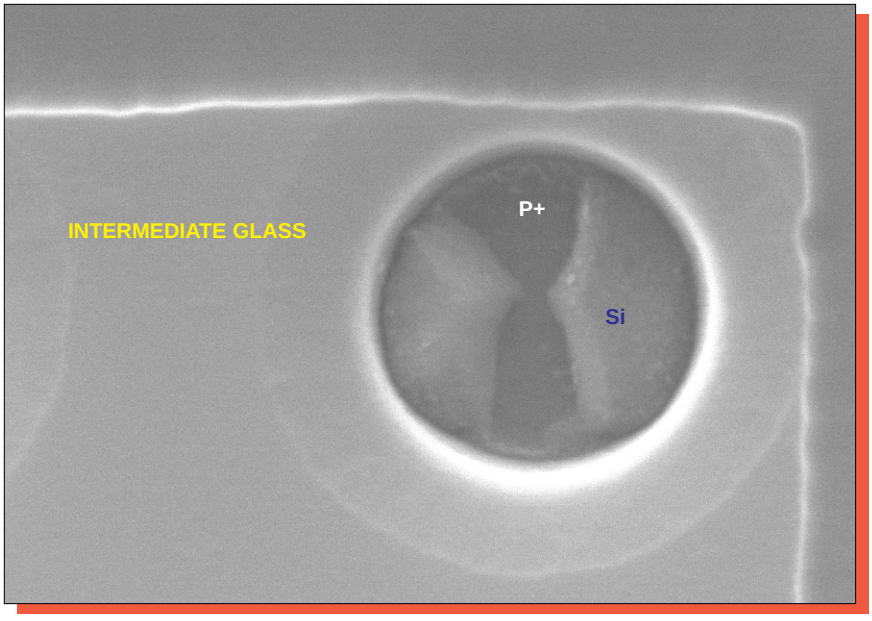
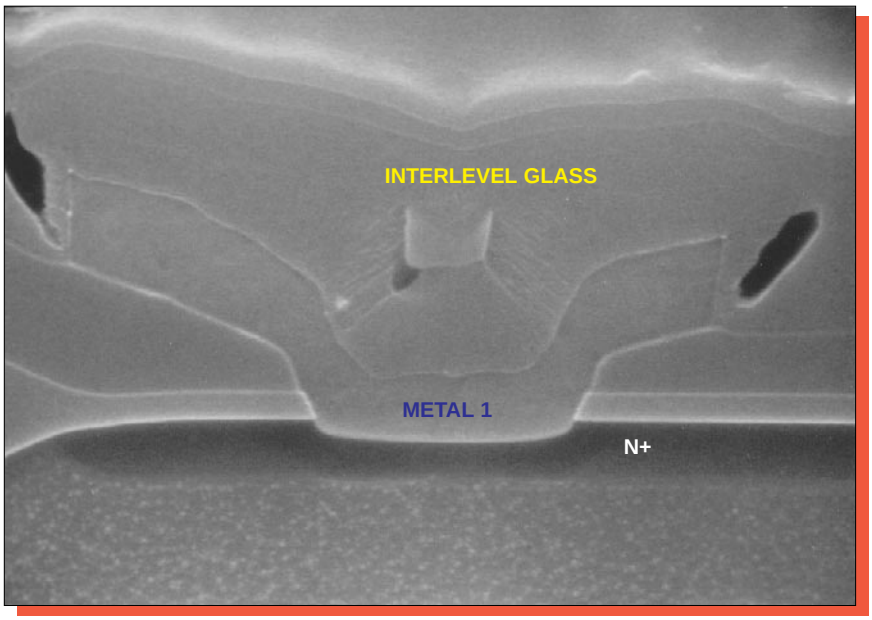
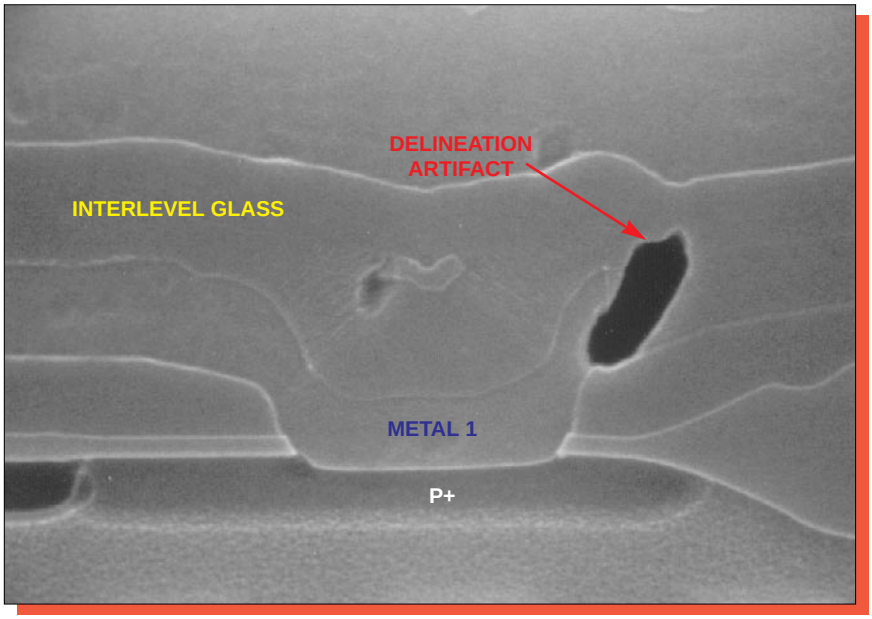


Figure 20a. Topological SEM views of P+ contacts illustrating silicon mound growth. Mag. 22,000x, 0°.

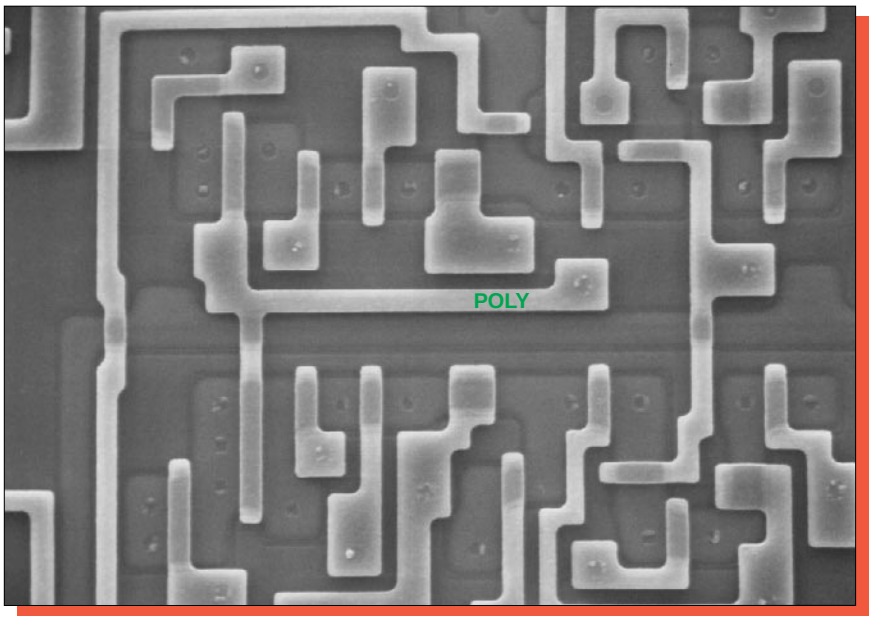


metal 1-to-N+

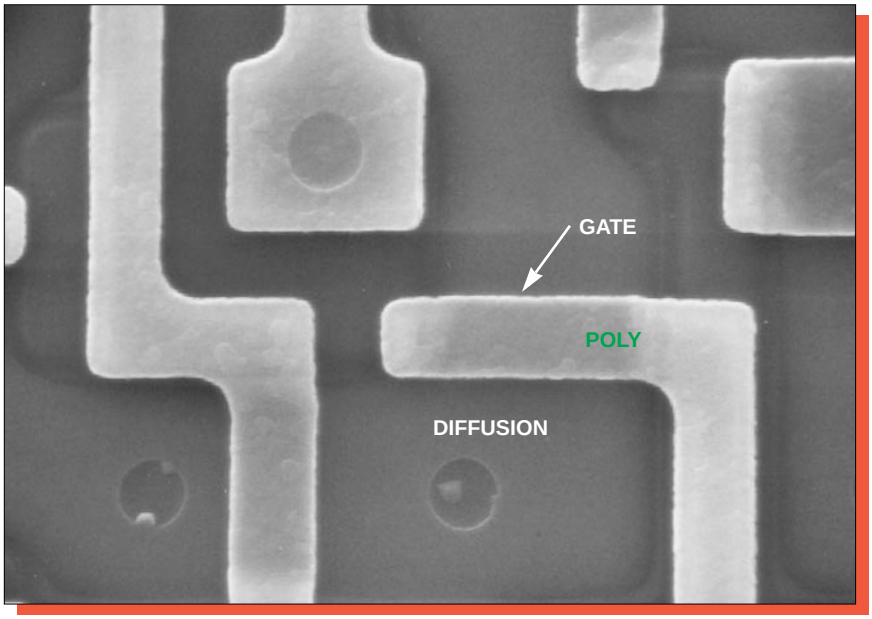


metal 1-to-P+

Figure 21. SEM section views of metal-to-diffusion contacts. Mag. 20,000x.

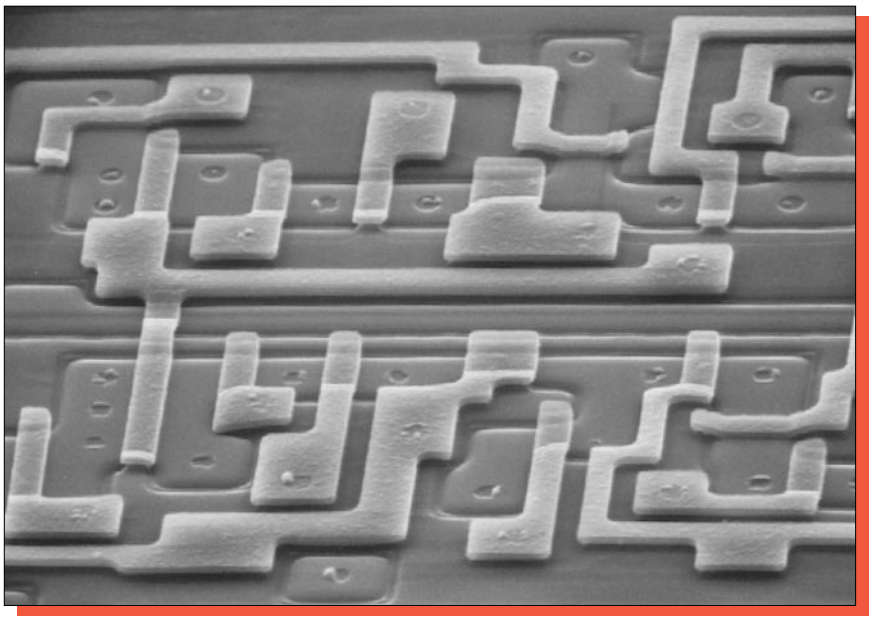


Mag. 1300x

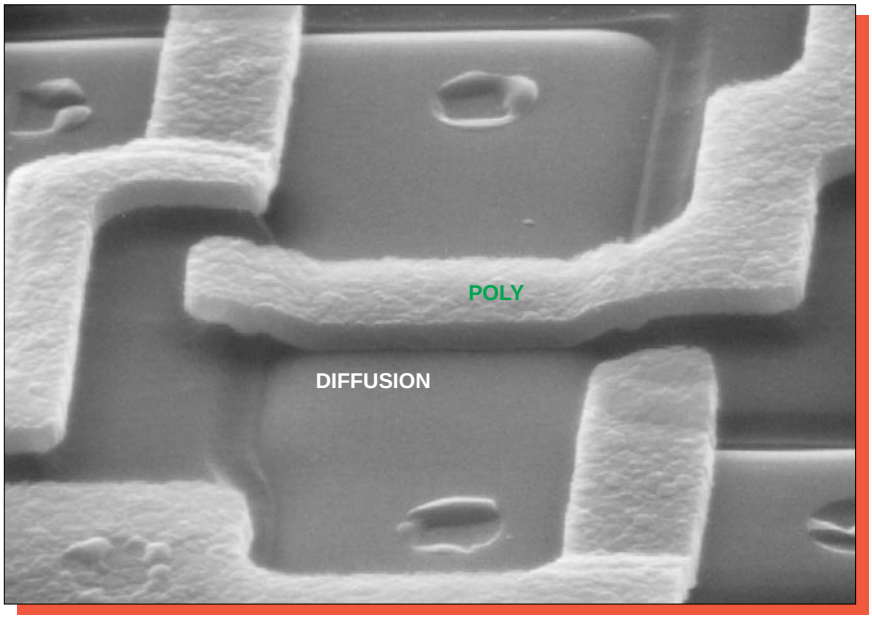


Mag. 5200x

Figure 22. Topological views of poly patterning. 0°.

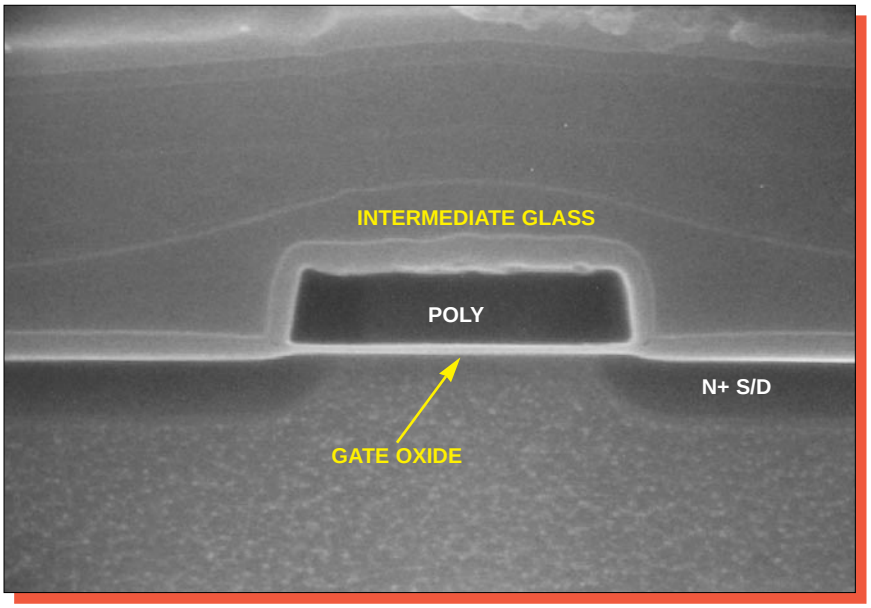


Mag. 2000x

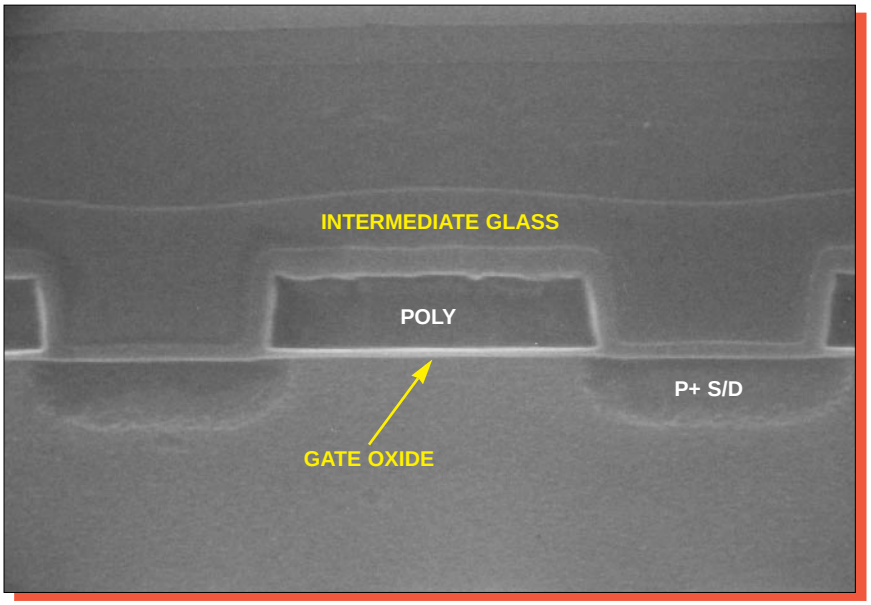


Mag. 8000x

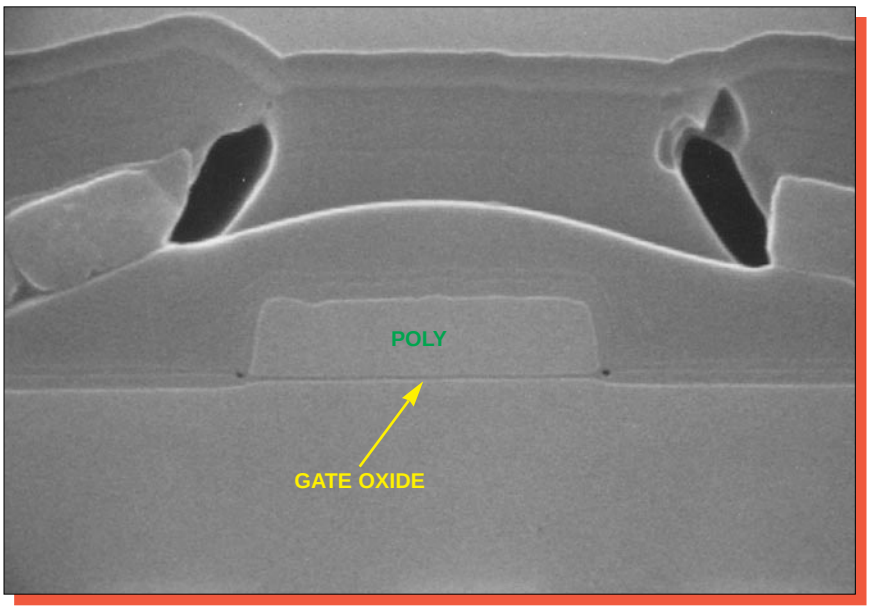
Figure 23. Perspective SEM views of poly coverage. 60°.



N-channel



P-channel



glass etch

Figure 24. SEM section views of typical transistors. Mag. 20,000x.

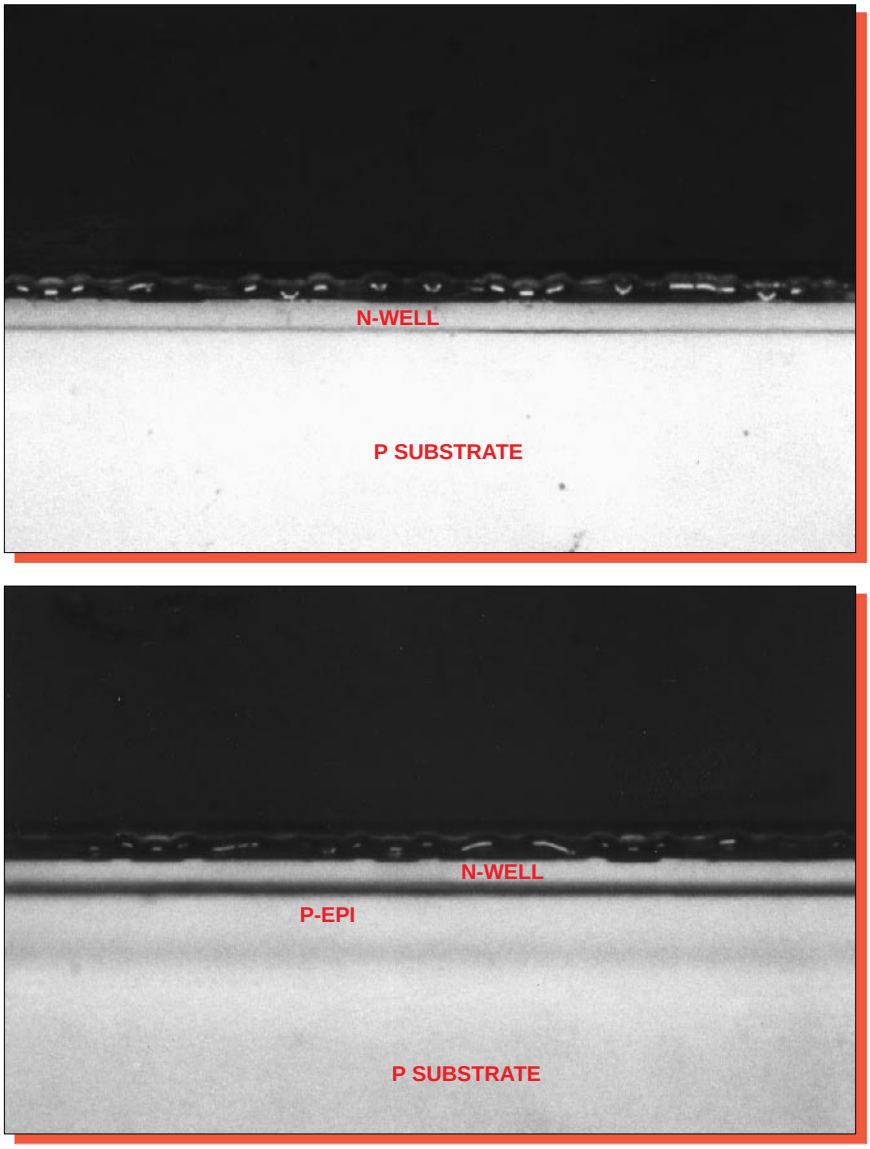


Figure 25. Optical views of the well and epi structure. Mag. 500x.

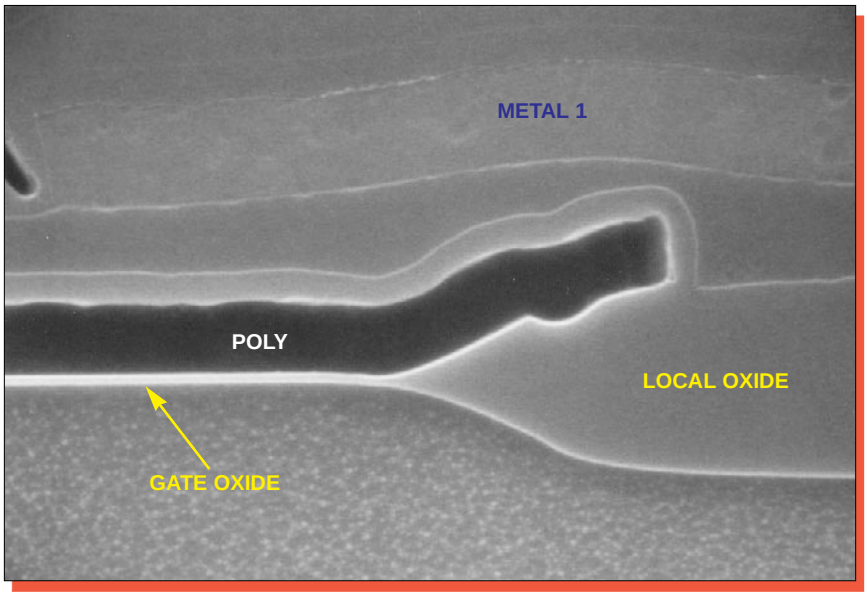
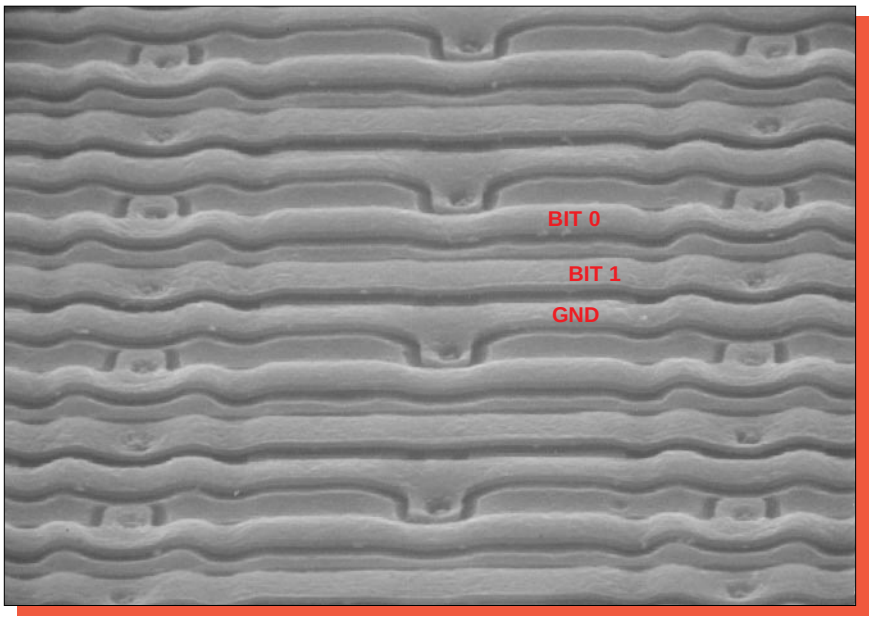
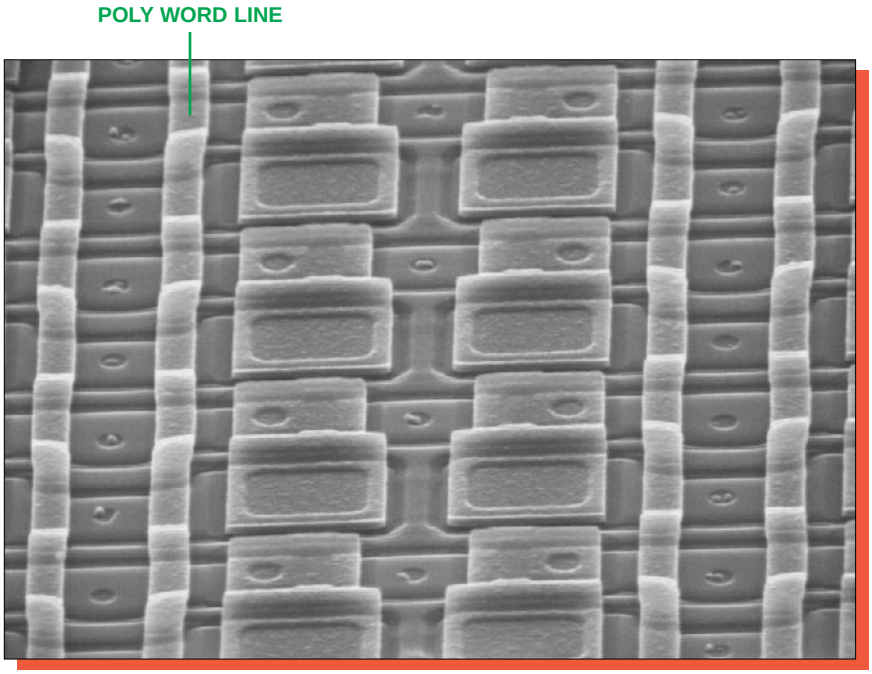


Figure 26. SEM section view of a local oxide birdsbeak. Mag. 20,000x.

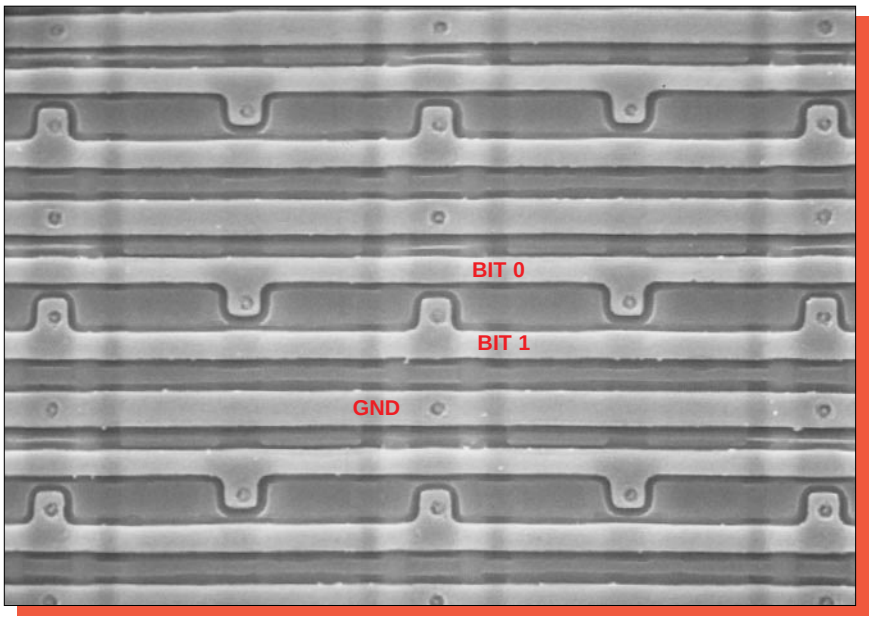


metal 1

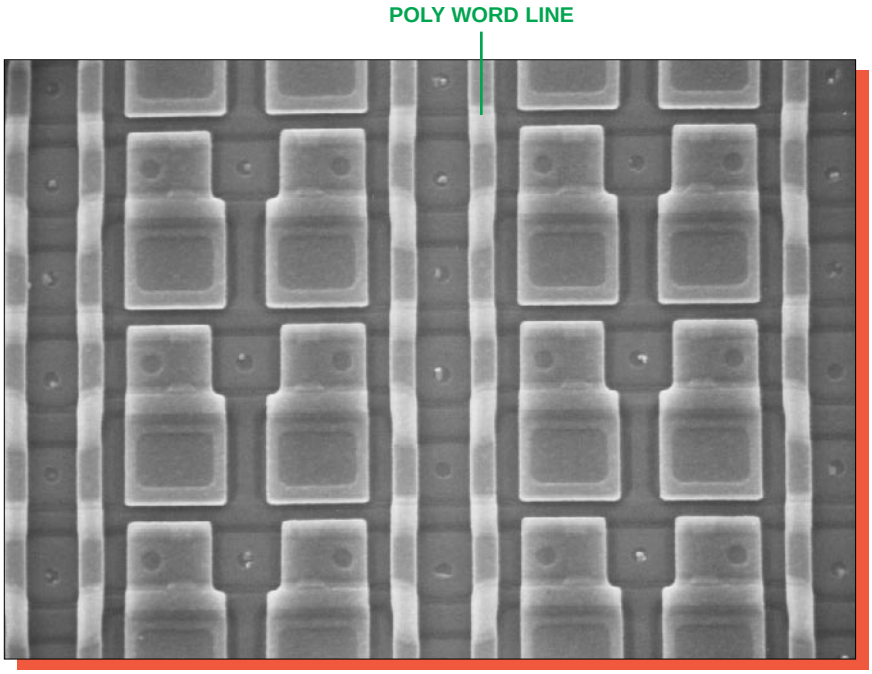


delayered

Figure 27. Perspective SEM views of the EEPROM cell array. Mag. 20,000x, 60°.

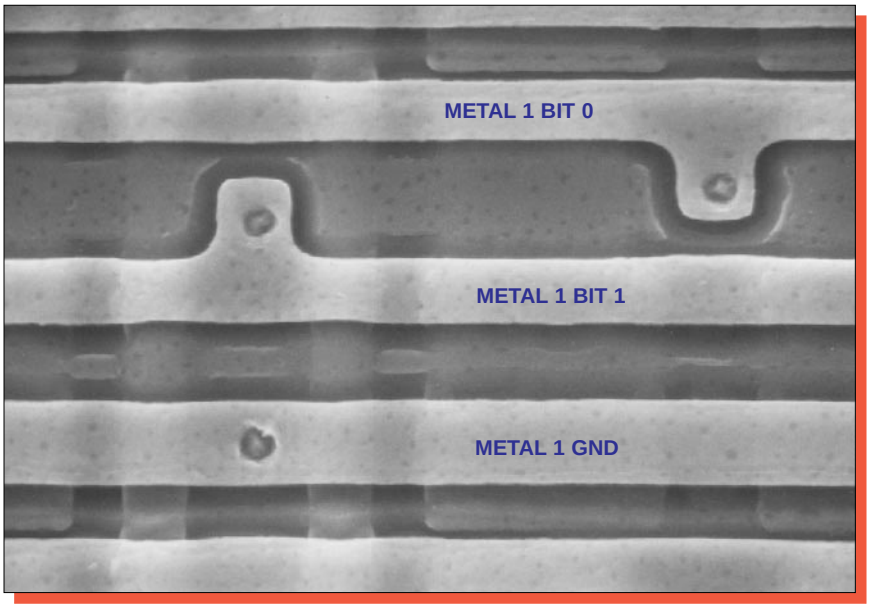


metal 1

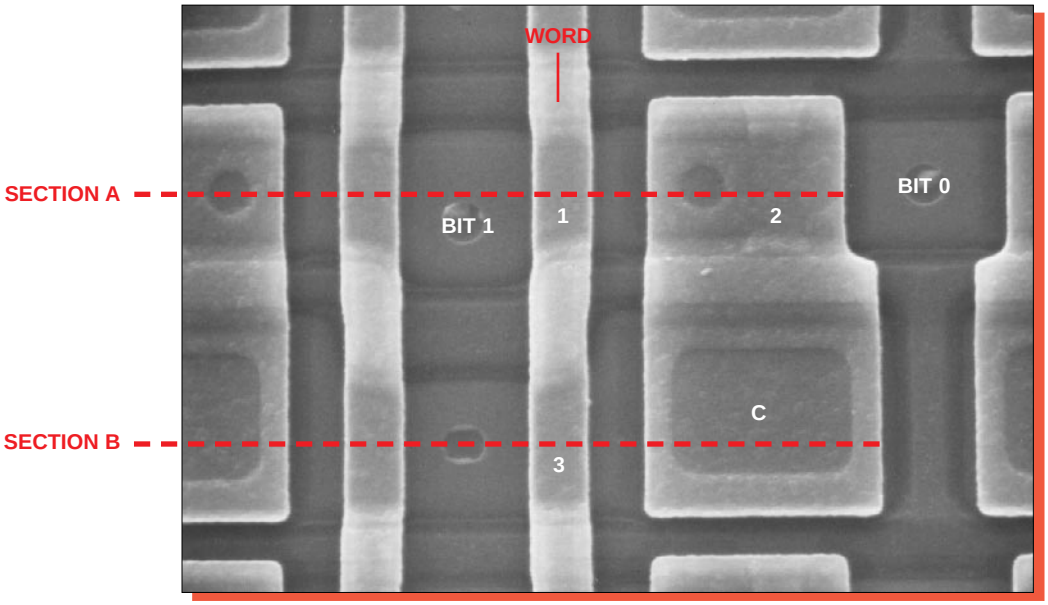


delayered

Figure 28. Topological SEM views of the EEPROM cell array. Mag. 1300x, 0°.



metal 1



delayered

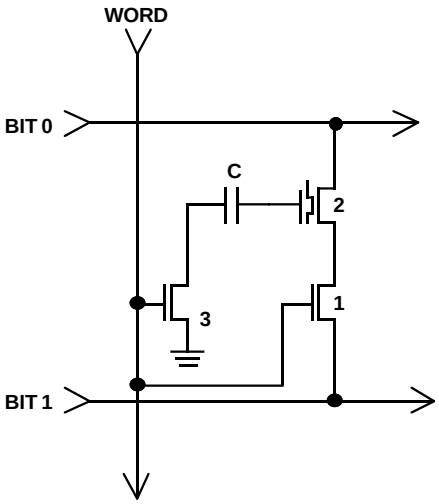
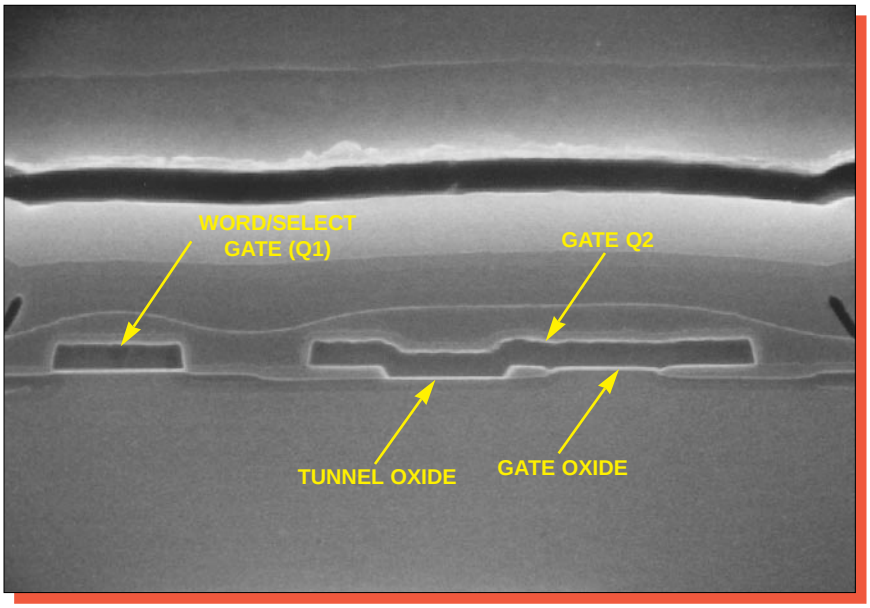
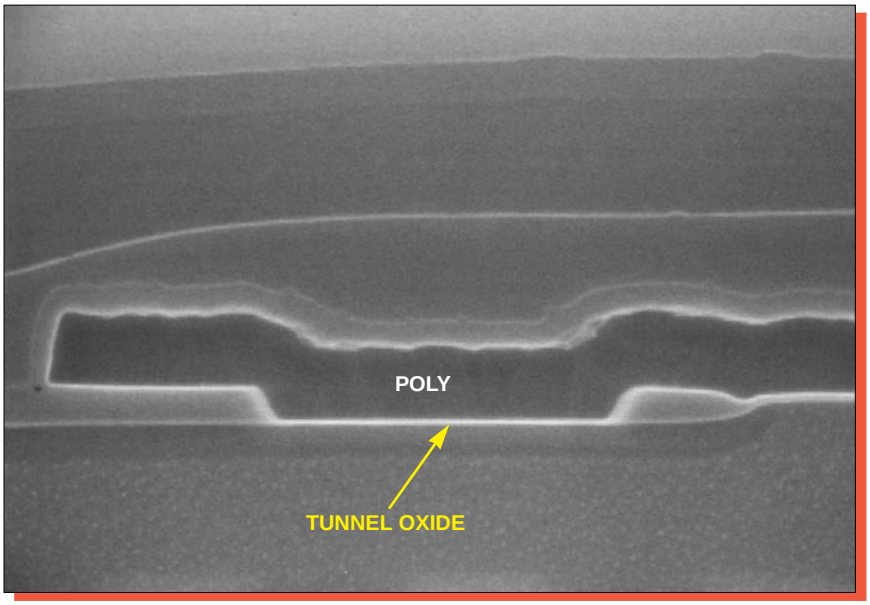


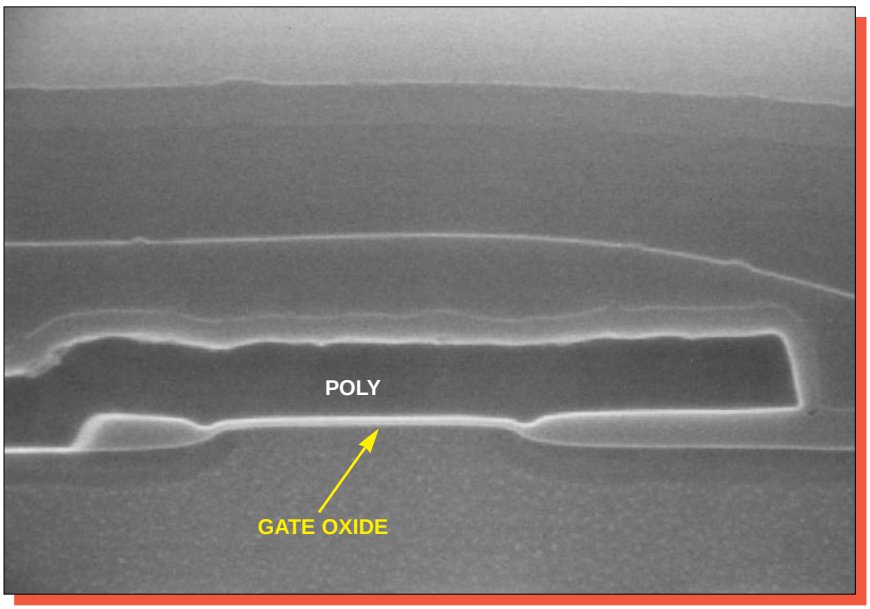
Figure 29. Topological SEM views and schematic of an EEPROM cell. Mag. 3100x, 0°.



Mag. 6750x

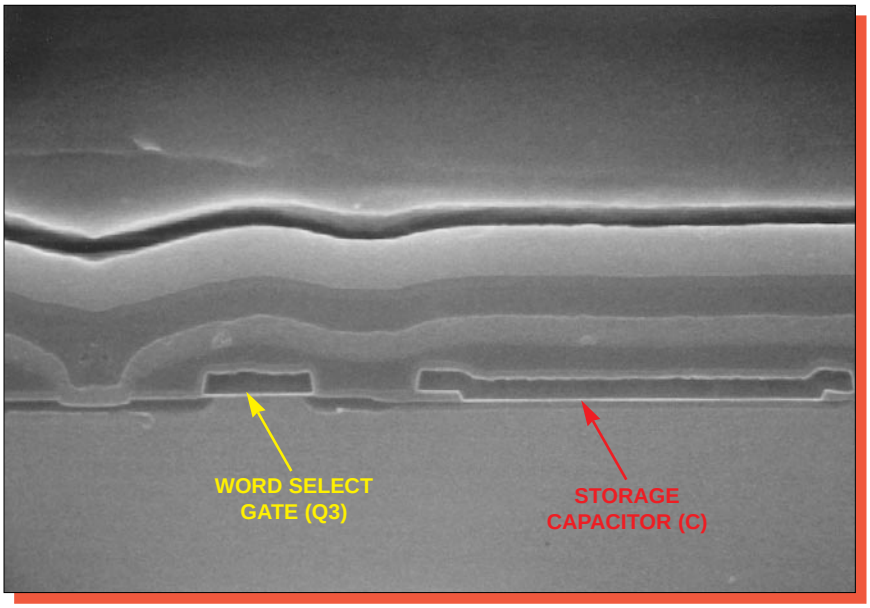


Mag. 20,000x

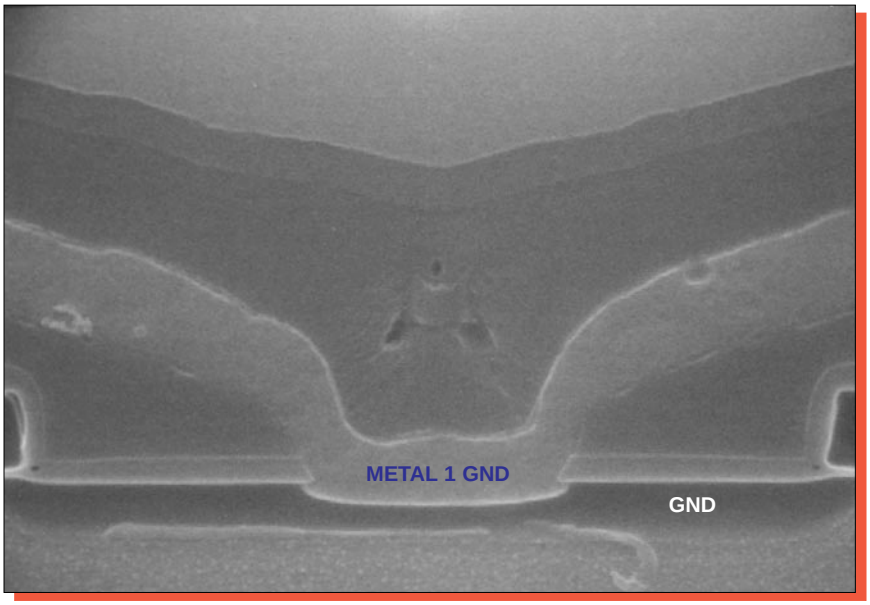


Mag. 20,000x

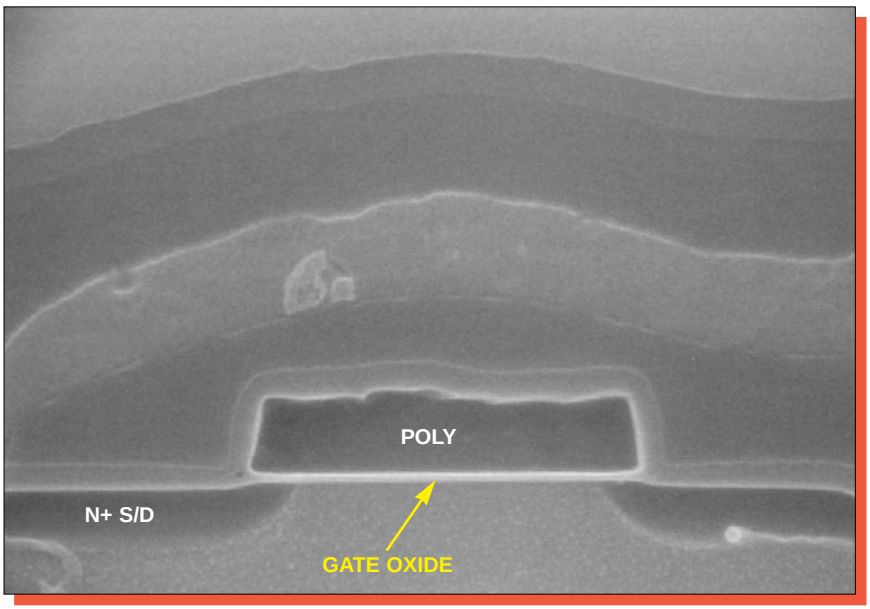
Figure 30. Detailed SEM section views of the EEPROM cell (Section A).



Mag. 5500x



Mag. 20,000x



Mag. 20,000x

Figure 31. SEM section views of the EEPROM cell (Section B).

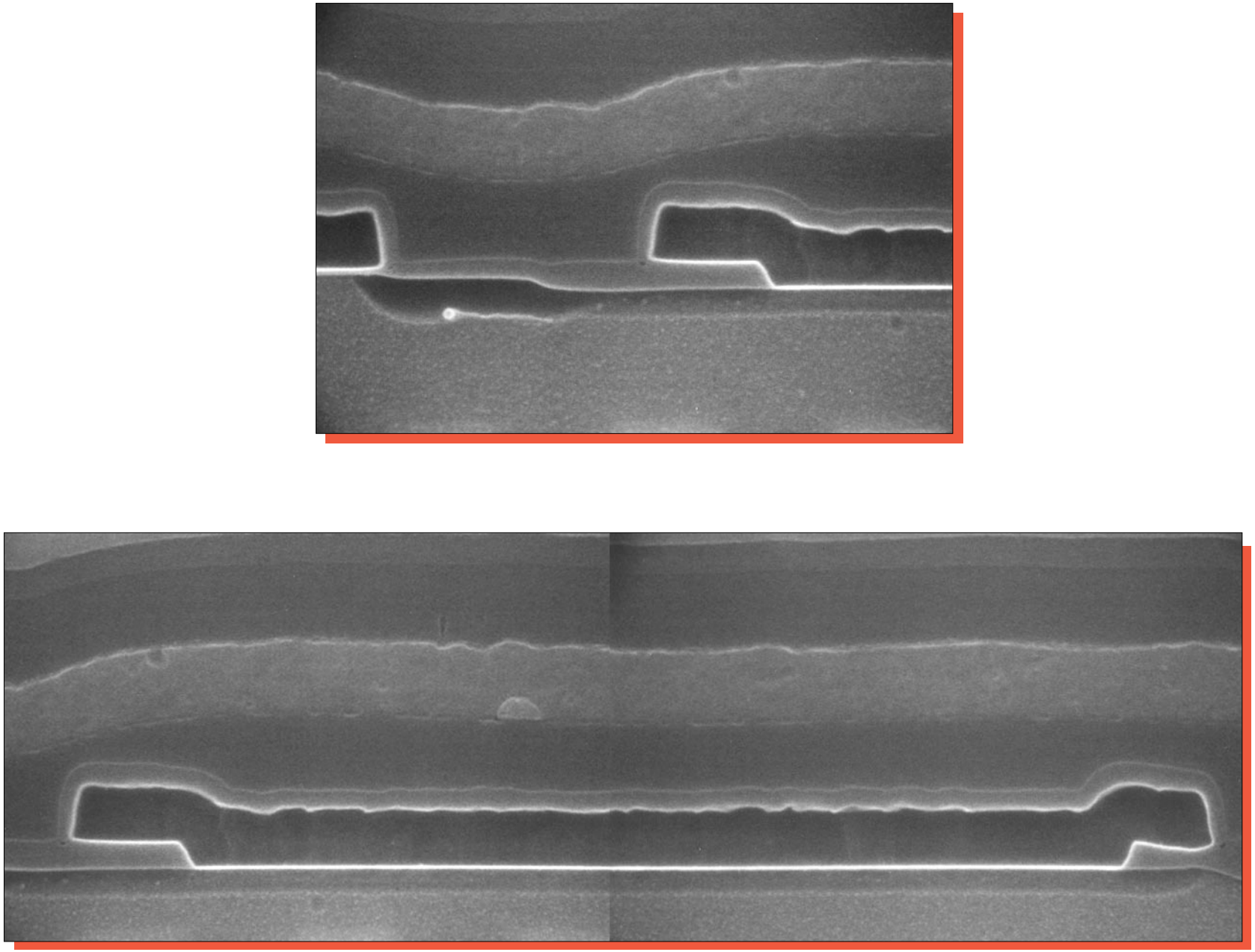
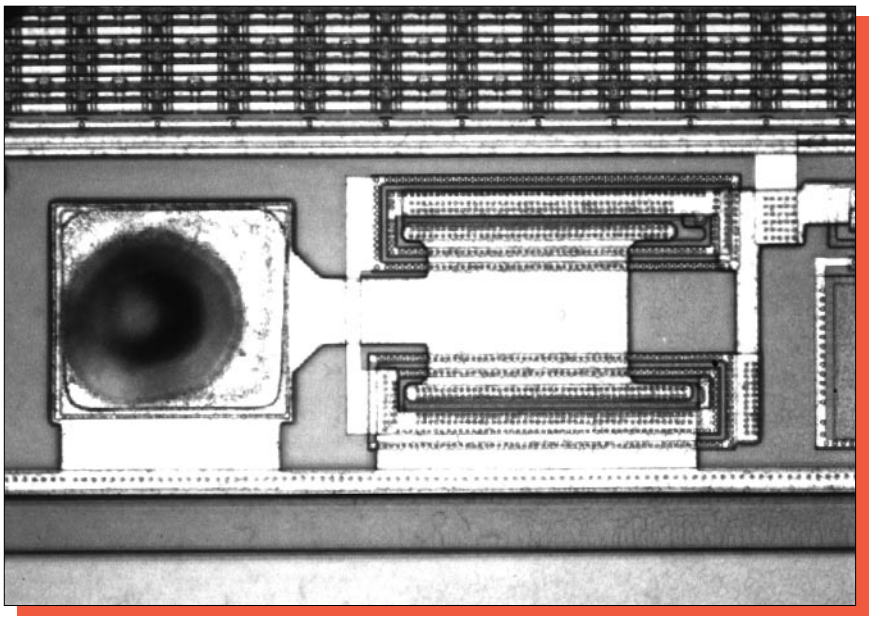


Figure 32. Detail of gate 3 to capacitor interface area. Mag. 20,000x.



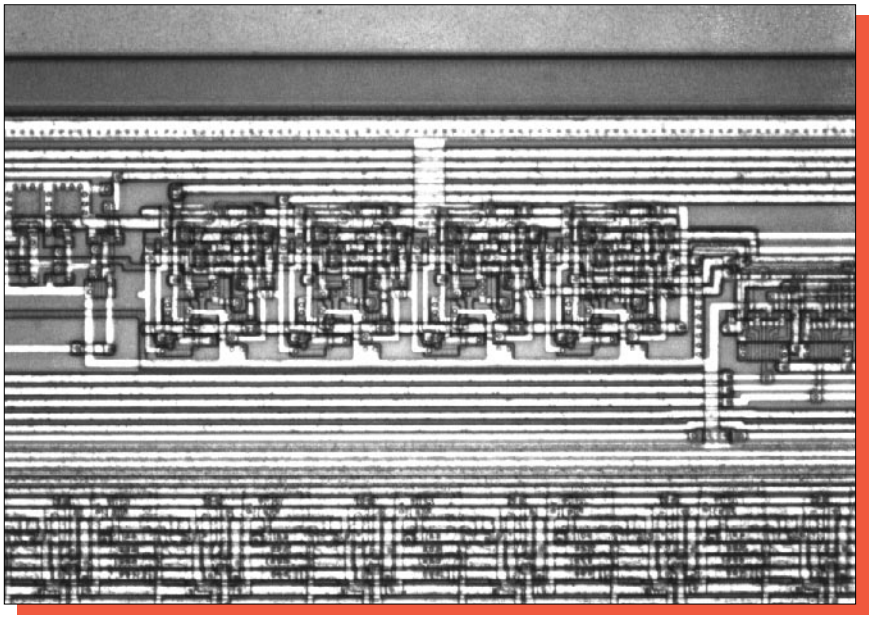
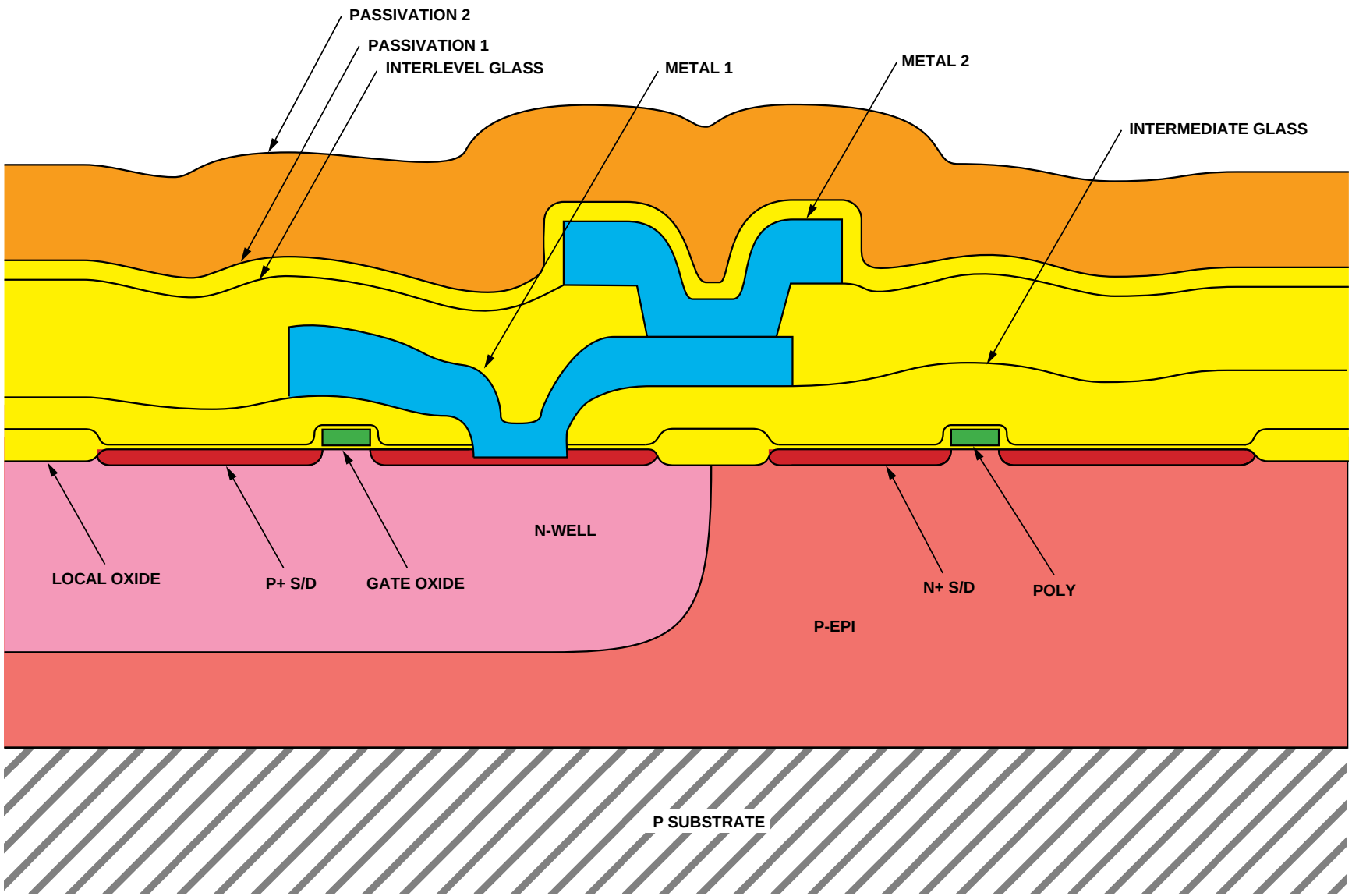


Figure 33. Optical views of input protection and general device circuitry. Mag. 260x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 34. Color cross section drawing illustrating device structure.