

Construction Analysis

Atmel AT27C010-45DC 1Mbit EPROM

Report Number: SCA 9504-408



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INTRODUCTION

This report describes a construction analysis of the Atmel AT27C010-45DC, 1 Mbit EPROM (UV or one time programmable EPROM). One device was supplied for the analysis. It was packaged in a 32-pin CERDIP which was received delidded. The device was date coded 9428.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

- Tungsten plugs used at contacts.
- Titanium silicide employed on poly 2 and diffusions (salicide process).
- Planarized passivation.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Assembly:

- The device was packaged in a 32-pin, CERDIP package (previously delidded).
- Silver-glass die attach was used to mount the die to the cavity.
- Die separation by sawn dicing (full depth).
- Wirebonding by the ultrasonic wedge bond method using 1.3 mil aluminum wire.
- Multiple wires were used at power pins.
- Pin 30 was not connected.
- A bonding post was employed in the package cavity.

Die Process

- Fabrication process: Selective oxidation twin-well CMOS process in a P substrate (no epi used).
- Final passivation: Two layers of what appeared to be silicon-dioxide (possibly undoped). The first layer was planarized.
- Metallization: A single level of metal defined by a dry-etch technique. Metal consisted of aluminum with a titanium-nitride barrier. Tungsten plugs were employed at contacts.
- Intermediate glass: A single layer of CVD reflow glass over various grown/densified oxides. The CVD glass was reflowed prior to contact cuts.
- Polysilicon: Two layers of polysilicon were employed. Polycide (poly 2 and titanium silicide) was used to form word lines in the cell array and all standard gates

TECHNOLOGY DESCRIPTION (continued)

on the die. Poly 1 was used to form the floating gates in the array. The interpoly dielectric consisted of oxide only (no nitride).

- Diffusions: Standard N+ and P+ diffusions formed the sources/drains of transistors. Titanium silicide was present on the diffusions (salicide process). Oxide sidewall spacers were used to provide the LDD spacing and were left in place.
- No buried contacts were employed.
- Wells: Apparent twin-wells in a P substrate. A slight step was noted in the oxide at the edge of the N-well which may indicate a twin-well process was employed. No epi was used.
- Memory cells: The memory cells consisted of a "stacked dual gate" EPROM-based design. Polycide formed the word lines, poly 1 formed the floating gates and metal formed the bit lines. As mentioned, the interpoly dielectric was oxide only (no nitride).
- Special design items: No slots or beveled corners (to reduce stress) were noted in any of the bus lines. All contacts were the same diameter, no bus line contacts were elongated. Some metal lines had small "pads" for probing purposes (see Figure 6).

ANALYSIS RESULTS I

Assembly:

Figures 1 - 3

Questionable Items:¹ None.

Special Features: None.

General Items:

- Overall package quality: Could not be evaluated since the device was received delidded.
- Die attach: Silver-glass of normal quality. No significant voids were noted.
- Die dicing: Die separation was by full depth sawing and showed normal quality workmanship. No large chips or cracks were present at the die surface. Edge seal was good as the passivation extended into the scribe lane to seal the metallization.
- Wirebonding: Ultrasonic wedge bond method using 1.3 mil aluminum wire. Bonds were well formed and placement was good. All bond pull strengths were normal and no bond lifts occurred (see page 10).

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 4 - 27

Questionable Items:¹ None.

Special Features:

- Tungsten plugs used at contacts.
- Titanium silicide employed on poly 2 and diffusions (salicide process).
- Planarized final passivation.

General Items:

- Fabrication process: Selective oxidation CMOS process with apparent twin-wells in a P substrate (no epi was used). No significant problems were found in the basic process.
- Design implementation: Die layout was clean and efficient. Alignment/registration was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: Two layers of what appeared to be silicon-dioxide (possibly undoped glass). The first layer was planarized. An integrity test indicated defect-free passivation. Edge seal was also good, as the passivation extended into the scribe lane to seal the metallization. No die coat was used on this device.
- Metallization: A single level of metallization. Metal consisted of aluminum with a titanium-nitride barrier. The metal layer was defined by a dry etch of good quality. Tungsten plugs were used at contacts.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II (continued)

- Metal defects: None. No voids or cracks were noted in the aluminum. Metal coverage of contact plugs was normal (90 percent coverage). No silicon nodules were found following aluminum removal.
- Metal step coverage: Metal (aluminum) coverage was good. Virtually no thinning of the metal was present due to the use of tungsten plugs. MIL-STD-883D allows up to 70 percent metal thinning at contacts of this size.
- Contacts: No over-etching or other defects were found at contacts.
- Intermediate glass: A layer of CVD reflow glass over various grown oxides. This layer was reflowed prior to contact cuts. No problems were found.
- Polysilicon: Two layers of polysilicon. Polycide (poly 2 and titanium silicide) was used to form all standard gates on the die and the word lines in the array. Numerous inactive(?) polycide gates were also present at the guardbands (i.e., poly crossed guardband diffusions on gate oxide) see Figure 14. This is not a standard design feature. Poly 1 was used to form the floating gates in the cell array. Definition of the poly layers was by a dry etch of good quality.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere.
- Diffusions: N+ and P+ implants were used for sources and drains. Titanium was sintered into the diffusions to reduce series resistance (salicide process). An LDD process (to reduce hot electron effects) was used employing oxide sidewall spacers. The spacers were left in place. No problems were found in any of these areas.
- Wells: Apparent twin-wells were used in a P substrate. The P-well could not be delineated; however, a small oxide step was noted at the edge of the N-well which may indicate a twin-well process was employed. Definition was normal. No epi was used.
- Buried contacts: None used.

ANALYSIS RESULTS II (continued)

- Memory Cells: The memory cells consisted of a "stacked dual gate" EPROM-based design. Polycide word lines, poly 1 formed the floating gates, and metal formed the bit lines. The dielectric between the gates consisted of oxide only. Cell pitch was 2.1 x 2.1 microns.
- Input protection: Standard diffusions (no deep diffusions) were used at the input protection structure. No poly was present under the bond pads.

PROCEDURE

The device was subjected to the following analysis procedures:

- Internal optical inspection
- SEM inspection of assembly features and passivation
- Wirepull test
- Passivation integrity test
- Delayer to metal and inspect
- Aluminum removal and inspect barrier
- Delayer to polycide/substrate and inspect
- Die material analysis
- Die sectioning (90° for SEM)*
- Measure horizontal dimensions
- Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package markings		G
Die placement	G	
Wirebond placement		G
Wire spacing		G
Wirebond quality		G
Die attach quality		N
Dicing quality		N
Die attach method		Silver-epoxy
Dicing method	Sawn (full depth)	
Wirebond method		Ultrasonic wedge bonds using 1.3 mil aluminum wire.
Die surface integrity:		
Toolmarks (absence)		G
Particles (absence)		G
Contamination (absence)		G
Process defects (absence)		G
General workmanship	G	
Passivation integrity		G
Metal definition		G
Metal integrity	G	
Metal registration		N
Contact coverage		N
Contact registration		N

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

MARKED ON CONTAINER

ATMEL AT27C010-45DC

BOTTOM OF PACKAGE

4B0688A-3-18706A
1 PHILIPPINES-F
4B9428

WIREBOND STRENGTH

Wire material:	1.3 mil diameter aluminum
Die pad material:	aluminum
# of wires pulled:	34
Bond lifts:	0
Force to break - high:	5.5g
- low:	4.0g
- avg.:	4.7g
- std. dev.:	0.5

DIE MATERIAL ANALYSIS

Overlay passivation:	Two layers of silicon-dioxide (possibly undoped glass).
Metallization:	Aluminum.
Barrier:	Titanium-nitride.
Intermediate glass:	CVD reflow glass over various densified oxides.
Polycide:	Titanium-silicide on polysilicon 2.
Diffusion silicide:	Titanium-silicide.

HORIZONTAL DIMENSIONS

Die size:	3.4 x 4.3 mm (133 x 170 mils)
Die area:	14.6 mm ² (22,610 mils ²)
Min pad size:	0.11 x 0.13 mm (4.5 x 5.0 mils)
Min pad window:	0.09 x 0.11 mm (3.7 x 4.3 mils)
Min pad space:	20 microns (0.8 mils)
Min metal width:*	1.2 micron
Min metal space:*	1.0 micron
Min metal pitch:	2.3 microns
Min contact:	0.9 micron
Min polycide width:	0.4 micron
Min polycide space:	0.9 micron
Min peripheral gate length**	
- (N-channel):	0.6 micron (array)
- (N-channel):	0.9 micron (typical minimum)
- (P-channel):	1.4 micron
Cell size:	4.4 microns ²
Cell pitch:	2.1 x 2.1 microns

**Minimum metal width was measured from the "body" of the line (aluminum). Minimum metal space was measured from the closest metal spacing (i.e., barrier-to-barrier).*

VERTICAL DIMENSIONS

Die thickness: 0.5 mm (20 mils)

Layers

Passivation 2:	1.0 micron
Passivation 1:	0.25 - 1.2 micron
Metal- aluminum:	0.8 micron
- barrier:	0.1 micron
Intermediate glass:	0.5 - 1.1 micron
Oxide on polycide:	0.1 micron
Polycide - silicide:	0.08 micron
- poly 2:	0.27 micron
Poly 1:	0.2 micron
Local oxide (under polycide):	0.7 micron
N+ S/D:	0.25 micron
P+ S/D:	0.3 micron
N- well:	6.5 microns
P-well:	Could not be delineated

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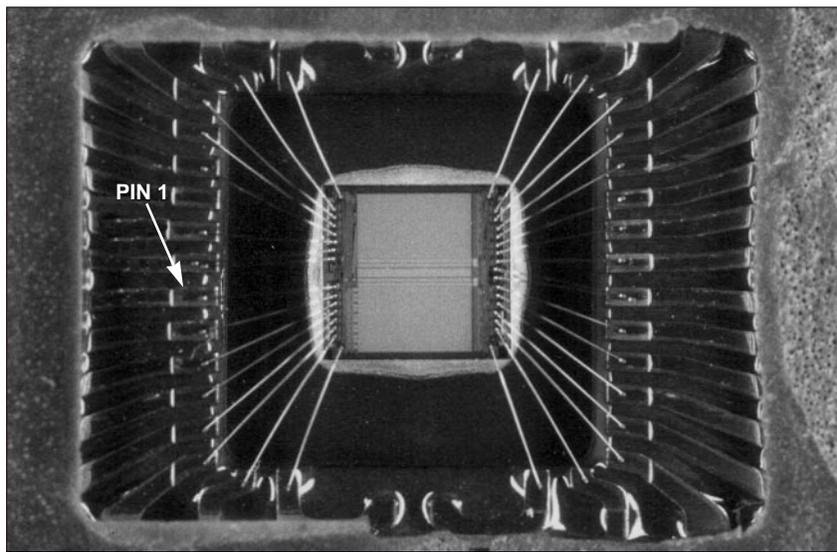


Figure 1. Cavity view of the SGS 27C1001. Mag. 6x.

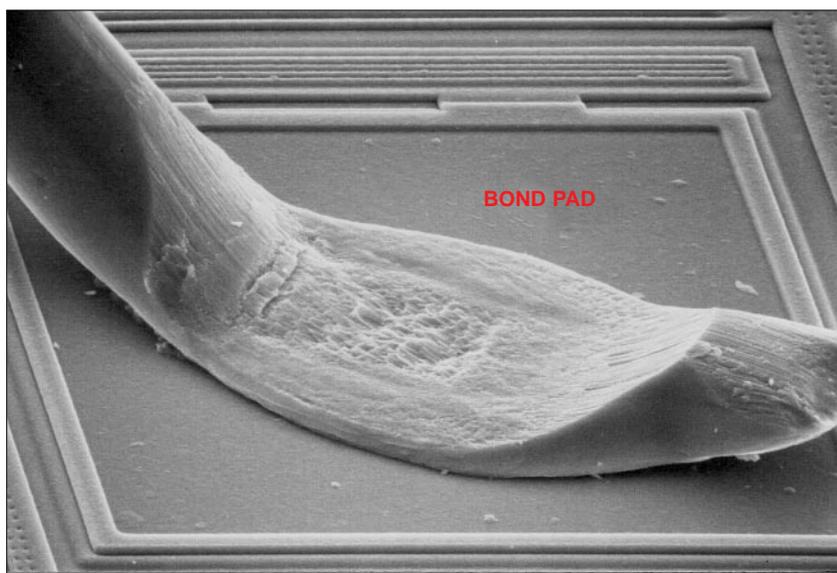
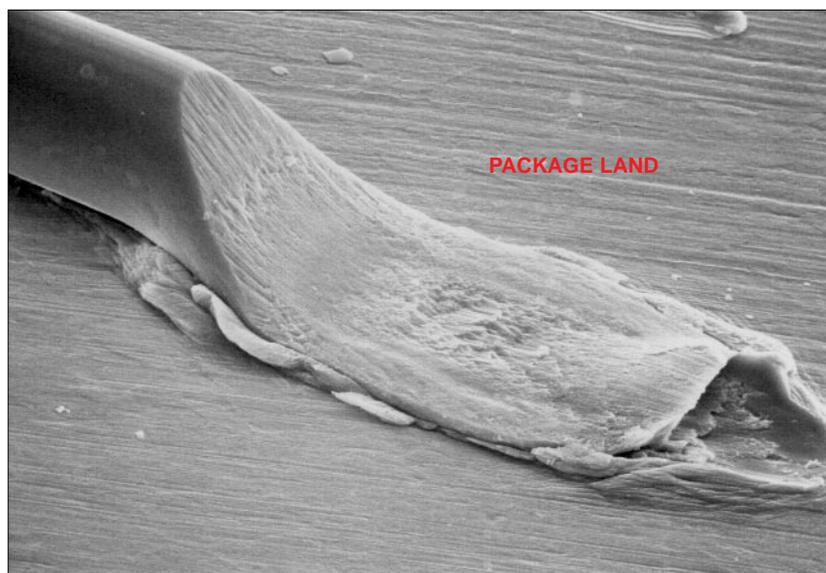
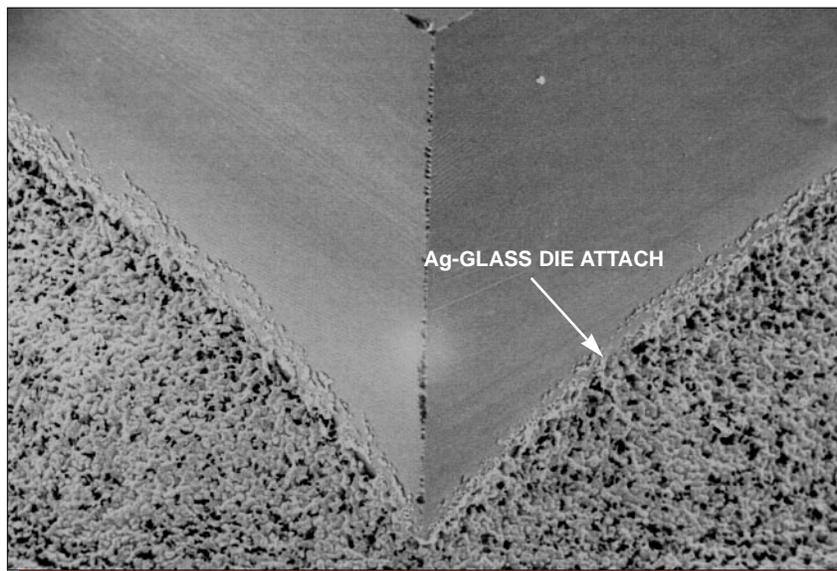
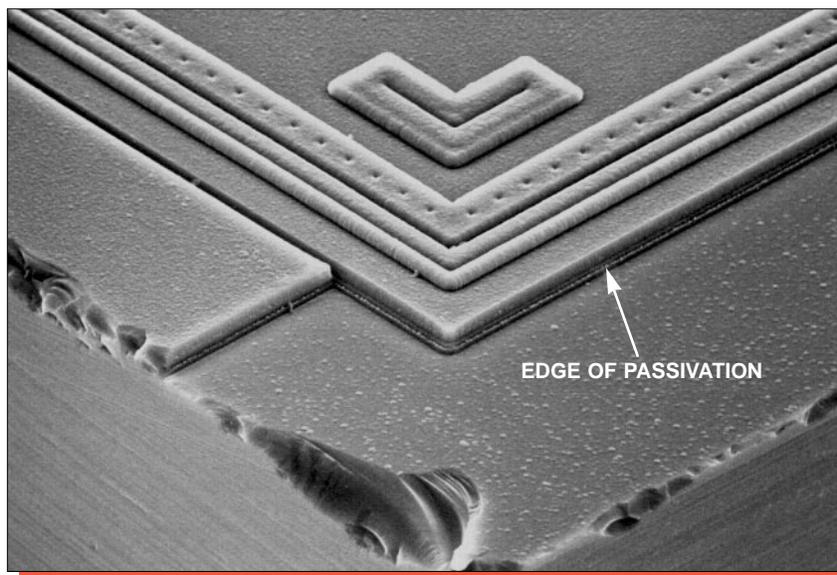


Figure 2. SEM views of typical wirebonds. Mag. 700x, 60°.



Mag. 130x



Mag. 1000x

Figure 3. SEM views of a die corner and edge seal. 60°.

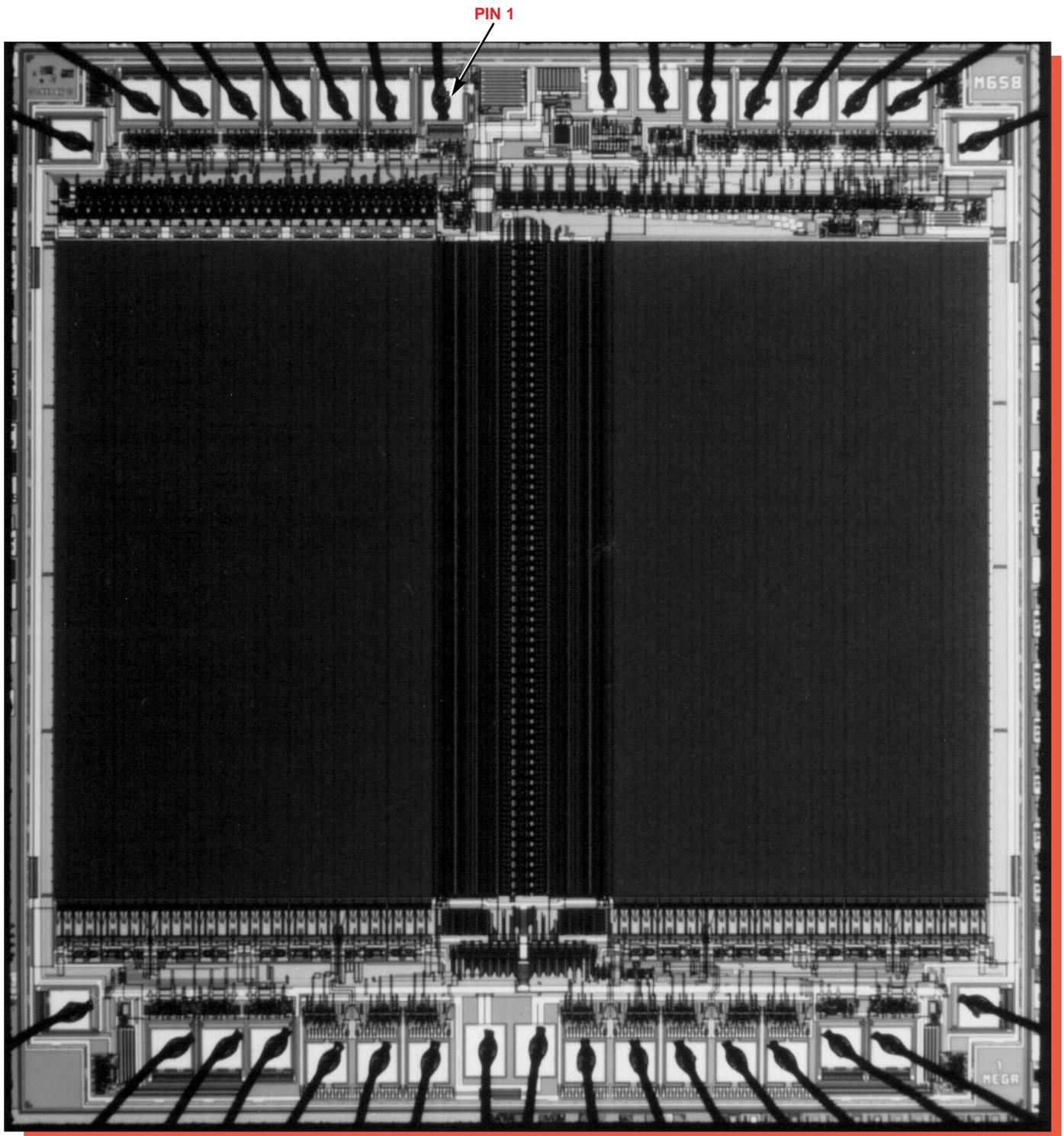


Figure 4. Whole die photograph of the SGS 27C1001. Mag. 47x.

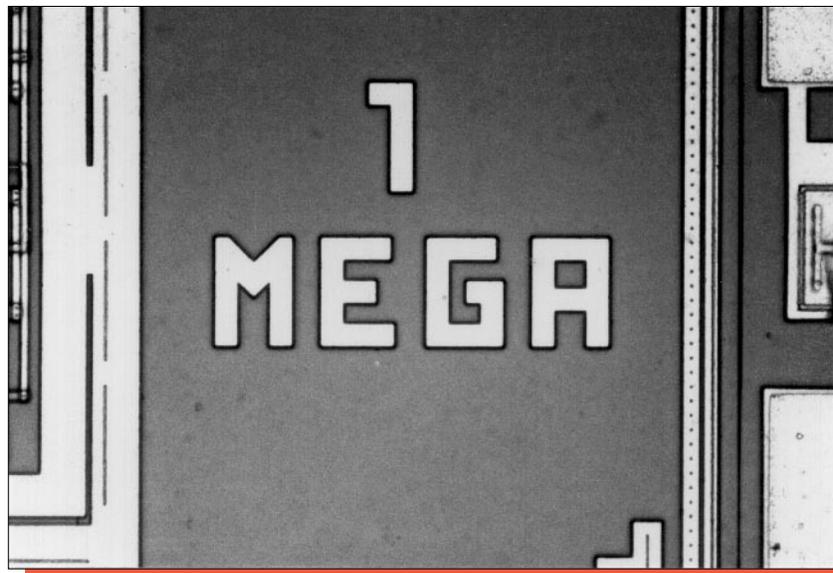


Figure 5. Identification markings from the die surface. Mag. 400x.

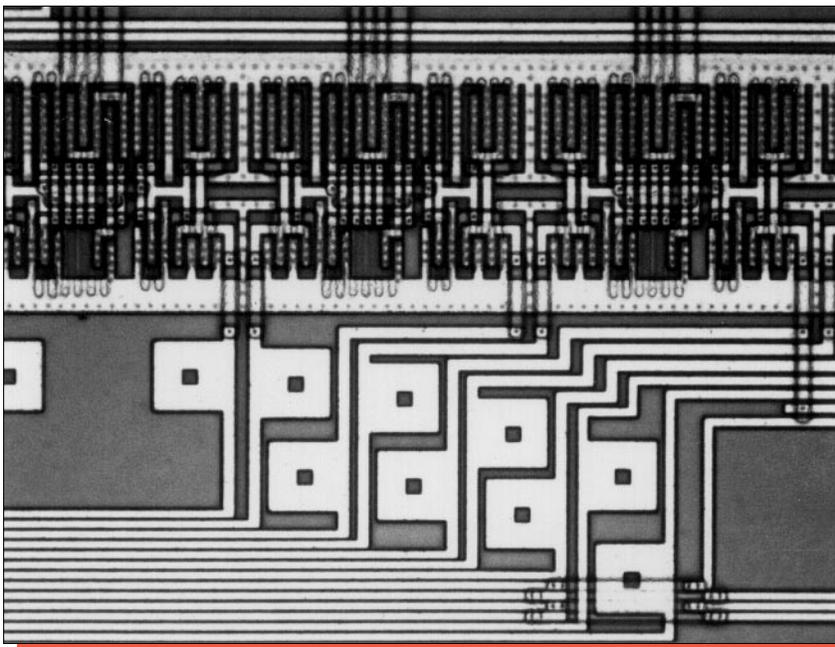
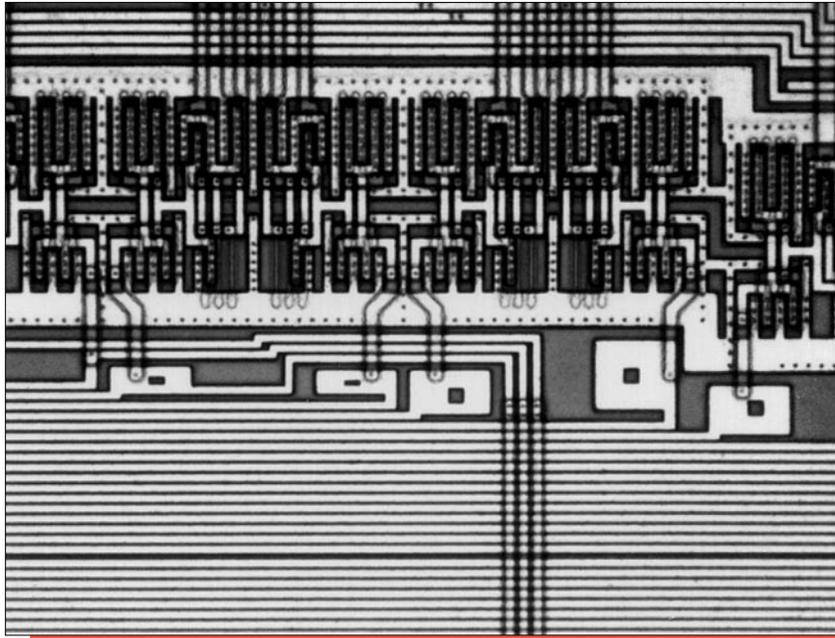
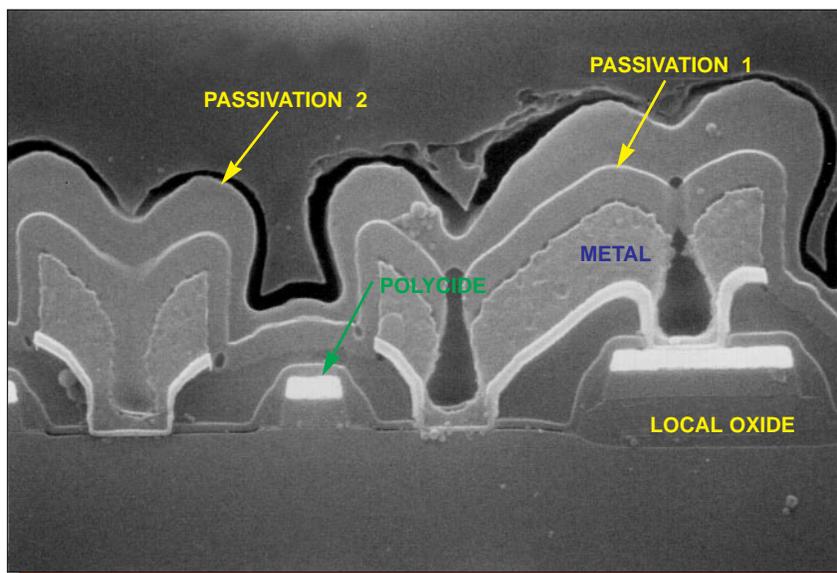
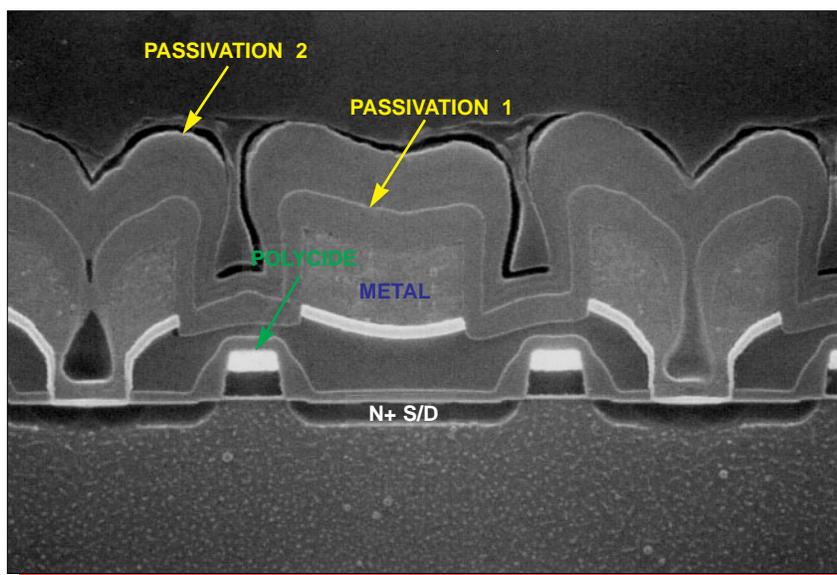


Figure 6. Optical views of metal design features. Mag. 500x.

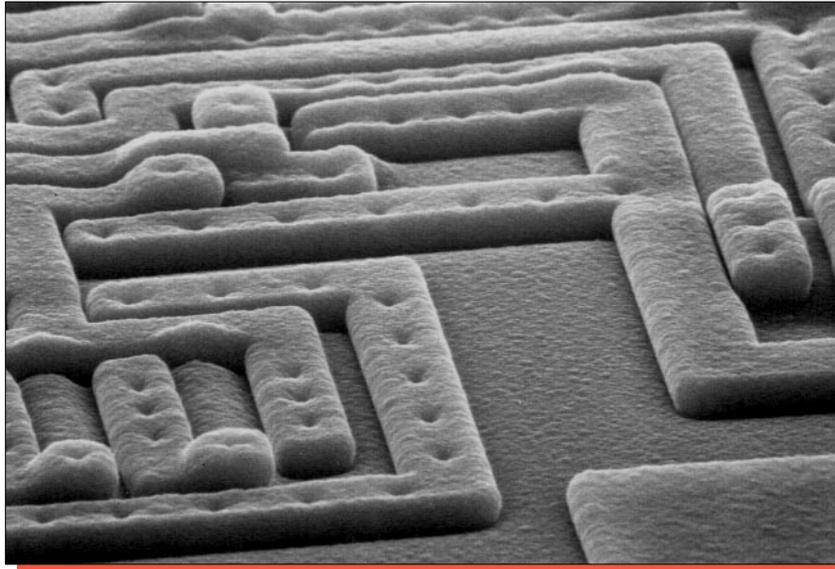


glass etch, Mag. 12,000x

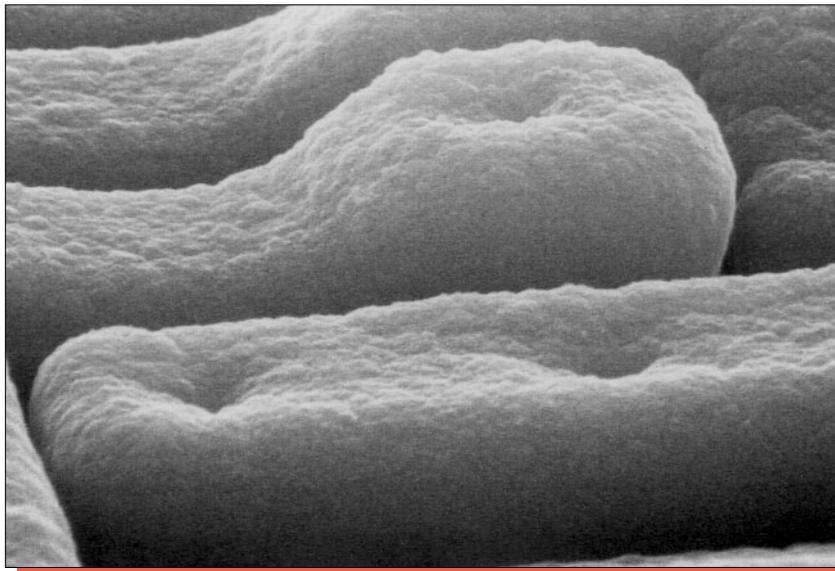


silicon etch, Mag. 13,500x

Figure 7. SEM section views illustrating general device structure.



Mag. 3000x



Mag. 13,000x

Figure 8. SEM views of general overlay passivation coverage. 60°.

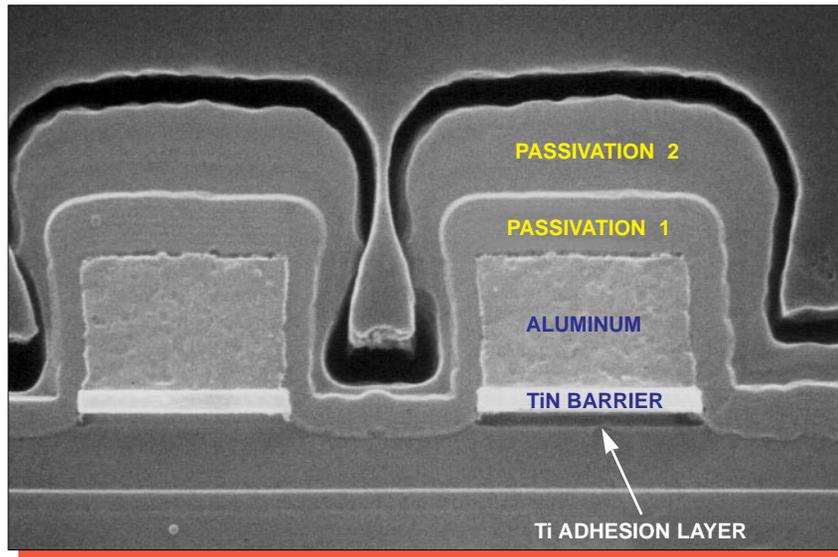
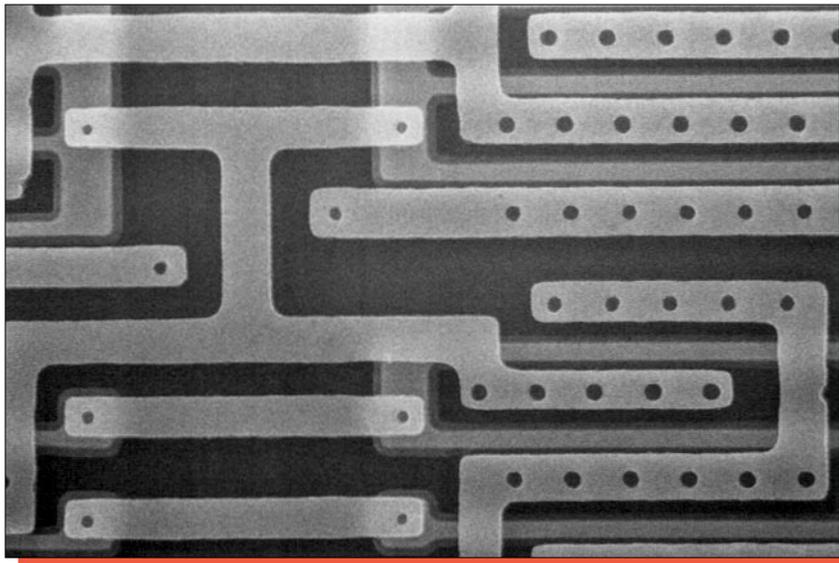
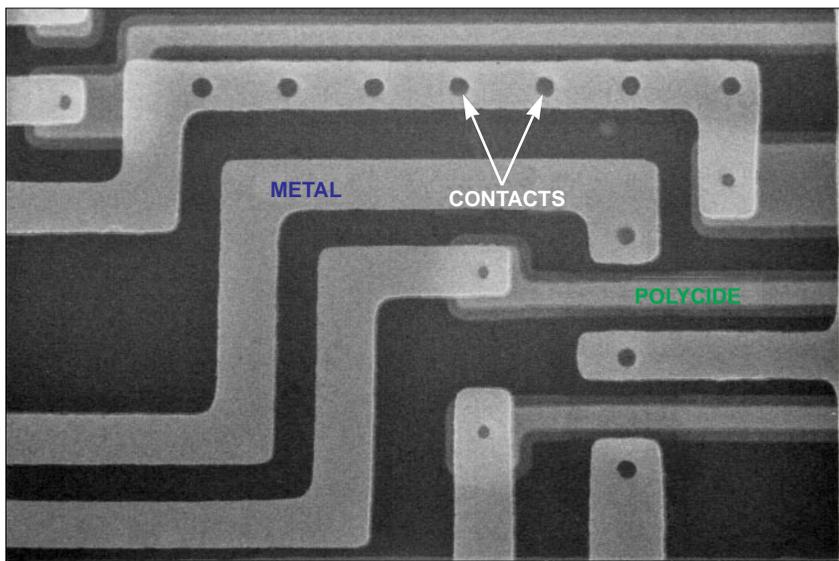


Figure 9. SEM section view of metal line profiles. Mag. 20,000x

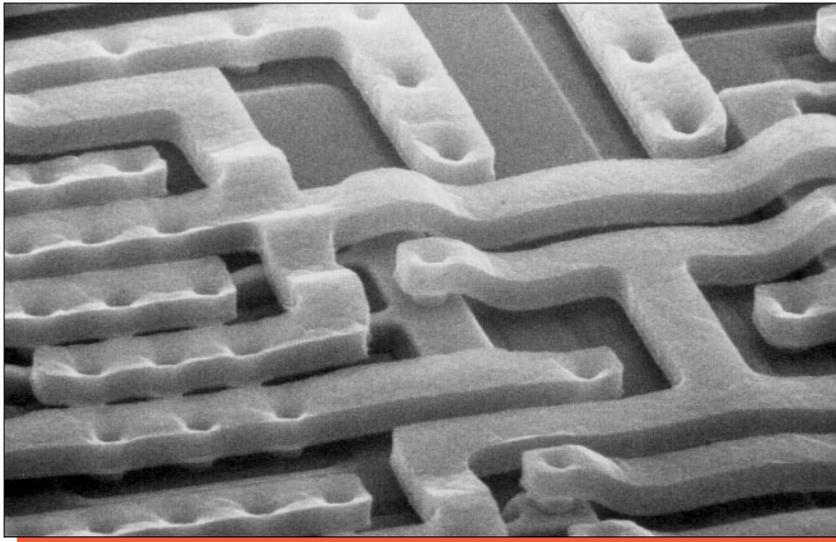


Mag. 3500x

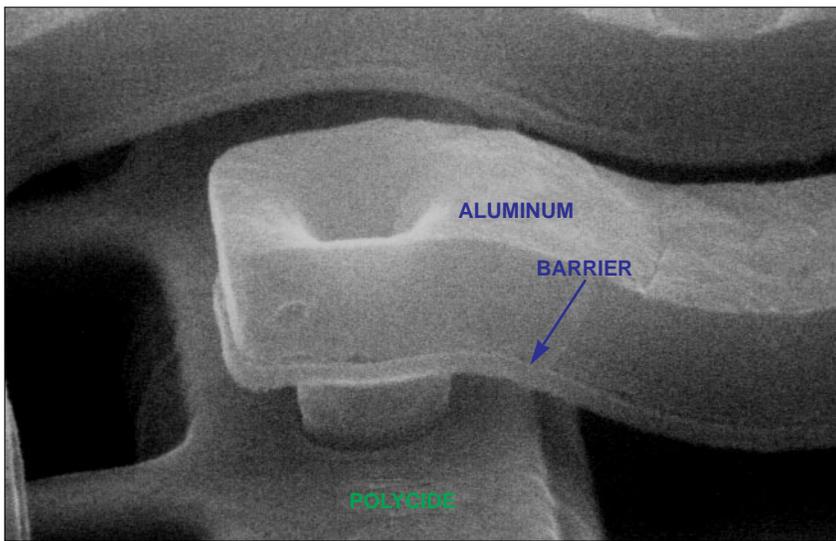


Mag. 4600x

Figure 10. Topological SEM views of metal patterning. 0°.



Mag. 4600x



Mag. 20,000x

Figure 11. SEM views illustrating general metal integrity. 60°.

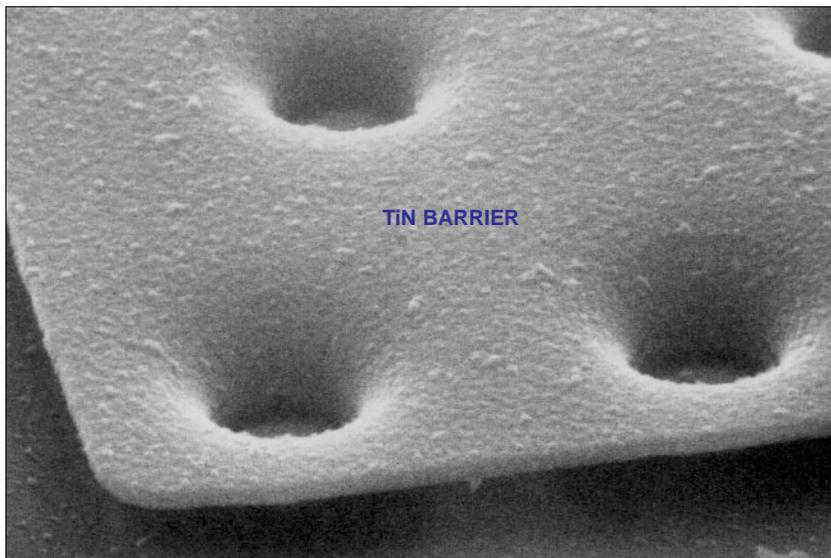
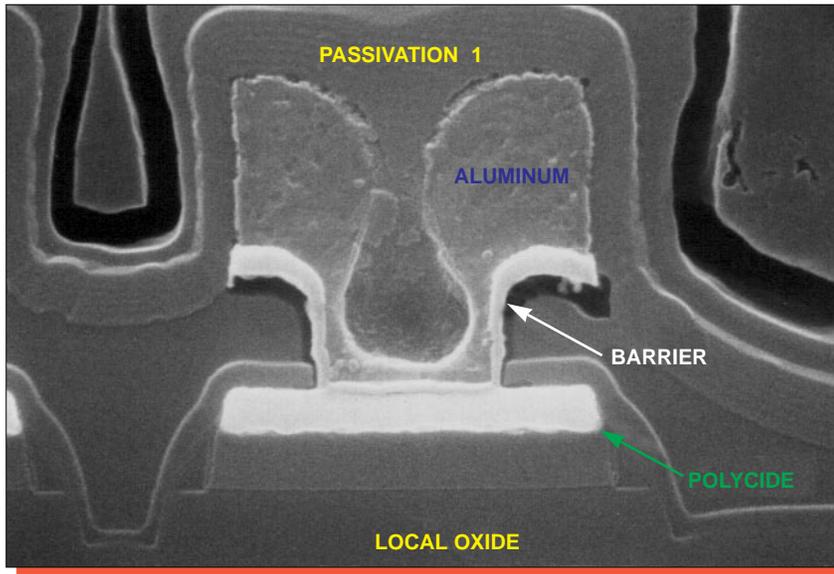
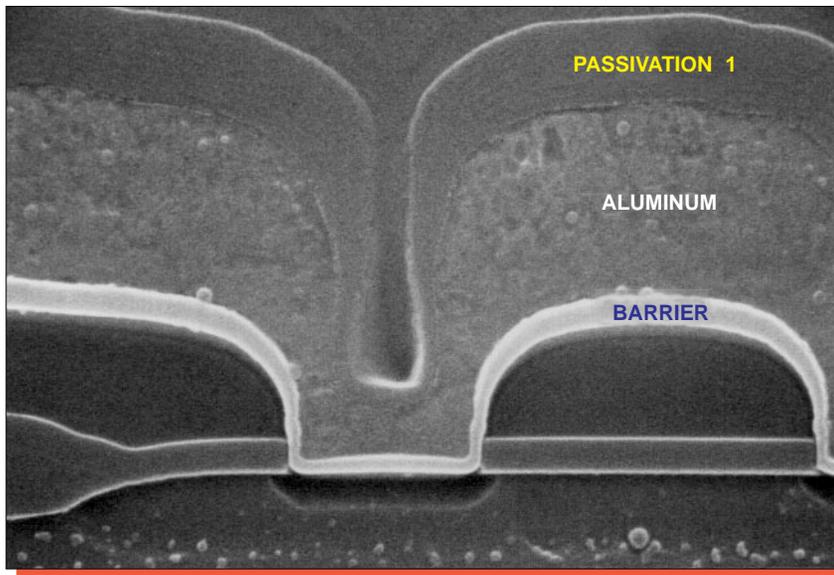


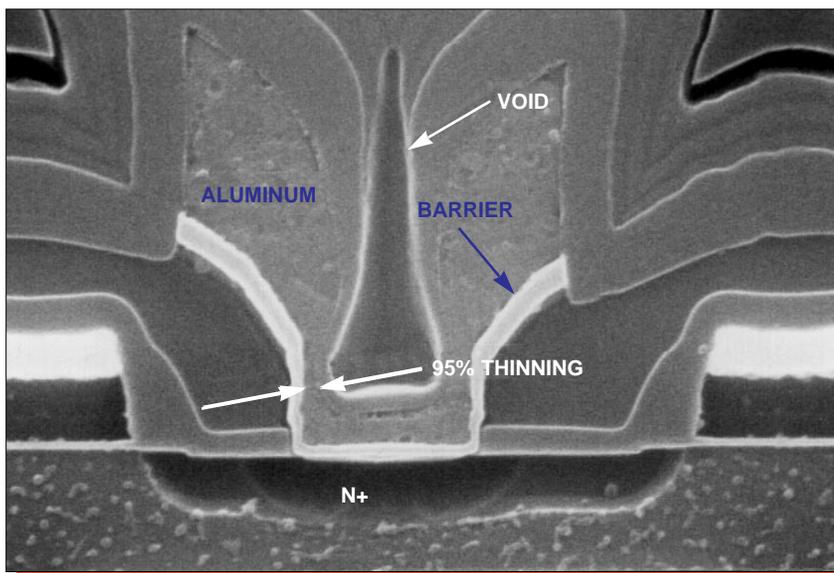
Figure 12. SEM view illustrating barrier coverage. Mag. 23,000x, 55°.



metal-to-polycide,
Mag. 26,000x,
(glass etch)

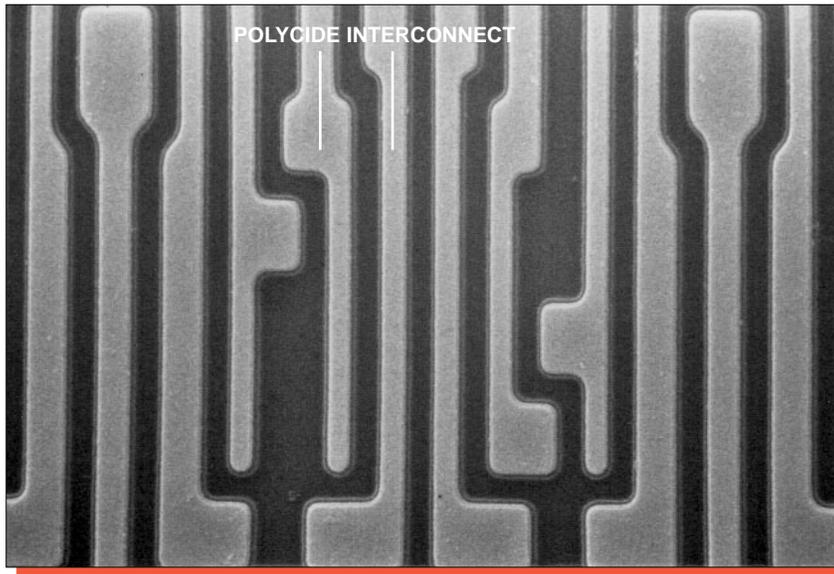


metal-to-P+,
Mag. 30,000x

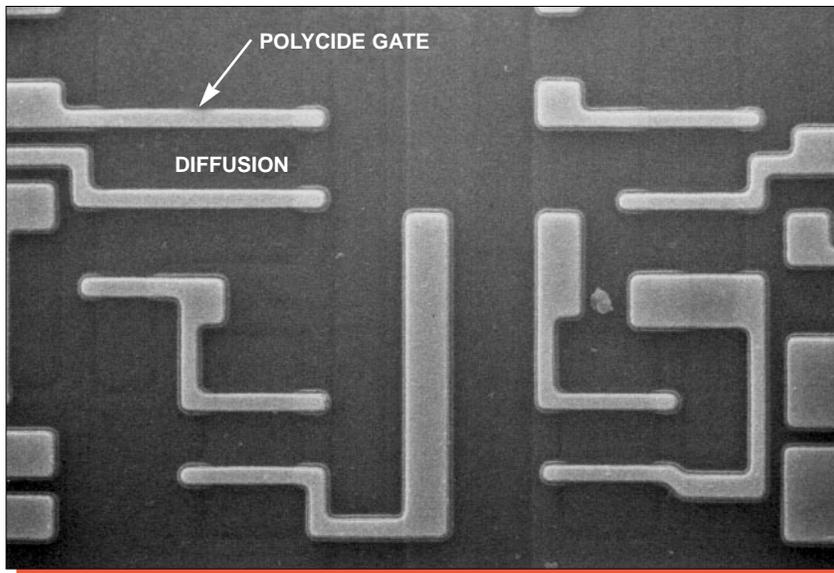


metal-to-N+,
Mag. 30,000x

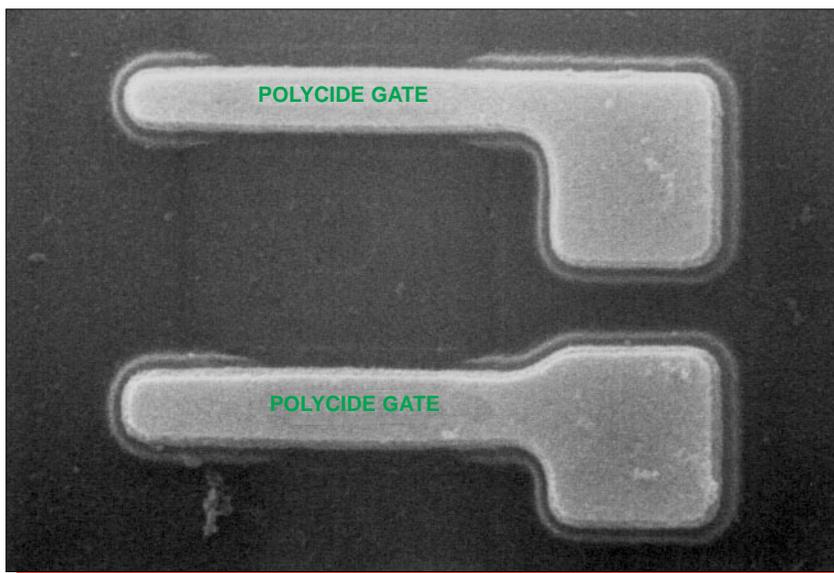
Figure 13. SEM section views of various metal contacts.



Mag. 4400x

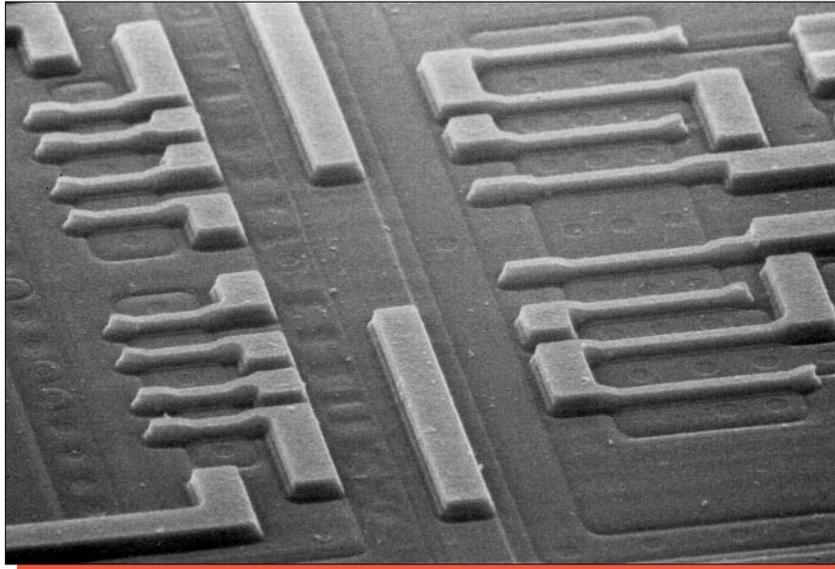


Mag. 3000x

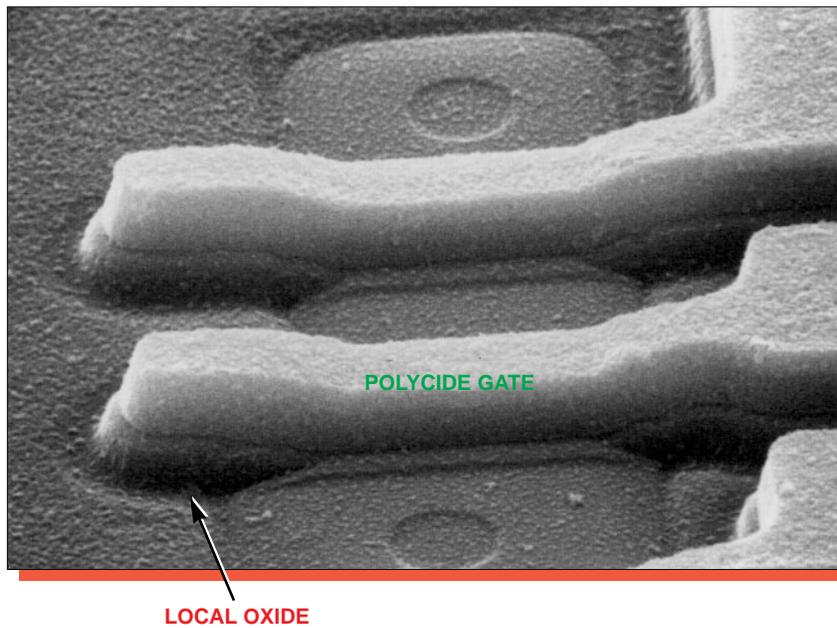


Mag. 11,000x

Figure 14. Topological SEM views of polycide patterning. 0°.

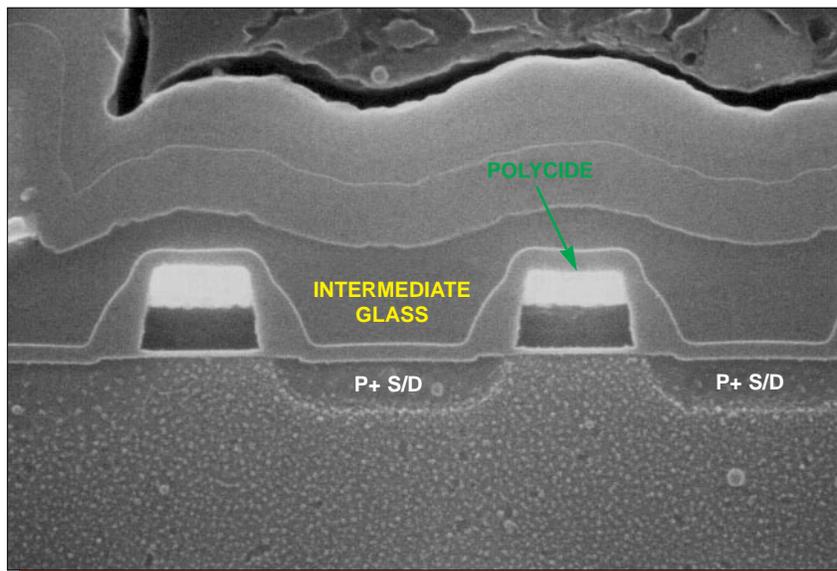


Mag. 3000x

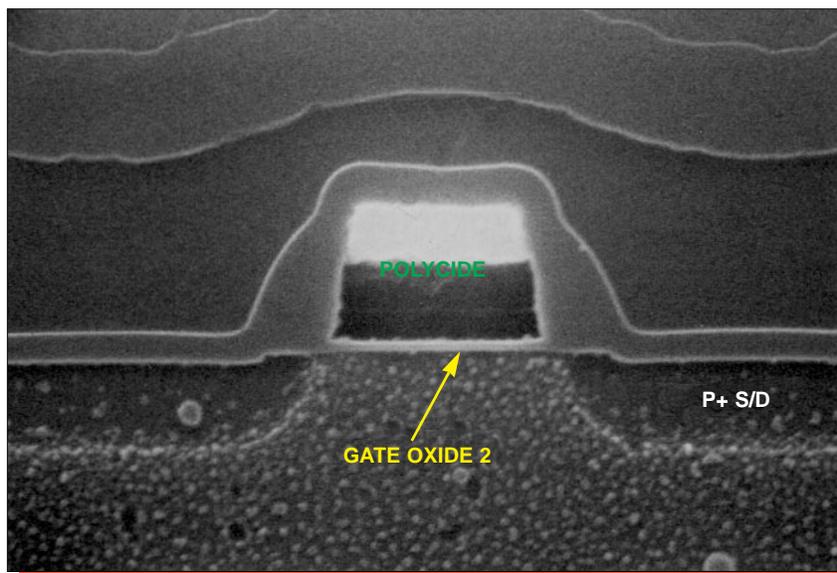


Mag. 15,000x

Figure 15. Perspective SEM views of polycide coverage. 60°.

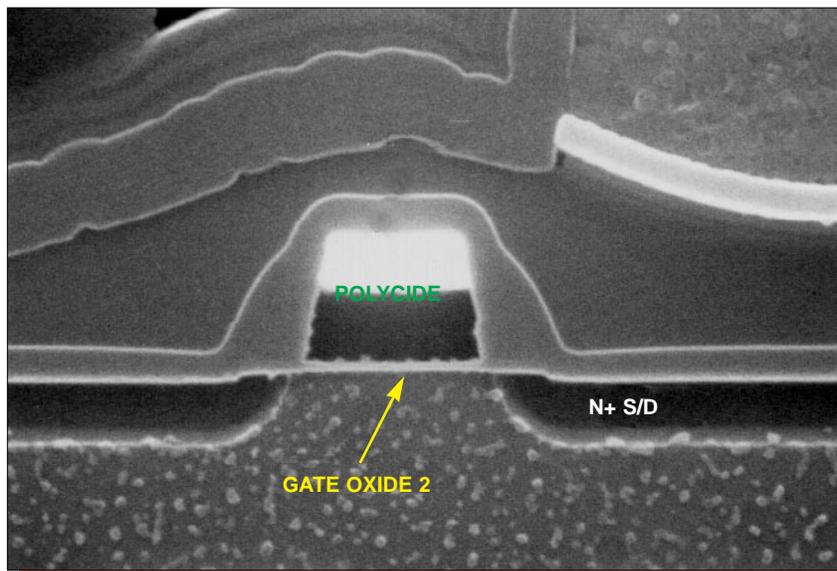


Mag. 20,000x

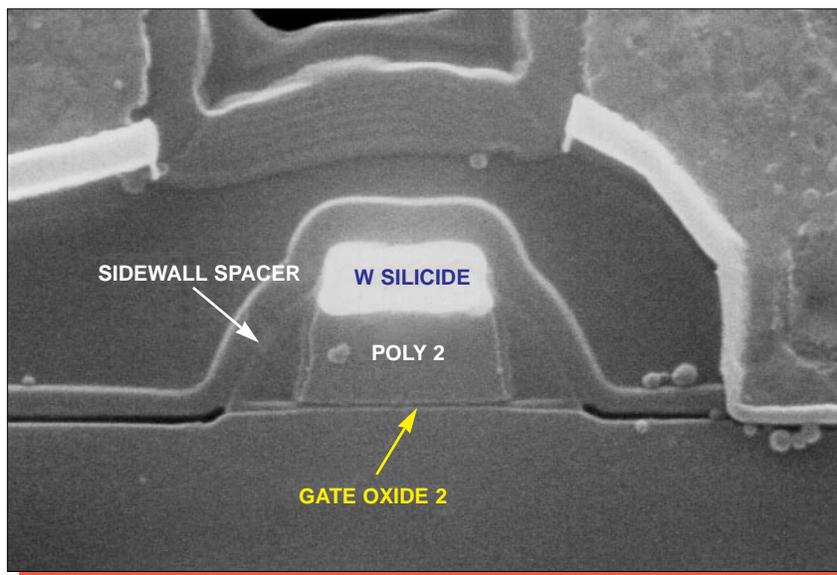


Mag. 35,000x

Figure 16. SEM section views of P-channel transistors.



Mag. 35,000x



glass etch, Mag. 40,000x

Figure 17. SEM section views of N-channel transistors.

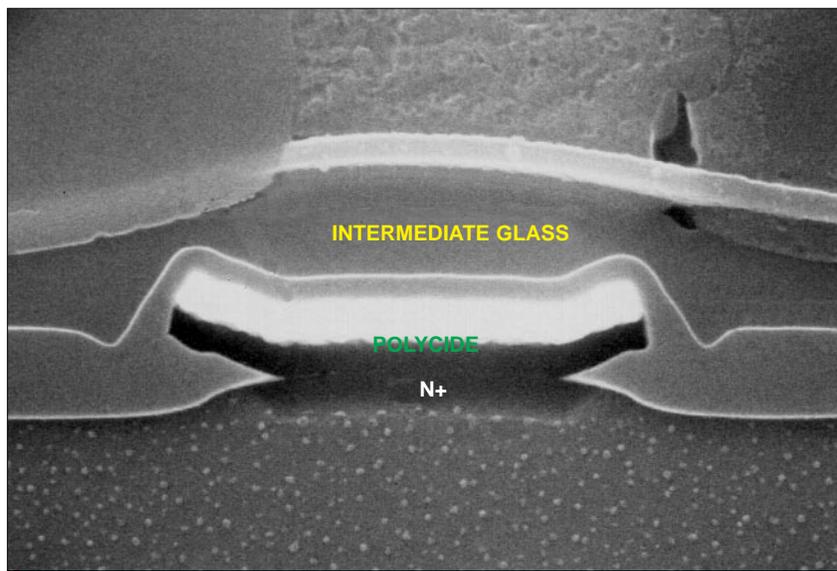


Figure 18. SEM section view of a buried contact. Mag. 26,000x.

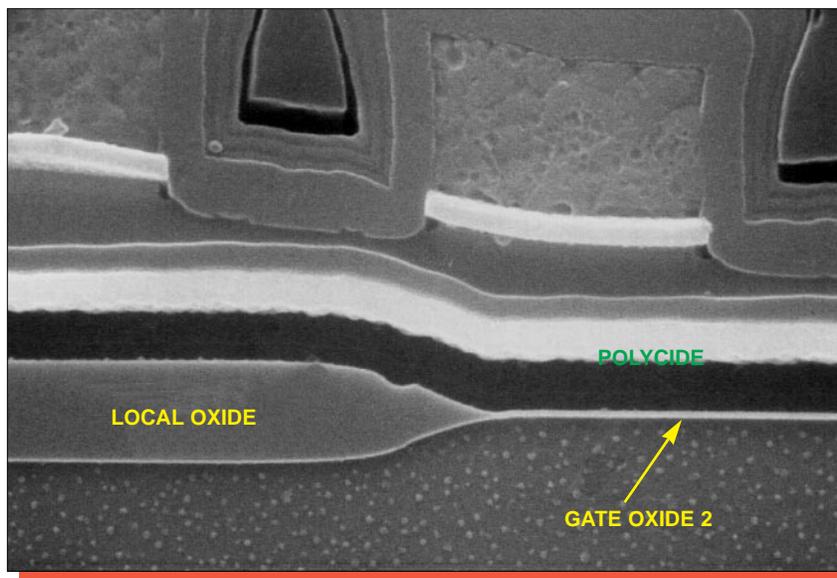
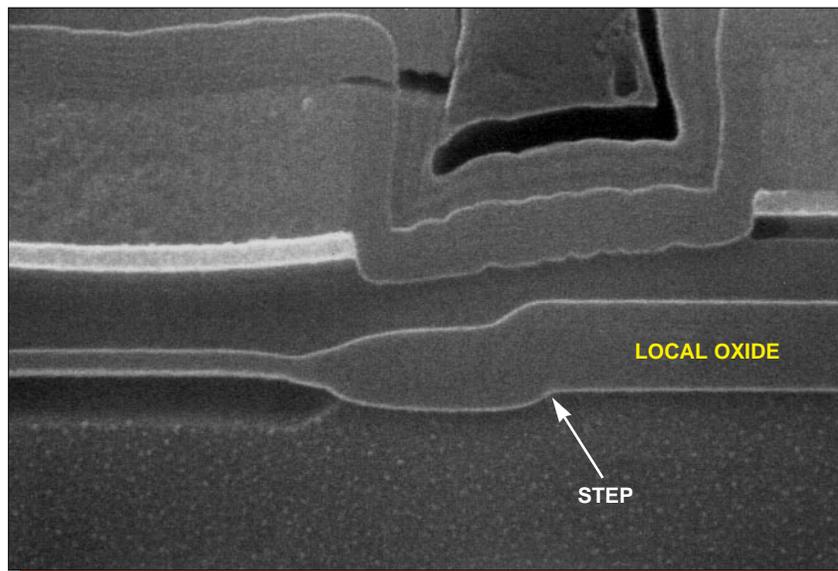
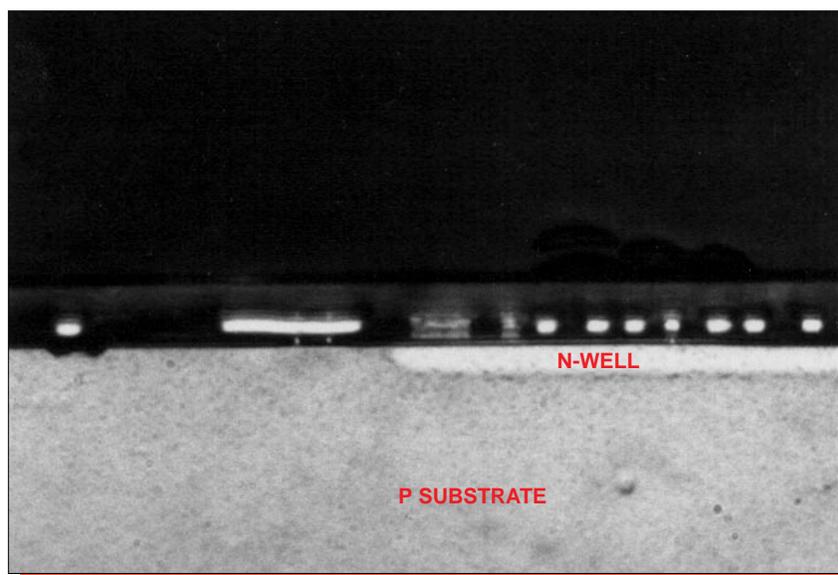


Figure 19. SEM section view of a local oxide birdsbeak. Mag. 25,000x.

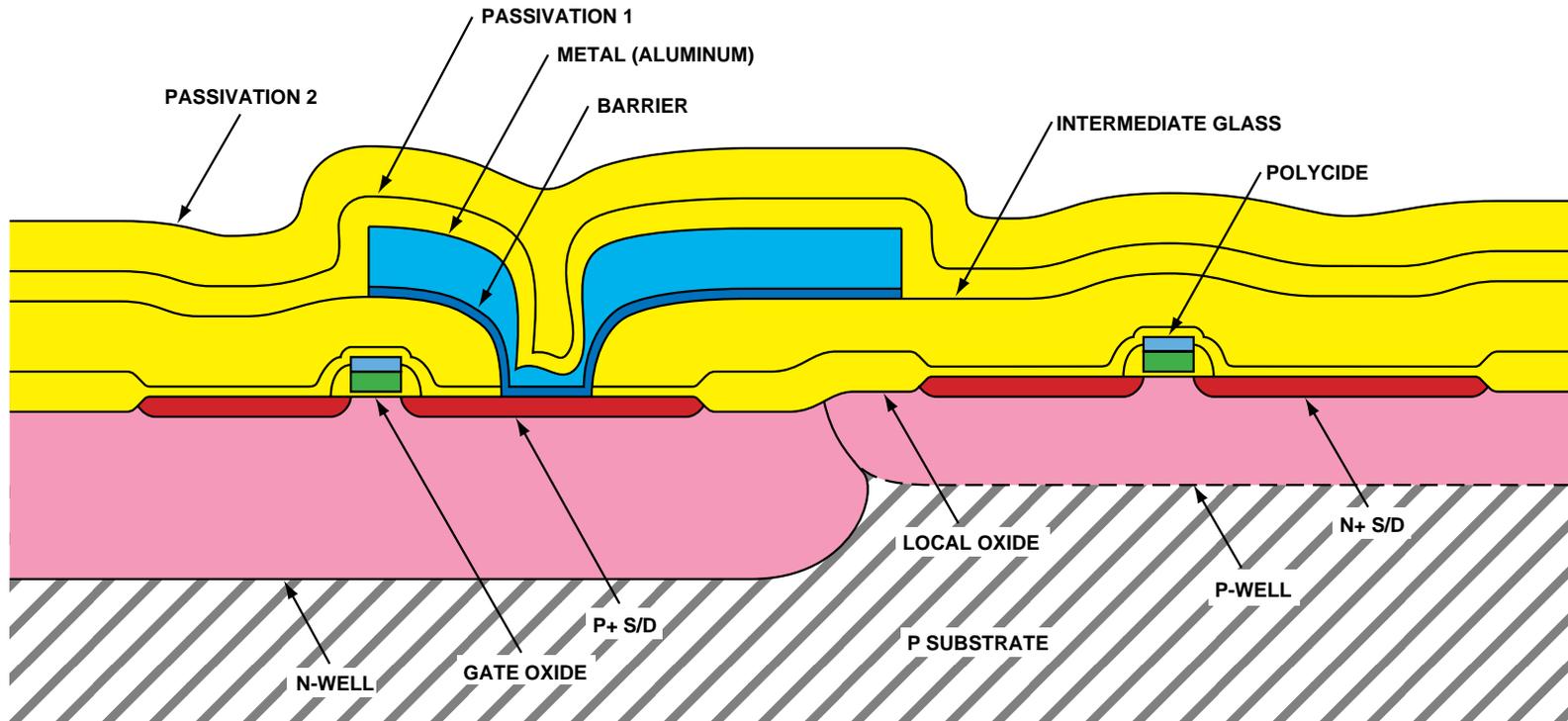


Mag. 25,000x



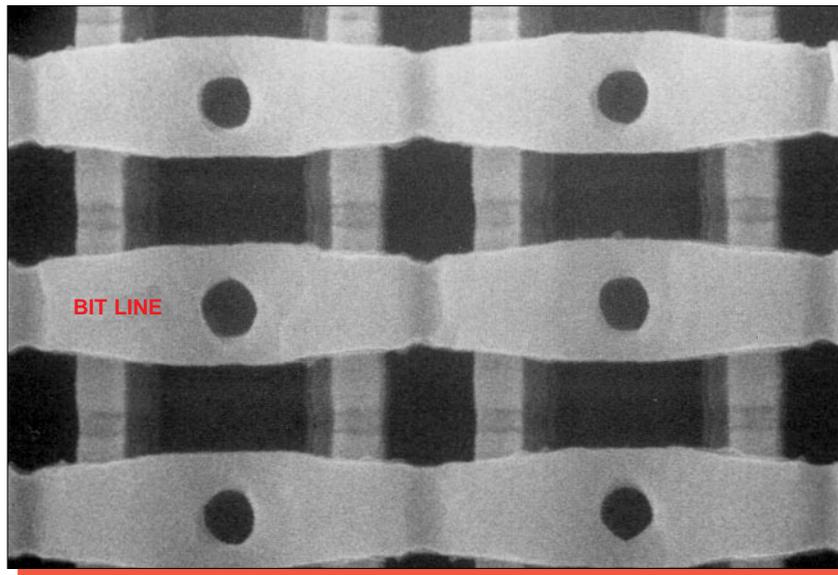
Mag. 1600x

Figure 20. Section views illustrating well structure.

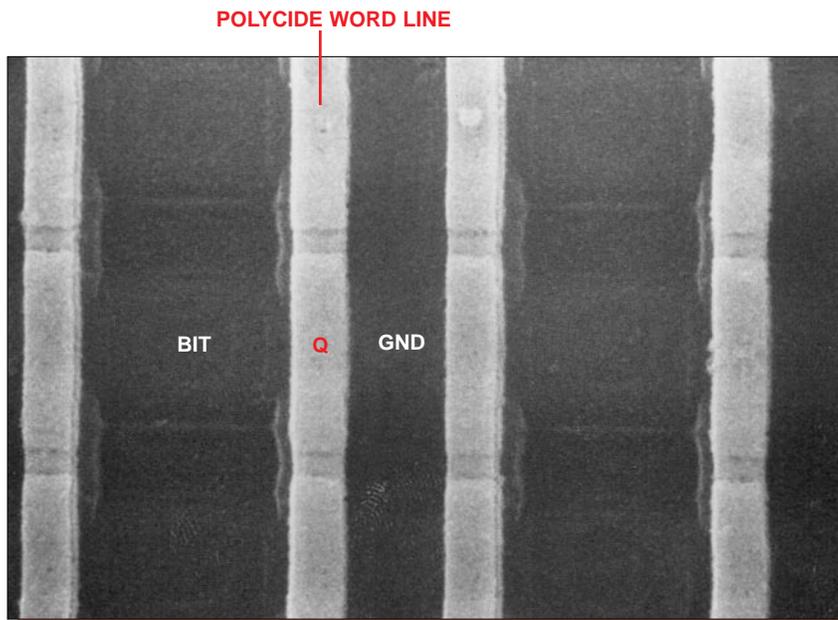


Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 21. Color cross section drawing illustrating device structure.



metal



unlayered

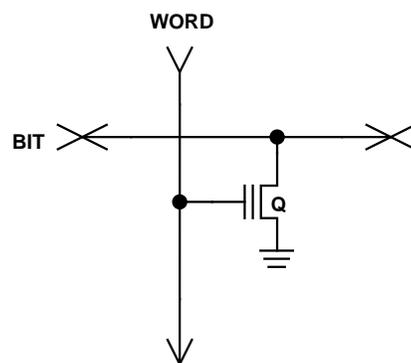
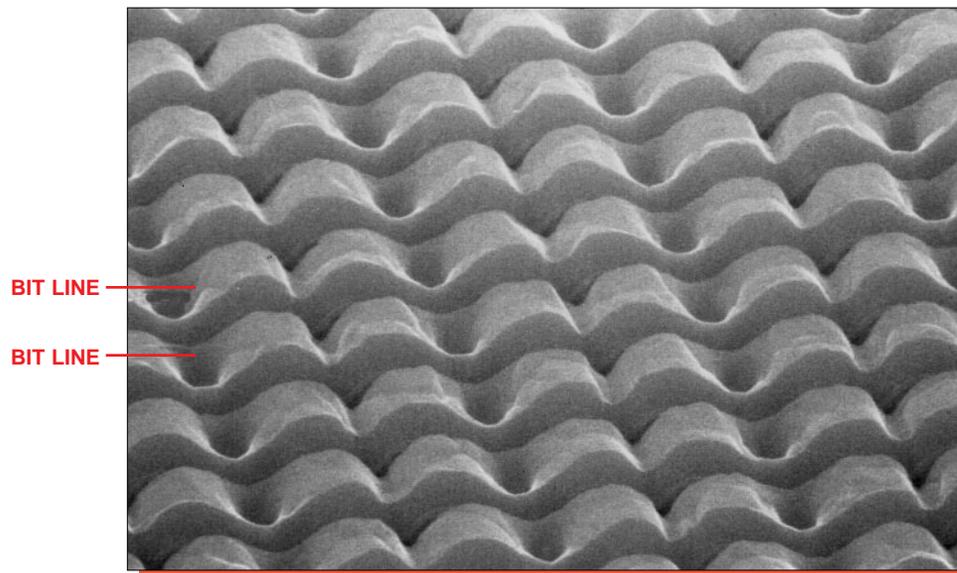
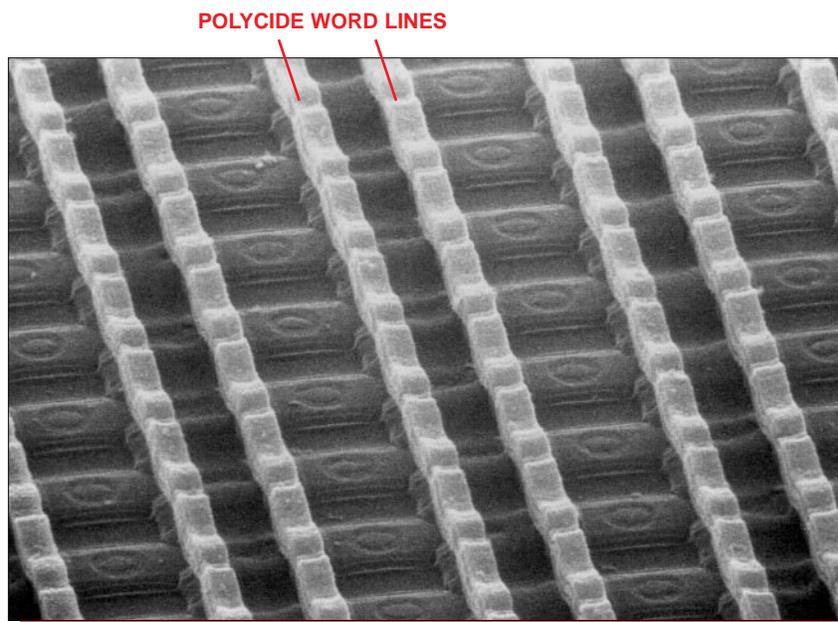


Figure 22. Topological SEM views of EPROM cells along with the cell schematic.
Mag. 13,000x, 0°.

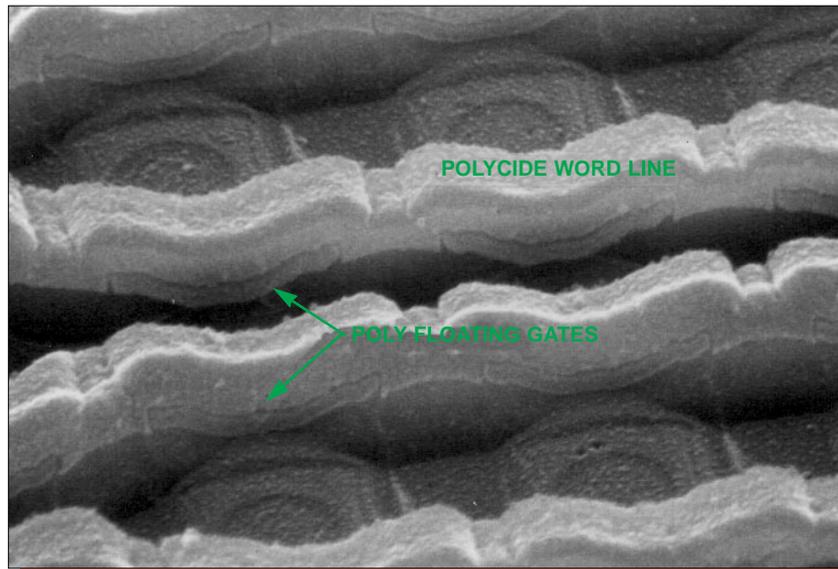


metal

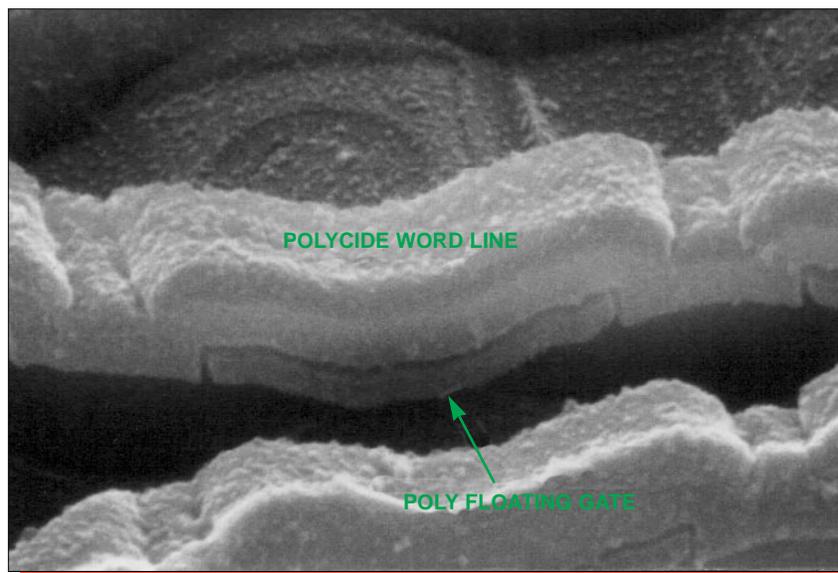


unlayered

Figure 23. Perspective SEM views of the cell array. Mag. 7000x, 60°.

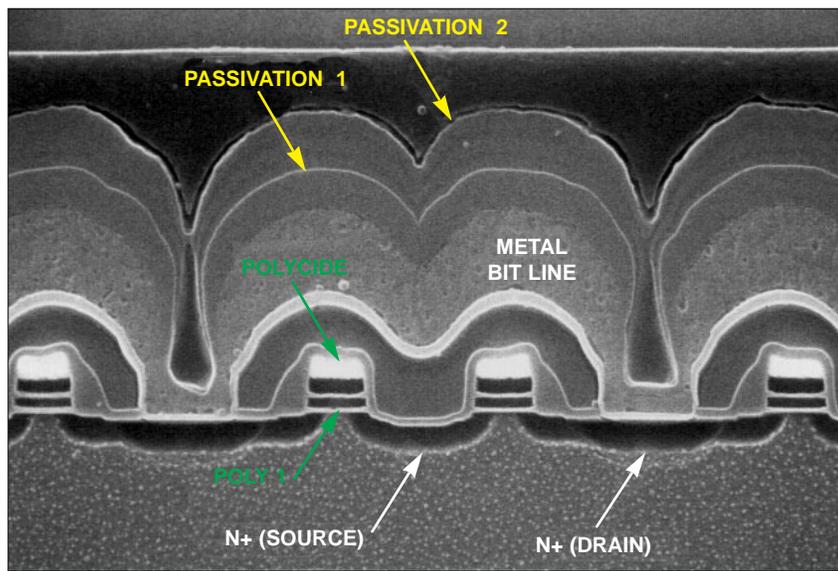


Mag. 20,000x

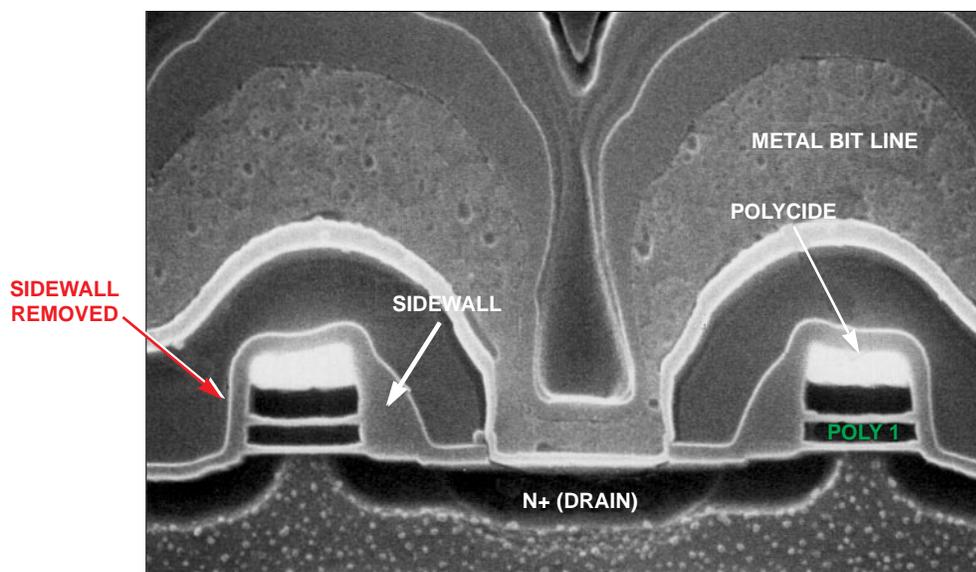


Mag. 36,600x

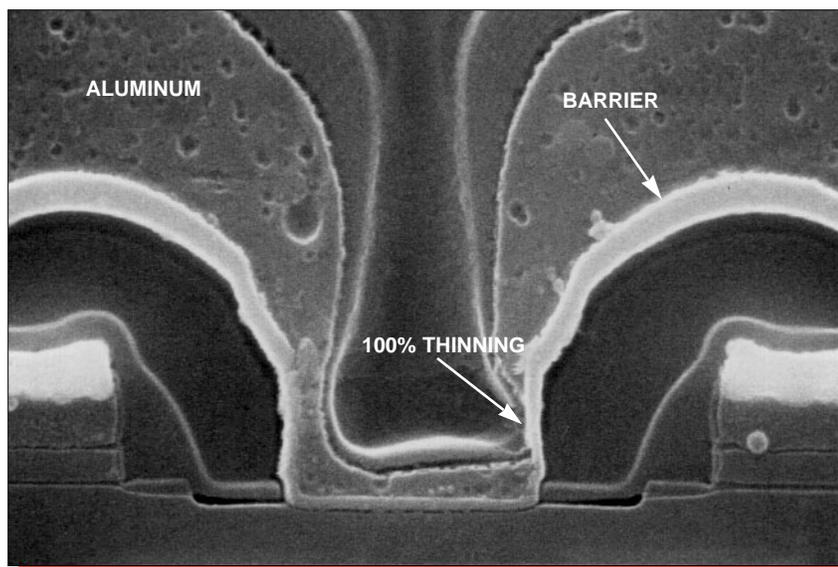
Figure 24. Detail SEM views of the cell array. 60°.



Mag. 13,000x

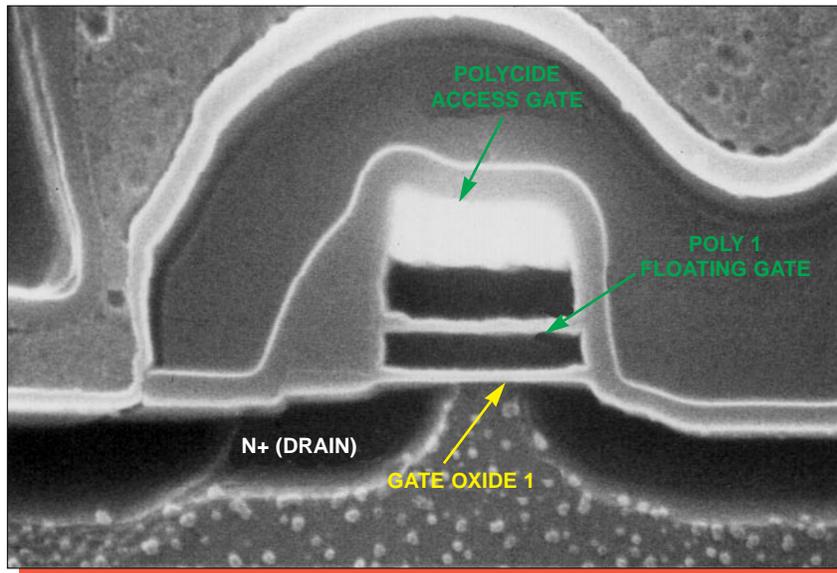


Mag. 25,000x

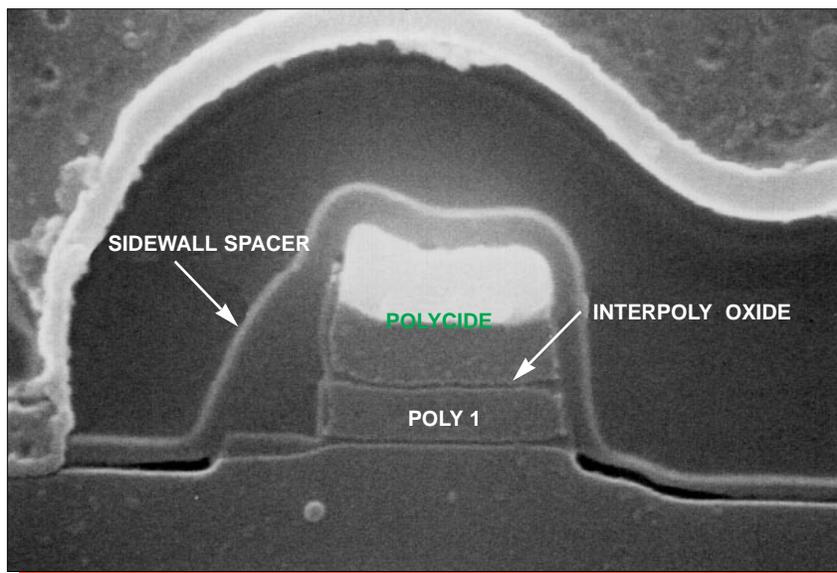


glass etch,
Mag. 32,000x

Figure 25. SEM section views of EPROM cells (X-direction).

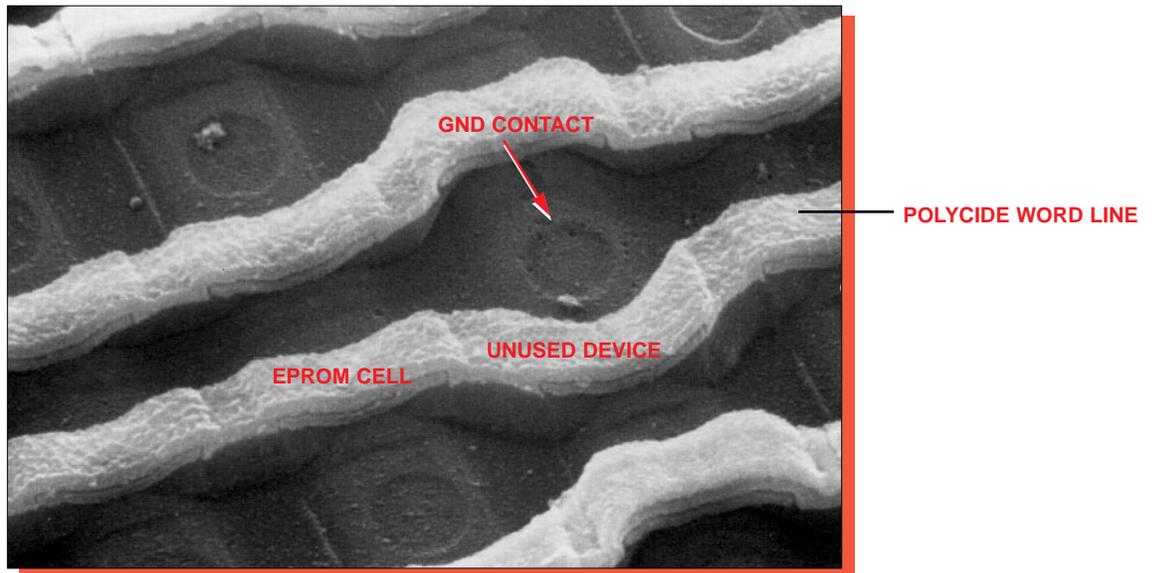


Mag. 45,000x

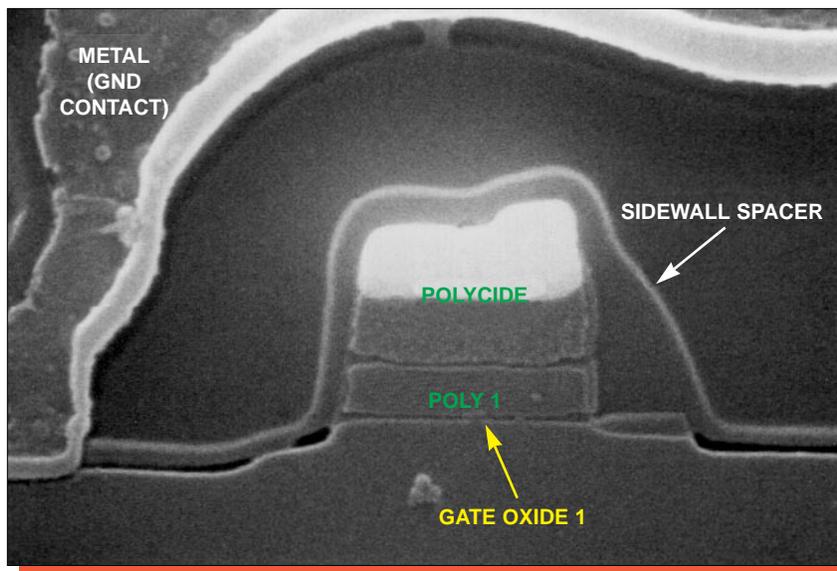


glass etch, Mag. 50,000x

Figure 26. SEM section details of EPROM cells (Y-direction).

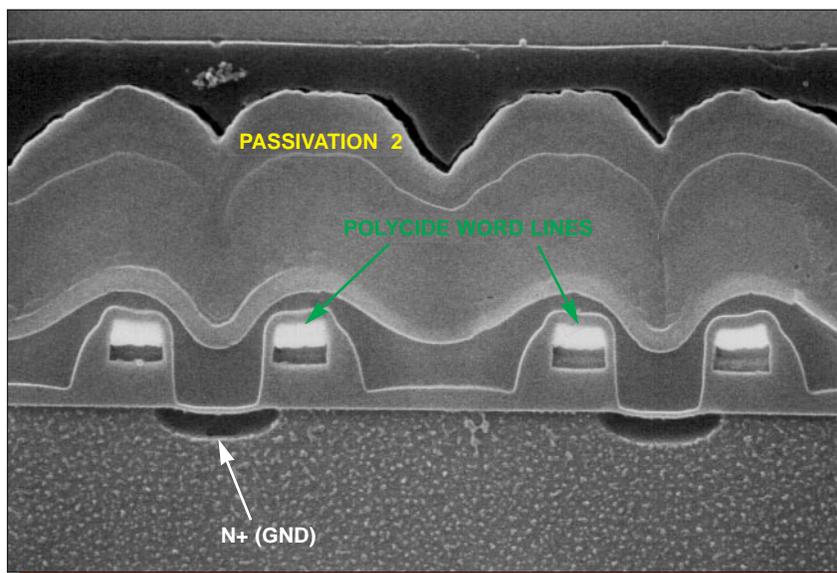


Mag. 15,000x, 45°

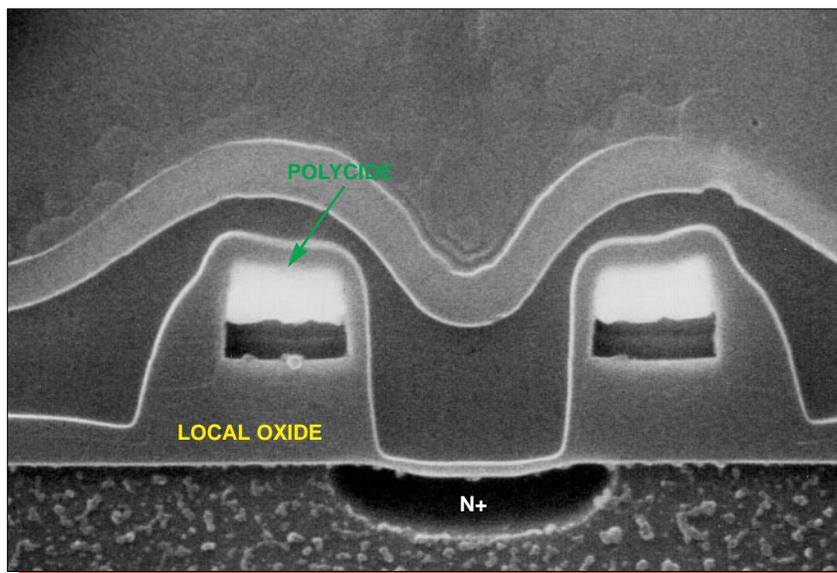


glass etch, Mag. 50,000x

Figure 26a. Topological and section views of unused floating gate device.

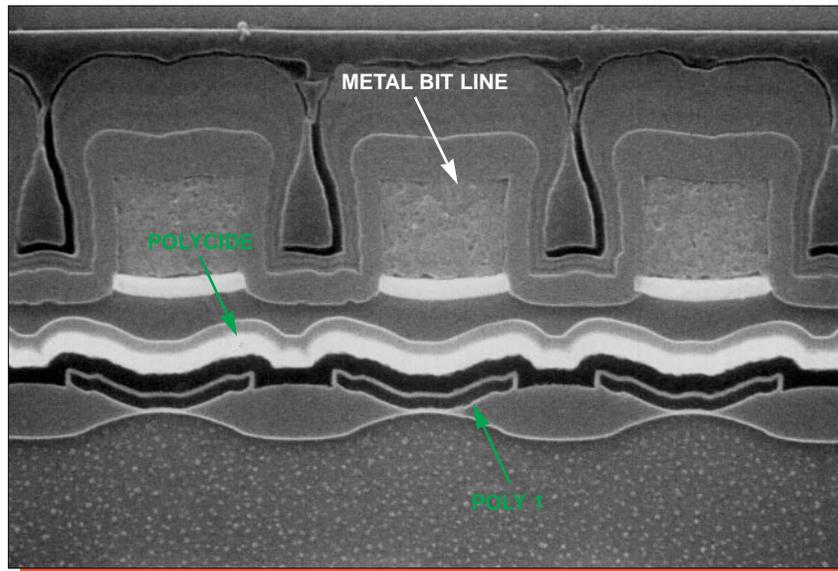


Mag. 13,000x

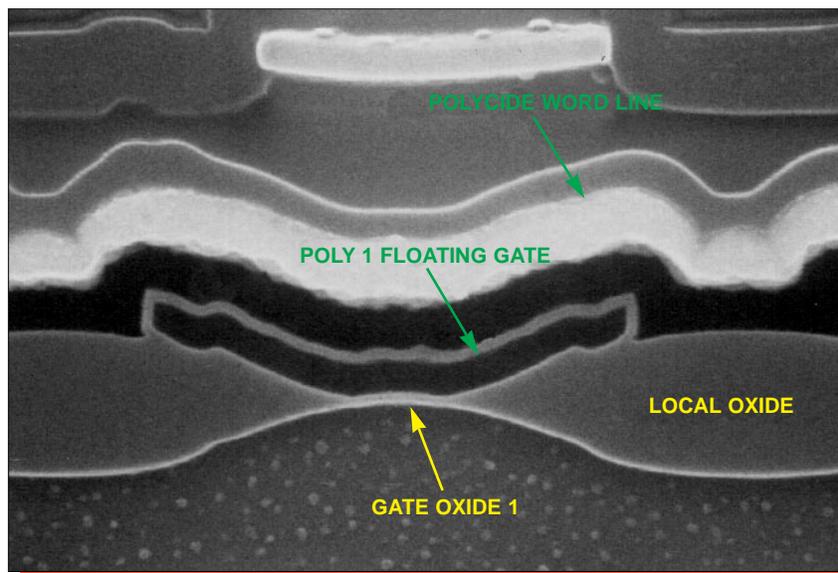


Mag. 30,000x

Figure 27. SEM section views of the cell array (X-direction).

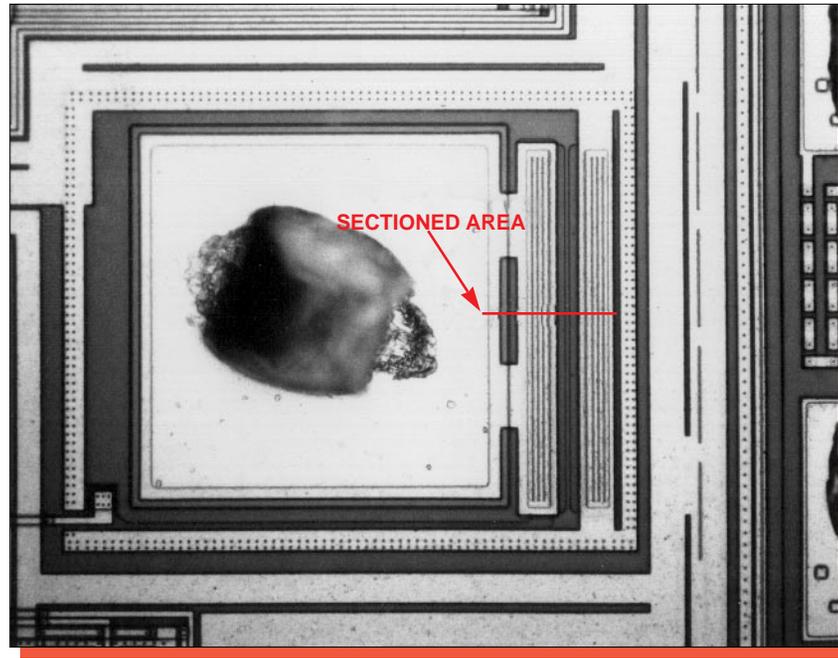


Mag. 15,000x

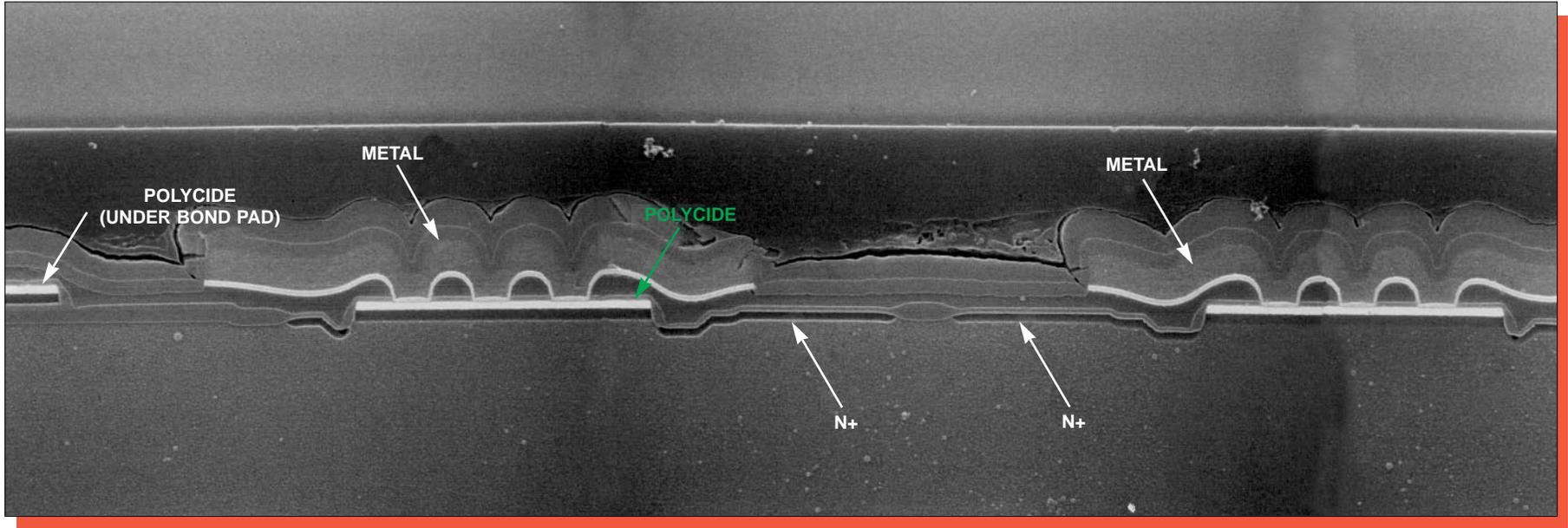


Mag. 40,000x

Figure 28. SEM section views of the cell array (Y-direction).



Mag. 400x



Mag. 6000x

Figure 29. Optical and section views of typical input protection.