

Construction Analysis

ISSI IS27HC010 1Mbit UVEPROM

Report Number: SCA 9504-407



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**COMPETITIVE ANALYSIS
OF THE
INTEGRATED SILICON SOLUTIONS INC. IS27HC010
1 MEG EPROM
DATE CODE 9335**

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INTRODUCTION

This report describes a construction analysis of the ISSI IS27HC010, 1 Mbit EPROM. Three devices were supplied. Two were packaged in 32 pin PLCC's date coded 9335, and one in a CERDIP package that had been delidded. During the analysis it was discovered that although die markings were the same, the die in the CERDIP was manufactured by a more modern process. All work was thus done on that die and on only the photos of die markings included are of the old die.

MAJOR FINDINGS

Questionable Items:¹ None.

Special Features:

- Recent process change using tungsten plugs at contacts.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

TECHNOLOGY DESCRIPTION

Die Process

- Fabrication process: Selective oxidation CMOS process with N- wells in a P substrate.
- Final passivation: Two thick layers of silicon-dioxide (probably undoped).
- Metallization: A single level of metal defined by a dry-etch technique. Metal consisted of aluminum with a titanium-nitride barrier on a titanium adhesion layer. Tungsten plugs were used at metal contacts.
- Intermediate glass: A single layer of CVD reflow glass over various grown/densified oxides. The CVD glass was reflowed prior to contact cuts.
- Polysilicon: Two layers of polysilicon were employed. Polycide (poly 2 and tungsten silicide) was used to form word lines in the cell array and all standard gates on the die. Poly 1 was used to form the floating gates in the array. The interpoly dielectric consisted of oxide-nitride-oxide (ONO).
- Diffusions: Standard N+ and P+ diffusions formed the sources/drains of peripheral transistors. Deep N+ diffusions were noted at contacts; however, this may be a staining artifact. Oxide sidewall spacers were used in the periphery to provide the LDD spacing. Spacers were left in place. Deep S/D implants in the memory array were done before sidewall formation.
- No buried contacts were employed.
- Wells: N-wells in a P substrate. No epi was used.
- Memory cells: The memory cells consisted of a standard "stacked dual gate" EPROM design. Polycide formed the word lines, poly 1 formed the floating gates and metal formed the bit lines. As mentioned, the interpoly dielectric was an oxide-nitride-oxide sandwich (ONO).

TECHNOLOGY DESCRIPTION (continued)

- Special design items: Some metal lines (bus lines and minimum feature lines) had beveled corners to reduce stress. No slots (also to reduce stress) were noted in any of the bus lines. All contacts were the same diameter, except at the input protection where some contacts were elongated. Various metal lines had small "pads" for probing purposes (see Figure 3).

ANALYSIS RESULTS

Die Process and Design:

Figures 1- 22

Questionable Items:¹ None.

Special Features:

- Some metal lines had beveled corners and probe pads.
- Tungsten plugs at contacts.

General Items:

- Fabrication process: Selective oxidation CMOS process employing N-wells in a P substrate. No significant problems were found in the basic process.
- Design implementation: Die layout was clean and efficient. Alignment/registration was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: Two layers of silicon-dioxide (probably undoped). No defects were noted and coverage was good. Edge seal was also good, as the passivation extended into the scribe lane to seal the metallization.
- Metallization: A single level of metallization. Metal consisted of aluminum with a titanium-nitride barrier on a titanium adhesion layer. The metal layer was defined by a dry etch of good quality, but significant rounding of both inside and outside corners was present.
- Metal defects: No voids or cracks were noted in the aluminum. Contacts (plugs) were completed surrounded by metal.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS (continued)

- Metal step coverage: Virtually no metal thinning was present due to the good control of the plug height.
- Contacts: Only very slight over-etching of the contacts was noted. The barrier and adhesion layers were present under the plugs. No defects were found at contacts.
- Intermediate glass: A layer of CVD reflow glass over various grown/densified oxides (TEOS?). This layer was reflowed prior to contact cuts. No problems were found.
- Polysilicon: Two layers of polysilicon. Polycide (poly 2 and tungsten silicide) was used to form all standard gates on the die and the word lines in the array. Poly 1 was used to form the floating gates in the cell array. Definition of the poly layers was by a dry etch of good quality.
- Isolation: Local oxide (LOCOS). No unusual conditions were present at the birdsbeaks or elsewhere.
- Diffusions: Standard N+ and P+ implants were used for bulk sources/drains. It was not possible to determine whether the shallow extension or double diffused method of light doping was used for the LDD process. Deep N+ diffusions may have been present at contacts; however, this could be a staining artifact. The LDD process (to reduce hot electron effects) employed oxide sidewall spacers that were left in place. No problems were found in any of these areas.
- Wells: N-wells were used in a P substrate. Definition was normal. No epi was used.
- Buried contacts: None used.
- Memory Cells: The memory cells consisted of a "stacked dual gate" EPROM design using ONO Enterpoly dielectric. Polycide word lines, poly 1 floating gates, and metal formed the bit lines. Heavy doping was used for source/drains in the array and significant overlap of gates to source/drains was present. These implants were done before sidewall formation. Cell pitch was 2.5 x 2.7 microns.

PROCEDURE

The device was subjected to the following analysis procedures:

SEM inspection of passivation

Delayer to metal and inspect

Aluminum removal and inspect

Delayer to polycide/substrate and inspect

Die material analysis

Die sectioning (90° for SEM)*

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package markings		Could not inspect
Die placement	G	
Wirebond placement		N
Wire spacing		N
Wirebond quality		N
Die attach quality		N
Dicing quality		N
Die attach method		Silver-epoxy (?)
Dicing method:		Sawn (full depth)
Wirebond method:		Ultrasonic wedge bonds using aluminum wire.
Die surface integrity:		
Toolmarks (absence)		G
Particles (absence)		G
Contamination (absence)		G
Process defects (absence)		G
General workmanship	G	
Passivation integrity		G
Metal definition		G
Metal integrity	G	
Metal registration		G
Contact coverage		G
Contact registration		G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

BOTTOM

IS7003BT
KOREA 14629

DIE MATERIAL ANALYSIS

Overlay passivation:	Two layers of silicon-dioxide (probably undoped).
Metallization:	Aluminum.
Barrier:	Titanium-nitride.
Adhesion layer:	Titanium.
Intermediate glass:	CVD reflow glass (probably BPSG) over various densified oxides.
Polycide:	Tungsten-silicide on polysilicon 2.
Interpoly dielectric:	Oxide-nitride-oxide (ONO).

HORIZONTAL DIMENSIONS

Die size:	4 x 4.5 mm (157 x 177 mils)
Die area:	18 mm ² (27,789 mils ²)
Min pad size:	0.11 x 0.11 mm (4.4 x 4.4 mils)
Min pad window:	0.1 x 0.1 mm (3.8 x 3.8 mils)
Min pad space:	0.17 mm (6.5 mils)
Min metal width:	1.0 micron (array)
Min metal space:	1.0 micron (periphery)
Min metal pitch:	2.2 microns (periphery)
Min contact:	0.8 micron
Min polycide width:	0.7 micron
Min polycide space:	0.9 micron
Min poly 1 width:	0.7 micron (floating gate)
Min peripheral gate length* -	
(N-channel):	0.7 micron
(P-channel):	0.85 micron
Cell size:	6.8 microns ²
Cell pitch:	2.5 x 2.7 microns

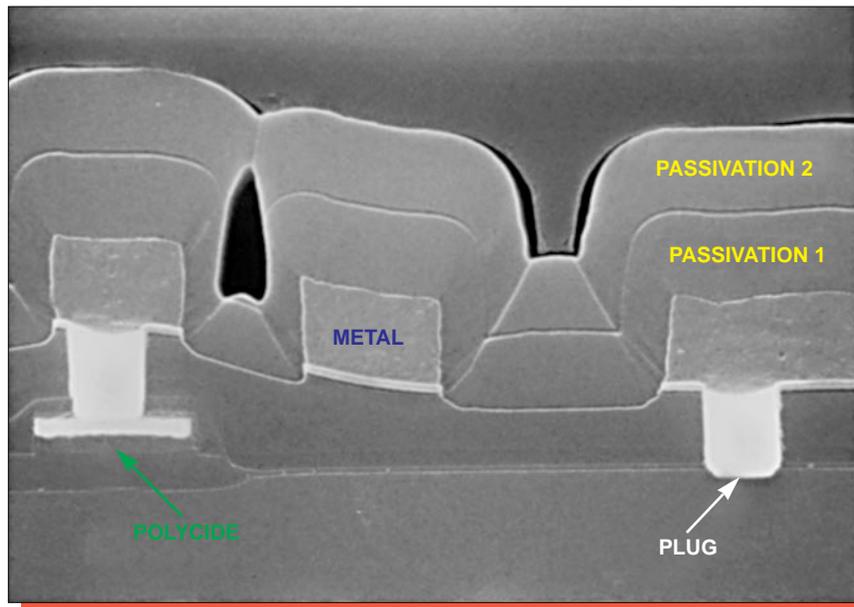
*Physical gate length.

VERTICAL DIMENSIONS

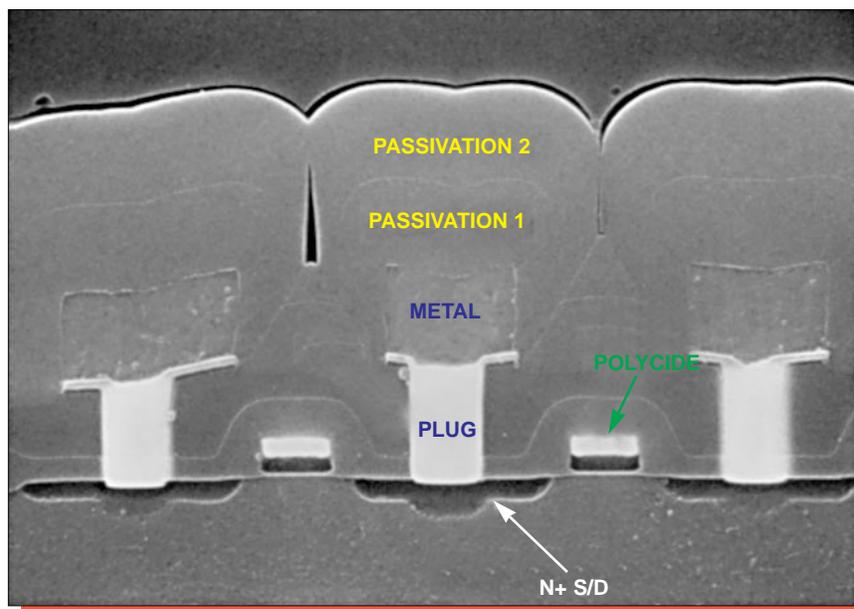
Layers

Passivation 2:	1.0 micron
Passivation 1:	0.9 micron
Metal 1 - aluminum:	0.9 micron
- barrier:	0.1 micron
- adhesion layer:	0.05 micron (approx.)
Intermediate reflow glass:	0.2 - 1.0 micron
Densified oxide:	0.2 micron
Oxide on polycide:	0.2 micron
Polycide - silicide:	0.2 micron
- poly 2:	0.2 micron
Poly 1:	0.15 micron
Local oxide (under polycide):	0.45 micron
N+ S/D periphery:*	0.25 micron (below gate oxide)
N+ S/D cell array:	0.3 micron (below gate oxide)
P+ S/D:	0.4 micron (below gate oxide)
N- well:	5.5 microns

**Lightly doped region could not be delineated.*

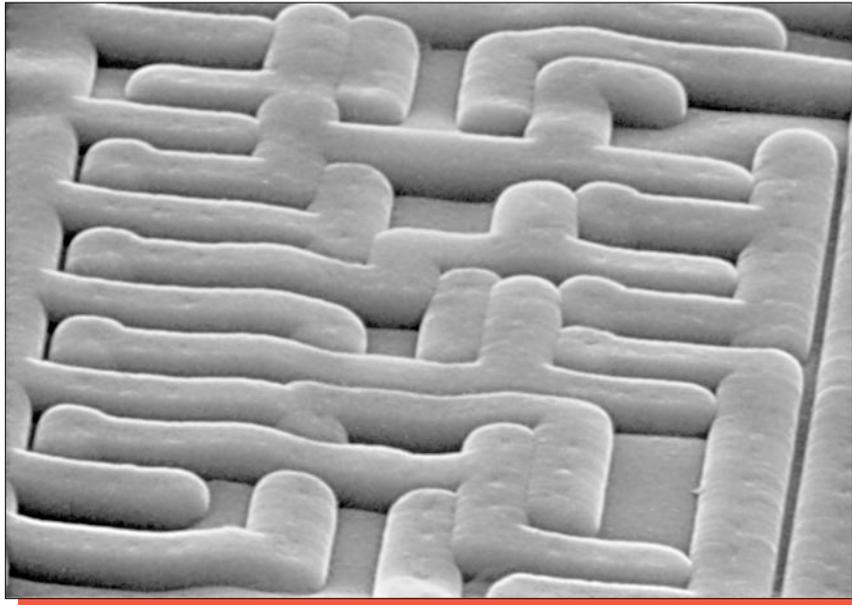


glass etch, Mag. 12,000x

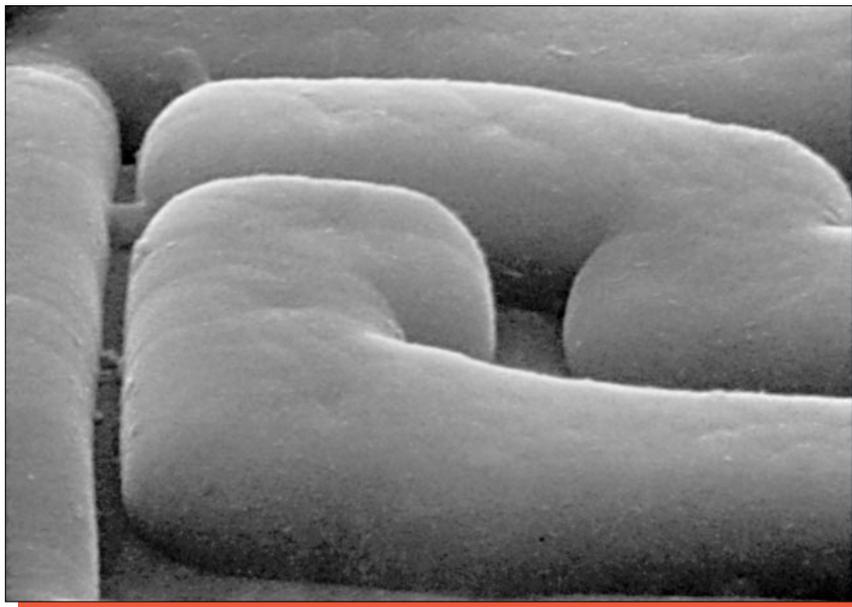


silicon etch, Mag. 13,000x

Figure 1. SEM section views illustrating general device structure on the ISSI IS27HC010.

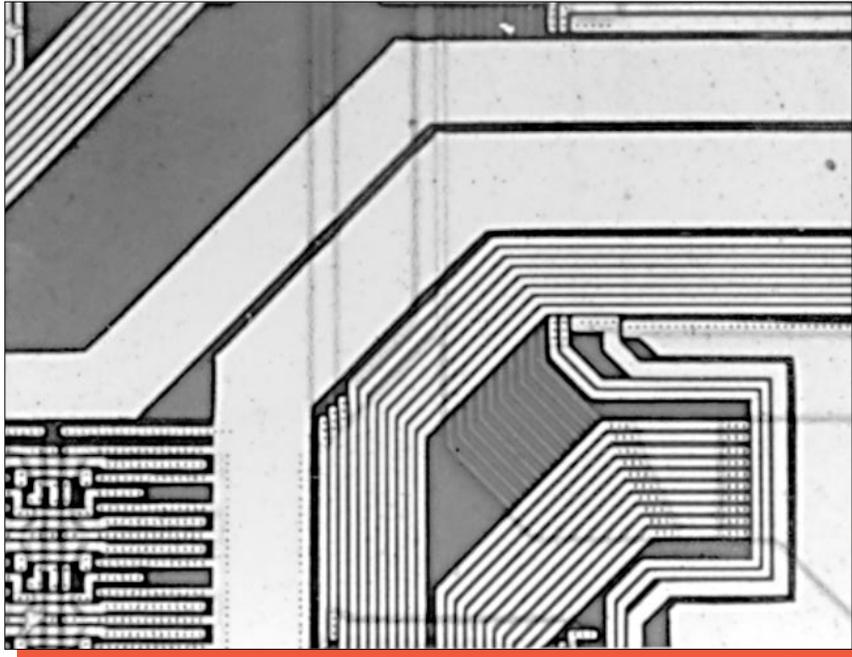


Mag. 3000x

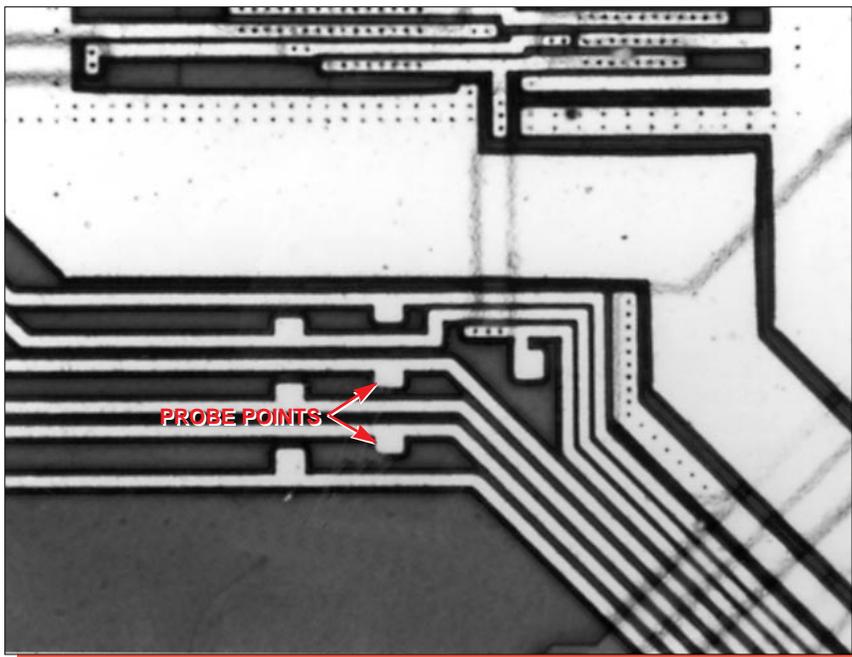


Mag. 10,000x

Figure 2. SEM views of general overlay passivation coverage. 60°.



Mag. 500x



Mag. 800x

Figure 3. Optical views of metal design features.

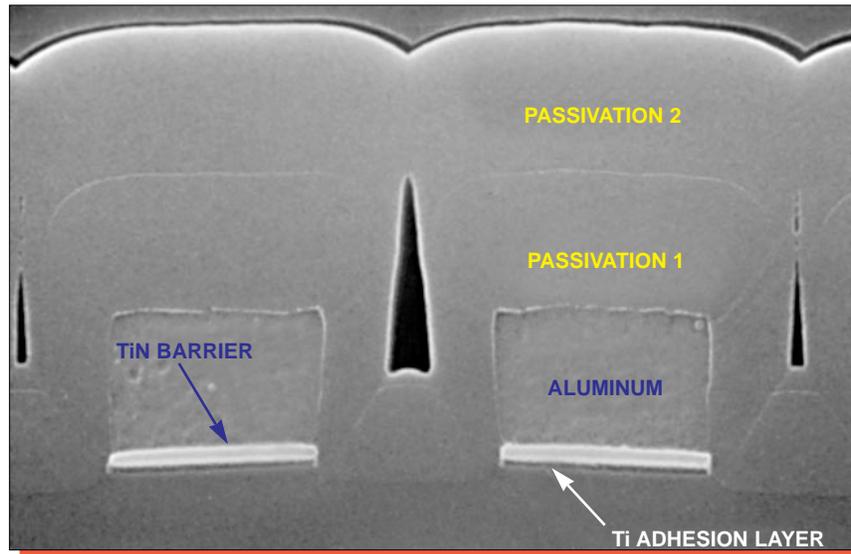


Figure 4. SEM section view of metal line profiles. Mag. 20,000x.

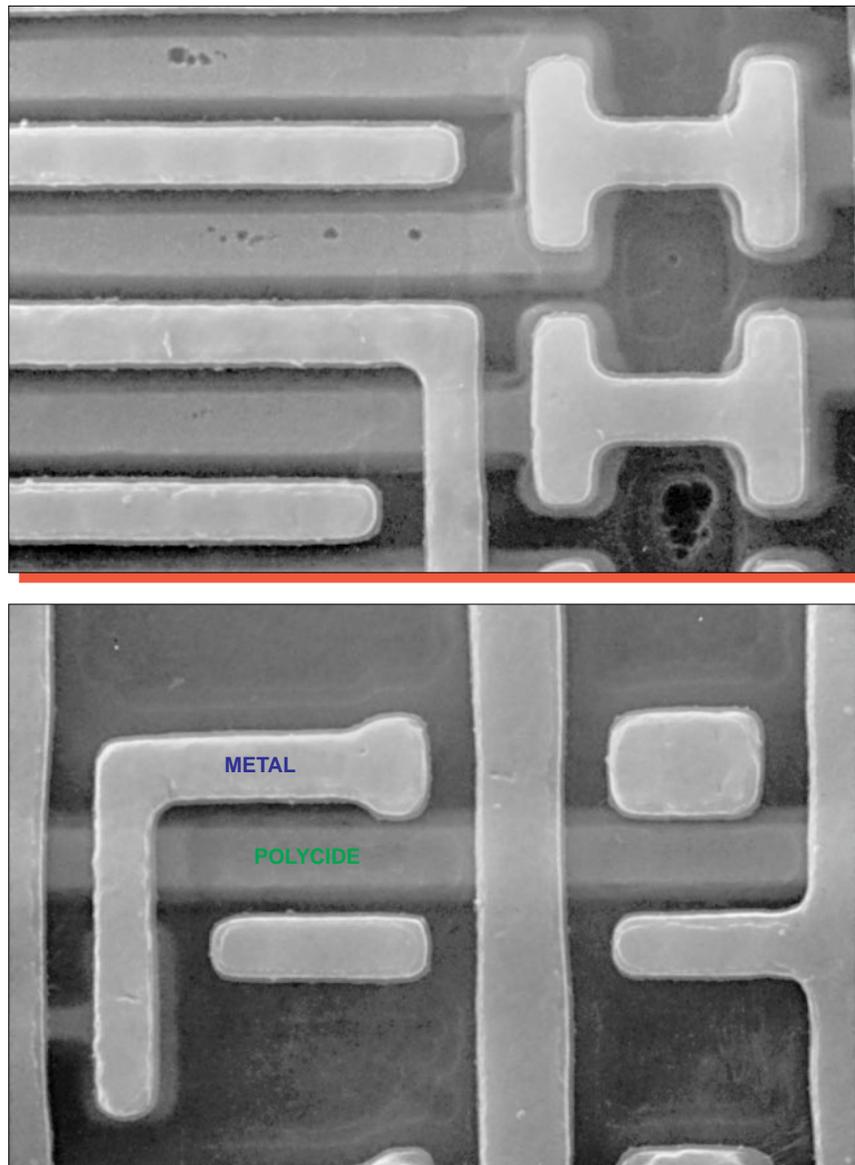
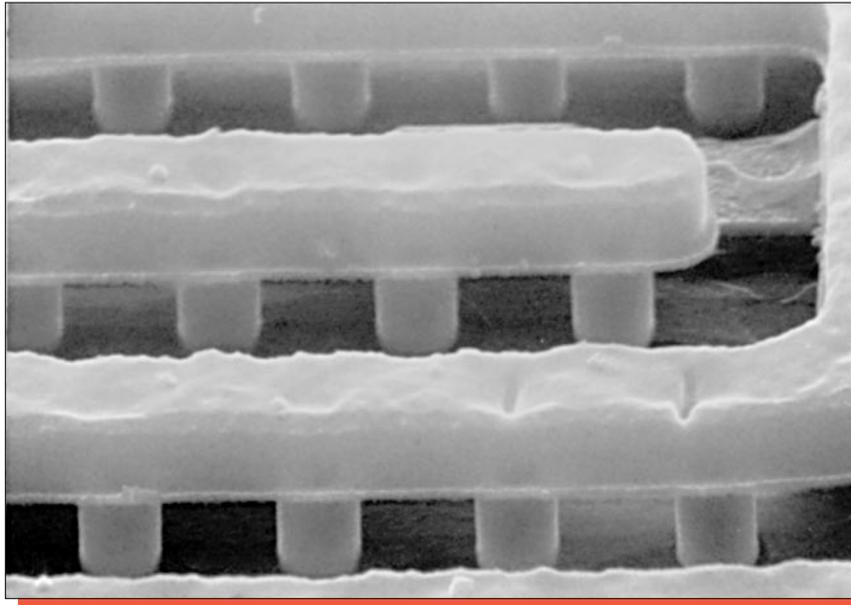
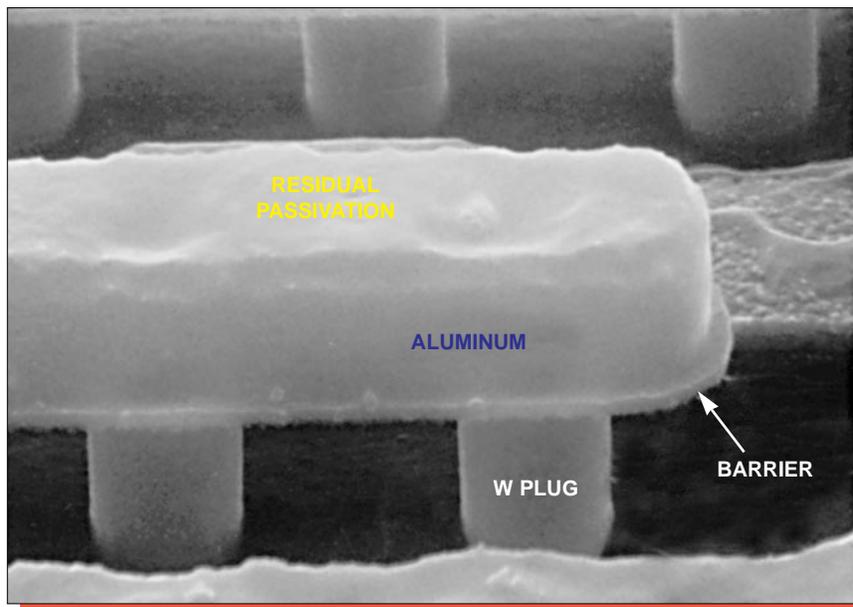


Figure 5. Topological SEM views of metal patterning. Mag. 5500x, 0°.

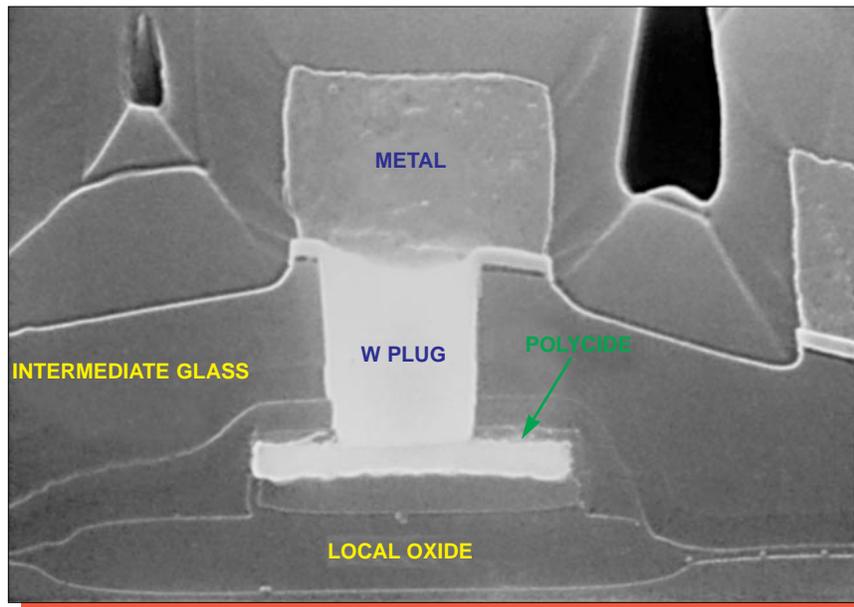


Mag. 12,500x

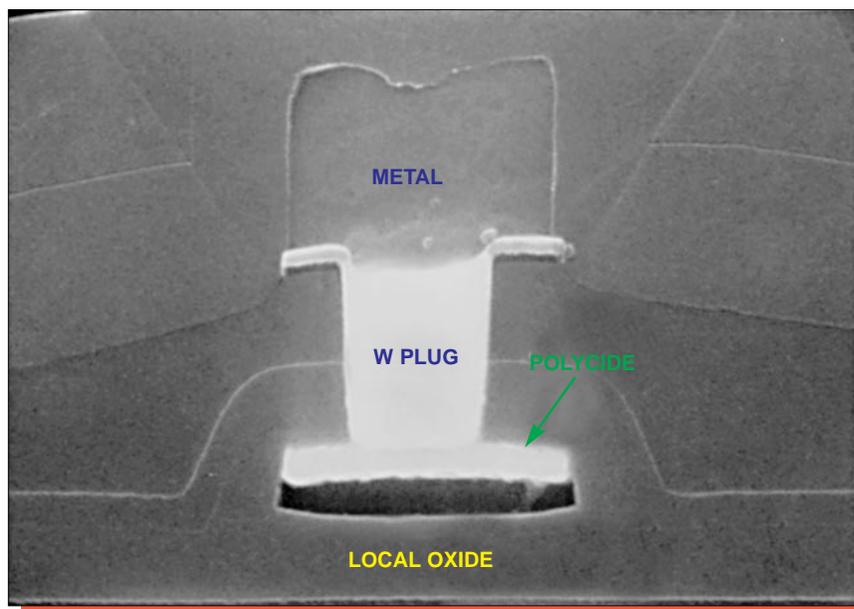


Mag. 23,000x

Figure 6. SEM views illustrating general metal integrity. 60°.



glass etch



silicon etch

Figure 7. SEM section views of metal-to-polycide contacts. Mag. 25,000x.

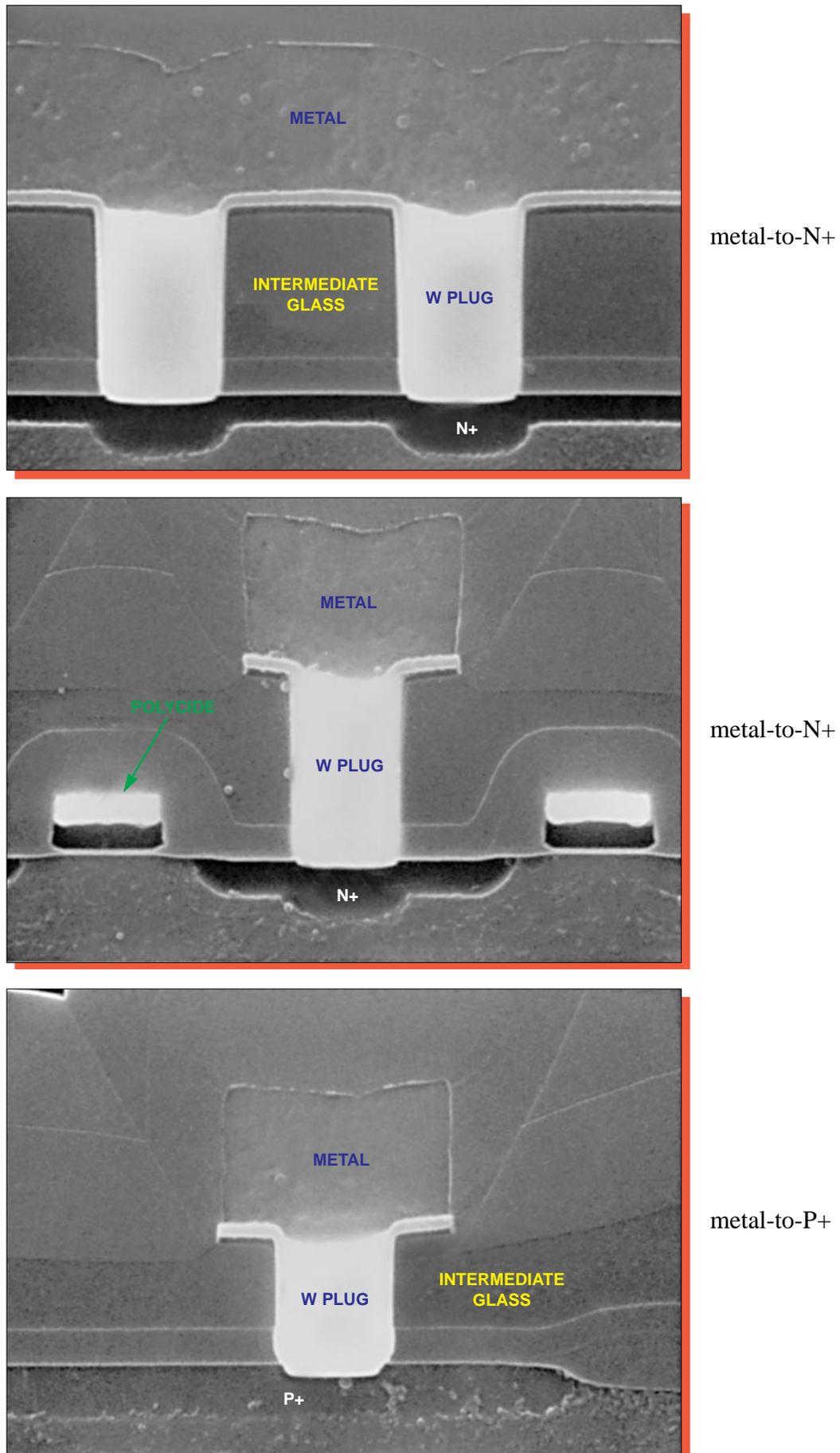


Figure 8. SEM section views of metal-to-diffusion contacts. Mag. 25,000x.

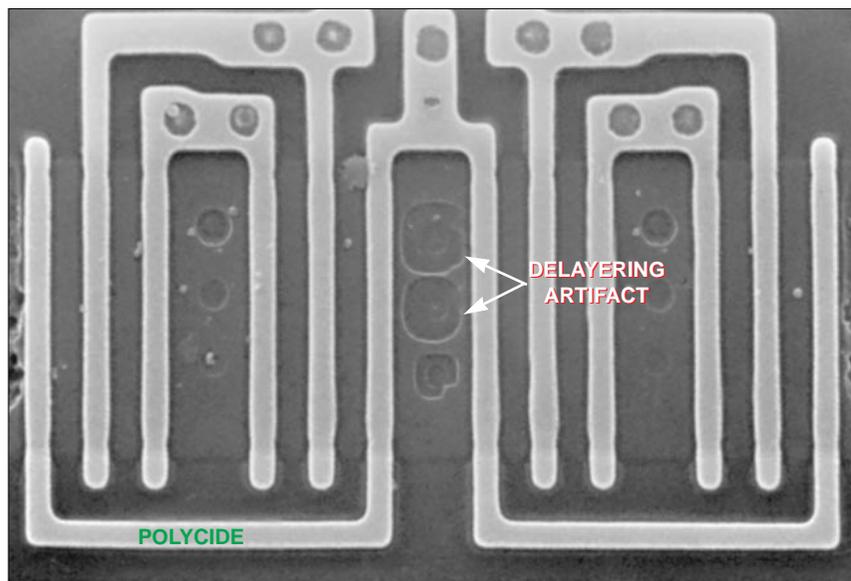
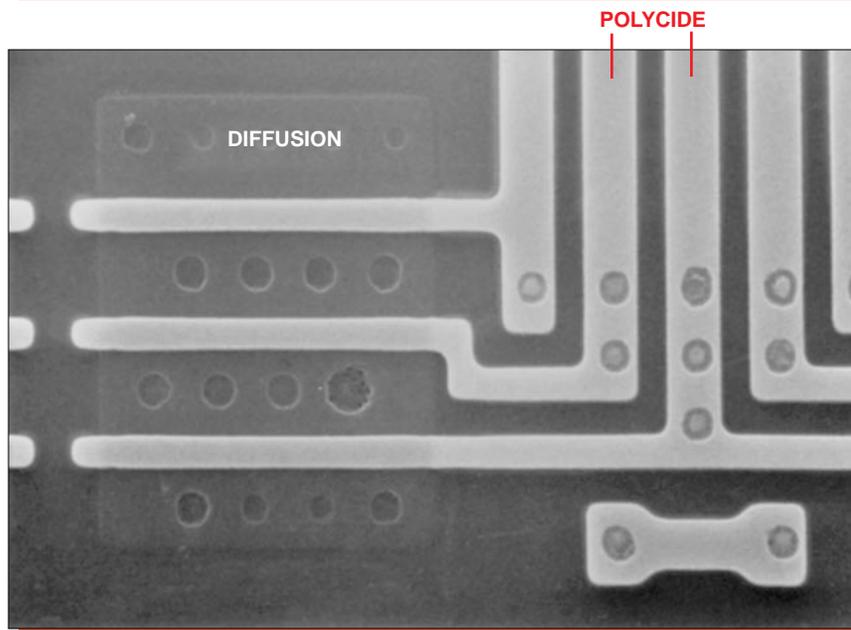
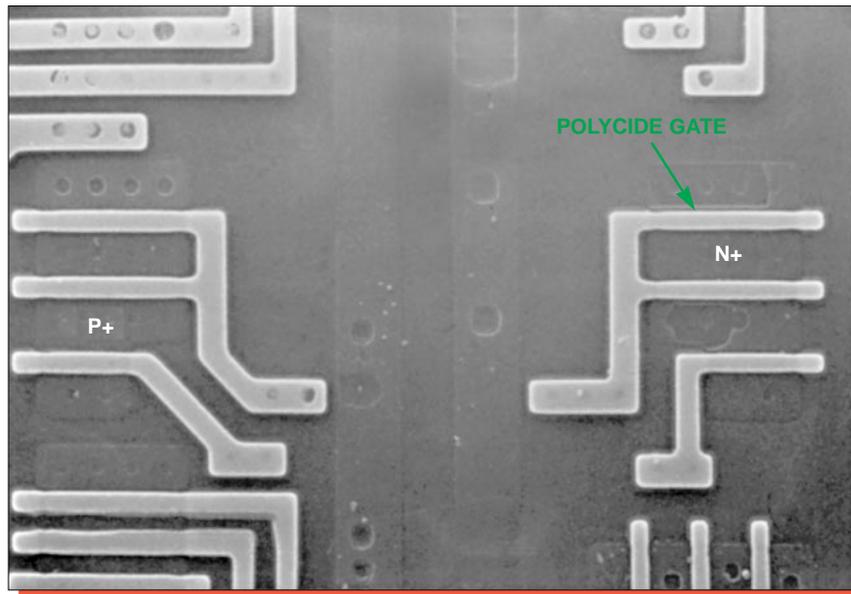
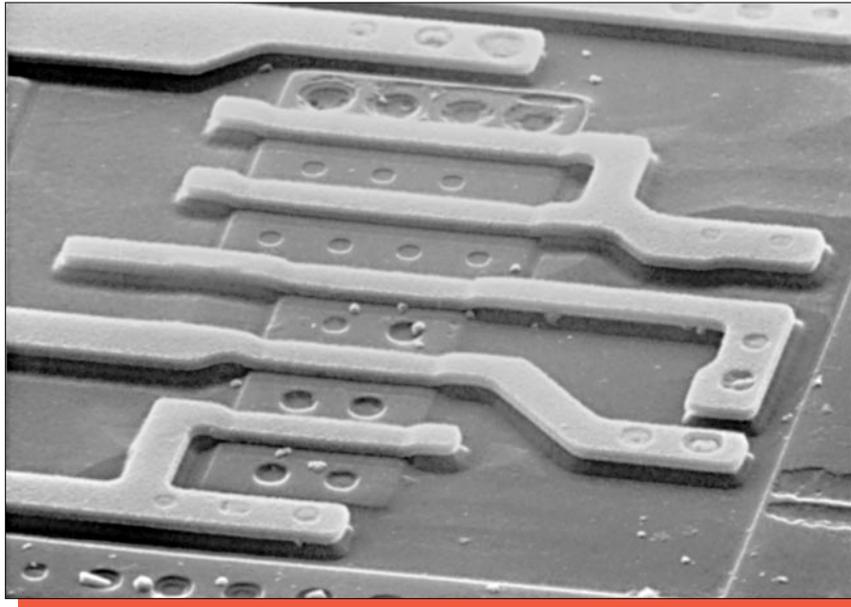
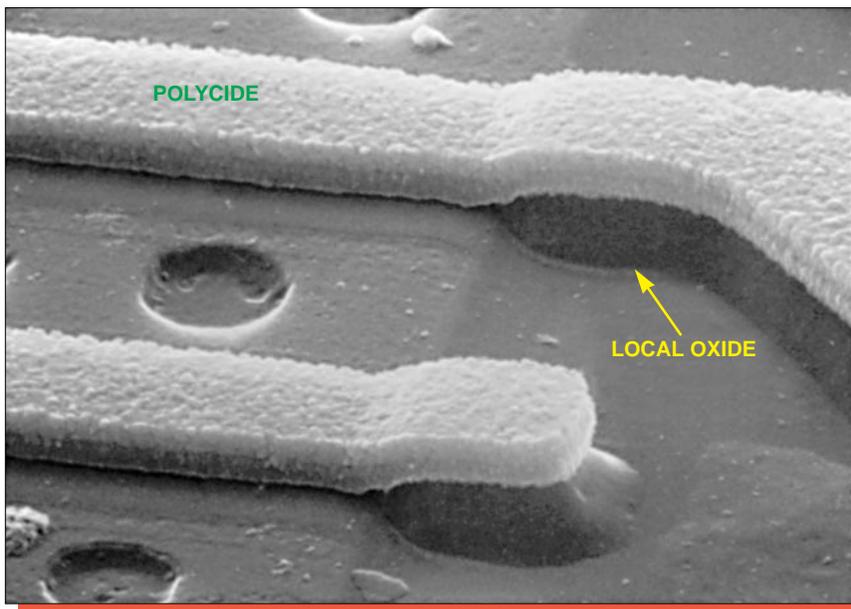


Figure 9. Topological SEM views of polycide patterning. 0°.

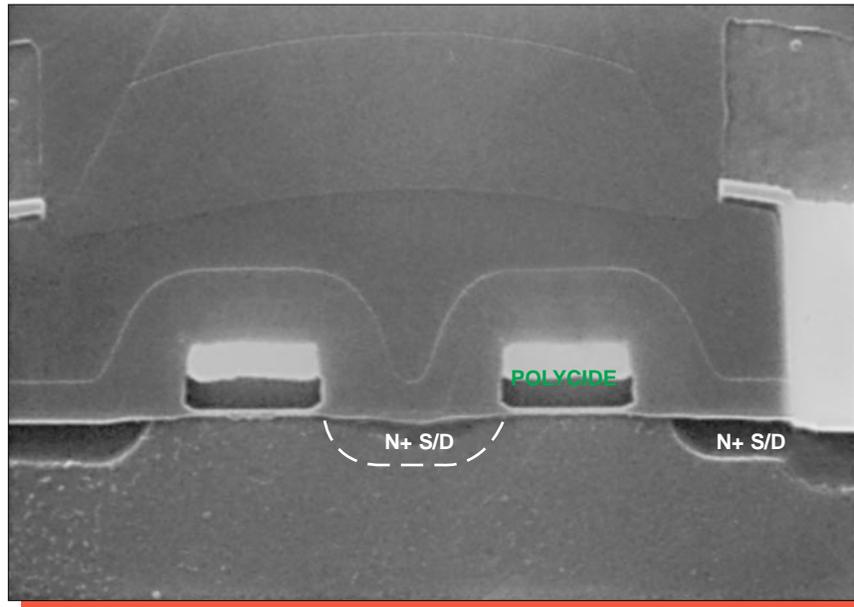


Mag. 5000x

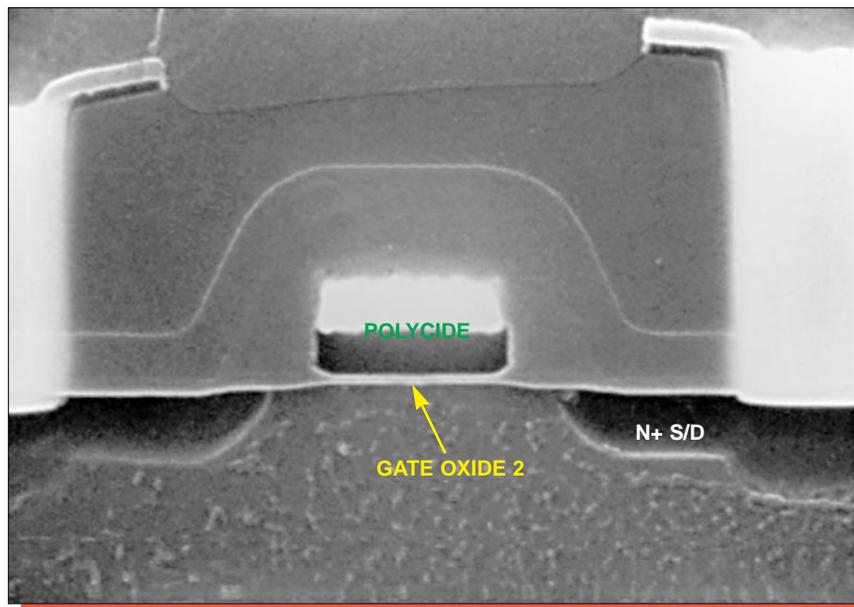


Mag. 20,000x

Figure 10. Perspective SEM views of polycide coverage. 60°.

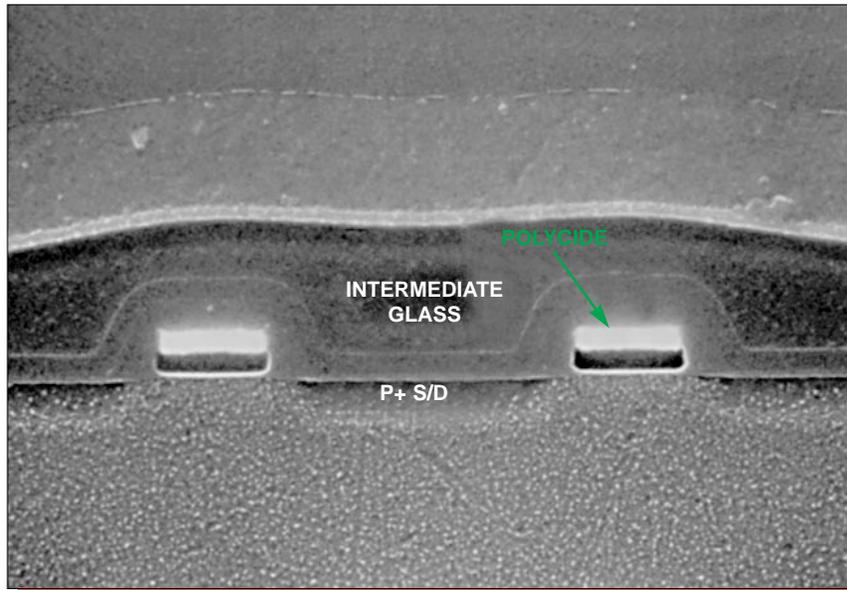


Mag. 25,000x

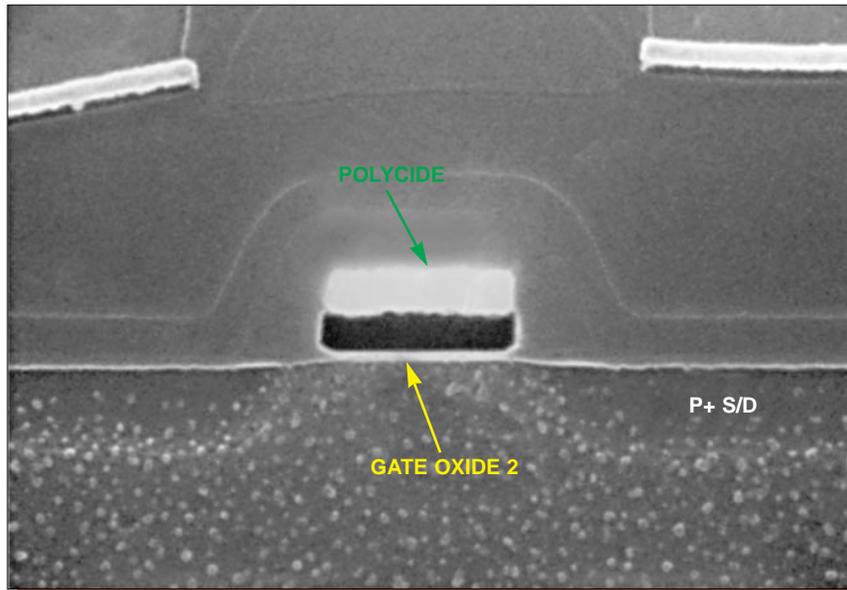


Mag. 35,000x

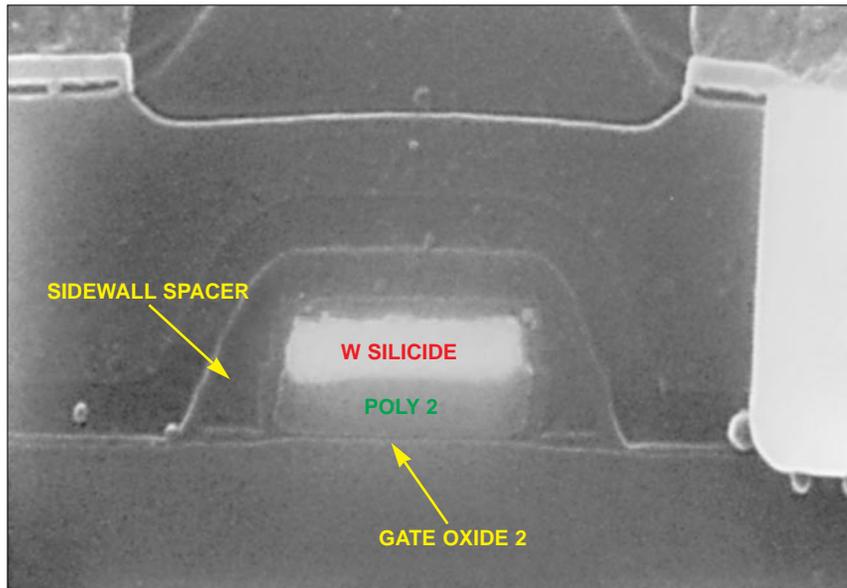
Figure 11. SEM section views of N-channel transistors.



Mag. 15,000x



Mag. 30,000x



glass etch,
Mag. 35,000x

Figure 12. SEM section views of P-channel resistors.

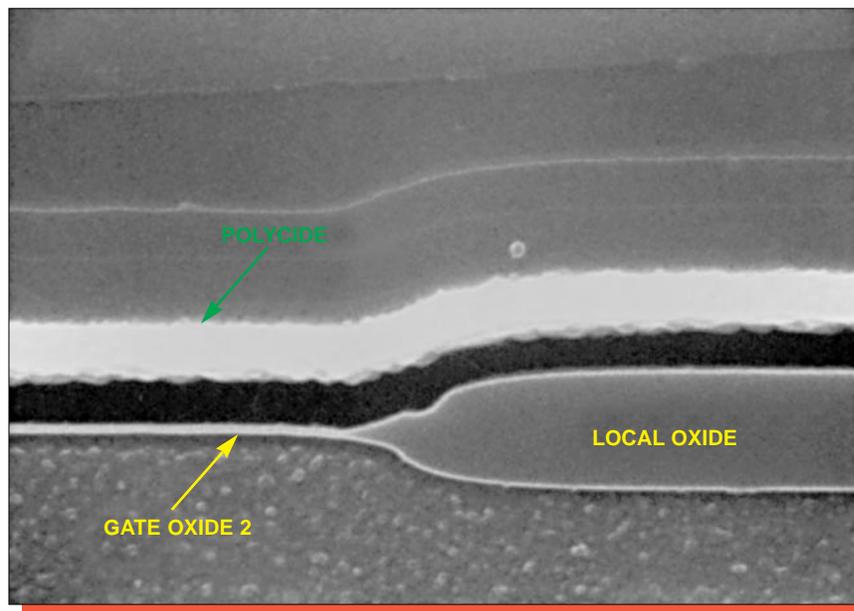


Figure 13. SEM section view of a local oxide birdsbeak profile. Mag. 35,000x.

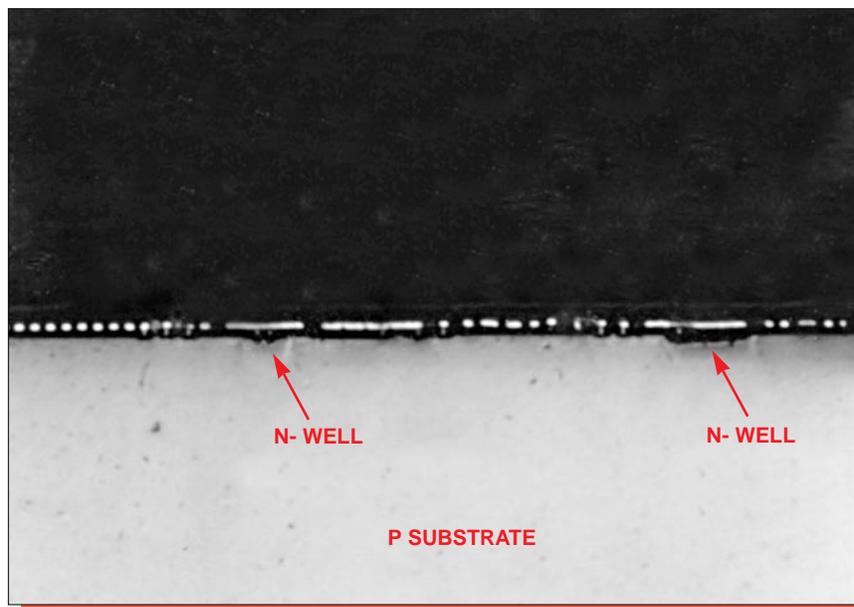
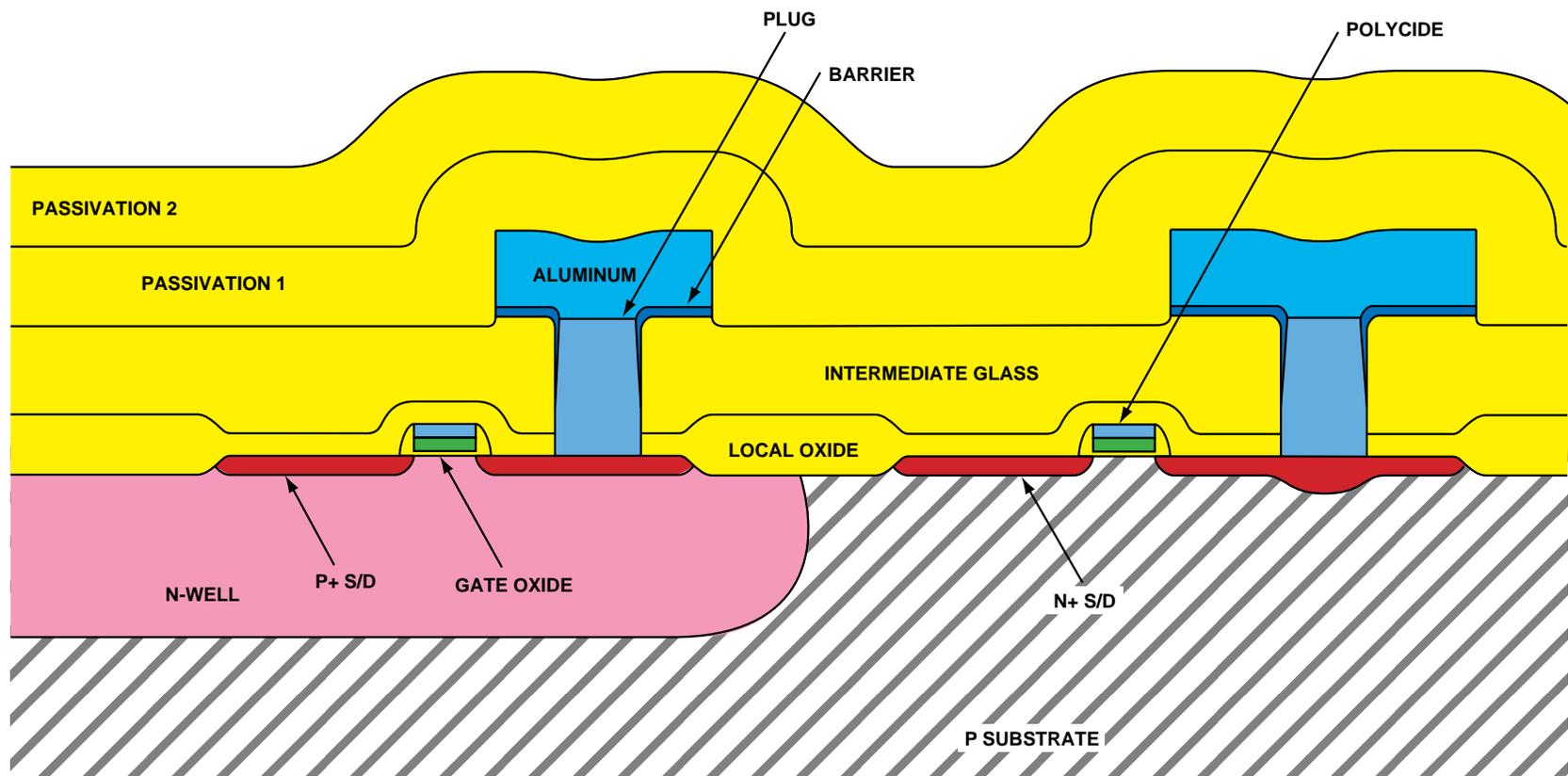


Figure 14. Optical section view of N-wells. Mag. 800x.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,
Red = Diffusion, and Gray = Substrate

Figure 15. Color cross section drawing illustrating device structure.

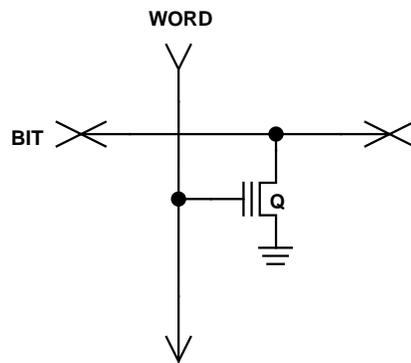
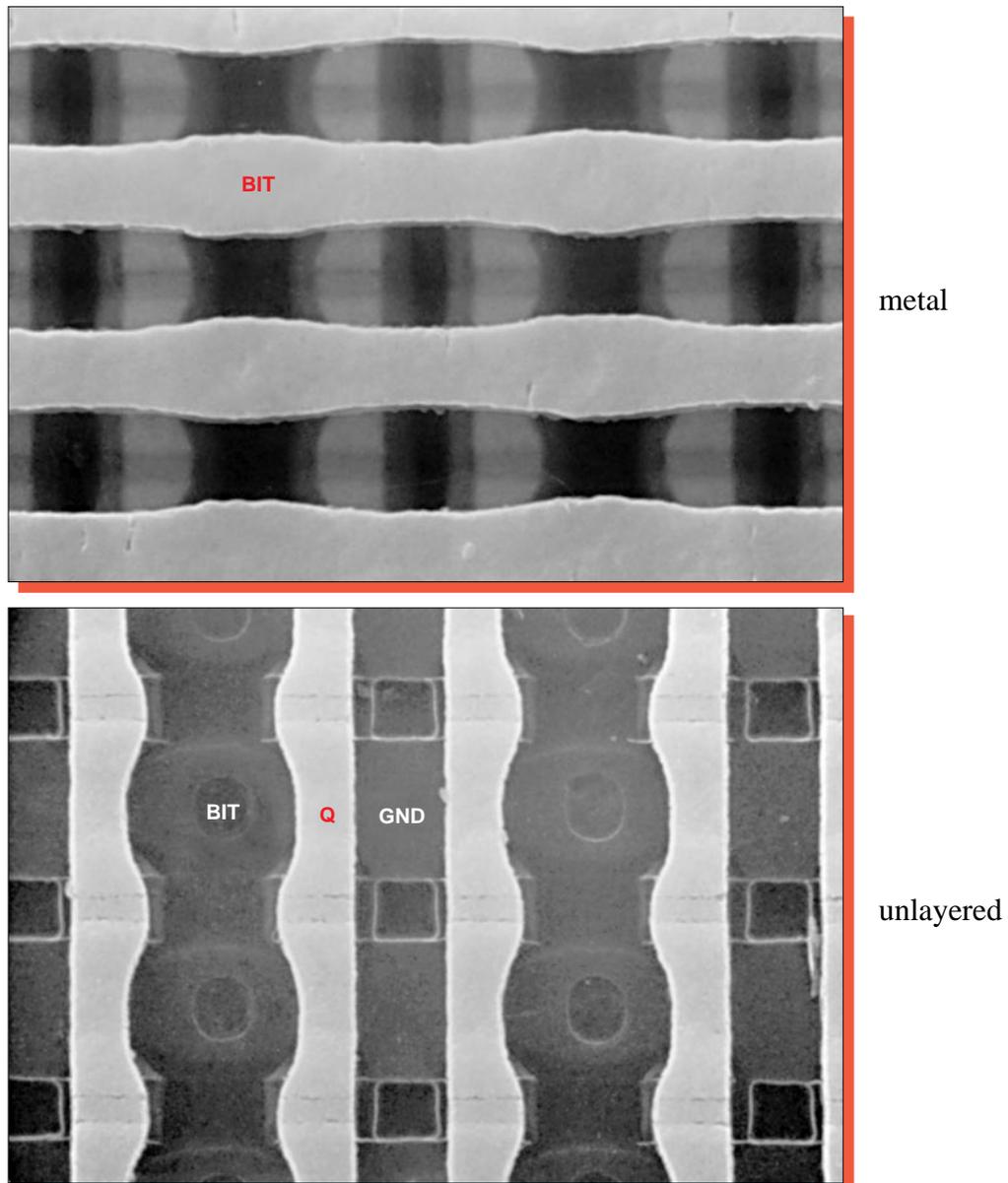
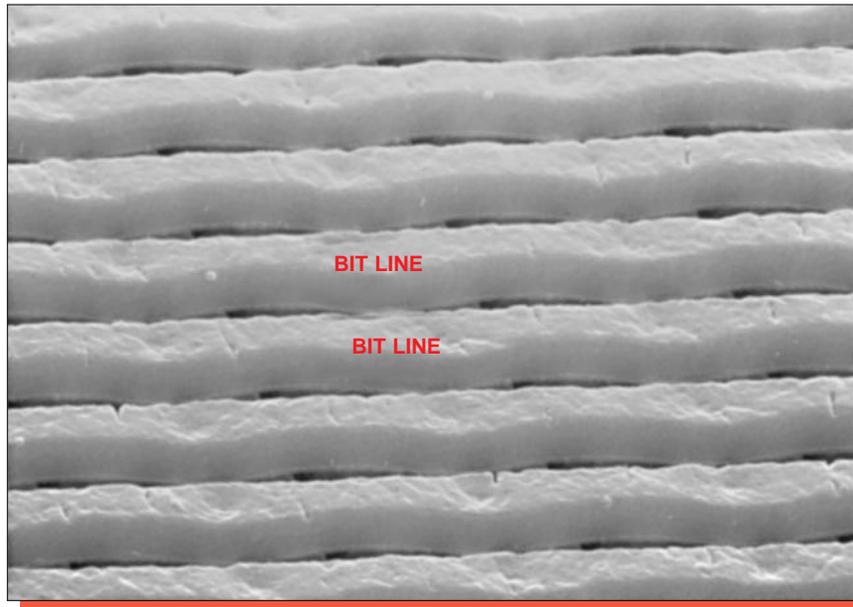
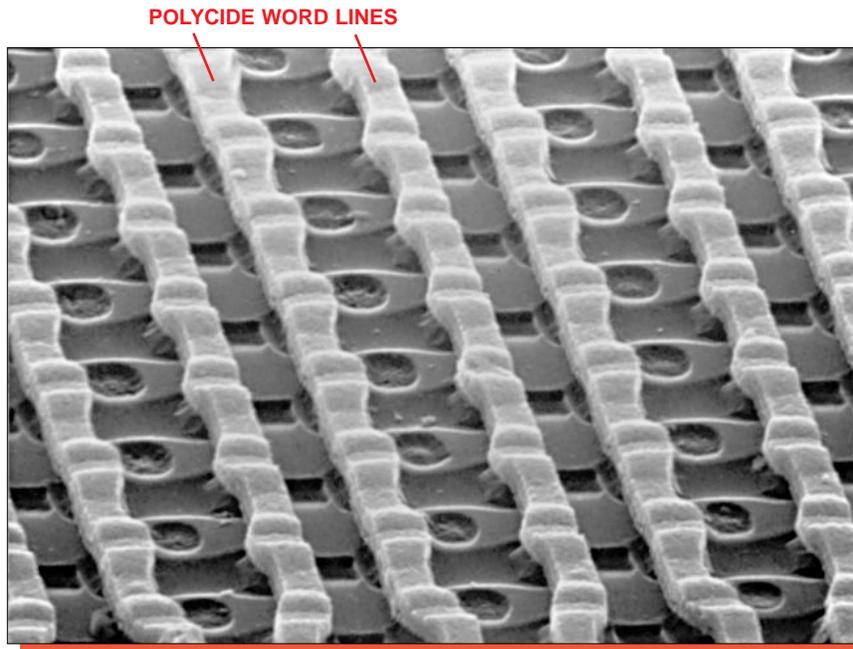


Figure 16. Topological SEM views of the cell array along with the cell schematic.
Mag. 10,000x, 0°.

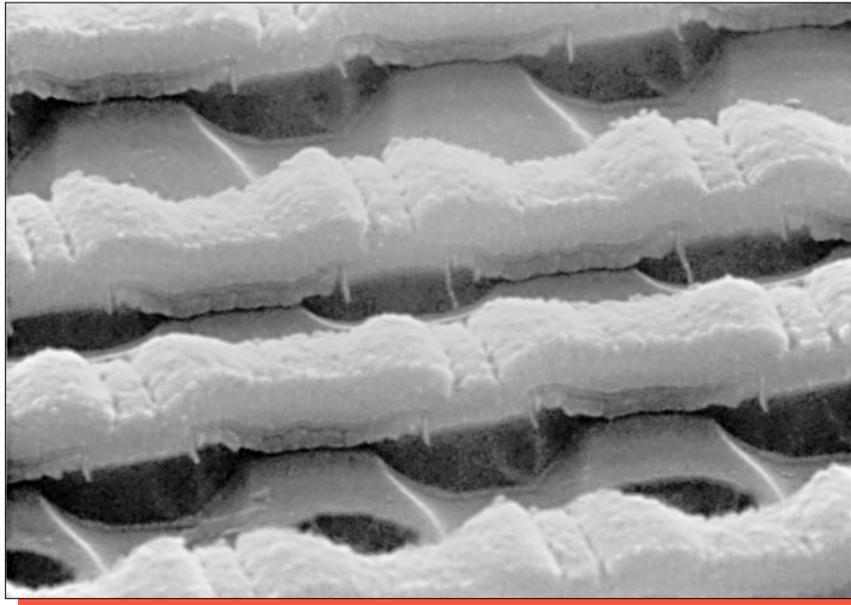


metal

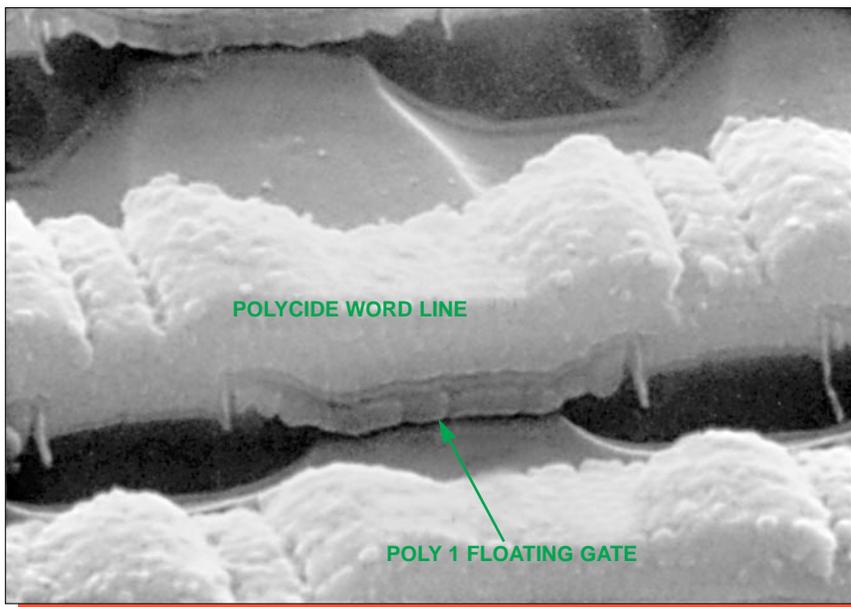


unlayered

Figure 17. perspective SEM views of the cell array. Mag. 8000x, 60°.

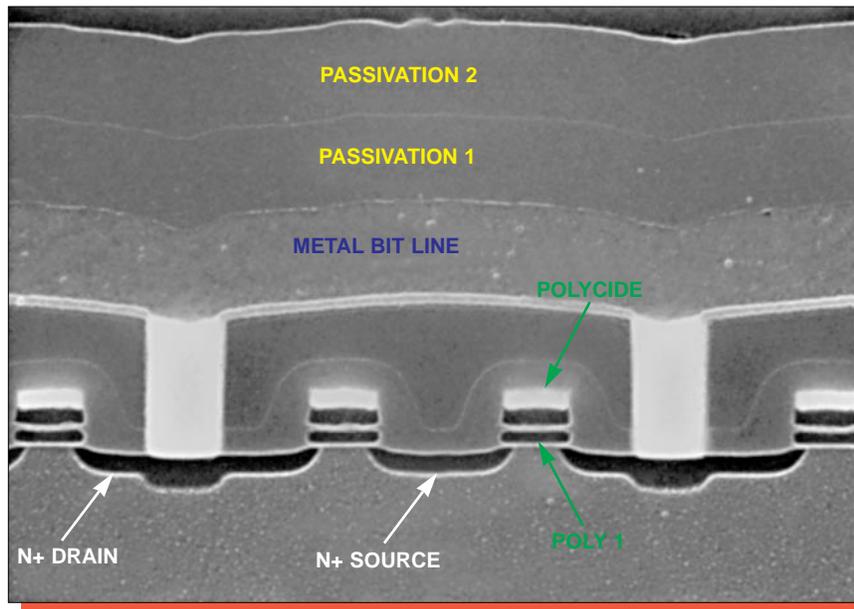


Mag. 20,000x

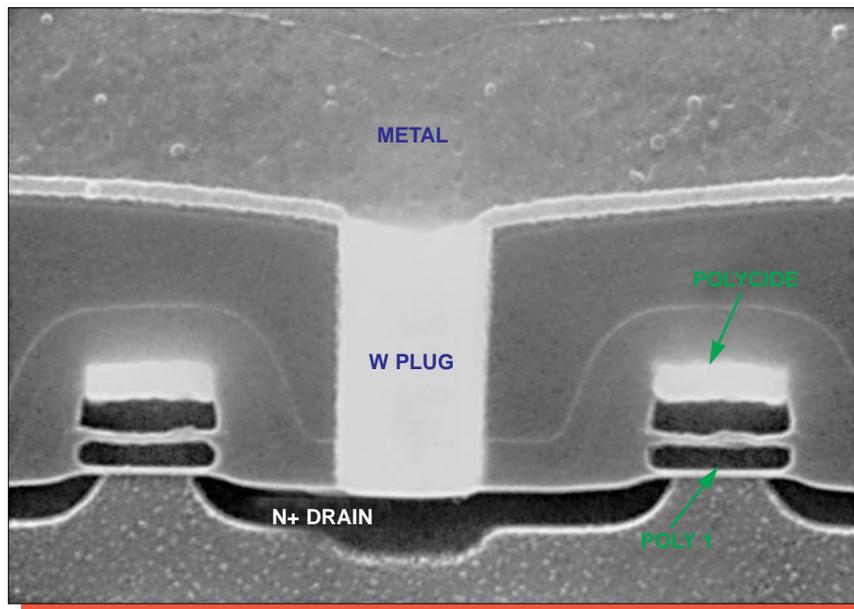


Mag, 35,000x

Figure 18. Detail SEM views of the cell array. 60°.

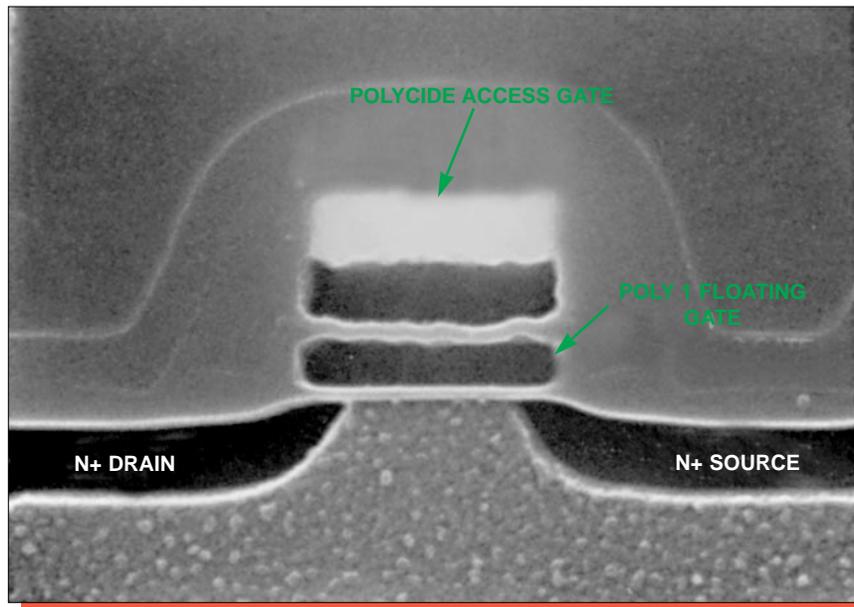


Mag. 13,000x

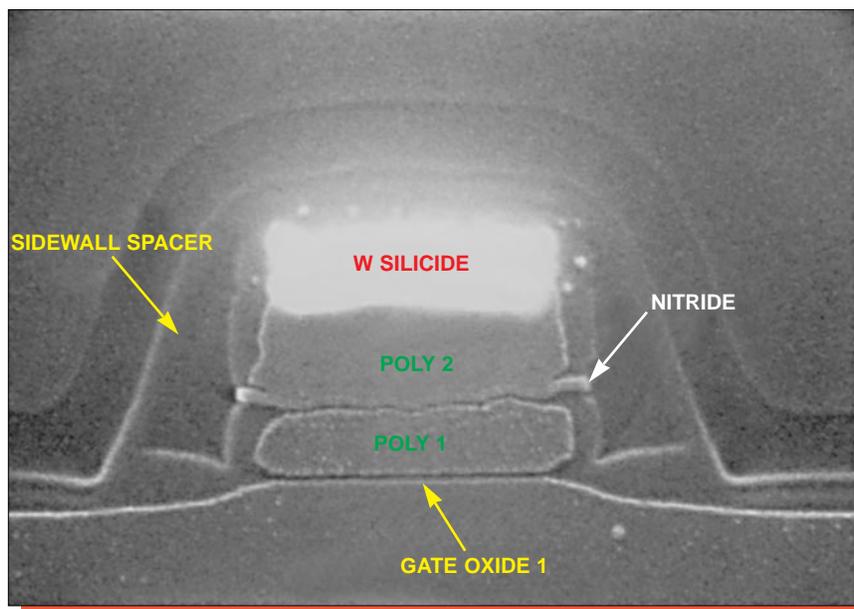


Mag. 25,000x

Figure 19. SEM section views of EPROM cells (X-direction).

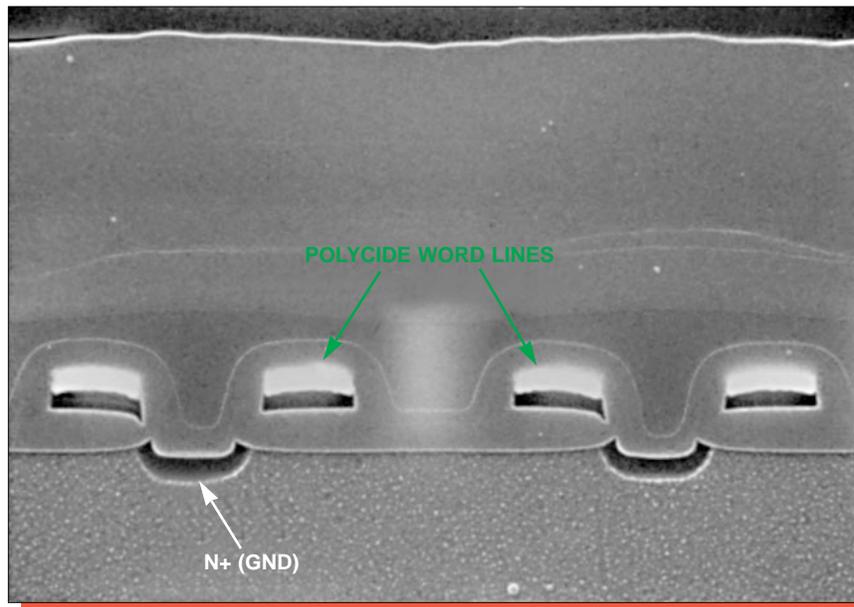


silicon etch, Mag. 45,000x

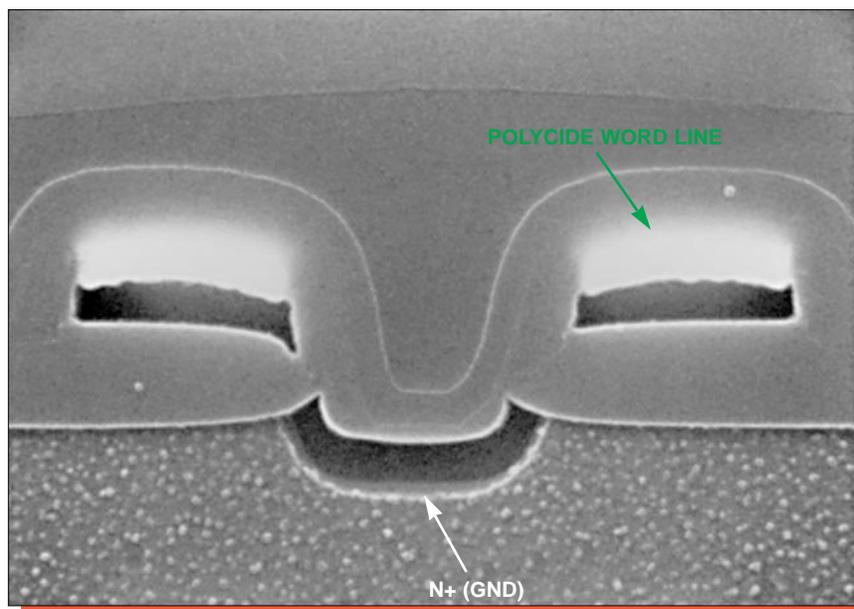


glass etch, Mag. 55,000x

Figure 20. SEM section details of a EPROM cell (X-direction).

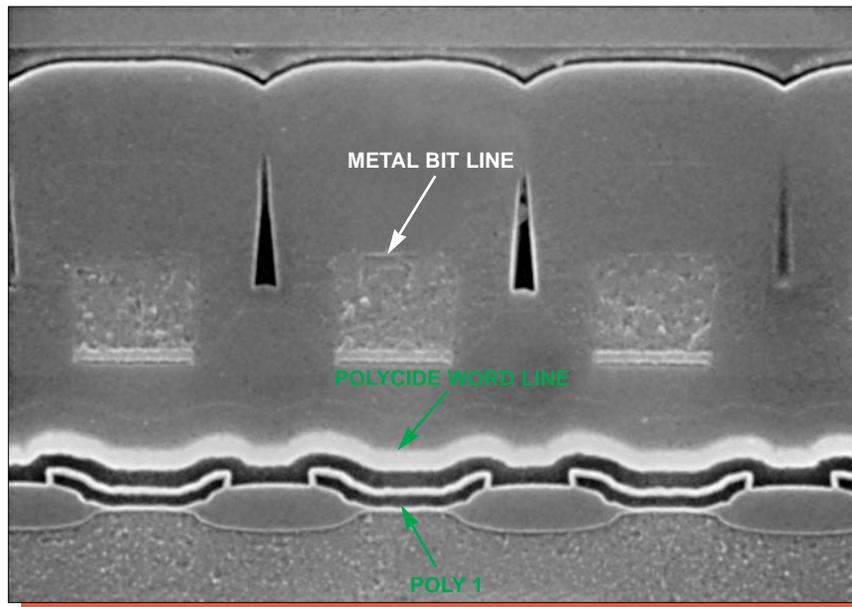


Mag. 12,500x

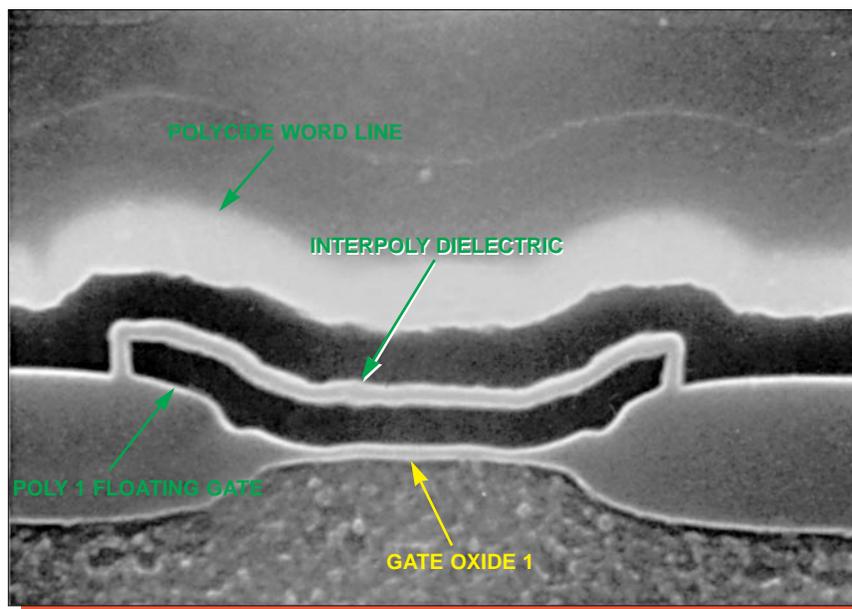


Mag. 30,000x

Figure 21. SEM section views of the cell array (X-direction).



Mag. 13,500x



Mag. 45,000x

Figure 22. SEM section views of EPROM cells (Y-direction).