

# Construction Analysis

## Actel A1440 FPGA

Report Number: SCA 9504-403



**INTEGRATED CIRCUIT ENGINEERING**

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## **INTRODUCTION**

This report describes a construction analysis of the Actel A1440A Field Programmable Gate Array (FPGA). Two devices packaged in a 160-pin Plastic Quad Flat Pack date coded 9424 were received for the analysis.

## **MAJOR FINDINGS**

### **Questionable Items:<sup>1</sup>**

- Metal 2 aluminum thinning up to 85 percent at vias<sup>2</sup> (Figure 12).
- Metal 1 aluminum thinning up to 95 percent<sup>2</sup> at contacts (Figure 18).

### **Special Features:**

- Sub-micron gate lengths (0.75 micron N-channel, 0.8 micron P-channel).

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application*

*<sup>2</sup>Seriousness depends on design margins.*

## TECHNOLOGY DESCRIPTION

### Assembly:

- The devices were packaged in 160-pin, Plastic Quad Flat Packs (PQFP) with gull-wing leads.
- Die was mounted to the header using silver-filled epoxy.
- Die separation by sawn dicing (full depth).
- Wirebonding by the thermosonic ball bond method using 1.2 mil gold wire.

### Die Process:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi on a P substrate.
- Final passivation: A layer of silicon-nitride over a layer of glass.
- Metallization: Two levels of metal defined by dry-etch techniques. Both metal layers consisted of silicon-doped aluminum. Metal 2 employed a titanium barrier. Metal 1 employed a titanium-nitride cap and barrier.
- Interlevel dielectric: Interlevel dielectric consisted of several layers of glass and a filler SOG. Via cuts through these layers were defined by a two step etch.
- Intermediate glass: The intermediate glass consisted of a layer of reflow glass probably Borophosphosilicate glass (BPSG) over various densified oxides. Contact cuts were defined by a two step etch (no reflow following contact cuts). A thin layer of nitride was present beneath the reflow glass.
- Polysilicon: Two layers of polysilicon (no silicide) was used. Poly 1 was used to form gates on the die while poly 2 was used exclusively in the cell array where it formed program lines.

## **TECHNOLOGY DESCRIPTION (continued)**

- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place. Although the 1280A used lightly doped N+ extensions, no such features were noted on this device.
- Wells: twin-wells in an P-epi.
- Programmable antifuse array: The antifuse array is processed with ACTEL'S PLICE (Programmable Low Impedance Circuit Element) technology. Each antifuse consists of very thin dielectric sandwiched between poly 2 program lines and an N+ program diffusion (as indicated by manufacturer's information). The antifuse is programmed by using a voltage to rupture the thin dielectric.

## ANALYSIS RESULTS I

### Assembly:

### Figures 1 - 4

**Questionable Items:**<sup>1</sup> None

**Special Features:** None

### **General Items:**

- Overall package quality: Normal. Device was received decapsulated.
- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. All bond pull strengths were normal and no bond lifts occurred (see page 10).
- Die attach: Silver-(Ag)-filled epoxy. No problems were found.
- Die dicing: Die separation was by sawing (full depth) and showed normal quality workmanship. No chips or cracks were present at the die surface.

*<sup>1</sup>These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

## ANALYSIS RESULTS II

### Die Process:

Figures 5 - 27

### **Questionable Items:<sup>1</sup>**

- Metal 2 aluminum thinning up to 85 percent at vias<sup>2</sup> (Figure 12).
- Metal 1 aluminum thinning up to 95 percent<sup>2</sup> at contacts (Figure 18).

### **Special Features:**

- Sub-micron gate lengths (0.75 micron N-channel, 0.8 micron P-channel).

### **General Items:**

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P-epi on a P substrate. No significant problems were found in the basic process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels. Slotted bus lines were used in both metal 2 and metal 1.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A layer of silicon-nitride over a layer of glass. Passivation integrity tests indicated defect-free passivation. Edge seal was also good.
- Metallization: Two levels of metallization. Both levels consisted of silicon-doped aluminum. Metal 2 employed a titanium barrier. Metal 1 employed a titanium-nitride cap and barrier.
- Metal patterning: Both metal layers were defined by a dry etch of good quality.

<sup>1</sup>*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

<sup>2</sup>*Seriousness depends on design margins.*

## ANALYSIS RESULTS II (continued)

- Metal defects: No notching or voiding of either metal layer was found. No significant silicon nodules were found following the removal of either metal layer.
- Metal step coverage: **Metal 2 aluminum thinning up to 85 percent was found at vias. Metal 1 aluminum thinned up to 95 percent at some contact edges. Total metal 1 thinning (including cap and barrier) was typically 90 percent.** MIL-STD 883D allows up to 70 percent metal thinning for contacts of this size. Some excessive thinning was due to the rough surface of the metal in contact areas where grooves in the surface created isolated areas of thinning.
- Interlevel dielectric: Interlevel dielectric consisted of several layers of glass with a filler SOG. Contact cuts were defined by a two step etch.
- Intermediate glass: The intermediate glass consisted of a layer of reflow glass, probably borophosphosilicate glass (BPSG) over various densified oxides. A thin layer of nitride was present beneath this layer.
- Polysilicon: Two layers of polysilicon (no silicide) was used. Poly 1 was used to form all gates on the die while poly 2 was used exclusively in the cell array where it formed program lines.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere. A step was noted between the wells.
- Diffusions: Implanted N+ and P+ diffusions were used for sources and drains. An LDD process was used employing oxide sidewall spacers. The spacers were left in place. Although the 1280A used lightly doped N+ extensions, no such features were noted on this device. No problems were found in any of these areas.
- Wells: Twin-wells appeared to be used in an P-epi. No problems were apparent.
- Buried contacts: No buried contacts were noted.

## **ANALYSIS RESULTS II (continued)**

- Programmable antifuse array: The antifuse array is processed with ACTEL'S PLICE (Programmable Low Impedance Circuit Element) technology. Each antifuse consists of very thin dielectric sandwiched between poly 2 program lines and an N+ program diffusion (as indicated by manufacturer's information). The antifuse is programmed by using a voltage to rupture the thin dielectric.
- Mask count: The device appeared to use 18 masks which is one more than the 1280A.

## PROCEDURE

The devices were subjected to the following analysis procedures:

Internal optical inspection

SEM inspection of assembly features and passivation

Wirepull tests

Passivation integrity test

Delayer to metal 2 and inspect

Aluminum removal (metal 2), inspect

Delayer to metal 1 and inspect

Aluminum removal (metal 1), inspect

Delayer to poly/substrate and inspect

Die sectioning (90° for SEM)\*

Measure horizontal dimensions

Measure vertical dimensions

*\*Delineation of cross-sections is by silicon etch unless otherwise indicated.*

**OVERALL QUALITY EVALUATION:** Overall Rating: Normal

**DETAIL OF EVALUATION**

Package integrity	-
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	G
Dicing quality	G
Die attach method	Silver (Ag) filled epoxy
Dicing method	Sawn (full depth)
Wirebond method:	Thermosonic ball bonds using 1.2 mil gold wire
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	NP <sup>1</sup>
Metal integrity	P <sup>2</sup>
Metal registration	N
Contact coverage	N
Contact registration	G

<sup>1</sup> Rough surface in contacts.

<sup>2</sup>Aluminum thinning up to 95 percent.

G = Good, P = Poor, N = Normal, NP = Normal/Poor

## WIREBOND STRENGTH

Wire material: 1.2 mil diameter gold

Die pad material: aluminum

	<u>1</u>
# of wires tested:	26
Bond lifts:	0
Force to break - high:	10.5g
- low:	8.0g
- ave.:	9.1g
- std. dev.:	0.8

## DIE MATERIAL ANALYSIS (EDX)

Overlay passivation: Silicon-nitride over a layer of glass.

Metallization 2: Silicon-doped aluminum with a titanium barrier.

Interlevel dielectric: Two layers of silicon-dioxide with a filler SOG.

Metallization 1: Silicon-doped aluminum with a titanium nitride cap and barrier.

Intermediate glass: A layer of reflow glass over densified oxides.



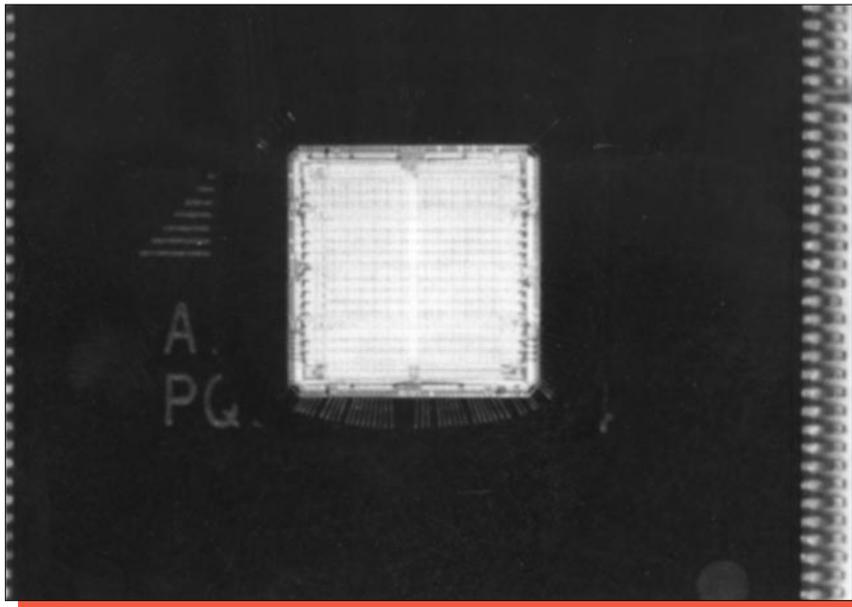
## VERTICAL DIMENSIONS

### Layers:

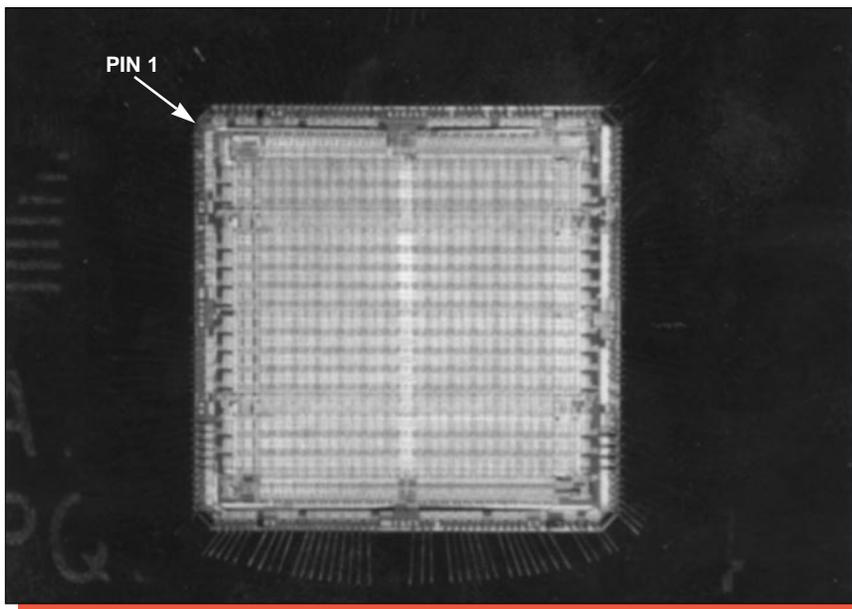
Passivation 2:	0.6 micron
Passivation 1:	0.3 micron
Metal 2:	
- aluminum:	1.0 micron
- barrier:	0.15 micron
Interlevel dielectric:	
- glass 3:	0.25 micron
- glass 2:	0.09 micron
- glass 1:	0.15 micron
Metal 1 - cap:	0.05 micron (approximate)
- aluminum:	0.5 micron
- barrier:	0.1 micron
Intermediate (reflow) glass:	0.6 micron
Nitride layer:	0.04 micron (approximate)
Oxide on poly:	0.07 micron (approximate)
Poly 2:	0.28 micron
Poly 1:	0.28 micron
Local oxide:	0.6 micron
N+ S/D diffusion:	0.25 micron
N+ program diffusion:	0.4 micron (approximate)
P+ S/D diffusion:	0.3 micron
N- well:	4.5 microns
Epi:	9.5 microns
Approximate mask count:	18

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DIE LAYOUT AND IDENTIFICATION	Figures 5 - 6a
PHYSICAL DIE STRUCTURES	Figures 7 - 26
PROCESS DRAWING	Figure 27



Mag. 3.5x



Mag. 6.5x

Figure 1. Cavity photographs of the ACTEL A1440 FPGA.

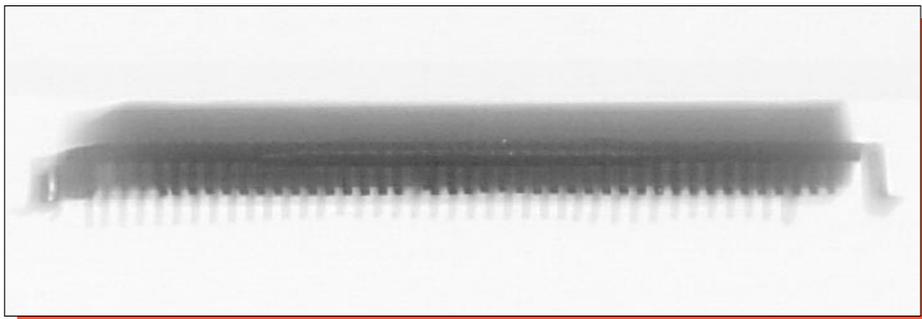
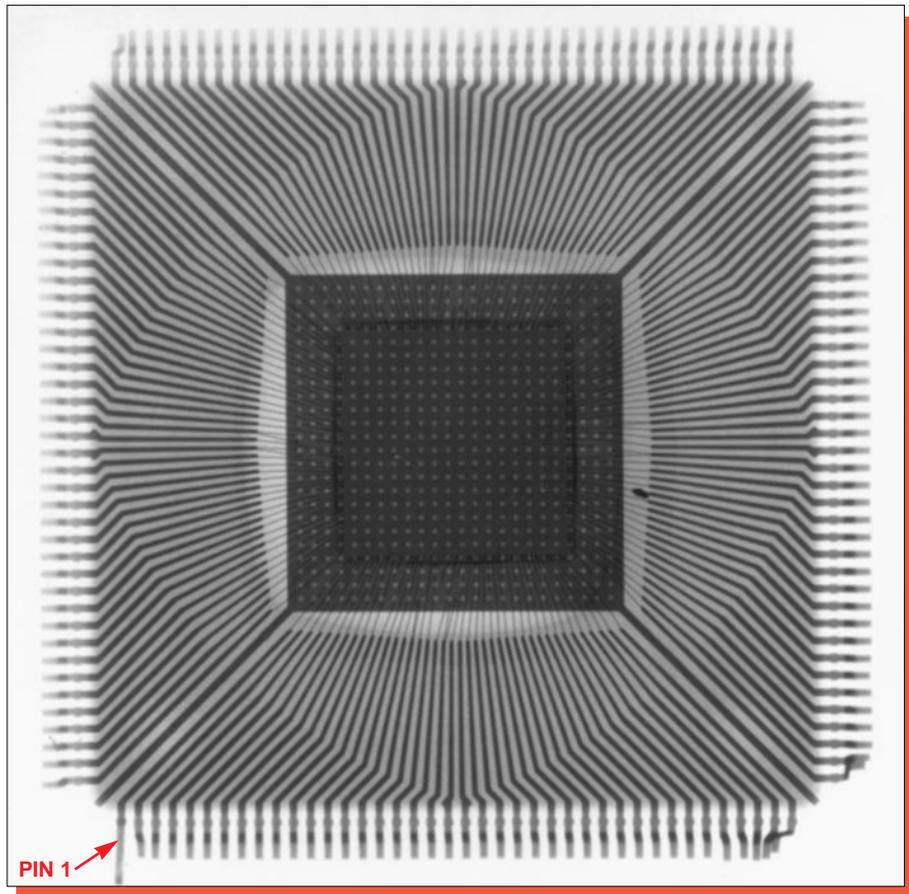


Figure 2. X-ray views of the decapsulated package. Mag. 3.5x.

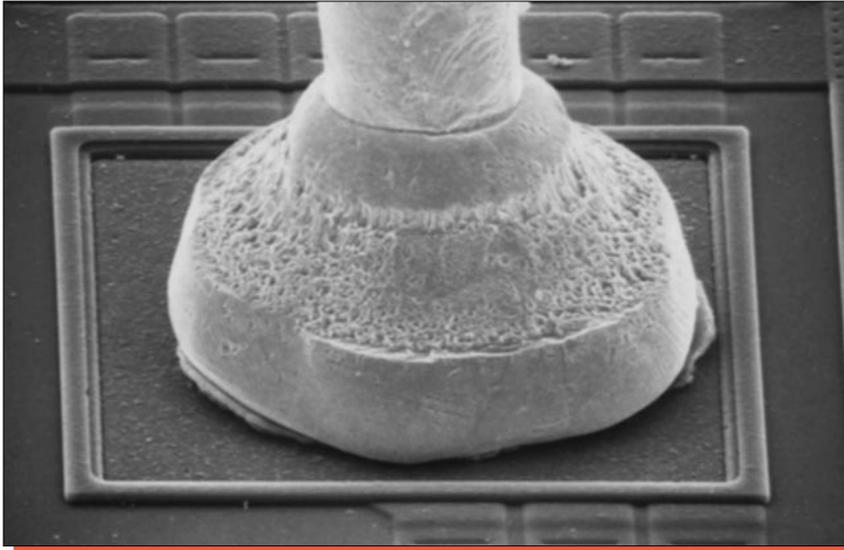
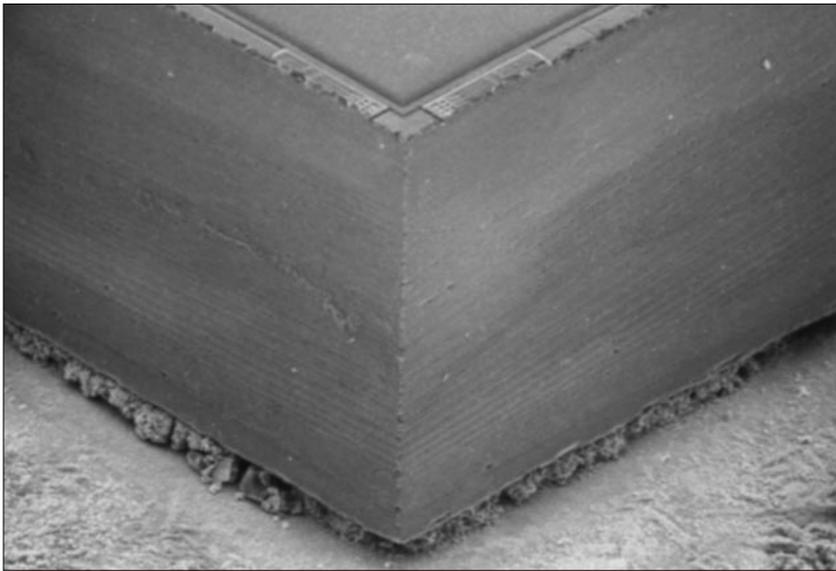
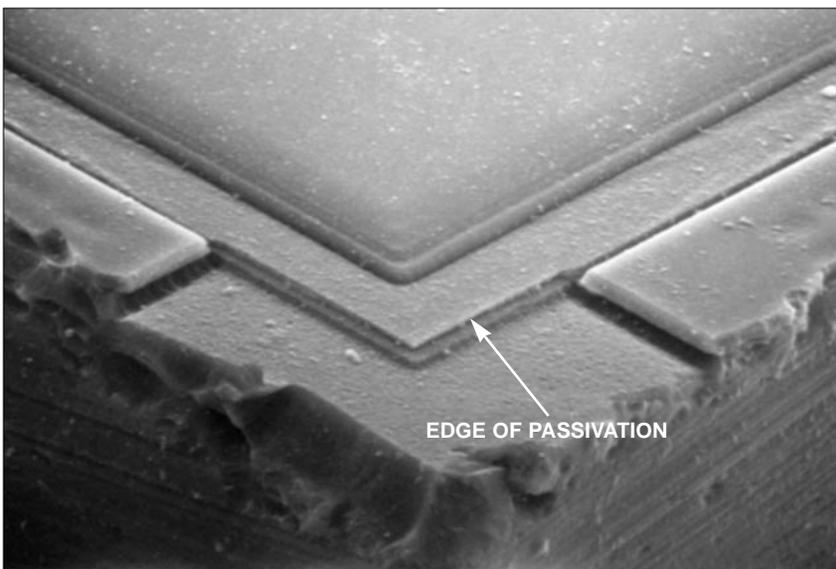


Figure 3. SEM view of a typical ball bond. Mag. 880x, 60°.



Mag. 160x



Mag. 1300x

Figure 4. SEM views of dicing, die attach, and edge seal. 60°.

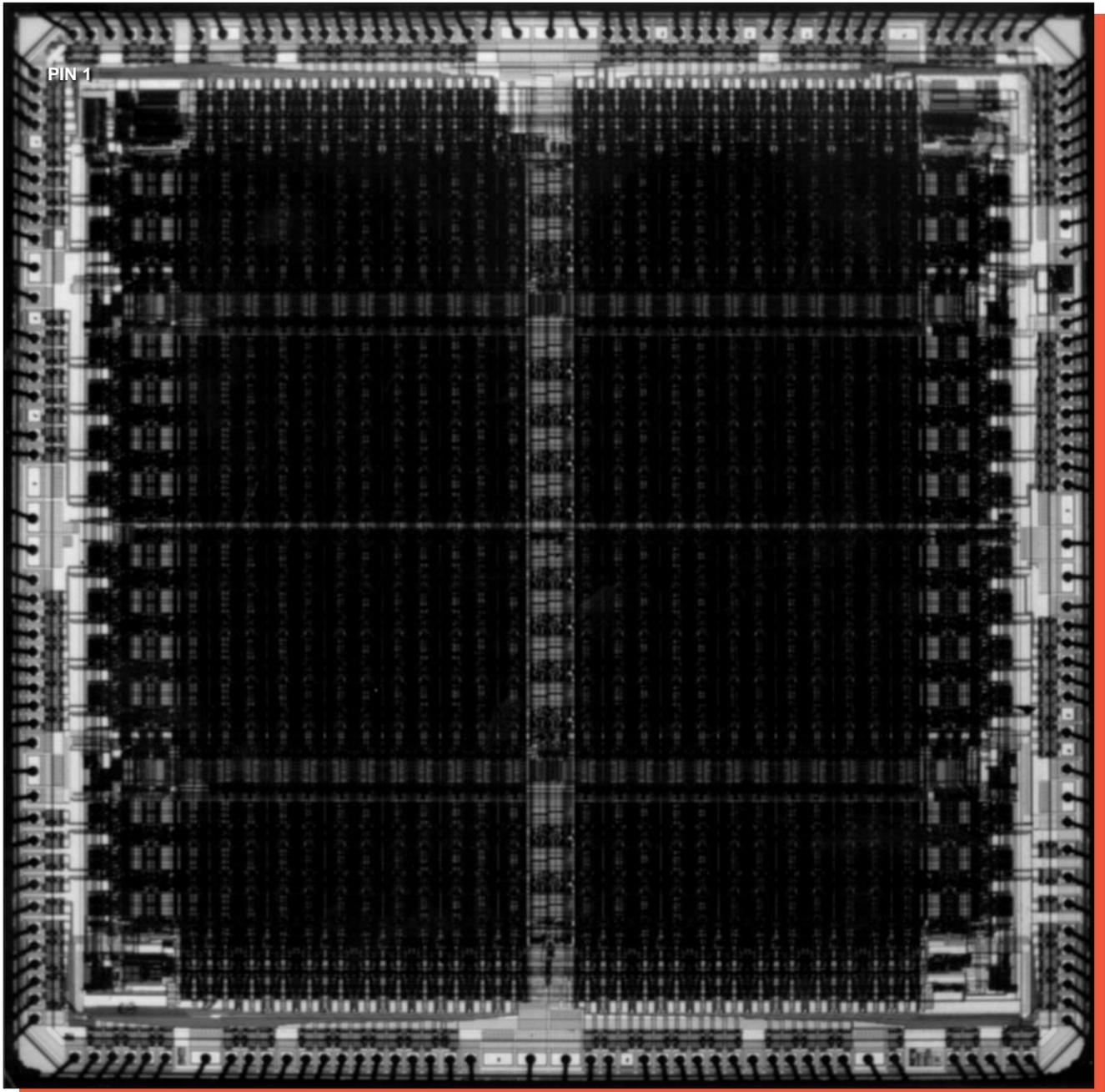


Figure 5. The ACTEL A1440 FPGA intact circuit die. Mag. 20x.



Mag. 500x



Mag. 400x

Figure 6. Markings from the die surface.

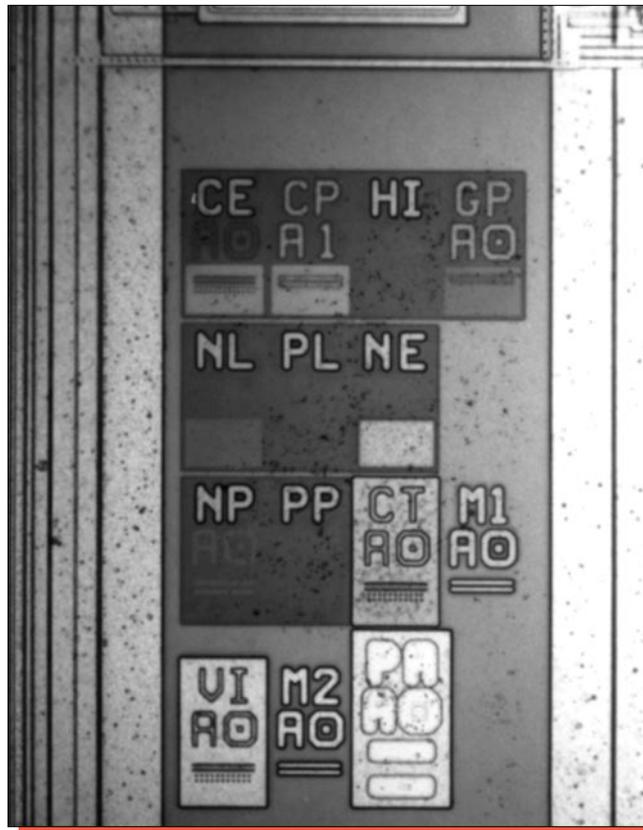
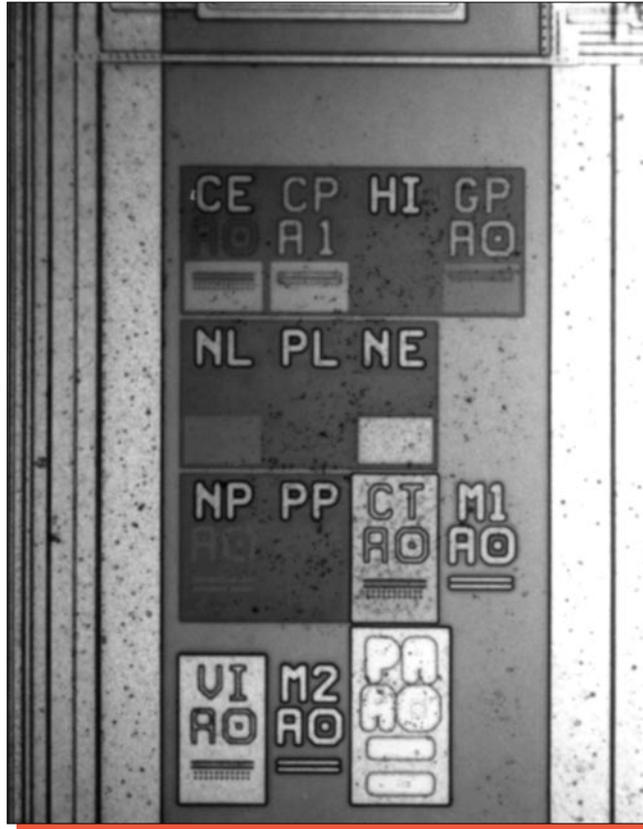
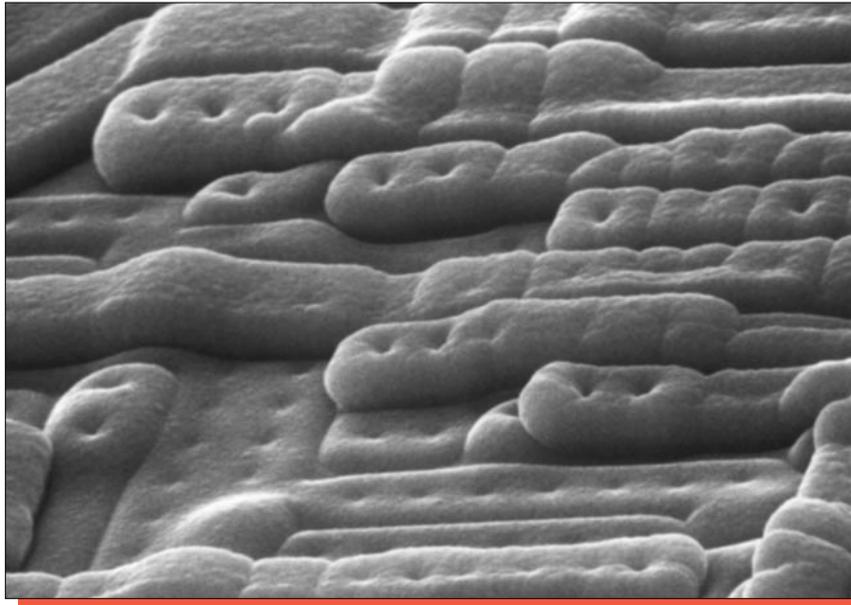
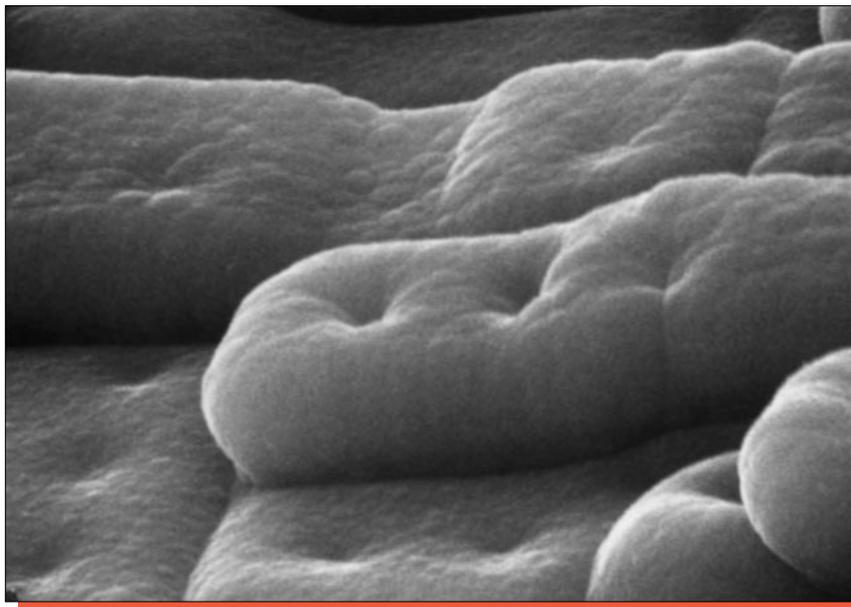


Figure 6a. Additional markings from the die surface. Mag. 320x.

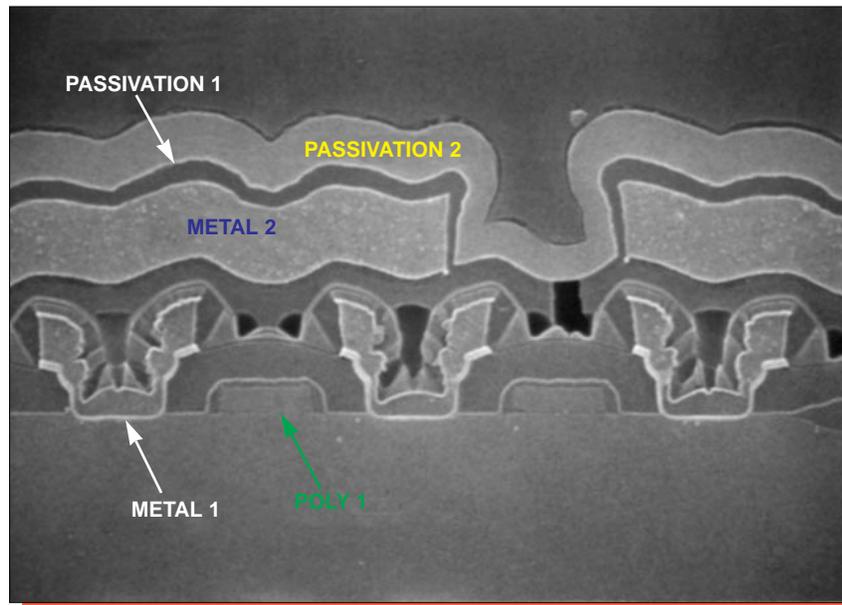


Mag. 3900x

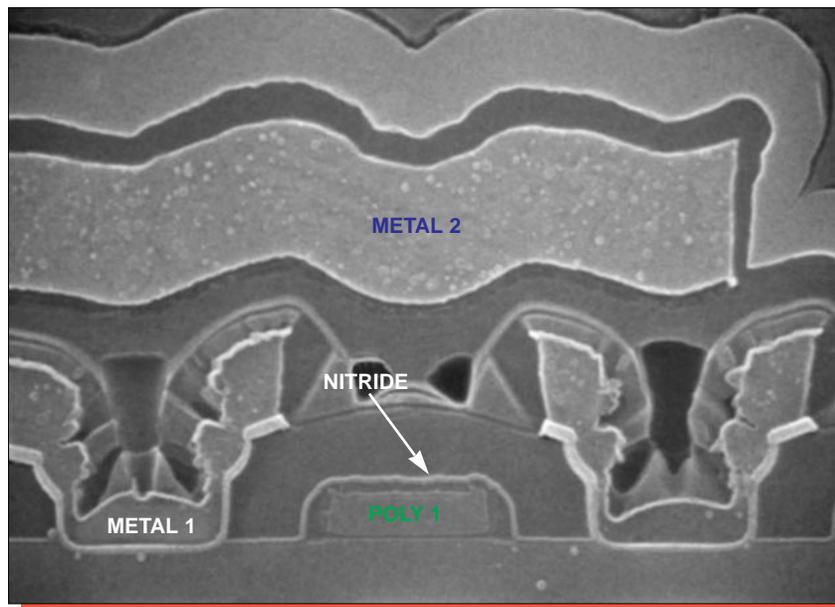


Mag. 11,000x

Figure 7. SEM views of overlay passivation coverage. 60°.

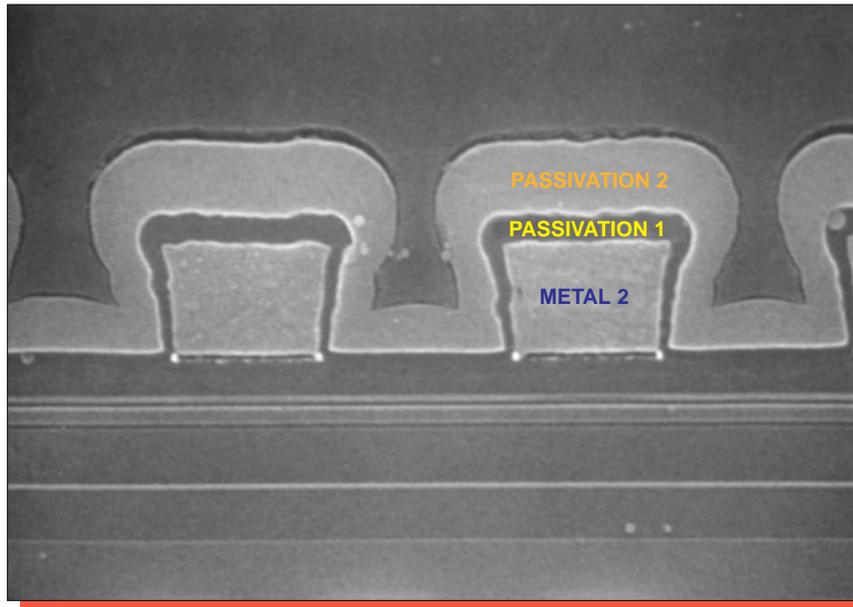


Mag. 10,000x

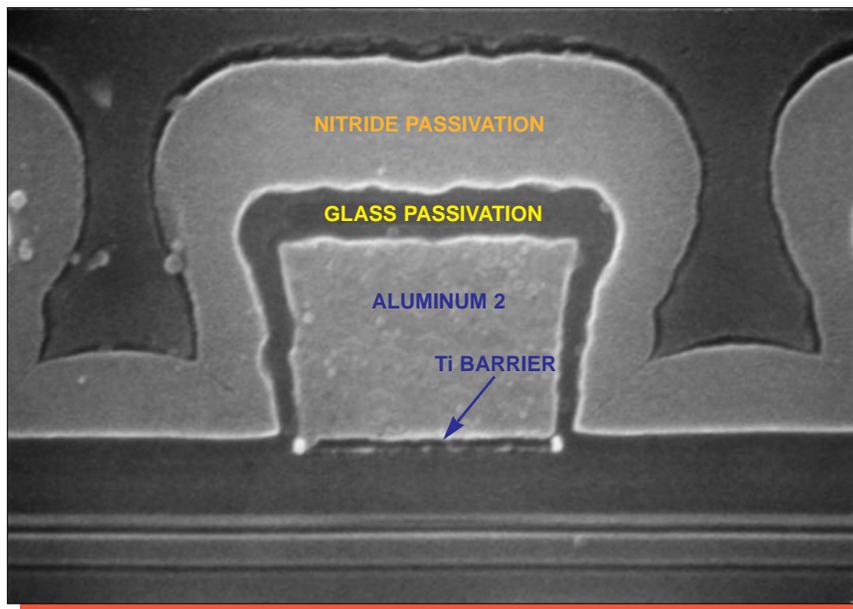


Mag. 17,500x

Figure 8. SEM section views of general device construction and contact/gate spacings.

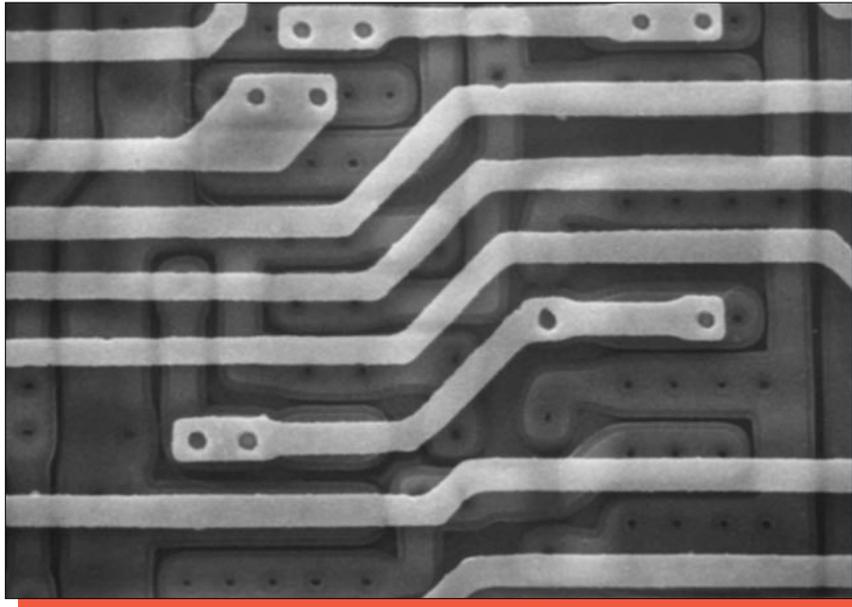


Mag. 15,000x

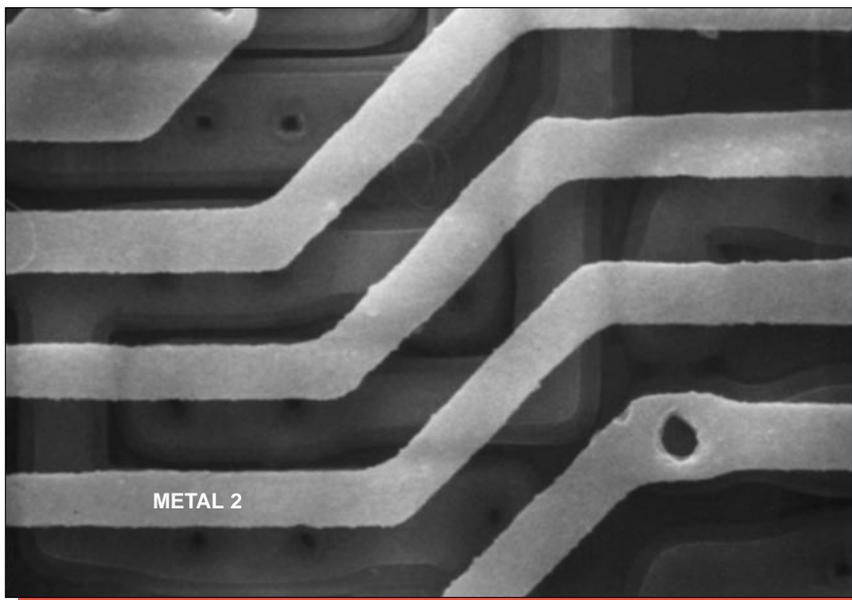


Mag. 26,000x

Figure 9. SEM section views of metal 2 line profiles.

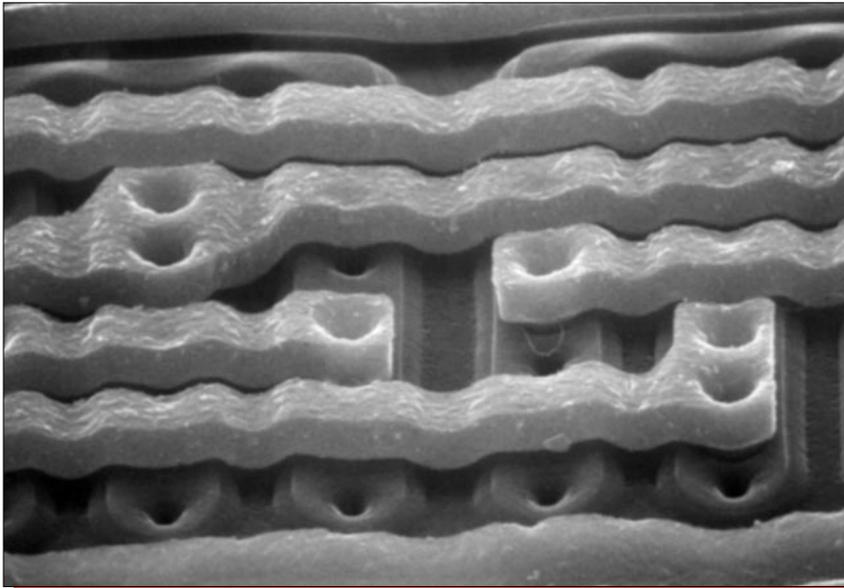


Mag. 2500x

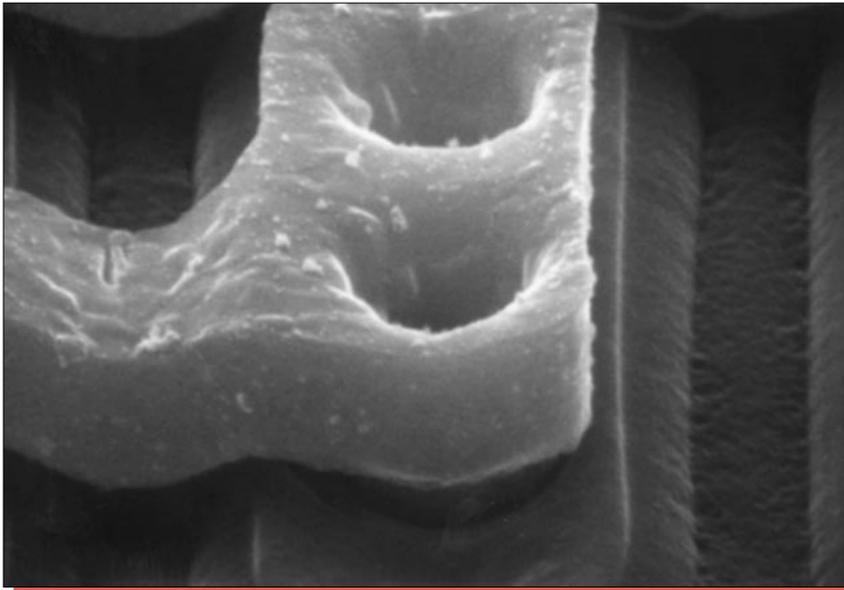


Mag. 5000x

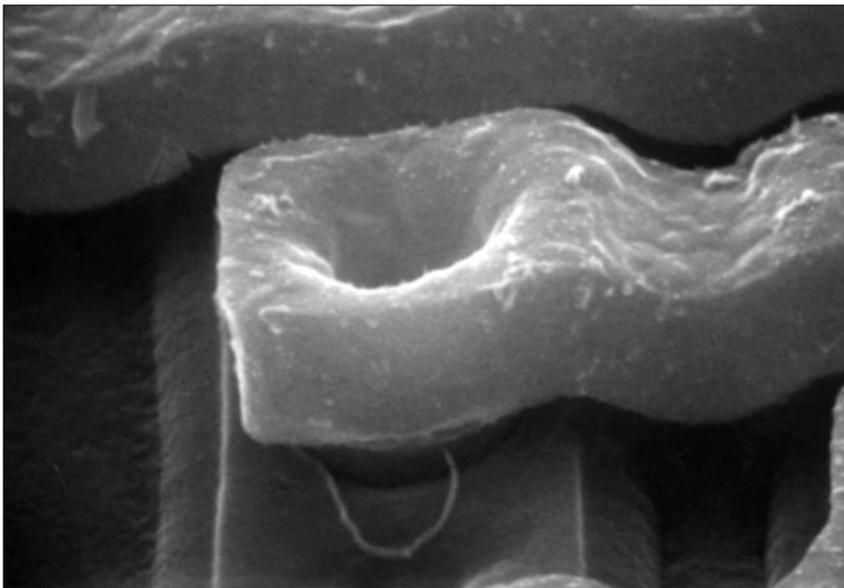
Figure 10. Topological SEM views of metal 2 patterning. 0°.



Mag. 5700x

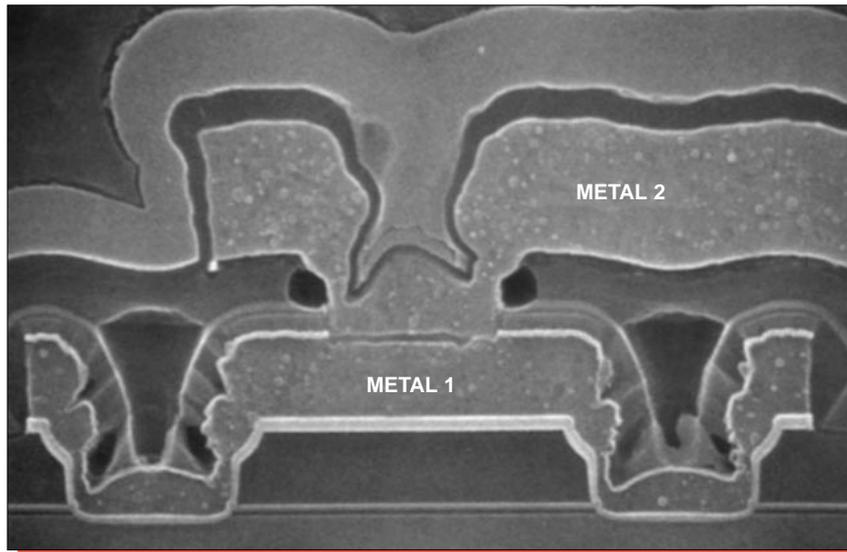


Mag. 20,000x

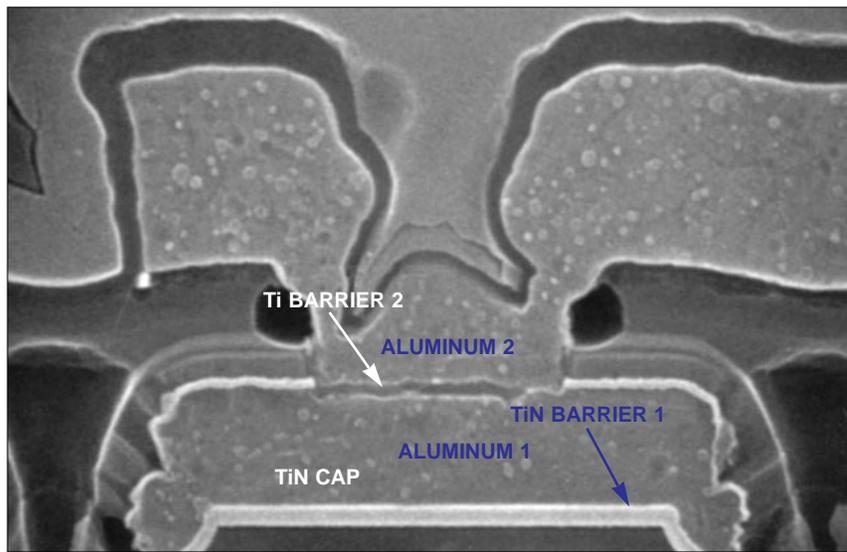


Mag. 20,000x

Figure 11. SEM views of metal 2 coverage.



Mag. 17,600x



Mag. 26,000x

Figure 12. SEM section views of a metal 2-to-metal 1 via.

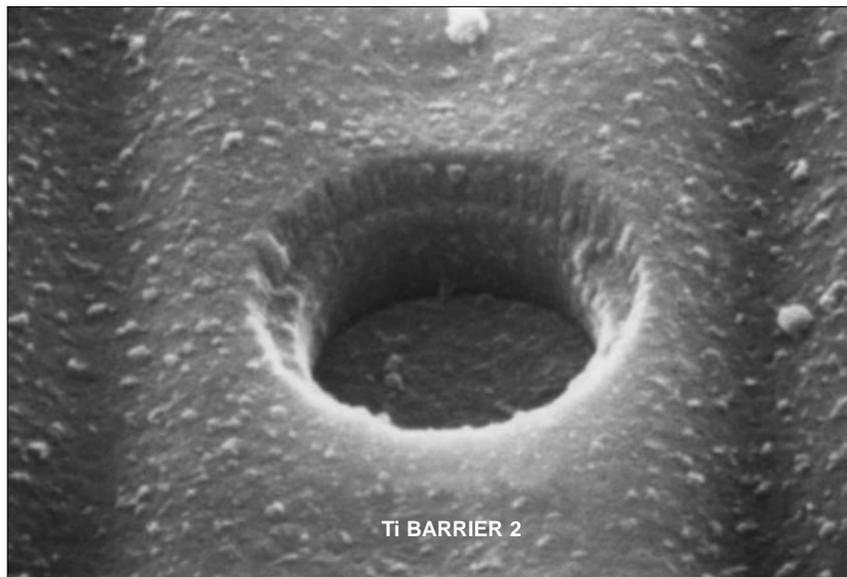
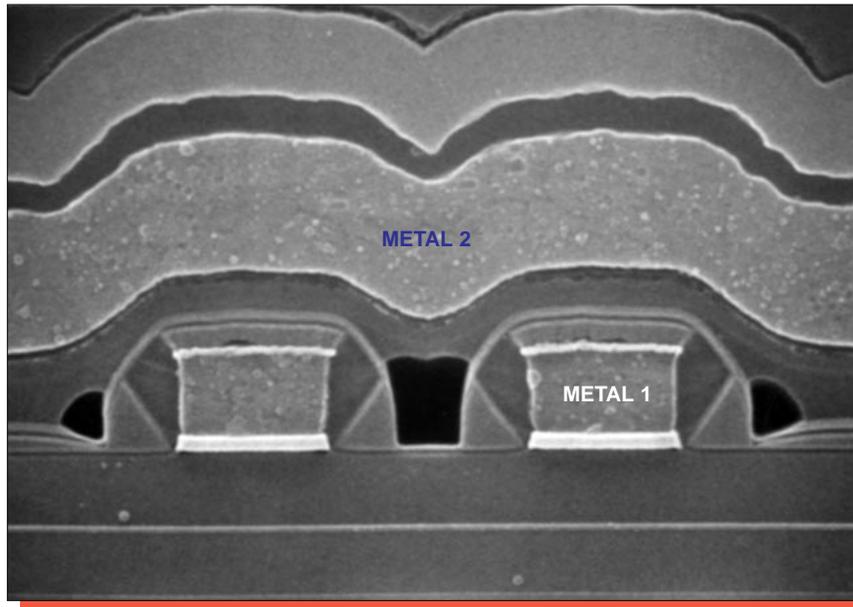
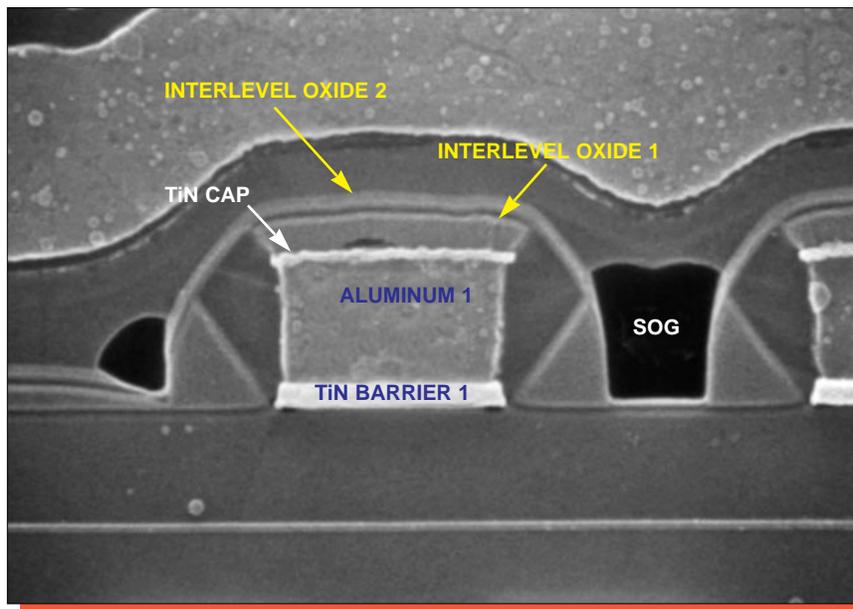


Figure 13. SEM view of metal 2 barrier following aluminum 2 removal. 45°.

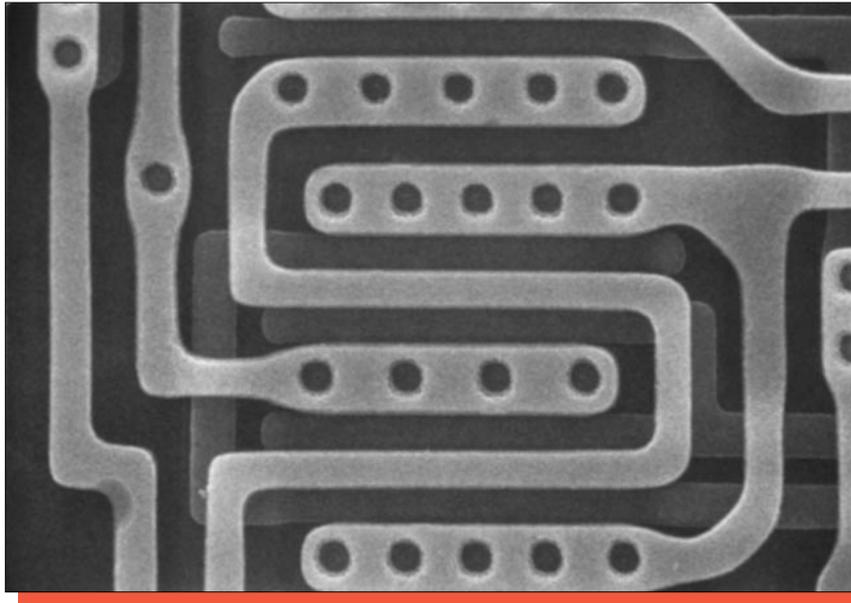


Mag. 18,000x

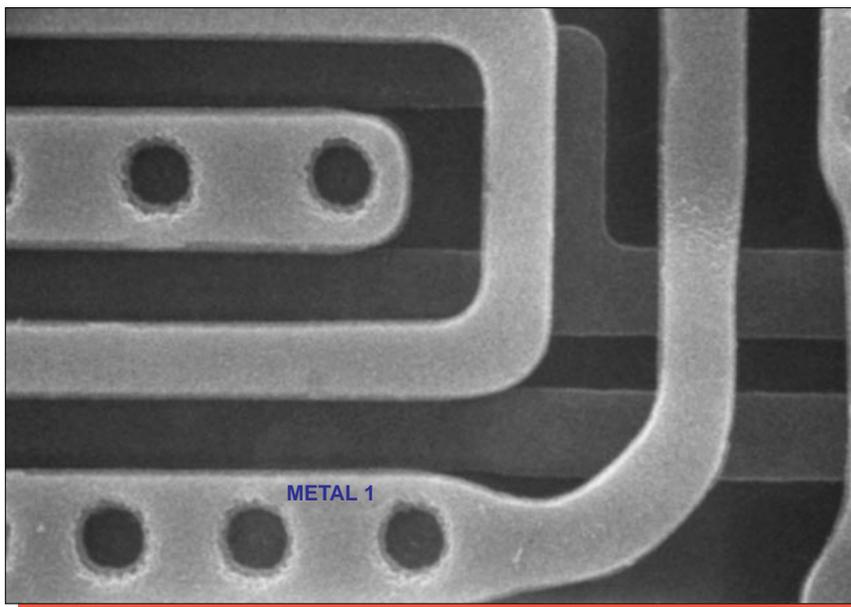


Mag. 27,000x

Figure 14. SEM section views of metal 1 line profiles.

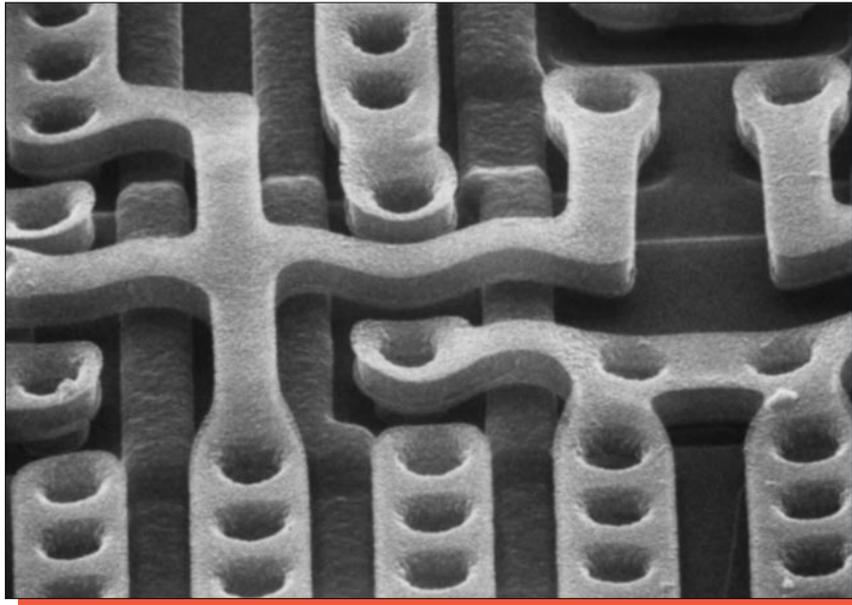


Mag. 4200x

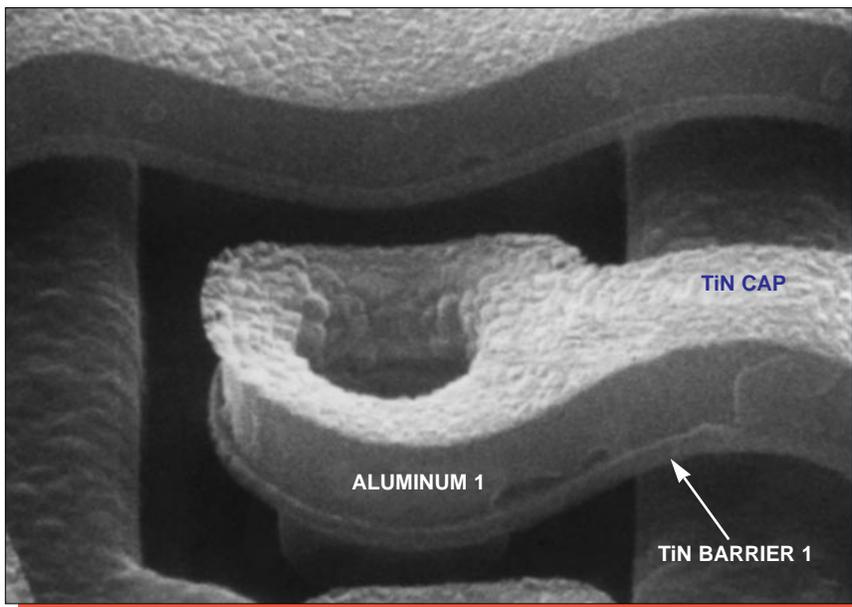


Mag. 8000x

Figure 15. Topological SEM views of metal 1 patterning. 0°.

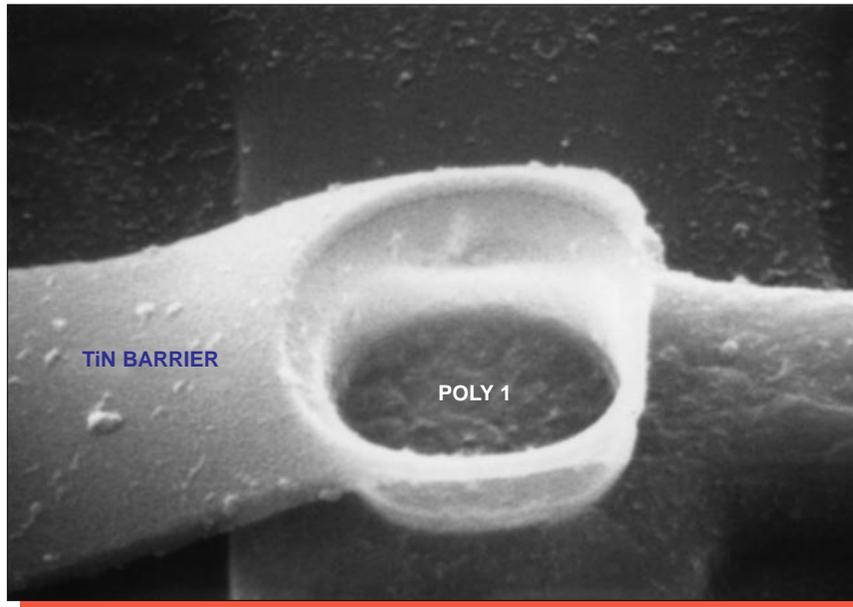


Mag. 6800x

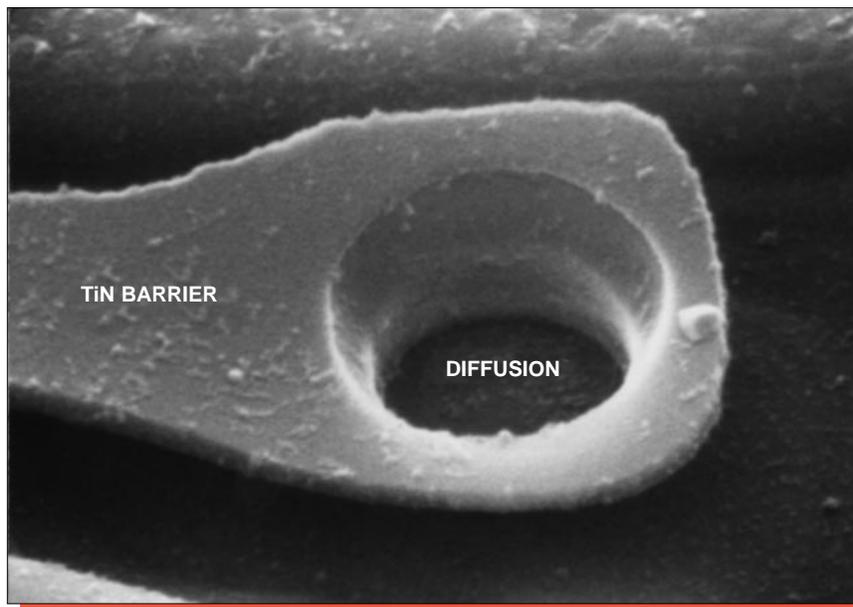


Mag. 22,000x

Figure 16. SEM views of metal 1 coverage. 60°.

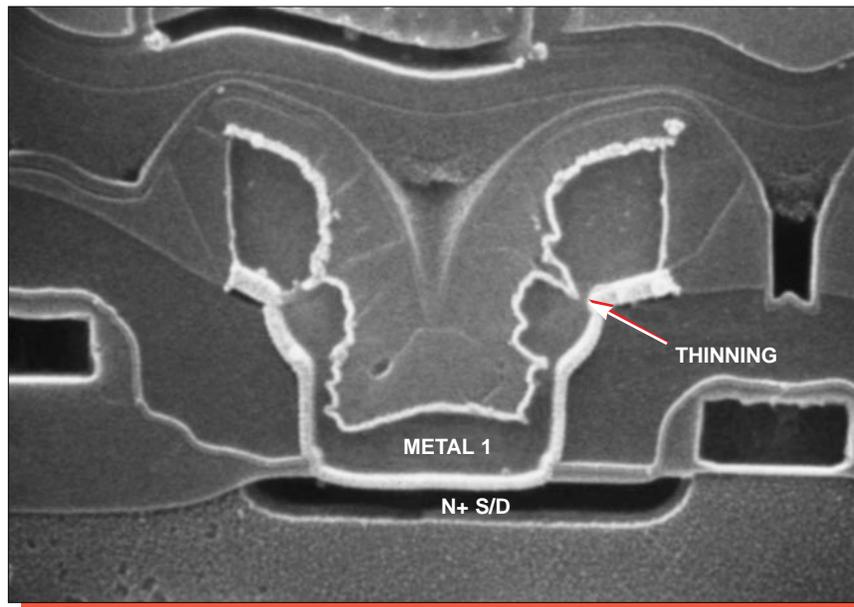


metal 1-to-poly 1

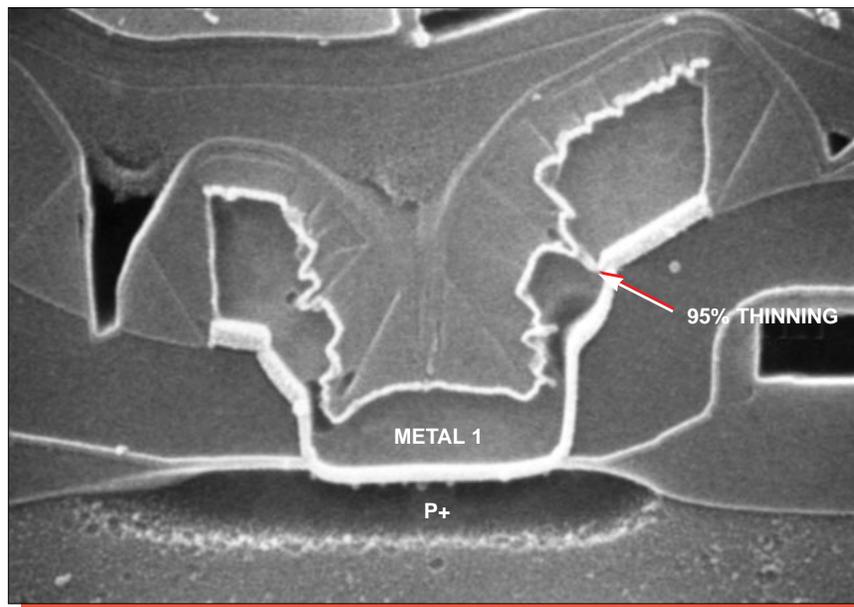


metal 1-to-diffusion

Figure 17. SEM views of metal 1 barrier following aluminum 1 removal. 45°.

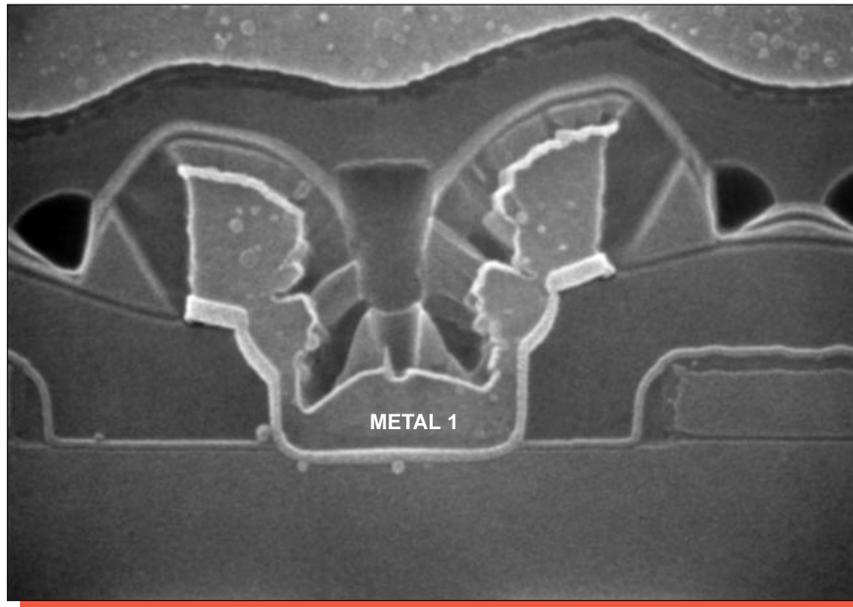


metal 1-to-N+

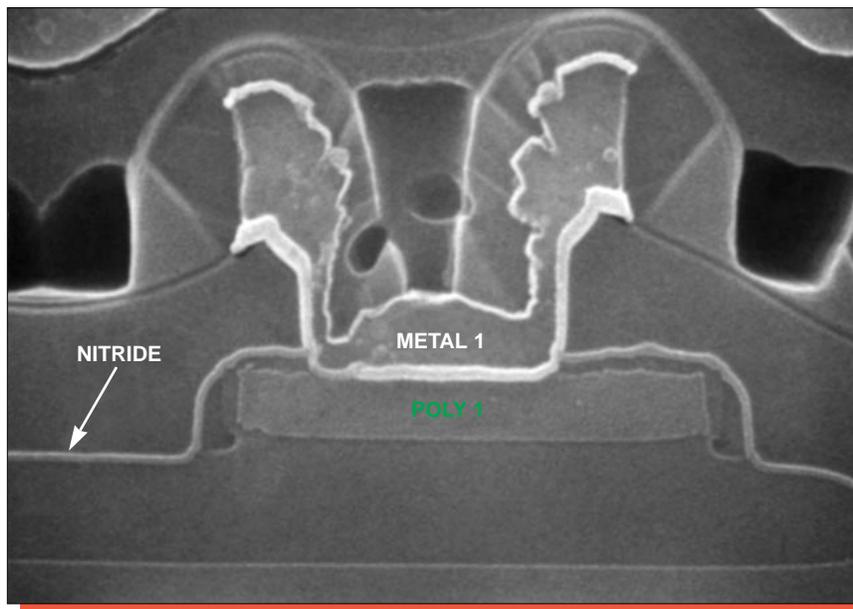


metal 1-to-P+

Figure 18. SEM section views of typical metal contacts. Silicon etch, Mag. 26,000x.

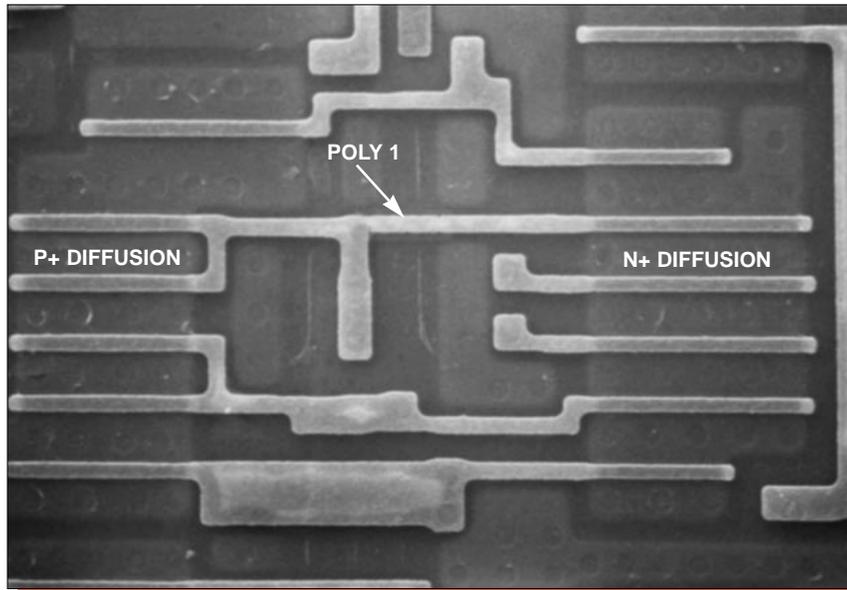


metal 1-to-diffusion

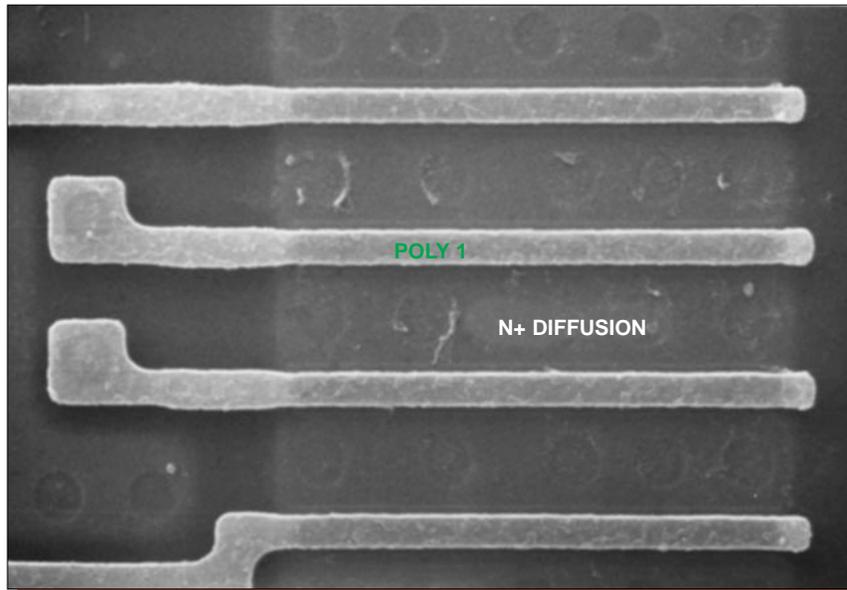


metal 1-to-poly 1

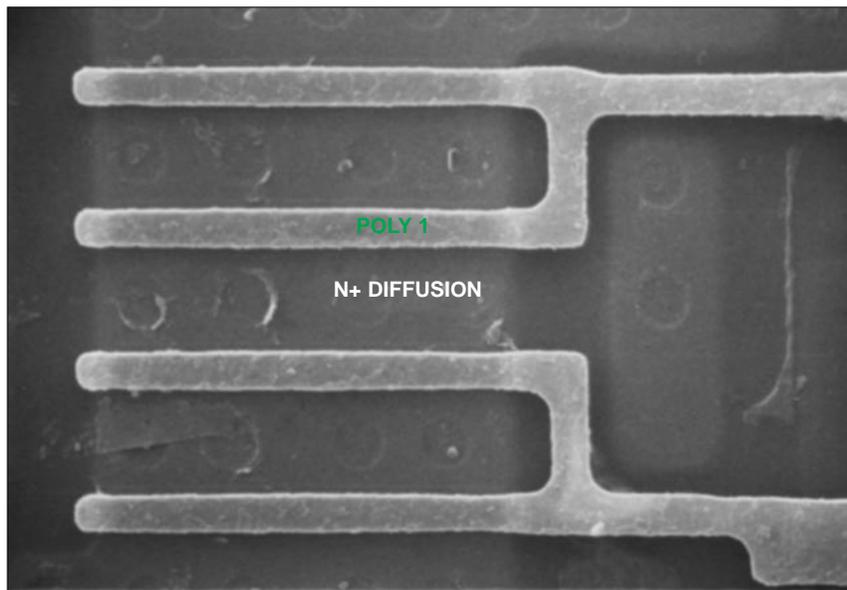
Figure 19. SEM section views of typical metal 1 contacts. Glass etch, Mag. 27,000x.



Mag. 2300x

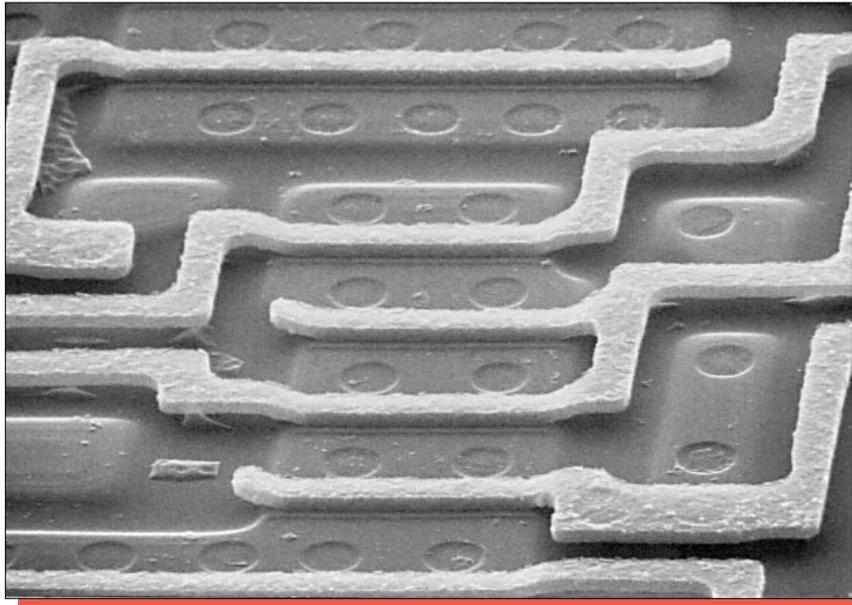


Mag. 5200x

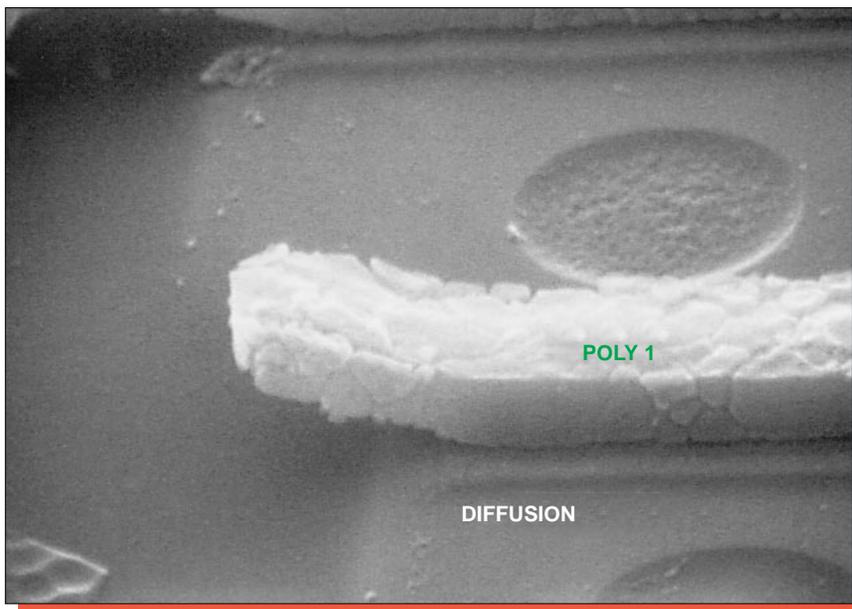


Mag. 5200x

Figure 20. Topological SEM views of poly 1 patterning. 0°.

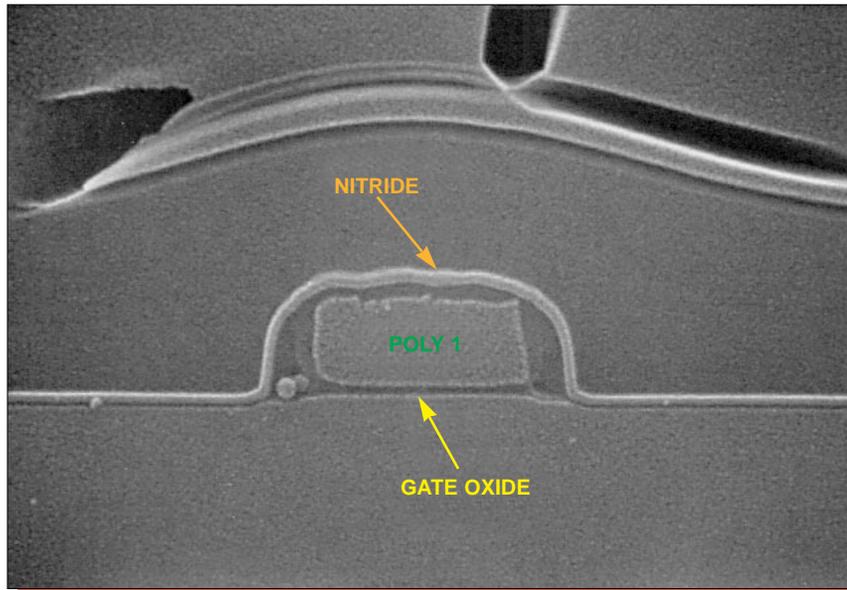


Mag. 5700x

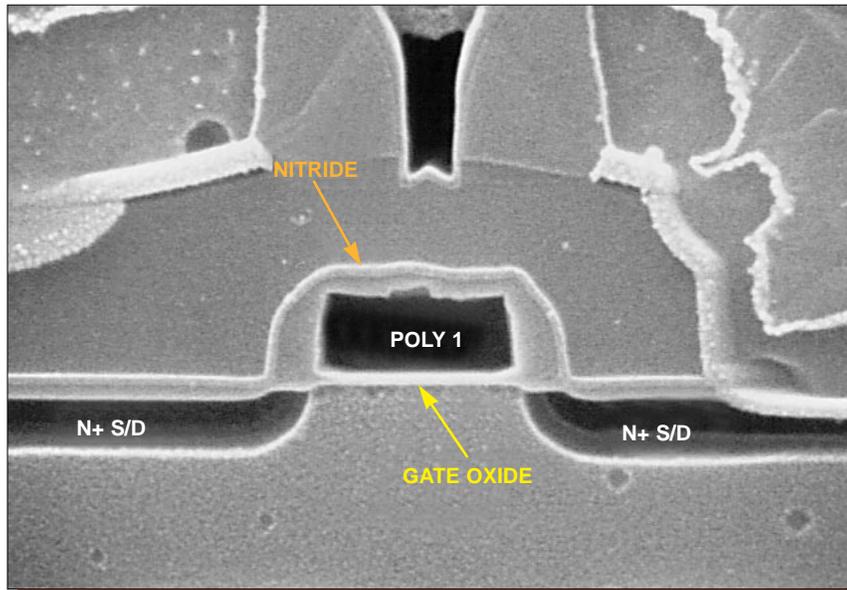


Mag. 30,000x

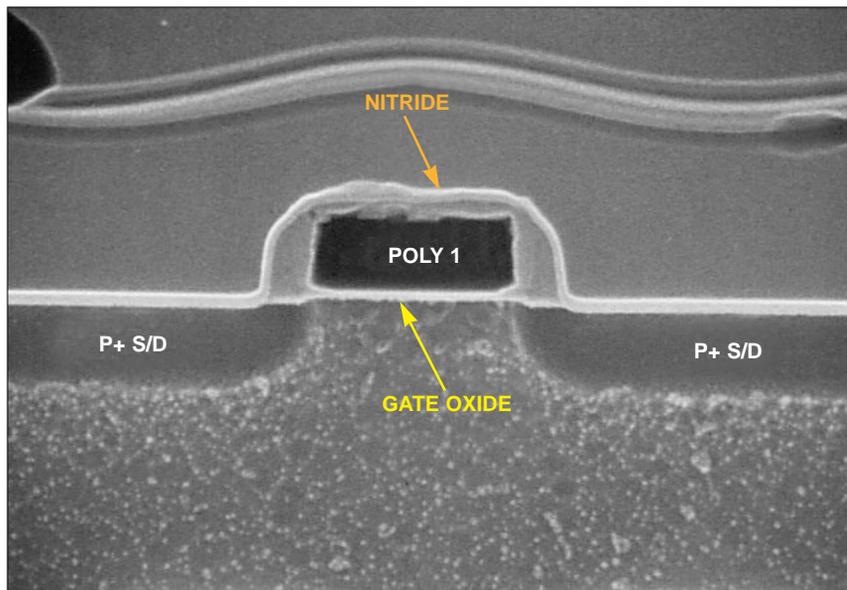
Figure 21. SEM views of poly 1 coverage. 60°.



glass etch,  
Mag. 35,000x



silicon etch,  
Mag. 32,000x



silicon etch,  
Mag. 32,000x

Figure 22. SEM section views of typical transistors.

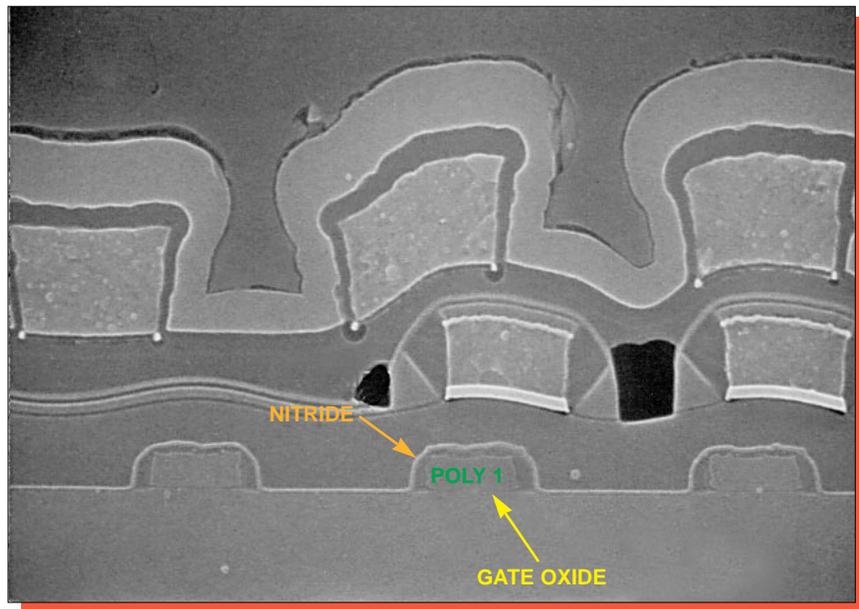


Figure 23. SEM section view illustrating minimum gate spacings. Mag. 13,500x.

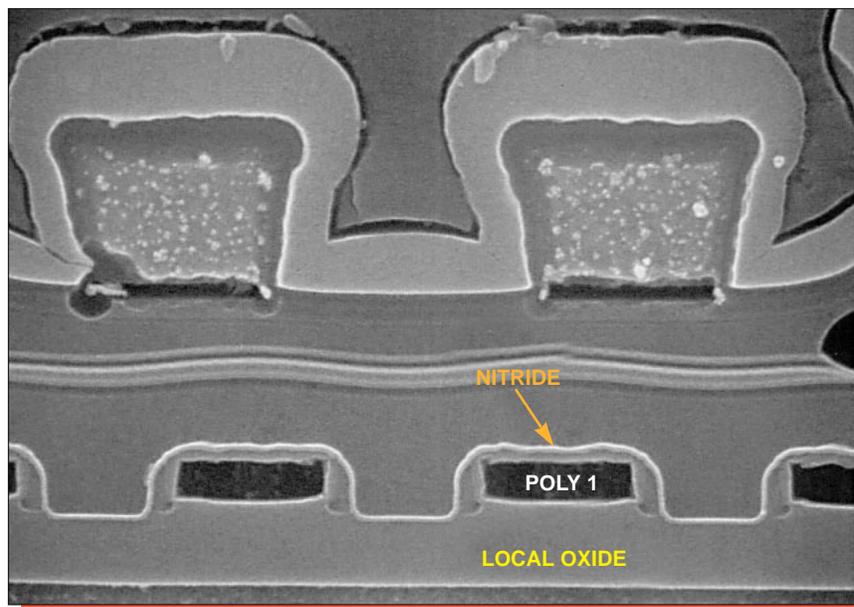
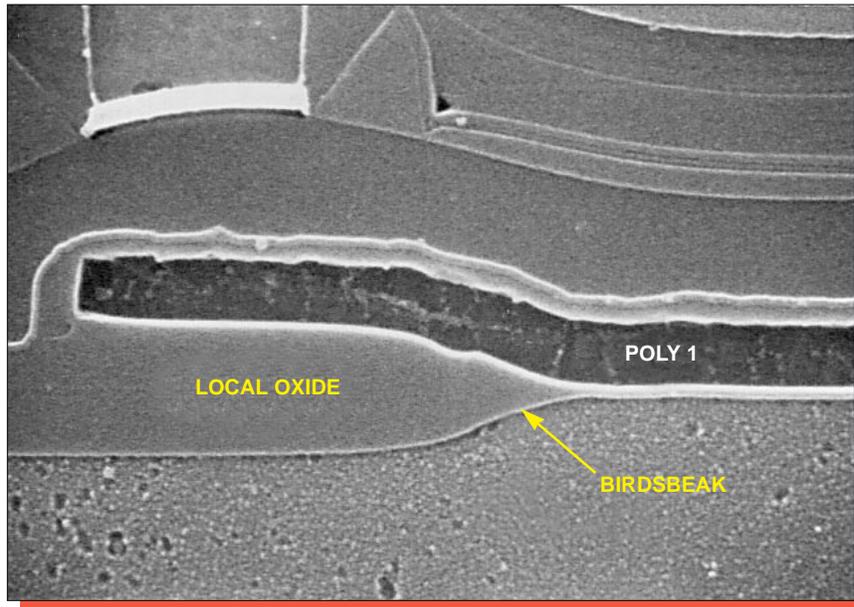
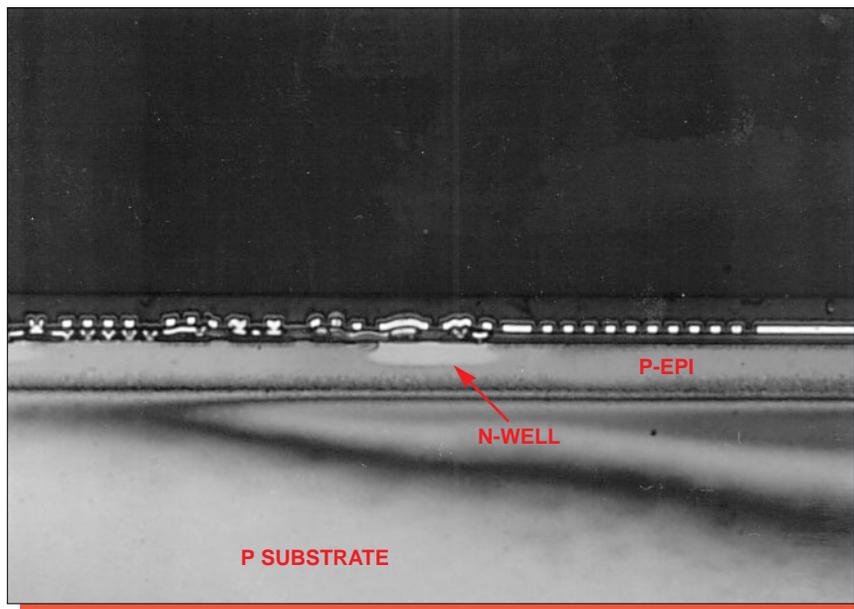


Figure 24. SEM section view illustrating minimum poly interconnect spacings. Mag. 17,500x.

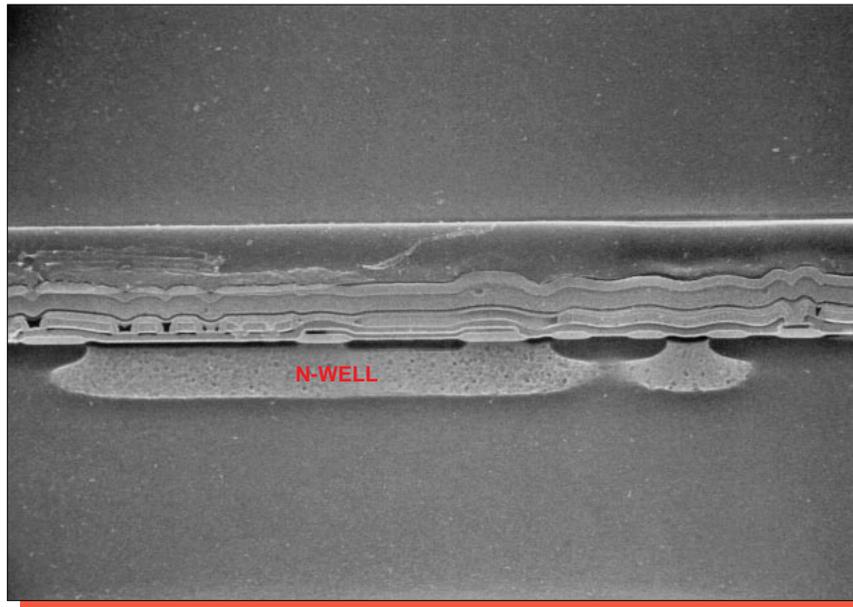


Mag. 26,000x

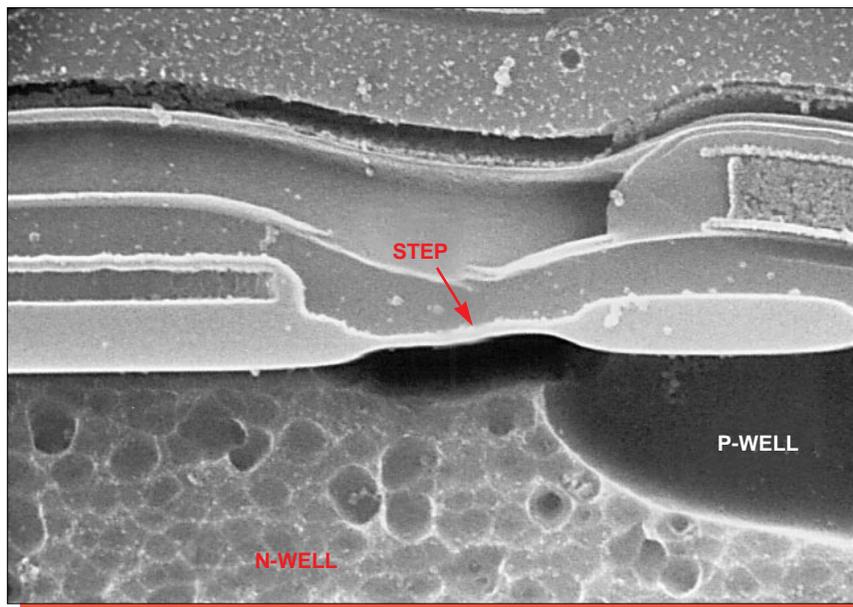


Mag. 800x

Figure 25. Section views of a local oxide birdsbeak and an N-well.

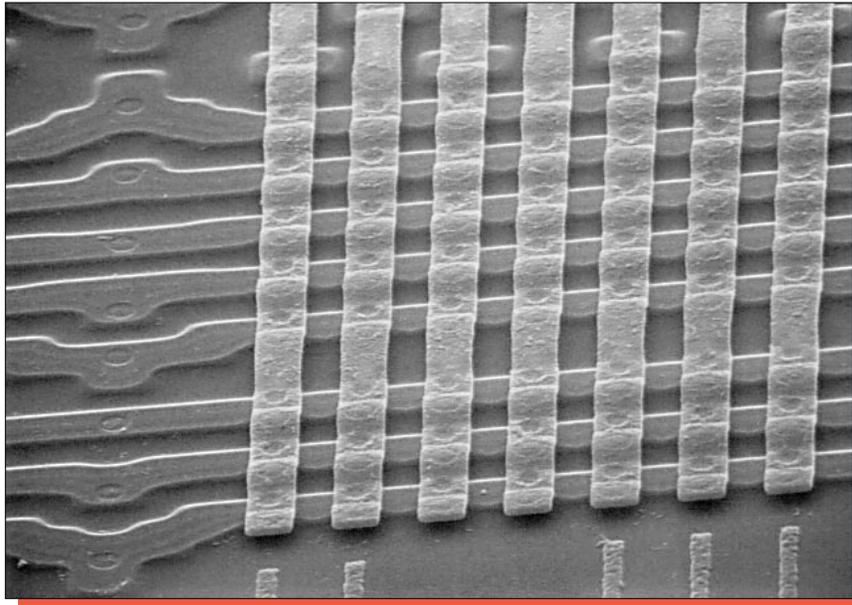


Mag. 1700x

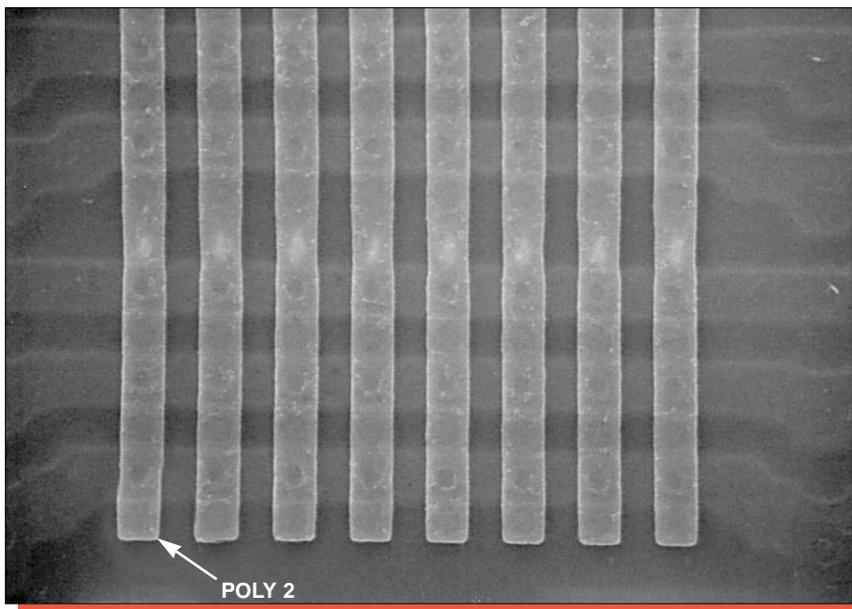


Mag. 13,500x

Figure 25a. SEM section views of the well structure.

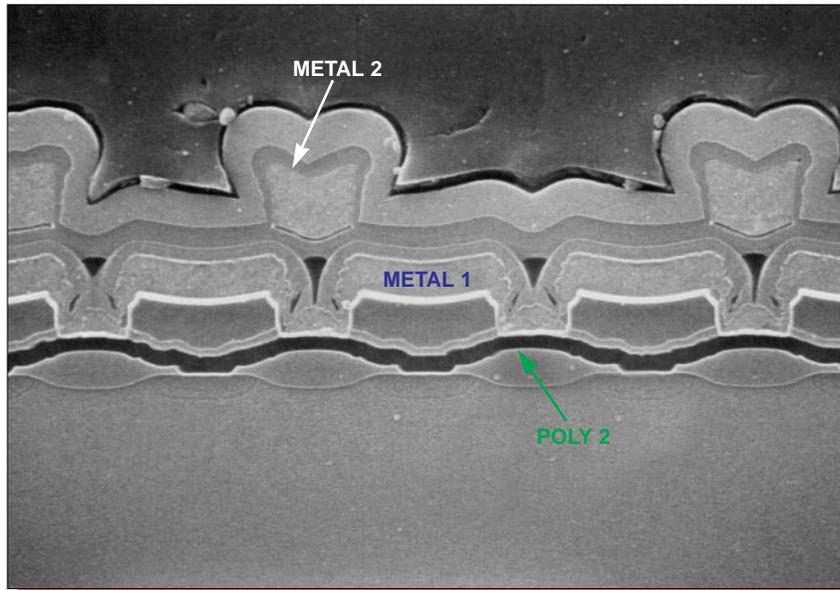


Mag. 3200x, 60°

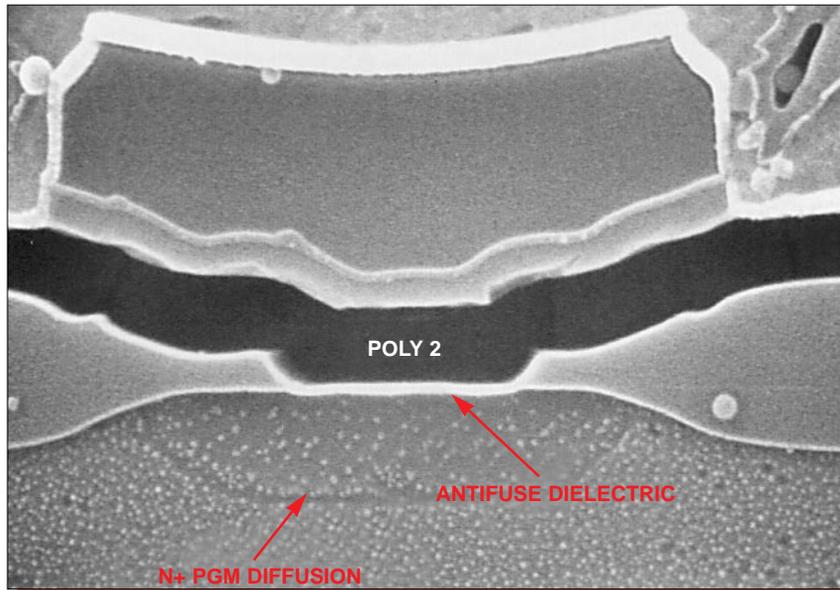


Mag. 3000x, 0°

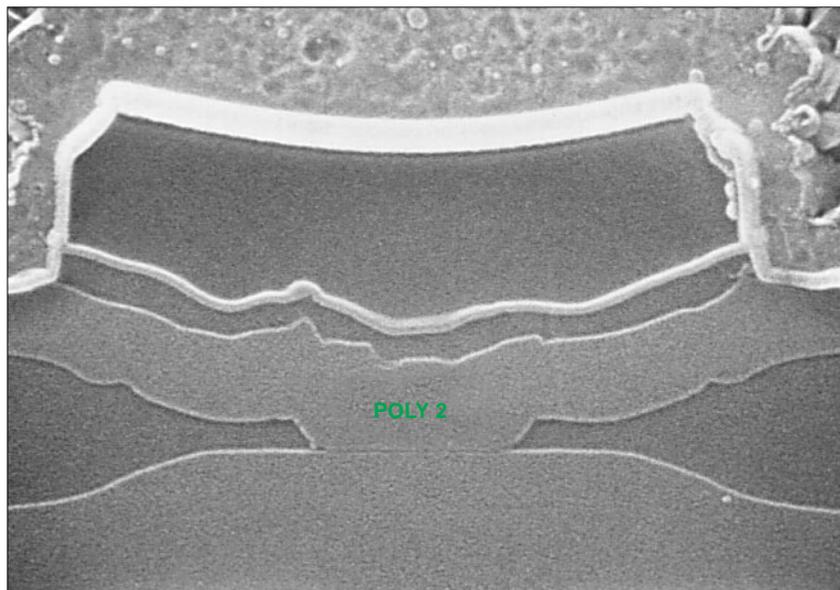
Figure 25b. SEM views of the antifuse structure.



silicon etch,  
Mag. 7000x

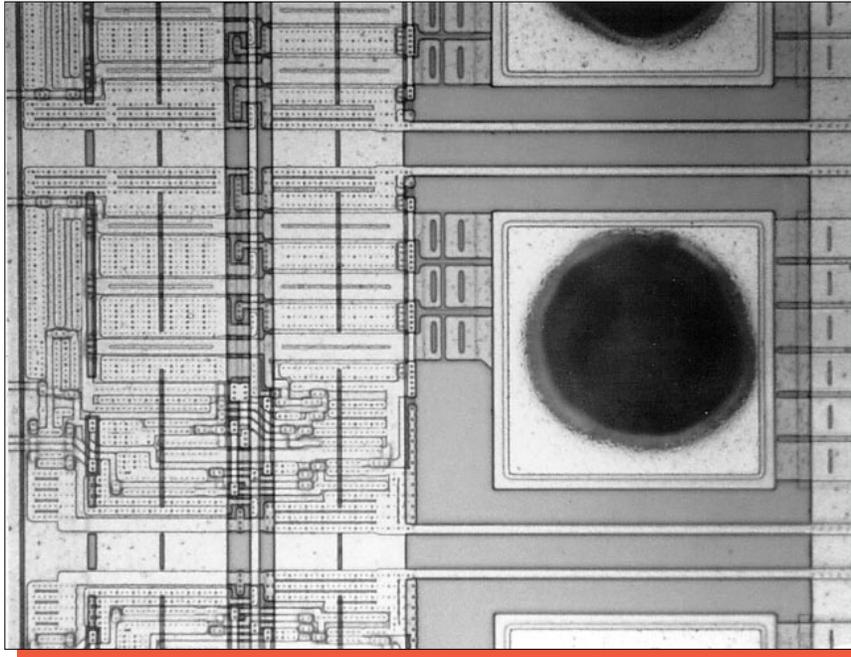


silicon etch,  
Mag. 32,000x

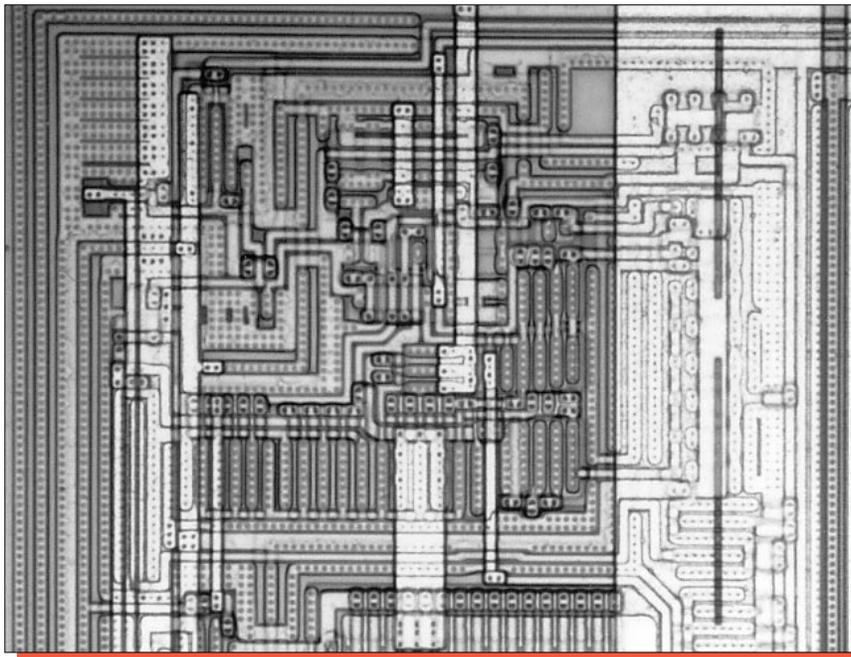


glass etch,  
Mag. 32,000x

Figure 25c. SEM section views of the antifuse structure.

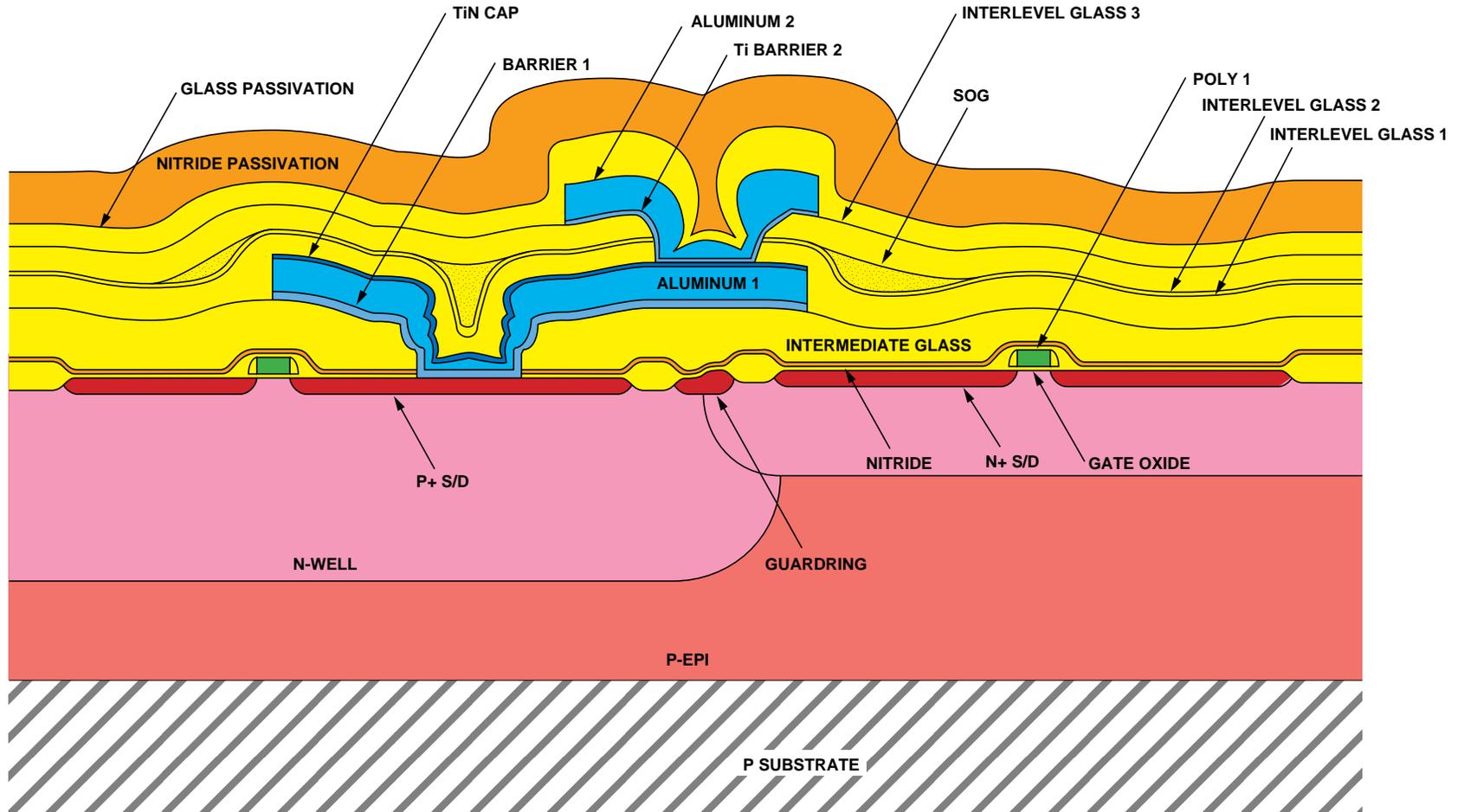


Mag. 320x



Mag. 500x

Figure 26. Optical views of input protection and typical device circuitry.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,  
 Red = Diffusion, and Gray = Substrate

Figure 27. Color cross section drawing illustrating device structure.