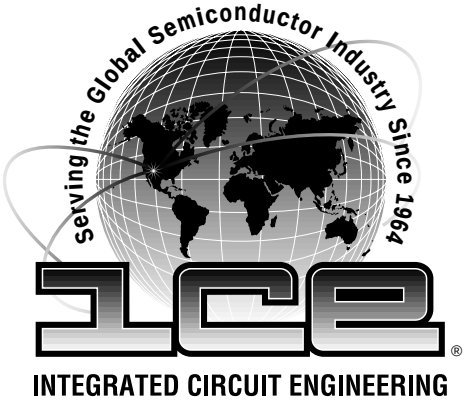
Construction Analysis

Xicor X28C010J-20
128K X 8 Bit EEPROM

Report Number: SCA 9504-401



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INTRODUCTION

This report describes a construction analysis of the Xicor X28C010J-20, 5V, Byte Alterable 128K x 8 Bit EEPROM. The devices were packaged in 32-pin Plastic Leaded Chip Carriers (PLCCs) date coded 9443. An analysis of the package is included.

MAJOR FINDINGS

Questionable Items:[1]

- Cracks through the metal 1 at the bottom perimeter of some contacts (Figures 22 and 29).

Special Features:

- Trench-oxide isolation CMOS twin-well process employing P-epi on a P-substrate.
- Molybdenum metallization with titanium-tungsten barrier for metal 1.

[1] *These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

TECHNOLOGY DESCRIPTION

Assembly:

- Devices were encapsulated in 32-pin Plastic Leaded Chip Carriers (PLCCs) with J-leads.
- Copper (Cu) leadframe internally spot plated with silver (Ag).
- External pins (J-lead) were tinned with tin-lead (SnPb) solder.
- Lead-locking provisions (anchors and some holes) at all pins and dimpled header.
- Thermosonic ball bonding using 1.3 mil O.D. gold wire.
- Pins 1 and 30 were not connected, Vcc and GND were double wire bonded.
- Sawn dicing (full-depth).
- Silver-filled polyimide die attach.

Die Process and Design:

- Devices utilized a trench-oxide isolation CMOS twin-well with P-epi process on a P-substrate.
- Passivation consisted of a layer of phosphorus-doped glass.
- Two layers of metal. Metal 2 consisted of aluminum doped with silicon (no copper detected), no cap or barrier metals were employed. Metal 1 consisted of molybdenum with a titanium-tungsten barrier, no cap metal was employed.
- Two layers of silicon-dioxide were used under metal 2 (interlevel oxide). Interlevel oxide 1 appeared to be an SOG and have been subjected to an etch back process.

TECHNOLOGY DESCRIPTION (continued)

- A layer of BPSG which was reflowed prior to contact cuts was used under metal 1 (intermediate oxide).

- Two layers of polysilicon (no polycide). Poly 2 was only used in the memory cell, poly 1 was used to form all gates on the die and in the memory cell. Direct poly-to-diffusion (buried) contacts were not used. Definition was by a dry etch of normal quality.

- The EEPROM memory cell consisted of metal 2 "piggyback" word lines, metal 1 bit lines, poly 2 word lines/select gates and poly 1 floating gates/program lines. Programming is achieved through a ultra-thin (tunnel) oxide inter-poly dielectric.

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. There was no indication that an LDD process was used.

ANALYSIS RESULTS I

Assembly: **Figures 1 - 9**

Questionable Items: None

General Items:

- Devices were encapsulated in 32-pin Plastic Leaded Chip Carriers (PLCCs) with J-leads.

- Overall package quality: Normal. Internal spot plating of leadframe was silver of good quality and well centered. External pins were tin-lead (SnPb) solder tinned and no cracks or voids were deserved. Small gaps were noted at lead exits; however, they did not extend far into the package. No internal plating was exposed so no problems are expected.

- Lead-locking provisions (anchors and some holes) at all pins. The die paddle was dimpled for better package strength.

- Wirebonding: Thermosonic ball method using 1.3 mil O.D. gold wire. Some incomplete intermetallic was noted but no bond lifts occurred and bond pull strengths were good (see page 10). Height of bonding wire arcs and vertical header offset resulted in good clearance between die edge and bonding wires.

- Pins 1 and 30 were not connected, VCC and GND pins were double wire bonded.

- Die attach: Silver-filled polyimide of good quality, a small void at the corner of the die was noted but should not be a reliability problem (Figure 6).

- Die dicing: Die separation was by sawing (full depth) with normal quality workmanship.

ANALYSIS RESULTS II

Die Process: **Figures 10 - 31**

Questionable Items:[1]

- Cracks in the metal 1 at the bottom perimeter of some contacts (Figures 22 and 29).

Special Features:

- Trench-oxide isolation, CMOS twin-well process employing a P-epi on a P-substrate.

- Metal 1 consisted of molybdenum metallization with a titanium-tungsten barrier.

General Items:

- Fabrication process: Trench-oxide isolation, twin-well process CMOS with P-epi on a P-substrate.

- Process implementation: Die layout was clean and efficient. Alignment was normal (minor metal 1 misalignment) and no damage or contamination was found.

- Overlay passivation: A layer of phosphorus-doped glass was used. Overlay integrity test indicated defect-free passivation. Edge seal quality was good.

- Metallization: Two layers of metal. Metal 2 consisted of aluminum doped with silicon (no copper detected), and no cap or barrier metals. Metal 1 consisted of molybdenum with a titanium-tungsten barrier, no cap metal was employed. Note: the metal 1 molybdenum was etched during cross section delineation using a normal silicon etch. These artifacts thus need to be disregarded.

[1]*These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.*

ANALYSIS RESULTS II (continued)

- Metal patterning: Dry etch of normal quality.

- Metal defects: No notching or neckdown was noted in any of the metal layers. Contacts were not completely surrounded (but were completely covered) by metal 1 due to slight misalignment (See Figures 20 and 21). Virtually no silicon nodules were noted following metal 2 removal. .

- Metal step coverage: Maximum metal 2 thinning was up to 80 percent at vias (Figure 18). Maximum metal 1 thinning was up to 70 percent at contacts (Figures 22 and 29). MIL-STD-883D states up to 70 percent thinning is allowable for contacts of this size (1.0 micron). **In addition to the 70 percent thinning, cracks were present at the bottom perimeter of some contacts (Figures 22 and 29).** This appears to be a result of over-etched contact cuts.

- Interlevel glass: Two layers of silicon-dioxide were used under metal 2. Interlevel 1 appeared to be a spin-on glass (SOG) possibly subjected to an etchback process. No problems were found.

- Intermediate glass: A layer of BPSG on grown/densified oxide was used under metal 1. The BPSG was reflowed prior to contact cuts. No problems were found.

- Contact defects: Via cuts appeared defined by a single-step sloped process. Contacts were overetched resulting in the cracks around the perimeter of some.

- Two layers of polysilicon (no polycide) were employed. Poly 2 was used exclusively in the memory cell and poly 1 was used to form all gates on the die and in the memory cells. Direct poly-to-diffusion (buried) contacts were not used. Poly to poly contact appears to occur in very small areas (edges) between poly 2 and poly 1 in the array. Definition was by dry-etch of normal quality.

- The EEPROM memory cell consisted of metal 2 "piggyback" word lines, metal 1 bit lines, poly 2 word lines/select gates and poly 1 floating gates/program lines. Programming is achieved through an ultra-thin (tunnel) oxide, inter-poly dielectric.

ANALYSIS RESULTS II (continued)

- Standard implanted N+ and P+ diffusions formed the sources/drains of the CMOS transistors. There was on indication that an LDD process was used.

- Trench oxide isolation was used. It consisted of very narrow grooves partly filled with a nitride layer.

Special items:

- ESD: ESD tests were performed on sample 1 revealed that no significant leakage occurred after pulses of ±4000V. Sample 2 pin 5 failed at +1000V all other pins passed ±3000V (see appendix).

- Latch-up: Latch-up tests were performed on samples 3 and 4 per the JEDEC Standard No. 17. Pins were tested from -200 ma to +200 ma and revealed that no pin latched up on either sample (see appendix).

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

ESD test

Latch-up test

X-ray

Package section and EDX

Decapsulate

Internal optical inspection

SEM of assembly features and passivation

Wirepull test

Passivation integrity test

Passivation removal

SEM inspection of metal 2

Metal 2 removal and inspect vias

Delayer to metal 1 and inspect

Delayer to silicon and inspect poly/die surface

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Normal-to-Poor

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Die attach quality	N
Wire spacing	G
Wirebond placement	G
Wirebond quality	N
Dicing quality	G
Wirebond method	Thermosonic ball bonds using 1.3 mil O.D. gold wire.
Die attach method	Silver-filled polyimide
Dicing method	Sawn (full depth)
Die surface integrity:	
Tool marks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	N
General workmanship	N
Passivation integrity	G
Metal definition	N
Metal integrity*	P
Metal registration	N
Contact coverage	N
Contact registration	N

**Cracks at contacts.*

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

XICOR X28C010J-20 V9443 ES	TAIWAN 39C 43BL33719I

WIREBOND STRENGTH

Wire material:	1.3 mil O.D. gold
Die pad material:	aluminum
Material at package land:	silver
Sample #	**1**
# of wires tested:	26
Bond lifts:	0
Force to break - high:	13.0g
- low:	10.0g
- avg.:	12.3g
- std. dev.:	0.7

PACKAGE MATERIAL ANALYSIS (EDX)

Leadframe:	Copper (Cu)
Internal plating:	Silver (Ag)
External plating:	Tin-lead (SnPb) solder
Die attach:	Silver (Ag)-filled polyimide

DIE MATERIAL ANALYSIS

Overlay passivation:	Phosphorus-doped glass (4.0 wt. percent).
Metallization 2:*	Aluminum (Al) doped with silicon (Si), no copper (Cu) detected.
Metallization 1:	Molybdenum (Mo).
barrier:	Titanium-tungsten (TiW).
Intermediate dielectric:	Borophosphosilicate glass containing (BPSG) 3.8 wt. percent boron and 3.5 wt. percent phosphorus.

**There is no know method for determining the exact amount of silicon or copper in the aluminum of a finished die.*

HORIZONTAL DIMENSIONS

Die size:	5.7 x 8.9 mm (225 x 350 mils)
Die area:	51 mm^2 (78,750 $mils^2$)
Min pad size:	0.16 x 0.16 mm (6.3 x 6.3 mils)
Min pad window:	0.14 x 0.14 mm (5.3 x 5.3 mils)
Min pad space:	0.1 mm (3.9 mils)
Min pad-to-metal:	0.03 mm (1.2 mil)
Min metal 2 width:	2.5 microns
Min metal 2 space:	1.7 micron
Min metal 1 width:	1.3 micron
Min metal 1 space:	1.5 micron
Min via:	1.7 micron
Min contact:	1.0 micron (round)
Min gate length* - (N-channel):	1.3 micron
- (P-channel):	1.5 micron
Min poly 2 width:	2.1 microns
Min poly 2 space:	0.5 micron
Min poly 1 width:	1.3 micron
Min poly 1 space:	1.0 micron
Cell pitch:	2.6 x 8.1 microns
Cell size:	21 $microns^2$ (0.013 mil^2)

* *Physical gate length*

VERTICAL DIMENSIONS

Die thickness:	0.7 mm (27 mils)

Layers:

Passivation :	1.1 micron
Metal 2:	1.2 micron
Interlevel glass 2:	0.7 micron
Interlevel glass 1:	0.3 micron
Metal 1:	
molybdenum:	0.45 micron
barrier:	0.2 micron
Intermediate glass :	0.6 micron
Poly 2:	0.2 micron
Poly 1 :	0.2 micron
Oxide over N+ diffusion:	0.15 micron
Oxide over P+ diffusion:	0.04 micron (approx.)
Trench isolation:	1.2 micron
Trench oxide:	0.5 micron
N+ diffusion:	0.2 micron
P+ diffusion:	0.4 micron
N-well	4.0 microns
P-well	3.5 microns (approx.)
Epi:	11 microns

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bottom

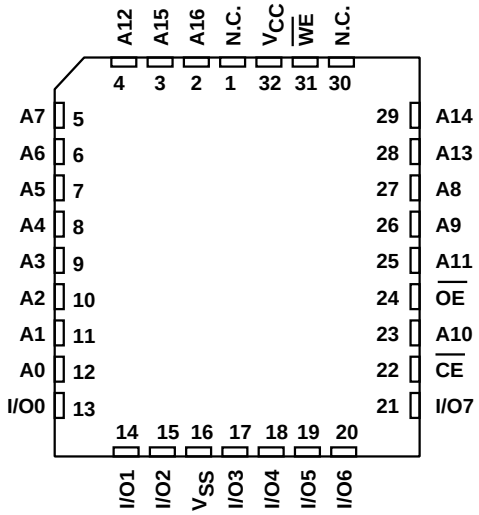
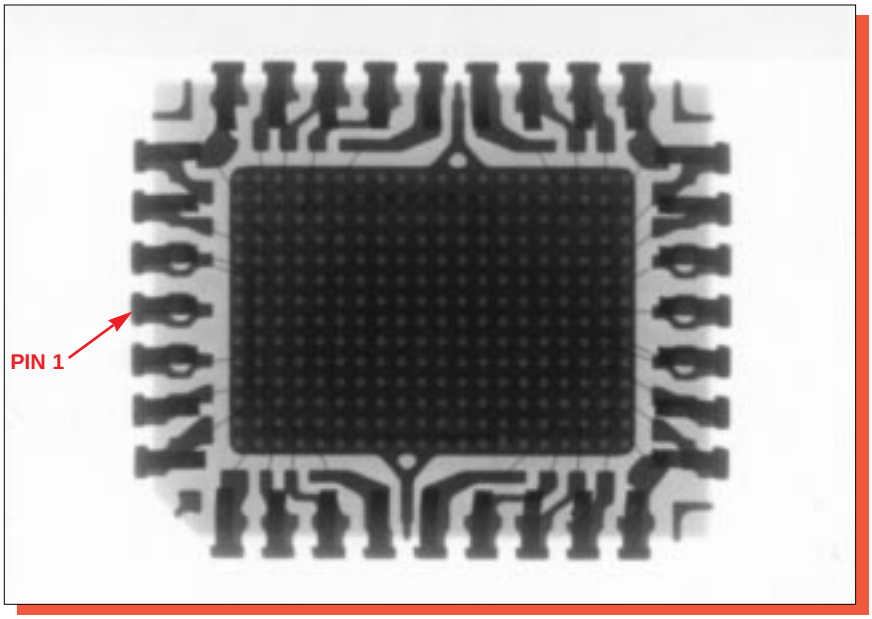


Figure 1. Package photograph and pinout of the Xicor X28C010J-20 128K x 8 EEPROM. Mag. 4x.



top

side

Figure 2. X-ray views of the package. Mag. 5x.

Figure 3. Optical section view of the package. Mag. 13x.

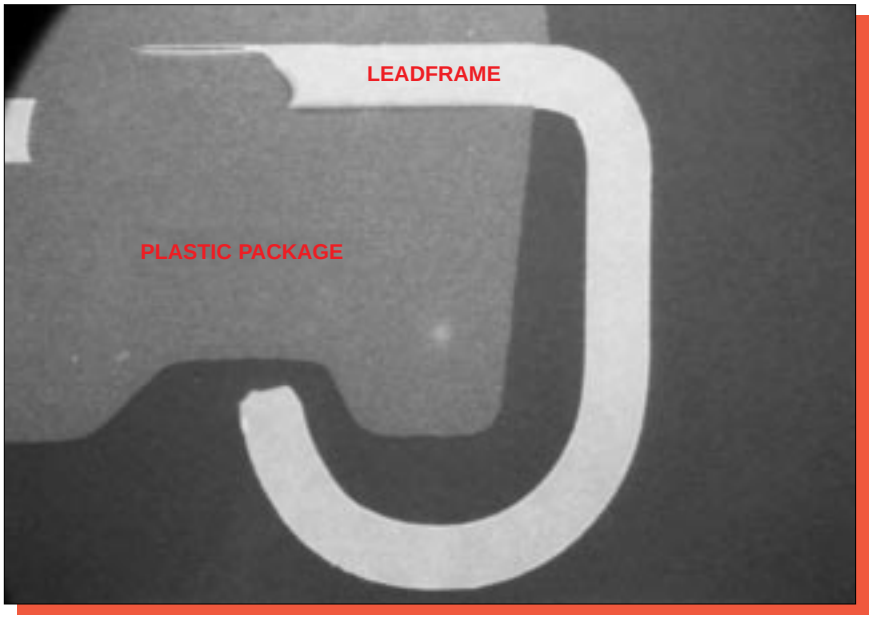
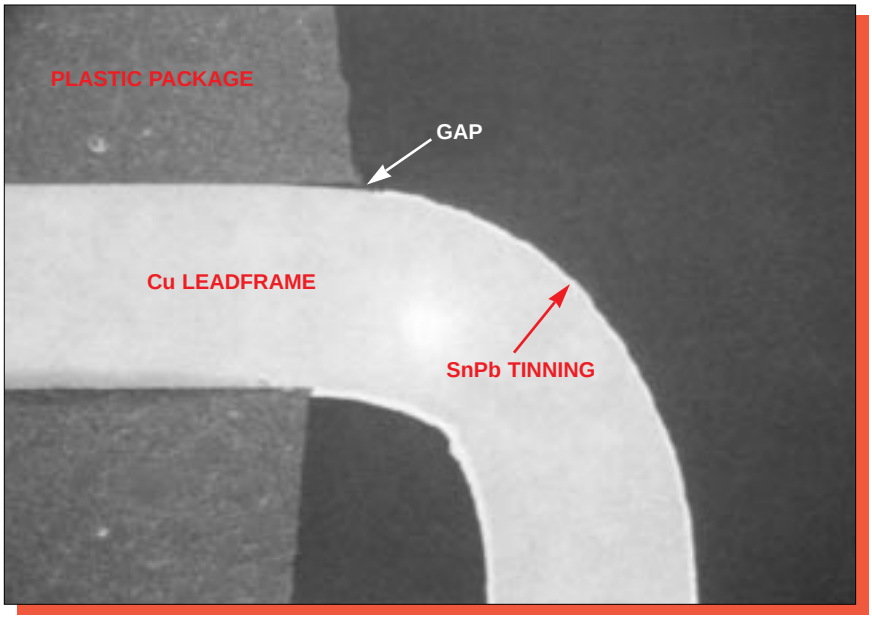
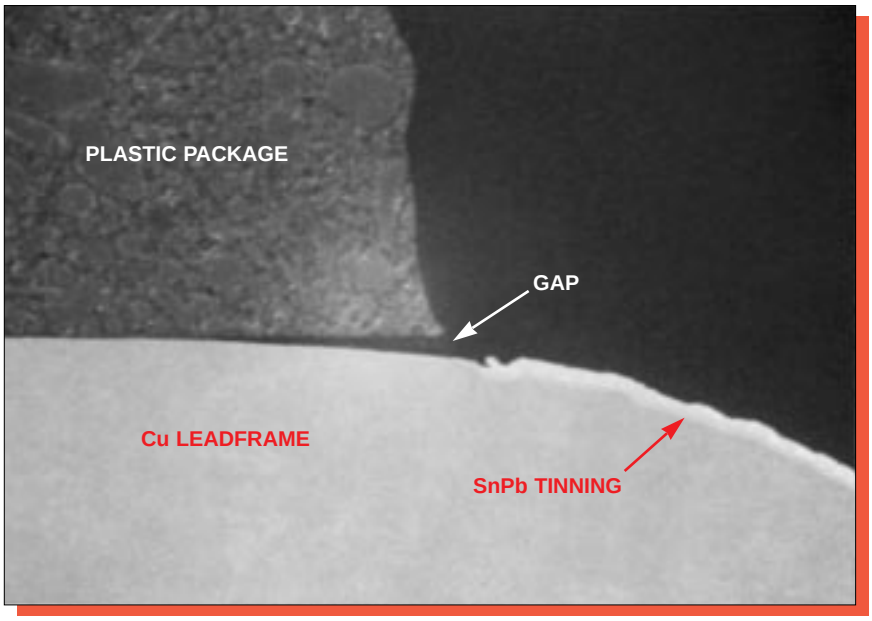


Figure 4. SEM section view of leadforming. Mag. 30x.

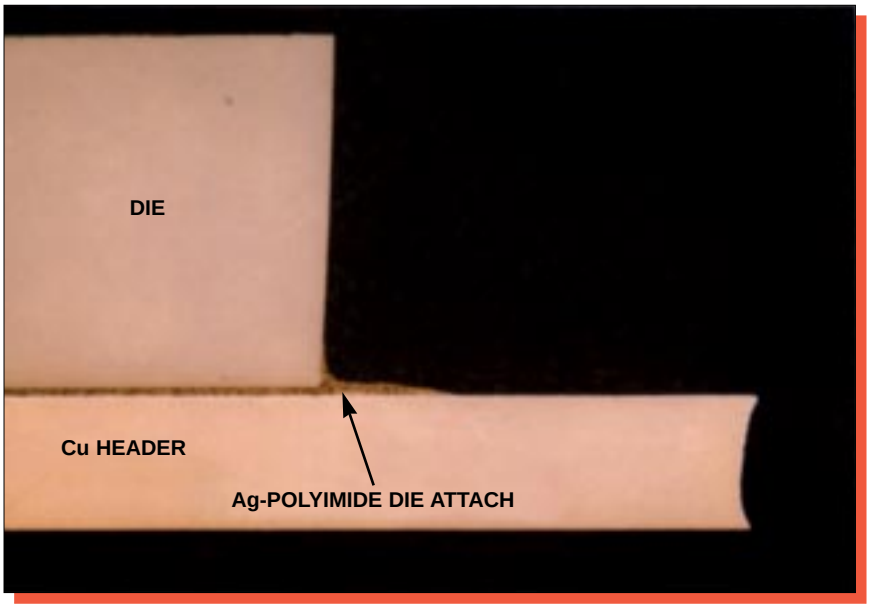


Mag. 100x

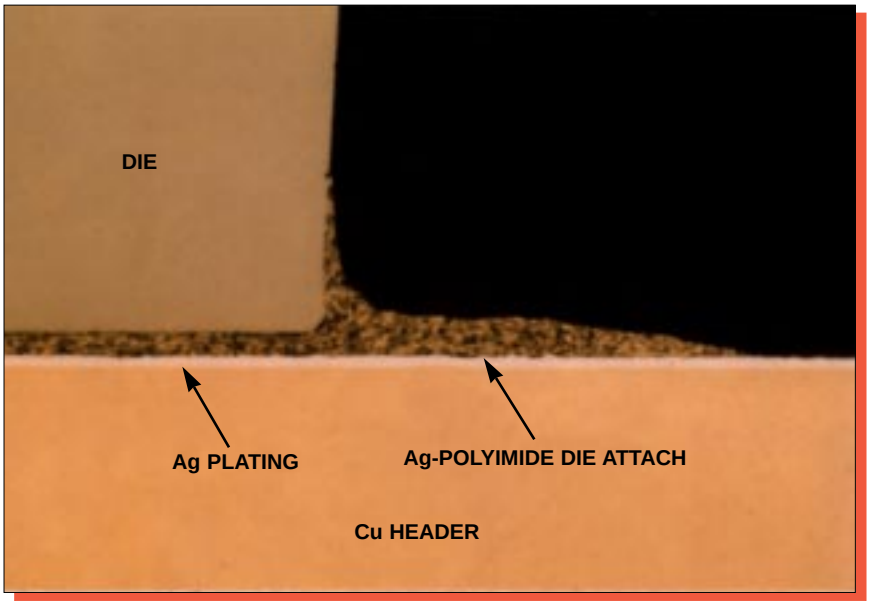


Mag. 300x

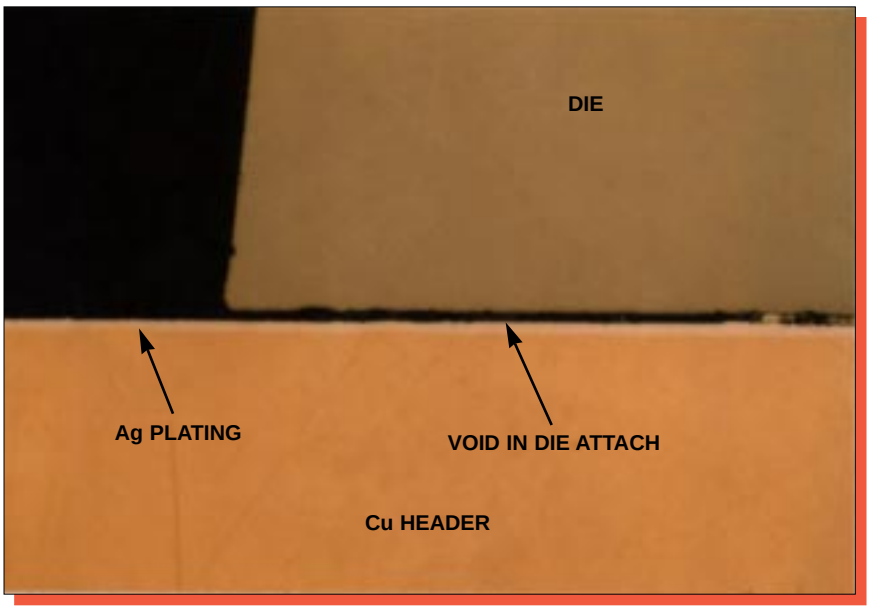
Figure 5. SEM section views of lead exit and tinning.



Mag. 65x

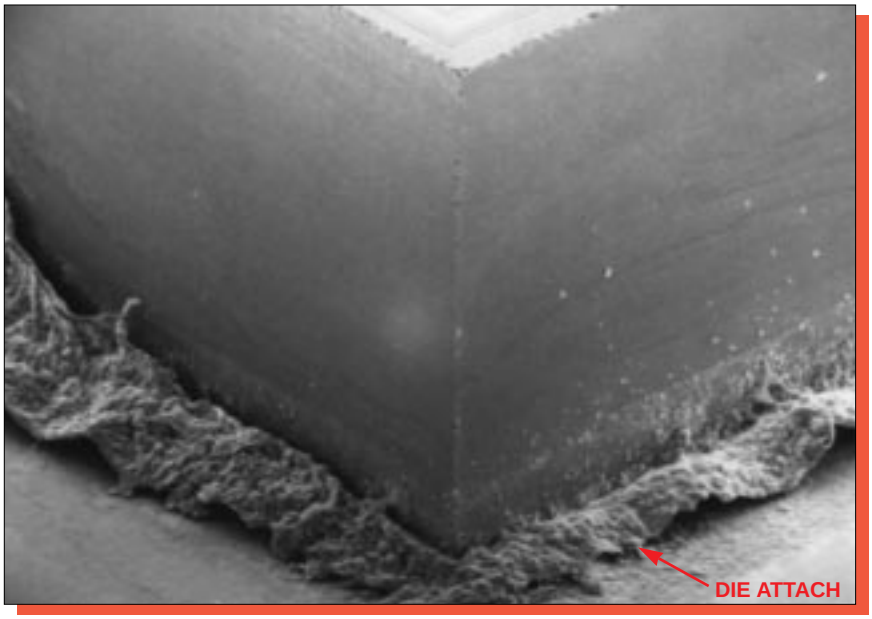


Mag. 200x

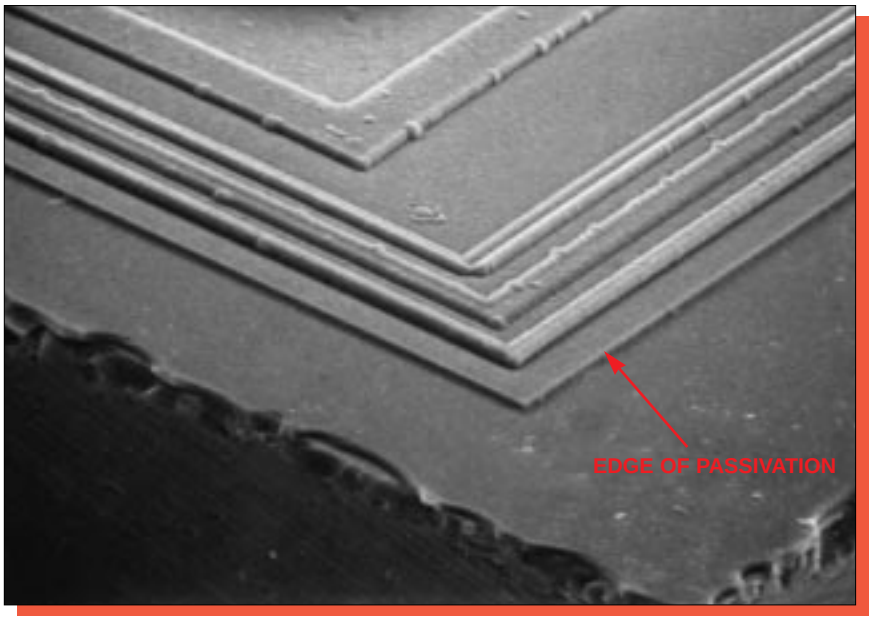


Mag. 200x

Figure 6. Optical section views of dicing and die attach.



Mag. 100x



Mag. 700x

Figure 7. Perspective SEM views of dicing and edge seal. 60°.

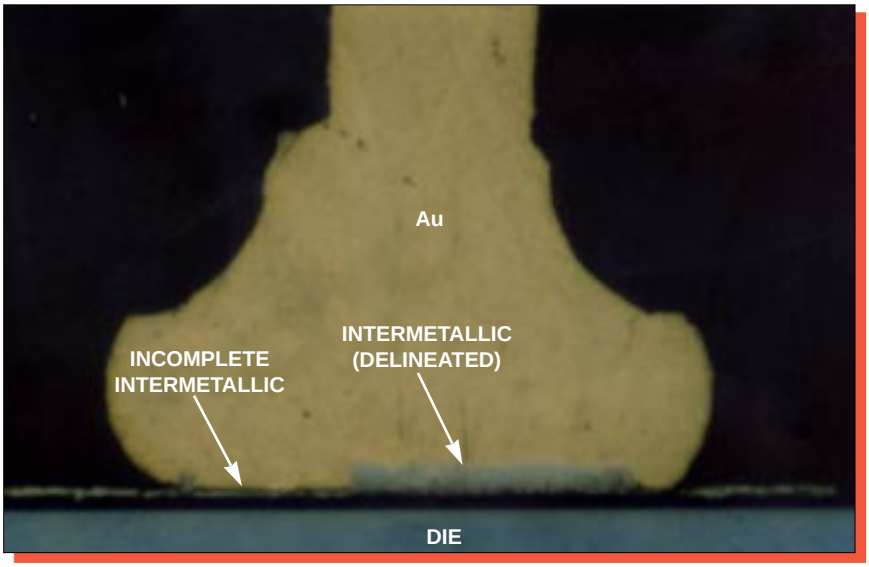


Figure 8. Optical view of a typical ball bond. Etched, Mag. 800x.

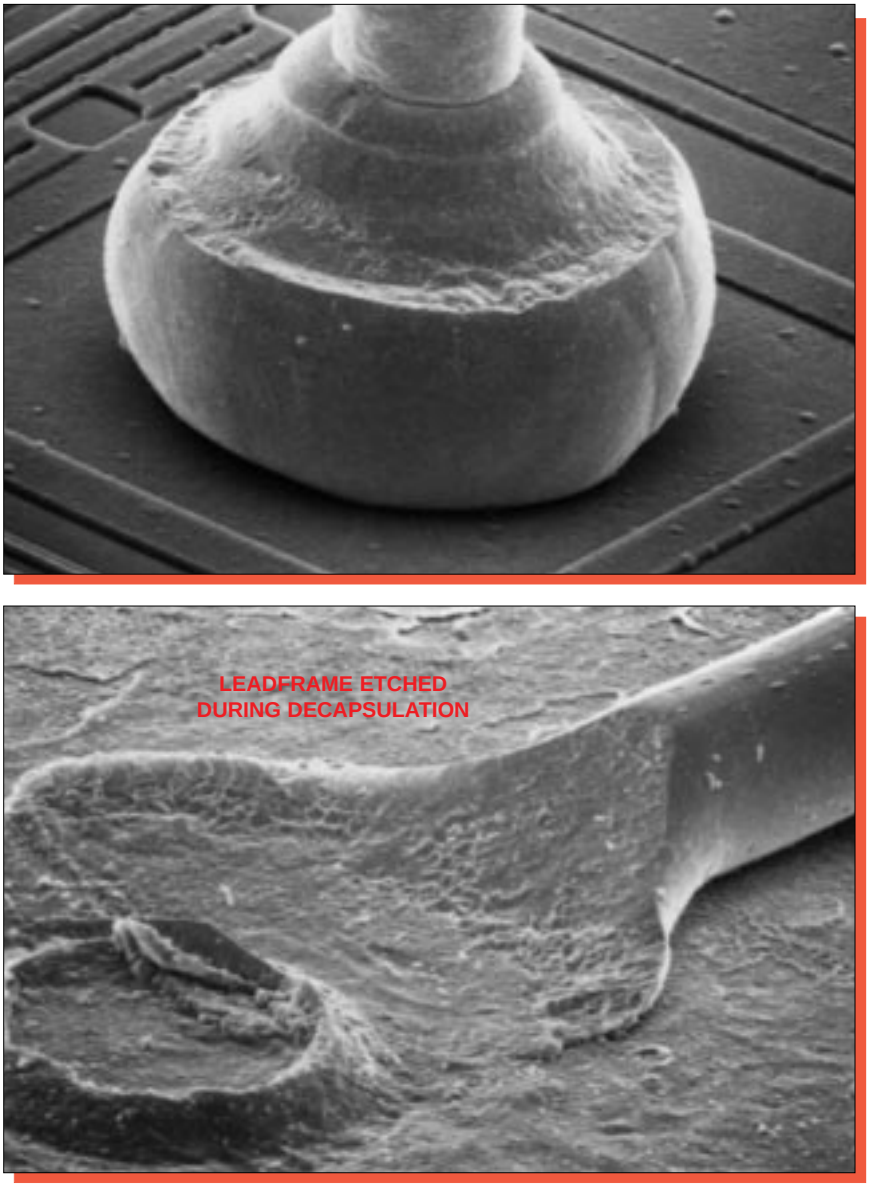


Figure 9. Perspective SEM views of typical wirebonds. Mag. 800x, 60°.

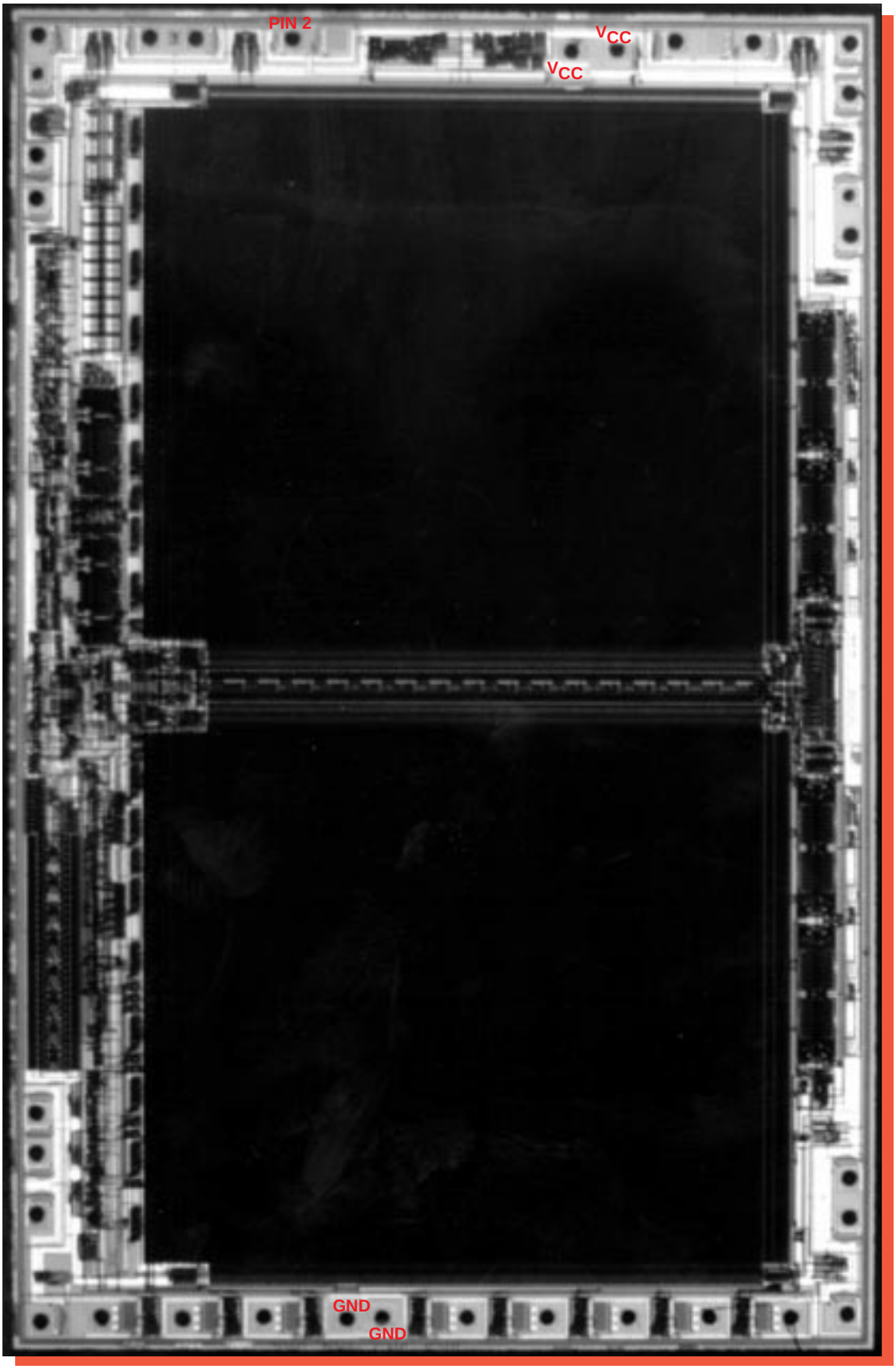
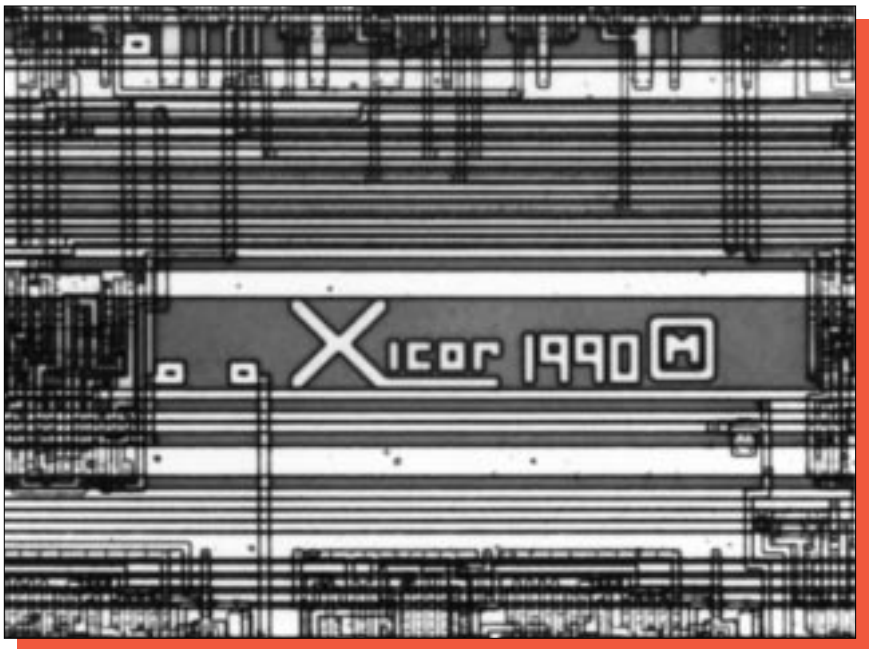


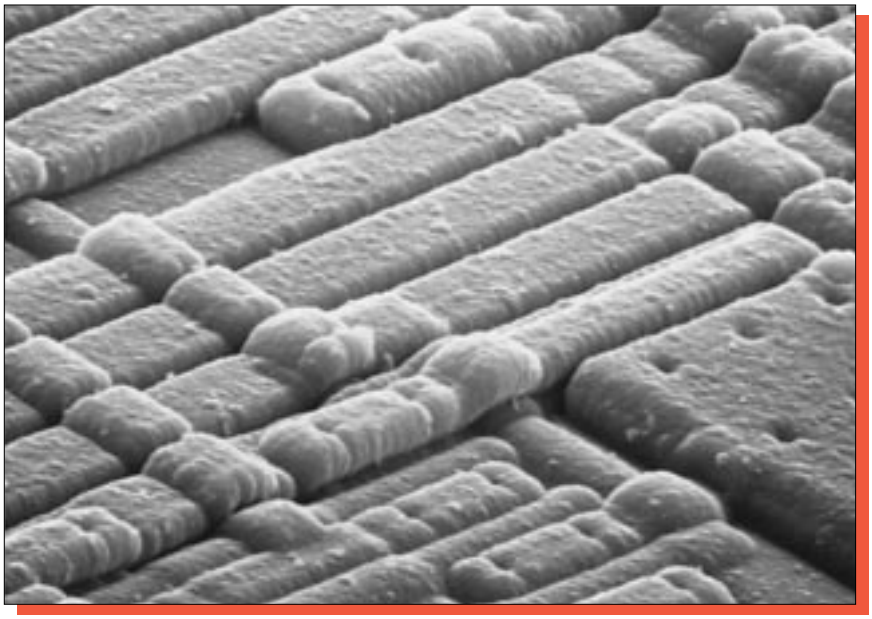
Figure 10. Whole die photograph of Xicor X28CO10J-20 128K x 8 EEPROM.
Mag. 26x.



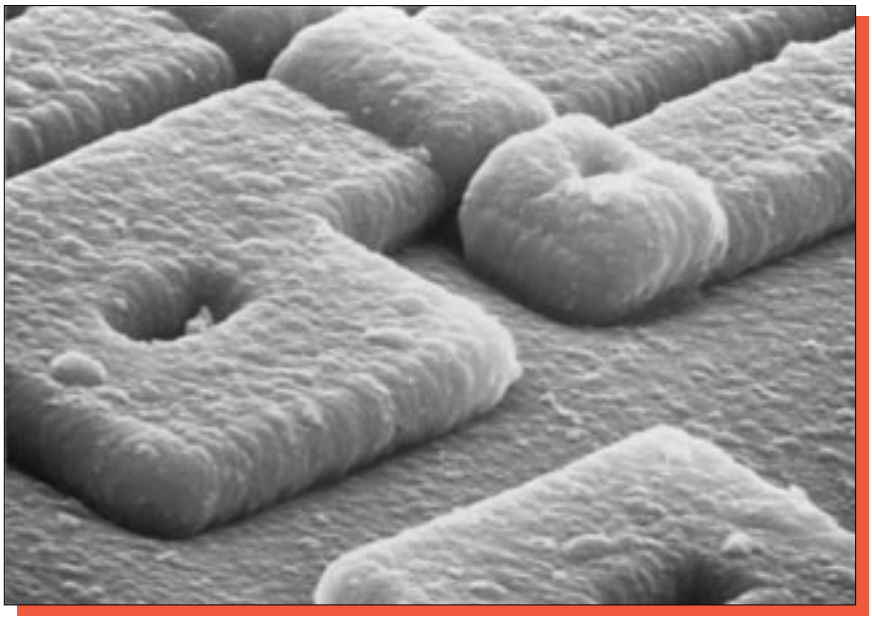
Mag. 320x

Mag. 160x

Figure 11. Optical views of markings from die surface.

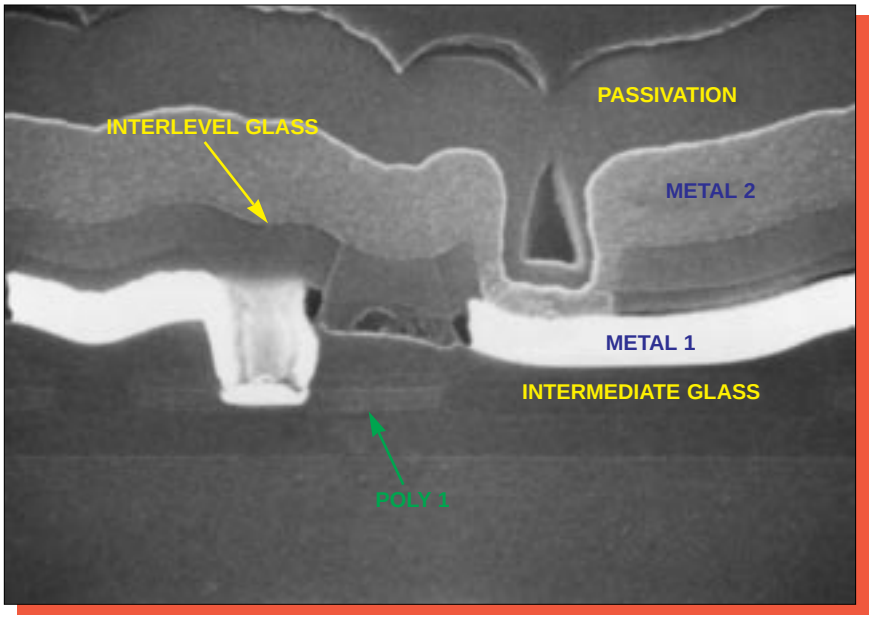


Mag. 3000x

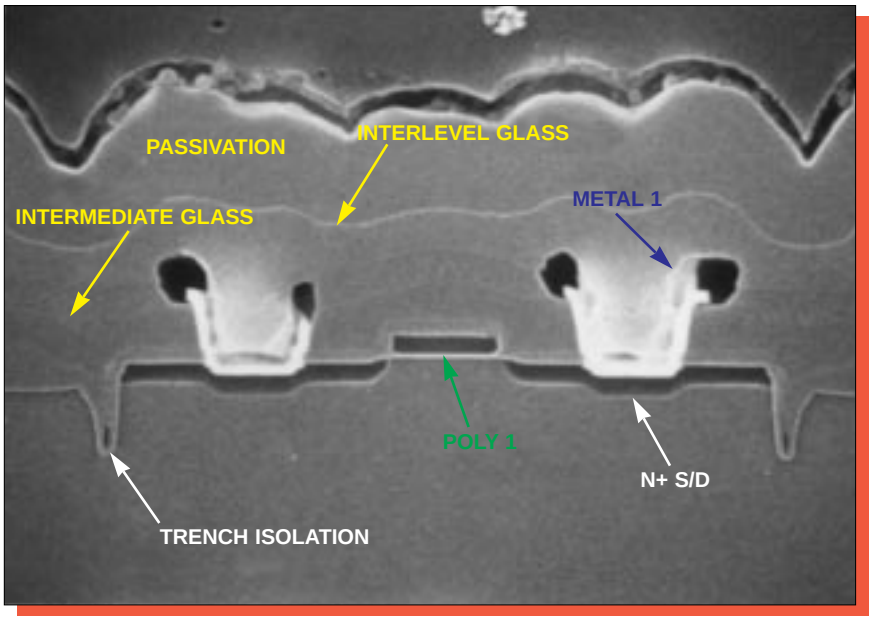


Mag. 6000x

Figure 12. Perspective SEM views illustrating overlay passivation coverage. 60°.



glass-etch



silicon etch

Figure 13. SEM section views illustration general structure. Mag. 10,000x.

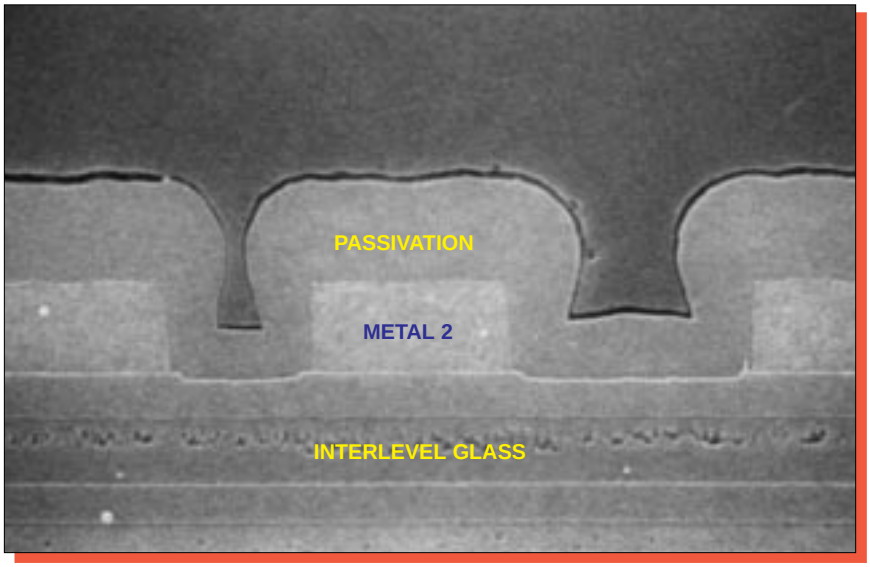


Figure 14. SEM section view of metal 2 line profile. Mag. 10,000x.

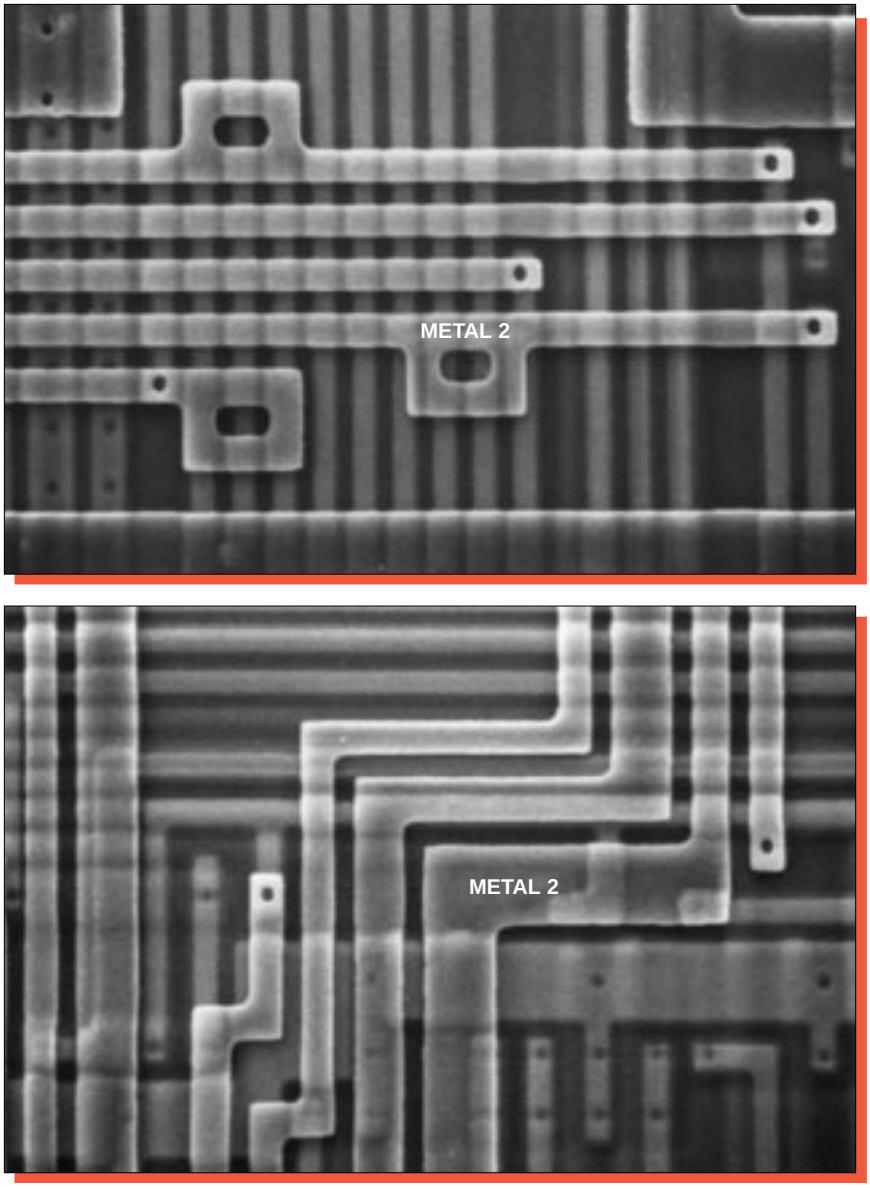
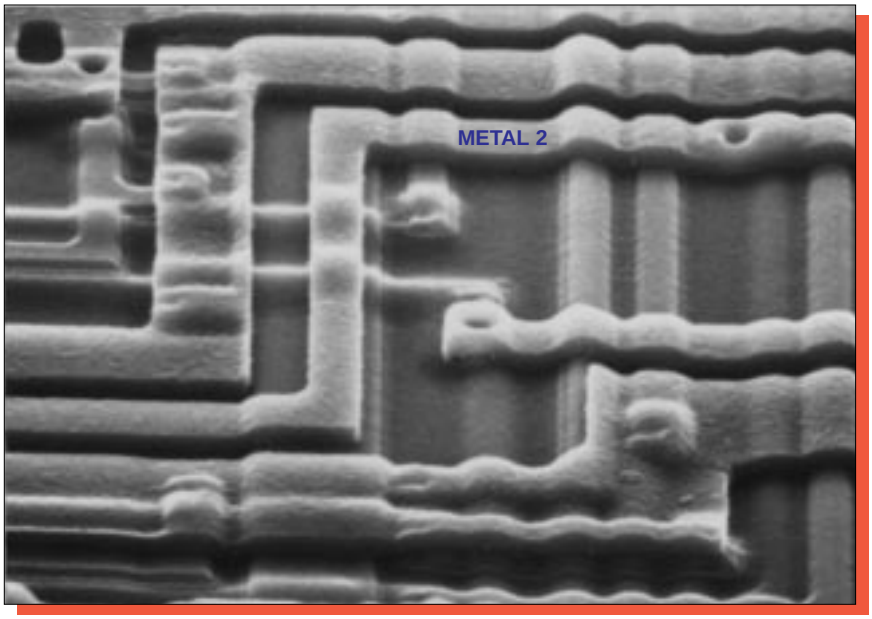
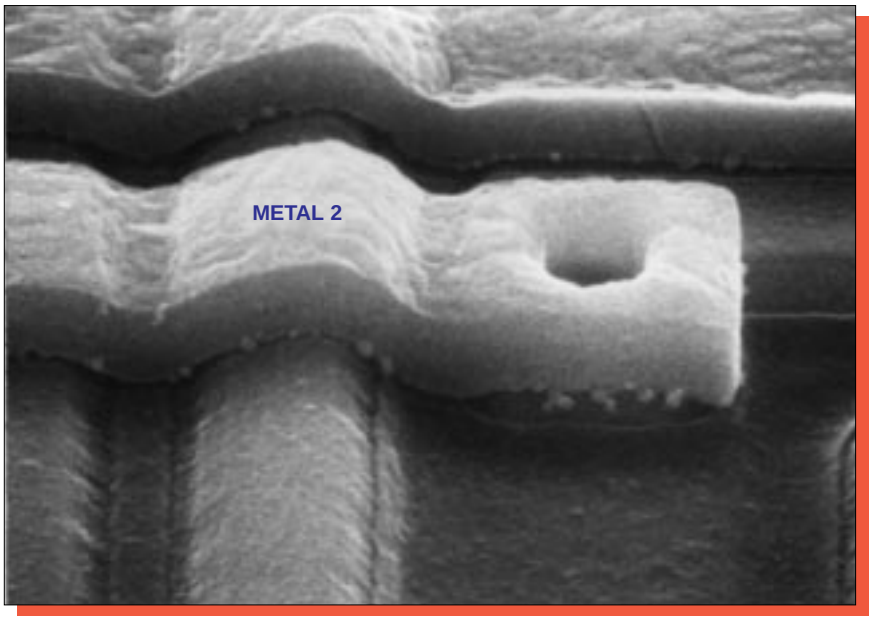


Figure 15. Topological SEM views of metal 2 patterning. Mag. 1500x.



Mag. 2500x



Mag. 10,000x

Figure 16. Perspective SEM views of metal 2 coverage. 60°.

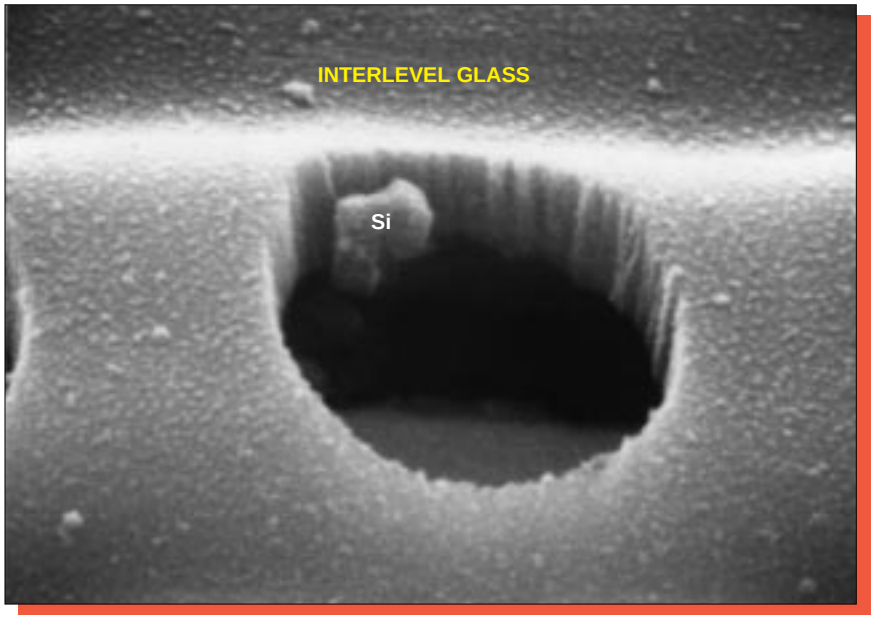


Figure 17. Perspective SEM view of via cut in oxide. Mag. 30,000x, 60°.

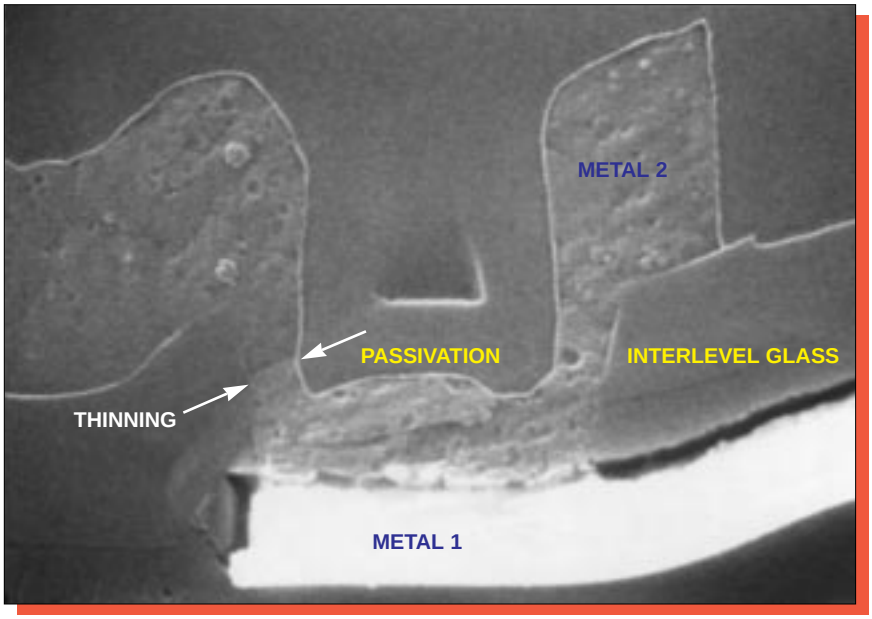


Figure 18. SEM section view of metal 2-to-metal 1 via. Mag. 25,000x.

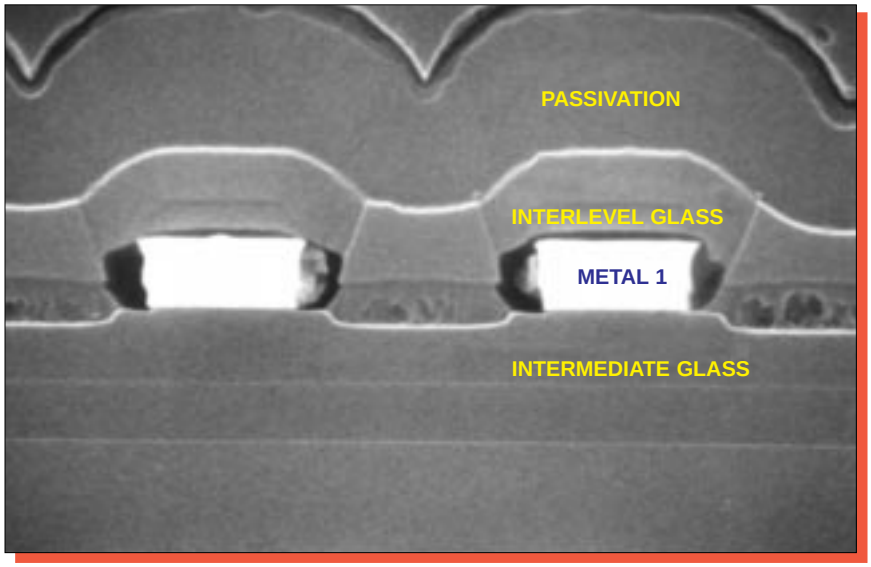
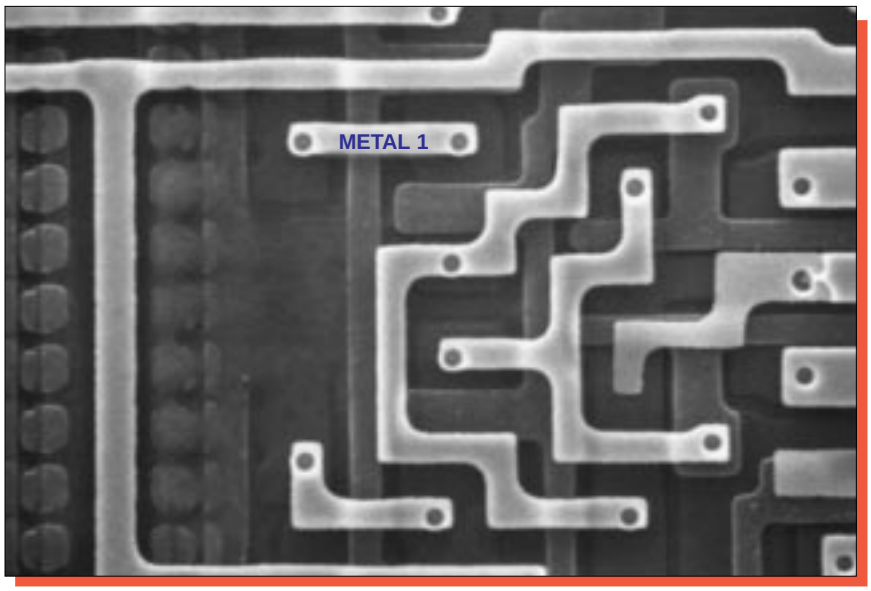
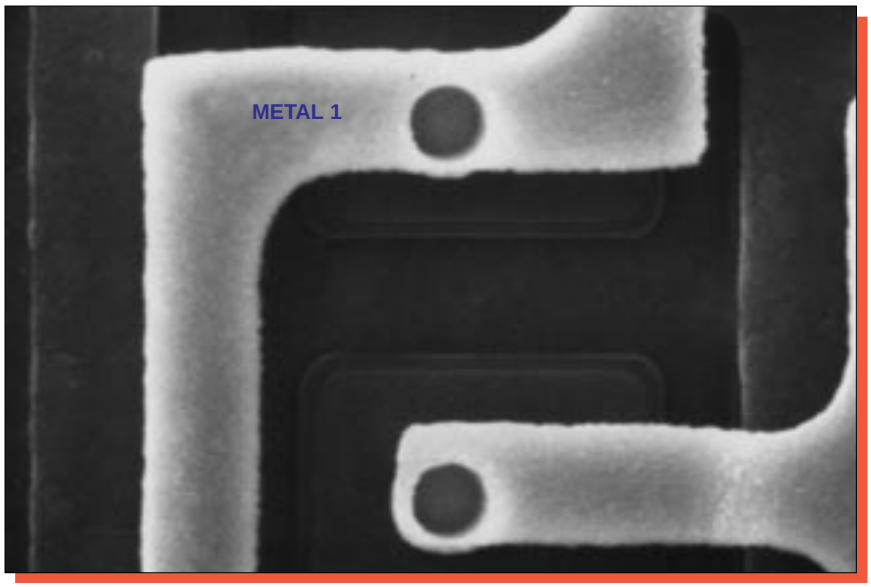


Figure 19. SEM section view of metal 1 line profiles. Mag. 14,000x.

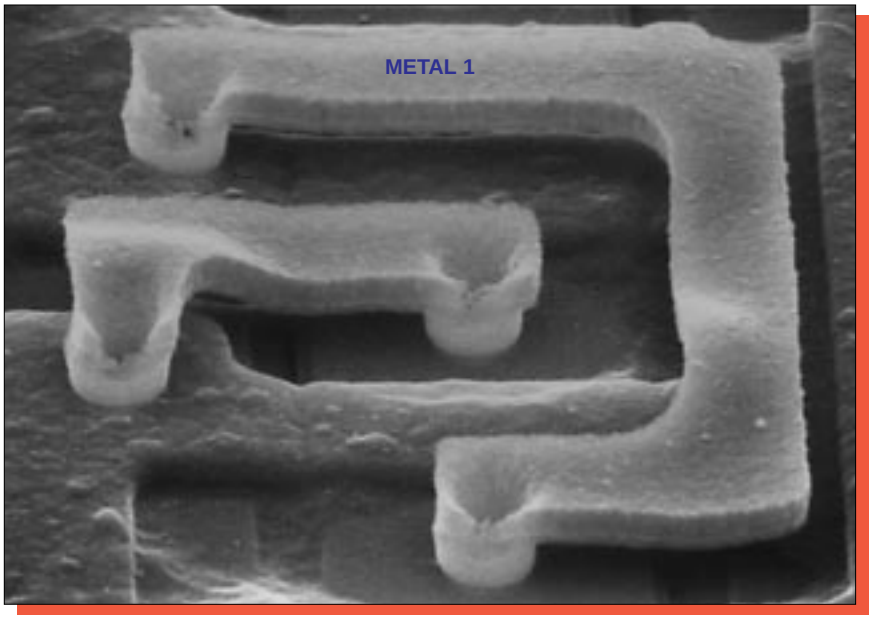


Mag. 2500x

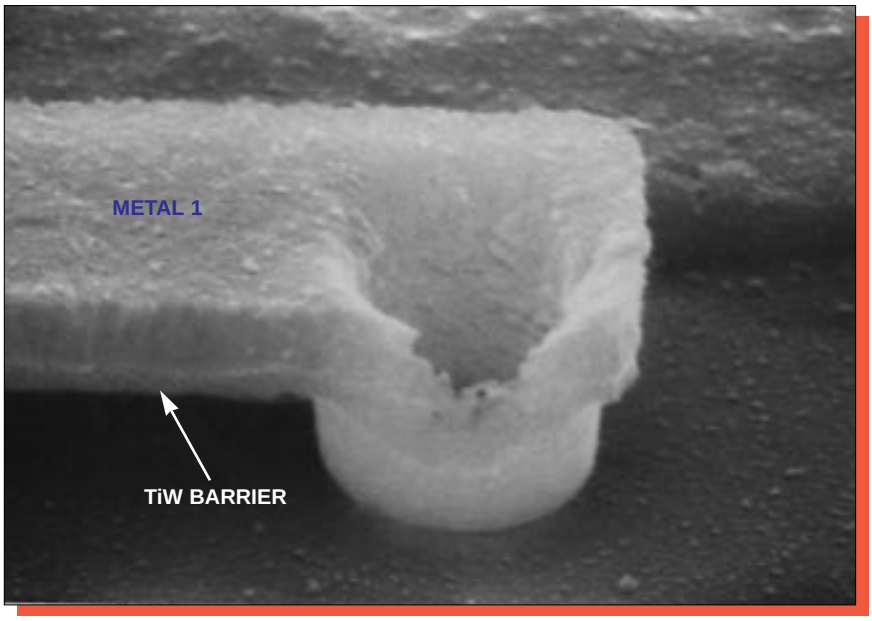


Mag. 10,000x

Figure 20. Topological SEM views of metal 1 patterning.

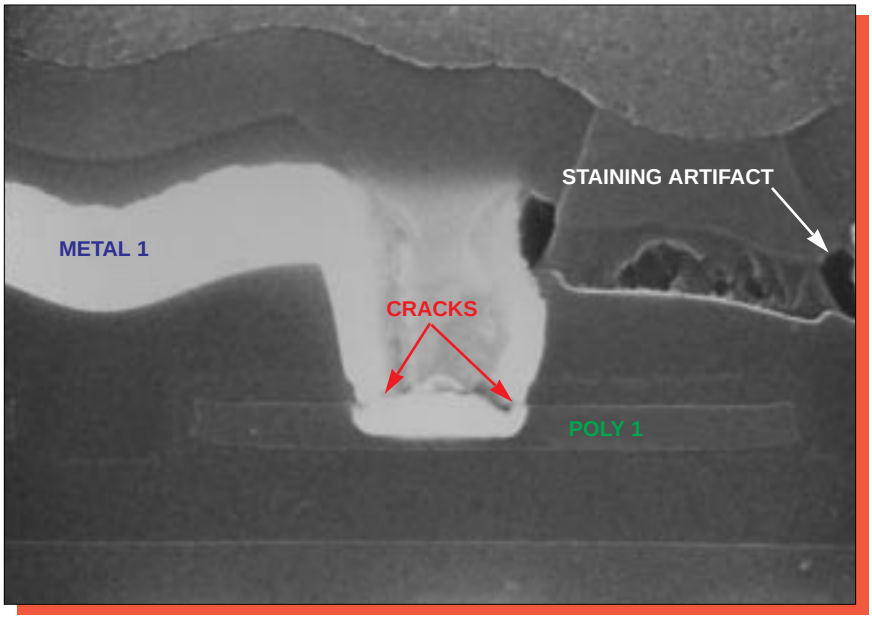


Mag. 9000x



Mag. 25,000x

Figure 21. Perspective SEM views of metal 1 coverage. 60°.



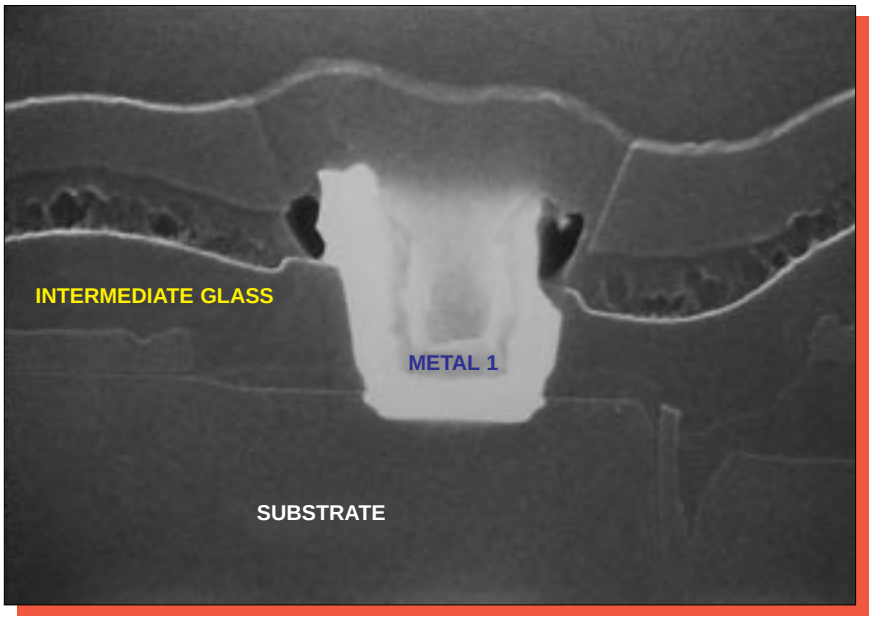
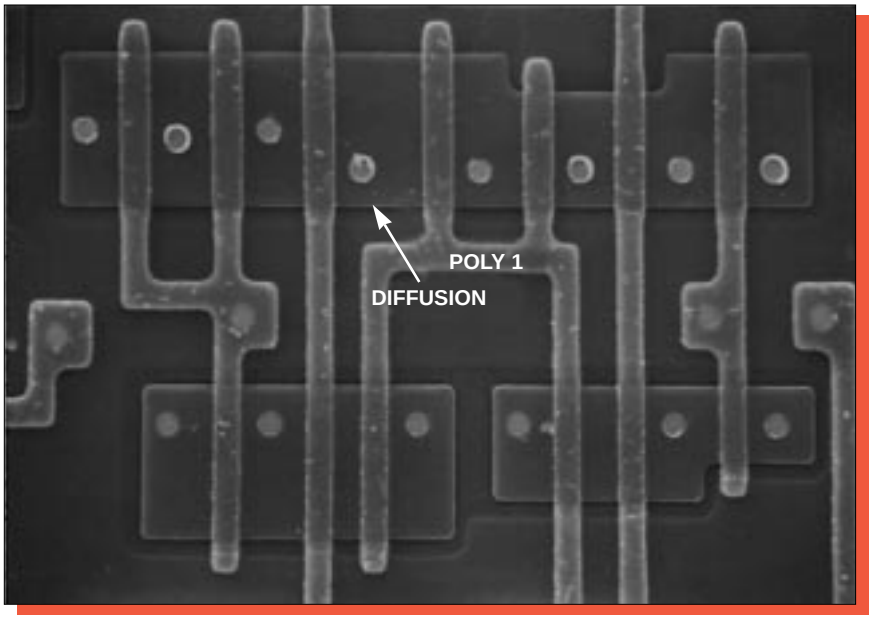


Figure 22. Glass etch SEM section views of typical metal 1 contacts. Mag. 20,000x.



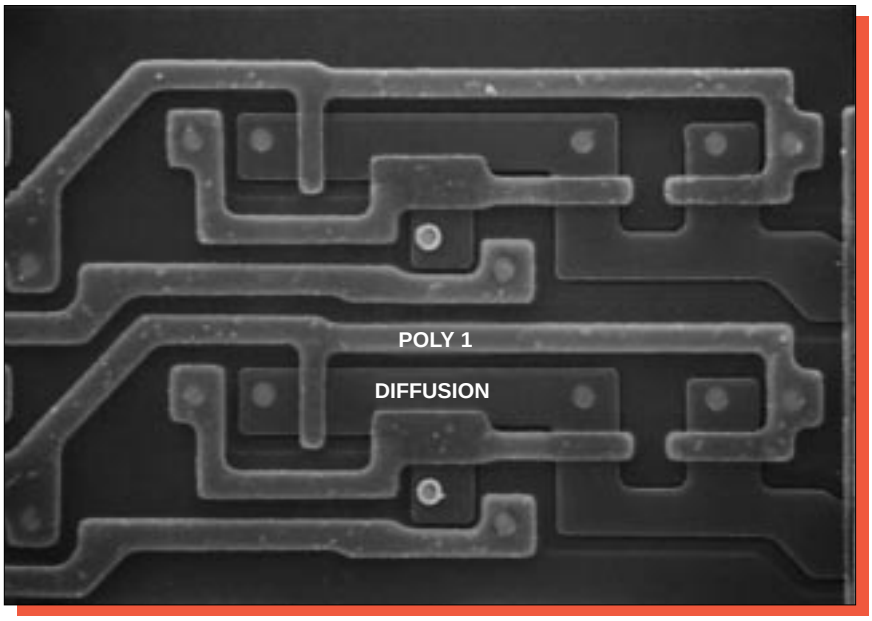
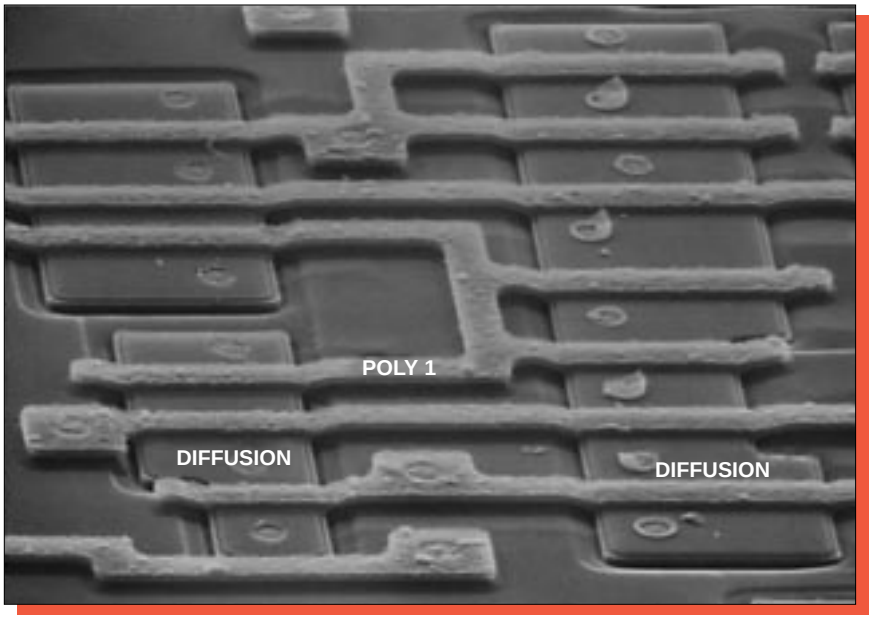
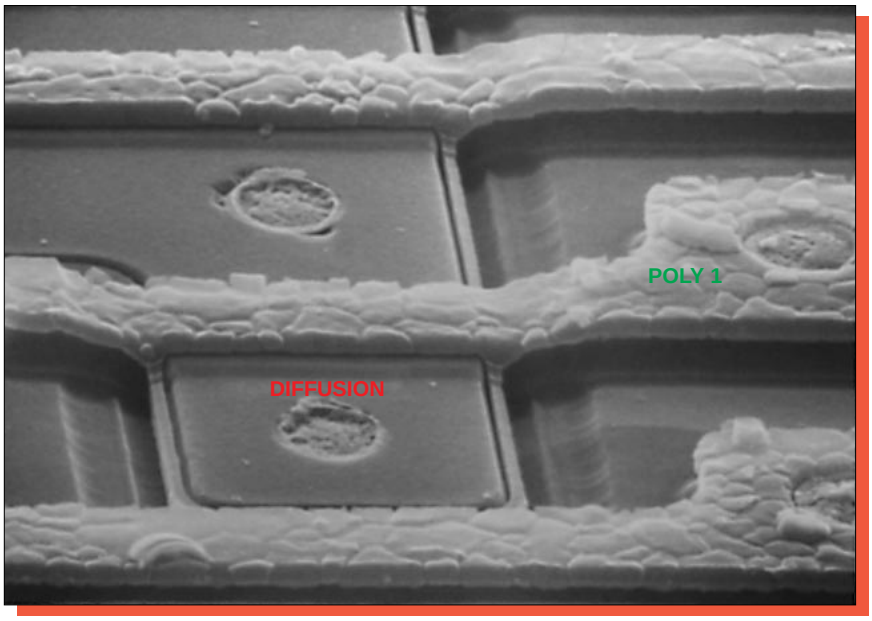


Figure 23. Topological SEM views of poly 1 patterning. Mag. 2500x.

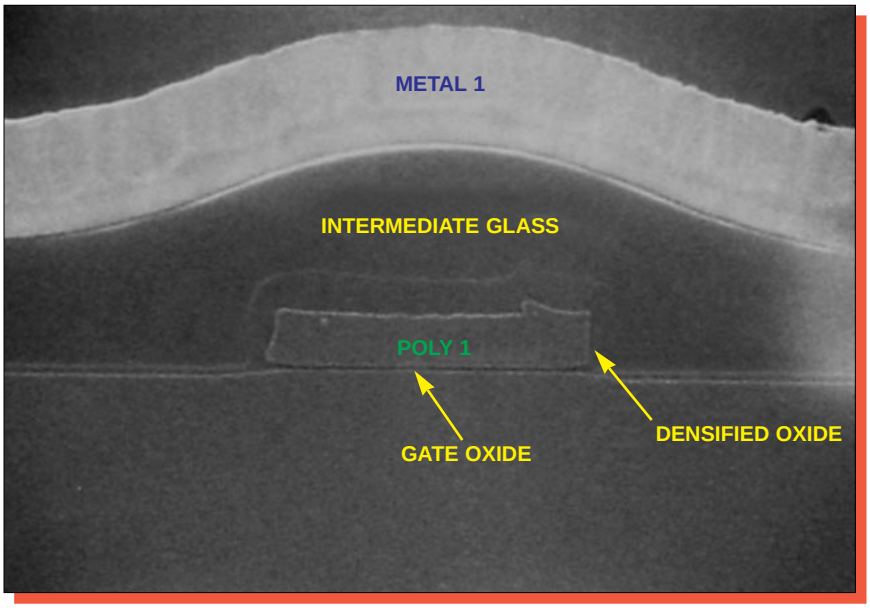


Mag. 4000x

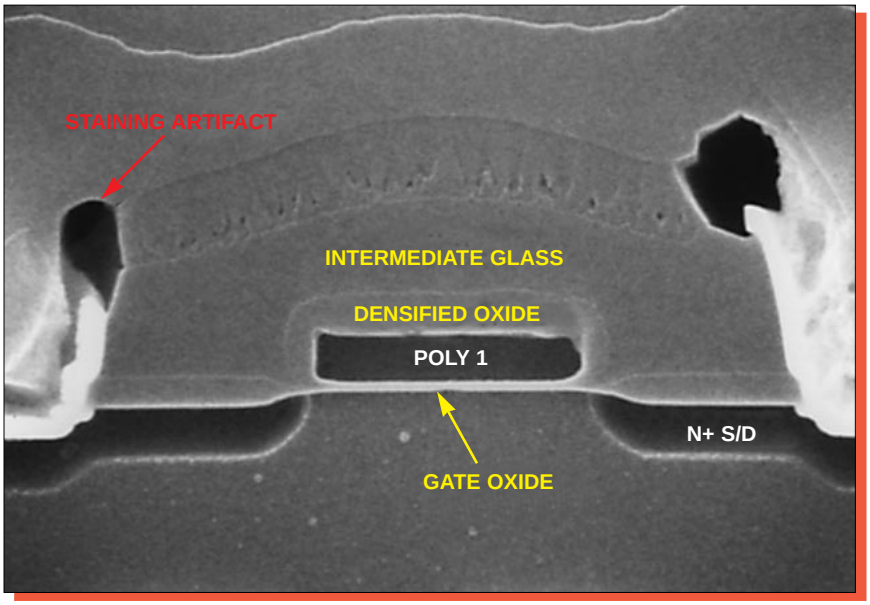


Mag. 12,000x

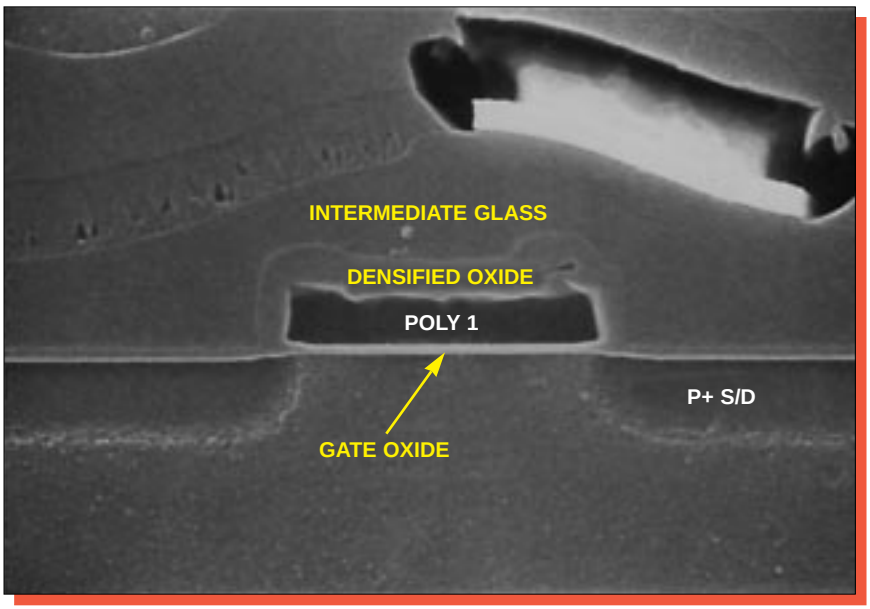
Figure 24. Perspective SEM views of poly 1 coverage. 60°.



glass-etch



N-channel



P-channel

Figure 25. SEM section views of typical transistors. Mag. 25,000x.

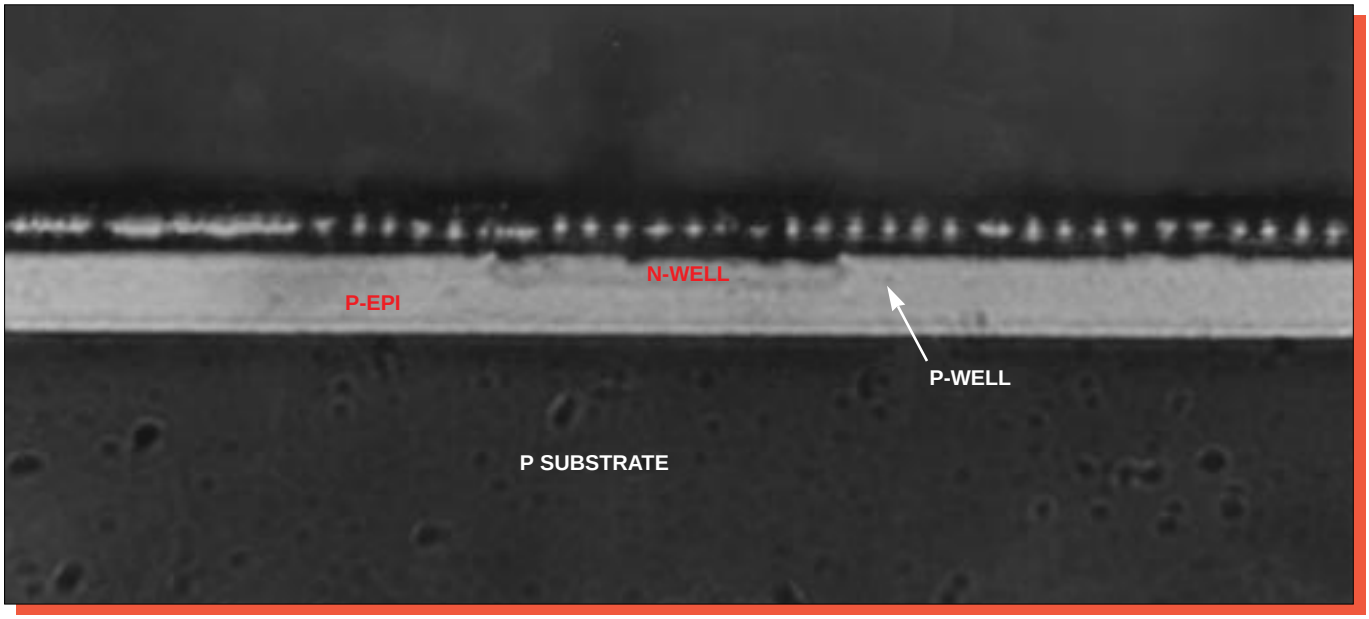


Figure 25a. Optical section view of well and epi layers. Mag. 1000x.

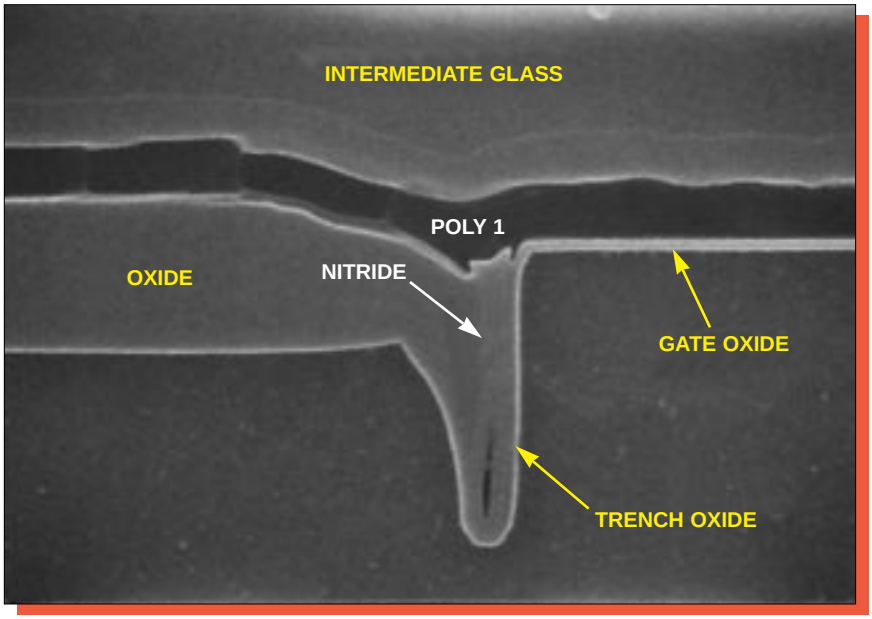
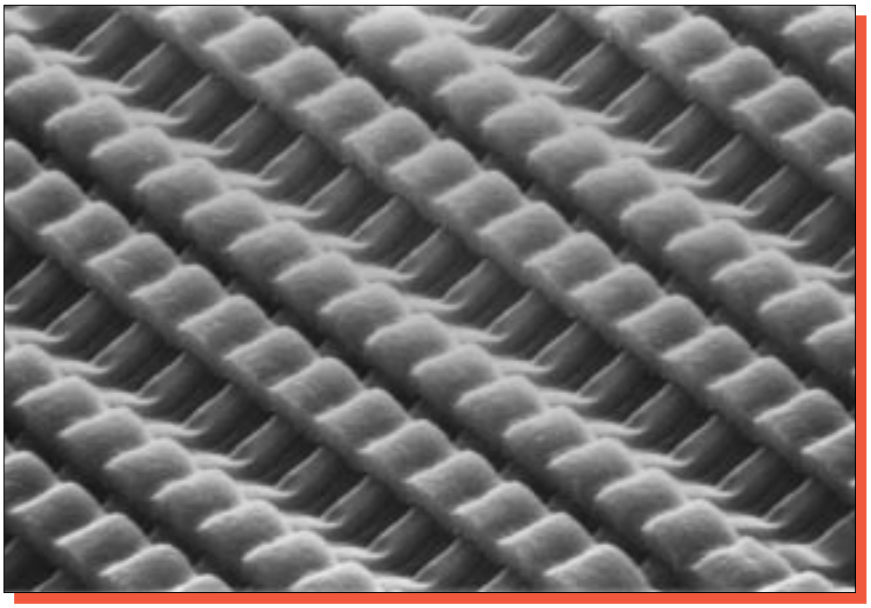
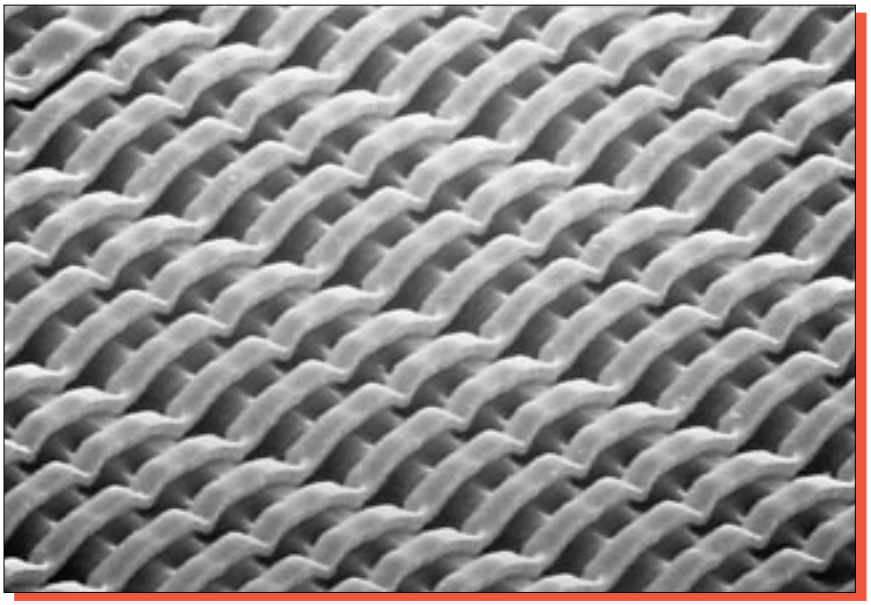


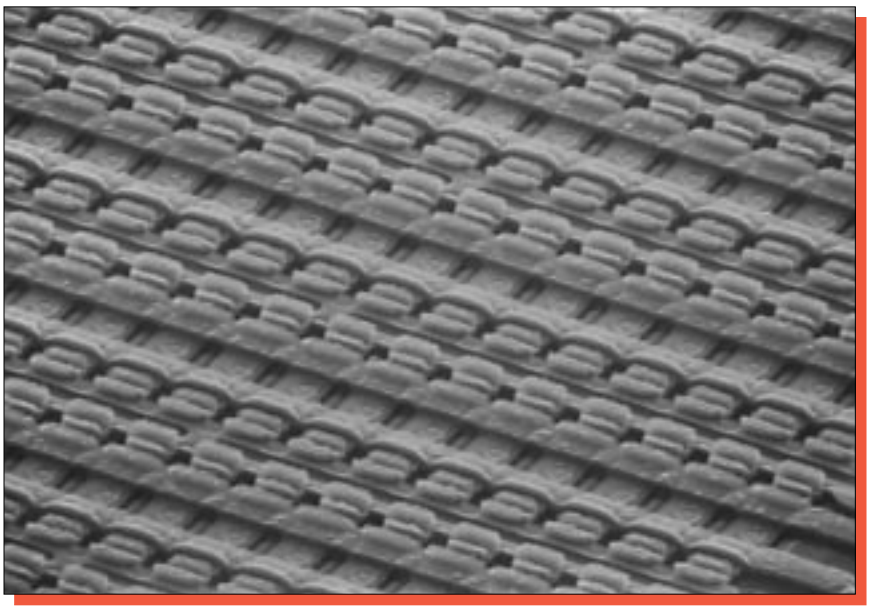
Figure 25b. SEM section view illustrating isolation. Mag. 30,000x.



metal 2



metal 1



poly

Figure 26. Perspective SEM views of EEPROM array. Mag. 3000x, 60°.

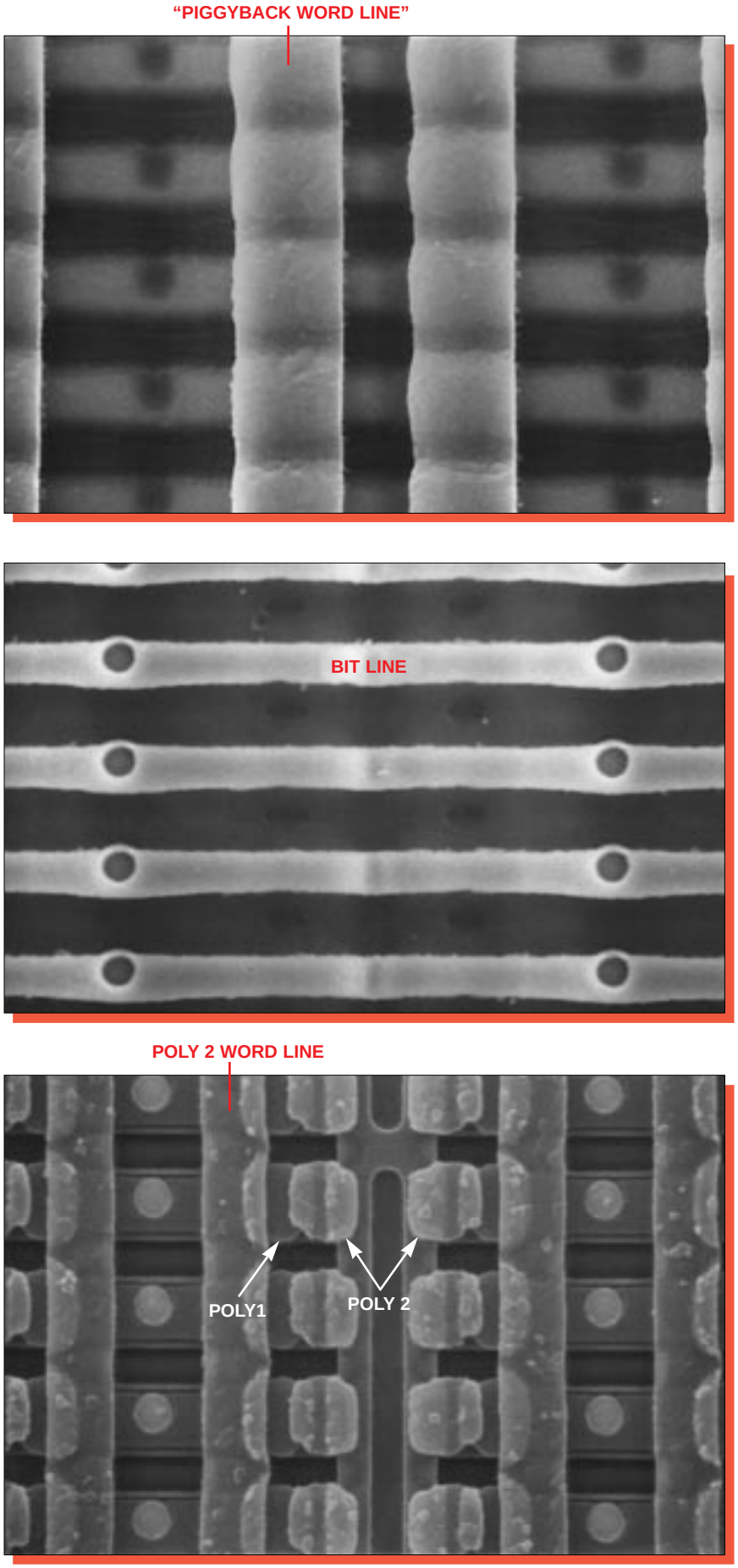
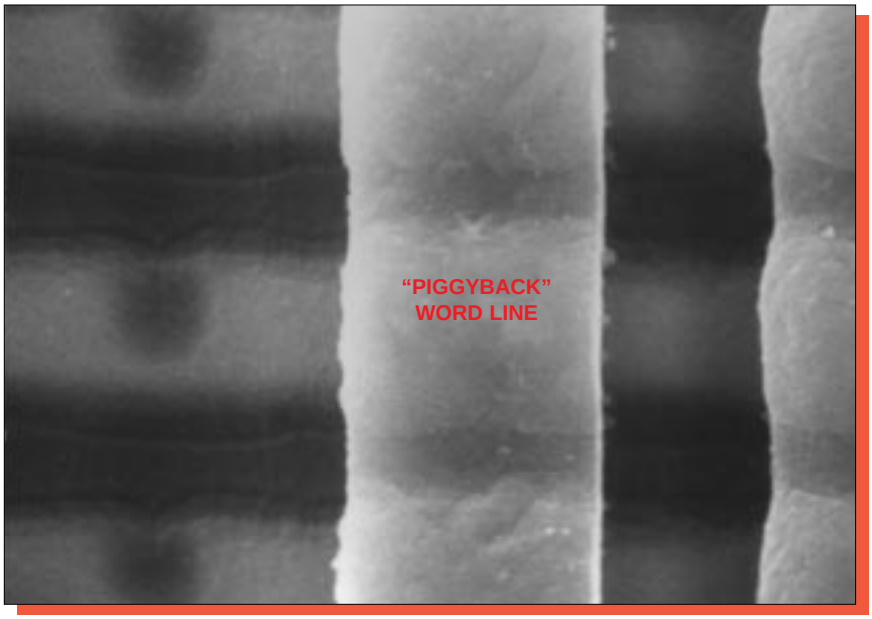
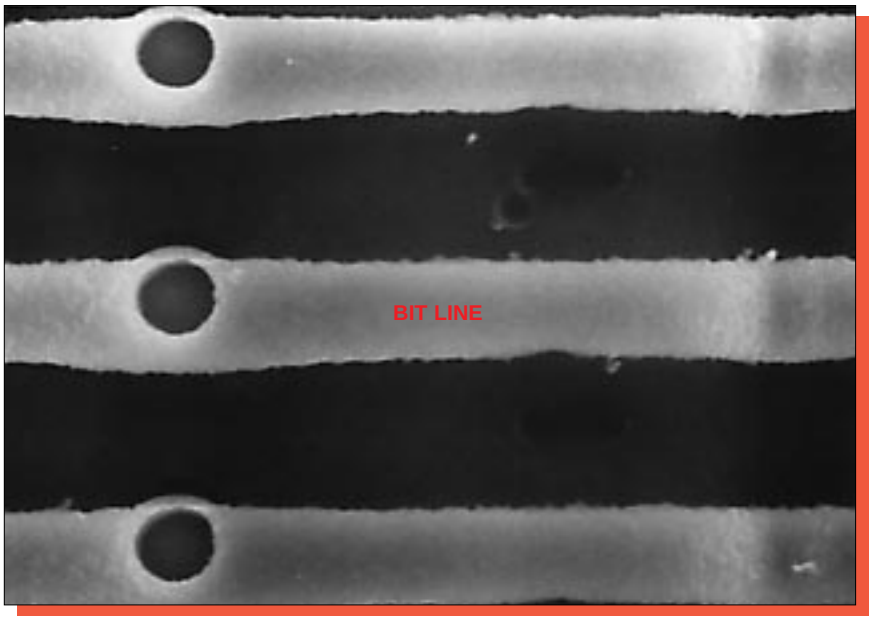


Figure 27. Topological SEM views of EEPROM cell array. Mag. 5000x, 0°.

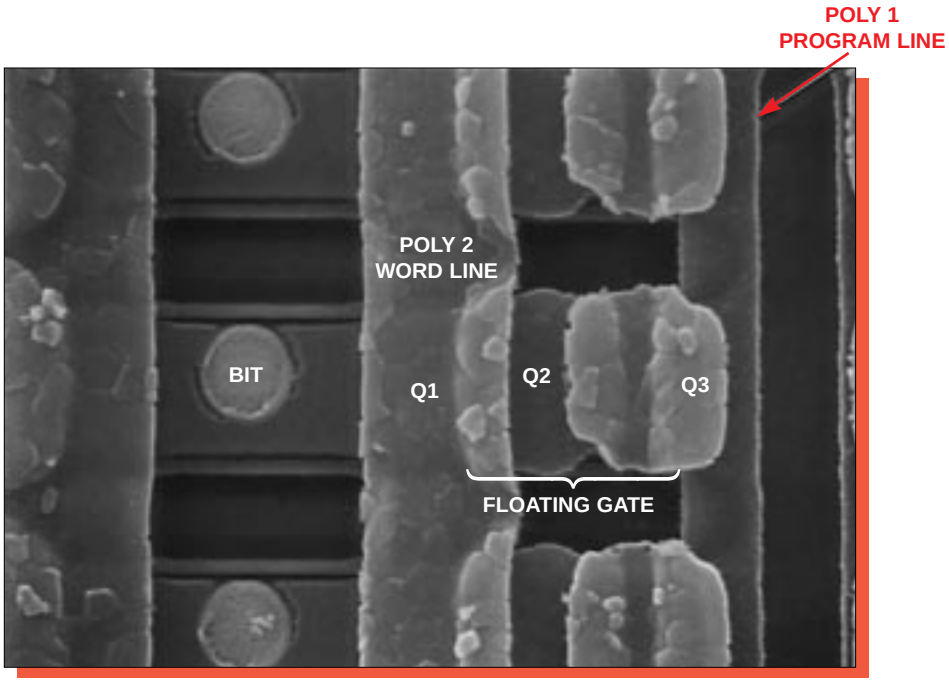


metal 2



metal 1

Figure 27a. Detailed topological SEM views of EEPROM array. Mag. 10,000x.



Delayered

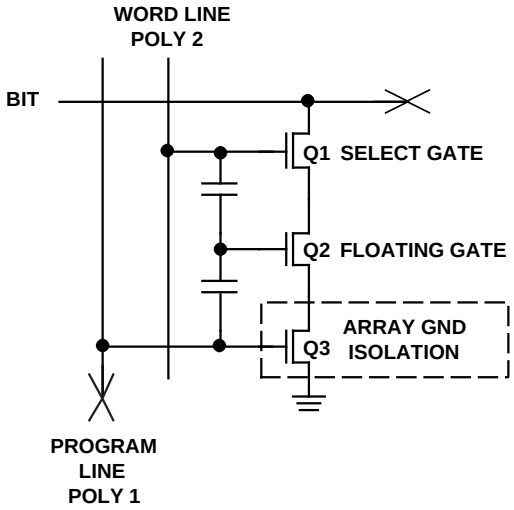
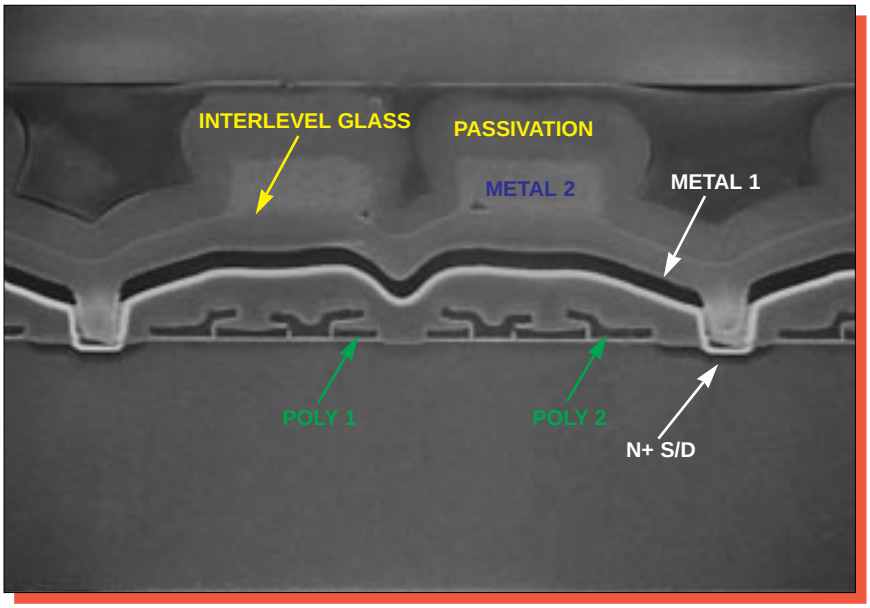
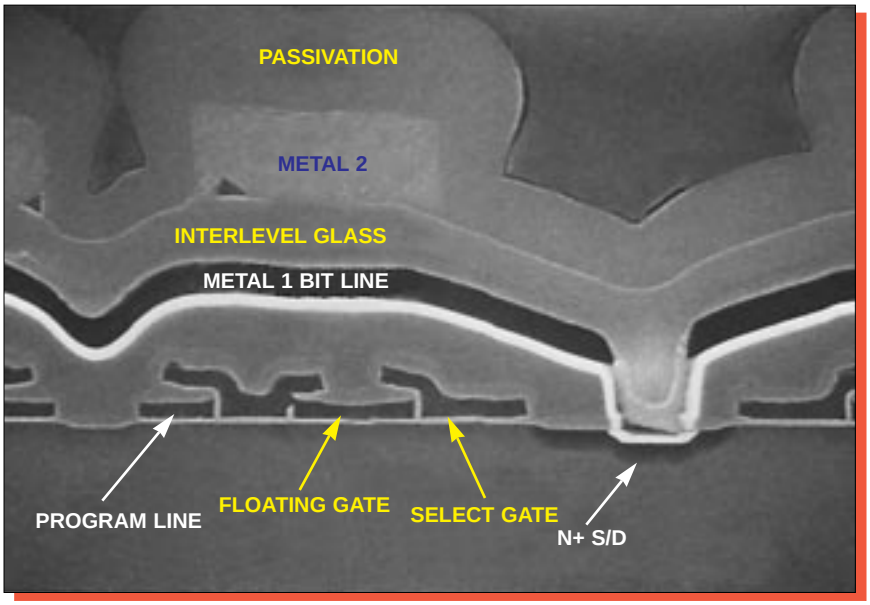


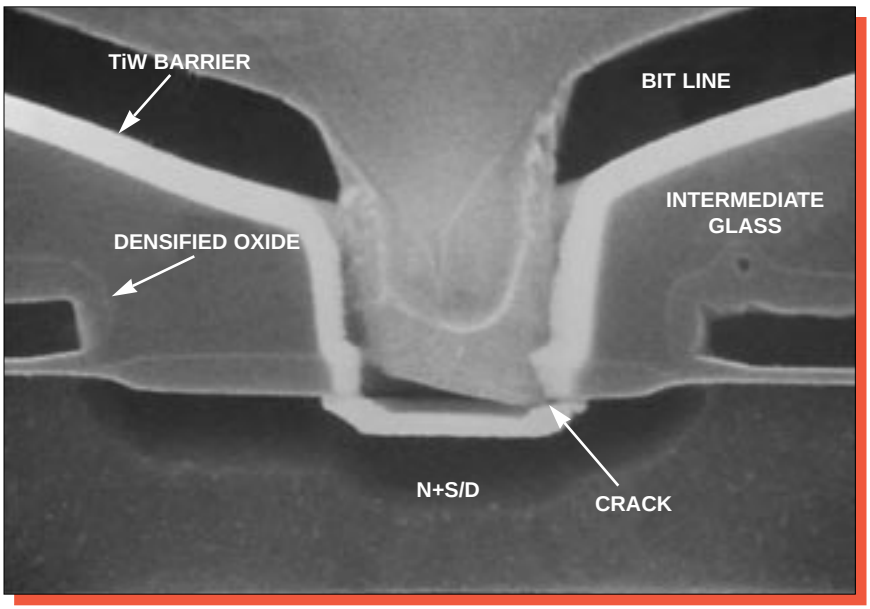
Figure 27b. Detailed topological view and schematic of an EEPROM cell.
Mag. 10,000x.



Mag. 6000x

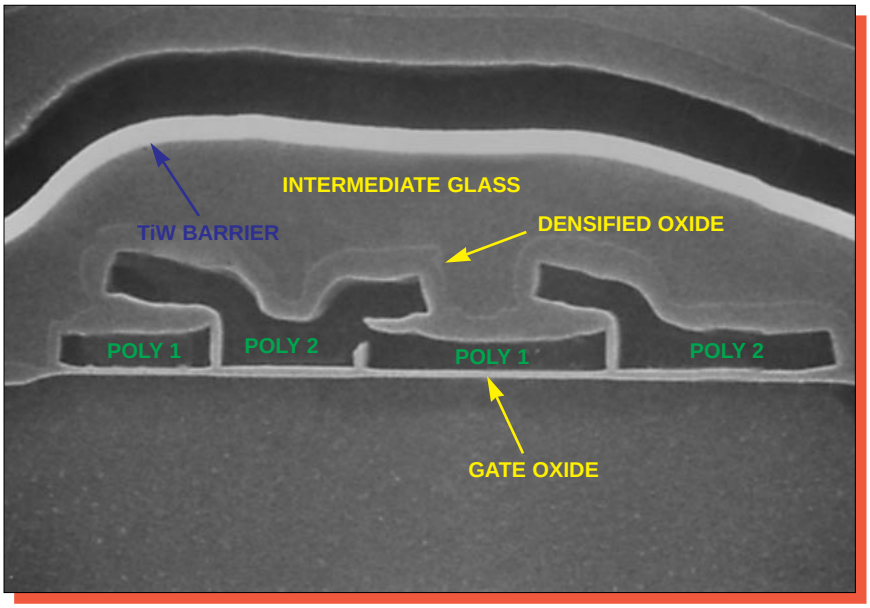


Mag. 10,000x

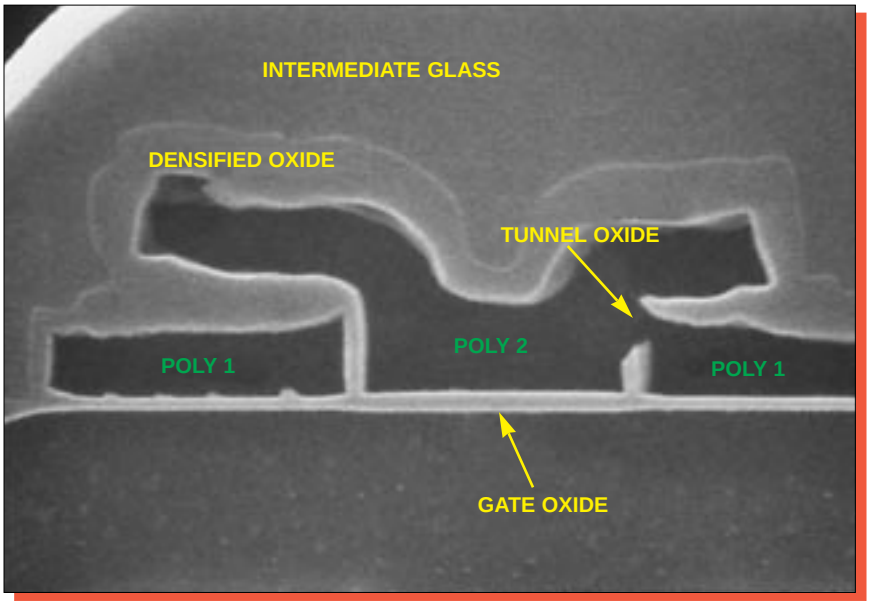


Mag. 30,000x

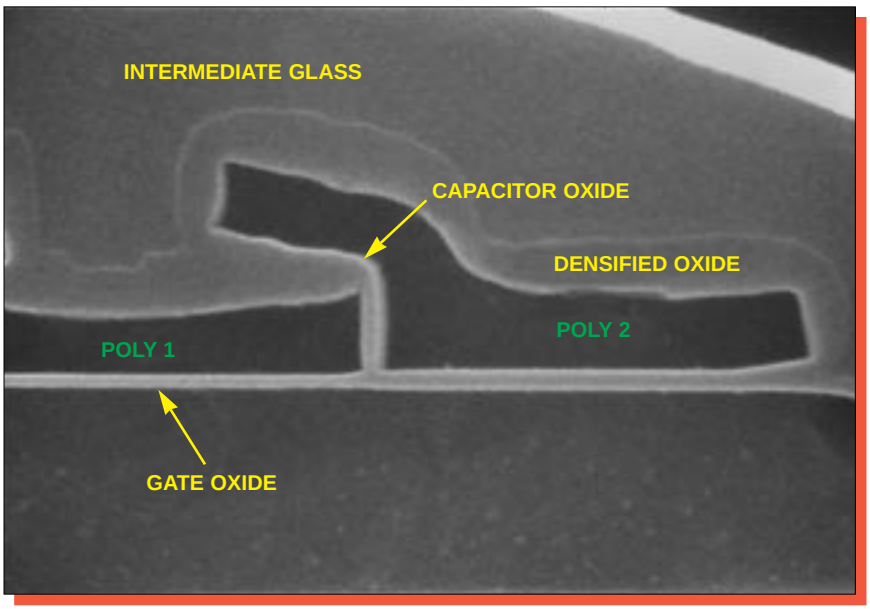
Figure 28. SEM section views of an EEPROM cell.



Mag. 20,000x

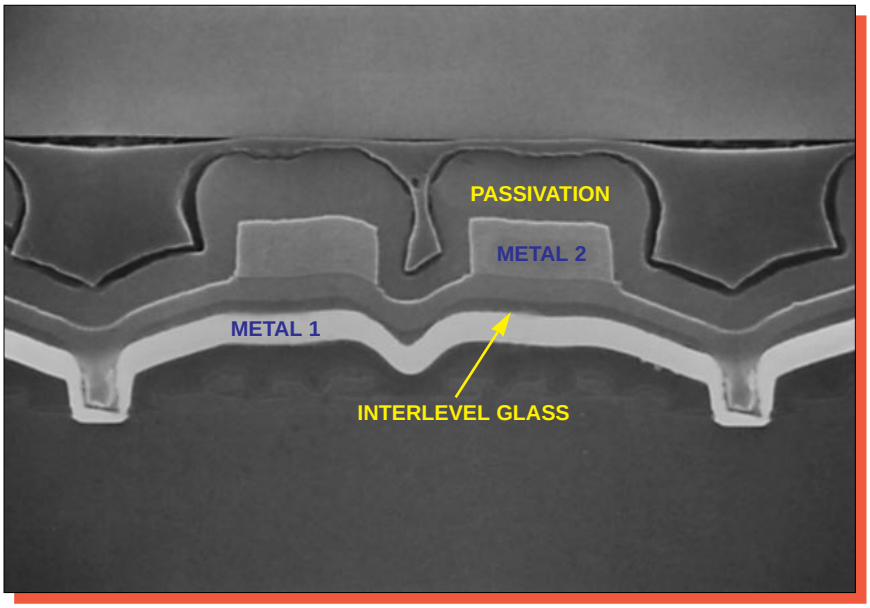


Mag. 40,000x

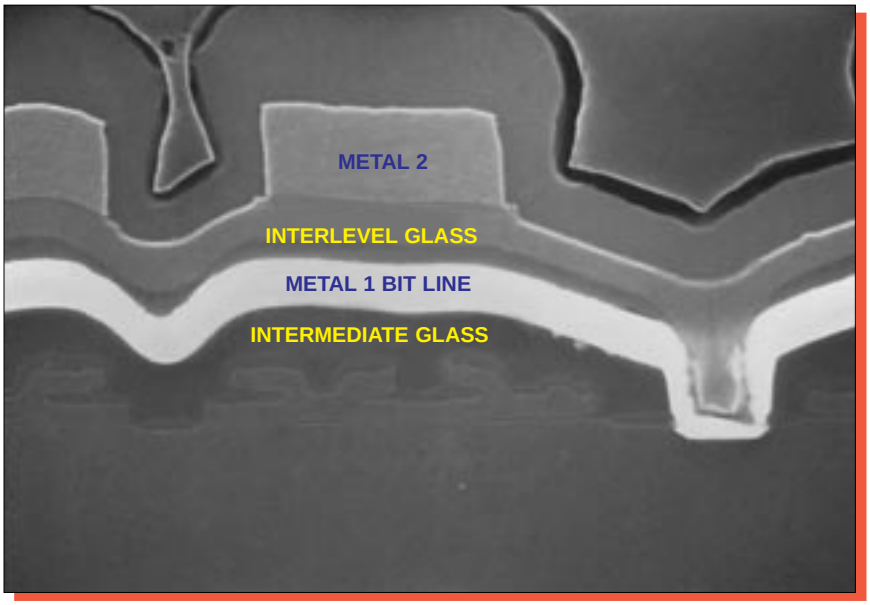


Mag. 40,000x

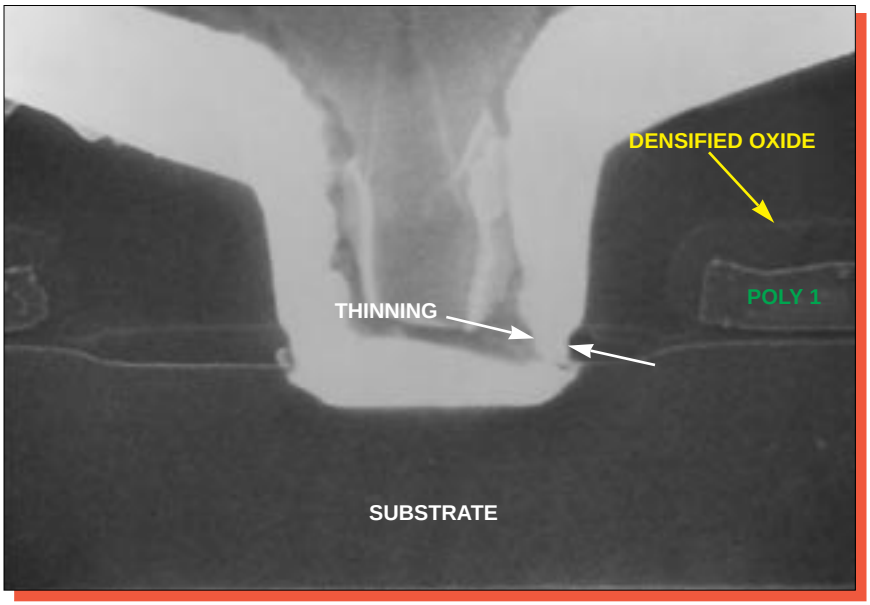
Figure 28a. Detailed SEM section views of an EEPROM cell.



Mag. 6000x

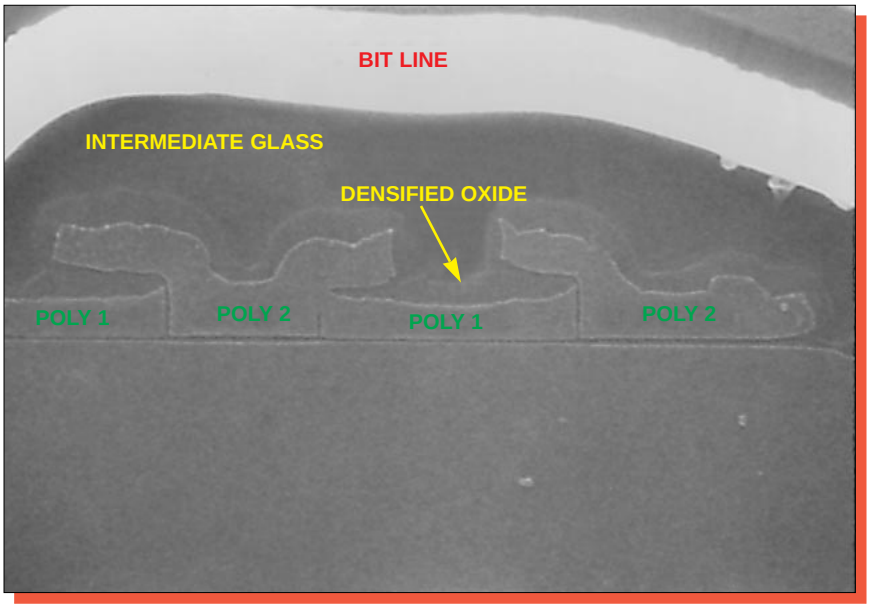


Mag. 10,000x

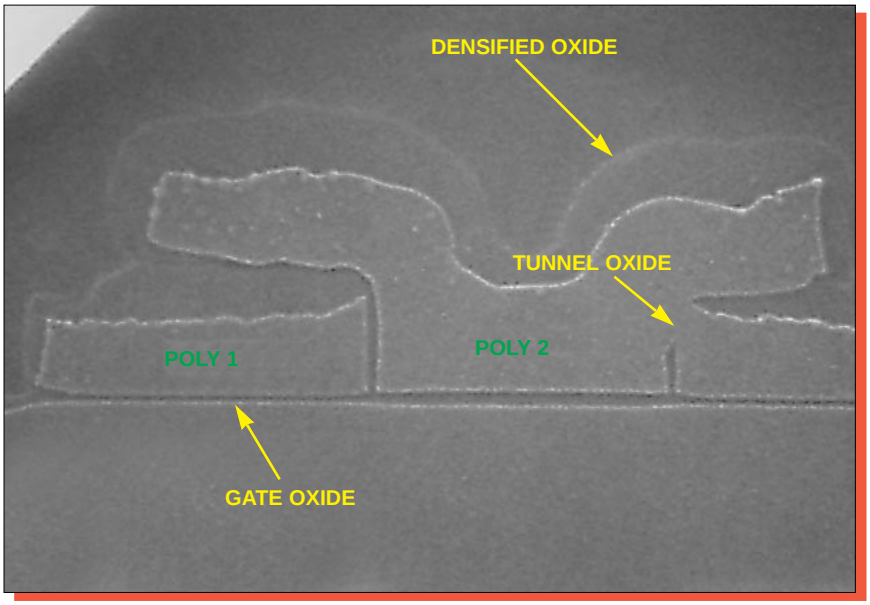


Mag. 30,000x

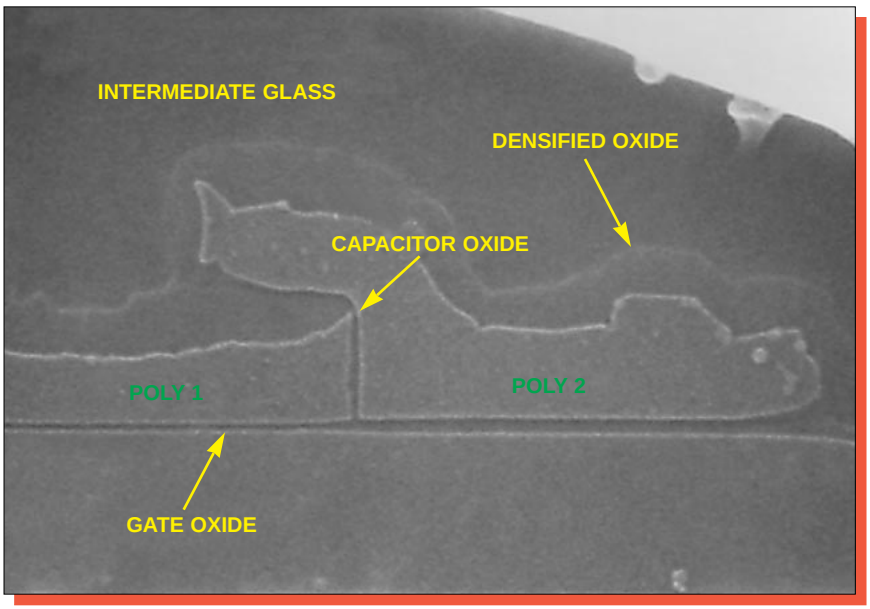
Figure 29. SEM section views of an EEPROM cell. Glass-etch.



Mag. 20,000x

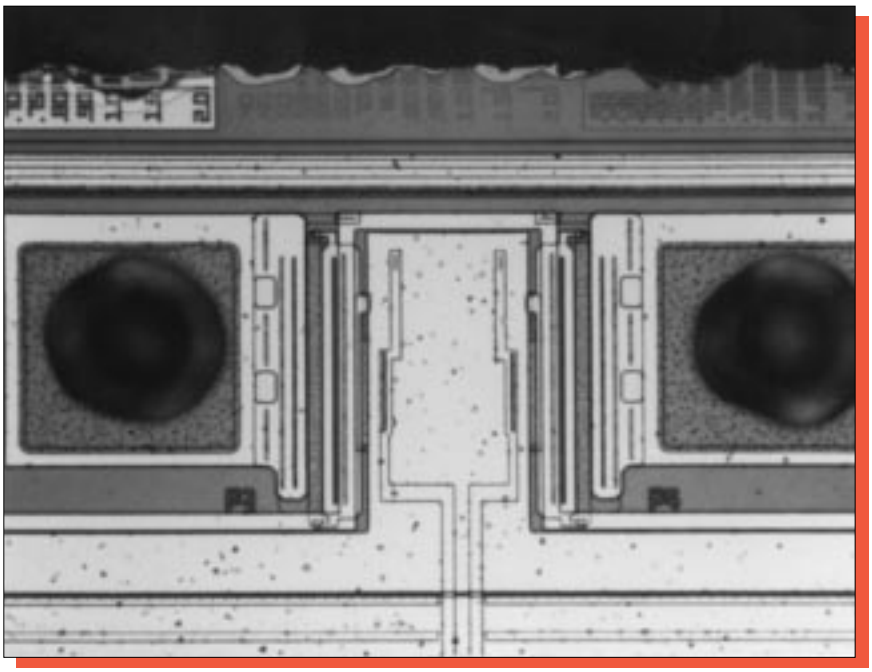


Mag. 40,000x

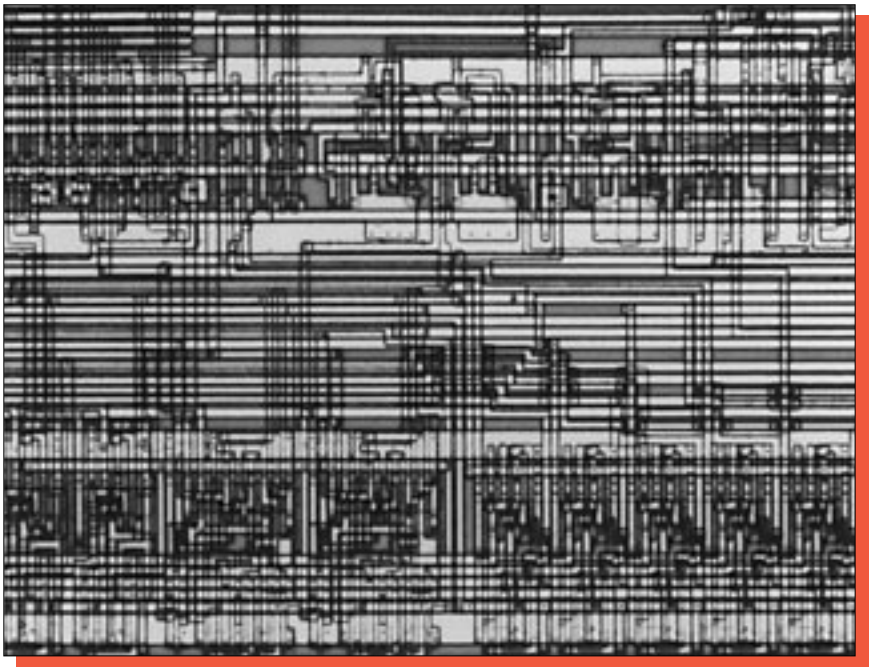


Mag. 40,000x

Figure 29a. Detailed SEM section views of an EEPROM cell. Glass-etch.

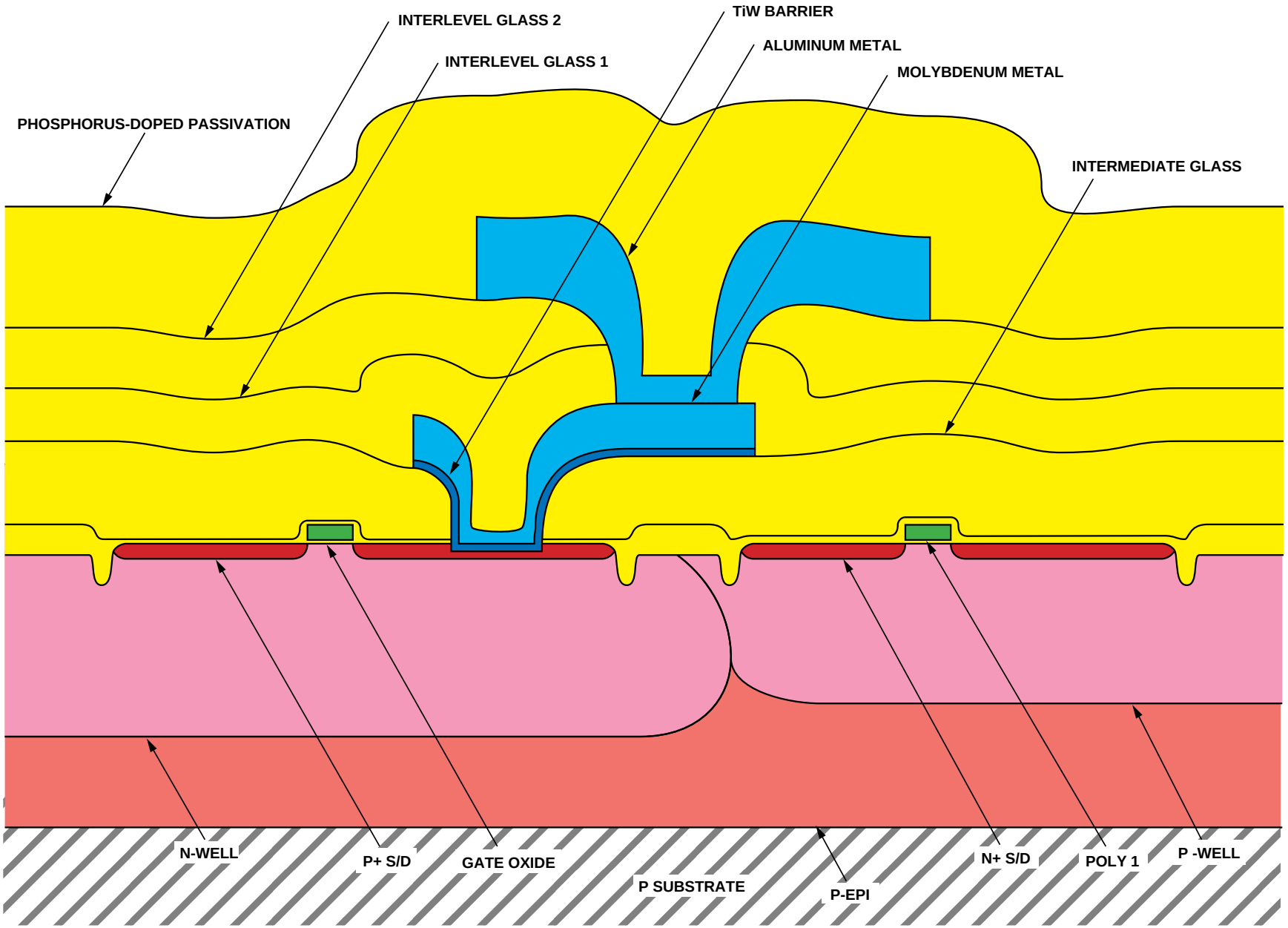


Mag. 200x



Mag. 320x

Figure 30. Optical views of input protection and general device circuitry.



Orange = Nitride, Blue = Metal, Yellow = Oxide, Green = Poly,

Red = Diffusion, and Gray = Substrate

Figure 31. Color cross section drawing illustrating device structure.