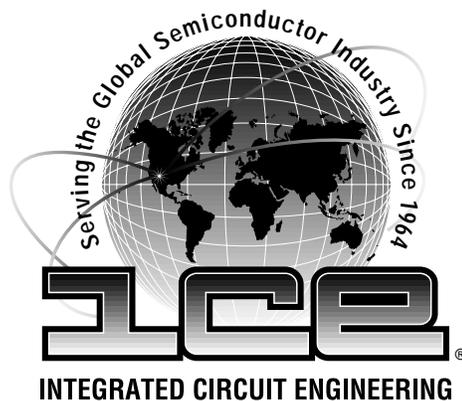


Construction Analysis

Micron Semiconductor MT5C64K16A1DJ 64K x 16 SRAM

Report Number: SCA 9412-394



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INDEX TO TEXT

<u>TITLE</u>	<u>PAGE</u>
INTRODUCTION	1
MAJOR FINDINGS	1
TECHNOLOGY DESCRIPTION	
Assembly	2
Die Process and Design	2 - 3
ANALYSIS RESULTS I	
Assembly	4
ANALYSIS RESULTS II	
Die Process and Design	5 - 7
ANALYSIS PROCEDURE	8
TABLES	
Overall Evaluation	9
Package Markings	10
Wirebond Strength	10
Package Material Analysis	10
Die Material Analysis	11
Horizontal Dimensions	12
Vertical Dimensions	13

INTRODUCTION

This report describes a construction analysis of the Micron Semiconductor MT5C64K16A1DJ-12 64K x 16-bit Static RAM. Six devices packaged in 44-pin SOJ packages were received for the analysis. All samples were date coded 9432.

MAJOR FINDINGS

Questionable Items: None

Special Features:

- Sub-micron gate lengths (0.5 micron N-channel and P-channel) with sidewall spacers (removed on P-channel only).
- Tungsten plugs at metal 1 contacts.
- Twin-well, CMOS LDD process.
- Chemo-mechanical planarization of intermediate oxide.

TECHNOLOGY DESCRIPTION

Assembly:

- The devices were packaged in 44-pin plastic Small Outline J-lead (SOJ) packages for surface mount applications.
- The leadframe was constructed of copper with a trace of iron and plated externally with tin-lead solder.
- Leadframe was plated internally with silver.
- Lead-locking leadframe design (anchors and holes) on all pins. Four pins at each corner of the package had no holes.
- Die separation by sawn dicing (full depth).
- Wirebonding by the thermosonic ball bond method using 1.2 mil gold wire.
- Pins 22, 23 and 28 were not connected.
- Unpatterned polyimide die coat (i.e. over ball bonds).

Die Process

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate. No epi was present.
- Final passivation: A layer of silicon-nitride over multilayered glass.
- Metallization: Two levels of metal defined by dry-etch techniques. Both metal layers consisted of silicon-doped aluminum. Metal 2 employed a titanium-nitride cap. Metal 1 employed a titanium barrier and tungsten plugs.

TECHNOLOGY DESCRIPTION (continued)

- Interlevel dielectric: Interlevel dielectric (between M2 and M1) consisted of two layers of glass. The second layer of glass was multilayered. Both layers were subjected to etchbacks for planarization.
- Intermediate glass: A single layer of BPSG (borophosphosilicate glass) over various densified oxides. This layer was chemo-mechanically planarized.
- Polysilicon: Two layers of polysilicon were employed. Poly 1 was used to form all standard gates on the die. Poly 2 was used exclusively in the array to form pull-up resistors and at bit line contacts.
- Diffusions: Standard implanted N+ and P+ diffusions formed the sources/drains of transistors. Oxide sidewall spacers were used to provide the LDD spacing and were left in place on N-channel devices only.
- Wells: Twin-wells in a P substrate.
- Memory cells: The memory cell consisted of a standard 4T NMOS SRAM cell design. Metal 1 formed the bit lines, metal 2 formed piggyback word lines. Poly 1 formed all word lines/select gates. Selectively-doped poly 2 was used exclusively to form the pull-up resistors in the array and at bit line contacts.
- Fuses: Redundancy fuses were noted. Cutouts in the passivation were present over fuses. Blown fuses were noted.

ANALYSIS RESULTS I

Assembly:

Figures 1 - 8

Questionable Items:¹ None.

Special Features:

- Unpatterned polyimide die coat.

General Items:

- Overall package quality: Good. No significant defects were found on the external or internal portions of the packages. No voids or cracks were noted in the plastic package. External pins were well formed and tinning of the leads was complete. Very small gaps were noted at lead exits, but they did not extend far into the package. Internal silver plating was of good quality and well centered.
- Wirebonding: Thermosonic ball bond method using 1.2 mil gold wire. Bonds were well formed and placement was good. Good intermetallic formation was found at the ball bonds. All bond pull strengths were normal and no bond lifts occurred (see page 10). The leadframe was partially etched during acid decapsulation.
- Die attach: An adequate amount of silver-filled epoxy. No voids were found.
- Die dicing: Die separation was by sawing (full depth) and showed normal quality workmanship. No large chips or cracks were present at the die surface.
- Die coat: An unpatterned (over ball bonds) polyimide die coat was present over the entire die surface. Die coat thickness was minimal at the die perimeter.

¹These items present possible quality or reliability concerns. They should be discussed with the manufacturer to determine their possible impact on the intended application.

ANALYSIS RESULTS II

Die Process and Design:

Figures 9 - 36

Questionable Items: None

Special Features:

- Twin-well, CMOS, LDD process.
- Tungsten plugs at metal 1 contacts.
- Sub-micron gate lengths (0.5 micron N-channel and P-channel) with sidewall spacers removed on P-channel only).

General Items:

- Fabrication process: Selective oxidation CMOS process employing twin-wells in a P substrate (no epi). No significant problems were found in the basic process.
- Design implementation: Die layout was clean and efficient. Alignment was good at all levels.
- Surface defects: No toolmarks, masking defects, or contamination areas were found.
- Final passivation: A layer of silicon-nitride over multilayered glass. A passivation integrity test indicated defect-free passivation. Edge seal was also good. (An unpatterned polyimide die coat was used on these dice over the passivation).
- Metallization: Two levels of metallization. Both metals consisted of silicon-doped aluminum. Metal 2 employed a titanium-nitride cap. Metal 1 employed a titanium barrier with tungsten plugs.
- Metal patterning: Both metal layers were defined by a dry etch of good quality.

ANALYSIS RESULTS II (continued)

- Metal defects: No notching or voiding of either metal layer was found. No silicon nodules were found following the removal of either aluminum layer. EDX analysis detected the presence of silicon in the metal layers.
- Metal step coverage: Typical metal 2 aluminum thinning did not exceed 45 percent at vias. Metal 2 lines widened at vias. There was virtually no metal 1 thinning due to the presence of the tungsten plugs. No significant thinning was noted outside of contacts.
- Vias and contacts: Via cuts were slope-etched and metal 1 contacts (plugs) were dry-etched. Minimal over-etching of the contacts was present, but does not create a problem.
- Interlevel dielectric: Interlevel dielectric consisted of two layers of glass. The second layer of glass was multi-layered. Both layers were subjected to etchbacks. No problems were found with these layers.
- Intermediate glass: A layer of BPSG over various densified oxides. This layer was chemo-mechanically planarized (CMP). No problems were found.
- Polysilicon: Two layers of standard polysilicon were employed. Poly 1 was used to form all standard gates on the die and the word lines in the array. Selectively-doped poly 2 was used exclusively in the array to form pull-up resistors and at bit line contacts.
- Isolation: Local oxide (LOCOS). No problems were present at the birdsbeaks or elsewhere.
- Diffusions: Implanted N⁺ and P⁺ diffusions were used for sources and drains. An LDD process was used with oxide sidewall spacers removed on P-channel devices only. No problems were found in any of these areas.
- Wells: Twin-wells were used in a P substrate (no epi). Definition was normal. No step was present in the oxide, however it does appear that twin-wells were used.

ANALYSIS RESULTS II (continued)

- Buried contacts: Interpoly/buried contacts were used in the cell array only.
- Memory cells: The memory cell consisted of a standard 4T NMOS SRAM cell design. Metal 1 formed the bit lines. Metal 2 formed piggyback word lines. Poly 1 formed all word lines/select gates. Poly 2 was used exclusively to form pull-up resistors (selectively doped) in the array, and at metal 1 bit line contacts. Cell pitch was 4.3 x 7.6 microns

Special Items:

- ESD: In process.
- Latch-up: In process.

PROCEDURE

The devices were subjected to the following analysis procedures:

External inspection

ESD sensitivity tests

Latch-up tests

X-ray

Package section and material analysis

Decapsulate

Internal optical inspection

SEM inspection of assembly features and passivation

Wirepull test

Passivation integrity test

Delayer to metal 2 and inspect

Aluminum removal (metal 2), inspect vias

Delayer to metal 1 and inspect

Aluminum removal (metal 1), inspect

Delayer to poly/substrate and inspect poly and substrate

Die sectioning (90° for SEM)*

Die material analysis

Measure horizontal dimensions

Measure vertical dimensions

**Delineation of cross-sections is by silicon etch unless otherwise indicated.*

OVERALL QUALITY EVALUATION: Overall Rating: Good

DETAIL OF EVALUATION

Package integrity	G
Package markings	G
Die placement	G
Wirebond placement	G
Wire spacing	G
Wirebond quality	G
Die attach quality	N
Dicing quality	N
Die attach method	Silver-filled epoxy
Dicing method:	Sawn (full depth)
Wirebond method:	Thermosonic ball bonds using 1.2 mil gold wire.
Die surface integrity:	
Toolmarks (absence)	G
Particles (absence)	G
Contamination (absence)	G
Process defects (absence)	G
General workmanship	G
Passivation integrity	G
Metal definition	N
Metal integrity	G
Metal registration	N
Contact coverage	G
Contact registration	G

G = Good, P = Poor, N = Normal, NP = Normal/Poor

PACKAGE MARKINGS

TOP

9432 A USA
MT5C64K16A1DJ
-12
72QY

BOTTOM

72QY

WIREBOND STRENGTH

Wire material: 1.2 mil diameter gold

Die pad material: aluminum

Material at package lands: silver

# of wires pulled:	26
Bond lifts:	0
Force to break - high:	14.5g
- low:	11.5g
- avg.:	13.3g
- std. dev.:	0.9

PACKAGE MATERIAL ANALYSIS (EDX)

Leadframe:	Copper (Cu) with a trace of Iron (Fe)
External pin plating:	Tin-lead (SnPb) solder
Internal plating:	Silver (Ag)
Die attach:	Silver (Ag)-filled epoxy

DIE MATERIAL ANALYSIS (EDX and WDX)

Overlay passivation:	Silicon-nitride [†] over multilayered glass.
Metallization 2:	Silicon-doped aluminum with a titanium-nitride cap.
Interlevel dielectric 1 (M2 to M1):	Two layers of silicon-dioxide.
Metallization 1:	Silicon-doped aluminum with a titanium barrier and tungsten plugs.
Intermediate glass: [†]	BPSG containing 3.5 wt. percent boron and 6.3 wt. percent phosphorus over grown/densified oxides.

[†] WDX analysis.

VERTICAL DIMENSIONS

Die thickness: 0.47 mm (18.5 mils)

Layers

Passivation:

- nitride: 0.7 micron

- glass: 0.7 micron

Metal 2 - cap: 0.04 micron (approximate)

- aluminum: 1.2 micron

Interlevel glass 2: 0.4 micron

- glass 1: 0.25 micron

Metal - aluminum: 0.6 micron

- barrier: 0.09 micron (approximate)

Intermediate glass: 0.6 to 1.1 micron

Poly 2: 0.08 micron (approximate)

Interpoly oxide: 0.15 micron

Poly 1: 0.35 micron

Local oxide : 0.55 micron

N+ S/D diffusion: 0.2 micron

P+ S/D diffusion: 0.25 micron

N- well: 6.3 microns

P- well: 4.7 microns

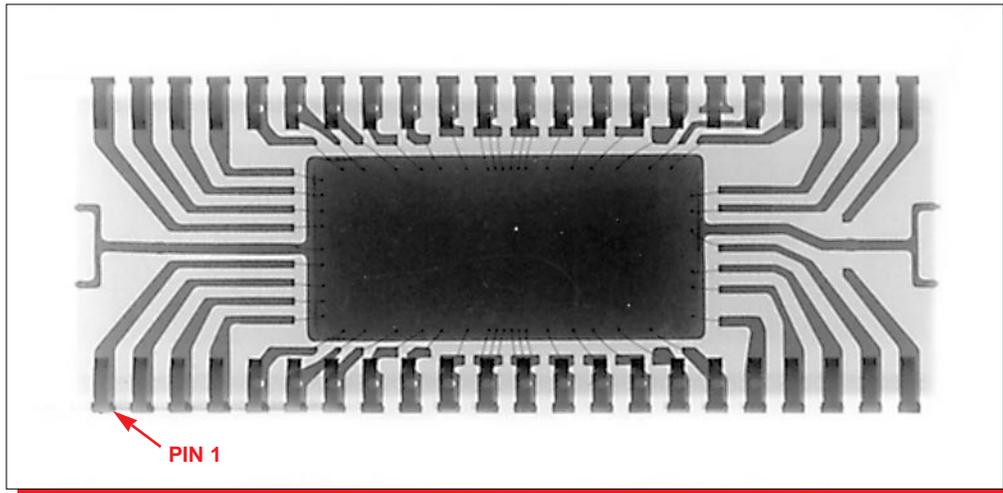
INDEX TO FIGURES

ASSEMBLY	Figures 1 - 8
DIE LAYOUT AND IDENTIFICATION	Figures 9 - 10
PHYSICAL DIE STRUCTURES	Figures 11 - 34
MEMORY CELL STRUCTURES	Figures 29 - 34
CIRCUIT LAYOUT AND INPUT PROTECTION	Figure 35
COLOR DRAWING OF DIE STRUCTURE	Figure 36

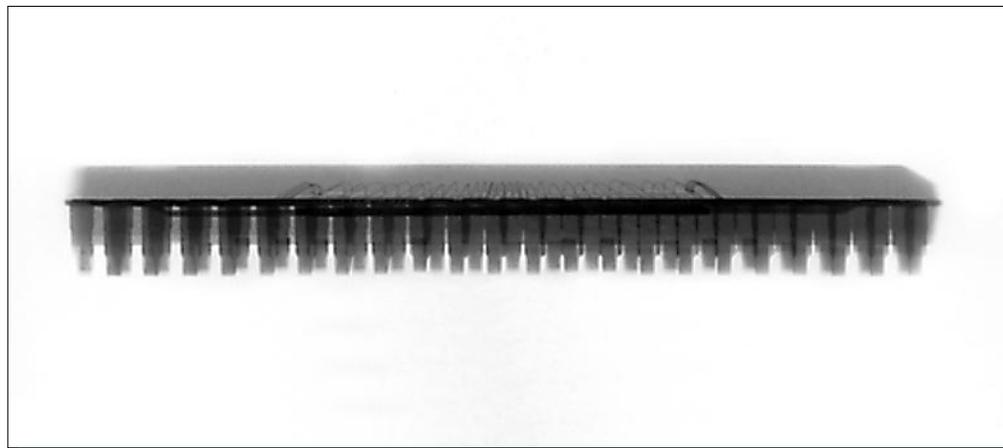


A4	1	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	OE
A0	5	40	BHE
CE	6	39	BLE
DQ1	7	38	DQ16
DQ2	8	37	DQ15
DQ3	9	36	DQ14
DQ4	10	35	DQ13
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
DQ5	13	32	DQ12
DQ6	14	31	DQ11
DQ7	15	30	DQ10
DQ8	16	29	DQ9
WE	17	28	N.C.
A15	18	27	A8
A14	19	26	A9
A13	20	25	A10
A12	21	24	A11
N.C.	22	23	N.C.

Figure 1. Package photograph and pinout of the Micron Semiconductor MT5C64K16A1 64K x 16 SRAM. Mag. 3x.

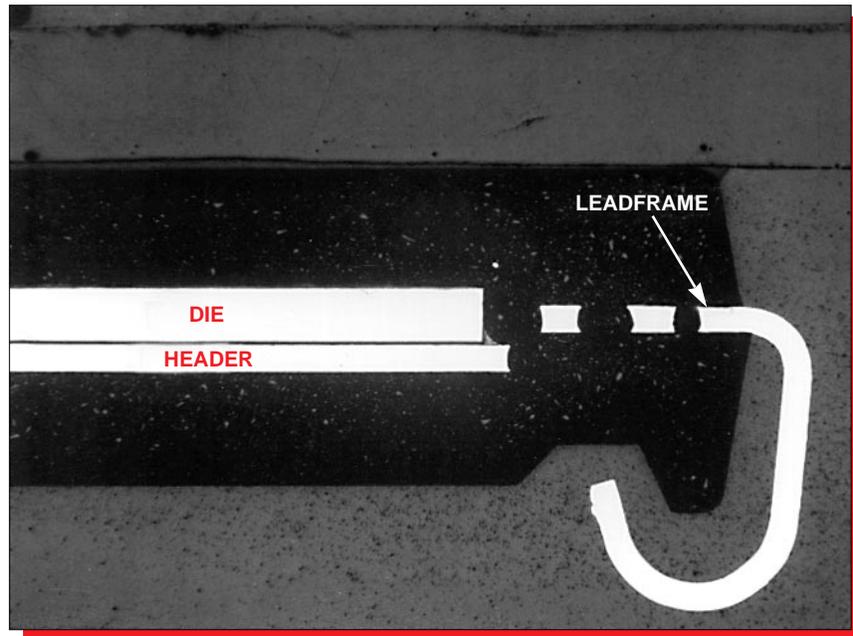


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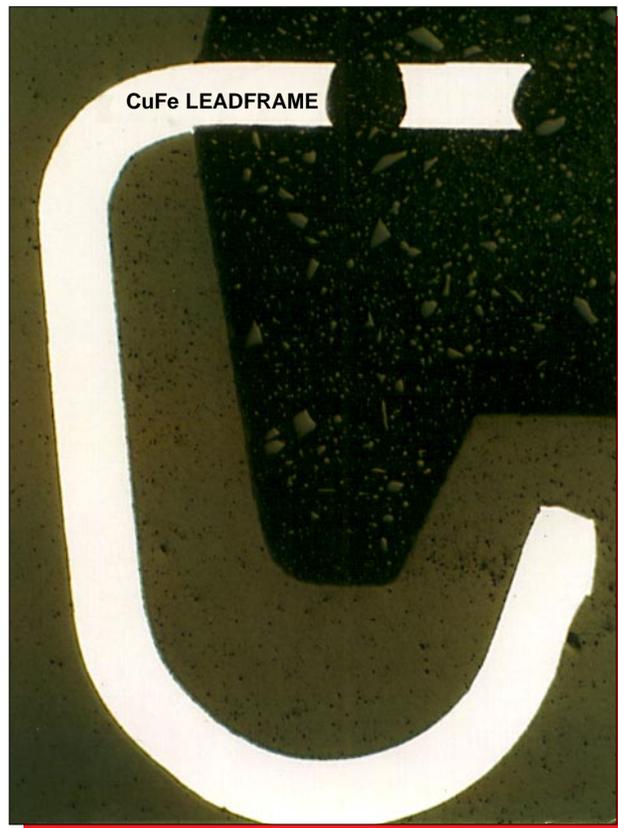


side

Figure 2. X-ray views of the package. Mag. 5x.

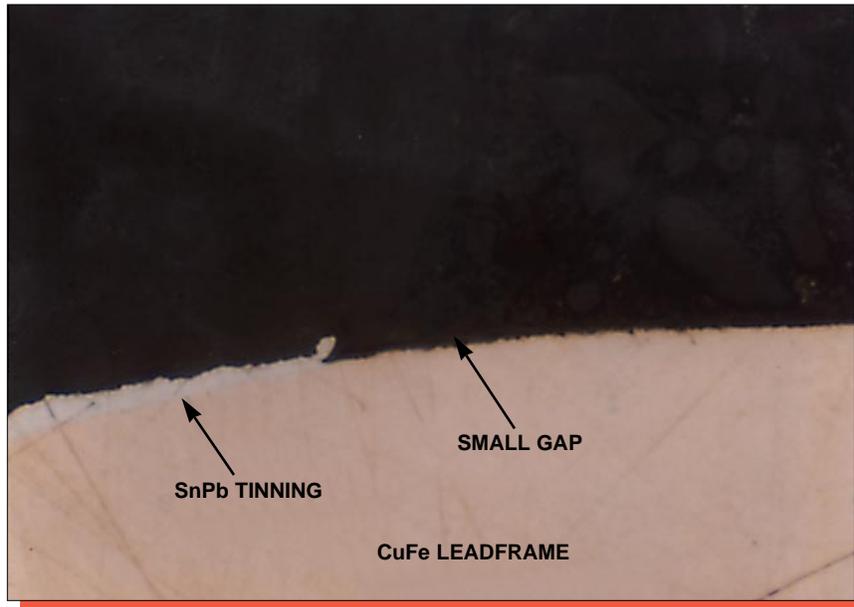


Mag. 16x

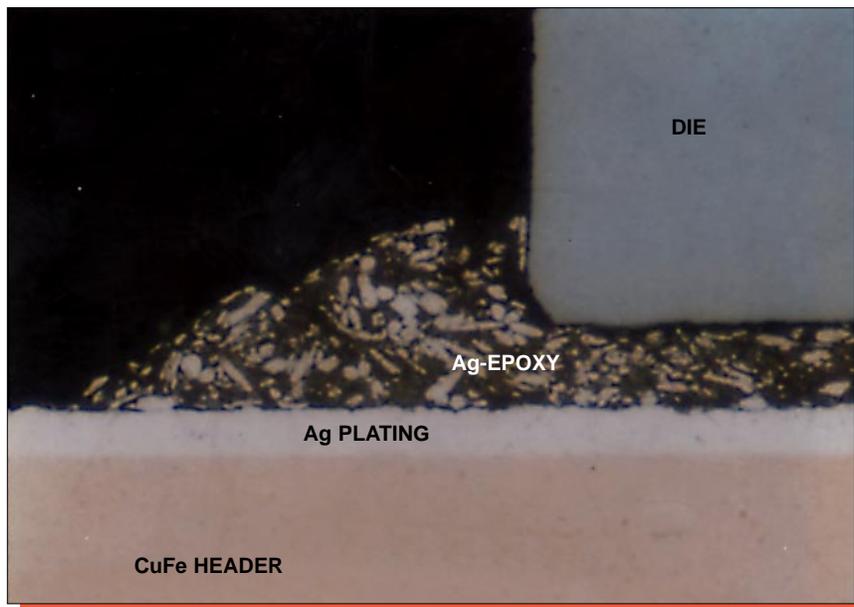


Mag. 40x

Figure 3. Package section views of general package construction and lead forming.

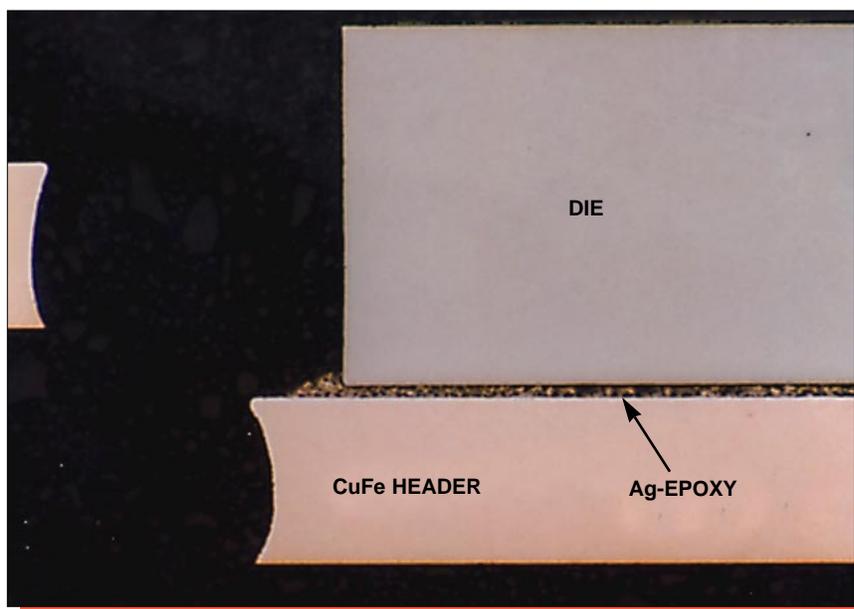


Mag. 500x

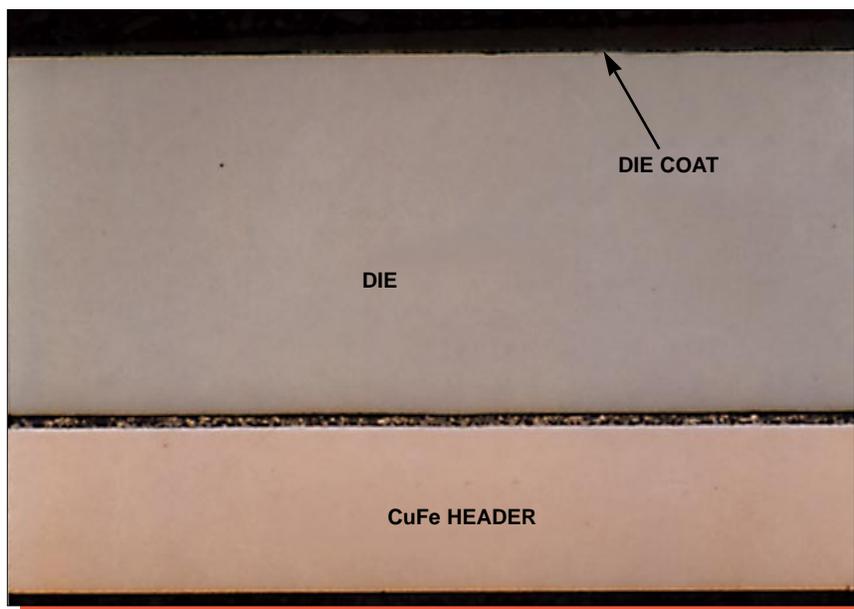


Mag. 800x

Figure 4. Package section views of lead exit and die attach.

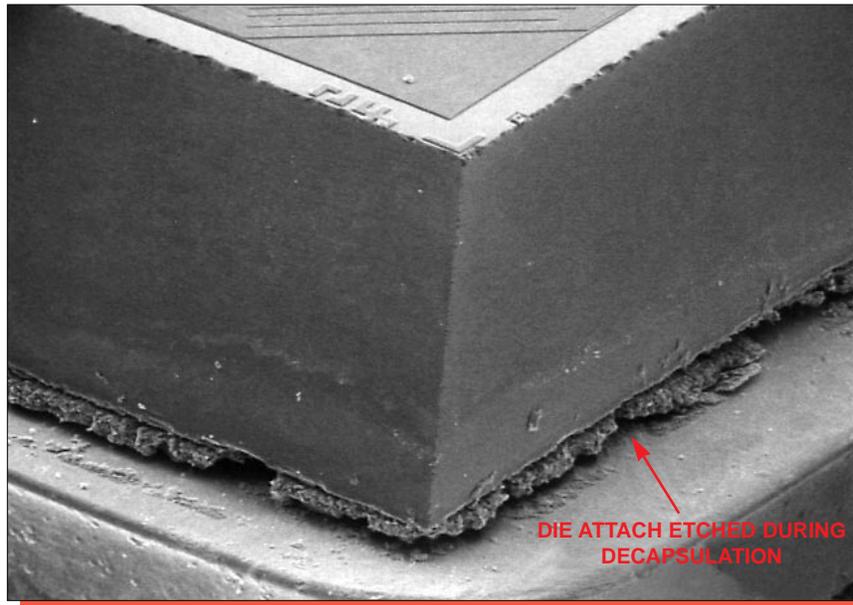


Mag. 100x

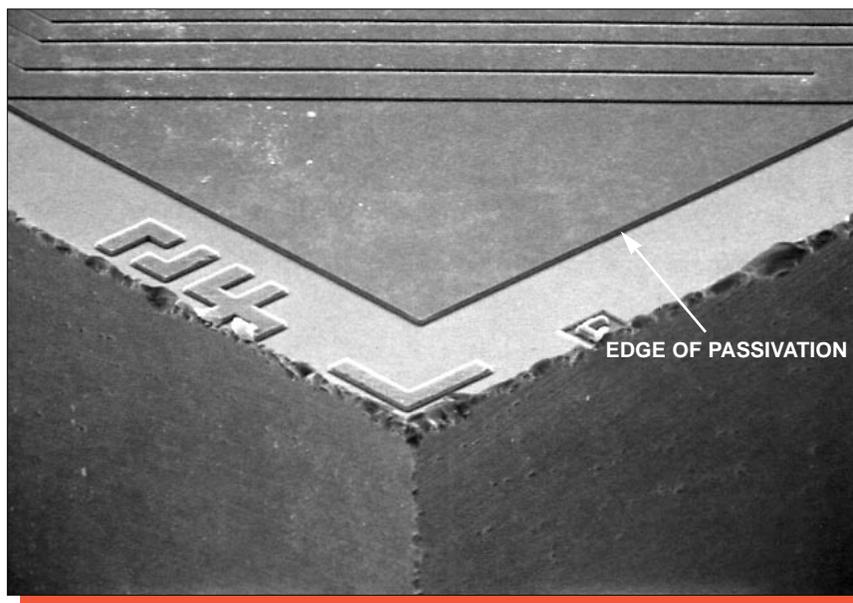


Mag. 400x

Figure 5. Package section views of dicing and die coat.



Mag. 120x



Mag. 300x

Figure 6. SEM views of dicing, die attach and edge seal. 60°.

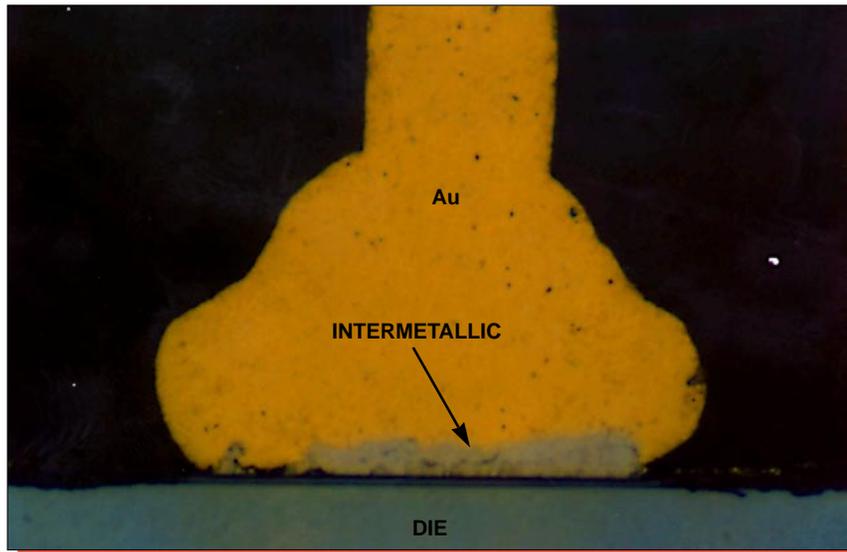
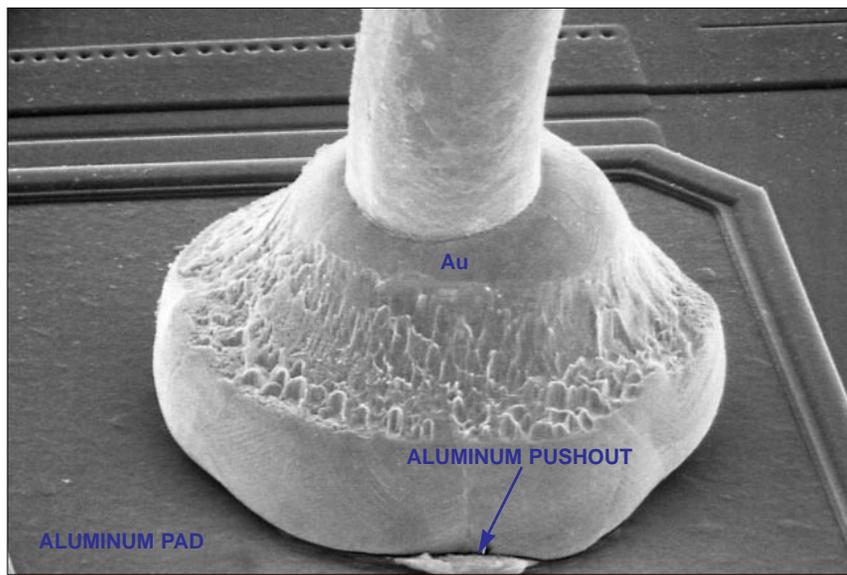
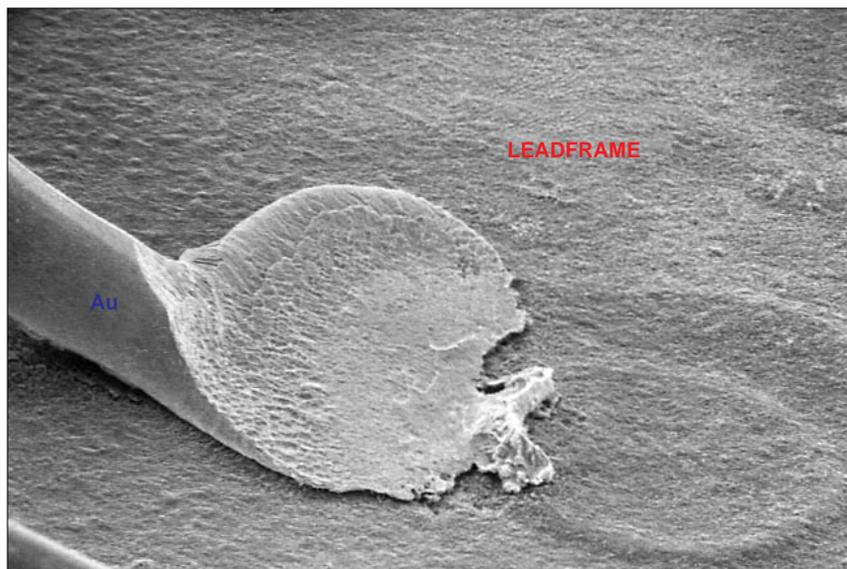


Figure 7. Package section view of a typical ball bond. Mag. 800x.



Mag. 850x



Mag. 575x

Figure 8. SEM views of typical wirebonds. 60°.

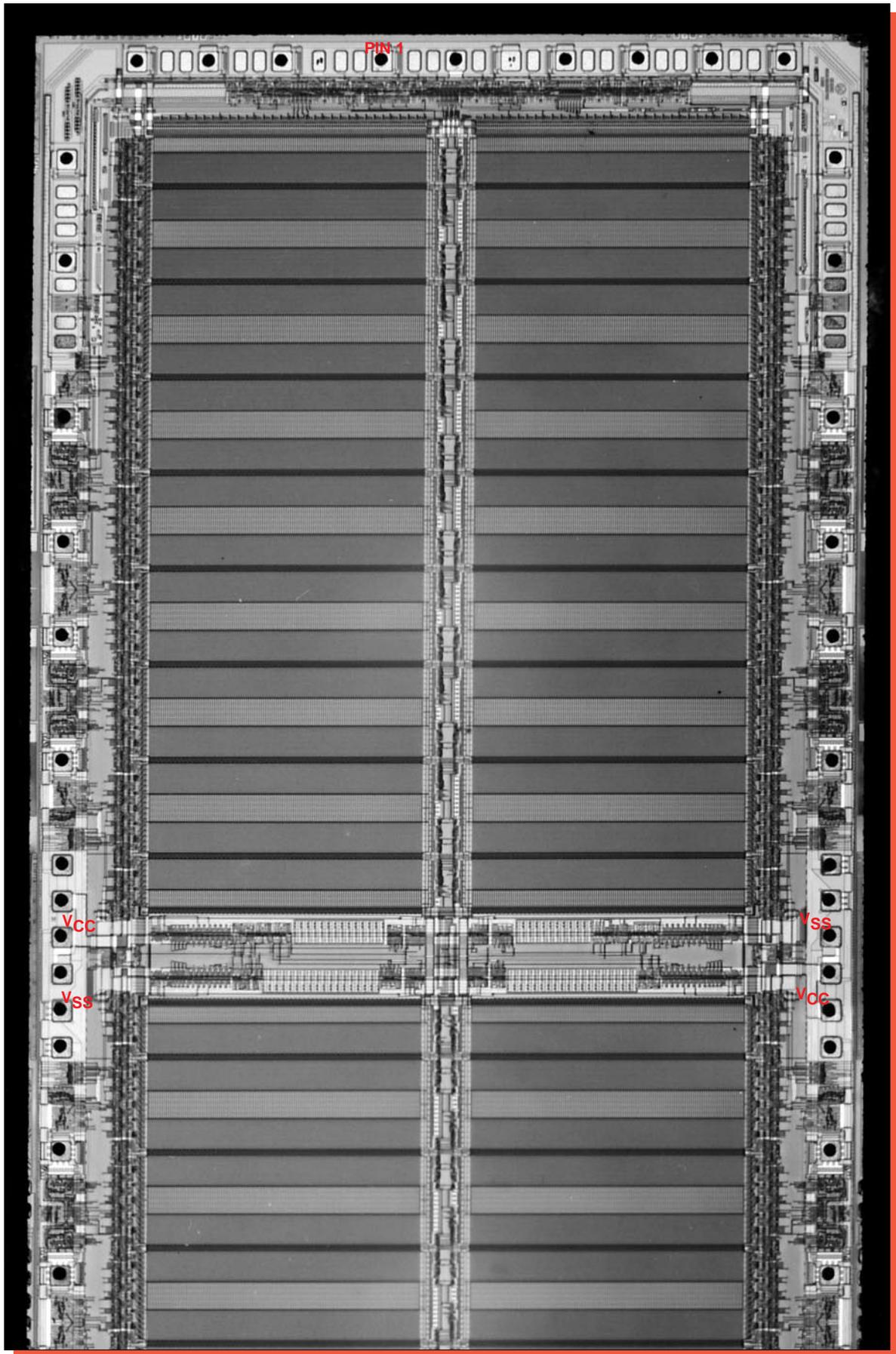


Figure 9. Portion of the Micron Semiconductor MT5C64K16A1 64K x 16 SRAM. Mag. 26x.

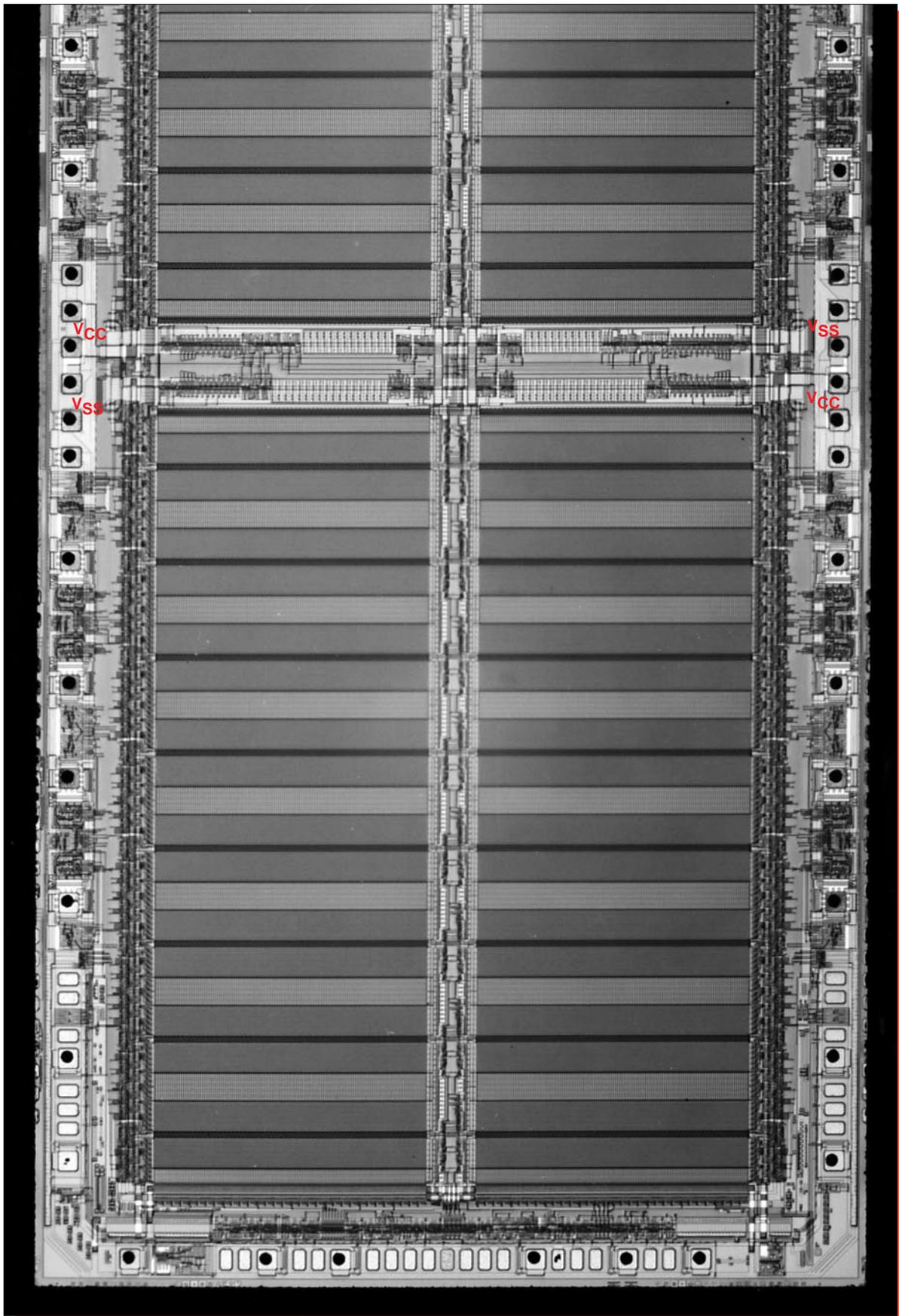
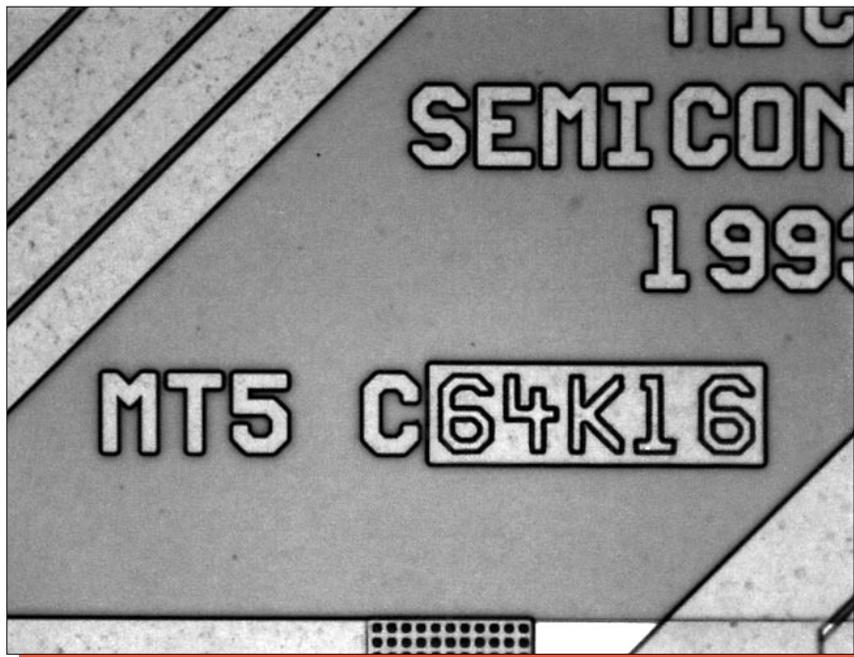


Figure 9a. Remaining portion of the Micron Semiconductor MT5C64K26A1 64K x 16 SRAM. Mag. 26x.

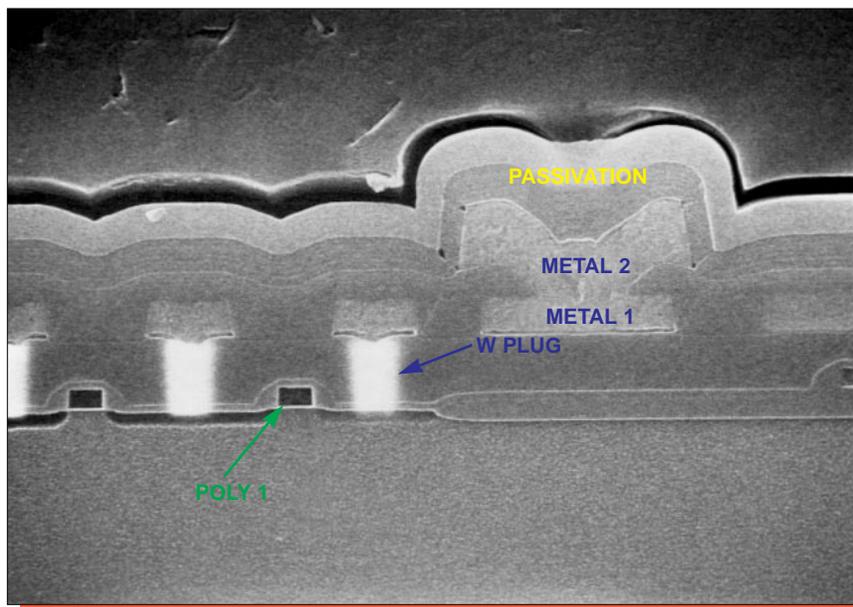


Mag. 400x

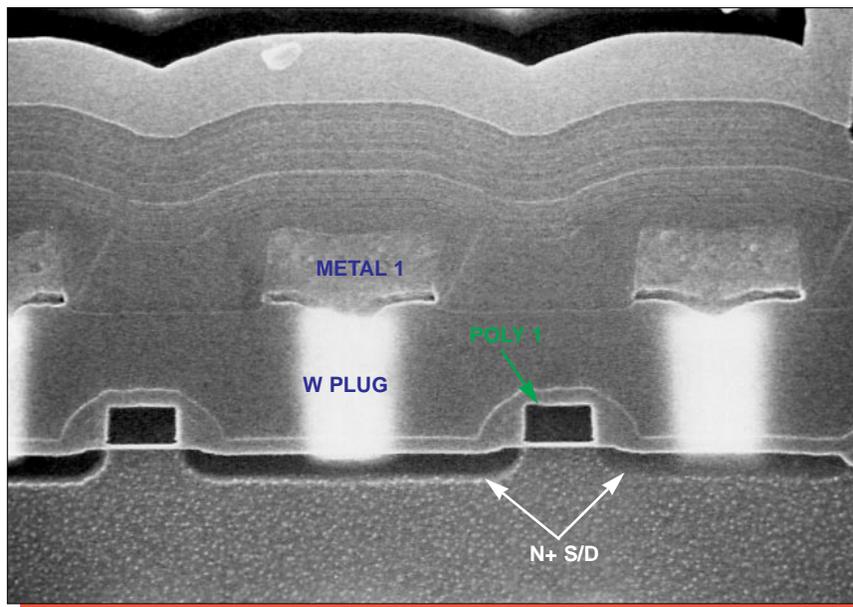


Mag. 500x

Figure 10. Markings from the die surface.

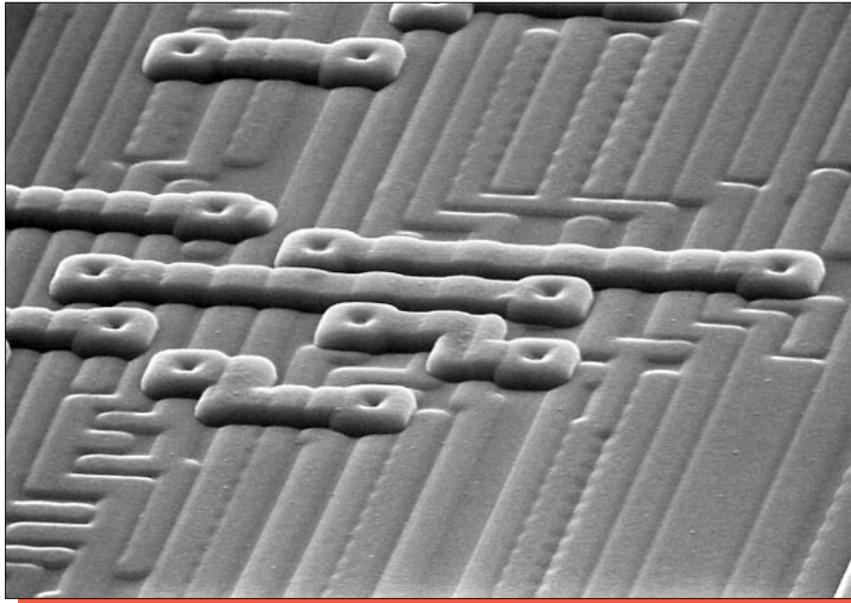


Mag. 7000x

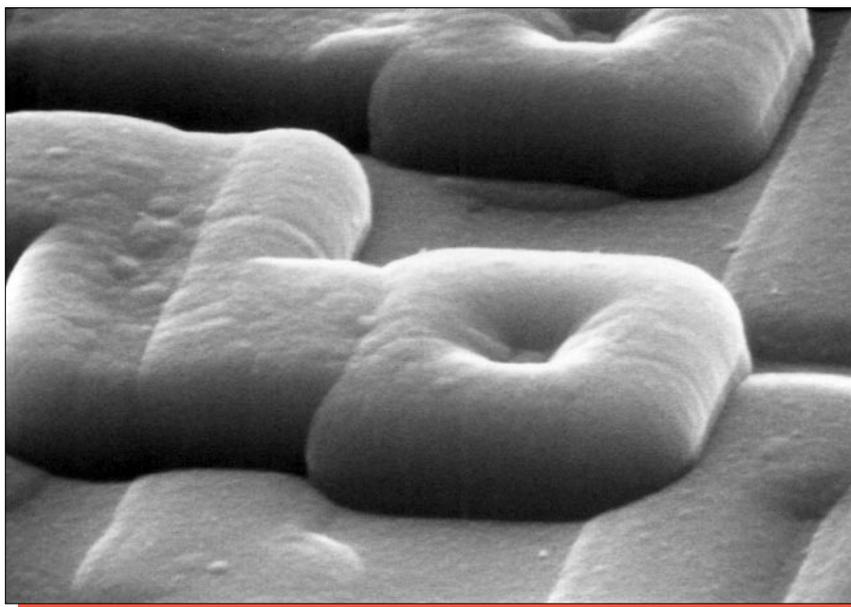


Mag. 14,000x

Figure 11. SEM section views of general die construction.



Mag. 1800x



Mag. 9200x

Figure 12. SEM views of overlay passivation coverage. 60°.

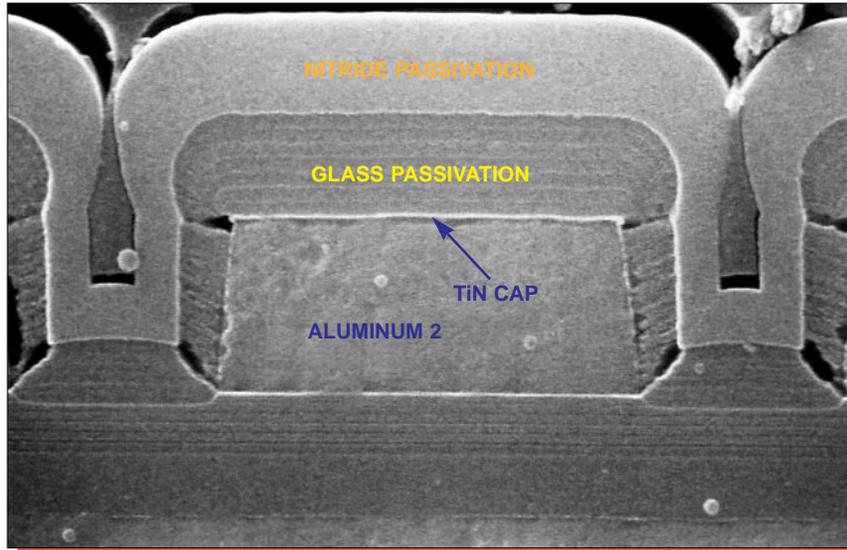
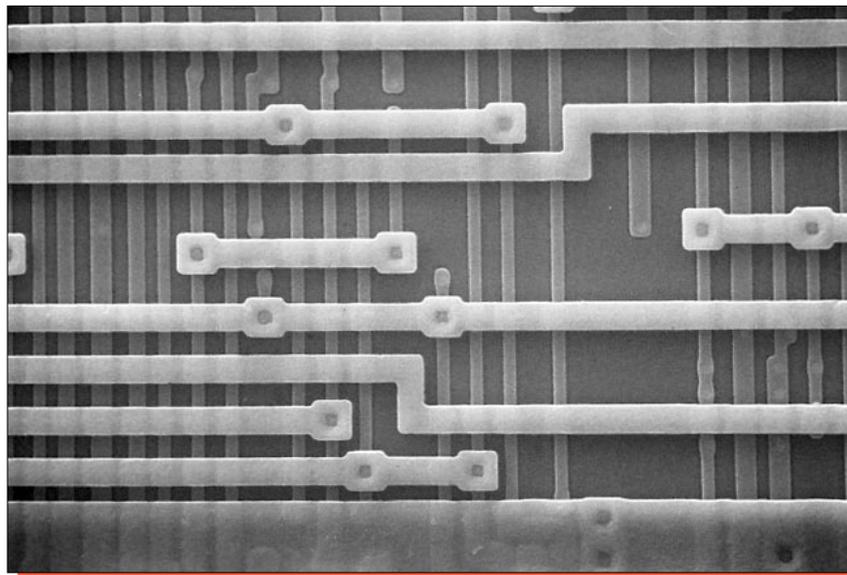
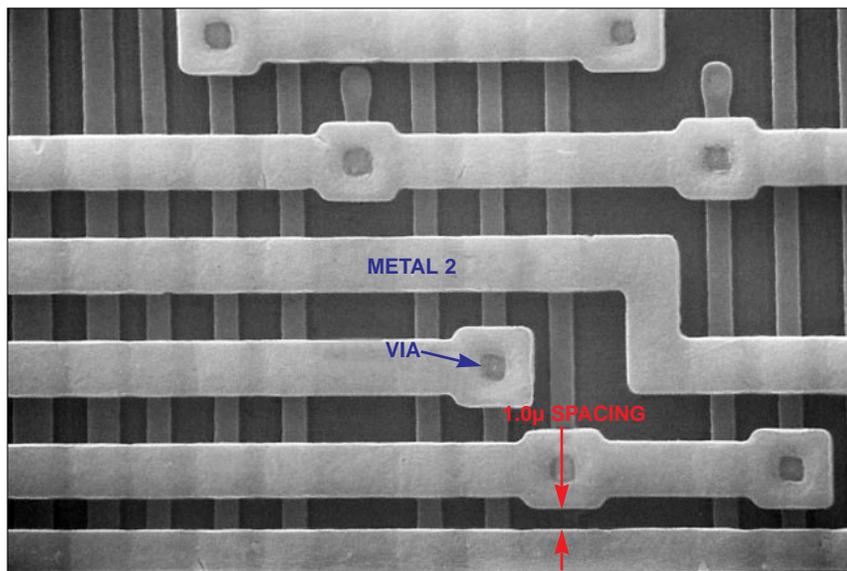


Figure 13. SEM section view of a metal 2 line profile. Mag. 20,000x.

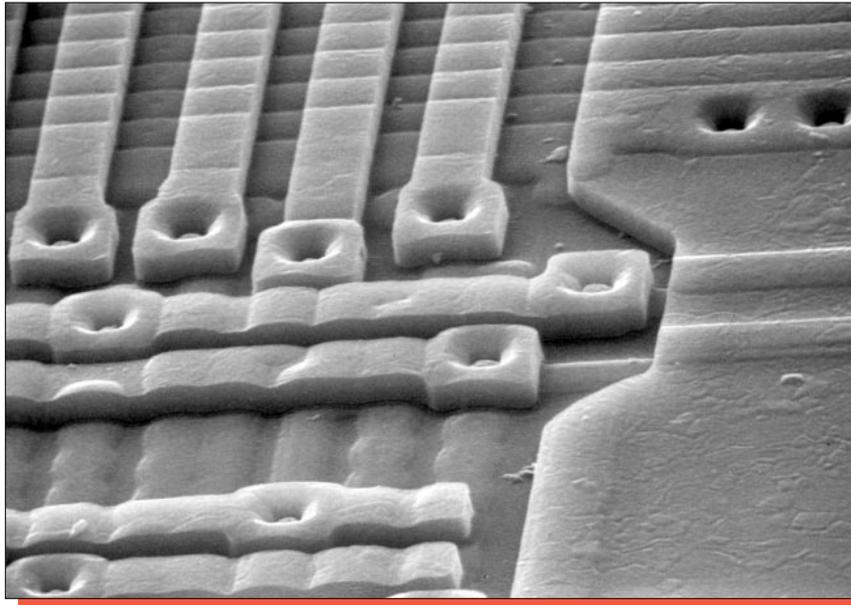


Mag. 1300x

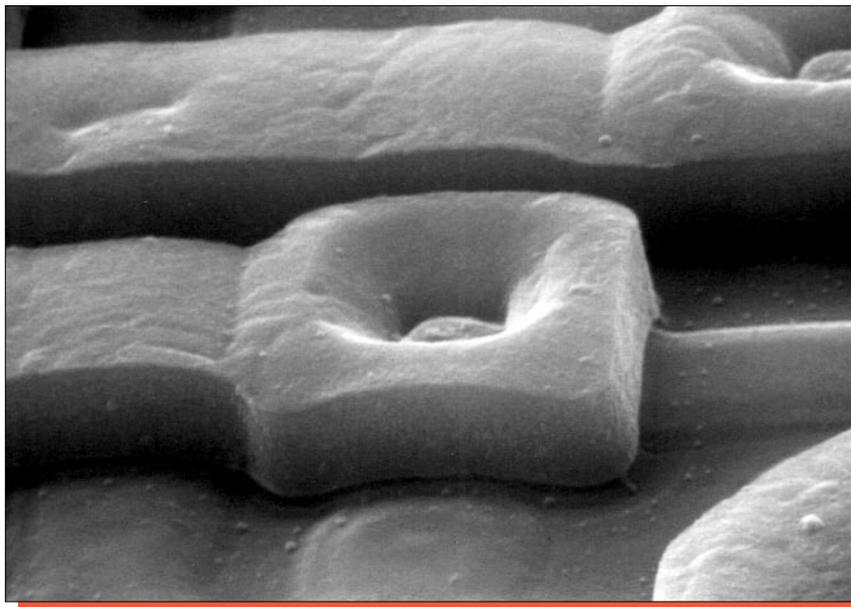


Mag. 2600x

Figure 14. Topological SEM views of metal 2 patterning. 0°.



Mag. 3400x



Mag. 12,000x

Figure 15. SEM views of metal 2 coverage. 60°.

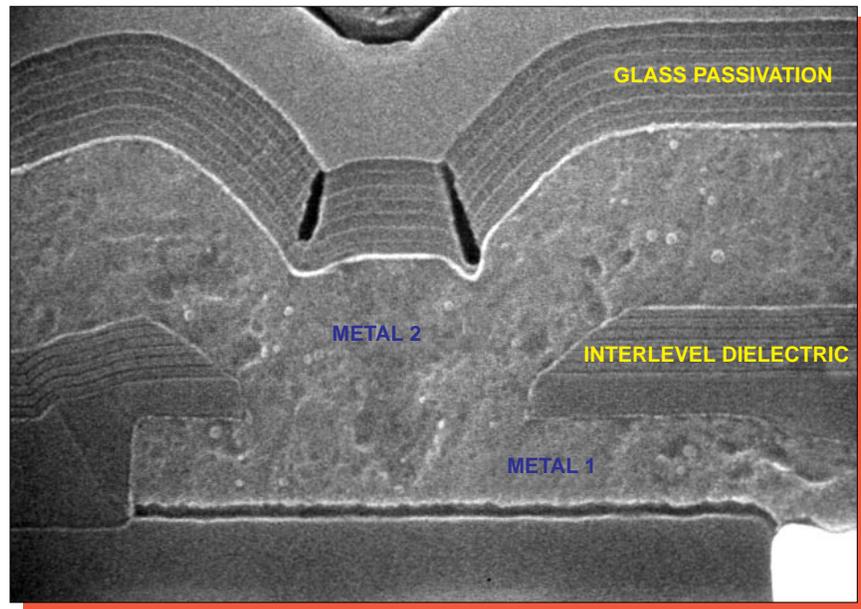


Figure 16. SEM section view of a metal 2-to-metal 1 via. Mag. 20,000x.

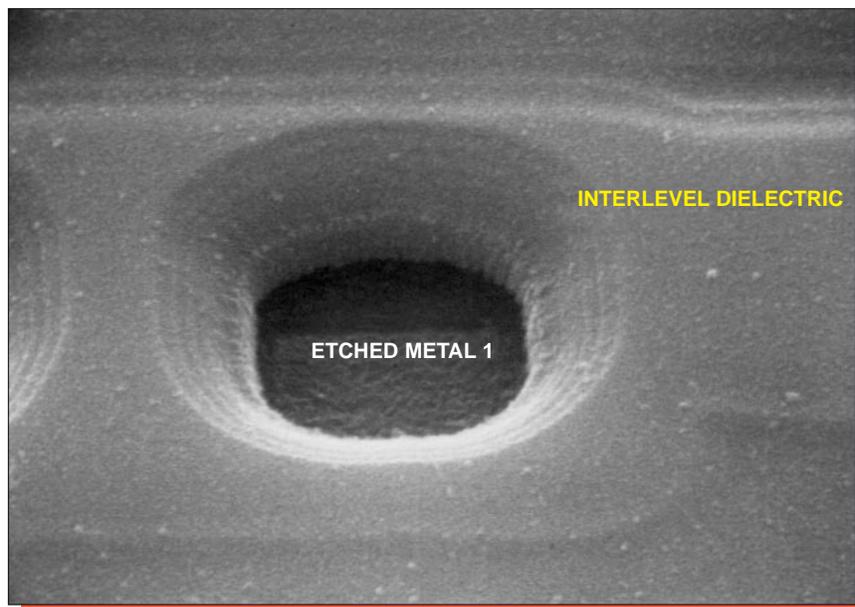


Figure 17. SEM view of a metal 2-to-metal 1 via following removal of metal 2.
Mag. 18,300x, 45°.

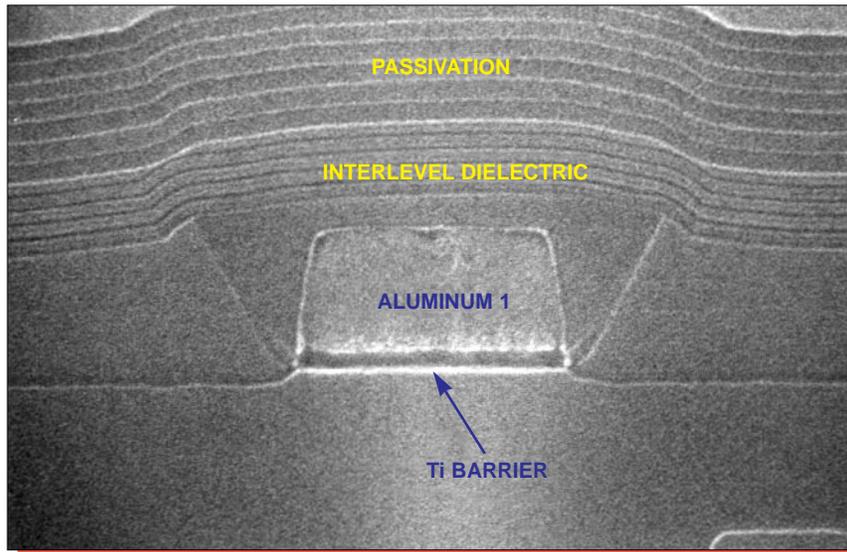
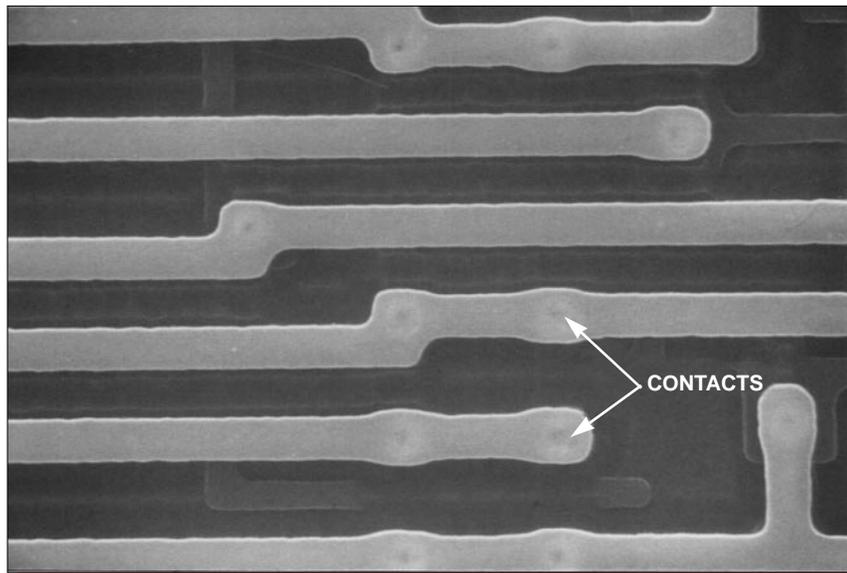
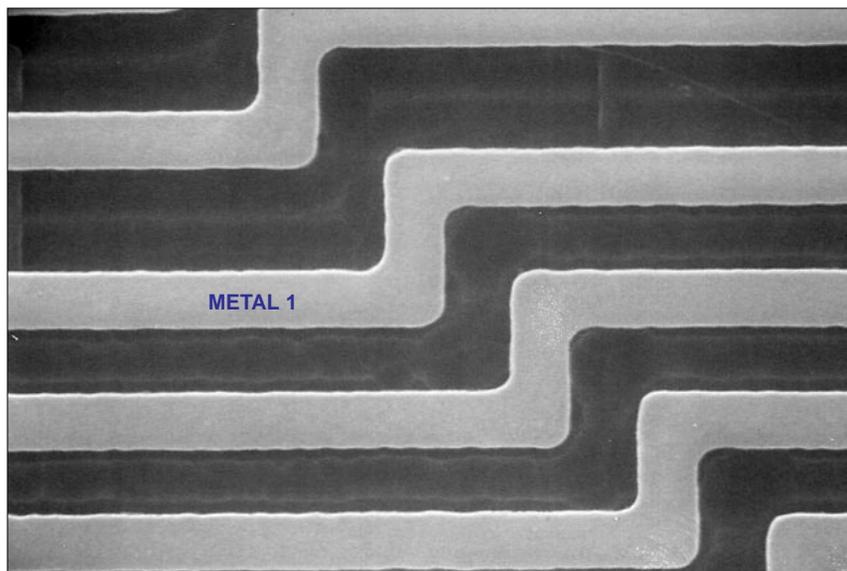


Figure 18. SEM section view of a metal 1 line profile. Mag. 28,000x.

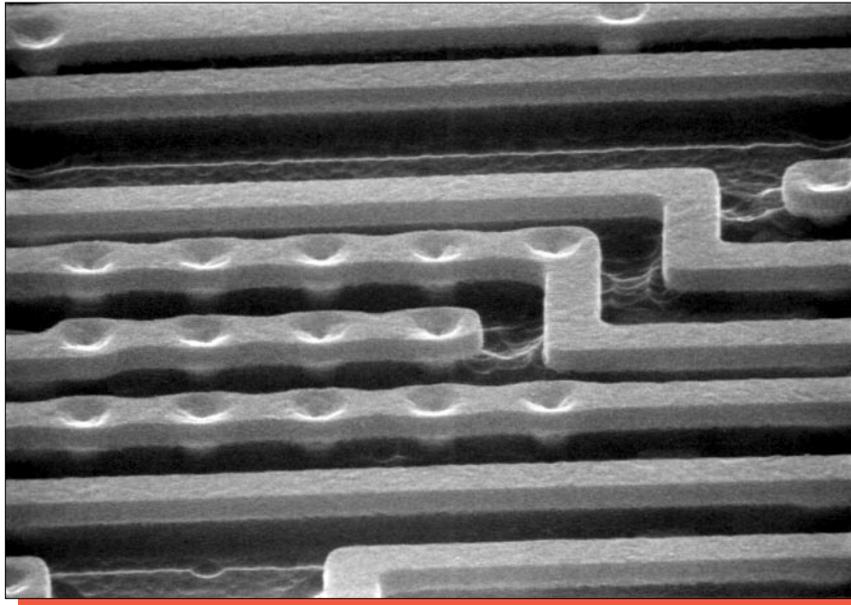


Mag. 4800x

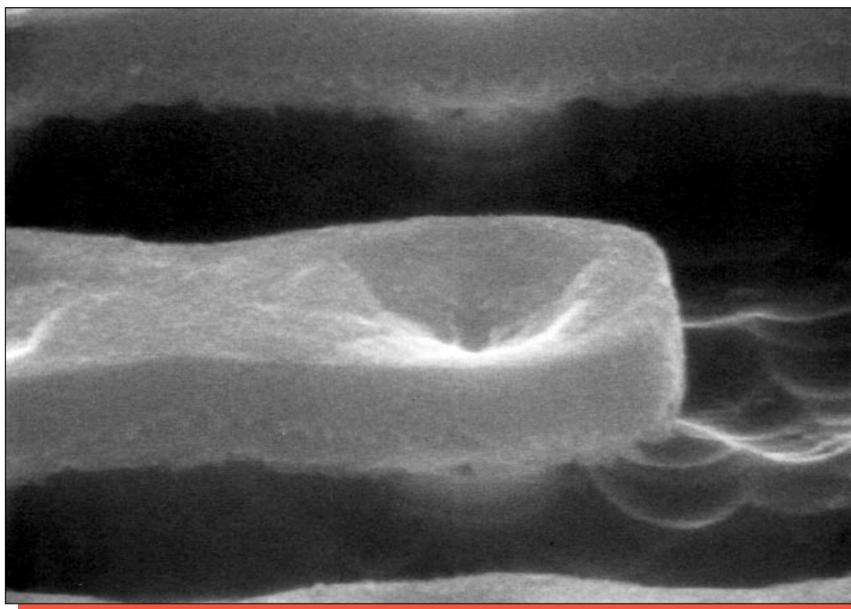


Mag. 6200x

Figure 19. Topological SEM views of metal 1 patterning. 0°.

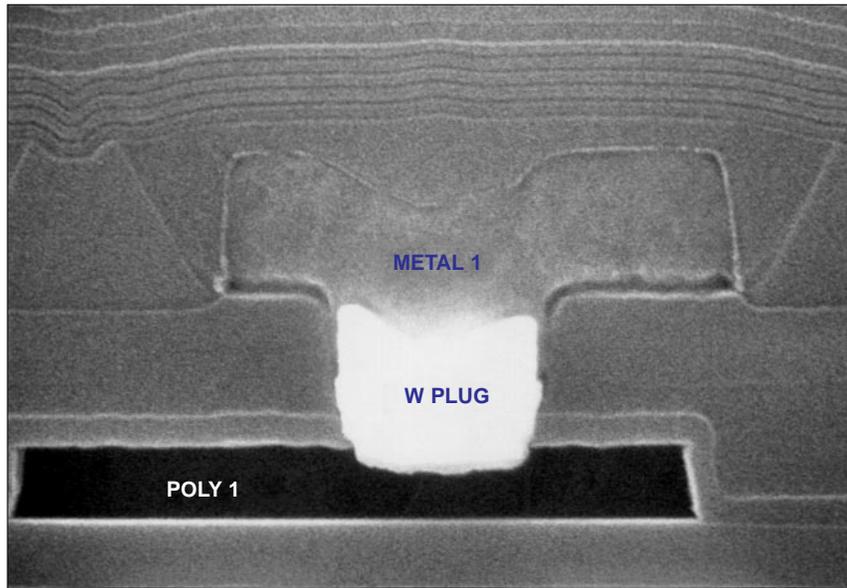


Mag. 5700x

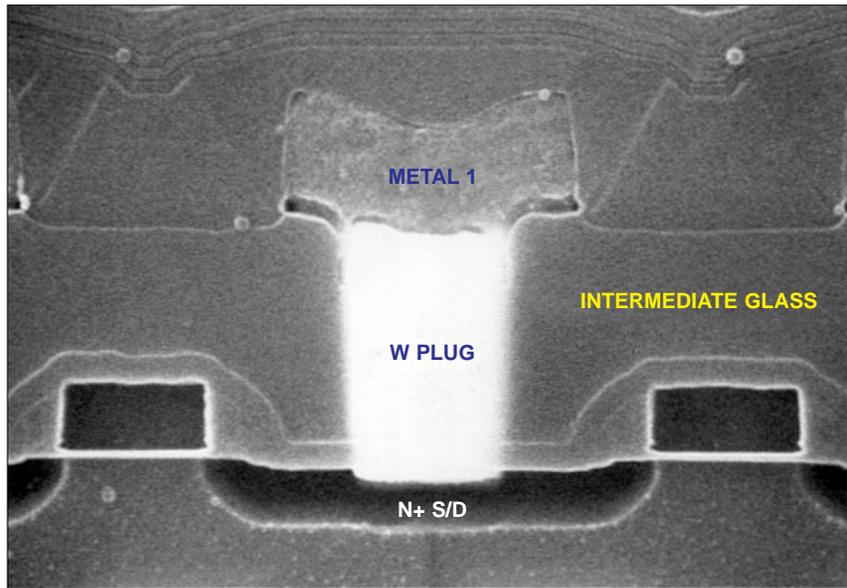


Mag. 27,000x

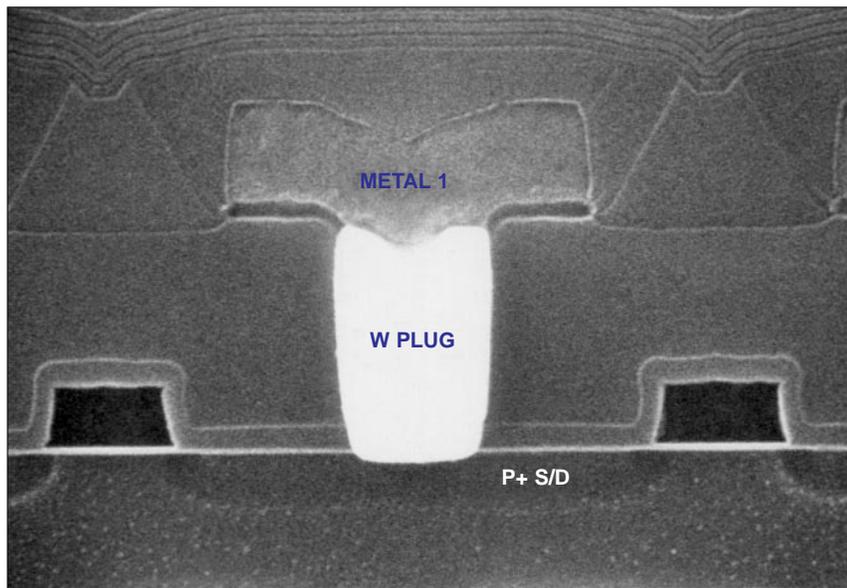
Figure 20. SEM views of metal 1 coverage. 60°.



metal 1-to-poly 1,
Mag. 30,000x

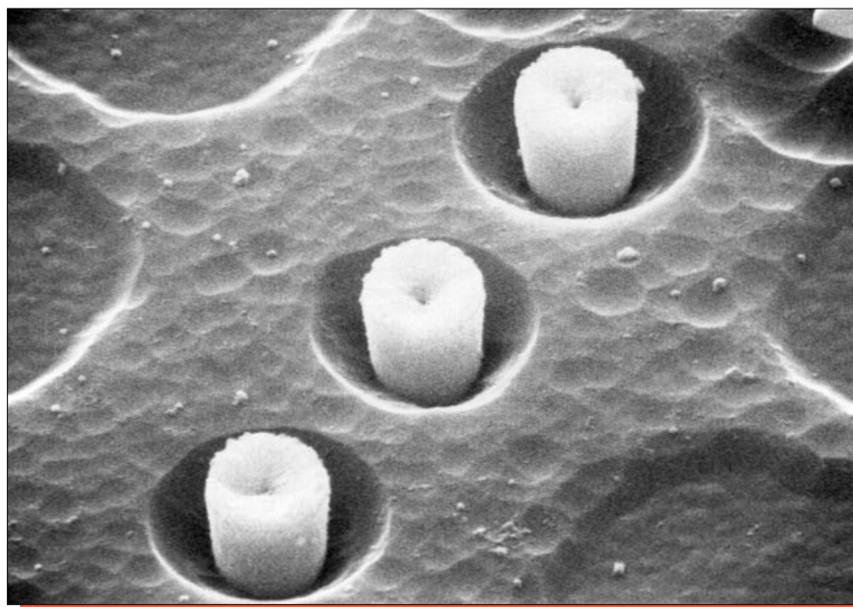


metal 1-to-N+,
Mag. 25,000x

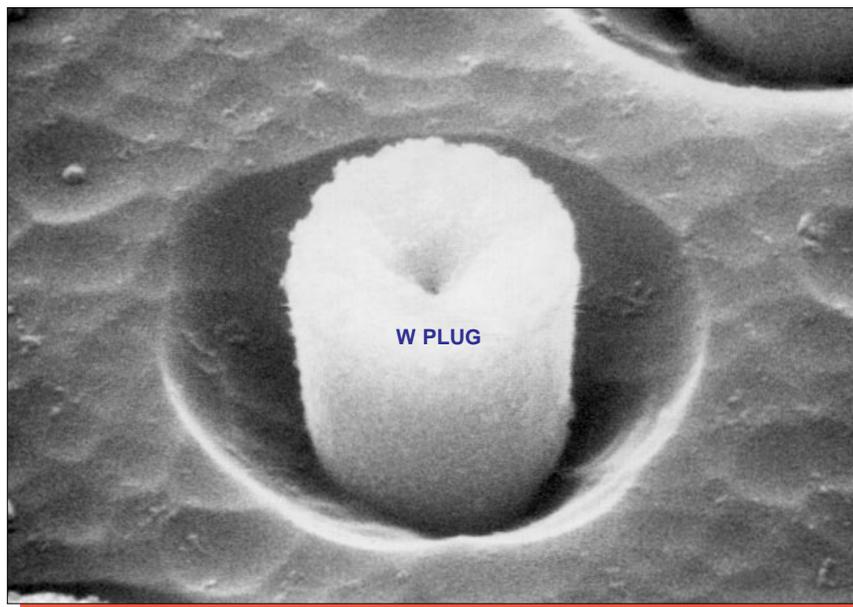


metal 1-to-P+,
Mag. 25,000x

Figure 21. SEM section views of typical metal 1 contacts.

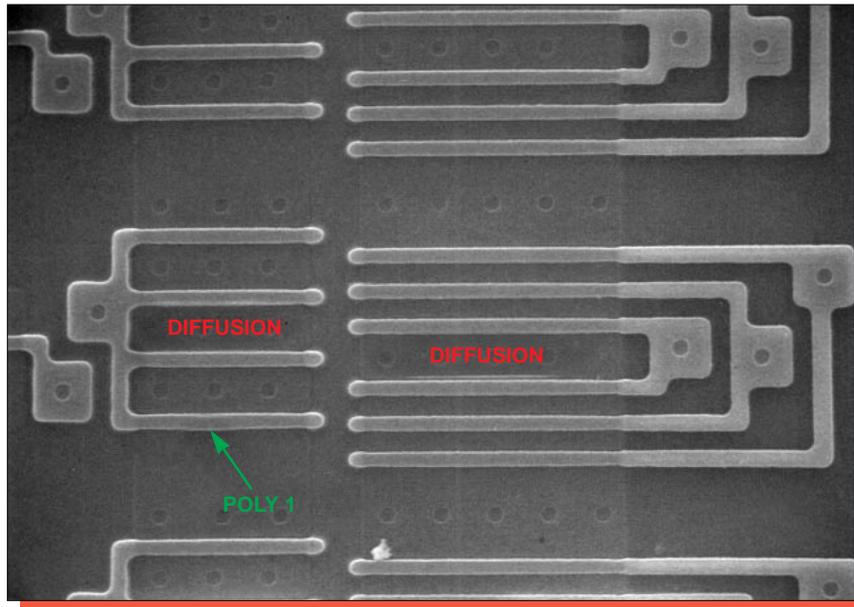


Mag. 16,000x

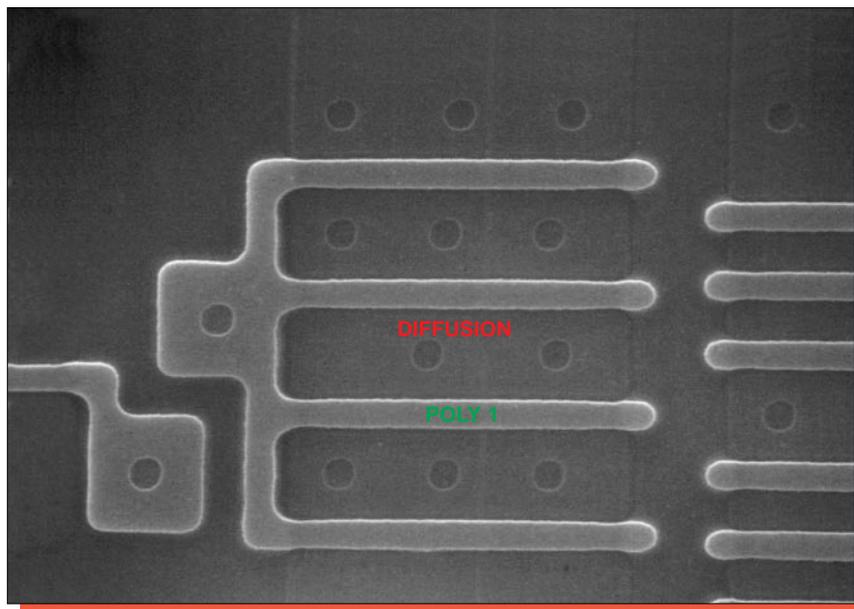


Mag. 40,000x

Figure 22. SEM views of tungsten plugs following removal of metal 1. 45°.

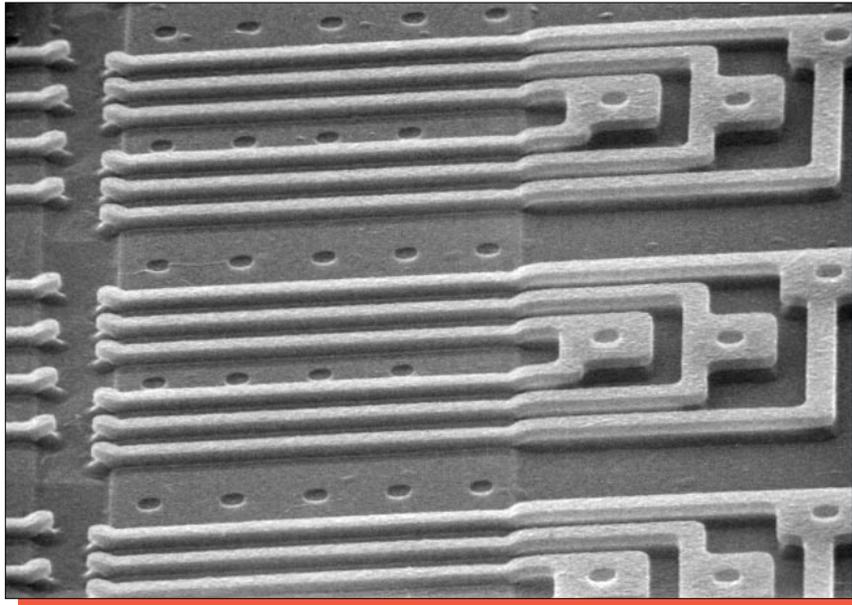


Mag. 2700x

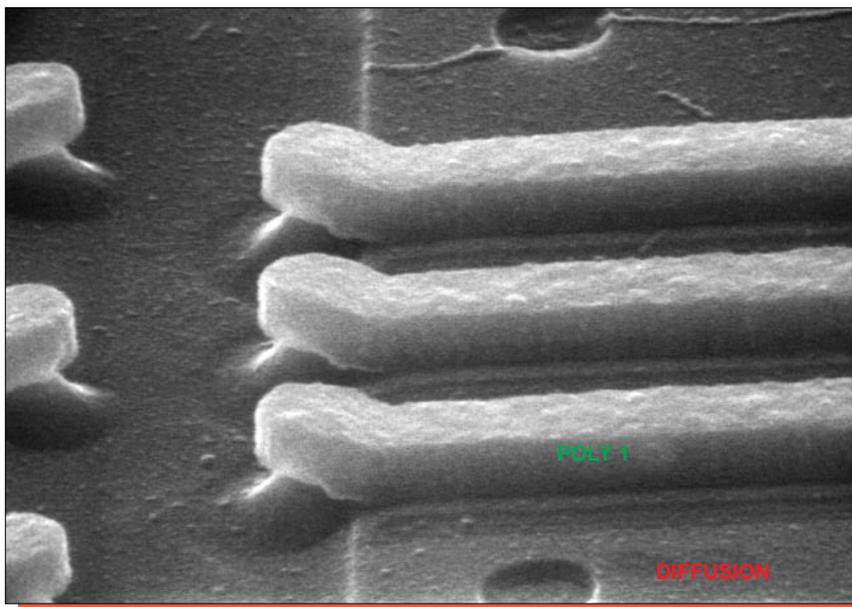


Mag. 5500x

Figure 23. Topological SEM views of poly 1 patterning. 0°.

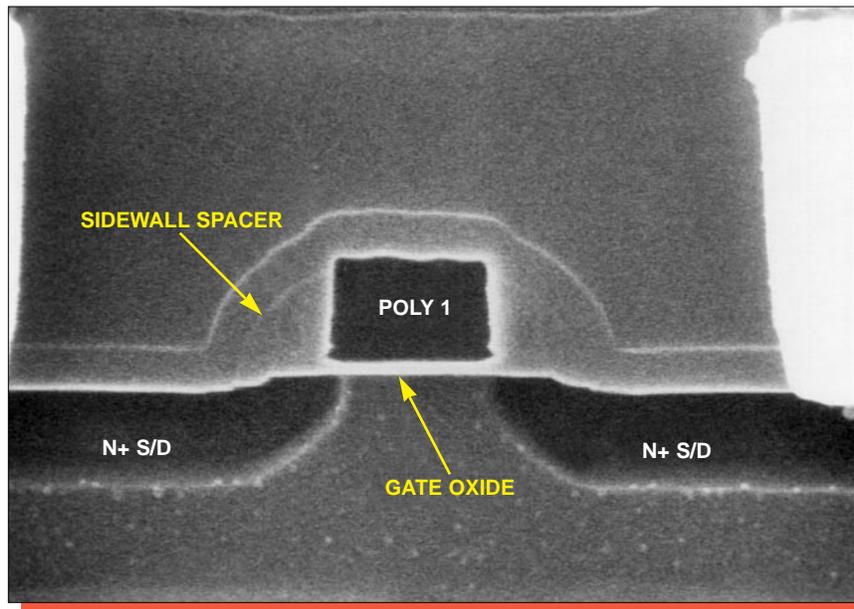


Mag. 4200x

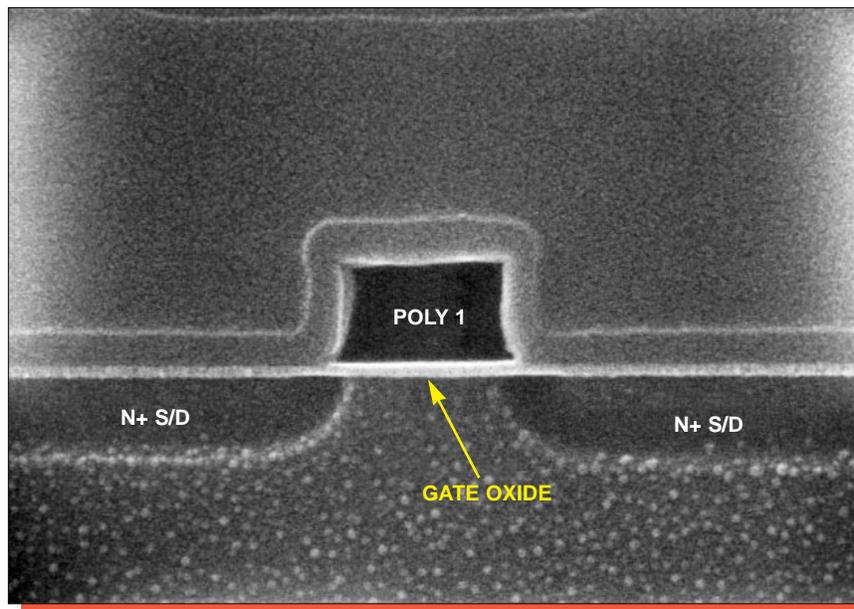


Mag. 20,000x

Figure 24. SEM views of poly 1 coverage. 60°.

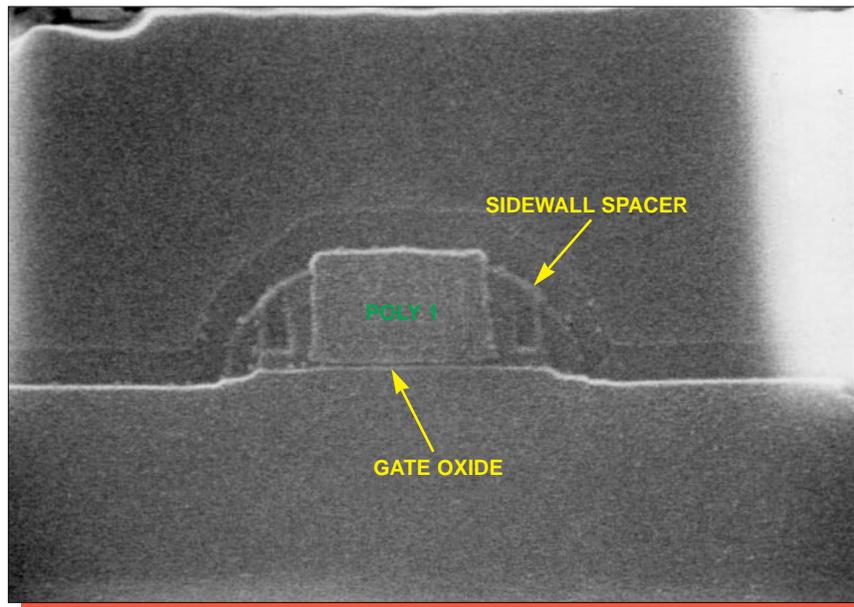


N-channel

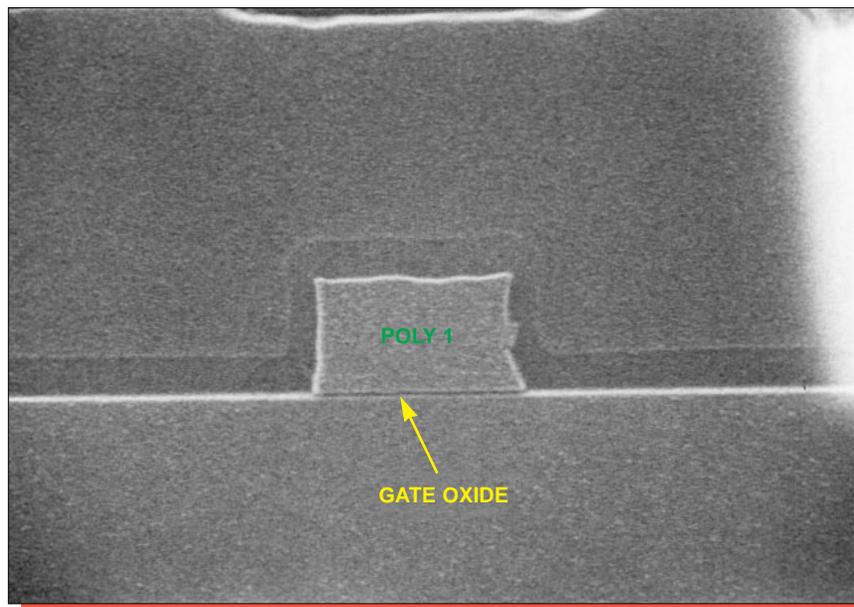


P-channel

Figure 25. SEM section views of typical transistors. Silicon etch, Mag. 40,000x.

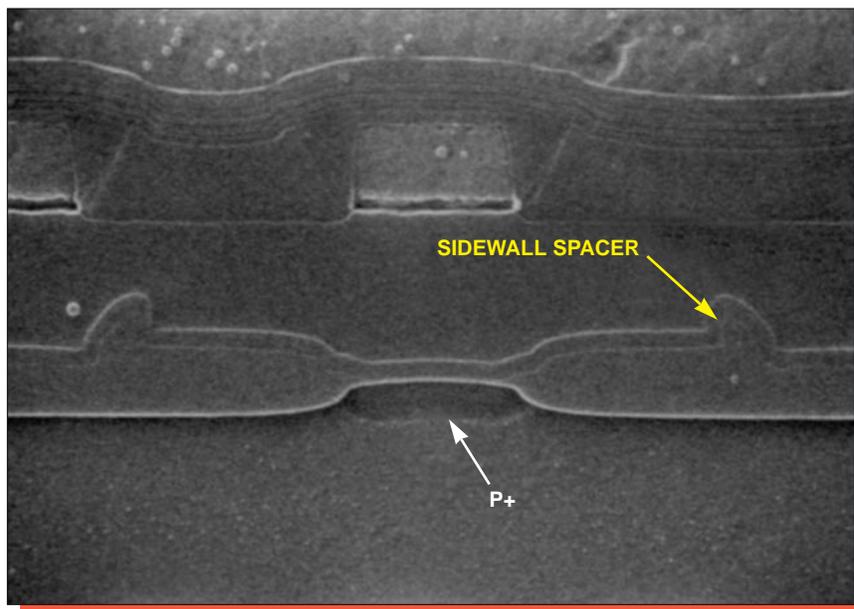


N-channel

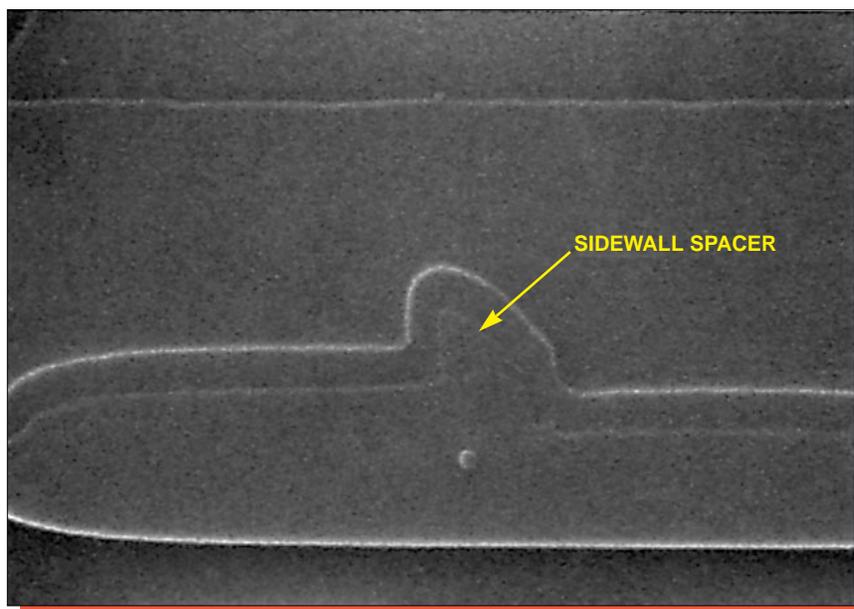


P-channel

Figure 25a. SEM section views of typical transistors. Glass-etch, Mag. 40,000x.



Mag. 17,000x



Mag. 40,000x

Figure 26. SEM section views of residual oxide sidewall spacers.

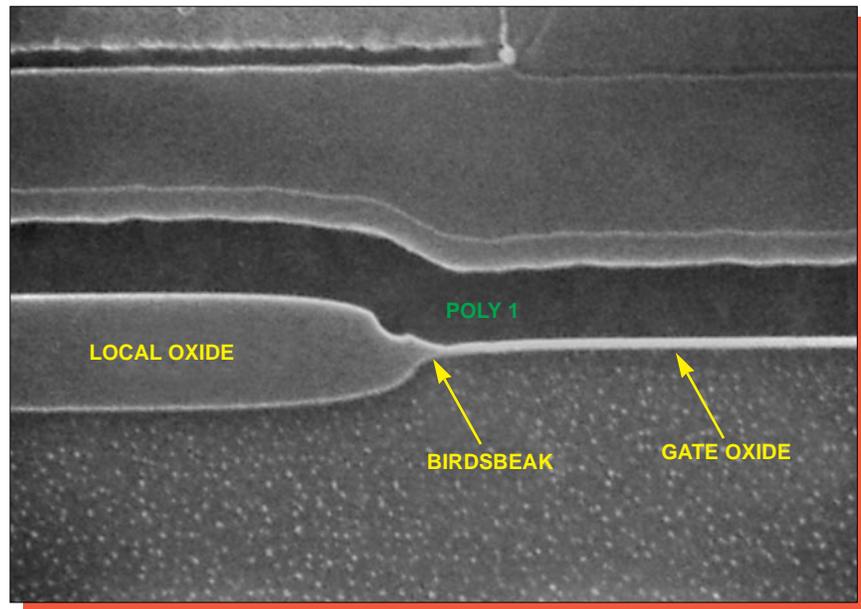


Figure 27. SEM section view of a local oxide birdsbeak. Mag. 28,000x.

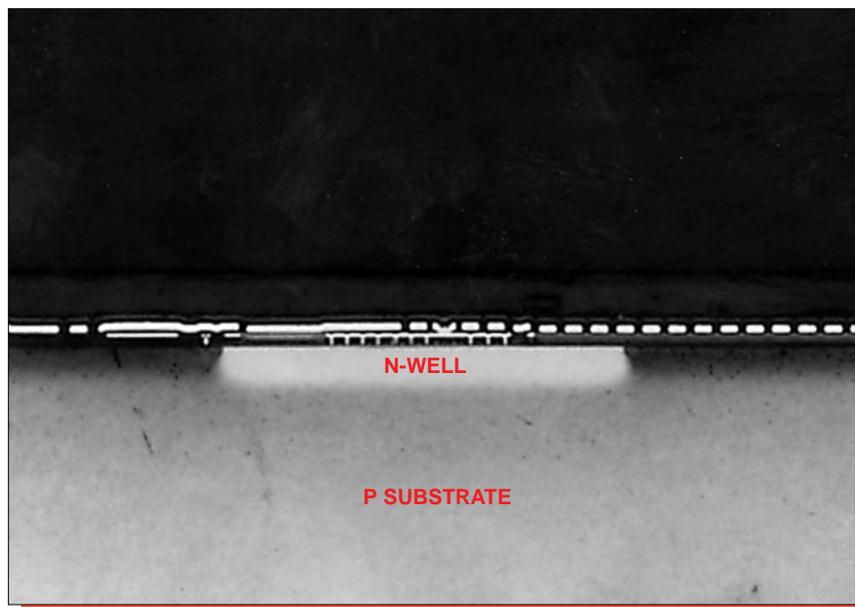
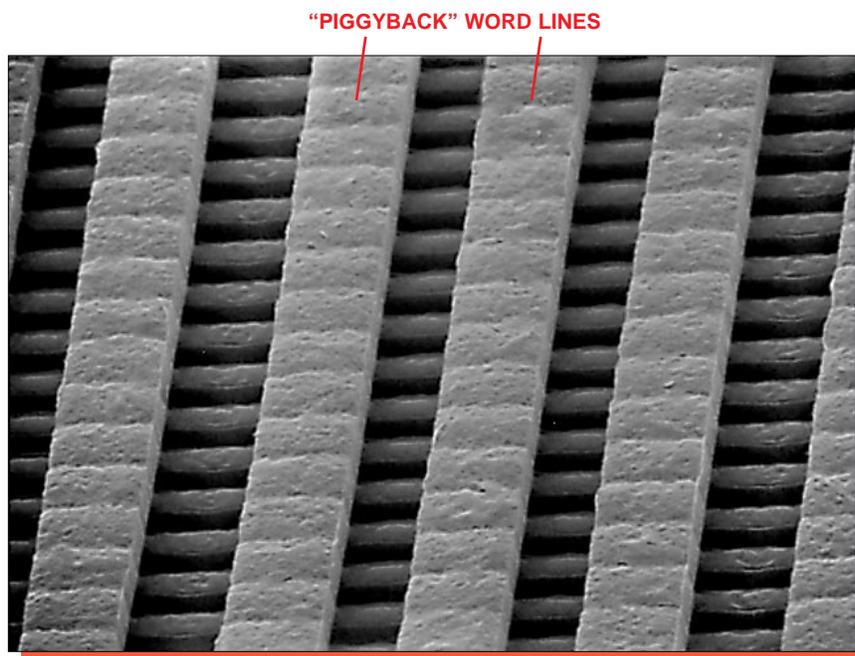
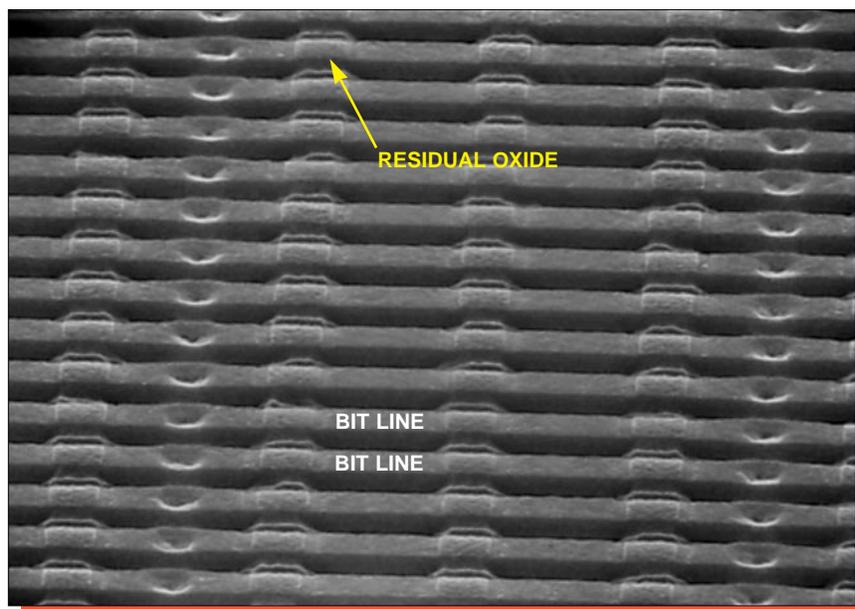


Figure 28. Section view of well structure. Mag. 800x.

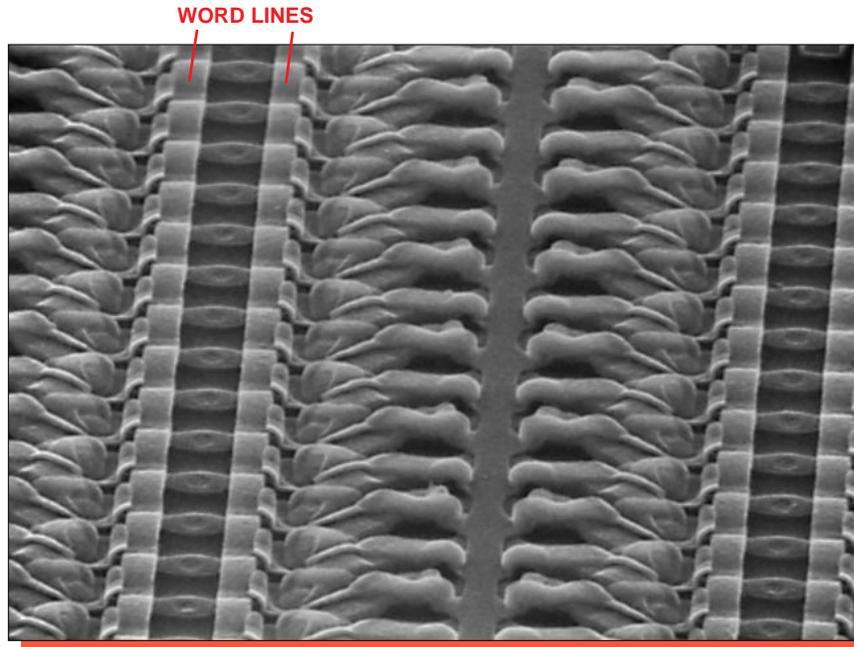


metal 2

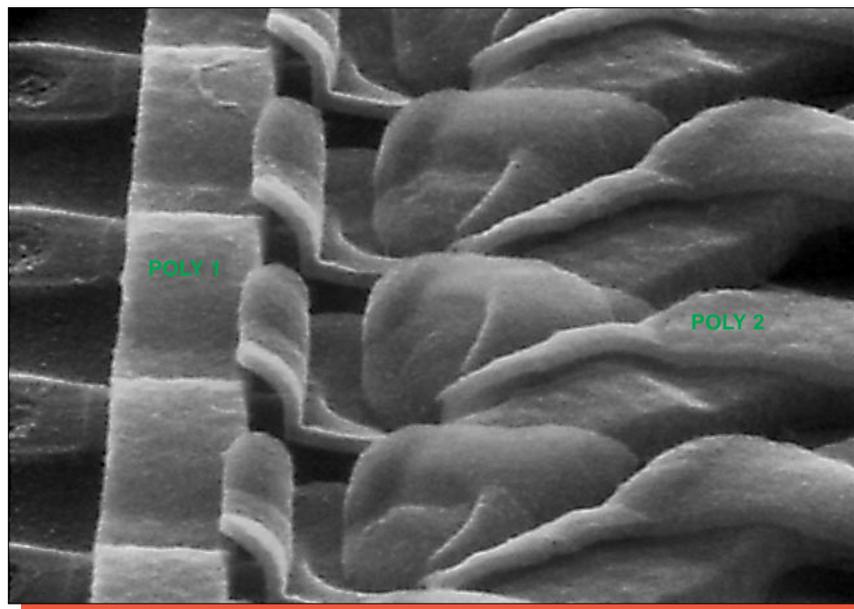


metal 1

Figure 29. Perspective SEM views of the SRAM array. Mag. 5000x, 60°.



Mag. 5000x



Mag. 20,000x

Figure 30. Perspective unlayered SEM views of the SRAM array. 60°.

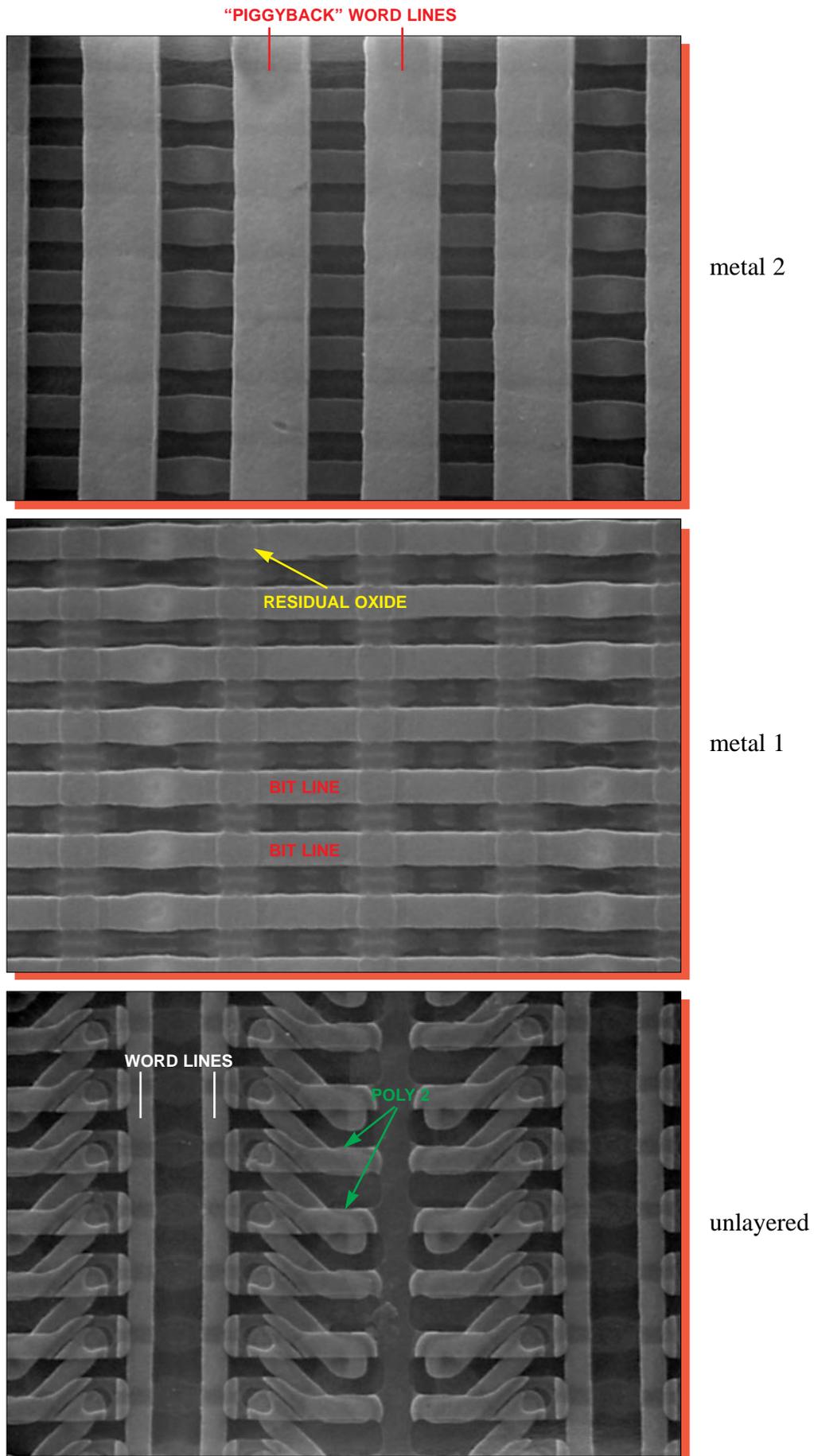
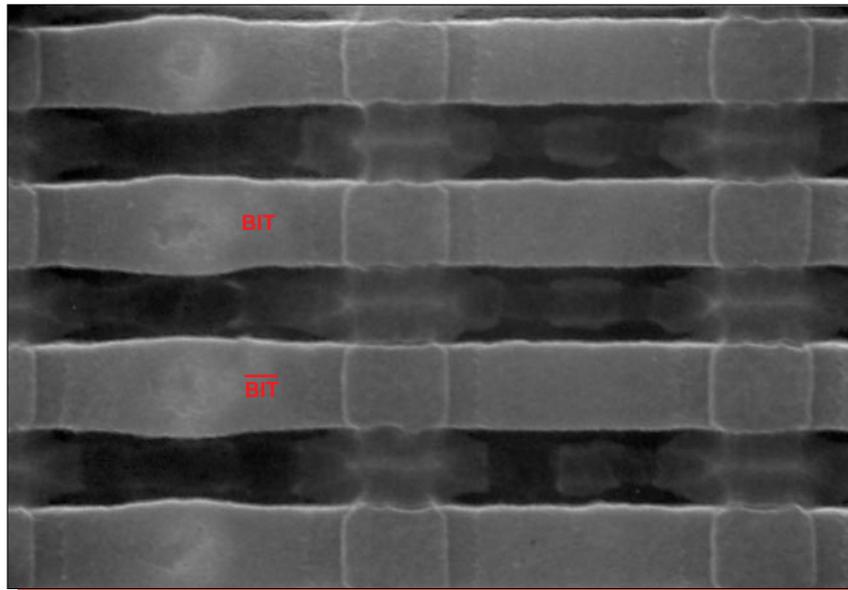
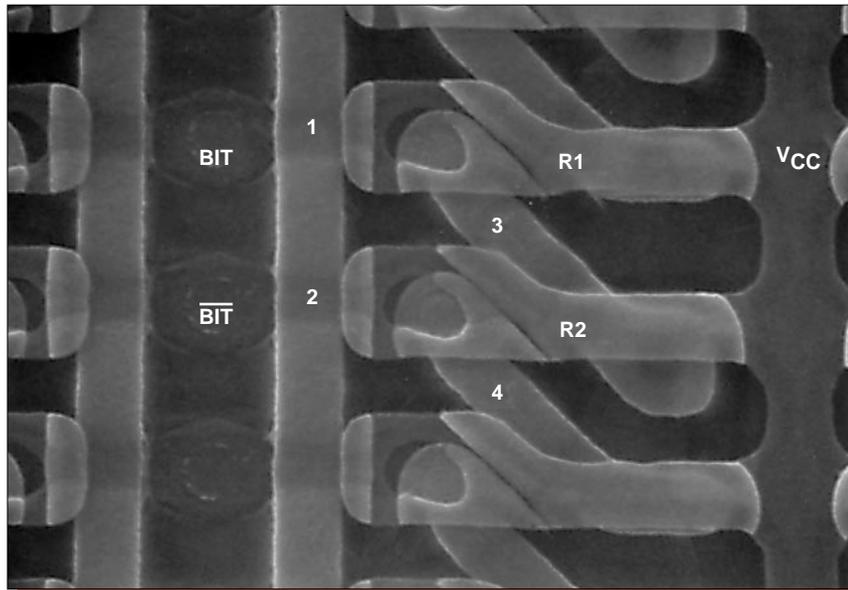


Figure 31. Topological SEM views of the SRAM array. Mag. 4800x, 0°.



metal 1



unlayered

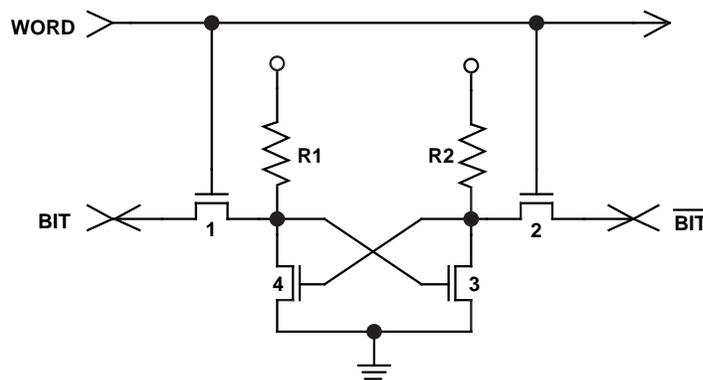
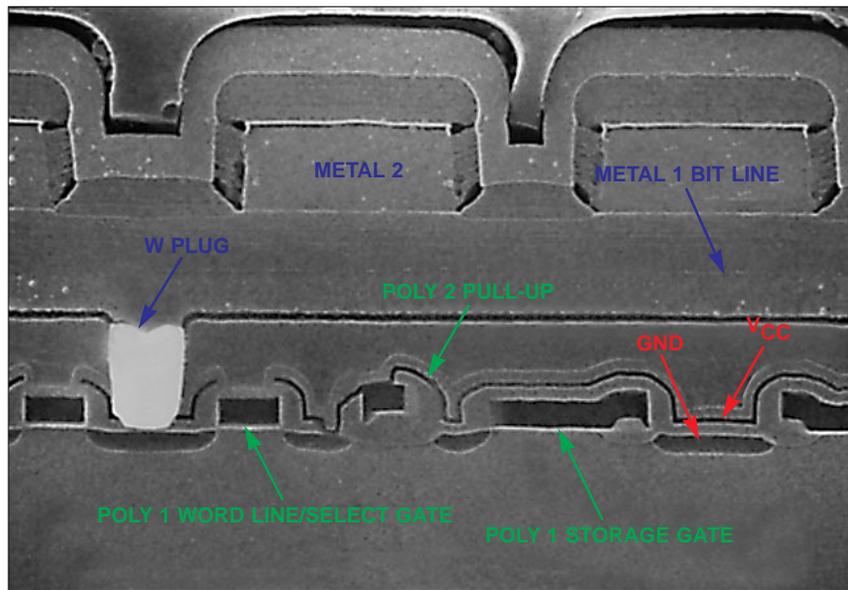
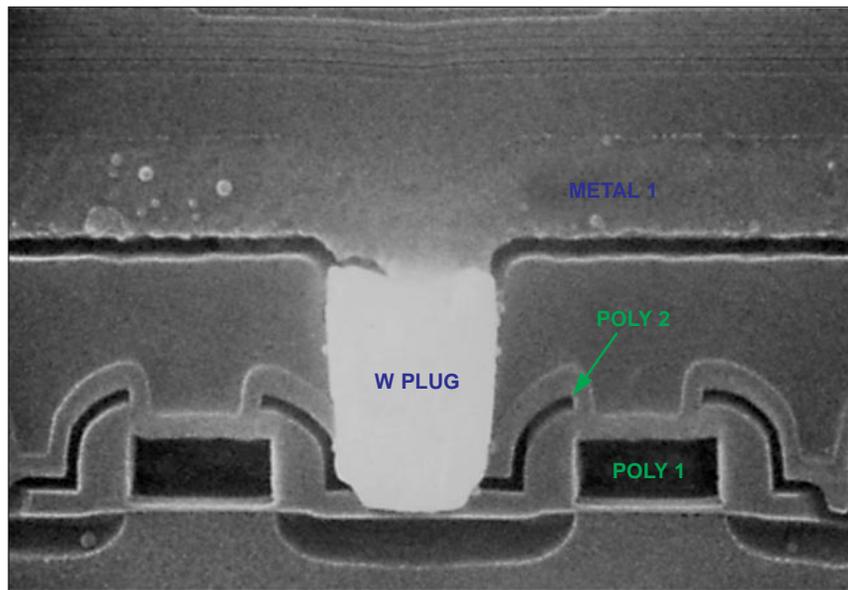


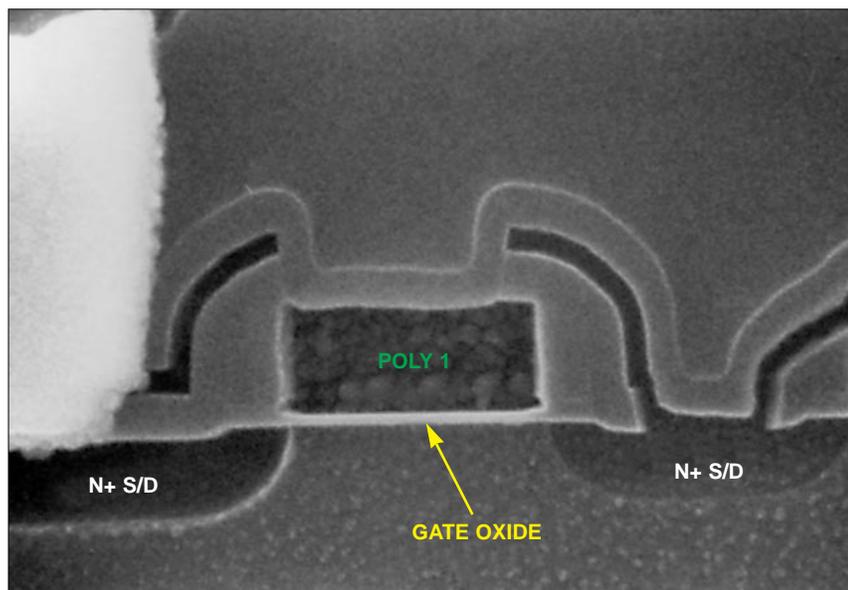
Figure 32. Topological SEM views and schematic of an SRAM cell. Mag. 10,000x, 0°.



Mag. 10,000x

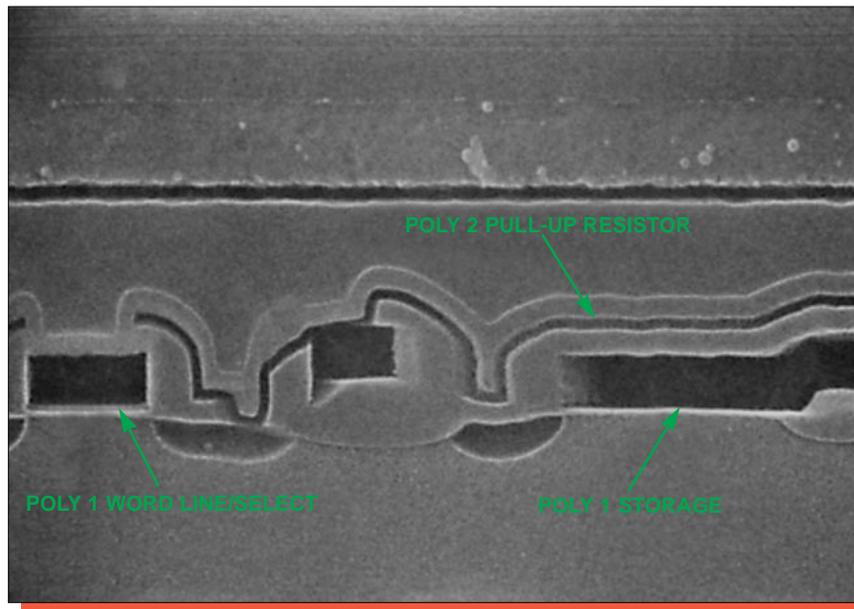


Mag. 24,000x

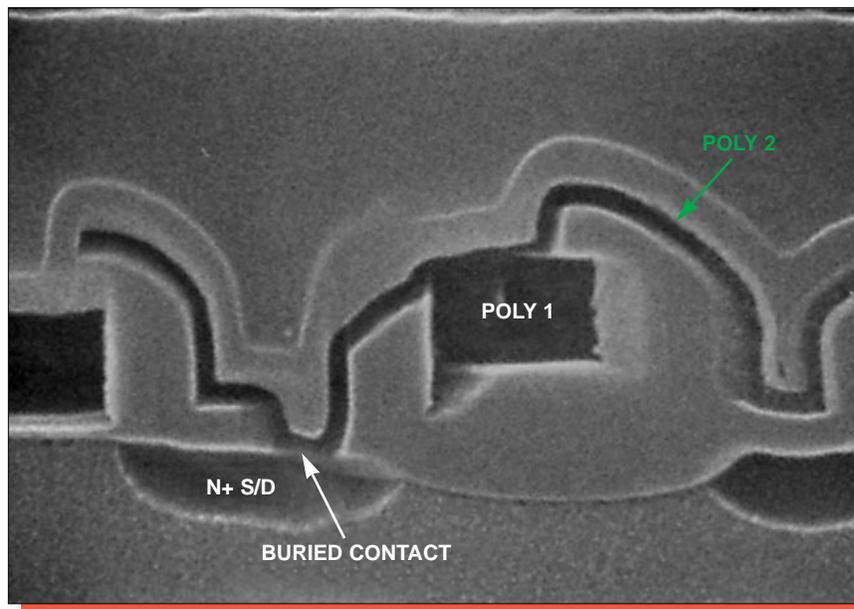


Mag. 40,000x

Figure 33. SEM section views of the SRAM cell.

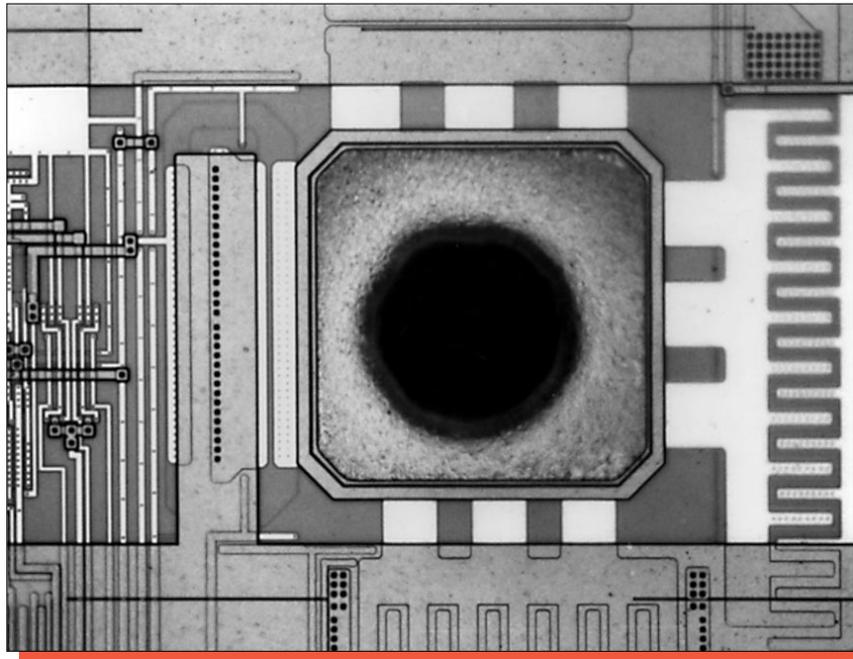


Mag. 20,000x

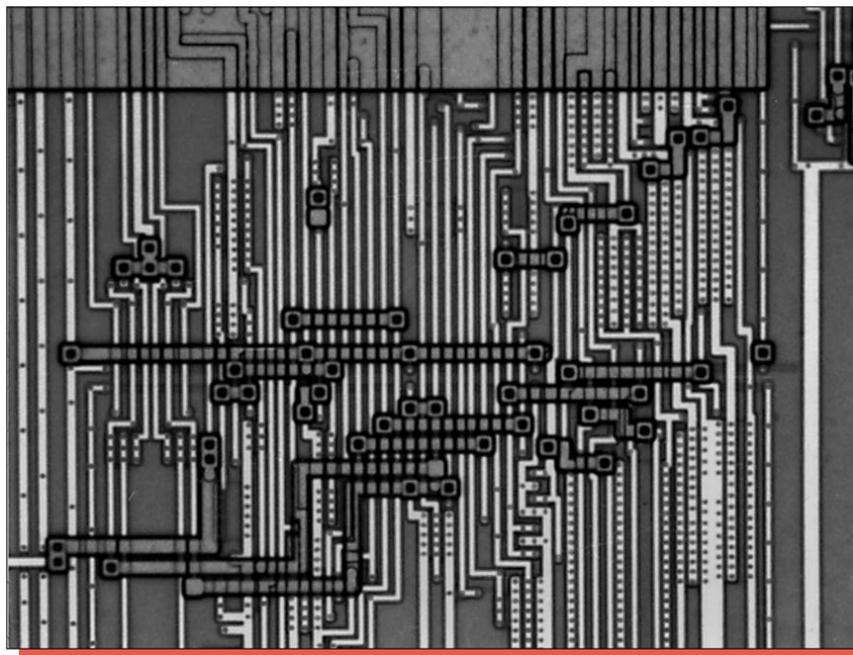


Mag. 40,000x

Figure 34. Detailed SEM section views of the SRAM cell.



Mag. 320x



Mag. 500x

Figure 35. Optical views of input protection and general device circuitry.

