MOTOROLA

High-Performance Internal Product Portfolio Overview

Issue 10
Fourth Quarter, 1995

PREFACE

Welcome to the High-Performance Embedded Systems Marketing Group in Austin.

This document has been prepared as a quarterly guide to the broad range of 16- and 32-bit microprocessors available from Motorola. It is intended to be a handy reference guide to Motorola's microprocessor portfolio that complements the other sources of technical product information.

Our High Performance product family is still growing rapidly. The 68000 Family continues to win new customers with increasing levels of integration, low-power operation, and high-performance networking solutions that improve price/performance thus enabling our customers to develop new market segments. The large base of installed software and development environments available for the family make the 68000 Family the processor of choice for the embedded control world.

Because of the increasing complexity and range of our products, the tools we provide to the field need to be appropriate and user friendly. Thus, we have tried to produce this document in a similar format to other offerings from High-Performance Embedded Systems Division.

If you have any questions, please do not hesitate to call either your local High-Performance PME or the factory Technical Marketing Group.

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M68000 FAMILY STRATEGY

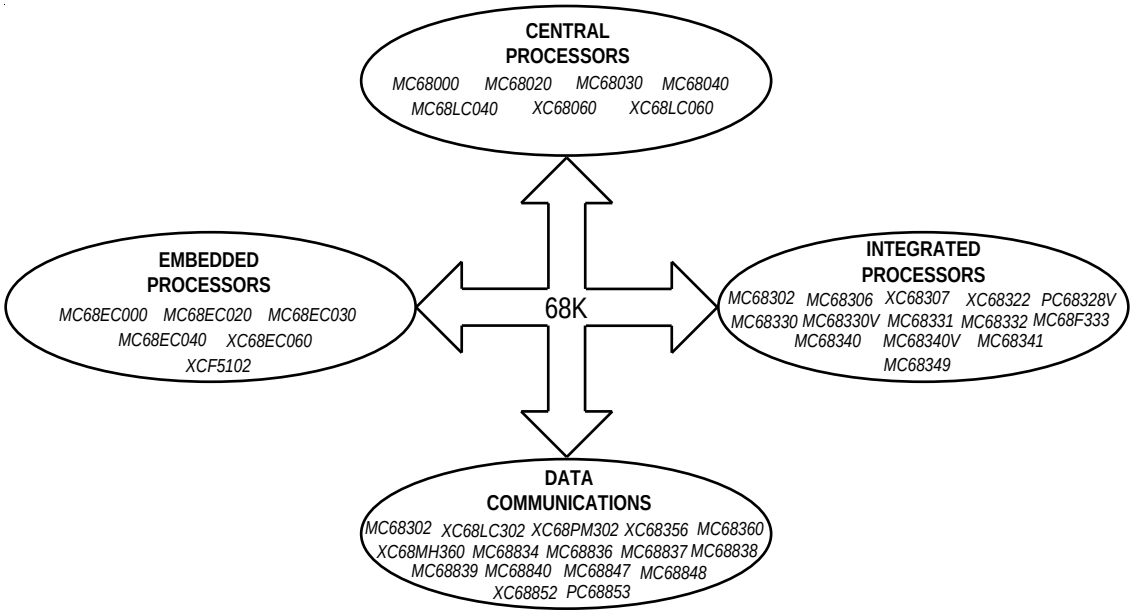
The M68000 Family is already the industry standard in computing and embedded control applications.

Markets:

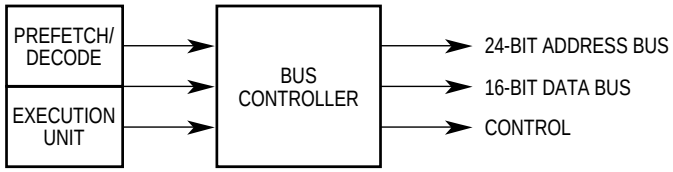
- Low- to Mid-Range Computing
- Laptop and Hand-Held Computing
- Telecommunications (Digital Switches, SDH Platforms, PABX)
- Office Automation (Printers, Faxes, Servers, X-Terminals)
- Network Controllers
- Consumer Products

The M68000 Family provides industry-standard architecture in an extremely cost-effective package/solution. Solutions are available from less than $3 and to more than 100 MIPS with an excellent migration path.

M68000 FAMILY ROADMAP



MC68000



Features:

- 24-Bit Address Bus, 16-Bit Data Bus
- 16 32-Bit Registers
- 7 Interrupt Levels

Target Markets/Applications:

Not recommended for new designs.

Orders will be accepted until December 1, 1995 and shipped through May 1996. After that date, the 68000 will no longer be available but replaced by the pin compatible CMOS 68HC000. Also see MC68EC000, MC68306, and 68307.

Competitive Advantages:

8086–8088—Similar performance but limited migration path to higher performance Microprocessors

Alternative Source:

Hitachi, Signetics, SGS-Thomson

Literature:

Title	Order Number
MC68000 Technical Summary	MC68000/D
M68000 User's Manual	M68000UM/AD Rev 8
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D

Support Tools:

M68EC000IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68440/450—DMA Controllers
MC68901—Multi-function Peripheral
MC68230—Parallel Interface Timer
MC68681—DUART

Package/Speed Options:

Device	Package	Speed	Rev	Temperature	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68000	64-Lead L*	8, 10, 12	—	—	6	6	216	
	64-Lead P	8, 10, 12	—	—	6	6	192	
	68-Lead R, RC*	8, 10, 12	—	—	0	21	210	SPAK000RCXX
	68-Lead FN	8, 10, 12	—	—	0	18	1008	SPAK000FNXX

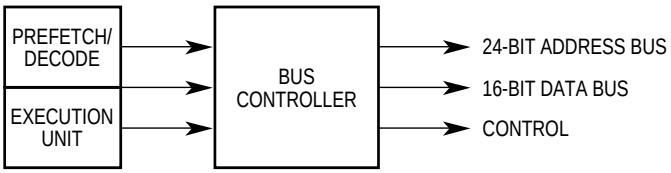
NOTE: FN = Plastic Leaded Chip Carrier (PLCC)
L = Ceramic DIP
P = Plastic Dual-In-Line Pin (PDIP)
R = Pin Grid Array (PGA)
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity
*Not recommended for new designs

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
C91E	4	30%	MOS5	2.5µ	Production	—	—	Elimination of CFC processing
C91E	3	30%	MOS5	2.5µ	Canceled	—	—	Never released to production
C91E	2	30%	MOS5	2.5µ	Production	—	—	Conversion of MOS5 to 5” line
B26M	4	30%	MOS5	2.5µ	Canceled	—	—	Improved yield/speed (220 × 227)
A72E	3	20%	MOS5	2.8µ	Canceled	—	—	Improved mask quality (230 × 260)
A72E	2	20%	MOS5	—	Canceled	—	—	AS noise reduction, split ground
A72E	1	20%	MOS5	—	Canceled	—	—	Stress relief
A72E	0	20%	MOS5	—	Canceled	—	—	Add long fix
A74J	—	10%	MOS5	—	Canceled	—	—	
A92K	—	10%	MOS3	—	Canceled	—	—	
NK8	—	—	—	—	—	—	—	
18GN7	—	10%	MOS5	—	Canceled	—	—	(257 × 291) Hi-rel only
17GN7	—	10%	MOS5	—	Canceled	—	—	
8GN7	—	10%	—	—	Canceled	—	—	Hi-rel only
7GN7	—	10%	—	—	Canceled	—	—	
CCI	—	10%	—	—	—	—	—	

First Silicon: July 1979
MC Qualification Date: Sept 1979
Die Size: 204 × 227 @ 30% (C91E)
Devices: Sites = 68,000; Active = 37,000
Process: HMOS

MC68EC000



Features:

- 24-Bit Address Bus, 8-Bit or 16-Bit Data Bus
- 16 32-Bit Registers
- Interrupt Levels
- 2.7 MIPS Performance at 16.67 MHz

Target Markets/Applications:

The 68EC000 represents the most inexpensive entry point to any 32-bit architecture. Upward migration to higher performance processors is possible because of software compatibility of the architecture. CMOS process ensures low power consumption. Target applications are PABX low level, line cards, GSM fax, modems, industrial control, instrumentation, etc. The 68EC000 is recommended for 8-bit applications that require higher performance and extended addressing range.

Also see MC68306 and 68307.

Competitive Advantages:

Z80—Low cost but limited performance upgrade potential

8086/8088—Requires external support chips to avoid technical limitations

Literature

Title	Order Number
MC68EC000 Technical Summary	MC68EC000/D
M68000 User's Manual	M68000UM/AD Rev 8
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Fact Brochure	BR1109/D

Support Tools:

M68EC000IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68901—Multi-function Peripheral
MC68681—DUART

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68EC000	68-Lead FN	8, 10, 12, 16, 20	—	—	0	18	1008	SPAKEC000FNXX
	64-Lead FU	8, 10, 12, 16, 20	—	—	0	84	840	SPAKEC000FUXX

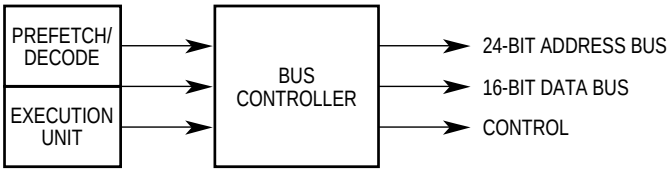
NOTE: FN = Plastic Leaded Chip Carrier (PLCC)
FU = Plastic Quad Flat Pack (PQFP)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History:

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1F30A	1	78%	MOS8	0.71µm	In Qualification	—	—	Changed contact sizing
0F30A	0	78%	MOS8	0.71µm	Canceled	—	—	Die shrink, die size 130 × 143
0F86C	0	63%	Tohoku	1.2µ	Production	—	—	Die size = 213.4 × 237.4
1F90A	1	75%	MOS8	0.8µ	Production	—	—	Changed polyimide reticle
0F90A	0	75%	MOS8	.8µ	Canceled	—	—	Die shrink
5C71T	2	70%	MOS8	1.0µ	Canceled	—	—	

First Silicon: 3Q91
MC Qualification Date: 4Q91
Die Size: 146 × 162 (F90A), 213 × 237 (F86C), 130 × 143 (F30A)
Devices: Sites = 68,000; Active = 37,000
Process: HCMOS

MC68HC000



Features:

- 24-Bit Address Bus, 16-Bit Data Bus
- 16 32-Bit Registers
- 7 Interrupt Levels
- 2.7 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68HC000 processor is a low-power dissipation HCMOS version of the MC68000 16/32-bit microprocessor. It is completely pin, timing, parameter and code compatible with the standard (HMOS) MC68000. The 68HC000 offers power consumption lower by an order of magnitude than that for the HMOS 68000. Worst case power dissipations are: 0.131W @ 8 MHz, 0.158 W @ 10 MHz, 0.184 W @ 12.5 MHz, 0.263W @ 16.67 MHz.

The 64-pin P version is not sold in the United States.

Competitive Advantages:

8086/8088—Similar performance but limited migration path to higher performance Microprocessors

Alternative Sources:

Hitachi, Toshiba

Literature:

Title	Order Number
MC68HC000 Technical Summary	MC68HC000/D Rev 4
M68000 User's Manual	M68000UM/AD Rev 9

Support Tools:

M68EC000IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68901—Multi-function Peripheral
MC68681—DUART

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68HC000	64-Lead P	8, 10, 12, 16	—	—	6	6	192	SPAKHC000PXX
	68-Lead R*, RC*	8, 10, 12, 16	—	CRC8,10,12,16	0	21	210	SPAKHC000RCXX
	68-Lead FN	8, 10, 12, 16, 20	—	CFN8,10,12,16	0	18	1008	SPAKHC000FNXX
	68-Lead FC*	8, 10, 12, 16	—	CFC8,10,16	0	78	780	SPAKHC000FCXX

NOTE: FC = Plastic Quad Flat Pack (PQFP)
FN = Plastic Leaded Chip Carrier (PLCC)
P = Plastic Dual-In-Line Pin (PDIP)
R = Pin Grid Array (PGA)
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

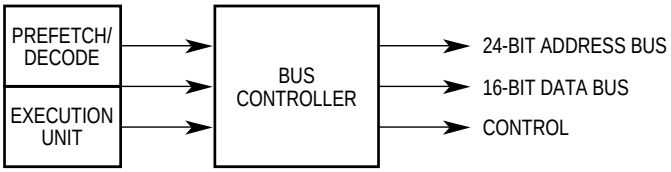
* Not recommended for new designs

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
0G54B	0	75%	MOS11	0.8µ	In Qualification	—	—	MOS11 version of E72N - 147.1 x 162.1
2E60R	2	63%	Tohoku	1.2µ	Production	—	—	
1E60R	1	63%	Tohoku	1.2µ	Canceled	—	—	
0E60R	0	63%	Tohoku	1.2µ	Canceled	—	—	Die shrink, 212.6 × 236.6
1E72N	1	75%	MOS8	0.8µ	Production	—	—	Die shrink 147.1 × 163.2
4C71T	4	70%	MOS8	1.0µ	Canceled	—	—	Used on DIP and ext tempo versions
2B89N	2	56%	Tohoku	1.5µ	Canceled	—	—	Utilizes a differentially sized poly mask
1C71T	1	70%	MOS8	1.0µ	Canceled	—	—	Die size = 201 × 220
3C44C	3	0	MOS8	—	Canceled	—	—	1.2µ process in MOS8
1B89N	1	56%	Tohoku	1.5µ	Canceled	—	—	Die size = 242 × 271
1B66R	1	20%	MOS8	—	Canceled	—	—	Shrink and fix latch up problem
2C44C	2	0	MOS8	—	Canceled	—	—	Poly sizing change for speed improvement
1C44C	1	0	MOS8	—	Canceled	—	—	Fix latch up problem
4B12C	3	0	MOS8	—	Canceled	—	—	Poly sizing change for yield enhancement
3B12C	2	0	MOS8	—	—	—	—	Speed path fix for speed enhancement
1B12C	1	0	MOS8	—	Canceled	—	—	Poly layer sized for speed enhancement
0B12C	0	0	MOS8	—	Canceled	—	—	Original Motorola mask set

First Silicon: Aug 1986
MC Qualification Date: 4Q86
Die Size: 147.1 × 163.2 (E72N), 147.1 × 162.1 (0G54B), 213 × 237 (E60R)
Devices: Sites = 68,000; Active = 42,000
Process: HCMOS

MC68HC001



Features:

- 24-Bit Address Bus, 16-Bit Data Bus
- 16 32-Bit Registers
- 7 Interrupt Levels
- 2.7 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68HC001 is functionally and software compatible with the 68HC000. In addition, the 68HC001 features a mode function which allows the processor to operate as a 16-bit 68000 or an 8-bit 68008.

MC68HC001 will be discontinued in 1995. The 68HC001 8-bit functionality will be incorporated into the 68HC000.

Literature:

Title	Order Number
MC68HC001/D Technical Summary	MC68HC001/D Rev 4
M68000 User's Manual	M68000UM/AD Rev 8

Support Tools:

M68EC000IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68901—Multi-function Peripheral
MC68681—DUART
MC68HC05I8—MCU

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68HC001*	68-Lead FC*	8, 10, 12, 16	—	—	0	78	780	SPAKHC001FCXX
	68-Lead FN*	8, 10, 12, 16	—	CFN8,10,12,16	0	18	1008	SPAKHC001FNXX
	68-Lead RC*	8, 10, 12, 16	—	CRC8,10,12,16	0	21	210	SPAKHC001RCXX

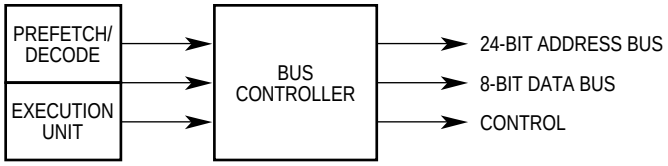
NOTE: FC = Plastic Quad Flat Pack (PQFP) MPQ = Minimum Package Quantity
FN = Plastic Leaded Chip Carrier (PLCC) POQ = Preferred Order Quantity
RC = Pin Grid Array (PGA), Gold Lead Finish SOQ = Sample Order Quantity
*No new designs.

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
2E60R	2	63%	Tohoku	1.2µ	Production	—	—	
1E60R	1	63%	Tohoku	1.2µ	Canceled	—	—	
0E60R	0	63%	Tohoku	1.2µ	Canceled	—	—	Die shrink, 212.6 × 236.6
1E72N	1	75%	MOS8	0.8µ	Production	—	—	Die shrink 147.1 × 163.2
4C71T	4	70%	MOS8	1.0µ	Canceled	—	—	
1C71T	1	70%	MOS8	1.0µ	Canceled	—	—	Die size = 201 × 220
2C72P	2	56%	MOS8	1.5µ	Canceled	—	—	Downsized PO5 by .22µm
1C72P	1	56%	MOS8	1.5µ	Canceled	—	—	Increased bus speed
C72P	0	56%	MOS8	1.5µ	Canceled	—	—	Die size = 242 × 270
0G54B	0	75%	MOS11	0.8µ	In Qualification	—	—	MOS11 version of E72N

First Silicon: 4Q89
MC Qualification Date: 4Q89
Die Size: 147.1 × 162.1 (0G54B), 147.1 × 163.2 (E72N), 213 × 237 (E60R)
Devices: Sites = 68,000; Active = 42,000
Process: MOS

MC68008



Features:

- 8-Bit Data Bus
- 16 32-Bit Data and Address Registers
- 14 Addressing Modes
- Complete Compatability with the MC68000

Target Markets/Applications:

Not recommended for new designs.

Orders will be accepted until December 1, 1995 and shipped through May 1996. After that date, the 68008 will only be available from SGS-Thomson. The LC version was discontinued in March, 1992.

The 68008 has the same register set, same instructions, and same functionality as the 68000. The major differences between the 68000 and 68008 are that the 68008 has an 8-bit data bus, it can only address up to 4 megabytes of memory (PLCC), and it has a two wire bus arbitration scheme.

Literature:

Title	Order Number
Minimum System Configuration	AN897/D
M68008 Technical Summary	BR259/D
M68000 User's Manual Rev 8	M68000UM/AD

Support Tools:

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

No longer available

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68008	52-Lead FN	8, 10	—	—	0	23	1955	SPAK008FN
	48-Lead P	8, 10	—	—	7	7	294	

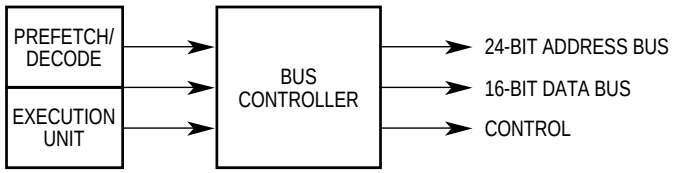
NOTE: FN = Plastic Leaded Chip Carrier (PLCC)
P = Plastic Dual-In-Line Pin (PDIP)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
C88P	1	30%	MOS5	2.5µ	Production	—	—	Elimination of CFC processing
C88P	0	30%	MOS5	2.5µ	Canceled	—	—	5” wafer conversion
PR4	0	20%	MOS5	—	Canceled	—	—	Logic fix, radial die

First Silicon: 2Q82
MC Qualification Date: 1Q83
Die Size: 230 × 209
Devices: Sites = 70,000; Active = 36,750
Process: HMOS

MC68010



Features:

- 16 32-Bit Data and Address Registers
- 16 Mbyte Direct Addressing Range
- Virtual Memory, Machine Support
- 24-Bit Address Bus, 16-Bit Data Bus

Target Markets/Applications:

Not recommended for new designs.

Orders will be accepted until December 1, 1995 and shipped through May 1996. After that date, the 68010 will no longer be available. The LC version was discontinued in March, 1992.

The 68010 is pin-for-pin compatible with the 68000 and has all the features of the 68000 plus faster instruction execution, virtual memory operation, vector base register, and automatic “loop mode”.

Literature:

Title	Order Number
M68000 User’s Manual	M68000UM/AD Rev 8
M68010 Technical Summary	BR269/D

Support Tools:

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

No longer available

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68010	68-Lead FN*	8, 10, 12	—	—	0	19	1064	SPAK010FNXX
	64-Lead P*	8, 10, 12	—	—	6	6	192	
	68-Lead R*, RC*	8, 10, 12	—	—	0	21	210	SPAK010RCXX

NOTE: FN = Plastic Leaded Chip Carrier (PLCC)
P = Plastic Dual-In-Line Pin (PDIP)
R = Pin Grid Array (PGA(
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

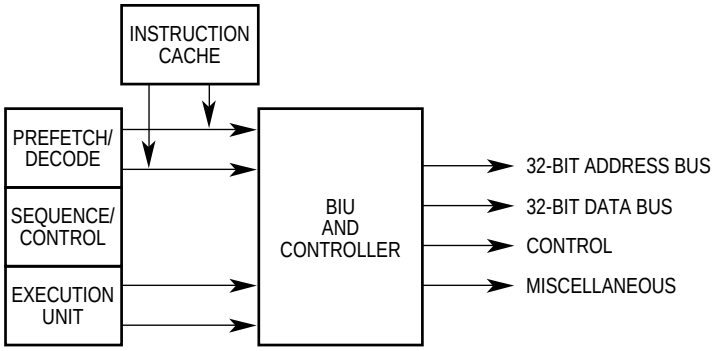
* Not recommended for new designs

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
C97R	3	25%	MOS5	2.6µ	Production	—	—	Resizing 01/05 layers
C97R	2	25%	MOS5	2.6µ	Canceled	—	—	Elimination of CFC processing
C97R	1	25%	MOS5	2.6µ	Canceled	—	—	5” wafer conversion
A71R	0	25%	MOS5	2.6µ	Canceled	—	—	AS ring noise reduction, split ground ring
TA2	2	10%	MOS5	3.2µ	Canceled	—	—	Speed fix
TA2	1	10%	MOS5	3.2µ	Canceled	—	—	

First Silicon: 3Q82
MC Qualification Date: 4Q82
Die Size: 237.5×270
Devices: Sites = 84,000; Active = 43,990
Process: HMOS

MC68020



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 256-Byte Instruction Cache
- Coprocessor Interface
- 9.8 MIPS/0.25MFLOPS Performance at 33 MHz

Target Markets/Applications:

The 68020 is the first microprocessor to use a full 32-bit internal and external architecture and offers a vast increase in performance over 8- and 16-bit processors. The dynamic bus feature improves system flexibility, which allows use of 8- or 16-bit peripherals. The MC68EC020 should also be considered unless there is a clear need for a 32-bit address bus.

Literature:

Title	Order Number
MC68020 Technical Summary (Rev 4)	MC68020/D
M68020 User's Manual	M68020UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD

Support Tools:

M68EC020IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68882—Enhanced Floating-Point Coprocessor

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68020	114-Lead RC	12,16, 20, 25, 33	E	CRC16, 20, 25	1	1	14	MC68020RCXXE
	114-Lead RP	16, 20, 25	E	CRP16	1	1	13	MC68020RPXXE
	132-Lead FE*	16, 20, 25, 33	E	—	2	36	180	SPAK020FEXXE
	132-Lead FC	16, 20, 25, 33	E	CFC16, 20, 25	2	36	360	SPAK020FCXXE

NOTE: FC = Plastic Quad Flat Pack (PQFP)
FE = Ceramic Quad Flat Pack (CQFP)
RC = Pin Grid Array (PGA), Gold Lead Finish
RP = Plastic Pin Grid Array
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

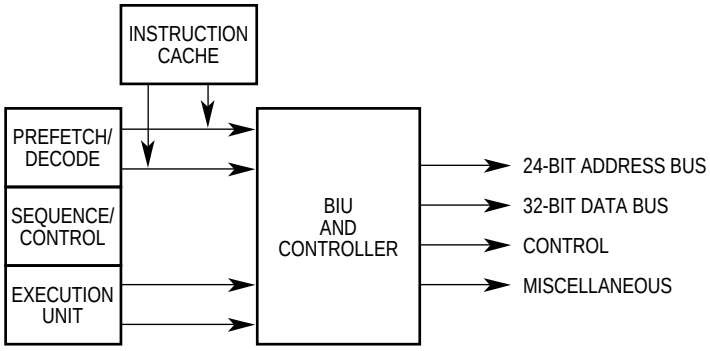
*Not recommended for new designs

History:

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
C54S	A	67%	MOS8	1.0µ	Production	—	—	Military product only
C10H	A	60%	Tohoku	1.2µ	Production	—	—	Extended temperature only
B69R	B	60%	APRDL	1.2µ	Canceled	—	—	33 MHz - 60% shrink only
B49N	B	60%	APRDL	1.2µ	Canceled	—	—	33 MHz - 60% shrink only
B47K	B	50%	MOS8	1.5µ	Canceled	—	—	Same as B87E but for NIKON stepper
B87E	B	50%	MOS8	1.5µ	Canceled	—	—	Internal rev. # change
B40G	A	55%	MOS8	1.35µ	Canceled	—	—	
2A70N	—	40%	MOS8	1.7µ	Canceled	—	—	
1A43S	—	50%	MOS8	1.5µ	Canceled	—	—	Speed enhancement/cost reduction
2A45J	—	40%	MOS8	1.7µ	Canceled	—	—	Phased out - March, 1986
1A45J	L	40%	MOS8	1.7µ	Canceled	—	—	Phased out - March, 1986
A45J	K	40%	MOS8	1.7µ	Canceled	—	—	Virtual bug
A23G	J	40%	MOS8	1.7µ	Canceled	—	—	
A92E	—	40%	APRDL	1.7µ	Canceled	—	—	
E30G	A	67%	TSC	1.0µ	Production	—	—	Optical identical to C54S

First Silicon: May 1984
MC Qualification Date: 2Q85
Die Size: 252 × 244, 282 × 276
Devices: Sites = 190,000; Active = 103,000
Process: HCMOS

MC68EC020



Features:

- 24-Bit Address Bus, 32-Bit Data Bus
- 256-Byte Instruction Cache
- Coprocessor Interface
- 7.4 MIPS Performance at 25 MHz

Target Markets/Applications:

The strategy behind the 68EC020 is to upgrade current 68000 and 68HC000 users to a higher performance product with minimum increase in device or system cost. Key applications are PABX low level, GSM basestations, network controllers, printers, dumb terminals, robotics, VME boards, instrumentation, etc. The MC68EC020 has a 24-bit address bus and does not support extended temperature.

Competitive Advantages:

960SA—Similar price range, but overall system cost increased due to extra logic

960SB—On-chip floating point unit. Can be attacked with higher performance 68EC020/68882 combination at aggressive price

Literature:

Title	Order Number
MC68EC020 Technical Summary	MC68EC020/D
M68020 User's Manual	M68020UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68EC0x0 Family Fact Brochure	BR1109/D

Support Tools:

M68EC020IDP—Integrated Development Platform: hardware/software evaluation module.

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68882—Floating-Point Coprocessor
MC68307—Slave Mode

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68EC020	100-Lead FG	16, 25	—	CFG16	2	66	264	SPAKEC020FGXX
	100-Lead RP	16, 25	—	CRP16, 25	1	1	13	MC68EC020RPXX

NOTE: FG = Plastic Quad Flat Pack (PQFP)
RP = Plastic Pin Grid Array

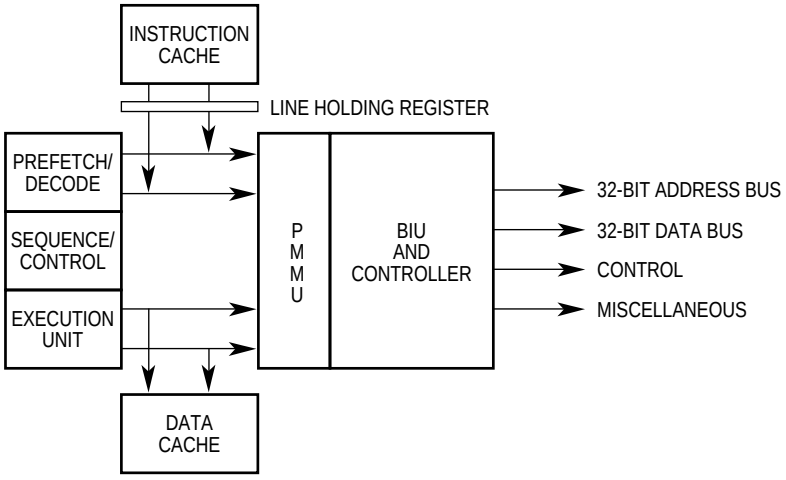
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History:

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
E13G	A	67%	Tohoku	1.0µ	Production	—	—	Optically identical to D76E
D76E	A	67%	MOS8	1.0µ	Production	—	—	
C10H	A	60%	Tohoku	1.2µ	Production	—	—	On RP package, has been replaced by E13G

First Silicon: May 1991
MC Qualification Date: 2Q91
Die Size: 239 × 247
Devices: Sites = 190,000; Active = 103,000
Process: HCMOS

MC68030



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 256-Byte On-Chip Instruction Cache
- 256-Byte On-Chip Data Cache
- 17.9 MIPS at 50 MHz
- Burst Memory Interface
- Internal Harvard Architecture
- Dynamic Bus Sizing
- On-Chip Memory Management

Target Markets/Applications:

The 68030 is well suited for all applications requiring moderate performance and low cost (via dynamic bus sizing, burst memory interface, etc.). Memory management support provides protection for users and tasks allowing controlled execution of programs. Target markets are high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, mid-range PCs, low-end workstations, servers, etc.

Principle markets include low-end to mid-range personal computers as well as embedded applications that require the protection features of a memory management unit.

Competitive Advantages:

Intel 386—Comparable 030 performance

Weaknesses—Has awkward register set and memory management

Intel 960KA—Comparable 68030 performance at approximately the same price range

Weaknesses—Multiplexed address and data buses. No data cache. Performance very

susceptible to wait states. Interrupt latency poor—**Intel quote *typically* 1 ms at 33 MHz**

Literature:

Title	Order Number
MC68030 Technical Summary	MC68030/D
MC68030 User's Manual	MC68030UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D

Support Tools:

M68EC030IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68882—Floating-Point Coprocessor
MC88915/MC88916—Clock Driver
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM6206C, MCM6226A
MC68307—Slave Mode

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68030	128-Lead RC	16,20,25,33,40,50	C	CRC16,20,25,33	1	1	14	
	124-Lead RP	16,20,25,33	C	CRP16,20,25,33	1	1	13	
	132-Lead FE	16,20,25,33	C	—	0	36	180	SPAK030FEXXC

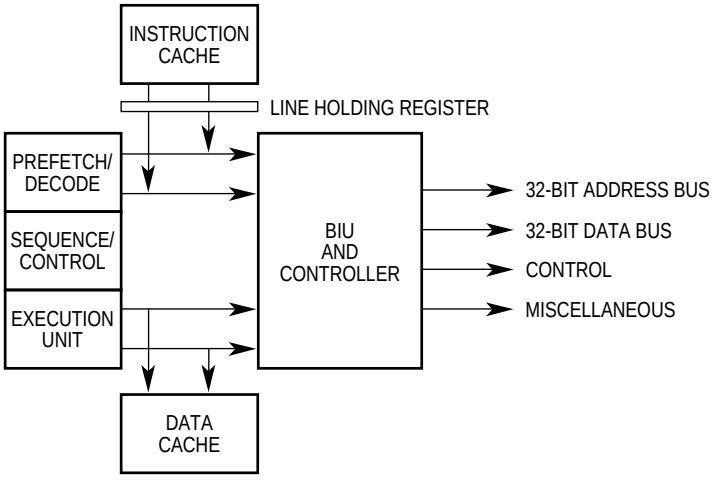
NOTE: FE = Ceramic Quad Flat Pack (CQFP) MPQ = Minimum Package Quantity
RC = Pin Grid Array (PGA), Gold Lead Finish POQ = Preferred Order Quantity
RP = Plastic Pin Grid Array SOQ = Sample Order Quantity

History:

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
C74N	B	67%	MOS8	1.0µ	Production	No	Yes	Process change
D62C	B	60%	Tohoku	1.2µ	Canceled	No	Yes	Tohoku die
D66C	B	67%	Tohoku	1.0µ	Production	No	Yes	Tohoku die
F91C	C	73%	Tohoku	0.8µ	Production	No	Yes	RC, FE package only
C48A	G	60/67%	APRDL	1.2µ	Canceled	—	—	33-MHz evaluation & bug fixer
C43C	B	60%	MOS8	1.2µ	Canceled	No	—	
B67R	I	60%	MOS8	1.2µ	Canceled	—	—	33-MHz MOS8 process certification-C48A
1B56P	D	55%	APRDL	1.35µ	Canceled	Yes	—	25 MHz, 1 errata
3B47B	C	55%	APRDL	1.35µ	Canceled	Yes	—	2 Errata
B47B	0	55%	APRDL	1.35µ	Canceled	—	—	Internal evaluation

First Silicon: April 1987
MC Qualification Date: 4Q87
Die Size: 311 × 276 (C74N), 305 × 282 (D66C), 256 × 238 (F91C)
Devices: Sites = 273,000; Active = 186,000
Process: HCMOS

MC68EC030



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 256-Byte On-Chip Instruction Cache
- 256-Byte On-Chip Data Cache
- 14.3 MIPS at 40 MHz
- Burst Memory Interface
- Internal Harvard Architecture
- Bus Sizing

Target Markets/Applications:

The 68EC030 is well suited for all mid-range embedded control applications that require moderate performance, low cost and the option of surface-mount packaging. Target markets are high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, etc.

Competitive Advantages:

Intel 960KA—Around 68EC030 performance at roughly same price

Weaknesses: Multiplexed address and data buses. No data cache. Performance very susceptible to wait states. Interrupt latency poor—Intel quote *typically* 1 ms at 33 MHz.

AMD29000—Performance lies between 68EC030 and 68EC040 levels

Weaknesses: Lower performance with DRAMs in burst-mode and much more susceptible to wait states. Large register sets—not well suited to multi-tasking.

Literature:

Title	Order Number
MC68EC030 Technical Summary	MC68EC030/D
MC68EC030 User's Manual	MC68EC030UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D

Support Tools:

M68EC030IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

MC68882—Floating-Point Coprocessor
MC68307—Slave Mode
MC88915/MC88916—Clock Driver
FSRAMS—MCM6206C, MCM6226A
Crystals—Champion, Kyocera, ACT

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68EC030	124-Lead RP	25, 40	C	—	1	1	13	
	132-Lead FE	25, 40	C	—	0	36	180	SPAKEC030FEXXC
	144-Lead PV	25	C	—	—	300	300	

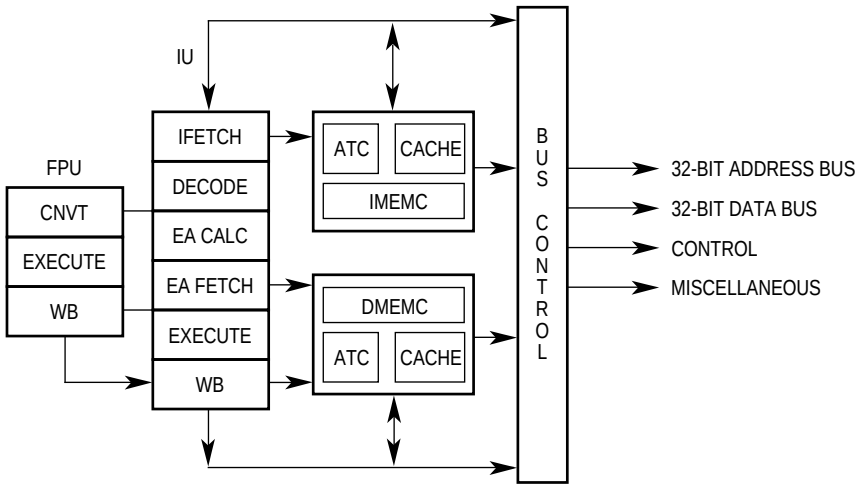
NOTE: FE = Ceramic Quad Flat Pack (CQFP)
PV = Thin Quad Flat Pack (TQFP)
RP = Plastic Pin Grid Array
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History:

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
C74N	B	67%	MOS8	1.0µ	Production	No	Yes	
D66C	B	67%	Tohoku	1.0µ	Production	No	Yes	Tohoku die
D62C	B	60%	Tohoku	1.2µ	Canceled	No	Yes	Tohoku die
F91C	C	73%	Tohoku	0.8µ	Production	No	Yes	FE package only

First Silicon: 1Q91
MC Qualification Date: 1Q91
Die Size: 311 × 276 (C74N); 305 × 282 (D66C), 256 × 238 (F91C)
Devices: Sites = 251,000; Active = 183,000
Process: HCMOS

MC68040



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 4-Kbyte On-Chip Instruction Cache
- 4-Kbyte On-Chip Data Cache
- On-Chip Floating-Point Support
- 43.8 MIPS at 40 MHz
- 5.3 MFLOPS at 40 MHz
- Burst Memory Interface
- On-Chip Memory Management

Target Markets/Applications:

The 68040 is well suited for all applications that require high-integer and floating-point performance while still retaining compatibility with the 68K architecture. Target markets include servers, X-terminals, graphics low-end workstations, high-performance embedded applications.

Competitive Advantages:

Intel 486—Dominates PC-DOS market

Weaknesses: 25-MHz 68040 outperforms 50-MHz 486 in both Ingram Labs and *PC Week* benchmarks. Numerous clones confuse functional and performance issues.

IDT 3051/52—Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states. Limited range of development tools compared to 68K

AMD29030/35—Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multi-processor system

Literature:

Title	Order Number
MC68040 Technical Summary	MC68040/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

MC68150—Dynamic Bus Sizer
MC68307—Slave Mode
MC88915/MC88916—Clock Driver
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68040	179-Lead RC	25,33, 40	—	—	1	1	10	
	184-Lead FE	25, 33, 40	—	—	0	24	96	SPAK040FEXX

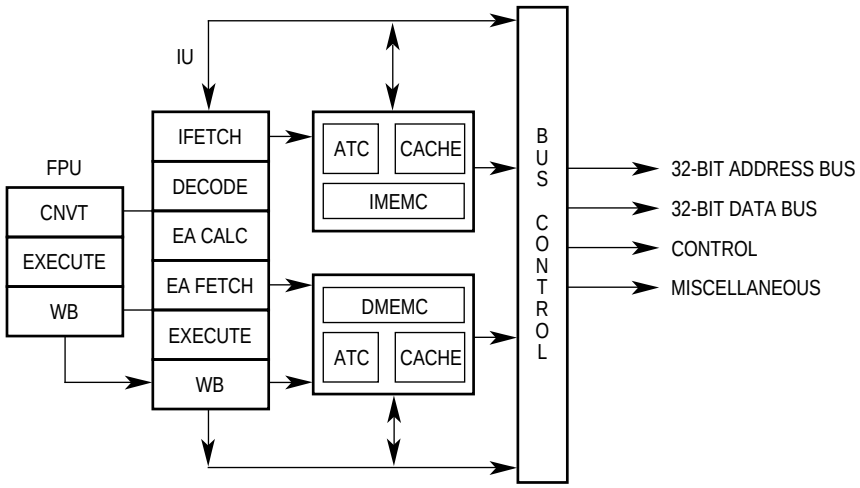
NOTE: FE = Ceramic Quad Flat Pack (CQFP)
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
2E42K	—	80%	MOS11	0.65µ	Production	No	Yes	See addendum to user's manual on AESOP
2E31F	M	80%	MOS11	0.65µ	Canceled	Yes	Yes	
OE31F	M	80%	MOS11	0.65µ	Canceled	Yes	Yes	
7D98D	E	75%	MOS8	0.8µ	Canceled	Yes	—	
D43B	B	75%	MOS8	0.8µ	Canceled	Yes	—	
4D50D	A	75%	MOS8	0.8µ	Canceled	Yes	—	
5D98D	E	75%	MOS8	0.8µ	Canceled	Yes	Yes	100 C test temperature only at this time
9D50D	B	75%	MOS8	0.8µ	Canceled	Yes	—	

MC Qualification Date: 2Q95
Die Size: 473 × 500
Devices: Sites = 1,170,000; Active = 844,000
Process: HCMOS

XC68040V



Features:

- Low Voltage (3.3v), Low Power (1.5 watts @ 33 MHz)
- Low-Power Mode for Full Power-Down Capatibility (660uW)
- Full Static Design
- Dual Input/Output Voltage Compatibility (3.3 V & 5 V TTL)
- Identical Code to the MC68040 plus LPSTOP Command for Power Down
- Non-Multiplexed 32-Bit Address Bus, 32-Bit Data Bus
- 4K-Byte On-Chip Instruction Cache
- 4K-Byte On-Chip Data Cache
- 26.1 MIPS Integer Performance at 25 MHz
- Burst Memory Interface
- On-Chip Memory Management Unit

Target Markets/Applications:

The principle target for the MC68040V is for all high-performance, power-sensitive, general computing and embedded processing applications.

Competitive Advantages:

Intel 960CA/F: Marketed as a RISC high-end solution

Weaknesses: High-Power consumption and less performance RISC machine intolerant of wait states, requires expensive high speed SRAM. Poor IDT 3051/52, 3081/3082: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states, requires expensive high-speed SRAM. High-power consumption

AMD29030/35—Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multiprocessor system. RISC machine intolerant of wait states, requires expensive high-speed SRAM. High-power consumption

Literature:

Title	Order Number
MC68040 VT Product Brief	MC68040V/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
The 68K Source	BR729/D
3.3 Volt Logic and Interface Circuits	BR1407/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module
In-Circuit emulation—Applied Microsystems

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

MC68150—Dynamic Bus Sizer
MC88915/MC88916/MC8892—Clock Driver
Crystals—Champion, Kyocera, ACT
National NM27C6841 Burst EPROM
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68040V	179-Lead RC	25,33	—	—	0	1	0	
	184-Lead FE	25, 33	—	—	1	21	0	SPAK040FEXXV

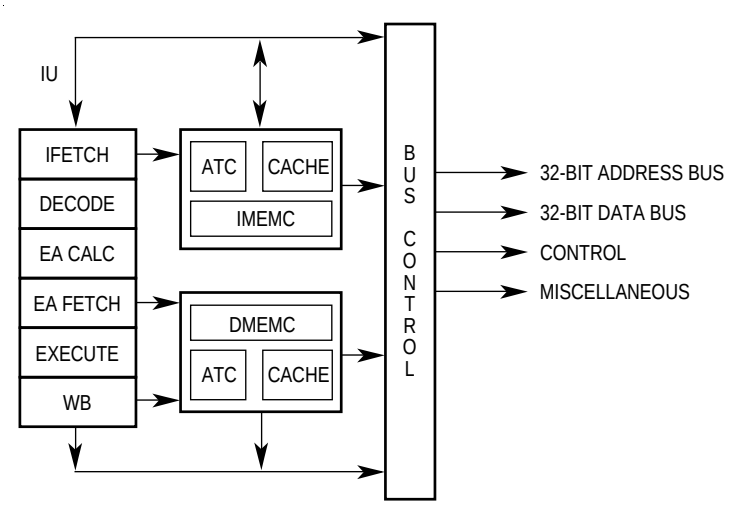
NOTE: FE = Ceramic Quad Flat Pack (CQFP)
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History:

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
0F54F	—	80%	MOS11	.5 TLM	Sampling	Yes	No	
6D33T	—	80%	MOS11	.5 TLM	Canceled	Yes	No	

MC Qualification Date: 2Q96
Die Size:
Devices:
Process: .5µ TLM

MC68EC/LC040



Features:

- 32-Bit Address Bus, 32-Bit Data Bus
- 4-Kbyte On-Chip Instruction Cache
- 4-Kbyte On-Chip Data Cache
- 27.4 MIPS at 25 MHz
- Burst Memory Interface
- On-Chip Memory Management on LC040 Only

Target Markets/Applications:

The MC68EC/LC040 is well suited for all high-end embedded control applications that require high performance, low cost, and memory management.

Competitive Advantages:

Intel 486SX: Lowest cost 486 entry point

Weaknesses: No acceptance outside of DOS compatible marketplace.

IDT 3051/52: Aggressive pricing, high performance, surface mount

Weaknesses: Multiplexed bus requires external components. RISC machine intolerant of wait states. Limited development tool support compared to 68K.

AMD29030/35: Aggressive pricing, 4K/8K instruction cache

Weaknesses: No data cache. Very high bus usage. No support for multi-processor system.

Literature:

Title	Order Number
MC68LC040 Technical Summary	MC68LC040/D
MC68EC040 Technical Summary	MC68EC040/D
M68040 User's Manual	M68040UM/AD Rev 1
M68000 Programmer's Reference Manual	M68000PM/AD
68000 Microprocessor Family	BR1115/D

Support Tools:

M68EC040IDP—Integrated Development Platform: hardware/software evaluation module

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Support Chips:

68150—Dynamic Bus Sizer
MC68307—Slave Mode
MC68360—Integrated Communication Controller
MC88915/MC88916—Clock Driver
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68EC040	179-Lead RC	20, 25, 33	—	—	1	1	10	
MC68LC040	184-Lead FE	20, 25, 33	—	—	0	24	96	SPAKLC040FEXX

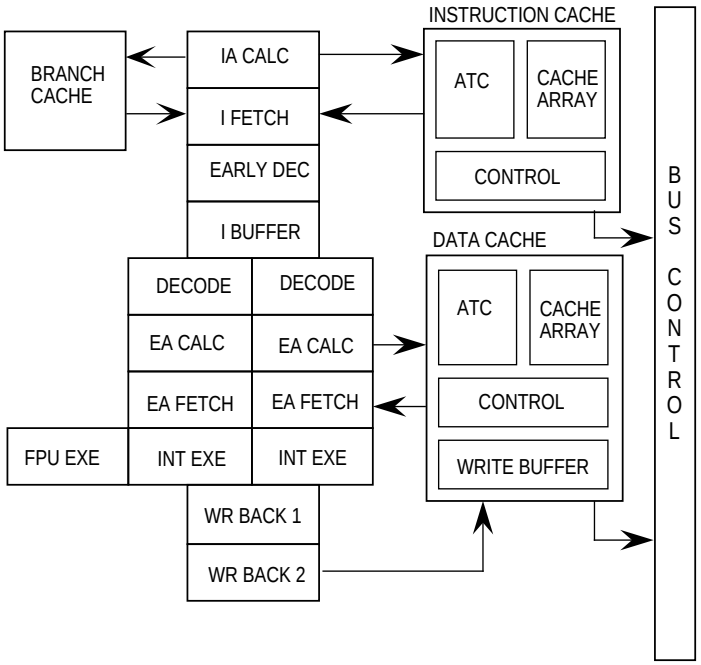
NOTE: FE = Ceramic Quad Flat Pack (CQFP)
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
2E71M	—	80%	MOS11	0.65µ	Production	No	Yes	See Addendum User's Manual on AESOP
2E23G	B	80%	MOS11	0.65µ	Canceled	Yes	—	XC orders supplied in 2E23G
D39H	A	75%	MOS8	0.8µ	Canceled	Yes	No	

MC Qualification Date: 4Q95
Die Size: 461.4 × 431.6
Devices: Sites = 777,092
Process: HCMOS

XC68060



Features:

- Greater than 50 Integer SPECmarks at 50 MHz
- Dual Issue Execution Pipeline
- 32-Bit Address Bus, 32-Bit Data Bus
- 8-Kbyte On-Chip Instruction Cache
- 8-Kbyte On-Chip Data Cache
- 256-Entry Branch Cache
- On-Chip Floating-Point Support
- On-Chip Memory Management
- Burst Memory Interface
- Designed for Low Power
- 3.3 Volt Operation

Target Markets/Applications:

The 68060 is well suited for all applications that require very high integer and floating-point performance while still retaining compatibility with the 68K architecture.

Competitive Advantages:

Intel Pentium: Dominates PC-DOS market

Weaknesses: Requires 64-bit bus.

68060: Superior integer performance with low-cost memory system

Literature:

Title	Order Number
MC68060 Product Brief	MC68060/D
M68060 User's Manual	M68060UM/AD
M68000 Family Brochure	BR1115/D Rev 1
M68060 Family Brochure	BR1153/D

Support Tools:

M68060IDP—Integrated Development Platform: hardware/software evaluation module. Available 2Q95.

Support Chips:

MC68150—Dynamic Bus Sizer
MC88926—Clock Driver
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68060	206-Lead RC	50	—	—	1	1	10	

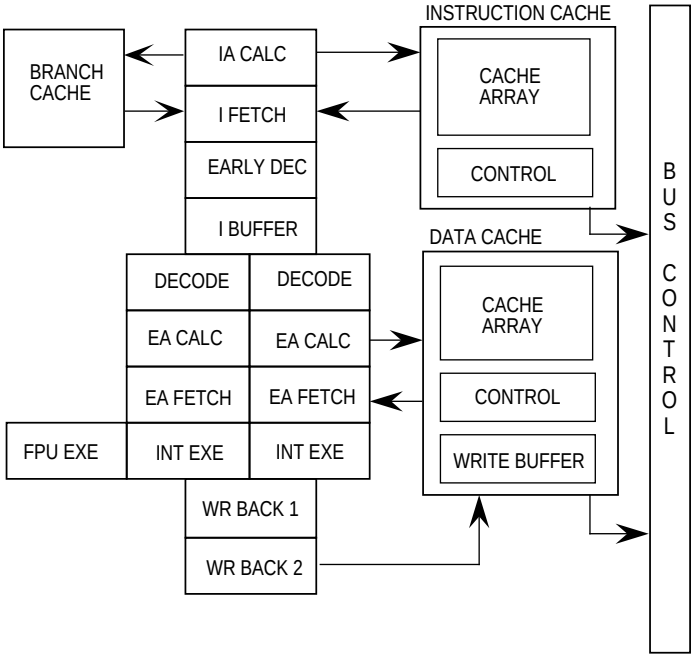
NOTE: RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1F43G	C	85%	MOS11	0.5µ	Production	Yes	—	
0F43G	B	85%	MOS11	0.5µ	Canceled	Yes	—	
D11W	A	85%	APRDL	0.5µ	Canceled	Yes	—	

First Silicon: Dec 1993
XC Qualification Date: 1Q95
Die Size: 582 × 579
Devices: Active = 2,530,000
Process: HCMOS

XC68EC060



Features:

- Greater than 50 Integer SPECmarks at 50 MHz
- Dual-Issue Execution Pipeline
- 32-Bit Address Bus, 32-Bit Data Bus
- 8-Kbyte On-Chip Instruction Cache
- 8-Kbyte On-Chip Data Cache
- 256-Entry Branch Cache
- Burst Memory Interface
- Designed for Low Power
- 3.3 Volt Operation

Target Markets/Applications:

The 68EC060 is suited for high-end embedded control applications that require high performance low cost. Target markets include high-speed LAN controllers (Ethernet, FDDI, X.25, etc.), I/O processors, laser printers, X-terminals, routers, bridges, etc.

Competitive Advantages:

Intel Pentium: Dominates PC-DOS market

Weaknesses: Requires 64-bit bus.

68060: Superior integer performance with low-cost memory system

Literature:

Title	Order Number
MC68060 Product Brief	MC68060/D
M68060 User's Manual	M68060UM/AD
M68060 Family Brochure	BR1153/D

Support Tools:

M68060IDP—Integrated Development Platform: hardware/software evaluation module. Available 2Q95.

Support Chips:

MC68150—Dynamic Bus Size
MC88926—Clock Driver
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68EC060	206-Lead RC	50	C	—	1	1	10	

NOTE: RC = Pin Grid Array (PGA), Gold Lead finish

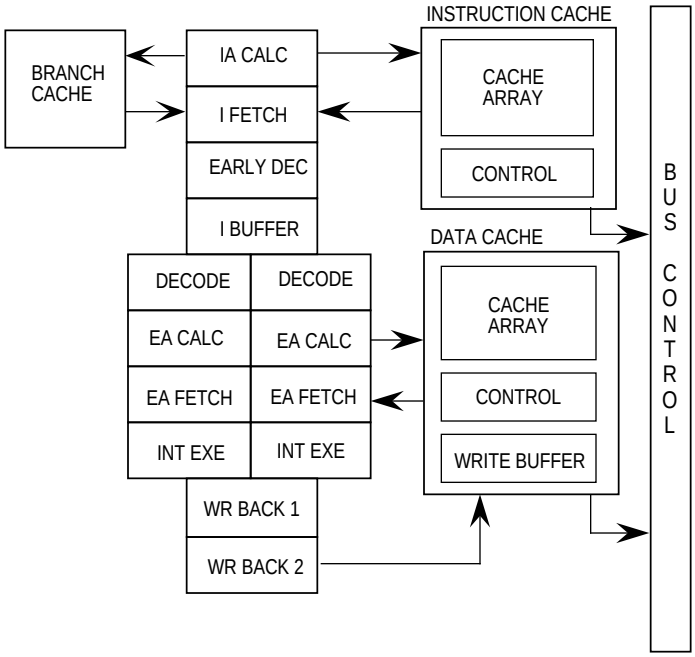
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1F43G	C	85%	MOS11	0.5µ	Production	Yes	—	
0F43G	B	85%	MOS11	0.5µ	Canceled	Yes	—	
D11W	A	85%	APRDL	0.5µ	Canceled	Yes	—	EC060s temp. sourced from full '060 mask

First Silicon: Dec 1993
XC Qualification Date: 1Q95
Die Size: 582 × 579
Devices: Active = 2,530,000
Process: HCMOS

XC68LC060



Features:

- Greater than 50 Integer SPECmarks at 50 MHz
- Dual-Issue Execution Pipeline
- 32-Bit Address Bus, 32-Bit Data Bus
- 8-Kbyte On-Chip Instruction Cache
- 8-Kbyte On-Chip Data Cache
- 256-Entry Branch Cache
- Burst Memory Interface
- On-Chip Memory Management
- Designed for Low Power
- 3.3 Volt Operation

Target Markets/Applications:

The 68LC060 is well suited for all high-end embedded control applications that require high performance, low cost, and the function of memory management.

Competitive Advantages:

Intel Pentium: Dominates PC-DOS market

Weaknesses: Requires 64-bit bus.

68060: Superior integer performance with low-cost memory system

Literature:

Title	Order Number
MC68060 Product Brief	MC68060/D
M68060 User's Manual	M68060UM/AD
M68060 Family Brochure	BR1153/D

Support Tools:

M68060IDP—Integrated Development Platform: hardware/software evaluation module. Available 2Q95.

Support Chips:

MC68150—Dynamic Bus Sizer
MC88926—Clock Driver
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM62940 Burst Mode SRAM

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68LC060	206-Lead RC	50, 66	—	—	1	1	10	

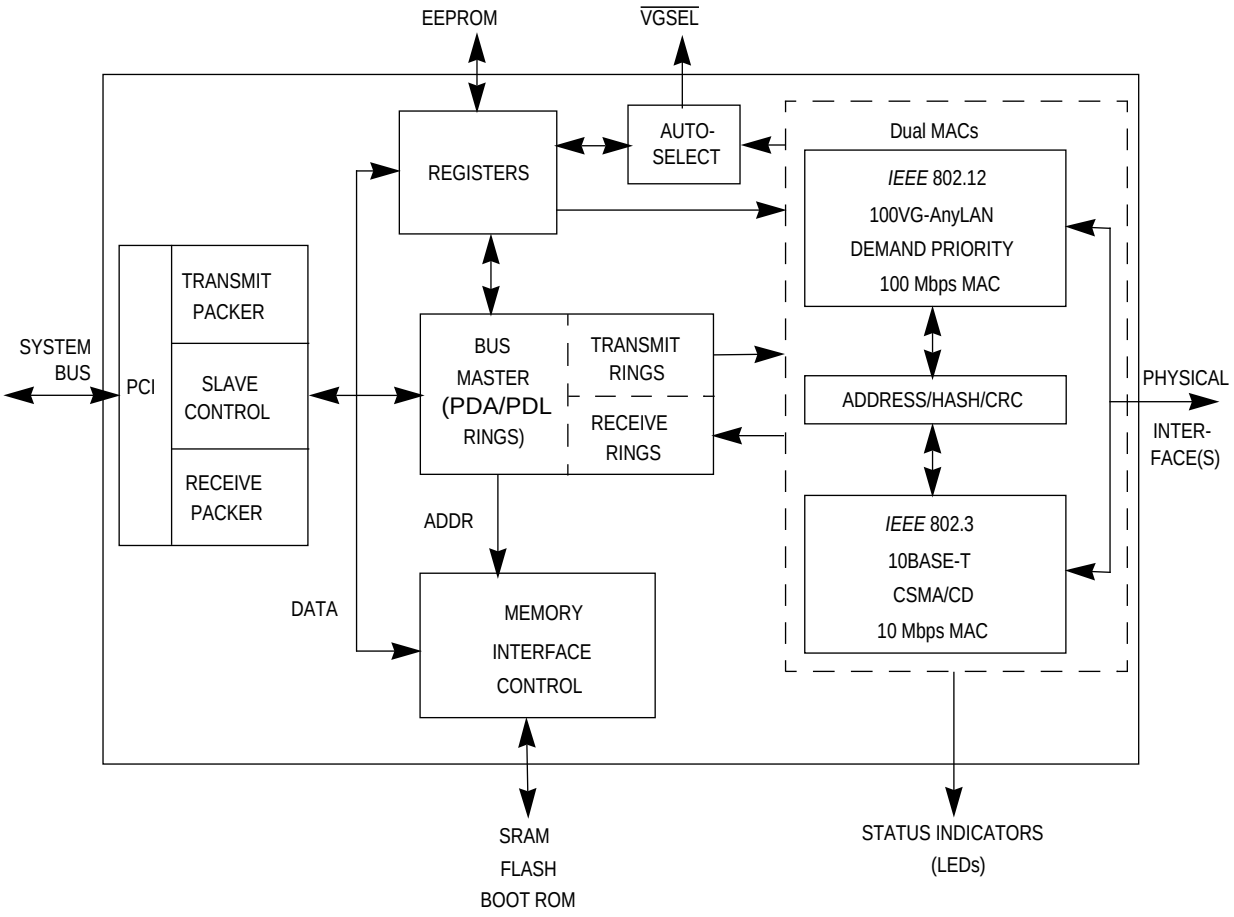
NOTE: RC = Pin Grid Array (PGA), Gold Lead finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1F43G	C	85%	MOS11	0.5µ	Production	Yes	—	
0F43G	B	85%	MOS11	0.5µ	Canceled	Yes	—	
D11W	A	85%	APRDL	0.5µ	Canceled	Yes	—	LC060s temp. sourced from full 060 mask

First Silicon: Dec 1993
XC Qualification Date: 1Q95
Die Size: 582 × 579
Devices: Active = 2,530,000
Process: HCMOS

XC68852 PCI MASTER INTERFACE



Features:

- IEEE 802.12 100VG - AnyLAN Media Access Control Specification
  - —Enables 100-Mbps Transmission over UTP, STP and Fiber
  - —Supports Token Ring and Ethernet Formatted Packets
  - —Supports Multimedia Applications with Two Levels of Priority
- Dual Media Access Controllers Included for 100VG-AnyLAN and 10BASE-T
- Integration of 10BASE-T Signals with the 100VG-AnyLAN MII Allows for Single Connector 10Mbps/100-Mbps Designs with Automatic Speed Detection
- 132-Mbytes Transfer Rate (PCI)
- Address Recognition of Broadcast, Multicast, and Station Addressed Packets
- LED Interface for Activity and Status Indicators
- 5-Volt Operation

Target Markets/Applications:

The XC68852 fully implements the IEEE 802.12 100VG-AnyLAN standard and the IEEE 802.3 10BASE-T standard. This chip offers a high-integrated, high-performance, low-cost solution for 100 Mbps network adapter card applications. The 100VG-AnyLAN IEEE 802.12 standard supports all popular cable types, is a superset of Ethernet and Token Ring topologies, and provides guaranteed bandwidth for emerging applications such as multimedia

Competitive Advantages:

TI—ThunderLAN chip (PCI only) is higher priced, but supports 10BASE-T, 100VG-AnyLAN and 100BASE-T.

Literature:

Title	Order Number
M68852 Product Brief	MC68852/D

Package/Speed Options:

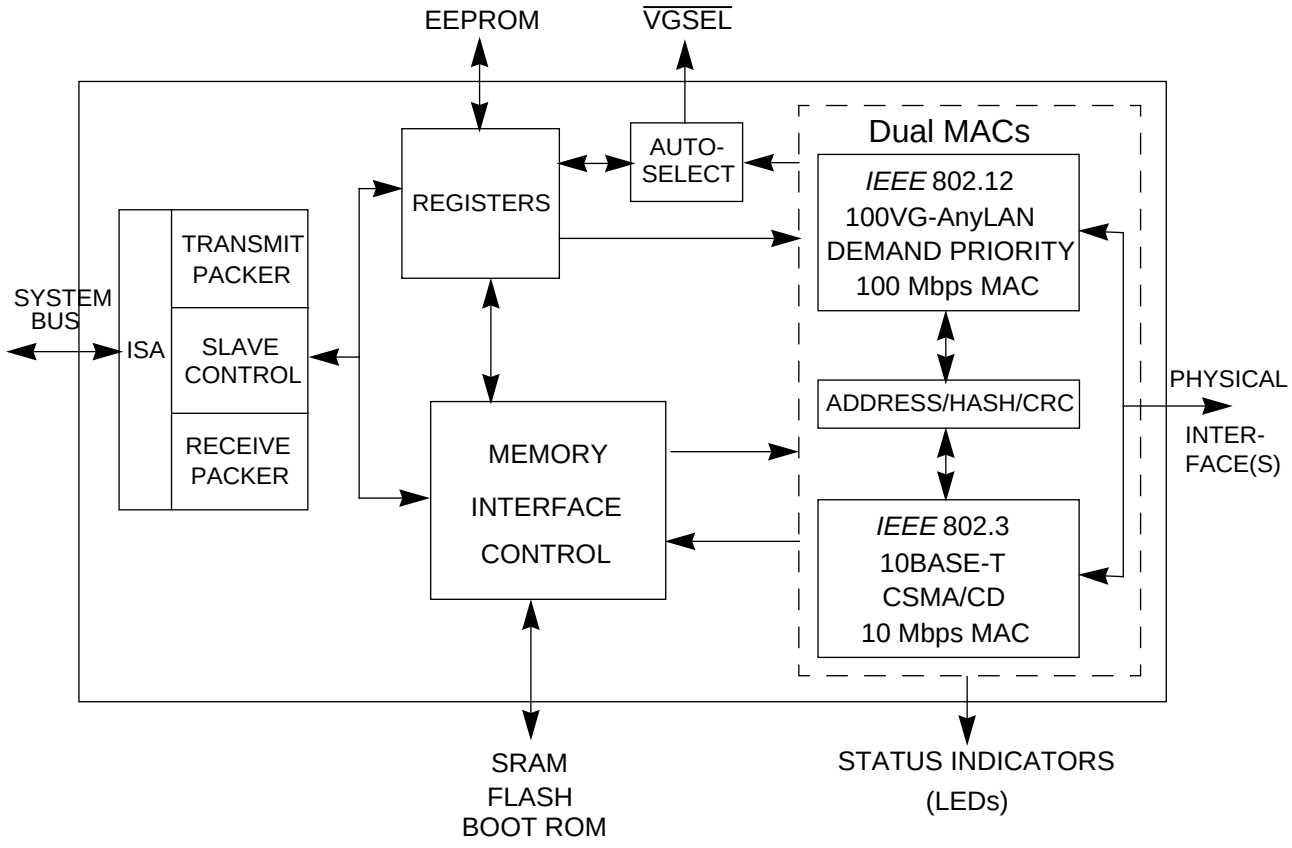
Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68852	160-Lead FT	33	—	0 to 70	—	—	—	SPAK852FT

NOTE: FT = Plastic Quad Flat Pack (PQFP)

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

First Silicon: Sept 1995
MC Qualification Date: 2Q96
Die Size: 306 × 306
Devices:
Process: .65µ TLM HCMOS

PC68853 ISA SYSTEM INTERFACE



Features:

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  - —Supports Multimedia Applications with Two Levels of Priority
- Dual Media Access Controllers Included for 100VG-AnyLAN and 10BASE-T
- Integration of 10BASE-T Signals with the 100VG-AnyLAN MII Allows for Single Connector 10Mbps/100-Mbps Designs with Automatic Speed Detection
- 8-Mbytes Transfer Rate (ISA)
- Address Recognition of Broadcast, Multicast, and Station Addressed Packets
- LED Interface for Activity and Status Indicators
- 5-Volt Operation

Target Markets/Applications:

The PC68853 fully implements the IEEE 802.12 100VG-AnyLAN standard and the IEEE 802.3 10BASE-T standard. This chip offers a high-integrated, high-performance, low-cost solution for 100 Mbps network adapter card applications. The 100VG-AnyLAN IEEE 802.12 standard supports all popular cable types, is a superset of Ethernet and Token Ring topologies, and provides guaranteed bandwidth for emerging applications such as multimedia

Competitive Advantages:

AT&T:—Poor support. Combined EISA/ISA chip is higher priced due to EISA overhead.

Literature:

Title	Order Number
M68853 Product Brief	MC68853/D

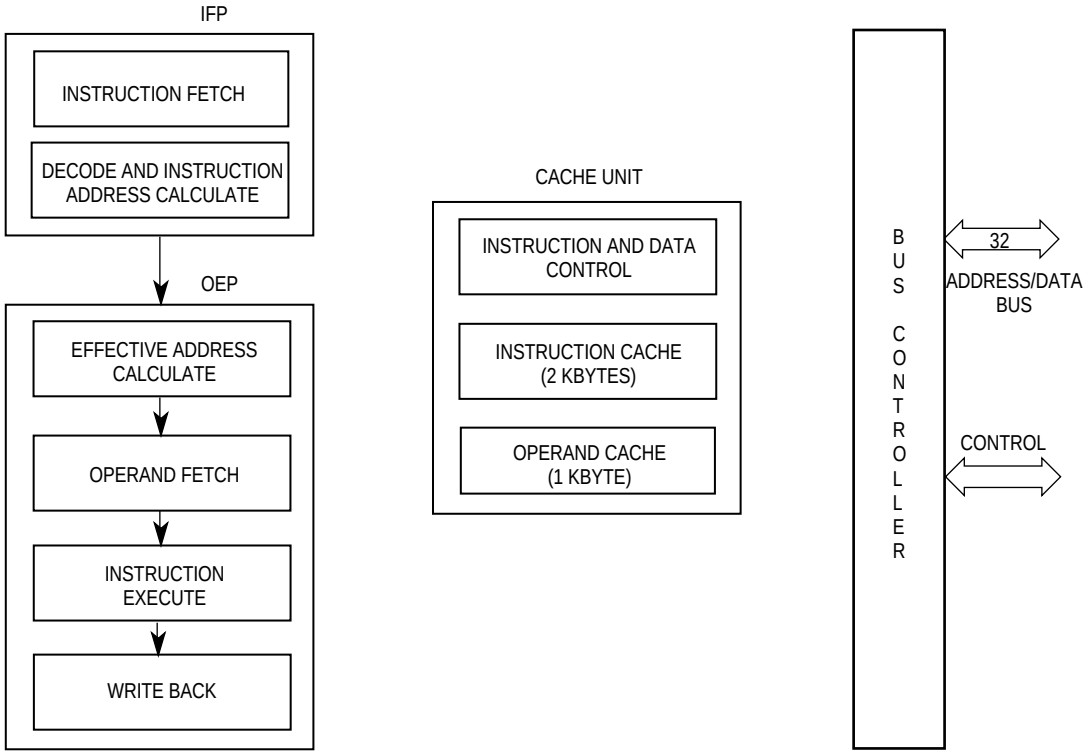
Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
PC68853	144-Lead PV	33	—	0 to 70	—	—	—	SPAK853PV

NOTE: PV = Thin Quad Flat Pack (TQFP)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

First Silicon: Nov 1995
MC Qualification Date: 2Q96
Die Size: 204 × 236
Devices:
Process: .65µ TLM HCMOS

XCF5102



Features:

- High Integer Performance
  —1 Instruction Per Clock Peak Performance
- Full Static Design Allows Operation Down to DC to Minimize Power Consumption
- On-Chip Caches
  —2K-bytes Instruction Cache
  —1K-bytes Data Cache
- 4 Separate Access Control Registers
- Simple Instruction Set Architecture
  —16 User Visible 32-Bit Wide Registers
  —User-mode Compatible with M68K Instruction Set
  —Supervisor / User Modes For System Protection
  —Vector Base Register To Relocate Exception Vector Table
  —Optimized For High Level Language Constructs
- Low Interrupt Latency
- Multiplexed 32-Bit Address and 32-Bit Data Bus To Minimize Board Space and Interconnections

- 3.3-Volt Operation
- 5-Volt TTL Compatible, 5-Volt CMOS Tolerant
- Three-State Pin
- Snoop
- JTAG IEEE 1149.1
- Single Bus Clock Input
- Fast Locking PLL

Target Markets/Applications:

The XCF5102 is fully ColdFire code compatible. As the first chip in the ColdFire Family, it has been designed with special capabilities that allow it to also execute the M68000 code that exists today. These extensions to the Coldfire instruction set allow Motorola customers to utilize the XCF5102 as a bridge to future ColdFire processors for applications requiring the advantages of a variable-length RISC architecture. Compatibility with existing development tools such as compilers, debuggers, real-time operating systems and adapted hardware tools offers XCF5102 developers access to a broad range of mature tool support; enabling an accelerated product development cycle, lower development costs and critical time-to-market advantages for Motorola customers.

Literature:

Title	Order Number
MCF5102UM/AD	MCF5102 User's Manual
M68000PM/AD	M68000 Family Programmer's Reference Manual

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XCF5102	144-Lead PV	16, 20, 25	A	—	0	60	300	SPAK5102PVXXA

NOTE: PV = Thin Quad Flat Pack (TQFP)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

M68300 FAMILY STRATEGY

The M68300 Family consist of highly integrated processors aimed at the embedded computing and control market. The core processor is either the 68000 (MC68302, MC68306, MC68307, MC68322, MC68328) the CPU32 (MC68330, MC68340, MC68341), or the CPU32+ (MC68349, MC68360) which is a derivative of the MC68020.

The M68300 Family is the dominant 32-bit architecture in the area of integrated processors. This is achieved via the ongoing matching of Motorola capabilities to customer needs with particular focus in the following markets:

CONSUMER—CD-I, information terminals, global positioning (navigation aids) and personal computing.

COMMUNICATIONS—Network control and portable applications such as phones.

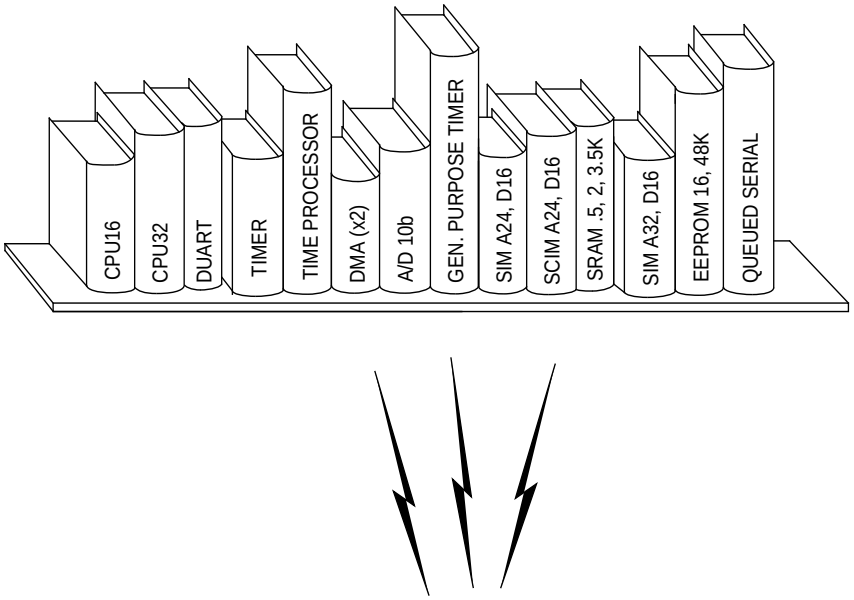
OFFICE EQUIPMENT—Copiers, network interfaces, portable computers and personal information computers.

AUTOMOTIVE—Engine and transmission management and navigation systems.

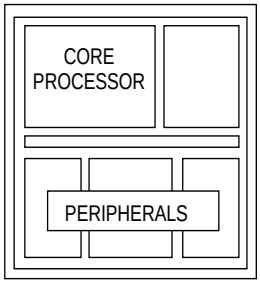
PORTABLE INSTRUMENTS—Measuring, monitoring, medical, inventory control, and computers.

Much of the M68300 Family is based around the intermodule bus (IMB), which allows the device to be assembled from a library of peripheral modules as shown in the following illustration.

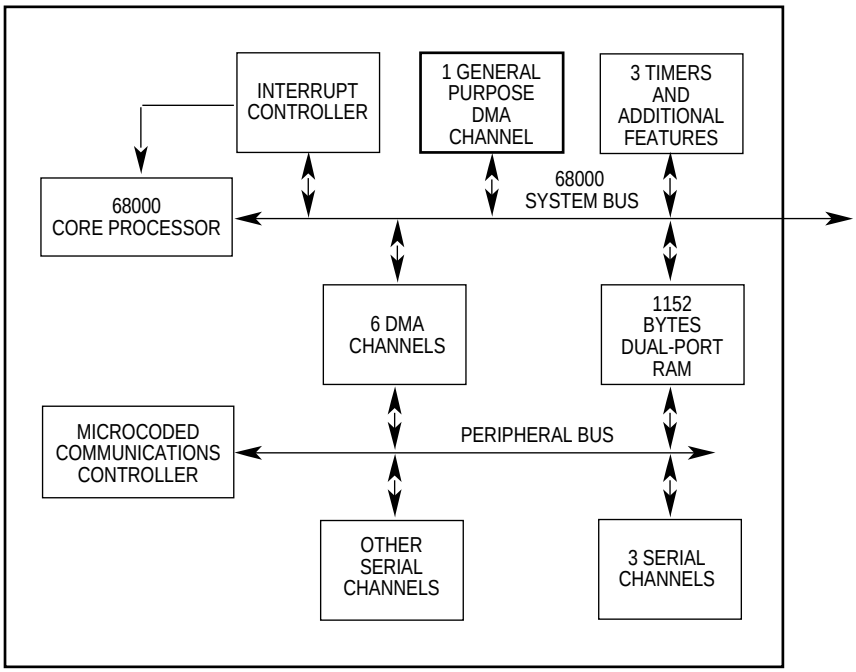
PERIPHERAL LIBRARY



68300



MC68302



Features:

- 68000 Core Processor
- System Integration Block
- RISC Communications Processor
- 3 SCC’s
- Slave Mode Option to Disable 68000

Target Markets/Applications:

- Modems
- Computer I/O Subsystems
- Routers and Bridges
- Switching Networks
- ISDN
- Industrial Control

Literature:

Title	Order Number
MC68302 User's Manual (Rev 2)	MC68302UM/AD
MC68302 Technical Summary (Rev 2)	MC68302/D
MC68302 Development Tools Technical Summary	BR469/D
M68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

MC68195 LocalTalk Adapter for the MC68302—The MC68195 interfaces the MC68302 to AppleTalk. Order as MC68195FN.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

M68302ADS—Application Development System
M68302ADI—Host Interface Card
M68302ICERC—PGA Target Cable

Package/Speed Options:

Commercial Temperatures (0 to 70°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68302	132-Lead RC	16, 20, 25	C	—	1	1	14	
	132-Lead FC	16, 20, 25	C	—	0	36	144	SPAK302FCXXC
	144-Lead PV*	16, 20	C	—	0	60	300	SPAK302PVXXC

NOTE: FC = Plastic Quad Flat Pack (PQFP)
PV = Thin Quad Flat Pack (TQFP)
RC = Pin Grid Array (PGA), Gold Lead Finish
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

*Available in 3.3V V_{CC}

Industrial Temperatures (-40 to +85°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68302CRC	132-Lead PGA	16, 20	C	–40 to 85	0	1	14	
MC68302CFC	132-Lead PQFP	16, 20	C	–40 to 85	0	36	144	SPAK302CFCXXC

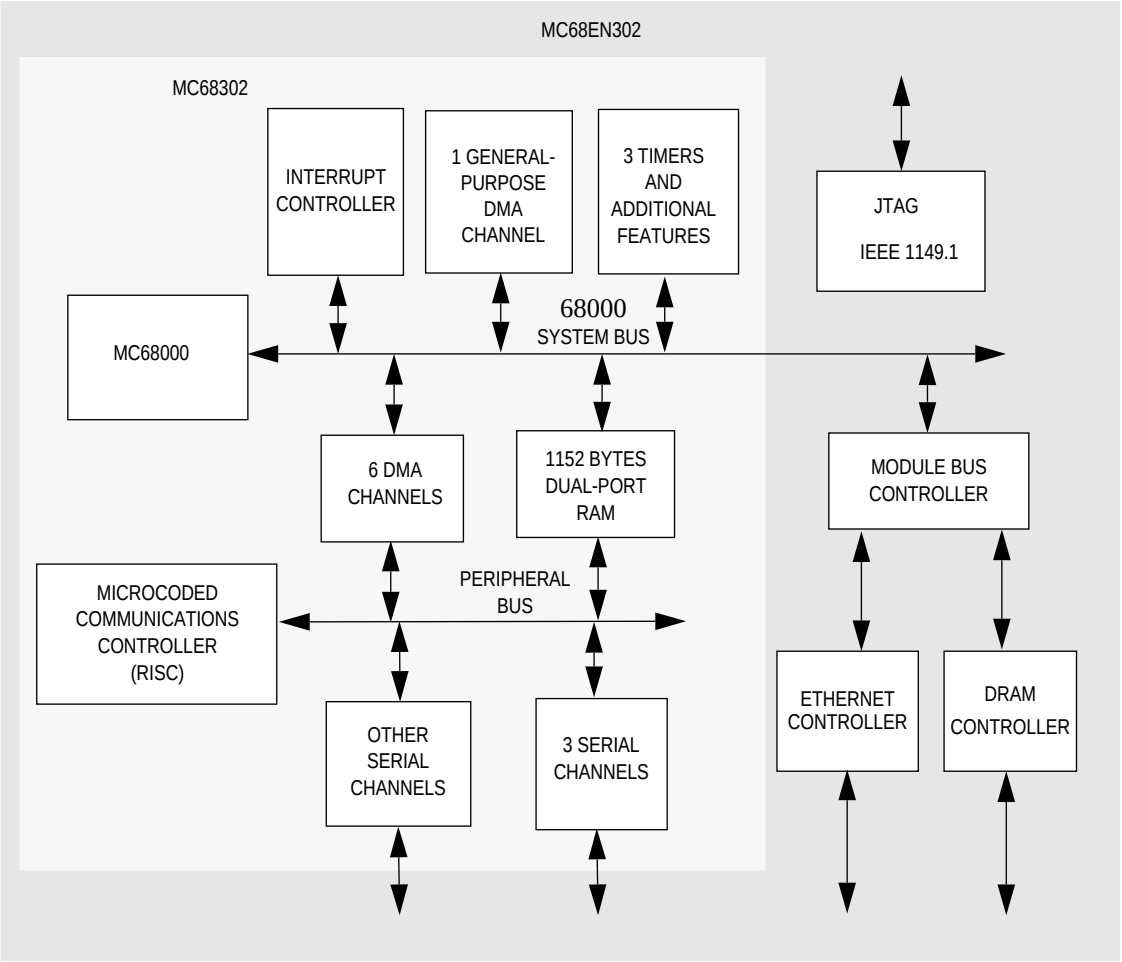
NOTE: CXX = Extended Temperatures

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1F26E	C	—	MOS11	0.65µ	Production	Yes	Yes	Shrink; plastic package, ceramic
1C65T	C	—	MOS8	0.8µ	Canceled	Yes	Yes	Shrink; ceramic package
4B14M	B	—	MOS8	1.0µ	Canceled	Yes	—	Double-layer metal

First Silicon: 2Q89
MC Qualification Date: 3Q89
Die Size: 258 × 251
Device: Sites = 320,000; Active = 210,000
Process: CMOS

XC68LC302



Features:

- 68EC000 Core CPU (16, 20, or 25 MHz)
- System Integration: 3 Timers Including a Watchdog, Independent DMA Controller, 1152 Bytes of Dual-Port Static RAM, 4 Chip Selects (CS), Interrupt Controller, Parallel Input/Output (I/O) Ports, On-Chip Clock Generator with Output Signal, Periodic Interrupt Timer (PIT).
- Communications Processor: RISC-Based Communications controller, Serial Communication Channels Each Supporting HDLC/SDLC, UART, BISYNC, AUTOBAUD, and Transparent Modes, 4 Serial DMAs for the 2 SCCs, SCP for Synchronous Coummnications, Flexible Physical Interface Including IDL, NMSI, GCI, and PCM. Two Serial Management Controllers to Support IDL & GCI Auxiliary Channels.
- Available in Low Voltage (MC68LC302V)
- Low-Power Features: On-Chip Phase Lock Loop (PLL), Low-Power Modes in µA Range

Target Markets/Applications:

- V.32 bis and V.34 Modems (Internal, External, or PCMCIA)
- Switching Networks
- ISDN
- Industrial Control
- Portable/Handheld Devices
- Cable Interface Units

Literature:

Title	Order Number
MC68LC302 Reference Manual	MC68LC302RM/AD
MC68LC302 Technical Summary	MC68LC302/D
MC68302 Development Tools Technical Summary	BR469/D
M68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

MC68195 LocalTalk Adapter for the XC68LC302—The MC68195 interfaces the XC68LC302 to AppleTalk. Order as MC68195FN.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

M68302FADS—Family Application Development System
M68302ADI—Host Interface Card

Package/Speed Options:

Commercial Temperatures (0 to 70°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68LC302	100-Lead PU	16*, 20*, 25	B	—	0	84	420	SPAKLC302PUXXB

NOTE: PU = Thin Quad Flat Pack

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

*Available in 3.3V V_{CC}

Industrial Temperatures (-40 to +85°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68LC302CPU	100-Lead TQFP	16*, 20*	B	–40 to 85	0	84	420	

NOTE: CPU = Extended Temperatures

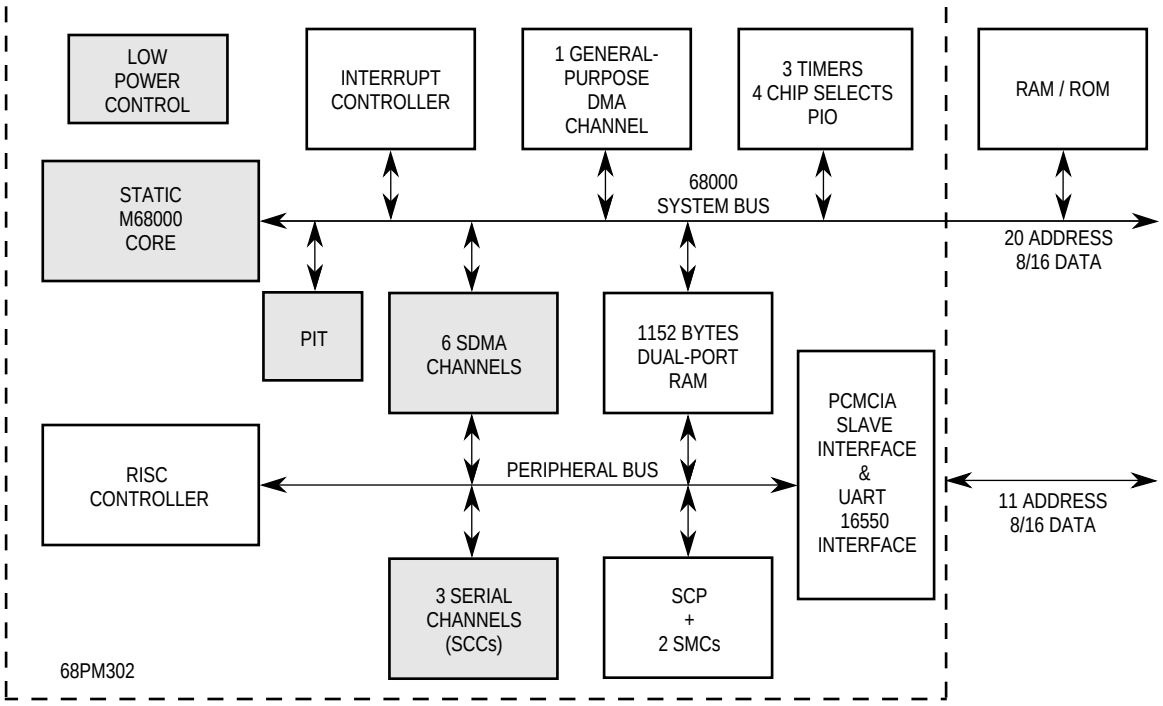
*Available in 3.3 V V_{CC}

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
E65C	—	—	MOS11	0.65µ	Production	Yes	Yes	
F81S	B	—	MOS11	0.65µ	Samples	Yes	Yes	Lower Power Core

First Silicon: 1Q95
MC Qualification Date:
Die Size: 258 × 251
Device: Sites = 320,000; Active = 210,000
Process: CMOS

XC68PM302



Features:

- 68EC000 Core CPU (16, 20, or 25 MHz)
- System Integration: 3 Timers Including a Watchdog, Independent DMA Controller, 1152 Bytes of Dual-Port Static RAM, 4 Chip Selects (CS), Interrupt Controller, Parallel Input/Output (I/O) Ports, On-Chip Clock Generator with Output Signal, Periodic Interrupt Timer (PIT).
- Communications Processor: RISC-Based Communications controller, 3 Serial Communication Channels Each Supporting HDLC/SDLC, UART, BISYNC, AUTOBAUD, and Transparent Modes, 6 Serial DMAs for the 3 SCCs, SCP for Synchronous Coummnications, Flexible Physical Interface Including IDL, NMSI, GCI, and PCM. Two Serial Management Controllers to Support IDL & GCI Auxiliary Channels.
- PCMCIA Controller: Slave Interface with 8- or 16-Bit Data, 11-Bit Addressing, Compatible with PC Card Classic Specification.
- 16550 Emulation Block: Complete Hardware and Software Emulation of 16550 UART.
- Available in Low Voltage (MC68PM302V)
- Low-Power Features: On-Chip Phase Lock Loop (PLL), Low-Power Modes in µA Range

Target Markets/Applications:

- PCMCIA Modems (V.32 bis, V.34 and GSM)
- Wireless LAN Cards
- ISDN
- CDPD Cards
- Portable/Handheld Devices

Literature:

Title	Order Number
MC68PM302 Reference Manual	MC68PM302RM/AD
MC68PM302 Technical Summary	MC68PM302/D
MC68302 Development Tools Technical Summary	BR469/D
M68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

MC68195 LocalTalk Adapter for the XC68PM302—The MC68195 interfaces the XC68PM302 to AppleTalk. Order as MC68195FN.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

M68302FADS—Family Application Development System
M68302ADI—Host Interface Card

Package/Speed Options:

Commercial Temperatures (0 to 70°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MOQ	POQ	
XC68PM302	144-Lead PV*	16*, 20*, 25	B	—	0	60	300	SPAKPM302PVXXB

NOTE: PV = Thin Quad Flat Pack (TQFP)

*Available in 3.3V V_{CC}

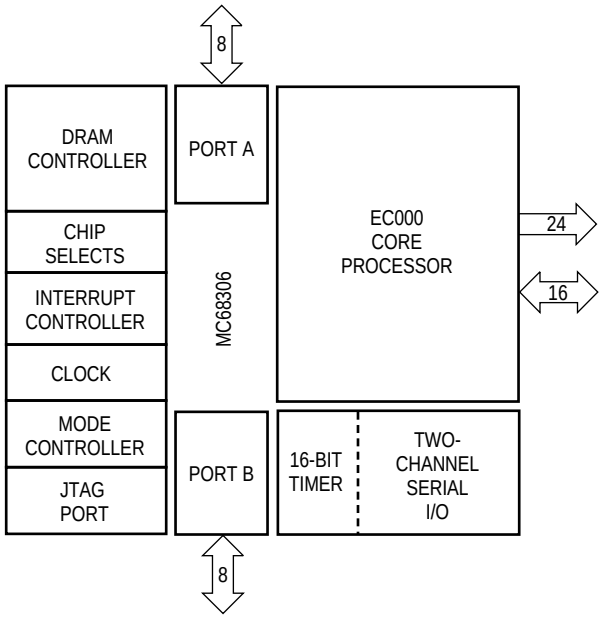
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
E66C	—	—	MOS11	0.65µ	Canceled	Yes	Yes	
F80S	B	—	MOS11	0.65µ	Production	Yes	Yes	Lower Power Core, Bootstrap

First Silicon: 1Q95
MC Qualification Date:
Die Size: 310 × 282
Device: Active = 273,000
Process: CMOS

MC68306



Features:

- EC000 Core CPU
- 68681 Two-Channel Serial UART
- DRAM Controller
- 16 Parallel I/O
- 2.7 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68306 is currently the only integrated device with a DRAM controller priced at less than $10. As such, it holds broad appeal to designers of 68000-based systems. The integrated features, particularly the DRAM controller, simplify system design and speed time-to-market.

Competitive Advantages:

Intel 80186: Slightly lower price, similar processor performance

Weaknesses: Mulitplexed address and data buses. No DRAM controller. Segmented architecture.

Toshiba 68301, 68303: Similar price, similar processor performance

Weaknesses: No DRAM controller

Literature:

Title	Order Number
MC68306 Product Brief	MC68306/D
MC68306 User's Manual	MC68306UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

None needed

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68306	132-Lead FC	16	—	—	0	36	144	SPAK306FCXX
	144-Lead PV	16	—	—	0	60	600	SPAK306PVXX

NOTE: FC = Plastic Quad Flat Pack (PQFP)
PV = Thin Quad Flat Pack (TQFP)

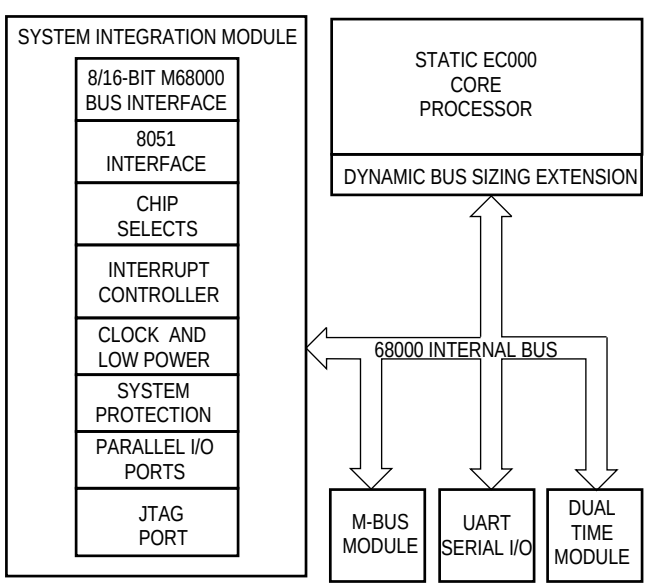
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
E94M	4	75%	MOS8	0.8µ	Production	Yes	—	Fab process improvements “MC” rev
E94M	3	75%	MOS8	0.8µ	Discontinued	Yes	—	
E94M	2	75%	MOS8	0.8µ	Canceled	Yes	—	
E94M	1	75%	MOS8	0.8µ	Canceled	Yes	—	

First Silicon: 1Q93
MC Qual Date: Nov 1994
Die Size: 293 × 225
Device: 111,000
Process: HCMOS

XC68307/XC68307V



Features:

- Static EC000 Core CPU
- 8051 Interface
- M-Bus (I2C) Interface
- 68681 Type UART
- 8 Chip Selects
- Interrupt Controller
- 24 Programmable I/O
- Watch Dog Timer
- JTAG Testability
- 2.7 MIPS Performance at 16 MHz

Target Markets/Applications:

The 68307 holds a broad appeal to designers of 68000 systems. Some applications include system upgrades, computer I/O subsystems, portable phones, DECT, GSM basestations, and POS terminals.

Competitive Advantages:

Intel 80186: Slightly lower price, similar processor performance

Weaknesses: One less serial channel, no DMA

Toshiba 68301, 68303: Similar price, similar processor performance

Weaknesses: One less serial channel, no DMA

Literature:

Title	Order Number
MC68307 Technical Summary	MC68307/D
MC68307 User's Manual	MC68307UM/AD (2Q94)
M68000 Programmer's Reference Manual	M68000PM/AD
M68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

Software support provided through various third-party vendors of 68000 software tools.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

None needed

Package/Speed Options:

Commercial Temperatures (0 to 70°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68307	100-Lead FG	16	—	0 to 70	0	66	264	SPAK307FG16
	100-Lead PU	16	—	–40 to +85	0	84	420	SPAK307CFG16
XC68307V	100-Lead FG	8, 16*	—	0 to 70	0	66	264	SPAK307FG16V
	100-Lead PU	8, 16	—	0 to 70	0	84	420	SPAK307PU16

NOTE: FG = Plastic Quad Flat Pack (PQFP)
PU = Thin Quad Flat Pack
*Available in 3.3V V_{CC}

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

Industrial Temperatures (0-40 to +85°C)

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MOQ	POQ	
XC68307CFG	100-Lead FG	16	—	—	0	66	264	SPAK307CFGXXB

NOTE: PV = Thin Quad Flat Pack (TQFP)

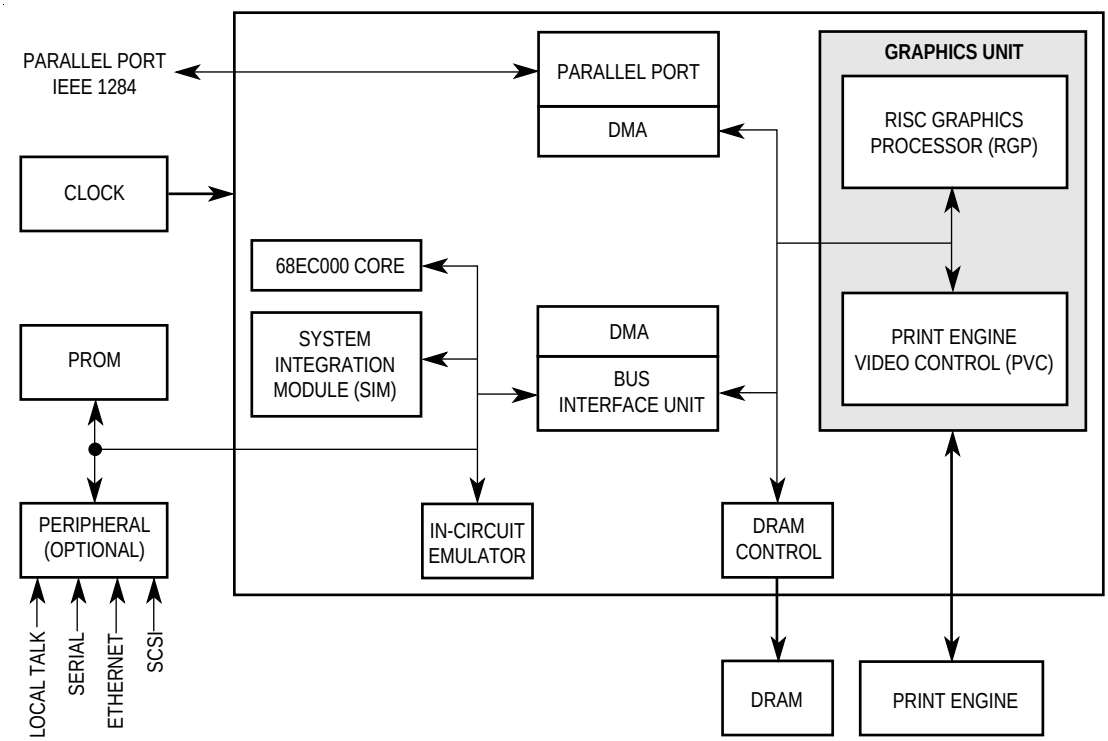
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
F37C	1	75%	MOS8	0.8µ	XC Production	Yes	—	Up sizing the 06 layer
F37C	0	75%	MOS8	0.8µ	Canceled	Yes	—	First Silicon
G57B	0	75%	MOS8	0.8µ	In Qualification	Yes	—	TD0 fix, IS6, SPOR8

First Silicon: 4Q93
Production Date: 2Q94
Die Size: 281 × 247
Device:
Process: HCMOS

XC68322



Features:

- Static EC000 Core Processor
- RISC Graphic Coprocessor
- Print Engine Video Controller
- General-Purpose DMA Unit
- System Integration Module
- Parallel Communication Port (IEEE 1284)
- Low-Power Device
- Dual Bus Architecture
- Distributed Processing
- 16 and 20 MHz

Target Markets/Applications:

The 68322 is optimized for the low-end (up to 8 ppm @ 600 dpi) laser printer market. The highly integrated, low power, single-chip printer solution can also be targeted for inkjet printers, multi-function peripherals (Fax/Modem/Printers), Bar Code printers and other portable printing applications. The 68322 will find ready applications to other embedded control applications that require very fast bit manipulations.

Competitive Advantages:

Intel 960SA: Slightly lower cost, RISC processor

Weaknesses: When applied to printer market, 960SA requires ASIC.

AMD 29205: Slightly lower cost, RISC processor

Weaknesses: When applied to printer market, 29205 requires ASIC.

Literature:

Title	Order Number
MC68322 Product Brief	MC68322/D
MC68322 User's Manual	MC68322UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
M68300 Brochure (Rev 2)	BR1114/D

Support Tools:

Software support provided through various third-party vendors of 68000 software tools.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Support Chips:

None needed

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68322	160-Lead FT	16, 20	—	—	0	24	240	SPAK322FTXX

NOTE: FT = Plastic Quad Flat Pack (PQFP)

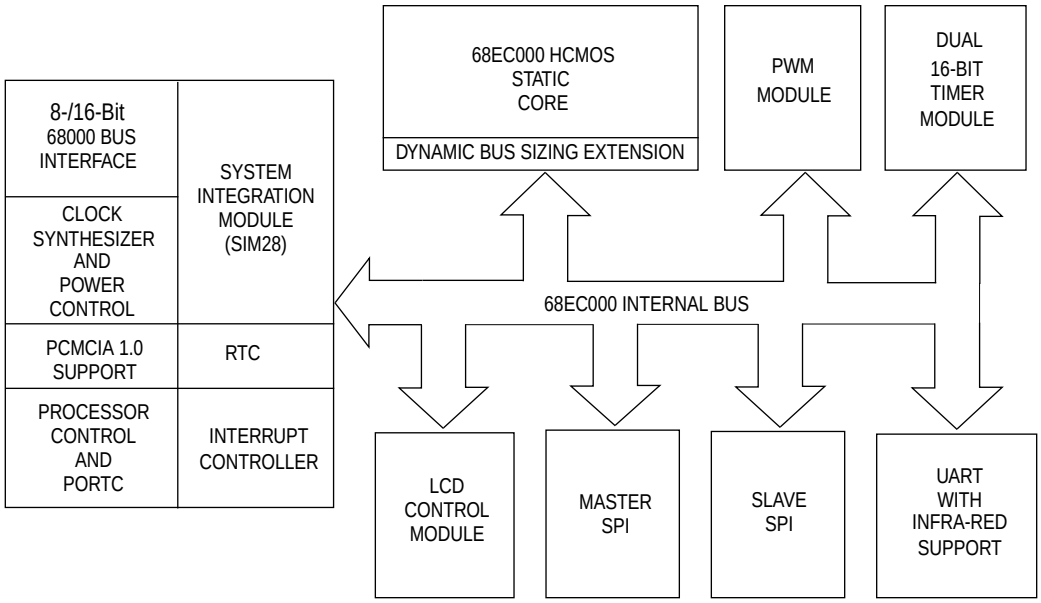
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
F65E	2	75%	MOS8	0.8µ	XC	—	—	Fixed bus contention problem
F65E	1	75%	—	—	—	—	—	Fixed assorted design anomalies
F65E	0	75%	MOS8	0.8µ	Canceled	—	—	Original silicon

First Silicon: 1Q94
Production Date: 3Q95
Die Size: 331 × 389
Device: 120,000 (74,000 Active)
Process: CMOS

PC68328V



Features:

- Static 68EC000 Core Processor—Identical to MC68EC000 Microprocessor
  - —Full Compatibility With MC68000 And MC68EC000
  - —32-Bit both External and Internal Address Bus capable of Addressing 4GB Space
  - —16-Bit On-Chip Data Bus For MC68000 Bus Operations
  - —Static Design Allows Processor Clock To Be Stopped Providing Dramatic Power Savings
  - —2.7 MIPS Performance At 16.67-MHz Processor Clock
- External M68000 Bus Interface with Dynamic Bus Sizing for 8-bit and 16-bit Data Ports
- System Integration Module (SIM28), Incorporating Many Functions Typically Relegated to External Array Logic, such as:
  - —System Configuration, Programmable Address Mapping
  - —Glueless Interface to SRAM, EPROM, FLASH Memory
  - —Sixteen Programmable Peripheral Chip Selects With Wait State Generation Logic
  - —Interrupt Controller with 13 flexible inputs
  - —Programmable Interrupt Vector Response For On-Chip Peripheral Modules
  - —Hardware Watchdog Timer
  - —Software Watchdog Timer
  - —Low-Power Mode Control
  - —Up to 78-Bit Individually Programmable Parallel I/O Ports
  - —PCMCIA 1.0 Support

- UART
  - —Support IrDA Physical Layer Protocol
  - —8 Bytes FIFO on Rx and Tx
- Two Separated Serial Peripheral Interface Ports (Master and Slave)
  - —Support For External POCSAG Decoder (Slave)
  - —Support for Digitizer from A/D Input or EEPROM (Master)
- Dual Channel 16-Bit General Purpose Counter/timer
  - —Multimode Operation, Independent Capture/Compare Registers
  - —Automatic Interrupt Generation
  - —240-ns Resolution At 16.67-MHz System Clock
  - —Each Timer Has An Input And An Output Pin for Capture and Compare
- Pulse Width Modulation Output For Sound Generation
  - —Programmable Frame rate
  - —16 Bit programmable
  - —Supports Motor Control
- Real Time Clock
  - —24 Hour Time
  - —One Programmable Alarm
- Power Management
  - —5 V or 3.3 V Operation
  - —Fully Static HCMOS Technology
  - —Programmable Clock Synthesizer for Full Frequency Control
  - —Low Power Stop Capabilities
  - —Modules Can Be Individually Shut-down
  - —Lowest Power Mode Control (Shut Down CPU and Peripherals)
- LCD Control Module
  - —Software Programmable Screen Size To Support Single (Non-Split) Monochrome/ STN Panels
  - —Capable Of Direct Driving Popular LCD Drivers/Modules From Motorola, Sharp, Hitachi, Toshiba etc.
  - —Support Up To 4 Grey Levels
  - —Utilize System Memory as Display Memory
- IEEE 1149.1 Boundary Scan Test Access Port (JTAG)
- Operation From DC To 16.67 MHz (Processor Clock)
- Operating Voltages of 3.3V $\pm$ 0.3V and 5V $\pm$ 0.5V
- Compact 144-Lead Thin Quad Flat Pack (TQFP) Package

Target Markets/Applications:

DragonBall definitely has its sights set on the Portable Digital Assistance (PDA) market but that's not all. The applications served by this device are countless, ranging from security control panels, GPS systems and instrumentation to interactive games, meter reading, and portable medical equipment. DragonBall is the first in a series of products addressing the battery-powered consumer electronic products.

Literature:

Title	Order Number
M68328 User's Manual	MC68328UM/AD
M68328 Product Brief	M68328/D
M68000 Family Programmer's Reference Manual	M68000PM/AD
M68328 Errata	AESOP Bulletin Board 1-800-843-3451

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
PC68328	144-Lead PV*	16	B	0 to 70	2	2	2	PC68328PV16V

NOTE: PV = Thin Quad Flat Pack (TQFP)

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

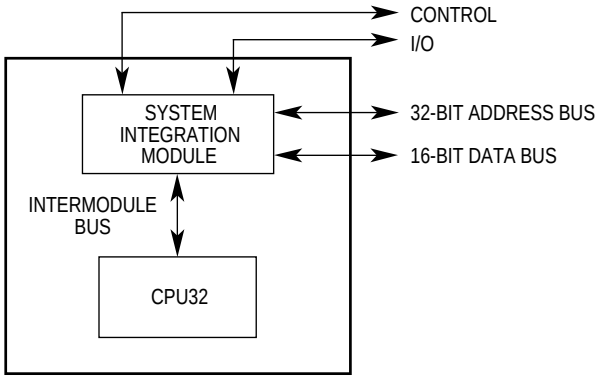
Extended temperature available 1Q96.
*Available in 3.3V V_{CC}

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
0G58B	—	—	MOS 8	0.65µ	Canceled	Yes	No	Errata available on AESOP
1G58B	—	—	MOS 8	0.65µ	Sampling	Yes	—	Errata available on AESOP

First Silicon: July 1995
XC Qualification Date: 4Q95
Die Size: 256 × 260
Devices:
Process: .65µ TLM HCMOS

MC68330/MC68330V



Features:

- CPU32 Processor
- System Integration Module (SIM40)
- 3.3 V Operation Available (68330V)
- 8.3 MIPS Performance at 25 MHz

Target Markets/Applications:

Applications requiring 68020 performance from a 16-bit memory system; minimal glue logic (SIM40 contains most of it); static design/low power modes—e.g., low-power consumption; 5.0 V and 3.3 V parts; and 68000 upgrade solution for applications requiring performance of CPU32 with no on-chip peripherals.

The ability to operate at 3.3 V makes the 68330V an ideal solution for portable applications.

The 68330 is now available in a 144-pin TQFP (PV) package replacing the FC package. Orders for the FC will be accepted until November 14, 1995 and shipped through May 1996.

Literature:

Title	Order Number
MC68330 Technical Summary	MC68330/D
MC68330 User's Manual	MC68330UM/AD
M68000 Programmer's Reference Manual	M68000PM/AD
M68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Various hardware and software support available from third parties.

Support Chips:

M68340EVS—Low-Cost Evaluation System

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68330	144-Lead FC*	16, 25	A	CFC16	0	36	144	SPAK330FCXX
MC68330PV	144-Lead PV	16, 25	A	—	0	60	240	SPAK330PVXXA
MC68330V	144-Lead PV	16	A	CPV16	0	60	240	SPAK330PVXXA

NOTE: FC = Plastic Quad Flat Pack (PQFP)
PV = Thin Quad Flat Pack (TQFP)
V = Suffix for 3.3V
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

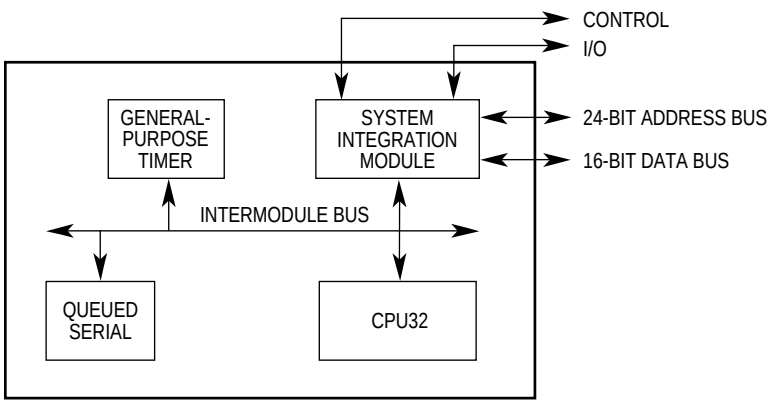
*Not recommended for new designs.

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
E84J	C	75%	MOS8	0.8µ	Production	Yes	—	Reduced errata
1D81H	B	75%	MOS8	0.8µ	Canceled	Yes	—	
D81H	A	75%	MOS8	0.8µ	Canceled	Yes	—	
D37E	0	67%	MOS8	1.0µ	Canceled	Yes	—	

First Silicon: 2Q91
MC Qualification Date:
Die Size: 268 × 230
Devices: Sites = 235,000; Active = 130,000
Process: HCMOS

MC68331



Features:

- CPU32 Processor
- System Integration Module (SIM)
- General-Purpose Timer (GPT)
- SCI and Queued SPI (QSM)

Target Markets/Applications:

General-Purpose Embedded Control—e.g.:

- Communications—Mobile Phones
- Office Equipment—Mobile Equipment
- Industrial Control—Peripheral Control

Literature:

Title	Order Number
MC68331 User's Manual	MC68331UM/AD
MC68331 Technical Summary	MC68331TS/D
32-Bit Central Processing Unit (CPU32) Ref. Manual	CPU32RM/AD
Queued Serial Module (QSM) Reference Manual	QSMRM/AD
General-Purpose Timer (GPT) Reference Manual	GPTRM/AD
System Integration Module (SIM) Reference Manual	SIMRM/AD

Support Tools:

M68331EVS—Low-Cost Evaluation System (contact AMCU marketing for more details)

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

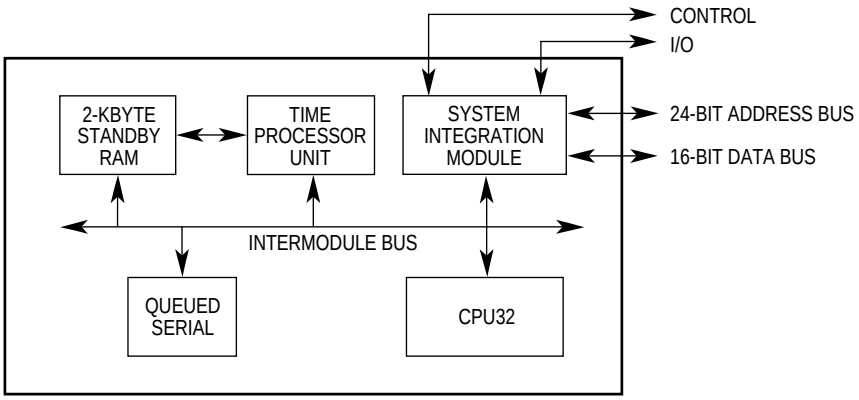
Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68331	132-Lead	16	—	—	*	*	*	
	144-Lead	16	—	—	*	*	*	

NOTE: MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

*** Contact AMCU Marketing (512) 891-2758 for more details.**

MC68332



Features:

- CPU32 Core
- System Integration Module (SIM)
- Programmable Time Processor Unit (TPU)
- SCI and Queued SPI (QSM)
- 2-Kbyte Standby Ram with TPU Emulation (TPU RAM)

Target Markets/Applications:

Any advanced real-time control application—e.g.:

- Powertrain—Engine management and gearbox
- Office Equipment—I/O and motor control in plotter, printer, copier, fax, etc.
- Industrial Control—DC and AC motor control

The ability to operate at 3.3 V makes the 68330V an ideal solution for portable applications.

Competitive Advantages:

The MC68332 has the most advanced timer unit on the market today.

Literature:

Title	Order Number
MC68332 User's Manual	MC68332UM/AD
MC68332 Technical Summary	BR756/D
32-Bit Central Processing Unit (CPU32) Ref. Manual	CPU32RM/AD
Time Processor Unit (TPU) Reference Manual	TPURM/AD
Queued Serial Module (QSM) Reference Manual	QSMRM/AD
System Integration Module (SIM) Reference Manual	SIMRM/AD

Support Tools:

M68332EVS—Low-Cost Evaluation System

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Package/Speed Options:

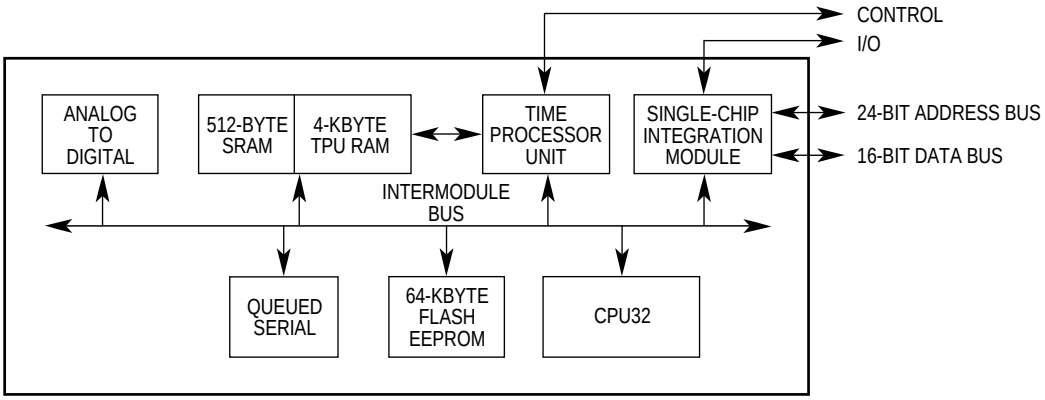
Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68332	132-Lead FC/FD	16	—	—	*	*	*	
	144-Lead FM, FV	16	—	—	*	*	*	

NOTE: FC = Plastic Quad Flat Pack (PQFP) in extended temperature (–40 to +85C)
FD = Plastic Quad Flat Pack (PQFP) with molded carrier ring in extended temperature (–40 to +85C)
FM = Molded Carrier Ring
FV = 20 mm × 20 mm Quad Flat Pack

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

*** Contact AMCU Marketing (512) 891-2758**

XC68F333



Features:

- CPU32 Processor
- Single-Chip Integration Module (SCIM)
- 8/10-Bit Analog-to-Digital Converter (ADC)
- Programmable Time Processor Unit (TPU)
- SCI and Queued SPI (QSM)
- 512 Bytes of Standby RAM (SRAM)
- 3.5-Kbyte Standby Ram with TPU Emulation (TPU RAM)
- 64-Kbyte Flash EEPROM

Target Markets/Applications:

- Engine Management (Powertrain)
- Motor Control

Competitive Advantages:

First microcontroller to integrate flash EEPROM on-chip.

Literature:

Title	Order Number
MC68F333 Product Preview	MC68F333/D
MC68F333 Technical Summary	MC68F333TS/D
32-Bit Central Processing Unit (CPU32) Ref. Manual	CPU32RM/AD
Timer Processor Unit (TPU) Manual	TPURM/AD
Queued Serial Module (QSM) Reference Manual	QSMRM/AD
Analog-to-Digital Converter (ADC) Reference Manual	ADCRM/AD

Support Tools:

Low-cost evaluation board will be available (contact AMCU marketing for more details).

Hardware and software development tools are available from third parties.

Package/Speed Options:

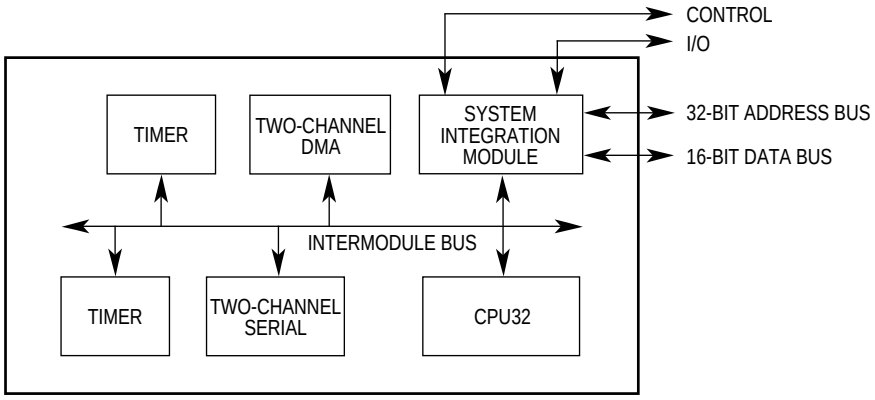
Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68F333	160-Lead FC	40, 50, 66	—	—	*	*	*	

NOTE: FC = Plastic Quad Flat Pack (PQFP)

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

* **Contact AMCU Marketing (512) 891-2758 for more details.**

MC68340/MC68340V



Features:

- CPU32 Processor
- System Integration Module (SIM40)
- Two-Channel DMA Controller
- Two-Channel Serial UART
- Two-Timer Modules
- 3.3 V Operation Available (68340V)
- 8.3 MIPS Performance at 25 MHz

Target Markets/Applications:

High-Speed Data Movement—terminals, disk controllers, printers, copiers, CD-I, audio-video processing and global positioning systems (navigation aids).

Mobile/Portable Applications—pen-based computers, portable computers, portable phones, and medical instruments.

The ability to operate at 3.3 V makes the 68340V ideal for portable applications.

The 68340RP is being replaced by the 144-pin TQFP (PV) package. Orders for the RP will be accepted until November 10, 1995 and shipped through May 1996.

Literature:

Title	Order Number
MC68340 User's Manual	MC68340UM/AD Rev. 1
MC68340 Product Brief	MC68340/D
MC68340 User Manual Addedum	MC68340UMAD/AD
M68300 Family Brochure	BR1114/D

Support Tools:

M68340EVS—Low-Cost Evaluation System.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Various hardware and software support available from third parties.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68340	144-Lead FE	16**, 25	C	CFE16, CFE25	0	24	96	SPAK340FEXXE
	144-Lead PV	16**, 25	C	CPV16, CPV25	0	60	60	SPAK340PVXXE
	145-Lead RP*	16**, 25	C	CRP16	1	1	11	
	144-Lead FT	16, 25	—	—	0	24	96	SPAK340FTXXE

NOTE: FE = Ceramic Quad Flat Pack (CQFP)
FT = Plastic Quad Flat Pack (PQFP)
PV = Thin Quad Flat Pack (TQFP)
RP = Plastic Pin Grid Array

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

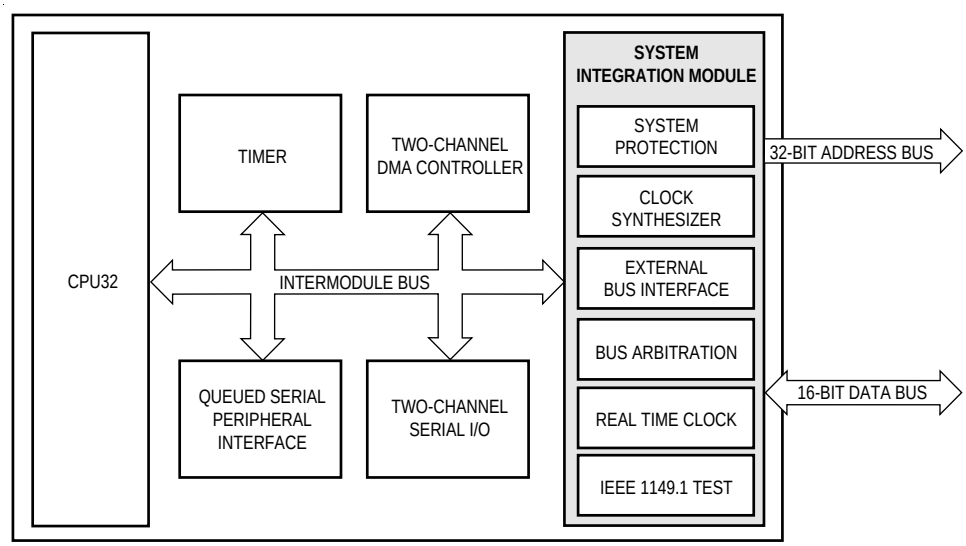
*Not recommended for new designs.
**Available in 3.3 V.

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
0G67F	P	80%	MOS11	.65µ	Production	Yes	Yes	MC orders
1F77J	N	75%	MOS8	.8µ	Production	Yes	Yes	
2E16G	K	75%	MOS8	.8µ	Production	Yes	Yes	
2D75M	G	70%	MOS8	1.0µ	Canceled	Yes	—	
D97R	H	70%	MOS8	.8µ	Canceled	Yes	—	Was shipped only as XC
1D75M	F	70%	MOS8	1.0µ	Canceled	Yes	—	
D75M	E	70%	MOS8	1.0µ	Canceled	Yes	—	Few shipped. Max 40
1D76F	D	70%	MOS8	1.0µ	Canceled	Yes	—	
D45C	B	70%	MOS8	1.0µ	Canceled	Yes	—	
1C67H	A	70%	MOS8	1.0µ	Canceled	Yes	—	Released Sept 1990

First Silicon: June 90
MC Qualification Date: 1Q92
Die Size: 331 × 316
Devices: Sites = 350,000; Active = 245,000
Process: HCMOS

XC68341/XC68341V



Features:

- High-Performance CPU32 Core Processor
- High-Speed Dual DMA Controllers for Low-Latency Transfers
- Counter/Timer
- Dual-Serial Communication Ports
- Queued Serial Peripheral Interface (QSPI)
- System Integration Module for Flexible and Cost-Effective System Interface
- Power Management
- 16- or 25-MHz Operation
- 160-Pin Plastic Quad Flat Pack (QFP)

Target Markets/Applications:

High-Speed Data Movement—terminals, disk controllers, printers, copiers, consumer video games, CD-I, audio-video processing, and global positioning systems (navigation aids).

Mobile/Portable Applications—pen-based and hand-held computers, portable computers, portable phones, and medical instruments.

The ability to operate at 3.3 V means that the 68341V is ideally suited for portable applications.

Central Processor for CD-I Players—full Motion video CD-I systems make the best use of the MC68341 high performance.

Literature:

Title	Order Number
M68300 Integrated Processor Family (Rev 2)	BR1114/D
MC68341 User's Manual	MC68341UM/AD
MC68341 Product Brief	MC68341/D

Support Tools:

Various hardware and software support available from third parties.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68341	160-Lead FT	16, 25	—	CFT16	0	24	96	SPAK341FTXX
XC68341V	160-Lead FT	16	—	—	0	24	96	SPAK341FTXXV

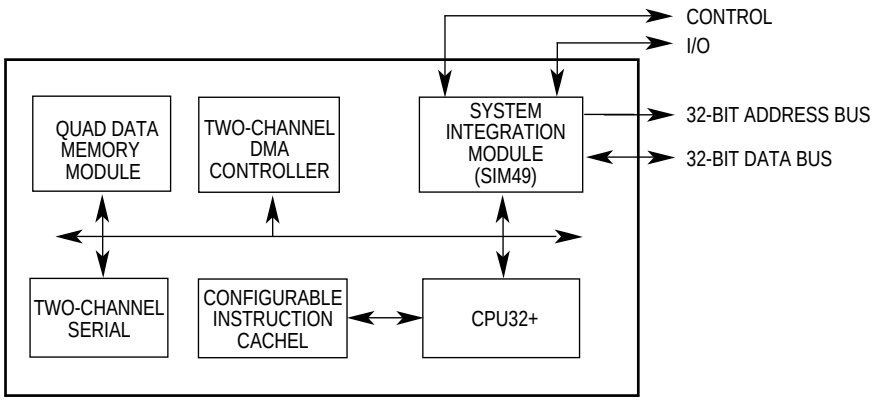
NOTE: FT = Plastic Quad Flat Pack (PQFP)
V = Suffix for 3.3 V V_{CC}
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
E41R	A	75%	MOS8	0.8µ	Production	Yes	—	XC orders
E10K	0	75%	MOS8	0.8µ	Canceled	Yes	—	

First Silicon: Jan 93
XC Qualification Date: 3Q93
Die Size: 352.6 × 328.5
Devices: Sites = 350,000; Active = 245,000
Process: HCMOS TLM

MC68349/MC68349V "DRAGON I™"



Features:

- 3.3-V (68349V) or 5-V (68349) Operation
- CPU32+ Processor
- Configurable Instruction Cache
- Quad Data Memory Module
- Two-Channel DMA Controller
- Two-Channel Serial UART
- System Integration Module (SIM49)

Target Markets/Applications:

The ability to operate at 3.3 V means that the 68349V is ideally suited for portable applications.

- Personal Intelligent Communicators (PICs)
- Personal Digital Assistants (PDAs)
- I/O Processors for High-Performance Systems
- Real-Time Control Engines

Literature:

Title	Order Number
M68349 User's Manual	MC68349UM/AD
MC68349 Product Brief	MC68349/D
M68300 Family Brochure (Rev 2)	BR1114/D

Support Tools:

Various hardware and software support available from third parties.

Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68349	160-Lead FT	16, 25	A	CFT16	0	24	240	SPAK349FTXXA
MC68349V	160-Lead FT	16	A	—	0	24	240	SPAK349FTXXVA

NOTE: FT = Plastic Quad Flat Pack (PQFP)
V = Suffix for 3.3 V V_{CC}

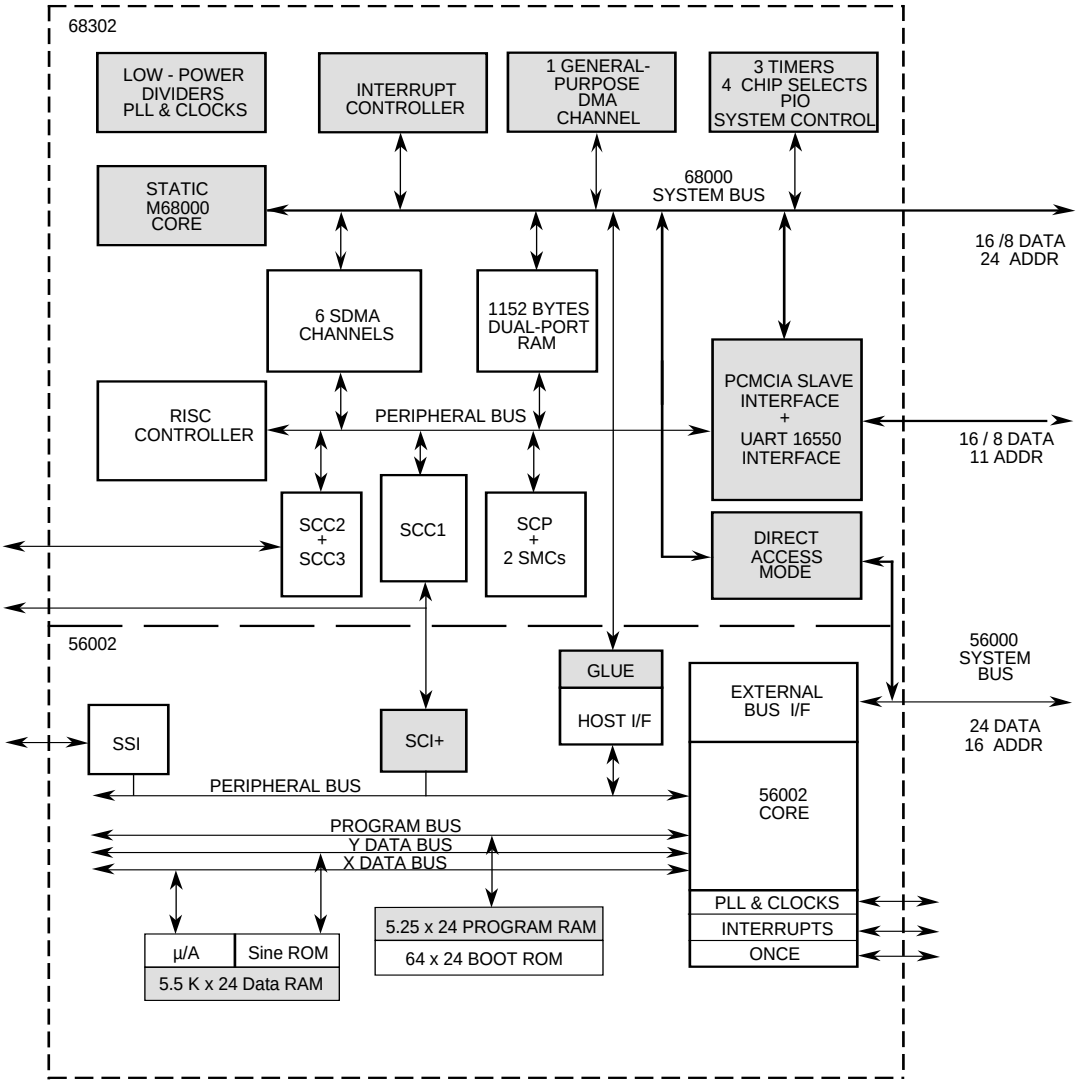
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1F13C	E	75%	MOS8	0.8µ	Production	Yes	—	MC orders
2E11T	C	75%	MOS8	0.8µ	Canceled	Yes	—	
1E11T	B	75%	MOS8	0.8µ	Canceled	Yes	—	
E11T	A	75%	MOS8	0.8µ	Canceled	Yes	—	
E44J	0	75%	MOS8	0.8µ	Canceled	Yes	—	

First Silicon: Jan 93
MC Qualification Date: 4Q94
Die Size: 463 × 333.5
Devices: 585,000
Process: HCMOS TLM

XC68356



Features:

- Static 68000 Processor
- System Integration Block
- Communications Processor
- 3 SCC’s
- PCMCIA Slave Interface
- UART 16550 Emulation
- 56002 DSP Core

- DSP FSRAM & ROM
- Low Power Control Module

Target Markets/Applications:

- Modems
- PCMCIA I/O Cards
- ISDN
- Base Stations
- Wireless Communication

Literature:

Title	Order Number
M68356 User's Manual	*MC68356UM/AD*
M68356 Product Brief	*MC68356/D*
DP356 Product Brief	*MC68DP356/D*
M68356ADS Description	*M68356ADS/D*

Support Chips:

M68356ADS — Application Development System
M68356ADI — Host T/F Card

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68356	357-Pin PBGA ZP	25	—	0 to 70°C	0	44	220	SPAK356XX
XC68DP356	357-Pin PBGA ZP	25	B	0 to 70°C	0	44	220	SPAKDP356XXB

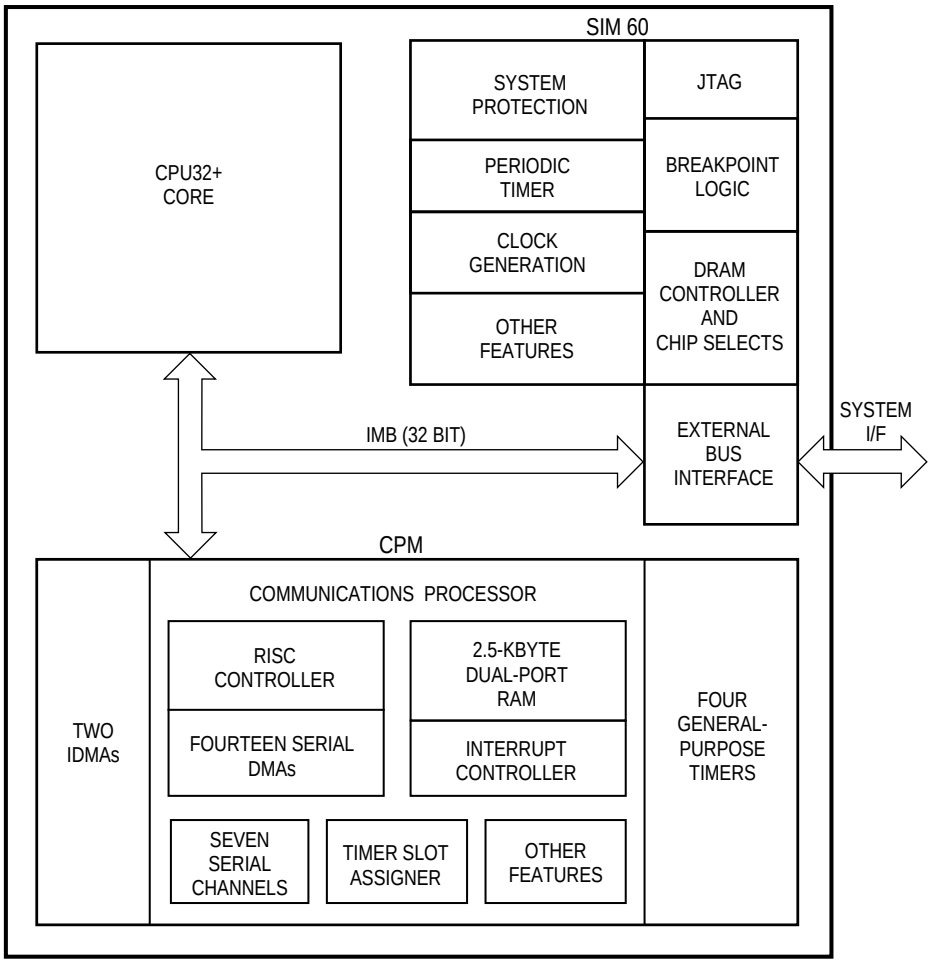
NOTE: ZP = Ball Grid Array (PGA)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History:

Device	Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
68356ZP25	1 E62C	A		MOS11	0.65µ	Production	Yes		
68DPS356ZP25	2E60C	B		MOS11	0.65µ	Production	Yes		

First Silicon: 2Q94
MC Qualification Date: 4Q94
Die Size: 518 × 494
Device: 2.1 Million Transistors
Process: CMOS

MC68360 "QUICC"



Features:

- CPU32+ Processor
- Slave Mode To Disable CPU32+ — Glueless Interface to 68040/EC040
- Memory Controller (Eight Banks)
- System Integration Module (SIM60)
- Communications Processor Module (CPM)
- Four SCCs
- Time-Slot Assigner

Target Markets/Applications:

- Bridges
- Routers
- T1 Line Card Controllers
- PABX's
- Cellular Base Stations
- Industrial Control Networking
- 040 Peripheral Chip

Industry's first 32-bit controller to integrate a CPU with WAN and Ethernet LAN capability on a single chip.

Literature:

Title	Order Number
MC68360 Product Brief	MC68360/D
M68360 User's Manual	MC68360UM/AD
MC68000 Family Programmer's Reference Manual	MC68000PM/AD
M68300 Family Brochure	BR1114/D
MC68360 RAM Microcode Package Overview	M68360MC/D
MC68MH360 Reference Manual	MC68MH360RM/AD

Support Tools:

M68360QUADS—QUICC Application Development Board
M68360ADI-PC—IBM PC Interface Card
M68360ADI-SUN4—Sun 4 Interface Card
M68360QUADS-040—360/EC040 Application Development Board
Third party support listed in *The 68K Source*, 1994 Edition, BR729/D.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68360	357 OMPAC ZP	25	C.1	—	0	44	220	SPAK360ZP25C SPAKEN360ZP25C
MC68EN360	241-Lead RC	25, 33	C.1	—	1	1	10	
	240-Lead FE	25, 33	C.1	—	0	24	120	SPAK360FEXXC SPAKEN360FEXXC
XC68MH360	241-Lead RC	25*, 33	C.1	—	1	1	10	
	240-Lead FE	25*, 33	C.1	—	0	24	120	SPAKMH360FEXXC

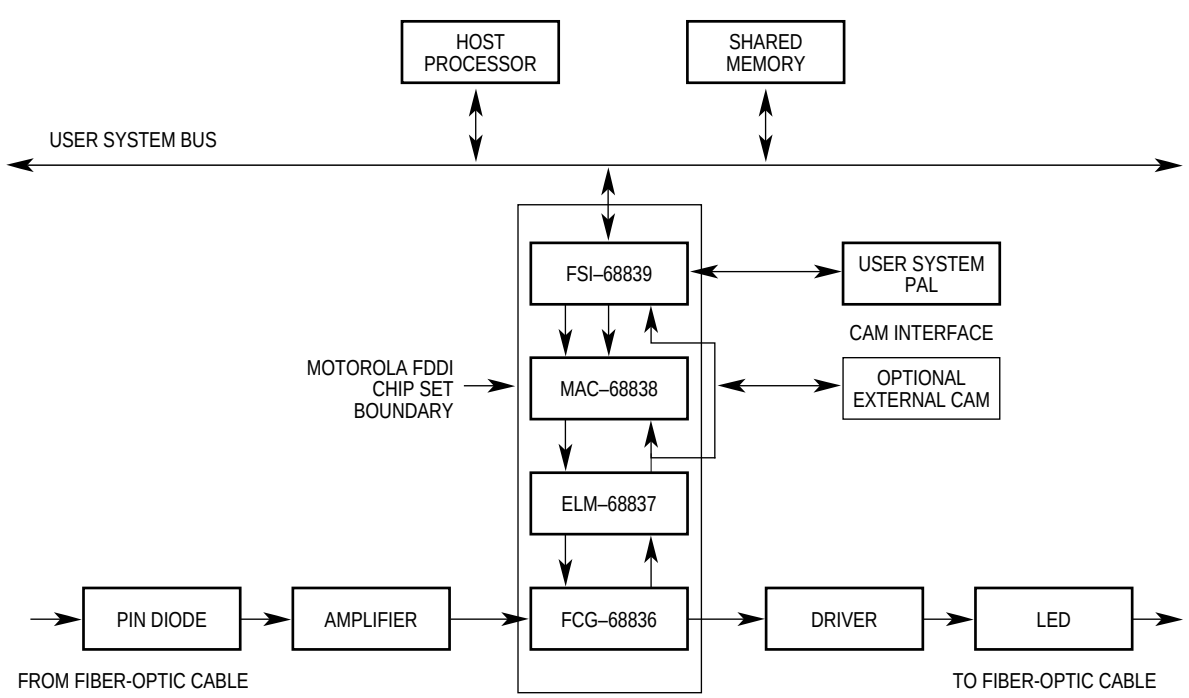
NOTE: FE = Ceramic Quad Flat Pack (CQFP) MPQ = Minimum Package Quantity
RC = Pin Grid Array (PGA), Gold Lead Finish POQ = Preferred Order Quantity
ZP = Ball Grid Array (PGA) SOQ = Sample Order Quantity
*Available in 3.3V (25 MHz only)

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
0G24F	C.1	80%	TSC	.65µ	Prototype	—	—	New wafer fab
1E68C	C.1	80%	MOS11	.65µ	Production	—	—	MC orders
0E63C	C.1	80%	MOS11	.65µ	Canceled	—	—	Discontinued
4F35G	B.4	75%	MOS11	.8µ	Canceled	Yes	—	Discontinued
1F35G	B.2	75%	MOS11	.8µ	Canceled	Yes	—	Discontinued
2C63T	A.2	75%	MOS8	.8µ	Canceled	Yes	—	Discontinued
0E68C	C.1	80%	MOS11	.65µ	Production	Yes	—	QUICC32

First Silicon: Mar 93
MC Qualification Date: 1Q95
Die Size: 450 × 450 (0.8µ); 365 × 364 (.65µ)
Devices: 4K Gates 750K Transistors
Process: HCMOS TLM

FIRST-GENERATION FDDI CHIP SET



Features:

- MC68836 FDDI Clock Generator (FCG)
- MC68837 Elasticity Buffer and Link Manager (ELM)
- MC68838 Media Access Controller (MAC)
- MC68839 FDDI System Interface (FSI)

Target Markets/Applications:

The fiber distributed data interface (FDDI) chip set fully implements the 100 Mbits/sec networking standard set up by the American National Standards Institute (ANSI). The chip set offers a high-performance, flexible, low-cost solution for applications such as FDDI adapter cards, bridges, and concentrators where large data-transfer rates are required.

Competitive Advantages:

AMD: Inferior performance, awkward to use, and shedding resources due to 386/486 opportunities.

National Semiconductor: Inferior performance and requires many external components.

Literature:

Title	Order Number
FDDI Chip Set Technical Summary	M68800/D
FDDI Chip Set Brochure	BR1104/D
FCG User's Manual	MC68836UM/AD
ELM User's Manual	MC68837UM/AD
MAC User's Manual	MC68838UM/AD
FSI User's Manual	MC68839UM/AD

Support Tools:

M68FDDISMT—Station Management Software (SMT) available in DOS and TAR format

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68836	52-Lead FN	—	B	—	1	1	23	
MC68837	120-Lead FC	—	E	—	0	24	120	SPAK837FCE
MC68838	120-Lead FC	—	C	—	0	24	96	SPAK838FCC
MC68839	184- Lead FE	—	—	—	0	24	96	SPAK839FE

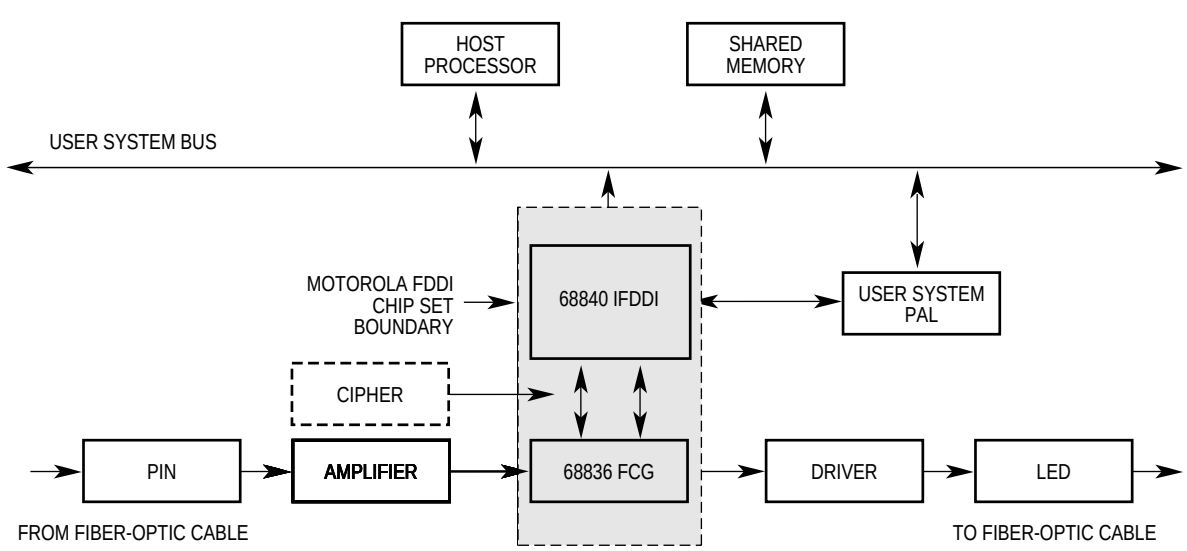
NOTE: FC = Plastic Quad Flat Pack (PQFP) MPQ = Minimum Package Quantity
FE = Ceramic Quad Flat Pack (CQFP) POQ = Preferred Order Quantity
FN = Plastic Leaded Chip Carrier (PLCC) SOQ = Sample Order Quantity

History

Device	Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
68836	3C69R	—	0%	Bi-Plr#3	1.5µ	Production	Yes	—	Going to 1F14B mask
68837	N/A	B	—	MOS6	1.0µ	Production	Yes	—	PGA only
	1E37K	D	—	MOS8	0.8µ	Production	Yes	Yes	QFP only
68838	N/A	C	—	MOS6	1.0µ	Production	No	—	
68839	OC66T	C	—	MOS8	0.8µ	Production	Yes	—	
	OC66T	—	—	MOS8	0.8µ	Canceled	Yes	Yes	

Device	MC Qualification Date	First Silicon	Die Size	Devices	Process
XC68836	1Q95 (XC)	Feb 1990	154 × 198	Sites = 10,000	Bipolar
MC68837	Aug 1994	Oct 1993	214 × 192	64K Transistors	HCMOS
MC68838	June 1990	June 1990	31K Gate Array	124K Transistors	HCMOS
MC68839	Sept 1993	Mar 1991	491 × 450	Sites = 750,000; Active = 650,000	HCMOS

NEXT-GENERATION FDDI CHIP SET



Features:

- XC68834 Stream Cipher Chip
- XC68836 FDDI Clock Generator (FCG)
- XC68840 Integrated Fiber Distributed Data Interface (IFDDI)

Target Markets/Applications:

Motorola's next generation FDDI chip set fully implements the 100 Mbits/sec networking standard set up by the American National Standards Institute (ANSI). The chip set offers a highly integrated, high-performance, flexible, low-cost solution for applications such as adapter cards, motherboards, bridges, and concentrators where large data transfer rates are required. Twisted pair wire can also be supported with the addition of the 68834 stream cipher chip or the 68840 Rev B which integrates 68834 functionality.

Competitive Advantages:

AMD: Inferior performance, awkward to use, and shedding resources due to 386/486 opportunities. No integration of first-generation components.

National Semiconductor: Inferior performance, requires many external components, and less flexible. No future FDDI roadmap.

Literature:

Title	Order Number
FCG User's Manual	MC68836UM/AD
IFDDI User's Manual	MC68840UM/AD Rev 1
Cipher Chip User's Manual	(Call factory)

Support Tools:

M68FDDISMT—Station Management Software (SMT) available in DOS and TAR format

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XC68834	44-Lead PB	—	—	—	0	96	480	SPAK834PB
XC68836	52-Lead FN	—	B	—	1	1	23	
XC68840B	184-Lead FE	25, 33	B	—	1	1	12	SPAK840FEXXB

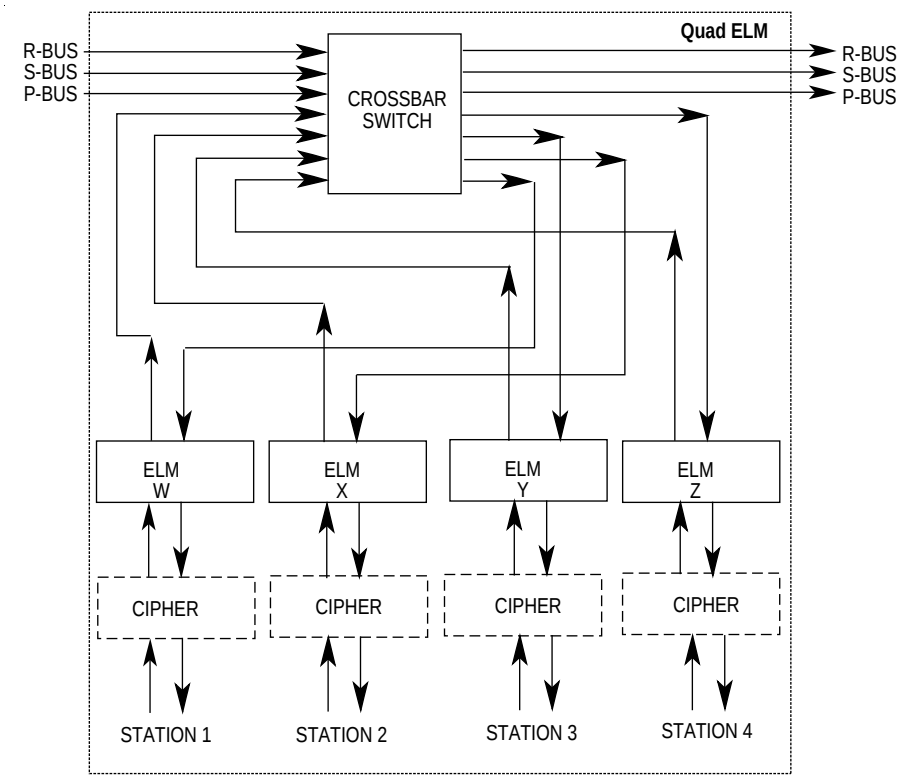
NOTE: FE = Ceramic Quad Flat Pack (CQFP) MPQ = Minimum Package Quantity
FN = Plastic Leaded Chip Carrier (PLCC) POQ = Preferred Order Quantity
PB = 10mm × 10mm Plastic Quad Flat Pack SOQ = Sample Order Quantity

History

Device	Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
68834	OE26P	—	75%	MOS8	0.8µ	Production	No	—	
68836	3C69R	—	0%	Bi-Plr#3	1.5µ	Production	Yes	—	1F14B Mask Introduction PCN issued
68840	OC67T	A	75%	MOS8	0.8µ	Production	Yes	—	
68840	1E59C	B	78%	MOS8	0.71µ	Production	Yes	—	
68840	2E59C	B	78%	MOS8	0.71µ	Production	Yes	—	

Device	Production Date	First Silicon	Die Size	Devices	Process
XC68834	June 1993	April 1993	104 × 105	4K Gates	HCMOS
XC68836	2Q91	Feb 1990	154 × 198	Sites = 10,000	Bipolar
XC68840	June 1993	Feb 1993	560 × 480	800K Sites	HCMOS

FDDI QUAD ELM



Features:

- MC68847 FDDI Quad ELM
- Able to perform any ANSI SMT standard configuration scheme
- JTAG compliant implementation
- Provides full functionality of individual ELM devices, including:
  - — Implements ANSI FDDI PHY standard
  - — Performs 4B/5B encoding and decoding, elasticity buffer, and smoother functions
  - — Provides data framing and alignment to byte boundaries
  - — Hardware assists PCM state machine to reduce load on SMT processing
  - — Contains line state detector and repeat filter
  - — Provides link error monitor detection and counting on chip
  - — Performs scrubbing
  - — Provides for nonconcatenation of frames

Target Markets/Applications:

The MC68847 Quad ELM implements four MC68837 ELM devices on a single chip, providing a low-cost solution for concentrator applications. The four ELMs are accessible by three unique data buses.

Competitive Advantages:

National Semiconductor: No integrated FDDI concentrator chip.

Literature:

Title	Order Number
Quad ELM User's Manual	MC68847UM/AD

Support Tools:

M68FDDISMT—Station Management Software (SMT) available in DOS and TAR format

Third party support listed in *The 68K Source,* 1994 Edition, BR729/D.

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
MC68847	208-Lead FC	—	—	—	0	24	96	SPAK847FC

NOTE: FC = Plastic Quad Flat Pack (PQFP)

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

History

Mask	Rev	Shrink	Fab	Geo	Status	Errata	PCN	Comments
1E38K	—	75%	MOS8	0.8µ	Production	Yes	—	
3E38K	B	75%	MOS8	0.8µ	Production	No	—	

First Silicon: Nov 1993
MC Qualification Date: Sept 1994
Die Size: 314 × 337
Devices: 304K Gates
Process: HCMOS

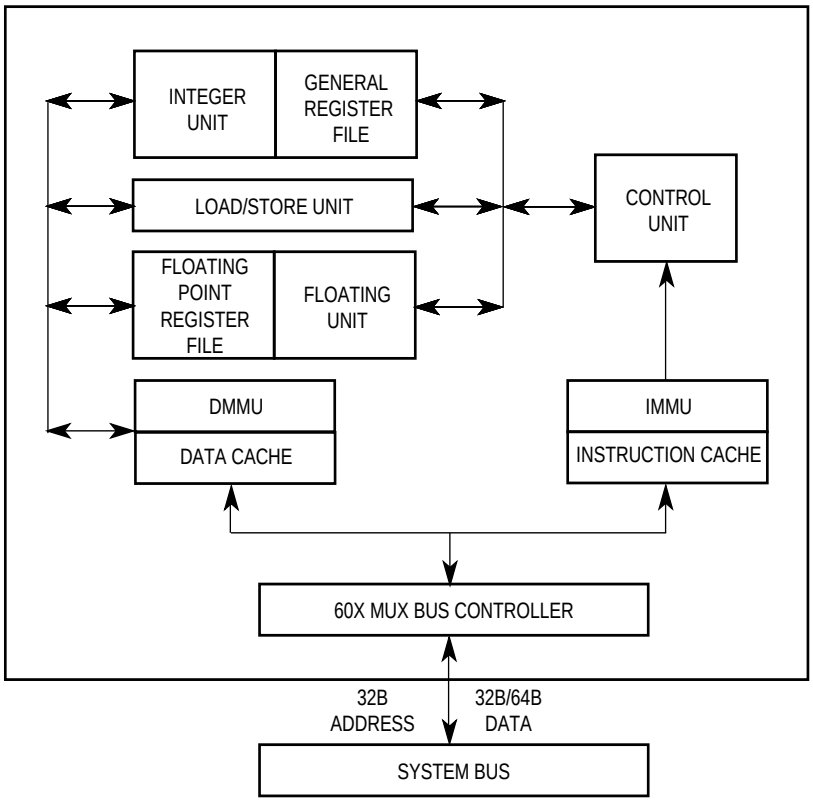
EMBEDDED POWERPC MICROPROCESSORS

The MPC600 Family is a full computer architecture for applications that require uncompromising performance or compatibility with desktop environments. Different versions are available including the cost-effective PowerPC 602™, PowerPC 603/603e, and the PowerPC 604 microprocessor.

The MPC800 Family comprises highly integrated designs that combine PowerPC core processors with popular on-chip peripherals.

Members of the MPC860 family are the first embedded PowerPC microprocessors to address the needs of the internet-working and data communications markets. The PowerQUICC™ (Quad Integrated Communications Controller) integrates a PowerPC core, a memory controller, a RISC-based communications processor module, and a circuit board's worth of system functions on a single chip.

XPC602



Features:

- 32-Bit PowerPC Implementation
- Dual 4-KB Caches
- Dynamically Selectable 32- or 64-Bit Data Bus
- Time Multiplexed Address/Data Bus
- Single-Precision FPU
- Special Mode Calls O.S. Without Incurring Exception Processing Latency
- Memory Management Unit
  —Block and Page Translation and Protection Mode
  —Page Protection-Only Mode for Embedded Applications
- Burst Memory Interface

- Low Power Static Design
  —3.3 Voltage Operation
  —Dynamic Power Management
  —1.2 Watt Maximum Power Consumption at 66 MHz Full Operation
  —Nap, Doze, & Sleep Modes
- Fully JTAG-Compliant
- On-Chip PLL for CPU Clock × 1, × 2, or × 3 Bus Clock
- Data Bus Snooping
- On-Chip Debug and Development Support
- Low-Cost 144-PQFP Package

Target Markets/Applications:

As the entry point into the MPC600 family, the XPC602 offers excellent performance at a lower cost. Applications include high-end laser printers, set-top3 boxes, and high-end games.

Literature:

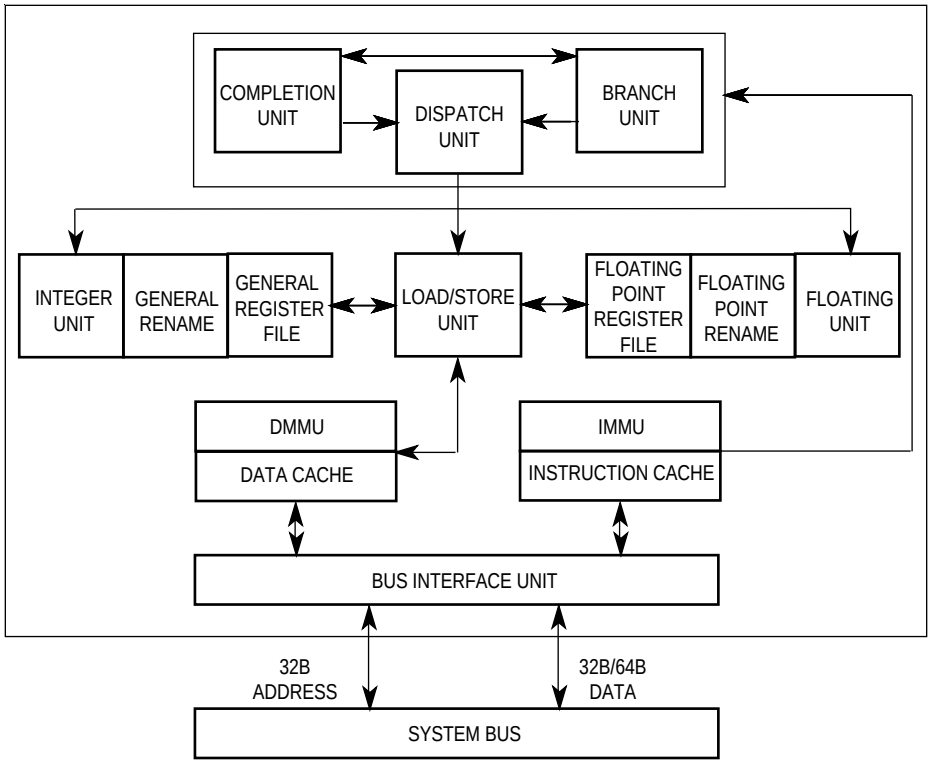
Title	Order Number
PowerPC602 Technical Summary	MPC602/D
PowerPC602 Microprocessor Fact Sheet	PPC602FACT/D

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XPC602	144-Lead FC	66	—	—	1	1	10	

NOTE: FC = Plastic Quad Flat Pack
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

XPC603/603e



603/603e Features:

- 32-Bit PowerPC Implementation
- Superscalar (3 IPC)
- Single/Double Precision FPU
- Memory Management
- Snooping of Data Cache
- Burst Memory Interface with Split and Pipelined Transactions
- Programmable CPU Clock Multiplier

  —603 - 1×, 2×, 3×, or 4× Bus Clock
  —603e - 1×, 1.5×, 2×, 2.5×, 3×, 3.5×, or 4× Bus Clock
- 64- or 32-Bit Data Bus
- Low Power

  —Dynamic Power Management
  —Nap, Doze, & Sleep Modes

603 Features Only:

- 75 SPEC int 92, 85 SPEC fp 92 @ 80MHz
- Dual 8-KB Caches with Snooping
- Low Power - 3 watts @ 80 MHz

603e Features Only:

- 120 SPEC int 92, 105 SPEC fp 92 @ 100 MHz
- Dual 16-KB Caches with Snooping
- Low Power - 3 watts @ 100 MHz

Target Markets/Applications:

The XPC603 and XPC603e are ideally suited to high-performance embedded control applications that require high performance at low cost. Target markets include high-speed LAN controllers (ATM, Ethernet, FDDI, X.25, etc.), I/O processor, laser printers, X-terminals, routers, bridges.

Literature:

Title	Order Number
PowerPC 603 Microprocessor Fact Sheet	PPC603FACT/D
PowerPC 603 Technical Summary (Rev 3)	MPC603/D
PowerPC 603 Hardware Specifications (Rev 0)	MPC603EC/D
PowerPC 603 User's Manual	MPC603UM/AD
PowerPC 603e Technical Summary	MPC603E/D

Support Chips:

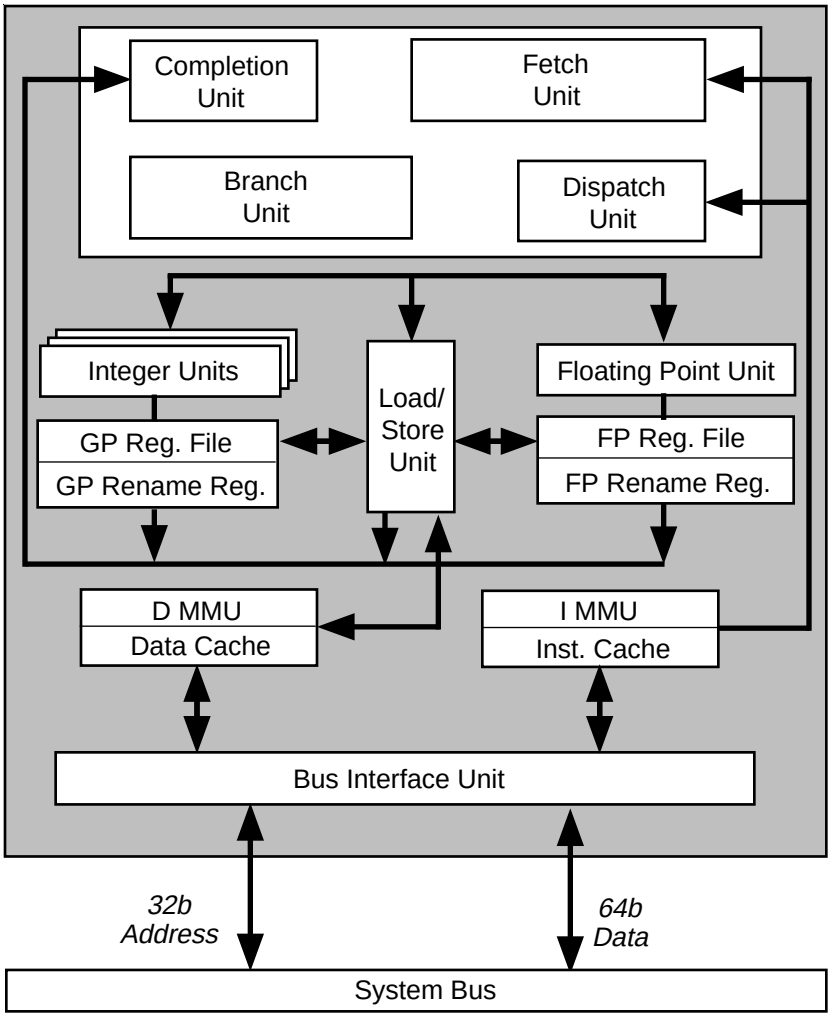
MPC105—PCI Bridge/Memory Controller
MPC930/931—Clock Drivers
Crystals—Champion, Kyocera, ACT
FSRAMS—MCM72MS32, MCM72MS64, MCM67M518, MCM67M618

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XPC603	240-Lead FE	66, 80	B	0 to 70°C	0	120	120	KXPC603AFEXXCB
	256-Lead RX	66, 80	B	0 to 70°C	1	1	1	
XPC603e	240-Lead FE	80, 90	D	0 to 70°C	1	120	120	KXPC603EFEXXCD
	256-Lead RX	80, 90, 100, 120, 133	—	0 to 70°C	1	1	1	

NOTE: FE = Ceramic Quad Flat Pack (CQFP)
RX = Ceramic Ball Grid Array (CBGA w/o Lid)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

XPC604



604 Features:

- 16-Kbyte Instruction Cache and 16-Kbyte Data Cache
- Superscalar – Four Instructions Per Clock Cycle
- Dynamic Branch Prediction
- Multiple Integer Units
- 64-Bit Data Bus
- Fully JTAG-Compliant

Tarket Markets/Applications:

The PowerPC 604 offers very high performance for the most demanding embedded applications such as telecom, switching, and internet working.

Literature:

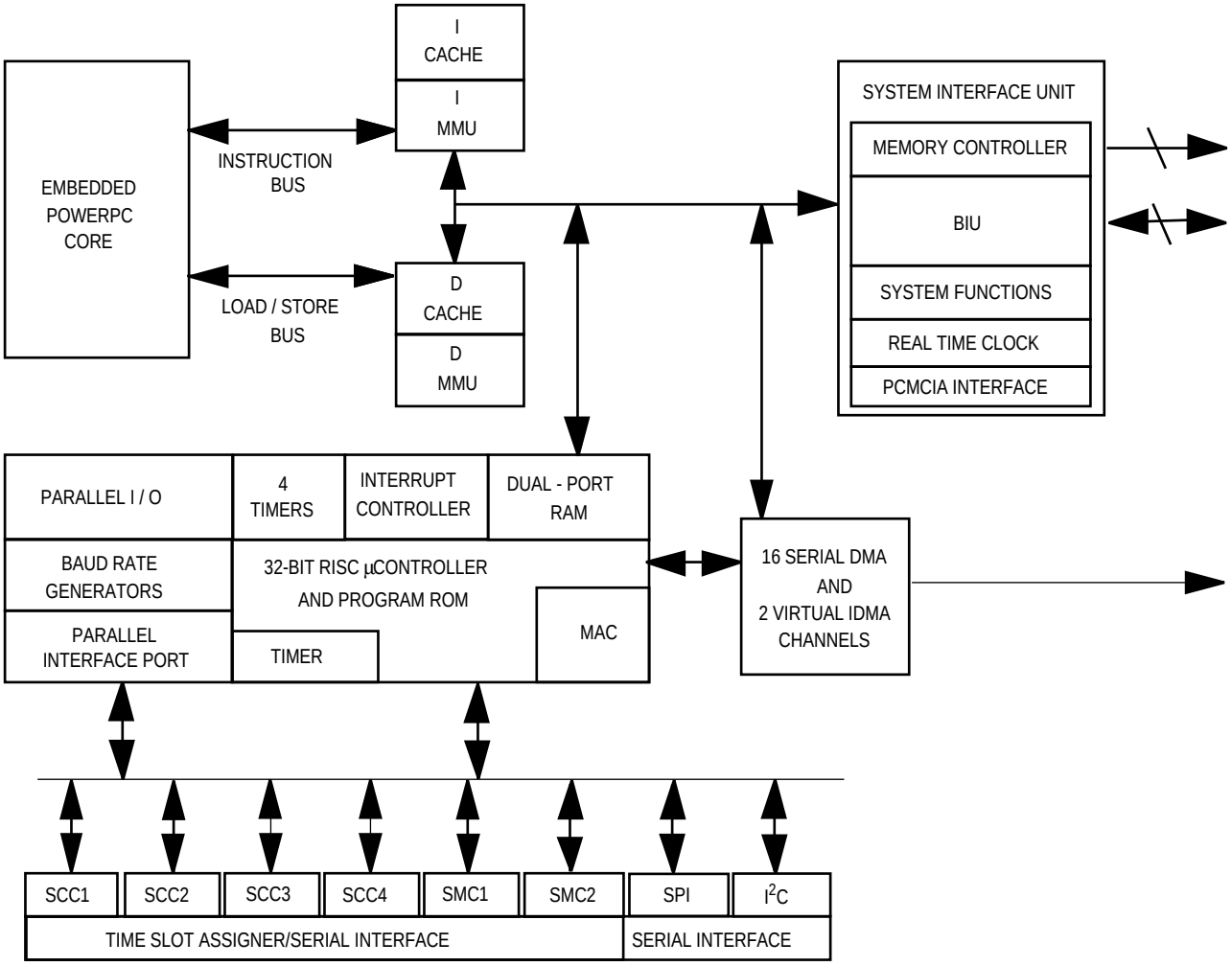
Title	Order Number
604 Technical Summary	MPC604/D
604 Hardware Specifications	MPC604EC/D
604 User's Manual	MPC604UM/AD
604 Fact Sheet	PPC604FACT/D
604 Microprocessor Brochure	BR1148/D

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
XPC604A	304-Lead FX	100, 120, 133	B, E	0 to 70°C	1	1	1	
	256-Lead RX	100, 120, 133	B, E	0 to 70°C	1	12	12	

NOTE: FX = C4 Ceramic Quad Flat Pack (CQFP)
RX = Ceramic Ball Grid Array (CBGA w/o Lid)
MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

PPC860



Features:

- Embedded PowerPC Core with 52 MIPS at 40 MHz (using Dhrystone 2.1)
- Single Issue, 32-Bit Version of the Embedded PowerPC Core (Fully Compatible with Book 1 of the PowerPC Architecture Definition) with 32 × 32 - Bit Fixed Point Registers
- Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8, 16, and 32 Bits)
- 32 Address Lines
- Complete Static Design (0–40 MHz Operation)
- Memory Controller (Eight Banks)
- General-Purpose Timers
- System Integration Unit (SIU)
- Interrupts

- Communications Processor Module (CPM)
- On-Chip 16 × 16 Multiply Accumulate Controller (MAC)
- Four Baud Rate Generators
- Four SCCs (Serial Communication Controllers)
- Two SMCs (Serial Management Channels)
- One SPI (Serial Peripheral Interface)
- One I^2C (Inter-Integrated Circuit) Port
- Time-Slot Assigner
- Parallel Interface Port
- PCMCIA Interface
- Low-Power Support
- Debug Interface
- 3.3 V Operation with 5V TTL Compatibility
- 357-Pin Ball Grid Array (BGA) Package

Target Markets/Applications:

- Ethernet Bridges and Routers
- Wireless Communication
- LAN to WAN Connections
- PBX Switches
- Smart Hubs
- Cellular Base Stations
- Simultaneous Voice and Data
- T1/E1 Interface Lines
- Fault-Tolerant LANs
- Remote Access Routers

Literature:

Title	Order Number
MPC860 User's Manaual	MPC860UM/AD

Support Tools:

MPC860ADS—PowerQUICC™ Application Development System

Package/Speed Options:

Device	Package	Speed	Rev	Temp	Order Quantity			For Sample Order
					SOQ	MPQ	POQ	
PPC860	BGA ZP	25		0 to 70	—	—	—	MPC860ZPXX

NOTE: ZP = Ball Grid Array (PGA)

MPQ = Minimum Package Quantity
POQ = Preferred Order Quantity
SOQ = Sample Order Quantity

First Silicon: Mar 93
MC Qualification Date: 1Q95
Die Size: 450 × 450 (0.8µ); 365 × 364 (.65µ)

COMPETITION

AMD

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
2903X	68EC030/040	• RISC core • SMT capability • 4-Kbyte on-chip instruction cache	• Very poor DRAM performance • No on-chip data cache • Not price aggressive • 29035 only in 16 MHz
29005/050	LC040	• RISC core • 17–32 MIPS at 40 MHz • Floating-point support	• MIPS rating < 040 at same clock frequency • Poor DRAM performance
29200	68340	• Performance (RISC vs. CSIC)	• Not price competitive • Little integration • No low power mode
	EC020	• Integrated device for laser printers	• Only 16 MHz available • 25-MHz EC020 has higher performance-to-cost ratio • Not general purpose
FDDI	FDDI	• Established Ethernet customer base • Provide excellent support and documentation • Sponsors of the European Advanced Networking & Test Center (EANTC)	• Poor integration strategy • Needs more external circuitry • Design team broken up to focus on 386/486
286	EC020	• Intel architecture	• Non-32-bit register set, dedicated registers • Segmented addressing range • Only a 16-bit data bus • Not CMOS
	CPU32	• Intel architecture • Comparable performance with CPU32	• No integration • Higher system cost
386	EC030/030	• 32-bit architecture • Intel architecture • CMOS implementation	• Compatibility/performance issues with '286 • Lower performance architecture • No on-chip caches, no burst mode

Hitachi

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
HC000	HC000	• Very price aggressive	• Not Hitachi proprietary architecture • No second-source support network
H8/500	68331/332	• A/D on-chip • Good timer performance • Small package	• Poorer CPU performance • Lower serial channel performance • Does not have flexibility of TPU

IDT

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
3051/2	EC040	• R3000 core • Price aggressive	• Poor DRAM performance • Multiplexed bus • Inferior development tools
3040	EC030	• Price	• Poor DRAM performance • Multiplexed bus • Inferior development tools

INTEL

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
960SA/B	68340 (25 MHz)	• Faster speeds available	• Lack of integration • Poorer price/performance ratio • No low-voltage parts available
	EC020	• Floating-point support on 'SB • Limited burst mode	• Multiplexed bus • Needs expensive memory for performance • RISC instruction set inefficient on memory usage
960KA/B	EC030	• RISC core (although only microcoded!)	• Poor performance in DRAM • Poor development tools • Not x86 code compatible • Not price aggressive • Multiplexed bus • No data cache
196	EC000		• EC000 is VERY price aggressive • No '196 upgrade path while EC000 is 68K entry point • Poor architecture • 8-bit bus
	68331/332/334	• A/D on-chip • Cost-effective 16-bit MCU	• No integration • Poor performance
186	EC000	• Good software base • Cost aggressive	• Not 32-bit architecture • Nonorthogonal architecture • No good migration path with integration
	68340	• 8 more chip selects • On-board memory refresh • Runs DOS	• Poorer CPU performance (0.5 × CPU32) • Lower addressing range • No JTAG support • Poorer DMA performance • No communications (serial) support
	68302		• No communications support
	68306	• 2 DMA channels	• Lower addressing range • No DRAM controller • No JTAG • No serial support
286	EC020/020	• Intel architecture	• Non-32-bit register set, dedicated registers • Segmented addressing range • Only a 16-bit data bus • Not CMOS
	CPU32	• Intel architecture • Comparable performance with CPU32	• No integration • Higher system cost
386SX	EC030	• 16-bit bus gives smaller package	• Performance limited by 16-bit bus • Compatibility/performance issues with '286 • Lower performance architecture • No on-chip caches, no burst mode

INTEL

386DX	EC030	• 32-bit architecture • Intel architecture • CMOS implementation	• Compatibility/performance issues with '286 • Lower performance architecture • No on-chip caches, no burst mode
486SX	EC030/EC040 LC040	• Entry point to '486 architecture • SMT option	• Part of confused marketing strategy vs 487SX • Architecture not as powerful as '040 • Unified cache—bottleneck
486D	68040	• PC base	• Lower performance than '040 at same clock (50-MHz '486 = 33-MHz '040) • Unified cache—bottleneck • No copy back cache—poor multi-processor
8051	EC000	• Cheap and cheerful	
	68330	• Price	• Poorer price/performance ratio

LSI Logic

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
LR33020	EC040	• Targeted at X-terminals • Cut-down R3000 core	• Poor DRAM performance • Not general purpose • Inferior development tools
33000	EC030	• Cut-down R3000 core • Integrated peripherals • SMT packaging	• Poorer DRAM performance • Not cost effective • Inferior development tools

National Semiconductor

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
FDDI	FDDI CHIP SET	• Basic MAC (BMAC) DP83261 very strong • Very price aggressive at strategic customers • Excellent documentation and support • Integration strategy firm	• Currently 5-chip solution • Critical layout required • No PCM state machine • BSI requires high-performance processor • No second source on MAC/PHY chips • No SMT software
HPC16400	68302	• Very price aggressive	• Lower performance core • Limited communications support (HDLC + UART) • Limited addressing range
NS32FX16	68331/332	• On-board DSP • Small package	• Only small installed software base • No configurable timing capabilities
	68302	• On-board DSP • Price aggressive	• Limited protocol support

NEC

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
V25/25+ V35/V35+	68302/340	• Very price aggressive • Single-chip versions available • Runs DOS	• Limited communications capability • Lower addressing range • Lower performance
78kVII	68331/332/ 333/340	• Very price aggressive	• Only half '302 performance • No timers/flash/microcode capability • No low-power capabilities • Limited installed software base

Siemens

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
80C166	68331/332	• Interrupt handler	• Low installed S/W base • Not a widely accepted architecture • No user-configurable timers

SGS-Thomson

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
ST10F166	68F333	• Interrupt handler	• Half as much flash EEPROM • Third of RAM size available • No silicon yet

Toshiba

Competition Device	Motorola Solution	Competition's Advantages	Competition's Disadvantages
HC000	HC000	• Very price aggressive	• Not Toshiba proprietary architecture • No second-source support network
	68330	• Very price aggressive	• Lower performance • No integration
68301	68302	• Price aggressive • Built-in Centronic	• No DMA • Only 3 dedicated UARTS—no multiple communications • No SCP port or microcode capability
	68306	• Built-in Centronics • 1 more serial channel	• No DRAM controller • Smaller address space
	68340	• Built-in Centronics	• No DMA • Lower CPU performance • No low power mode
68303	68340	• 1 superior timer • Dedicated motor control • DRAM controller	• Only 3 DMA channels • Lower CPU performance
	68306	• Timer • Dedicated motor control • DMA	• Smaller address space • Less robust DRAM controller

PRODUCT ROUTING

Device & Pkg.	Fab. Site	Probe	Assembly Site	Final Test Site
68000RC,L,P	MOS5	OHT	KLM	OHT/KLM
68000FN	MOS5	OHT	KLM/ANAM	OHT/KLM
68EC000FN	MOS8/TSC	OHT/TSC	KLM	OHT/KLM/SND
68EC000FU	MOS8/TSC	OHT/TSC	SHC	SHC
68HC000RC,FN,FC	MOS8/TSC	OHT/TSC	KLM	OHT/KLM/SND(FN)
68HC000P/LC	MOS8/TSC	OHT/TSC	CARSEM/KLM	OHT/KLM
68HC001RC,FN	MOS8/TSC	OHT/TSC	KLM	OHT
68HC001FC	MOS8/TSC	OHT/TSC	KLM	OHT
68008P	MOS5	OHT	ANAM	ANAM
68008L	MOS5	OHT	KLM	OHT
68008FN	MOS5	OHT	ANAM	OHT
68010RC,L,P,FN	MOS5	OHT	KLM	OHT
68020RC	TSC	TSC	KLM	KLM
68020FE	TSC	TSC	KLM	KLM
68020RP	TSC	TSC	CITIZEN	NML
68020FC	TSC	TSC	KLM	KLM
68EC020RP	TSC	TSC	CITIZEN	NML
68EC020FG	TSC	TSC	ANAM	SHC
68185FN,RC,FN	MOS3	CHNDLR	CHNDLR	CHNDLR
68030RC	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68030FE	MOS8/TSC	OHT/TSC	ATX/KLM	OHT
68030RP	MOS8/TSC	OHT/TSC	CITIZEN	OHT
68EC030RP	MOS8/TSC	OHT/TSC	CITIZEN	OHT
68040RC	MOS8	OHT	ATX	OHT
68060	MOS11	OHT	ATX/KLM	OHT
68230P	MOS5	MOS5	ANAM	ANAM
68230FN,LC	MOS5	MOS5	KLM	OHT
68302RC,FE,FC	MOS8	OHT	KLM	OHT
68306FC	MOS8	OHT	KLM	OHT
68306PVU	MOS8	OHT	ANAM	OHT
68307FG	MOS8	OHT	KLM	OHT
68307PU		OHT	SHC	OHT

Device & Pkg.	Fab. Site	Probe	Assembly Site	Final Test Site
68322FT	MOS8	OHT	SHC	OHT/SHC
68330FC	MOS8	OHT	KLM	OHT
68330PV	MOS8	MOS8	ANAM	OHT
68331FC	MOS8	OHT	ATX	OHT
68332FC	MOS8	OHT	ATX	OHT
68340FE	MOS11	MOS11	KLM	OHT
68340PV	MOS11	MOS11	ANAM	OHT
68340RP	MOS11	MOS11	CITIZEN	OHT
68340FT	MOS11	MOS11	ANAM	OHT
68341FT	MOS8	MOS8	ANAM	OHT
68349FT	MOS8	MOS8	ANAM	OHT
68360	MOS11	MOS11	KLM/CITIZEN	OHT
68450RC,L,P	MOS5	MOS5	KLM	OHT
68440RC,L,P,FN	MOS5	MOS5	KLM	OHT
68605RC	MOS8	OHT	KLM	OHT
68605FN	MOS8	OHT	ANAM	OHT
68606RC	MOS8	OHT	KLM	OHT
68606FN	MOS8	OHT	ANAM	OHT
68661PA,PB,PC	MOS3	MOS5	KLM	KLM
68681P,L	MOS5	MOS5	KLM	KLM
68681FN	MOS5	MOS5	KLM	OHT
2681P,L	MOS5	MOS5	KLM	KLM
2681FN	MOS5	MOS5	KLM	OHT
68824RC	MOS8	OHT	KLM	OHT
68824FN	MOS8	OHT	ANAM	OHT
68851RC	MOS8	OHT	KLM	OHT
68881RC,FN	MOS8	MOS8	KLM	OHT
68882RC,FN	MOS8	MOS8	KLM	OHT
68901LC,FN	MOS3	OHT	OHT	OHT
68901P	MOS3	OHT	ANAM	ANAM
68836FN	BIP3	BIP3	KLM	OHT
68837KB	MOS6	CHD	CHD	CHD

Device & Pkg.	Fab. Site	Probe	Assembly Site	Final Test Site
68837FC	MOS8	MOS8	ANAM	OHT
68838FC	MOS6	CHD	CHD	CHD
68839RC	MOS8	MOS8	KLM	OHT
68839FE	MOS8	MOS8	KLM	OHT
68847FC	MOS8	MOS8	Silicon Harbor	OHT
68840FE	MOS8	MOS8	KLM	OHT
68834PB	MOS8	MOS8	SWIRE	OHT

PACKAGE DESCRIPTION	SITE DESCRIPTION
EM = PLASTIC QUAD FLAT PACK (PQFP)	AIZU = AIZU, JAPAN
FC/FD = PLASTIC QUAD FLAT PACK (PQFP)	ANAM = KOREA
FE = CERAMIC QUAD FLAT PACK (CQFP)	ATX = AUSTIN, TEXAS
FG = PLASTIC QUAD FLAT PACK (PQFP)	CHNDLR = CHANDLER, ARIZONA
FM = MOLDED CARRIER RING	CITIZEN = CITIZEN
FN = PLASTIC LEADED CHIP CARRIER (PLCC)	EKB = EAST KILBRIDE, SCOTLAND
FT = PLASTIC QUAD FLAT PACK (PQFP)	KLM = KUALA LUMPUR, MALAYSIA
FU = PLASTIC QUAD FLAT PACK (PQFP)	MESA = MESA, ARIZONA
FV = 20 mm × 20 mm QUAD FLAT PACK	OHT = OAK HILL, TEXAS
FX = C4 CERAMIC QUAD FLAT PACK (CQFP)	SND = SONDAI, JAPAN
L/LC = CERAMIC DIP	TSC = TOHOKU, JAPAN
P = PLASTIC DUAL-IN-LINE PIN (PDIP)	
PB = 10mm × 10mm PLASTIC QUAD FLAT PACK	
PU = THIN QUAD FLAT PACK	
PV = THIN QUAD FLAT PACK (TQFP)	
R = PIN GRID ARRAY (PGA)	
RC = PIN GRID ARRAY (PGA), GOLD LEAD FINISH	
RP = PLASTIC PIN GRID ARRAY	
RX = CERAMIC BALL GRID ARRAY (CBGA W/O LID)	
ZP = BALL GRID ARRAY (PGA)	

FAB. SITE DESCRIPTION			
MOS1	EKB	4 INCH	>1.2 MICRON
MOS2	ATX	4 INCH	LOGIC PRODUCT
MOS3	ATX	4 INCH	>1.2 MICRON
MOS5	MESA	5 INCH	>1.2 MICRON
MOS6	MESA	6 INCH	ASIC PRODUCT
MOS7	AIZU	4 INCH	>1.5 MICRON
MOS8	ATX	5 INCH	.71–1.5 MICRON
MOS9	EKB	6 INCH	0.8–1.5 MICRON
TOHOKU	TSC	6 INCH	0.8–1.5 MICRON
MOS11	OHT	8 INCH	<0.8 MICRON
MOS13	OHT	8 INCH	7.5 MICRON

THIRD-PARTY SUPPORT

Please refer to BR729/D, *The 68K Source* for third-party support and contacts.

—NOTES—