	CICADA ENGINEERING SPECIFICATION	DOCUMENT NO. TFTR-10B4-H404A
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		DATE- 6/24/82
SUBJECT Timing Module Type 404		PREPARED BY Joe Bosco for Paul Sichta P. Sichta

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DATE	DESCRIPTION
6/24/82	Sections 4.0, 6.11.11, 6.11.12 and 6.12 revised Figures 10.1 and 10.2 revised

1.0 Abstract

This specification, in conjunction with reference documents, sets forth all characteristics of the subject module. The intended use of this document is to provide a minimum design goal for the module as well as a working dcoument for subsequent users.

2.0 Reference Documents

2.1 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), 1975. The Institute of Electrical and Electronic Engineers, Inc.

2.2 Telemetry Standards (Revised January 1971) IRIG, Document No. 106-71.

2.3 USA Standard Codes for Information Exchange, USAS X3.4-1968, ANSI X3.16-1966.

2.4 Printed Circuit Artwork Specification, Document TFTR-10A2-H53A.

2.5 Printed Circuit Board Fabrication ans Assembly Specification, Document TFTR-10A2-H54A.

2.6 PEP, Texas Instruments Bulletin, CR-114.

2.7 Electronic Schematic Specification, Document TFTR-10A2-H55.

2.8 Standard Timing Pulse Specification, Document TFTR-10A2-H57.

2.9 Facility Clock Subsystem Specification, Document TFTR-10B4-H401.

2.10 Reliability, Quality Control and Temperature Cycling Specification, TFTR-10A2-H58.

3.0 Introduction

The Timing Module when used in conjunction with the CICADA Facility Clock Subsystem provides the means for generating multiple timing signals throughout the Tokamak Fusion Test Reactor (TFTR) site at Princeton. In normal operation Timing Modules will continuously monitor a bi-phase encoded clock signal. Upon recognition of a particular code the Timing Module will start a count of clock pulses and then output a single timing pulse, the selection of assigned code as well as the counting time will be preselected by the CICADA computer system.

4.0 Basic Features

The Timing Module shall be housed in a double (2x) width CAMAC module and shall conform to the requirements defined by the CAMAC standard (reference 2.1). In addition to the standard CAMAC Dataway connections the module shall have one "Facility Clock" input channel and eight (8) independent output channels. The "Facility Clock" input shall be interfaced via a dedicated point on the Dataway Connector and the otuput channels shall be interfaced via a standard rear mounted auxiliary connector. The module shall function by monitoring the "Facility Clock" signal, which will be encoded in Bi-Phase Level format, (reference 2.2), for recognition of various assigned codes. Upon recognition of an assigned code the module shall cause the appropriate output channel(s) to go into an active state. When active, an individual output channel shall start a count of clock pulses which shall be internally derived from the encoded Facility Clock input. At the conclusion of the count the channel shall output a single timing pulse signal. The counting time for each output channel shall be independently assigned by CAMAC commands and may vary from one microsecond (1us) to approximately sixteen minutes (16 min). Code assignment for individual output channels shall be by CAMAC commands. Each output channel shall be capable of responding to any subset of sixteen (16) dedicated codes. A given channel will respond to all its assigned codes in the same manner. An additional feature of the module shall be the ability to respond to a dedicated "emergency stop" code. Upon recognition of the "emergency stop" code, the module shall reset all internal counters and output a pulse on all "emergency stop" channels. The assignment of "emergency stop" channels shall be accomplished by the placement of internal sitches. All channels, however, will reset in response to the "stop" code and will be inhibited from issuing an output pulse unless they are strapped as an "emergency stop" channel. Also, the module will accept simulated event codes via the CAMAC dataway write lines. When properly formatted, the module will accept the data and treat it as if it came from the TFTR Facility Clock system. In the case of "events" coming from both the dataway and the facility clock system, the facility clock system will have the higher priority.

5.0 Mechanical Characteristics

5.1 The module shall conform to mechanical specifications as indicated in reference 2.1.

5.2 The module shall be a double (2x) width CAMAC module.

5.3 The electrical components of this module are to be mounted on a high quality flame retardant epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. See reference specifcation 2.5.

5.4 This module is to contain all necessary mechanical components for insertion into a standard CAMAC crate. See referece specification 2.1.

5.5 All coponents are to be identified with a standard manufacturer's part number of standard method of marking (e.g., resistor color coing).

5.6 All electrical components are to be mounted on only one side of the board.

5.7 The condition of this module is to be monitored by LED's located on the module front panel. See Figure 10.1 for the suggested front panel layout. All lettering on the front panel shall be either engraved or silkscreened. The front panel material shall be aluminum with an iridite finish with contrasting colored lettering.

5.8 The 36 pin card edge connector (auxiliary connector) must mate with a Viking 3V18 connector (or equivalent). The card edge connector must be marked with pin 1 on top and pin 18 on the bottom on each side of the card.

5.9 All components are to be assigned an identifying part name (e.g., R1, C2, etc.) which is to be cross-referenced to the manufacturer's part number on the electrical schematic associated with this module. See reference specification 2.7.

5.10 Connector pin assignments shall conform to Figure 10.2.

6.0 Electrical Characteristics

6.1 This module must conform to the electrical requirements outlined in reference specification 2.1.

6.2 Whenever possible, low power circuitry (such as the 74LS series) shall be used to minimize power dissipation.

6.3 The module must derive its input power from the standard +/- 24 volt and +/- 6 volt CAMAC supply voltages.

6.4 Input/output signal characteristics for CAMAC Dataway operations shall conform to specifications as indicated in reference 2.1.

6.5 The Facility Clock input signal shall be a TTL compatible signal. The data format shall be as defined by reference 2.9, Section 6.3.2. The base frequency of the encoded Facility Clock signal shall be variable from 0.8MHz to 1.6MHz. The module shall operate over the fully frequency rnage and slew rate of the Facility Clock as defined by reference 2.9, Section 6.2.1.

6.6 The module shall continuously monitor and decode the Facility Clock signal. All elements of the ten bit code frame shall be tested for proper format as defined by reference 29. The module shall not respond unless all ten bits are determined to be correct. The module shall be capable of responding to octal codes 141/8 through 157/8. Upon recognition of an assigned code, the module will cause channel(s) assigned to the code to start counting. Any number of channels may be assigned to any code and any channel may be programmed to respond to any subset of the fifteen allowable codes. A given output channel will respond to all of its assigned codes in the same way.

Code 140/8 shall be designated as the "emergency stop" code. All output channels will respond to this code in one of two ways. Channels shall be designated as "stop" channels or "not stop" channels by the positioning of switches internal to the module. All hannels strapped as "stop" hannels shall respond to code 140/8 by outputting a timing pulse within 2 microsecond of receipt of the code, as meaured from the trailing edge of the Facility Clock stop bit and the leading edge of the output timing pulse. "Stop" channels that are active (counting) when the "emergency stop" code is received shall be reset so that a second timing pulse will not be transmitted for that channel. Channels strapped as "not stop" channels shall take no action in response to the "stop" code if they are in an inactive (non-counting) state. "Not stop" channels, active (counting) when a "stop" code is received shall be reset and the timing pulse that would normally occur at the end of the count shall be inhibitted.

Internal programming of the module (codes, count times and clock rates) shall not be affected by the receipt of an "emergency stop" code. All channels shall continue to respond to incoming codes after an "emergency stop" has occurred.

6.7 Individual output channels shall start a new cycle if one of its assigned codes is sensed while the channel is in its active (counting) state.

6.8 The module shall internally derive a clock signal from the Facility Clock for selective use by individual delay counters. The module shall provide three additional clock signals whose frequencies shall be counted down from the fundamental of the Facility Clock frequency, in the ratios of 1/10, 1/100 and 1/1000. Individual channels (8) shall selectively utilize one of the four (4) internal clocks for their respective delay counter. Selection of clock shall be accomplished by CAMAC commands.

6.9 The module shall provide, for each output channel, the capability for counting up to one million (10/6) clock periods. The accuracy of the delay time shall be +/- 1 clock period, (period of selected clock) and shall be measured from the trailing edge of the Facility Clock stop bit and the leading edge of the output pulse (see Figure 10.3).

6.10 The timing pulse output signal (8 channels) shall be transformer coupled and conform to the requirements defined by reference 2.8 (Standard Timing Pulse).

6.11 CAMAC Command Description

6.11.1 Command #1 Initialize or Clear [Z+C]

These commands must set all channels to an inactive state and disable all outputs.

6.11.2 Command #2 Read Module Number [F(6).A(0)]

This command gates the module identification number (decimal 404, binary 000110010100) on the Dataway read lines R1 through R12 with the LSB on R1.

6.11.3 Command #3 Read Assigned Code [F(1).A(*)]

This command gates a binary representation of codes assigned to chanel (*) onto Dataway read lines R1 through R16. Codes 141/8 through 157/8 shall correspond to lines R2 through R16 respectively. Dataway read line R1 shall be used to gate the channel's strapped designation. A logic '1' on line R1 will indicate that the channel is strapped as an "emergency stop" channel.

6.11.4 Command #4 Read Count and Clock [F(2).A(*)]

This command gates the assigned delay count length, for channel (*) onto Dataway read lines R1 through R20 with the LSB on R1, and the selected clock for channel (*) onto Dataway read lines. R1 and R22 in binary format as shown below.

Clock	R22	R21
1MHz	0	0
100KHz	0	1
10KHz	1	0
1KHz	1	1

6.11.5 Command #5 Write Code [F(16).A(*)]

This command loads the information on Dataway write lines W1-W16 to set assigned codes for channel (*). Codes 141/8 trhoguh 157/8 shall correspond to lines W2 through W16 respectively.

6.11.6 Command #6 Write Delay [F(17).A(*)]

This command loads the information on Dataway write lines W1 through W22 to set the assigned count and clock for channel (*). The information on lines W1 through W20 shall determine the count length in binary format with the LSB on W1. The information on lines W21 and W22 shall determine the assigned clock. The clock selection shall follow the format delineated in paragraph 6.11.4.

6.11.7 Command #7 Clear Code [F(9).A(*)]

This command clears all code assignments for channel (*) and disables channel (*) output.

6.11.8 Command Accepted (X) must be returned as logical "1" for all commands received and recognized as one that it is equipped to perform.

6.11.9 Q must be returned as a logic "1" for all addressed commands received by the module.

6.11.10 The module shall not generate or respond to CAMAC signals L, I, or B.

6.11.11 Command #8 Emergency Stop [F(26).A(0)]

This command will cause the module to respond as if an "emergency stop" code were received via the Facility Clock System. That is, all active counters will be reset and a pulse will be immediately issued on any channel switched to the "emergency stop" mode (see Section 4.0).

6.11.12 Command #9 Activate Event Code [F(18).A(1)]

This command loads the information on dataway write lines W1-W17 to force an event code into the module. The module would then treat this code as if it were received via the TFTR Facility Clock System. The information on the dataway must be formatted as shown below:

OCTAL CODE	HEX DATA FORMAT (W1-W24)
140	00 00 5F
141	00 00 1E
142	00 00 1D
143	00 00 5C
144	00 00 1B
145	00 00 5A
146	00 00 59
147	00 00 18
150	00 00 17
151	00 00 56
152	00 00 55
153	00 00 14
154	00 00 53
155	00 00 12
156	00 00 11
157	00 00 50

6.12 The module shall provide two LED indicators mounted on the front panel. One will be labelled "N" and will illuminate for 200ms whenever the module is addressed. The second LED will be labelled "code active". This will illuminate for 200ms whenever the module receives a valid event code; whether generated via the facility clock or the dataway write lines. The LED does not indicate whether any channels were programmed to respond to the event code.

7.0 Environmental Data

7.1 The module must operate over an ambient tempeature range of 0 to +50oC.

7.2 The module must operate over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must not be affected by an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 50 gauss in any direction.

7.4 The module must operate in a radiation environment of 1 rad/second (peak) with a total integrated lifetime dose of 1000 rad.

8.0 Reliability

8.1 The module must have an expected life of at least ten years under normal operating conditions. The module shall be rated for continuous operation.

8.2 All components on this module must be of high quality and have a MTBF rating of at least 10/6 hours. All components must have an exact replacement available from a second source manufacturer or have a readily available equivalent.

8.3 All integrated circuits used in this module must have undergone a burn-in procedure as provided by Texas Instruments PEP-3 Processing (see reference document 2.5). Equivalent processes from other manufacturers is acceptable.

9.0 Safety

9.1 All components of this module must be of flame retardant material.

	B	A	
Clean Earth (CE)	1	1	CE
CH1, HI	2	2	CH1, Low
CE	3	3	CE
CH2, HI	4	4	CH2, Low
CE	5	5	CE
CH3, HI	6	6	CH3, Low
CE	7	7	CE
CH4, HI	8	8	CH4, Low
CE	9	9	CE
CH5, HI	10	10	CH5, Low
CE	11	11	CE
CH6, HI	12	12	CH6, Low
CE	13	13	CE
CH7, HI	14	14	CH7, Low
CE	15	15	CE
CH8, HI	16	16	CH8, Low
CE	17	17	CE
	18	18	

FIGURE 10.2

PIN ASSIGNMENT, AUXILIARY CONNECTOR

(Viewed from front of crate)

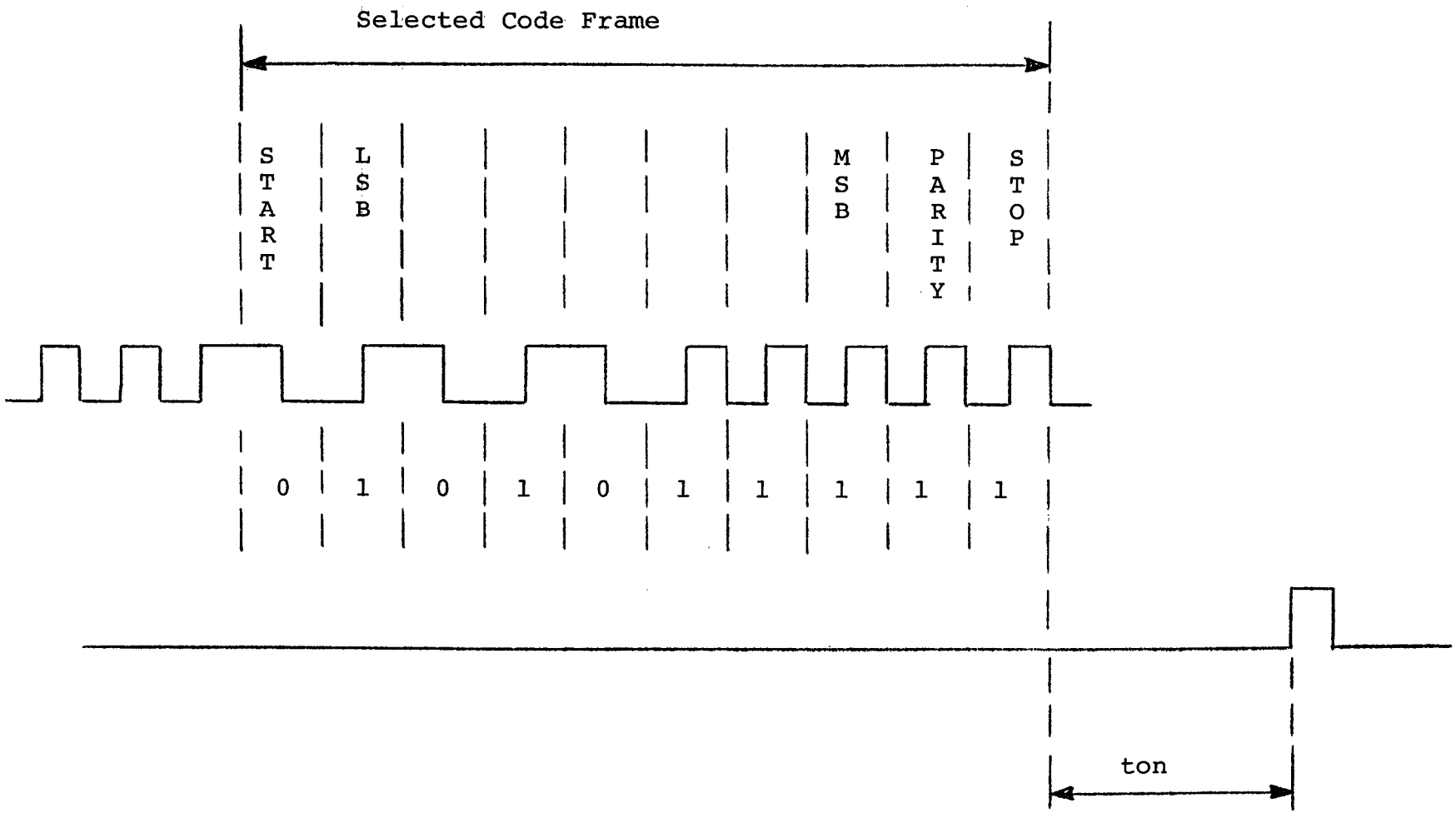


Figure 10.3 "On Time" Mark

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

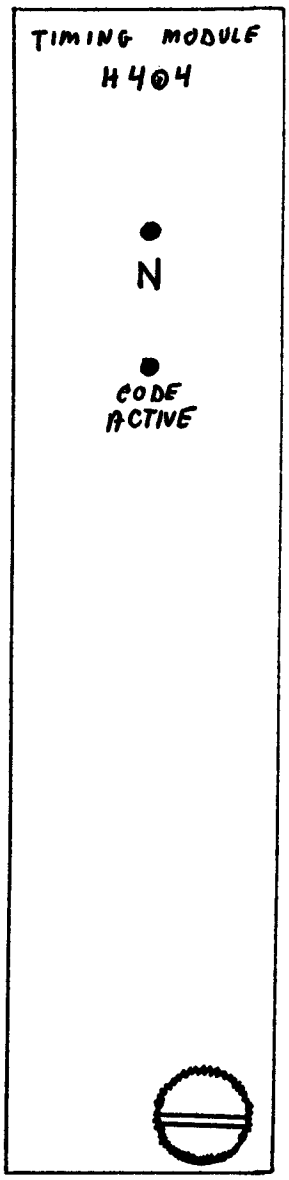
SUBJECT

DOUBLE WIDTH MODULE - TIMING MODULE H404

NAME

DATE 6/14/82

REVISION DATE



Facility Clock Codes

Octal code	404 Bit #	404 F(16) Hex Value	Clock Encoder F(16)	404 F(18)	Code Name
140	1	1	60	5F	Emerg Stop (Not used)
141	2	2	E1	1E	SOC
142	3	4	E2	1D	SOS
143	4	8	63	5C	T(-60)
144	5	10	E4	1B	SOP
145	6	20	65	5A	SOI (T(-1))
146	7	40	66	59	SOD (T(0))
147	8	80	E7	18	NBI
150	9	100	E8	17	T(+D)
151	10	200	69	56	EOD
152	11	400	6A	55	EOP
153	12	800	EB	14	Link Self Test
154	13	1000	6C	53	PC Fault
155	14	2000	ED	12	PC Event
156	15	4000	EE	11	FBL
157	16	8000	6F	50	Not used