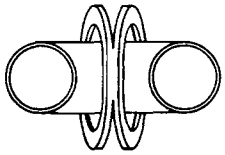


CICADA ENGINEERING SPECIFICATION

DOCUMENT NO.
TFTR-10B3-H337

PAGE 1 OF 15

DATE- 3/30/81

SUBJECT
Power Supply Controller Module

PREPARED BY
J. Pollock

APPROVED BY

CICADA HARDWARE SECTION HEAD

CICADA DEVICE CONTROL SOFTWARE SECTION HEAD

QUALITY ASSURANCE

CICADA MANAGER

REVISIONS

DATE	DESCRIPTION

1.0 Abstract

The purpose of this specification is to set forth the physical and electrical characteristics of the Power Conversion Power Supply Controller Module. This document in conjunction with referenced documents listed in Section 2.0 shall establish design and construction criteria.

2.0 Reference Documents

2.1 Power Conversion Data Link Protocol, Document #TFTR-10B3-H335.

2.2 IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), IEEE Standard #583-1975.

2.3 Printed Circuit Artwork Specification, Document #TFTR-10A2-H53.

2.4 Printed Circuit Board Fabrication and Assembly, Document #TFTR-10A2-H54.

2.5 Electronic Schematic Specification, Document #TFTR-10A2-H55.

2.6 Reliability, Quality Control and Temperature Cycling.

2.7 Power Conversion Link Repeater Module, Document #10B3-H336.

3.0 Introduction

The Power Supply Controller Module shall be used to interface the Power Conversion Link Repeater Module to the 12 bit parallel inputs of the firing angle generators in the Power Conversion power supplies. Thus, this module in conjunction with the Power Conversion Link Repeater Module (reference 2.7), shall be used as an element of the Central Instrumentation Control and Data Acquisition (CICADA) System to implement a distributed control system through the use of a single transmission cable loop around the TFTR Power Conversion area. The Power Supply Controller Module shall itself be controlled by the link repeater module (reference 2.7). Figure 11.5 is a functional block diagram of the module.

4.0 Basic Features

4.1 The module shall be programmable to recognize 1 of 6 power supply codes (0-5). The module shall ignore data from serial transmissions in which the power supply address field is not recognized.

4.1.1 Power Supply Address codes 6 and 7 are the aggregate power supply addresses. All power supply controller modules within a given house (i.e., those modules serviced by an addressed link repeater module) shall recognize this power supply address.

4.1.1.1 Aggregate power supply address code 6 (110) shall be recognized, but the contents of the output data register shall not change. This command shall be sent for the purpose of retriggering the 4ms time-out circuit (if R/W bit = Ø).

4.1.1.2 Aggregate power supply address code 7 (111) shall be recognized and all power supply controllers driven by the addressed link repeater module shall load their output data registers with the data in the data field of the transmission (if R/W bit = Ø).

4.2 The module shall have a 4 millisecond retriggerable "time out" circuit that shall be used to provide a "computer ready" signal output via an opto-isolator. If the "computer ready" time out is not retriggered at intervals less than 4 milliseconds apart, the "computer ready" output shall go into the open state. This condition will signal the power supply serviced by this module that the Power Conversion Link is down and the hardwired logic in the power supply must take approrpriate action.

4.3 The module shall analyze the power supply address field for the status of the read-write bit (reference document 2.1, Section 3.2.5) and shall act accordingly.

4.3.1 If R/W = 0, (write command) the data field shall be converted from the serial format into parallel data that is loaded into the output holding register.

4.3.2 If R/W = 1, (read command) the module shall load the data in the output holding register into a parallel to serial shift register which shall be used to send the output status back to the source of the serial data transmission (reference 2.1, Section 6.3.3).

4.4 The module shall not accept data under the following conditions:

4.4.1 The power supply address is not recognized.

4.4.2 The gap and parity bits in the power supply address field are not in the correct state.

4.4.3 The parity bit of the data field is not in the correct state.

4.5 The module shall be cascadable so that up to 6 (but typically 4) power supply controller modules can be operated from a single link repeater module (house address) (reference 2.1, Figure 11.1).

4.6 The module shall have 13 discrete and floating optoisolated outputs as per Figure 11.3 for the mode, firing angle, and READY bits.

4.7 The timing by which the power supply controller analysis and stores data transmissions is controlled only by the "clock" (reference 2.7, Section 6.7.1) from the Power Conversion Link Repeater Module. Thus, the module is synchronous with the link.

4.8 The module shall be equipped with the following status indicator LEDS on the front panel. See Figure 11.2.

4.8.1 PSA — This LED shall flash for 200ms when the module has recognized the power supply address field.

4.8.2 PSA ERR — This LED shall flash for 200ms when the module has detected a parity error in the power supply address field.

4.8.3 PSA AGG — This LED shall flash for 200ms when the module has detected the power supply address aggregate code of 110_2 or 111_2.

4.8.4 DATAERR — This LED shall flash for 200ms when the module has detected a parity error in the power supply data field. This status indicator is applicable for write transmissions only. Such errors prevent data from being loaded into the output register.

4.8.5 NOT RDY — This LED shall flash for 200ms when the module has not been addressed for 4 milliseconds. This shall also imply that a fault signal has been sent to the module's respective power supply via the "computer ready" output. This output must maintain a closed circuit condition for power supply operations. If it assumes the open state, the power supply shall through its hardwired logic, revert to a bypassed, non-rectifying status.

4.9 The module shall be equipped with a power-on-reset circuit which shall initialize all bits in the data output register to Ø. Thus, all of the optoisolated outputs are initialized to an open circuit state.

5.0 Mechanical Characteristics

5.1 The module shall be a single width (single slot) CAMAC module.

5.2 The module shall conform to the mechanical specifications as indicated in reference 2.2.

5.3 The electrical components of this module shall be mounted on a high quality epoxy glass printed circuit board such as NEMA Type FR-4 or equivalent. See reference documents 2.2 and 2.8.

5.4 This module shall be equipped with all of the necessary hardware for insertion into a standard CAMAC crate. See reference documents 2.2 and 2.8.

5.5 All electrical components are to be mounted on only one side of the printed circuit board.

5.6 The status of the module is to be monitored by front panel LED's. The layout and designated of those LEDS are illustrated in Figures 11.1 and 11.2.

5.7 All components are to be assigned an identifying part number which is to be cross referenced with the manufacturer's part number on the schematic.

5.8 The 36 pin card edge auxiliary connector must mate with a Viking 3V18 or equivalent. The pin assignments for this connector are listed in Figure 11.4. The parallel optically isolated outputs intended for the inputs of the power supply firing generator are assigned to this connector.

5.9 The I/O control and data signals that flow to/from the link repeater module are assigned to front panel shielded connectors (i.e., LEMO #RA.304N4LS4.2). See Figure 11.2.

5.10 The front panel shall be drilled as per Figure 11.1.

6.0 Electrical Characteristics

6.1 The module shall derive its required power from the +6 volt CAMAC power supply voltage on the dataway.

6.2 The module shall not interfere with the CAMAC link nor the crate in which the module is installed.

6.3 The module shall accept the following TTL level signals from the link repeater module via I/O connectors on the front panel.

6.3.1 Clock (Input)

This TTL level input shall control the sequence timing of the module.

6.3.2 Data (Input)

This TTL level input shall in conjunction with reference 6.3.1 be converted into parallel data by the power supply (PSA) address and output data shift registers.

6.3.3 Enable (Input)

The enable signal shall normally initialize all serial to parallel conversion link and inhibit that logic from accepting data unless the link repeater module has recognized the house address field of the transmission.

6.3.4 Clock and Data (Output)

The clock and data output is a TTL compatible open collector output which, if other power supply controller modules are assigned to the same link repeater module, it is or tied to the clock and data lines of the other power supply controller modules assigned to that link repeater module.

6.4 The +6 volt supply voltage must be bypassed to ground with an electrolytic capacitor of at least 33 microfarads. In addition, there must be at least one VVC (+5 volt) to ground ceramic bypass capacitor for every two integrated circuits on the module. The .01 microfarad capacitors shall be located as close as possible to the integrated circuits.

6.5 All digital outputs are optically isolated, open collector transistors.

6.6 The optically isolated transistor (opticoupler) outputs shall be rated as follows:

6.6.1 Collector current (on): 50ma maximum

6.6.2 Collector current (off): 10ma maximum

6.6.3 BVceo: 28 volts minimum

6.6.4 Vce (sat): 1.2 volts maximum

6.6.5 Rise time (tr): 20us maximum (Figure 11.4)

6.6.6 Fall time (ts): 20us maximum (Figure 11.4)

6.7 The eleven (11) outputs (Figure 11.3) represent the firing angle and mode. These outputs are latched.

6.8 The 12th output (ready) is sustained in the "on" state only by the presence of write commands that must be recognized by the module at intervals of not more than 4 milliseconds apart. If more than 4 milliseconds between write messages elapse, the ready output assumes a high impedance, open circuit condition. This shall be used to initiate the procedure as per section 4.7.4.

7.0 Environmental Data

7.1 The module must operate, as defined, over an ambient temperature range of 0 to $+50^{o}C$.

7.2 The module must operate, as defined, over a relative humidity range of 10% to 90%. It is not a requirement that the module operate under conditions of water condensation.

7.3 The module must operate, as defined, in the presence of an external magnetic field changing at a maximum rate of 100 gauss per second with a peak magnitude of 200 gauss in any direction.

7.4 The module must operate, as defined, in a radiation environment as follows:

Neutrons	2×10^{7} n/CM^{2}/sec
Rad-Dose	5×10^{-2} rad (Si)/sec
Integrated Dose	200 rad (Si)

8.0 Safety

8.1 All components of this module must be of flame retardant material.

9.0 Testing

The testing of this module shall be conducted with a known good link repeater module (H336) which shall receive transmissions from a test station. The test station shall generate and receive those test transmissions as per reference document 2.1. Each output stage shall be tested as per the circuit described in Figure 11.4. The outputs shall perform within the limits defined by paragraph 6.6 and Figure 11.4. After functional testing has been completed and any inconsistencies in performance have been corrected, then functional testing shall continue with the module operating in an environmental chamber as per reference document 2.6.

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: FRONT PANEL LAY OUT
POWER SUPPLY CONTROLLER MODULE

NAME: POLLOCK

DATE: 10-17-80

REVISION DATE:

FIGURE 11.2

SCALE; 1:1

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: FRONT PANEL LAYOUT
POWER SUPPLY CONTROLLER MODULE

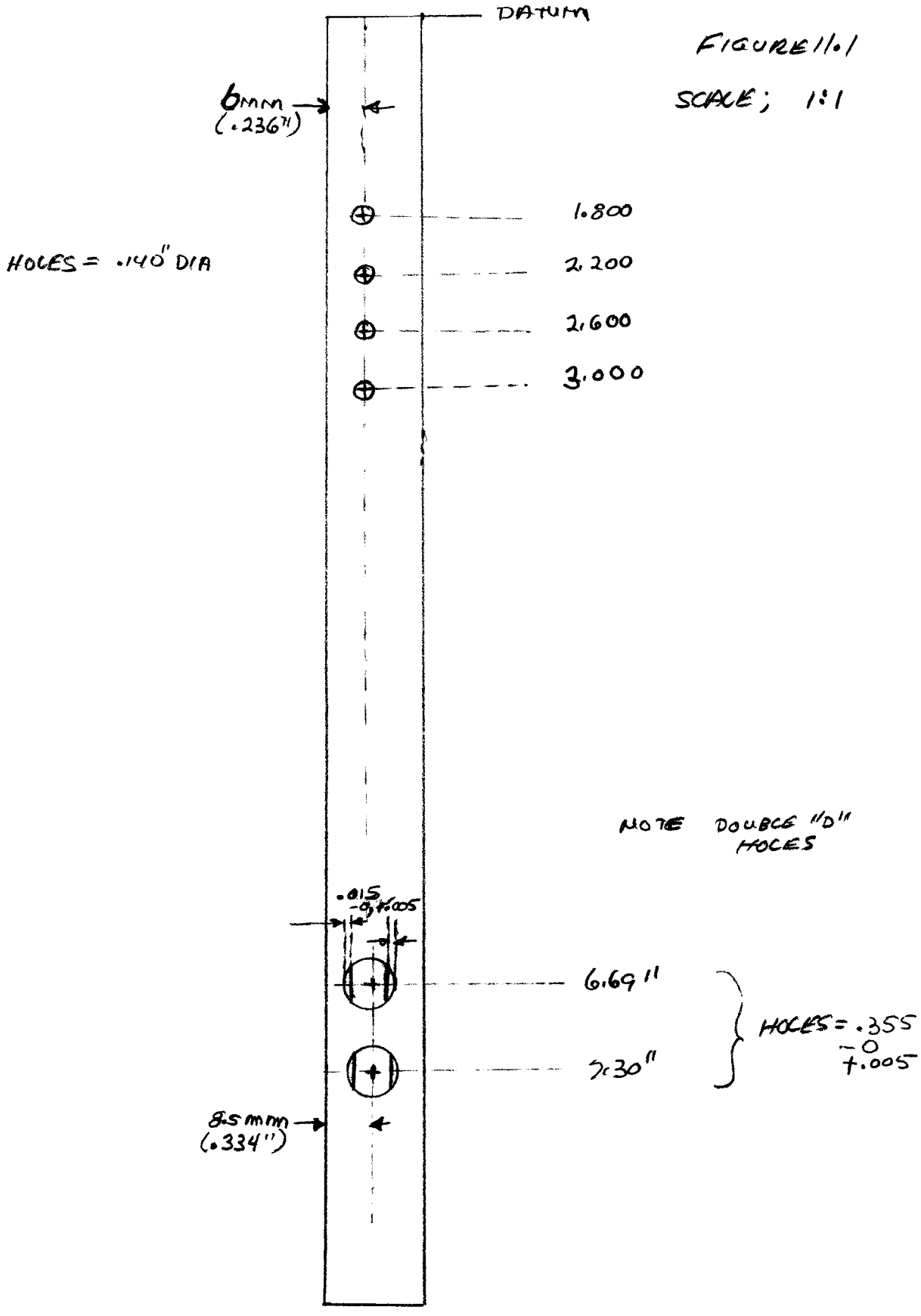
NAME: J. Pocock

DATE: 10-17-80

REVISION DATE:

FIGURE 11.1

SCALE; 1:1



NOTE DOUBLE "D" HOLES

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: POWER SUPPLY CONTROLLER MODULE AUXILIARY EDGE CONNECTOR PIN ASSIGNMENT

NAME: J. BLOCK

DATE: 10-17-80

REVISION DATE:

FIGURE 11.3

B		A		
1	1	1	2^0	LSB
1	2	1	2^1	
1	3	1	2^2	
1	4	1	2^3	
1	5	1	2^4	
1	6	1	2^5	
1	7	1	2^6	
1	8	1	2^7	MSB
1	9	1	CONVERT	
1	10	1	CYCLIC BYPASS	
1	11	1	BLOCK BYPASS	
1	12	1		
1	13	1		
1	14	1		
1	15	1		
1	16	1	RDY	

FIRING ANGLE DATA

POWER SUPPLY MODE

SPARES

VIEW FROM REAR OF CRATE

NOTE: THE EMITTER OF EACH

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

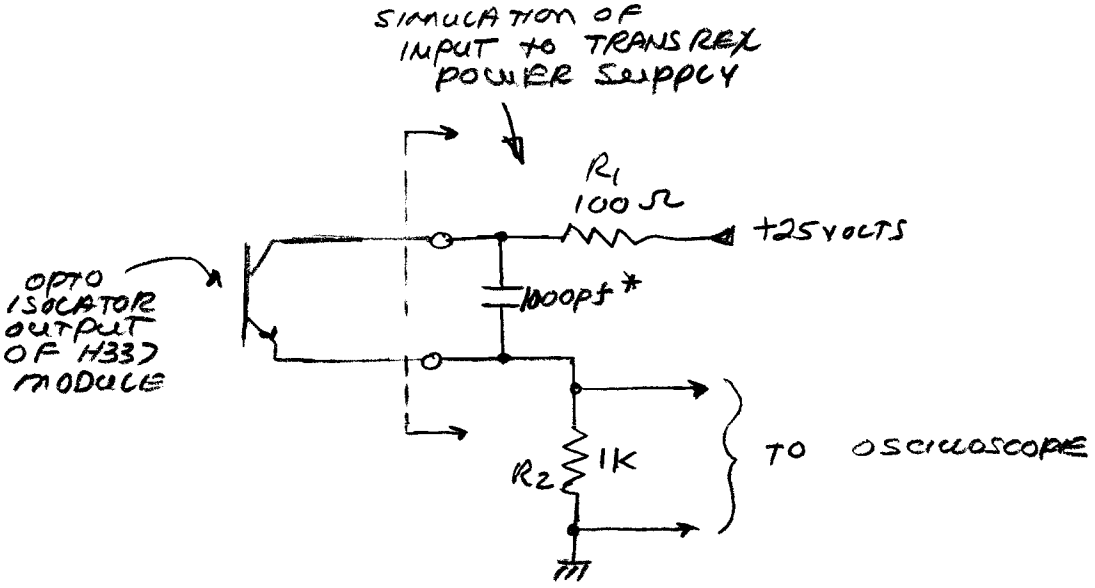
PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: TYPICAL OUTPUT TEST CIRCUIT.

NAME: J. Pollock

DATE: 10-12-80

REVISION DATE:



* 1000pf SIMULATES CABLE STRAY CAPACITANCE

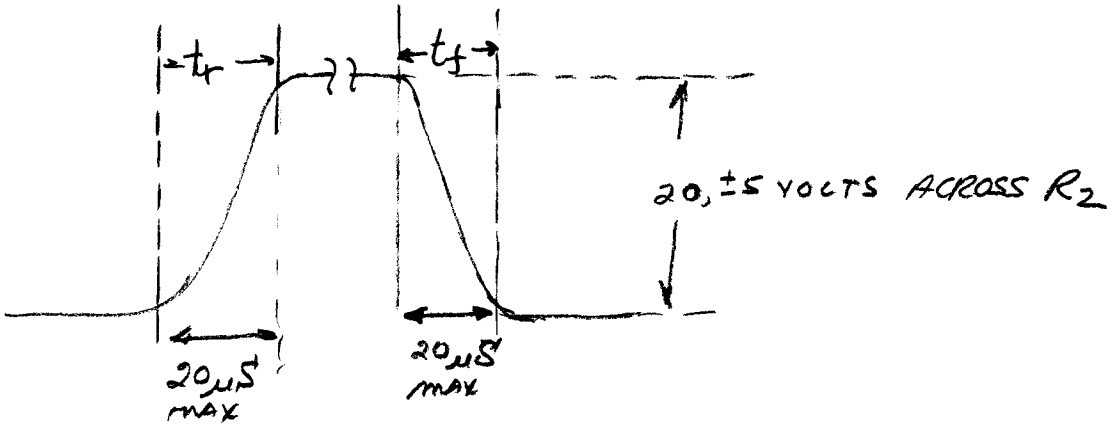


FIGURE 11.4

PRINCETON PLASMA PHYSICS LABORATORY

ENGINEERING NOTE

PROJECT	SERIAL-CATEGORY	PAGE

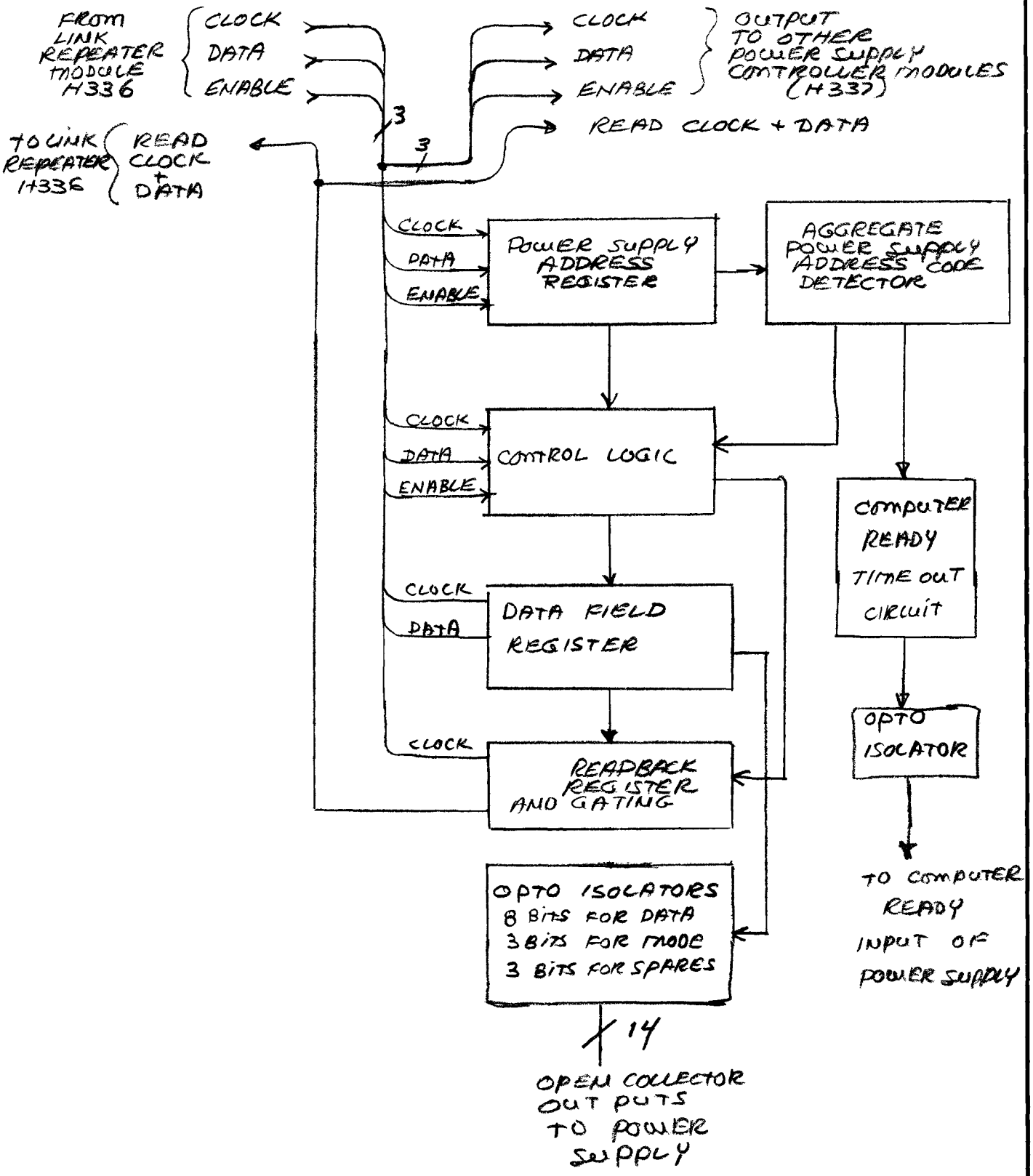
SUBJECT: POWER SUPPLY CONTROLLER MODULE BLOCK DIAGRAM

NAME: J. POLLOCK

DATE: 12-1-80

REVISION DATE:

FIGURE 11.5



6/24/91 JF

P.C. LINK MODULE ADDRESSING

- H336 Link Repeater Aggregate House Address:
  - Code: 111111_2 (63_{10})
  - To Disable: Lift pin 3 of U20, ground pin 12 of U20
  - Function: Addresses all H336's including TF, EF + OH Sub-Aggregate addresses.
  - Display: "HA AGG" LED lights when addressed.

- H336 Link Repeater Sub-Aggregate House Addresses:
  - Codes: 111110_2 (62_{10}) for all TF 336's
    111101_2 (61_{10}) for all EF 336's
    111011_2 (59_{10}) for all OH 336's
  - To Disable: Disabled if Aggregate House Address has been disabled (see above).
  - Function: Provides addressing of groups of H336's that are associated with one of the three types of Power Supplies (TF, EF or OH)
  - Display: "HA AGG" LED lights when addressed.
  - To Select: TF - Lift pin 3 + 12 of U20
    EF - Lift pin 11 of U20
    OH - Lift pin 6 of U20

- H336 Link Repeater House Addresses:
  - Codes: 000000_2 through 111111_2 (0_{10} through 63_{10})
    NOTE: Addresses used as Aggregate and Sub-Aggregate addresses (59_{10}, 61_{10}, 62_{10} & 63_{10}) are

invalid codes.

Function: Provides individual addressing of an H336.

Display: "HA" LED lights when addressed.

To Select: S1 (6 switch Dipswitch) selects logic level for each address bit.

Logic 1 = Open switch, associated Front Panel LED is on.

Logic 0 = Closed switch, associated Front Panel LED is off.

- H337 Power Supply Controller Aggregate Addresses:

Codes: 110_2 (6_{10}) for all H337's of an associated H336. No change in the output register.

111_2 (7_{10}) for all H337's of an associated H336. Data word loaded to the output register.

Function: Code 6_{10} used as a "Keep-Alive" signal to the 4 ms time-out circuit.

Code 7_{10} permits the outputs of all H337's of an associated H336 to be commanded to the same state.

Display: "PSA AGG" LED lights when addressed.

- H337 Power Supply Controller Addresses:

  Codes: 000_2 through 101_2 (0_{10} through 5_{10})

  Function: Provides individual addressing of one of, as many as, six H337's associated with a given H336.

  Display: "PSA" LED lights when addressed.

  To Select: Jumper on J3 installed in one of six positions associated with addresses 0_{10} through 5_{10}.