28XX Series Digitizers
4012 Controller
5000 Series Memories
DSP TECHNOLOGY INC.

TRAQ

REFERENCE MANUAL

PROPRIETARY STATEMENT

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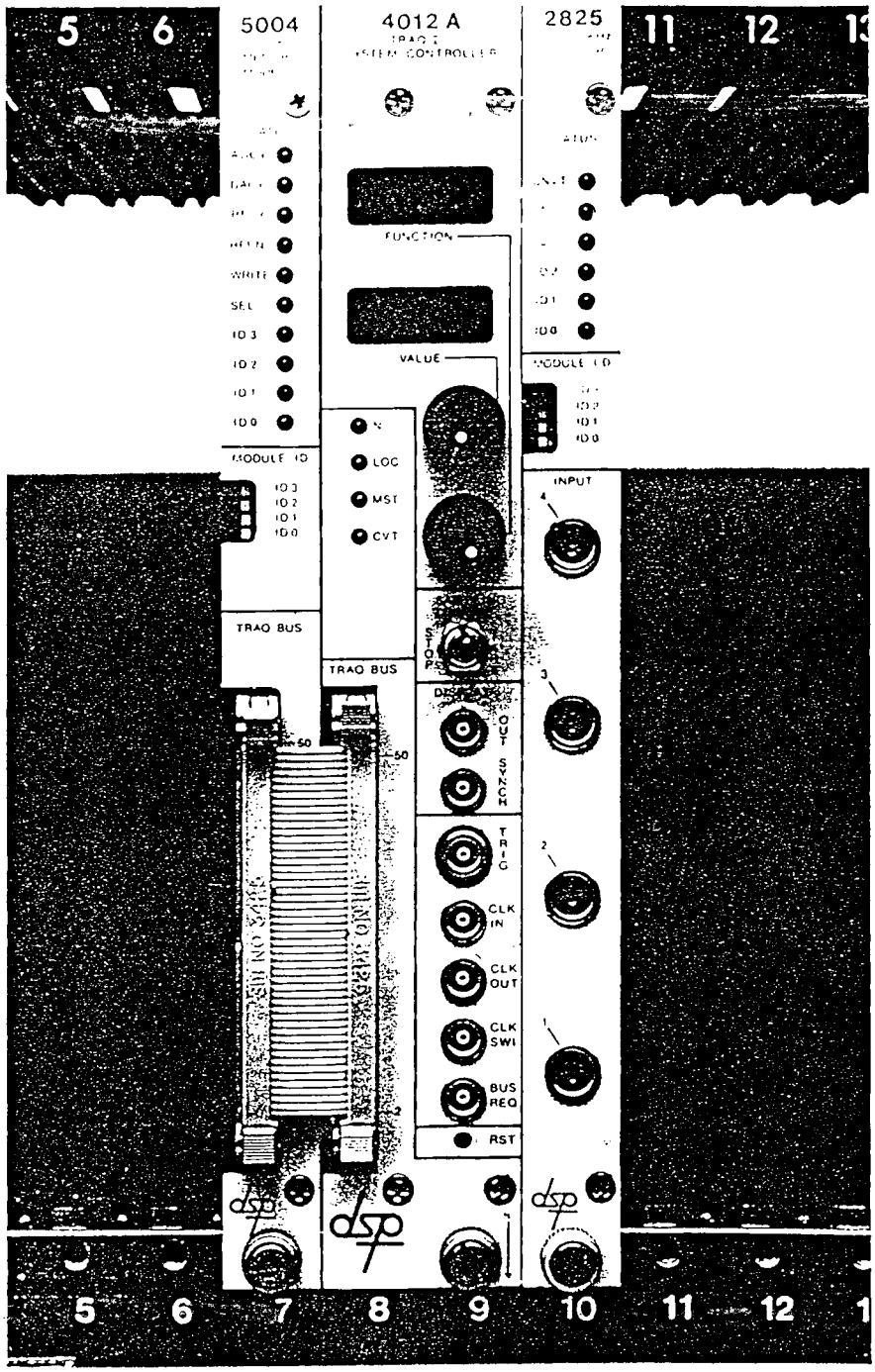
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TRAQ SYSTEM

SYSTEM DESCRIPTION

DSP Technology's TRAQ system is a modularized product to acquire analog or digital data from multiple input channels and store the information in local memory. Throughput rates up to 5 or 8 million data samples per second are available depending on which TRAQ controller is selected. Modularized memory and analog digitizer (or digital interface) units allow easy system field expansion or reconfiguration.

Each TRAQ system is defined by one controller (4012, 4012A or 4012P..), at least one memory module (5000, 5003, 5004, 5200..) and at least one digitzer module or input channel (2812, 2824, 2825, 2850...). See diagram 1.

Data transfer from the digitizer modules to memory is initiated by a clock pulse which the controller generates from an internal crystal or an external signal. There are actually two selectable internal clocks (CLK1,CLK2) which can be controlled by the user. This allows selected portions of the data to be sampled at different rates. There are many instances where some portions of the data which has higher frequency components needs to be sampled at faster rates. The 4012 will accept an external control signal which causes the unit to switch between the two clock frequencies. There is also available a mode in which the 4012 will switch to the second frequency after detecting a 'stop trigger'. When the 4012 is sampling with the second clock (CLK2) the 16th bit of the data (MSB) is set to a binary one. This allows the user to diffferentiate data sampled at the two clock rates. (Note: This option can be defeated by a jumper strap if the 16th bit is used by the digitizer unit, see 4012 Options)

Once the digitizer units receive the clock pulse (conversion command) all analog data is sampled simultaneously and the digital data is stored in a local buffer memory. Analog data is captured by sample & hold circuits which hold the signals constant as the analog to digital converters (ADCs) operate. Each sample & hold feeds directly into its own ADC or is mulitiplexed into a common ADC. At the end of the conversion cycle a signal is sent back to the controller signaling that data is ready for readout. The controller then sequentially reads data for all required channels. The user can select the number of channels (NOC) that are actively converting. As the NOC is decreased the controller will allocate more memory storage for the active channels. Data is transferred sequentially as 16 bit words to the controller at either a 5 Mhz or 8 Mhz maximum rate. The bus protocol allows the channel to control the rate of transfer.

The controller double buffers the digitizer data, forming a 32 bit word which is stored in memory. When sampling is started the first data sample is stored at address zero of the memory and

subsequent data at the next incremental memory location. After the memory is filled , new data is written over the previous data starting at address zero. This continuesin a 'round robin' fashion until a 'stop trigger' is received.The 'stop trigger' is either an external TTL signal, front panel switch, or computer command. This trigger initiates the 'post trigger' sampling sequence which determines how much data is recorded before the trigger versus after the trigger. If 'PTS'is set to '8/8' then all data is post trigger and sampling will stop once the entire memory is filled one more time.(I.E. if the memory size/ channel is 32 K samples, another 32K samples of data is recorded). If 'PTS' = '0/8' then recording stops immediately and all the data was recorded before the time of the trigger. The 4012 allows the user not only to select the amount of memory per data channel but also to divide this memory in 1/8th segments of post and pre trigger data. The controller also keeps track of where the earliest recorded sample resides in memory. All data read or displayed starts from this sample.

After recording is complete the controller will start to display the data or read it out to the computer. Data can be read starting at any 1024 block in the record. Also data readout can terminate at any point in the record and immediately go to another channel for readout.

TRAQ CONTROLLERS

The system controller is in command of all data acqusition. It communicates with the computer or user (through front panel controls) to determine the required sampling rate, pre/post trigger information, number of active data channels, memory allocation, data display and data readout. All control settings can be saved in a non-volatile memory to be restored on power-up. Communication with the computer is via the CAMAC bus, however, all data acquisition is passed through two private busses. Data from the input units is sequentially passed to the controller and then out to memory. The data is sequentially retrieved by the controller for display and readout.

The controller also executes a set of diagnostic routines on command or power up. These routines will usually catch and isolate any fatal system problem.

There are presently three controllers available for the TRAQ system:

Controller	Throughput speed (millions of samples/second)	Comments
4012	5	standard TRAQ controller
4012A	5 or 8	enhanced TRAQ controller
4012P	5 or 8	data retention on power down

The 4012P is used in environments where data retention upon loss of power is critical. The 4012P has extra control signals to protect acquired data and a reserved memory section for calibration data. This controller is used with 5200 memory modules.

TRAQ MEMORIES

The amount of data storage in a TRAQ system depends on the selected memory module. The combination of the memory and controller also determines the maximum throughput speed of the system.

Memory module	Data storage (samples/module)	Maximum data storage/system	Maximum throughput rate (samples/second)
5000	256 K (K = 1024)	2 Megasamples	5
5003	512 K	8 Megasamples	8
5004	1024 K	16 Megasamples	8
5200	128 K	2 Megasamples	8

All memory modules on a system must be of the same type; i.e a system cannot contain a mixture of two types of memories.

Controllers are delivered from the factory with timing set appropriate to the memories ordered with the system. The 4012A and 4012P timing can be changed by jumper selection on one of the pc boards (see 4012 Calibration section). Eight Mhz memories can run with controllers set for 5 Mhz operation without changing the controller timing. However, the resulting system will only run at a 5 Mhz maximum throughput speed.

ANALOG-to-DIGITAL CONVERTERS

A variety of analog to digital conversion units are currently available for the TRAQ system. A maximum of 256 channels of digitizers can be run on one system but the total throughput rate cannot exceed 5 or 8 million samples per second. The total throughput is calculated as the product of the number of active digitizer channels times the sampling rate.

Presently the following units are available:

Model	Number of channel/module	Maximum conversion speed/channel	Resolution
2812	8	100 kHz	12
2814	4	50 kHz	14
2824	2	2 MHz	12
2825	4	250 kHz	12
2860	4	1 MHz	12

Digitizers are delivered with strapping configurations to run either with 4012 or 4012A, 4012P controllers. Units with an 'A' after the model number of the side sticker (ex: '2812A') denote units compatible with the 4012A or 4012P controllers. Units can be field modified to run with different controllers (refer to Option sections of digitzers).

TYPICAL TRAQ CONFIGURATIONS

5 Megasample throughput system:

Contlr module	Memory module	Allowable memory sizes	Maximum number of ADC channels 2812	2825	2850	2824
4012 or: 4012A	5000 or: 5003 or: 5004	256K to 2 Meg : 512K to 8 Meg : 1 Meg to 16 Meg	50	20	10	2

8 Megasample througput systems: (requires 'A' strapping for digitizer units)

4012A or 4012P	5200 : 5200	128K to 2 Meg : 256K to 2 Meg	80	32	16	4

Note: This assumes that each channel of the
2812 is sampling at 100 Khz
2825 is sampling at 250 Khz
2850 is sampling at 500 Khz
2824 is sampling at 2 Mhz

TRAQ DIGITAL INTERFACE MODULE

This module is a general digital 32 line (two, sixteen bit digital channels) interface for the TRAQ system. It contains spare wire wrap socket space and a CAMAC interface for user customization.

TRAQ CURRENT & POWER REQUIREMENTS

Module	Current (amps) +6	-6	+24	-24 (volts)	Power (watts)
Controllers				(typical)	(typical)
4012	4.0	.05	.05	.05 (amps)	27 (watts)
4012A	same				27
4012P	same				27
Memories					
5000	1.8				11
5003	1.5				9
5004	2.5				15
5200	.9				6
Digitizers					
2812	1.5	.55	.15	.15	20
2824	1.0	.70	.10	.10	15
2825	1.0		.20	.30	18
2850	1.7		.25	.27	20

TRAQ INSTALLATION
(Also see diagrams one and two)

The minimum system configuration consists of one signal conversion channel (ADC), one controller, and 128K (256K for 4012P) of memory. A CAMAC crate is also required and usually a crate controller to allow the TRAQ system to communicate with a computer. (Only one crate controller is required for each CAMAC crate).

System interconnections are:

1) The memory modules are connected to the controller via a 50 pin flat cable. This cable plugs into the front panel TRAQBUS connectors. The memory modules usually reside to the left of the controller in the crate. This keeps the flat cable from interfering with the other controller signal cables. Traq systems are delivered with flat cables built for the system configuration ordered. If the system configuration is not specified, the cables will correspond to an equal distribution of ADC modules and memories.

During power-up diagnostics the 4012 will determine how much memory is on the bus. There must be at least 128K words (256k for the 4012P). The diagnostic routines will fail at the MEM1 test if no memory is found. Memory modules must have their I.D. switches set

so that one module has I.D.=0, another I.D.=1,etc, (see memory module sections). The modules can be located in any order in the crate relative to the 4012. The 50 pin flat cable connector should be as short as possible to reduce bus noise and crosstalk. Refer to the memory module sections and the diagnostic section of this manual for further information regarding memory configurations.

2) The digitizer modules are connected to the controller through a 40 pin flat cable at the rear of the modules. This cable is also built for the system configuration originally ordered. The digitizer modules are usually installed to the right of the controller in the crate. The first digitizer module must have its I.D. switch set to zero, the second to one, etc. The modules can be located in any order relative to the 4012. For DSP digitizers (ex: 2812 ,8 channel ADC), channel 1 will correspond to channel 1 of the module with I.D. switch set to zero; channel 9 will correspond to channel 1 of the module with I.D. switch set to 1,etc.

3) After installing the units in the crate and connecting the two flat cable connectors, turn on the crate power. The controller will now sequence through a set of diagnostics. If any problem is found the controller will display a 'FAIL' message at the current diagnostic. Refer to the diagnostic part of the controller section. Note: the 4012 is not able to check the connection to the digitizer units. This can be checked by setting NOC to the maximum number of channels and CLK1 to the maximum conversion rate. Depress the 'start' sampling switch and check that the 'CVT' and 'SEL' LEDs on the digitizer modules are on. Also the 'DACY' LEDs on the memory modules should be on. If more than one memory module is present the 'SEL' leds should be blinking on/off at a rate dependant on the sampling speed. If this fails check the cable interconnection between the controller and the digitizers.

4) A failed digitizer or memory can usually be determined without removing the interconnection cable. To locate a failed memory just change the I.D. to a number out of the contiguous memory address range (and the other memory I.D.s to fill in for the removed module), and repower the system. For example, consider a four module memory system where the third module is suspected to have failed:

Module # :	I.D. before:	I.D. after:
1	0	0
2	1	1
3	2	15
4	3	2

When the system is repowered the controller will find only 3 modules on the system (the controller assumes that an empty address space means the end of the memory chain). If the system is functional this implies that module 3 has failed.

The digitizers can be checked in the same fashion except that it is not necessary to repower the system. A failed digitizer can also be isolated by changing NOC. This will reduce the number of active channels and not address the modules with higher I.D.s.

5) When using the TRAQ system for transient recording there are several parameters that must be set carefully:

A) NOC (number of active ADC channels) must be equal to or less than the number of actual digitizer channels. The 4012 expects a 'handshake' signal from each channel when transferring data and if no channel is present the controller will wait indefinitely for the handshake.

B) CLK1 or CLK2 must not be greater than the maximum conversion speed of the channels or else erroneous data will be recorded. Also, the user must be careful not to select a combination of NOC and CLK1,CLK2 which exceeds the maximum TRAQBUS speed of 5 or 8 megasamples/second. I.E.:

CLK1 (FREQUENCY) <= (5 or 8 Mhz)/NOC
CLK2 (FREQUENCY) <= (5 or 8 Mhz)/NOC

Example: using 50 active channels of 2812 modules, each channel converting at 100 Khz gives:
5000 Khz / 50 = 100 Khz
which therefore does not exceed the maximum bus rate for 5 Mhz controllers/memories.

However:
52 channels at 100 Khz/channel gives:
5000 Khz / 52 = 96 Khz
which exceeds the maximum bus rate. If the clock rate is changed to 50 Khz then a maximum of 100 channels can be active.

C) Since the 4012 accommodates a large amount of memory/channel the user should be careful that 'stop triggers'are not generated before sufficient samples have been recorded or old and new data will be intermixed. This is especially true when PTS =0 (all pretrigger information). For example, consider using one active channel at 1Mhz (NOC=1, CLK1 = 1Mhz) and one megaword of memory. With these parameters it requires one second to sample all of memory. If PTS=0 and the 'stop trigger' is received 1/2 second after sampling begins the last 1/2 of memory is never written into and will contain old data. If PTS=8/8 there is no problem as all the data (and all of memory) will be recorded after the 'stop trigger' arrives.

ADDENDA TO SPECIFICATIONS

May 1987:
The following changes have been made for REV L10:

The 4012A and 4012P firmware have been merged into one PROM version consisting of two EPROM I.C.s located in sockets 1E & 2E on the 4012-02 board. This new version allows 4012P users to utilize commands that were only available for the 4012A.

Two new front panel control functions have been added:

1) MCAL- If YES then 128k samples are reserved for calibration memory. If NO then the entire memory is used to record data. This function was previously only available for the 4012P. MCAL can be set from either the front panel or CAMAC.
2) 4012- If P then the firmware assumes that the module is a 4012P; if A then a 4012A. 4012A users can now use the 5200 memory modules which have battery back-up of the data by using the '4012 P' setting .

An additional CAMAC command has been added to allow a complete memory dump (See 10 in WRITING THE 4012 CONTROL REGISTERS)

4012P users must be sure that '4012 P' has been saved in the non-volatile ram. On power-up the unit checks this control setting and aborts the memory diagnostics if '4012 P' is set, otherwise the data will be rewritten. The firmware also checks for a valid control setting; detection of an invalid control word forces a default setting to the '4012 A' mode but no memory diagnostics.

MODELS 4012, 4012A AND MODEL 4012P
TRAQ CONTROLLERS

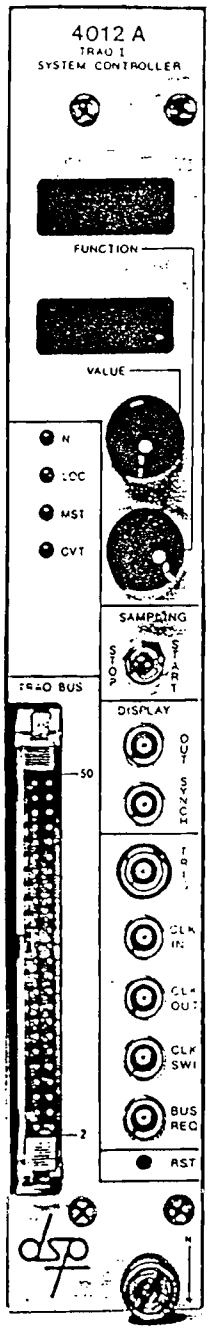
OPERATIONAL DESCRIPTION

GENERAL

The DSP models 4012, 4012A and 4012P TRAQ system controllers directs the flow of data between signal conversion units such as analog to digital converters (ADCs), scalers, etc. and memory storage units (models 5000,5001,5003,5004,5200). Up to 256 signal conversion channels can be controlled by one model 4012 with a maximum TRAQBUS transfer rate either 5 or 8 million samples per second. Up to 16 megasamples of 16 bit data can be stored in one TRAQ system.

As the number of active channels are decreased the 4012 will allocate more memory to each channel. Also the 4012 allows the user to increase the number of active channels (NOC) in increments of two (except for NOC=1), i.e. NOC can be 1, 2, 4, 6, 8, 10..256. The memory size (record size) allocated to each channel is controlled by the 4012 and depends on the number of active channels and the total memory size. The user may select record sizes from the maximum memory/channel allowed down to 1024 samples. Once data acquisition is initiated the memory is written into continuously until a 'stop trigger' is received which causes the controller to stop sampling after the correct number of post trigger samples have been recorded. The number of post-trigger samples is set in increments of 1/8 of the record size (0, 1/8, 2/8....8/8). The 'stop trigger'is either an external TTL signal, front panel switch, or computer command.

After completion of sampling, data is either displayed or read to the computer. The 4012 has an internal 12 bit digital to analog converter which allows the user to view a reconstructed analog waveform on an osscilo-scope. A trigger is also provided to synchro-nize the display. Data is displayed or read starting at the earliest sample recorded. The user can select which channel to view or read. The 4012 displays all of the recorded data however data can be read by the computer



starting at any 1K (1024) block.

Signal conversion units can either be DSP units such as models 2812, 2824, etc. or user supplied units. The interface timing between the 4012 and the signal conversion units is shown in diagram 3.

Two clock frequencies are available to accommodate switchable sampling rates and are controlled by either:

1. An external control signal 'CLK SWI' which turns on the first clock (CLK1) when the signal is at TTL low and the second clock (CLK2) when 'CLK SWI'is TTL high.

2. The 'TRIG' signal which causes the 4012 to start counting down the preset number of post-trigger samples. In this mode all pre-trigger samples are recorded using CLK1 and all post-trigger samples using CLK2.

The 4012 can also be clocked using an external user supplied signal. The sampling clock is also available to synchronize other controllers.

Model 4012 is designed to support multiple controllers on the TRAQBUS. After data transfer from the signal conversion units, the 4012 can relinquish control to allow another controller(s) to access and process data in the memory storage units. Control parameters stored in the 4012 are also available through the TRAQBUS to auxillary controllers.

All 4012 control parameters can be set from front panel switches and through CAMAC from a computer. These parameters are stored in nonvolatile memory and automatically reloaded on power-up. Also on power-up, the 4012 sequences through a series of diagnostics and signals the user if a problem is detected (see DIAGNOSTIC section).

Model 4012 uses a TI 9995 16 bit processor with program code stored in local EPROM. DSP provides support for the customization of the code for special user applications. This support includes source code for the TRAQ system firmware, a cross assembler for code development on an IBM XT/AT computer,and a special PROM to handle code down-loading to the 4012 over its RS-232 port for debugging.

4012A

The 4012A is an enhanced version of the 4012 which can transfer data at either 5 or 8 million samples/second. The rate is determined by which type of memory module is used and a jumper option on the 4012A-01 board. Models 5000 , 5003 and 5004 are five Mhz units while model 5200 is an eight Mhz unit. The five Mhz units will not run on 4012As set for eight Mhz transfer rates unless the jumper on the 4012A is selected for the slower rate. (see Calibration section). TRAQ systems are delivered with the rate adjusted to accommodate the memory module ordered with the system.

The 4012A has an improved circuit to accommodate the higher speed data transfers. This circuit also insures that the transfer cycle timing remains constant as more ADCs are added onto the bus. As a result old DSP ADC modules require slight modifications to run with 4012A or 4012P controllers (see the option section of the digitizer manual section). Check the side panel tag on the ADC modules to determine the type of ADC modules in the system. All 4012A / 4012P ADC compatible modules have an 'A' printed in the "OPTIONS" box on ADC side panel sticker.

4012P (also see 4012A, above)

The 4012P is a special version of the 4012. This system differs from the standard unit in that:

1) There is a 'LOCKOUT' signal which can force the 4012P to always be in the LOCAL control mode.

2) There are two signals which if received in the correct order will start the 4012 digitizing:
   a) 'MASTER ARM'
   b) 'MASTER ENABLED'

4) The 4012P records the memory address of the first sample digitized in its non-volatile memory chip. After power-up this address is restored and data can be displayed/read from the battery backed-up 5200 memory modules.

5) The 5200 memory modules used on the 4012P system have an input signal 'WRITE LOCK' which prohibit the 4012P from overwriting the memories.

An additional feature that was available only for the 4012P but with version 1.10 of the firwmare can also be used with the 4012A is:

1) A 128K sample section of memory can be reserved for calibration data. The 4012 will display a total memory size which is 128K less than on the TRAQBUS as this memory is reserved for calibration data only. When the unit is in the acquisition calibration mode, 'ACQ CAL',data is digitized as usual, however, after recording is complete the last 2048 samples of data for each channel are transferred to the reserved memory section (approximately 1/2 second is required to transfer data for each channel). The only time data is ever written into the reserved memory section is during this transfer time. The acquisition mode 'ACQ DATA' is the standard mode. Data can be read from both the calibration and data sections of memory depending which

acqusition mode is enabled. This feature requires a minimum memory size of 256K samples and can be enabled or disabled from the front panel (MCAL function) or by the computer.

SYSTEM DIAGNOSTICS

Whenever the 4012 microprocessor is reset, either by the front panel reset button or a CAMAC Z (or C) command a series of diagnostic tests are performed. Failure to pass any of these test indicates the system is not functional (refer to diagnostic test section).

After diagnostics are completed the signal conversion units can be checked by setting the number of channels (NOC) control, clock control (CLK1,CLKC,CKSW) and pushing the start sampling switch (the 4012 must be in local control mode). If the ADCs are properly connected the CVT (convert) LEDs will be on and also the memory modules' DACY (data cycle) LEDs . After pushing the stop sampling switch the CVT LEDs should go off after completion of post-trigger sampling. If the CVT LEDs are not on when sampling is initiated then:

1) Check the bus connection between the 4012 and the ADC units.

2) Check that the I.D. switches are set properly (Also refer to the 2812,2824 etc. sections).

3) Check that a clock is present (i.e. that CLKC = INT or if CLKC = EXT that an external clock signal is present)

4) Check that the clock rate is within the maximum sampling rate of the ADCs).

FRONT PANEL INDICATORS & CONTROLS:

ALPHANUMERIC LED INDICATORS:

The 4012 has two alphanumeric LED displays which are controlled by two corresponding rotary switches. The function switch selects a control to be set and the value switch selects the control parameter to be used. As the value switch is incremented/decremented the new values are used by the internal processor to set control registers. Once sampling is initiated the values are locked-in and changing the switch values will only affect the next shot. If the 4012 is in remote mode only the local/remote control and the display channel can be changed. When the 4012 is initialized by a CAMAC clear (Z or C) or the front panel reset a series of diagnostic tests are performed (see diagnostic section). If any of these tests fail, a 'FAIL' message will be displayed on the value LED with the corresponding test on the function LED. Failure to complete these tests indicates that the unit is not functional.

The following functions are settable from the front panel:

FUNCTION:	VALUE:	DESCRIPTION:
(4012P only)		
ACQ	DATA	The unit enabled to take data in the standard recording mode.
	CAL	The unit is enabled to take data for calibration recording. After calibration is complete the last 2048 samples for each channel are transferred to the reserved calibration memory.
CLKC	NONE	Both internal clocks(CLK1 & CLK2) and the external clock input are disabled.
	EXT	The external clock input is enabled and the internal clocks, CLK1 & CLK2, are disabled.
	INT	The internal clocks (CLK1 & CLK2) are enabled and the external clock input is disabled.
CKSW	NONE	Switching between CLK1 and CLK2 is disabled.
	FTRG	CLK1 is enabled when the SWI front panel input is TTL low. CLK2 is enabled when SWI is TTL high.

	STRG	CLK2 is enabled after receipt of a stop trigger. (All post-trigger samples are taken with CLK2) NOTE: CLK1 is the normal sampling clock. When CLK2 is active the 16th bit of the data is set to 1.
CLK1	5MHz-10Hz	Selects the sampling frequency for CLK1 NOTE: do not select a sampling speed greater than the maximum ADC conversion rate.
CLK2	5Mhz-10Hz	Selects the sampling frequency for CLK2 NOTE: 1) do not select a sampling speed greater than the maximum ADC conversion rate. 2) Whenever CLK2 is active the 16th bit (MSB) of the data is set to 1. (see DATA FORMAT section)
DISP	1..NOC	Displays recorded data from the selected channel. NOC (number of active channels) is selected by the NOC control. The display is active only after sampling is complete and if there is no CAMAC readout. All data is displayed except when NOC = 1 which displays every other data sample.
INCR	1,10,100	Selects the increment/decrement value used by some of the other functions such as MSCH.
MSCH	1...	Displays the memory/channel (record size) in 1k blocks. Changing the value switch will increment or decrement the memory/ channel by the amount selected in INTR. The minimum memory/channel is 1024 samples and the maximum is determined by the following algorithm: MSCH(MAX) = INTEGER(MSTO/NOC)

NOC = NUMBER OF ACTIVE CHANNELS
MSTO = TOTAL MEMORY SIZE

EXAMPLE: MSTO = 256k : NOC = 6
MSCH = INT(256k/6)
= 42k
NOTE: THE TOTAL MEMORY SIZE (MSTO) IS DETERMINED DURING THE POWER-UP TEST SEQUENCE.

MSTO	NOT ADJUSTABLE.	Displays the total memory size (1k blocks). The total memory size is determined during the power-up diagnostic test sequence.

Note: The 4012 will display 128K less memory for MSTO than actually present if enabled for calibration memory ('MCAL YES') since 128K is the required memory to store the calibration data.

MODE	LOCL	Local control- front panel controls are adjustable.
	RMOT	Remote control-front panel controls are not adjustable.

NOTE: The computer can override the LOCL control and change to RMOT. Also the front panel can override RMOT and change to LOCL. The display control is still settable in RMOT mode.

4012	A	Sets control firmware to run 4012A code.
	P	Sets control firmware to run 4012P code.

MCAL	NO	All TRAQ memory is used for data acquisition.
	YES	A 128K data block is reserved for calibration data.

NOC	1,2,4,6..256	Sets the number of active ADC channels.

NOC can be set from one to the total number of available ADC channels. Do not set NOC greater than the total number of available ADC channels.

PREV	xxx	Displays the current revision level of the microprocessor firmware. This message is only displayed after power-up diagnostics are completed.
PTS	0/8,1/8..8/8	Sets the number of post-trigger samples in 1/8 intervals. 0/8= all of the channel's data is recorded before the stop trigger. 1/8 = 1/8 of the channel's data will be recorded after the stop trigger,7/8 before. ..... 4/8 = 1/2 of the channel's data will be recorded after the stop trigger,1/2 before. ..... 8/8 = all of the channel's data will be recorded after the stop trigger.
SAVE	[blank] or DONE	Saves the control parameters in the non-volatile RAM memory. Turning the value switch one position forward or backwards causes the control parameters to be stored and the message 'DONE' to be displayed. On power-up the unit will use these settings for the control registers.

If on power-up the non-volatile RAM containing the control settings has incorrect settings, the 4012 will default to the following control values:

```
ACQ  :  DAT
CLKC :  INT
CKSW :  NONE
CLK1 :  100 khz
CLK2 :  100 khz
MSCH :  Full record size
4012 :  A
MCAL :  NO
MODE :  LOCAL
NOC  :  1
PTS  :  8/8
```

LED INDICATORS:

N	Momentary LED. On for approximately 1/2 sec when the 4012 is addressed by the CAMAC dataway.
MST	On when the 4012 is the TRAQ bus master. NOTE: Slave controllers are not supported in the present firmware.
LOC	On when the 4012 is in local mode/ off when in remote mode.
CVT	On when the 4012 is recording data.

SWITCH CONTROL:

START/STOP	Two position momentary switch. The 'START' position starts sampling, and the 'STOP' position generates a stop trigger (equivalent to the front panel input). The 4012 will initiate or reinitiate sampling any time 'START' sampling is depressed. After 'STOP' sampling is depressed, no further stop triggers will be acknowledged (until sampling is restarted.) This switch is not active in the remote mode.
RST	Resets the microprocessor and initiates the power-up diagnostic sequences.

SIGNALS:

(The following signals use LEMO ,single pin, coax connectors)

DISPLAY OUT	Analog output, approximately +/- 10 volts into 1Kohm minimum. Displays a reconstructed waveform of the recorded data. The channel to be displayed is controlled by the front panel switches or CAMAC. The display is 12 bits (4096 resolution) and will not display data points beyond the lower 12 bits of data (D11-D0). At the beginning of each sweep there is approximately a 100 usec. dead time during which no data is displayed. When there is only one active channel (NOC=1) every other data point is displayed (to minimize flicker). For all other cases all of the data is displayed.
SYNCH	TTL signal out, into 1Kohm minimum. The positive edge is synchronized to the beginning of the display sweep.

TRIG	Stop trigger which initiates post-trigger sampling. positive edge sensitive. After receipt of the first postive edge all further transitions are ignored until sampling is reinitiated. 4012: 1 Kohm input impedance, protected to +/- 100 volts for 10 msec, +/- 25 VDC. 4012A: Optically isolated, protected to 4012P: +/- 300 volts, requires approximately 1 ma. of current at 3 volts to activate.
CLK IN	External clock which initiates sampling of all active. ADC channels,positive edge sensitive, TTL, 1 Kohm impedance. The clock frequency may change arbitrarily but the user must insure glitch free transitions.
CLK OUT	TTL signal at the same frequency as the selected clock frequency (internal or external). Will drive one 50 ohm load.
CLK SWI	TTL signal causes sampling rate to change from clock 1 to clock 2 if enabled. 1 Kohm impedance, TTL low enables clock 1, TTL high enables clock 2.
BUS REQ	Priority bus control signal which is used to establish a TRAQBUS master/slave controller. Not implemented on the present software revision.

4012P SIGNALS (additional signals on the rear panel)

ARM	Optically isolated, TTL signal, protected to +/- 300 volts. A high TTL level must be detected by the 4012 followed by MASTER ENABLE before digitizing will be initiated. There should be at least a 100 usec. time delay between assertion of MASTER ARM and MASTER ENABLE. Requires approximately 1 ma. to activate at 3 volts.
MASTER ENABLE	Optically isolated, TTL signal, protected to +/- 300 volts. A high TTL level must be detected after assertion of MASTER ARM before digitizing will be initiated. Requires approximately 1 ma. to activate at 3 volts.
MASTER LOCKOUT	Optically isolated, TTL signal, protected to +/- 300 volts. A low TTL (or absence of) signal forces the 4012 into the local control mode. A high TTL level allows the remote control level to be activated. Requires approximately 1 ma. to activate at 3 volts.

(The following signals use multipin flat cable type connectors)

TRAQBUS	50 pin connector,TTL signals. 32 bits of multiplexed data/address and 12 control signals. Transfers data from the TRAQ controller to memory modules or slave controllers.
SIGNAL CONVERSION BUS	Rear panel,40 pin, connector,TTL levels. Transfers data from signal conversion units to the TRAQ controller.

CAMAC CONTROL:

The following list describes the response of the 4012 to the CAMAC dataway commands. All commands require N(station number) and return X=1 and Q=1 unless stated. (also see diagram I).

F(0)*A(0) -Read data from the requested command register (see READING the 4012 CONTROL REGISTERS, this section).

F(2)*A(0) -Read data for the selected channel number. Each F(2)*A(0) command reads one data sample and increments Traq memory to read the next sample. Data transfer rates up to the maximum CAMAC rates. Before data readout can proceed the correct CAMAC commands must be issued.

F(3)*A(0) -Read module I.D. ("4012")

F(8)*A(0) -Returns Q=1 if the internal LAM is on, regardless if the LAM was enabled by F(26)*A(0) or not.

F(9)*A(0) -Start sampling.(Only in remote control mode). There is, approximately, a 500usec delay from receipt of the F(9)*A(0) command to the actual start of sampling.

F(10)*A(0) -Reset LAM.Turns the internal and external(Camac dataway) LAM off.

F(16)*A(0) -RESERVED.

F(17)*A(0) -Selects a command register for reading/writing. (see WRITING the 4012 CONTROL REGISTERS, this section).

F(24)*A(0) -Disables the LAM (look-at-me) signal from the CAMAC dataway. However the internal status can be monitored by the F(8)*A(0) command (Q=1 returned if the internal LAM is on).

F(25)*A(0) -Stop sampling (equivalent to then front panel 'stop trigger'). NOTE: the 4012 will respond to this command in both local and remote control modes.

F(26)*A(0) -Enables the internal LAM (look-at-me) signal onto the CAMAC dataway.

Z/C -initializes the 4012,resets the microprocessor,and starts power-up diagnostics. NOTE: the 4012 will respond to this command in both local and remote control modes.

LAM - LAM, look-at-me is generated when sampling is complete and when data is ready for readout (if in remote mode.)

PROGRAMMING THE 4012 CONTROL REGISTERS

Control registers are programmed using the F(17)*A(0) command and W16-W1 CAMAC write lines. W16-W13 address the control registers and W12-W1 contain the data to be loaded.

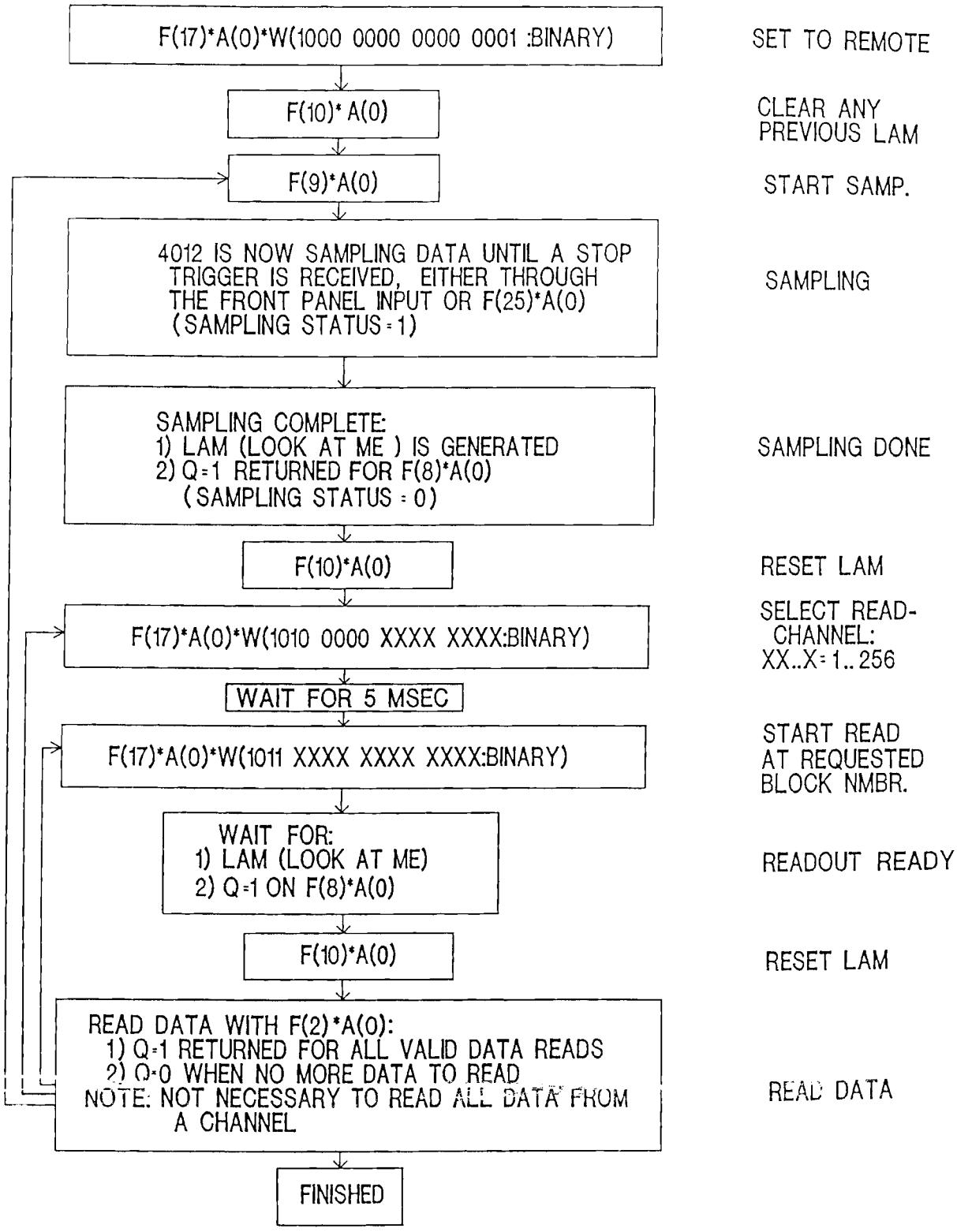
If the 4012 is in the local control mode only the local/remote (see 8 below) register can be changed. After commanding the unit to the remote mode all registers can be changed. As new values are programmed into the 4012, the new values/functions are displayed on the front panel LEDs.

Since all command registers are read/written through the microprocessor there is a response time of approximately 100 to 500 usec. The 4012 will respond with a Q=1 on F17*A(0) [F(0)*A(0)] if the unit is ready to accept (read) the command (data), otherwise a Q=0 is generated. When reading the control registers, which requires F(17)*A(0) to be followed by F(0)*A(0), both commands must be executed before the next F(17)*A(0) can be generated. **It is recommended that a minimum of 500 usec. delay be inserted between all commands which address the 4012 control registers.** This applies for F (17), F(0), and F(9) commands.

See Diagram 4.

DIAGRAM 4

CONTROLLING SAMPLING AND DATA READOUT FROM CAMAC



WRITING THE 4012 CONTROL REGISTERS
(F(17)*A(0)*W(W16..W1) COMMAND)

CMD W16 W15 W14 W13: (BINARY)	COMMAND REGISTER :	W12 -- W1: (DECIMAL)
1) 0 0 0 1 (HEX 0)	SET NUMBER OF ACTIVE CHANNELS (1,2,4,6,8,10 ....256)	1=1 active ch. 2=2 active ch. : : 256=256active ch.

[NOTE: Do not program more active channels than the total number of ADC channels, otherwise the 4012 will always be waiting for a 'conversion complete' signal from the erroneous channels]

---

2) 0 0 1 0 (HEX 2)

SET THE NUMBER OF POST-TRIGGER SAMPLES. 0,1,2,...8

0 = No post-trigger samples -sampling stops immediately after receipt of the 'stop trigger'.
1 = 1/8 of the channels memory is sampled after receipt of 'stop trigger'
2 = 2/8 of the channels memory is .....
3 = 3/8.....
8 = all data is recorded after receipt of 'stop trigger'

---

3) 0 0 1 1 (HEX 3)

SET THE MEMORY/CHANNEL IN 1K (1024) INCREMENTS. 1...

The minimum memory/channel is 1K and the maximum is determined by the number of active channels(NOC) and the total memory size.

Maximum memory/channel = NOC * integer(MSTO/NOC)
where
NOC = NUMBER OF ACTIVE CHANNELS (1,2,4,6...256)
MSTO = TOTAL MEMORY SIZE (128K,256,...)
MSTO is determined during the power-up diagnostic sequence.

The 4012 will default to the maximum memory/channel for any value out of bounds.

4) 0 1 0 0 (HEX 4)	SET CLK1 FREQUENCY (CLK1 is enabled for sampling unless SWI(front panel) is TTL high [FTRG] or a 'stop trg' has been detected [STRG] - then CLK2 will be active)	0 = 5MHz: 1 = 2MHz 2 = 1MHz: 3 =500KHz 4 =200KHz: 5 =100KHz 6 = 50KHz: 7 = 20KHz 8 = 10KHz: 9 = 5KHz 10 = 2KHz: 11 = 1KHz 12 =500 Hz: 13 =200 Hz 14 =100 Hz: 15 = 50 Hz 16 = 20 Hz: 17 = 10 Hz	
5) 0 1 0 1 (HEX 5)	SET CLK2 FREQUENCY [The W16 data bit is set to 1 for data sampled when CLK2 is active- see DATA FORMAT section]	(SAME AS SET CLK1)	

[NOTE: Do not set CLK1,2 frequencies higher than the maximum conversion rate of the ADC modules or the maximum transfer rate of the bus]

6) 0 1 1 0 (HEX 6)	SET CLOCK SWITCHING CONTROL REGISTER	0 =NO SWITCHING FROM CLOCK 1 TO CLOCK 2 1 =SWITCH FROM CLOCK 1 TO CLOCK 2 WHEN THE FRONT PANEL SIGNAL 'SWI' IS HIGH [FTRG]. 2 =SWITCH FROM CLOCK 1 TO CLOCK 2 WHEN 'STOP TRG' RECEIVED. [STRG]
7) 0 1 1 1 (HEX 7)	SET CLOCK CONTROL REGISTER	0 =BOTH EXTERNAL AND INTERNAL CLOCKING ARE DISABLED. 1 =THE EXTERNAL CLOCK ,FRONT PANEL INPUT, SIGNAL IS ENABLED. INTERNAL CLOCKS ARE DISABLED. 2 =INTERNAL CLOCKS 1,2 ARE ENABLED AND THE EXTERNAL CLOCK INPUT IS DISABLED.

8) 1 0 0 0 (HEX 8) — SET LOCAL/REMOTE CONTROL REGISTER — 0 =SET TO LOCAL CONTROL MODE; 1 =SET TO REMOTE CONTROL MODE

[NOTE: if the 4012 is in the local control mode the computer may override and set to remote mode. This is required in order to set any other control registers or read data. Also, the LOCAL/REMOTE can be changed from the front panel]

---

9) 1 0 0 1 (HEX 9) — SET THE DISPLAY CHANNEL. — 1,2,3,4,5.....256

Displays data from the selected channel, (see 'DISPLAY OUT',SIGNALS section).

[NOTE: Do not program a display channel greater then the number of active channels. If the 4012 is in the CAMAC readout mode then display can be reactivated by reading out the last block of data in a channel until Q=0 is returned on the 1025th read cycle.]

---

10) 1 0 1 0 (HEX A) — SELECT A CHANNEL FOR READOUT. — 1,2,3,4,5.....256

DATA STREAMOUT 512

DATA STREAMOUT WITH AUTO-RESTART 513

MEMORY DUMP 514

[NOTE: This command must be executed at least once before data readout can begin. It is not necessary to re-issue the command if the channel readout number is not changed. Do not program a channel number greater than the active number of channels.]

Data Streamout: If the channel number = 512 then the 4012 will immediately enter the data streamout mode. Data is ready to read approximately 1.5 msec after issuing the command. This mode is useful for users who wish to read all TRAQ data without the overhead of setting up each channel and starting address (app. 3 msec). This mode reads data out in the following the following sequence:

Channel(NOC), Sample(1)
Channel(NOC-1), Sample(1)
. .

```
Channel(1),      Sample(1)
Channel(NOC),    Sample(2)
Channel(NOC-1),  Sample(2)
      .               .
Channel(1),      Sample(2)
          etc.
```

Data Streamout with Auto-restart: This mode allows the 4012 to continuously sample/read/sample... data. After the 4012 is commanded into this mode it will automatically enter the data readout mode after sampling is complete. The data is read in the same format as above. After the last data sample + 1 is read the 4012 will automatically restart sampling. This mode is enabled until the channel readout number is changed from 513.

Data Dump: The entire memory is readout starting at address 0.

---

11) 1 0 1 1 (HEX B) START DATA READOUT AT REQUESTED ADDRESS. ADDRESS IS SELECTABLE IN 1K BLOCK INCREMENTS. 0,1,2.....N-1

0= Start readout at earliest sample digitized
1 = " " " " " " +1024
2 = " " " " " " +2048
. = ...
N-1 = " " " the last 1K memory block
(N= MEMORY/CHANNEL ,1K BLOCKS)

[NOTE: The 4012 will not respond to this command unless the unit is both in the remote mode and sampling is complete. Data readout will start approximately 500 usec. after receipt of this command. A LAM will be generated when data is ready for readout.
The LAM should be reset ,F(10)*A(0) before readout begins. A Q=1 on F(2)*A(0) will be generated for valid read data. A Q=0 on F(2)*A(0) will be generated after all data from the selected channel has been read. Also, the 4012 will be in the display mode (front panel 'DISPLAY OUT' active) until this command is received and will return to the display mode after the last 1K block of data has been read from the channel. It is not necessary to read all data from the channel before reading another channel or skipping to some other 1K data block. SEE Diagram 4.]

---

12)	1	1	0	0	ACQUISITION MODE = DATA	1
	(HEX C)				ACQUISITION MODE = CALIBRATE	2
					ARM UNIT (4012P)	4
					STOP SAMPLING	8
					RUN 4012A CODE	16
					RUN 4012P CODE	32
					ENABLE CALIBRATION MEMORY	64
					DISABLE CALIBRATION MEMORY	128

Note:
1) Acquisition mode = data is the standard transient capture mode and is the default on power-up.
2) Acquisition mode = calibrate will transfer 2k samples/ channel to the reserved memory after data is acquired.
3) Arm is the computer equivalent of the front panel MASTER ARM and must be (if in remote mode) before the 4012 will accept the F(9) command start digitizing.
4) Stop Sampling - This command will cause the 4012 to stop sampling immediately. The 4012 will execute the following:
   a) The internal or external clock is immediately stopped.
   b) The 4012 waits approximately 100 usec after disabling the clocks to allow all ADC converters to finish converting data.
   c) The number of post-trigger samples is read by the 4012 proccessor.

      If there have been no post-trigger samples (no stop trigger) then the earliest sample digitized is assumed to reside at the beginning of memory. The total number of samples converted is equal to the memory address of the last sample stored.

      Note: This will not be true if the memory address counters have wrapped around one time. It is advisable to use the forced stop mode only in all post-trigger mode. The user should be sure that a trigger is recieved before issuing this command.

      If a stop trigger was received the total number of samples converted is equal to the number of programmed pre-trigger samples plus the number of post-trigger samples actually converted.
   d) The number of samples converted is stored in registers for readout. (see w=16, w=17 under READING THE 4012 CONTROL REGISTERS)
   e) If no post-trigger samples were recorded then a flag bit is stored to notify the user that no stop trigger was received. (see w=14 under READING THE 4012 CONTROL REGISTERS)

5) Run 4012A code assumes the unit is a 4012A controller, 4012P a 4012P controller.

6) Enable/disable calibration memory reserves a 128K memory block for the calibration data.

---

13) 1 1 0 1 (HEX C) SAVE CONTROL REGISTERS. 0

All registers are saved in the non-volatile memory and used as control parameters on power-up. The 4012 contains a XYCOR non-volatile memory chip. The chip will retain the control parameters indefinitely but has a limited number of SAVE cycles (approximately 1000).

---

14) 1 1 1 0 (HEX E) RESTORE CONTROL REGISTERS. 0

Restores the control registers using the values stored in non-volatile memory. This is done automatically on power-up.

15)	1	1	1	1	INITIATE POWER-UP DIAGNOSTIC TESTS	0
	(HEX F)					

Allow approximately 3 seconds to execute. This test will reset the system (same as power-up). Also for the 4012P this test will exercise the memories and write over old data.

READING THE 4012 CONTROL REGISTERS
(F(0)*A(0)*R(R16..R1) COMMAND)

Control registers can be read at any time, either in remote or local control mode. The registers are read using a two step command process:

1) Address the register with F(17)*A(0)*W(register address) which causes the TRAQ processor to fetch the register data.

2) Read the register data with F(0)*A(0)*R(register data).

If the TRAQ processor is available to accept the F(17)*A(0) command, a Q=1 will be returned. The data to be read will be available within 500 usec and should be read by the F(0)*A(0) command within 1 sec after F(17)*A(0). The 4012 will not respond for one second to any other CAMAC command while waiting for F(0)*A(0) to read the control register.

F(17)*A(0)*W(W16..W1) (DECIMAL)		F(0)*A(0)*R(DATA) (DECIMAL)
W = 1	READ NUMBER OF ACTIVE SIGNAL CHANNELS (SEE CMD 1, previous section)	R = 1,2,4,...256
W = 2	READ POST-TRIGGER SAMPLES (SEE CMD 2, previous section)	R = 0,1,2,.....8
W = 3	READ MEMORY/CHANNEL (SEE CMD 3, previous section)	R = 1.....
W = 4	READ CLOCK 1 FREQUENCY (SEE CMD 4, previous section)	R = 0,1,2,....17
W = 5	READ CLOCK 2 FREQUENCY (SEE CMD 5, previous section)	R = 0,1,2,....17
W = 6	READ CLOCK SWITCH. REG. (SEE CMD 6, previous section)	R = 0,1,2
W = 7	READ CLOCK CONTROL REG. (SEE CMD 7, previous section)	R = 0,1,2
W = 8	READ LOCAL/REMOTE STATUS (SEE CMD 8, previous section)	R = 0,1
W = 9	READ DISPLAY CHANNEL (SEE CMD 9, previous section)	R = 1,2,3,4..256
W = 10	READ DATA CHANNEL TO BE READ (SEE CMD 10, previous section)	R = 1,2,3,4..256

W = 11 READ START ADDR OF DATA R = 0,1,2,3...N-1
(1K DATA BLOCKS)
(SEE CMD 11, previous section)

W = 12 READ TOTAL MEMORY SIZE R = 128,256..4096
AVAILABLE (1K BLOCKS)
128 = 128K WORDS
256 = 256K WORDS,ETC.

W = 13 RESERVED

W = 14 READ STATUS

	(binary) R8	R7	R6	R5	R4	R3	R2	R1
4012 not sampling	x	x	x	x	x	x	x	0
4012 sampling	x	x	x	x	x	x	x	1
Data acquisition mode	x	x	x	x	x	x	0	x
Calibration acquisition mode	x	x	x	x	x	x	1	x
4012P not master armed	x	x	x	x	x	0	x	x
4012P master armed	x	x	x	x	x	1	x	x
4012P not master enabled	x	x	x	x	0	x	x	x
4012P master enabled	x	x	x	x	1	x	x	x
Stop trigger received before EOC	x	x	x	0	x	x	x	x
Stop trigger not received before EOC	x	x	x	1	x	x	x	x
4012P not triggered	x	x	0	x	x	x	x	x
4012P triggered	x	x	1	x	x	x	x	x
4012A code running	x	0	x	x	x	x	x	x
4012P code running	x	1	x	x	x	x	x	x
Calibration memory not enabled	0	x	x	x	x	x	x	x
Calibration memory enabled	1	x	x	x	x	x	x	x

[Note: 1) The 4012 will turn the LAM on when sampling is complete in the remote mode.
2) In calibration mode the 4012 will store 2k/samples per channel in the reserved calibration section of memory after data acquisition.]
3) Stop trigger received before EOC: This status flag should be monitored when using the Stop Sampling Command. See 12) under Writing the 4012 CONTROL REGISTERS.

W = 16	READ NUMBER OF SAMPLES CONVERTED,LOWER WORD	R16-R1
W = 17	READ NUMBER OF SAMPLES CONVERTED,UPPER WORD	R16-R1

Read the total number of samples converted. This command is used when sampling has been forced to stop (see 12), WRITING THE 4012 CONTROL REGISTERS). Returns the TOTAL number of samples converted:

TOTAL samples converted = NOC * samples

therefore if 1000 samples have been taken and Number Of Channels = 6 then the total samples converted is 6000.

TOTAL samples converted =
65536 * (UPPER WORD) + LOWER WORD

NOTE: TOTAL samples converted can be greater than (record length * NOC) if no stop trigger was received and the samples converted are greater than the record length.

DIAGNOSTICS

During the power-up sequence the TRAQ microprocessor runs aseries of diagnostic tests. Failure to pass these tests implies the system is not functional. If a test does not pass a message will be displayed on the 'value' LED display while the 'function' LED displays the test being performed. For most of the test, the controller will continually loop through the failed test to facilitate oscilloscope probing of the failed circuitry. To restart the testing sequence hit the reset button or issue CAMAC Z(or C) commands. The tests are performed sequentially as listed below. Note: In the following discussions the 4012-01 board is on the left side (as viewed from the front) and the 4012-02 (processor board) is the board on the right. The 4012-03 is the front panel board. Also, 4012P units do not use the MEM2 and MEM4 tests as stored data would be erased after power-up.

TEST: NO DISPLAY (OR RANDOM DISPLAY)
MESSAGE: NO DISPLAY "
DESC: Either the 4012-02 board has no +6V power, the 4012-03 is not connected to the 4012-02 or there is some failure on the 4012-02 (such as a bad PROM,RAM,etc) that is inhibiting the processor from initializing.
CHECK: 4012-02 and 4012-03 connections, 4012-02 fuses. Or generate repetitve CAMAC Z(or C) cycles and probe the T.I. 9995 address/data lines for correct logic states. Immediately after reset the processor will access the RAM memory (starting at location A000,hex)-check for memory access signals.

TEST: 'RAM'
MESS: 'FAIL'
SCH: 4012-02 Sheet 3
DESC: The processor writes an alternating 1010.. and 0101.. pattern into the onboard static RAM and attempts to read it back.
CHK: Failure implies a bad RAM or non-functioning CPU board. The test will continually loop through the read/write sequence at the failed address. Check the address and data lines.

TEST: 'INTP'
MESS: 'FAIL'
SCH: 4012-02 Sheet
DESC: The processor sets-up the 9519 interrupt control chip, fires interrupt #7 (internally) and checks the 9519's interrupt status register for interrupt #7.

CHK: Failure implies either a bad 9519 I.C. or bad connections to the chip. Since a message is being displayed,the processor and associated bus circuitry are probably O.K. Probe pin 1 of 1L (9519) for chip select. Also, check for wr(write) and rd(read).

TEST: 'L646'
MESS: 'FAIL'
SCH: 4012-01 Sheet 3
DESC: This is the first test that checks the board interconnection, the state of the 4012-01 board and the TRAQBUS. The processor loads a pattern (AAAA 5555 ,hex) into the LS646s (6H-9H) on the 4012-01 board and then reads the pattern back.
CHK:
1) Remove the cable from the 50pin TRAQBUS connector and restart the test. If the test passes, the problem is either a bad TRAQBUS cable or a bad memory module which is generating data on the bus when not addressed.
2) Check all fuses on the 4012-01 board and the interconnection cable between the 4012-01 and 4012-02.
3) If the test still fails, this indicates a component failure on the 4012-01 or 4012-02 board. The 4012-01 has three data busses:
   1) A 32 bit data bus (IB31-IB0); main data bus
   2) A 16 bit data bus (MD15-MD0); CAMAC data bus
   3) A 8 bit data bus (PD7-PD0) ; u-processor data bus

   Communication between the microprocessor the the IB bus is through the CAMAC MD bus; i.e.
   u-processor - CAMAC - data bus
   For the 'L646' test the test pattern (AAAA 5555) is loaded as:
   1) Byte 4: AA(hex) loaded into LS646,6H : IB31-IB24
   2) 3: AA LS646,7H : IB23-IB16
   3) 2: 55 LS646,8H : IB15-IB8
   4) 1: 55 LS646,9H : IB7 -IB0

   The data bytes are written/read to/from the LS646's in the following manner:
   1) Byte 4: AA(hex):LS645(7B)-LS645(5B)- LS646(6H)
   2) Byte 3: AA(hex):LS645(8B)-LS645(7D)- LS646(7H)
   3) Byte 2: 55(hex):LS645(7B)-LS645(6B)- LS646(8H)
   4) Byte 1: 55(hex):LS645(8B)-LS645(8D)- LS646(9H)

After data bytes are latched into the LS646 B latches they are transferred to the A latches and then read back through the same data paths. Any problems on the TRAQBUS will show up during the LS646 B to A transfer. To check the data in the LS646 latches, trigger a scope on pin 9H(1),the signal which transfers the data in the latches. Check 6H(4 to 11),7H(4-11),etc. for the AAAA

5555 pattern. Failure of the pattern at this point implies either bad signal levels on the PD,MD, or IB bus, defective I.C.s or bad enable,latch signals to the data path chips.

TEST: 'LPTS'
MESS: 'FAIL'
SCH: 4012-01, Sheet 3
DESC: Loads a 24 bit pattern (AA 5555,hex) into the 24 bit PTS counter composed of LS593s (9D,6C,6D) and reads the pattern back.
CHK: Since the 'L646' test passed the data bus, connections between the 4012-01 and 4012-02 board are o.k. Also, the IB ,MD, and PD bus are o.k. The transfer of data bytes to/from the microprocessor is the same as the 'L646' test except data is latched into the PTS counters not the LS646s. Data bytes are loaded into the LS593 storage latches by strobing the LOPTS1,LOPTS2,and LOPTS3 lines. Data is then transferred to the internal eight bit counters of the LS593s by strobing the LO-DMA-CNT line (pin 9). Data is then read when RD-PTS-CNT line goes low (3 times to read 3 bytes). Failure of this test may be due to a bad LS593 or bad strobe,latch lines.

TEST: 'ADDR'
MESS: 'FAIL'
SCH: 4012-01 Sheet 4
DESC: Loads a 24 bit test pattern (AA 5555) into the 24bit address counter composed of LS593s (5D, 5C), LS374s (8E,3D), LS645 (9E) and adders (6E,7E). The circuitry composed of 9C, 8E, 6E, 7E and 3D enable the address counter to auto-skip address' in increments of 1 to 255 under hardware control only. It is used to readout the data for display or CAMAC. The upper two pattern bytes (AA 55 ,hex) are loaded directly into 5D and 5C using the LOADR2 and LOADR3 strobe lines. See 'L646' test for the description of the data byte transfer to/from the microprocessor. The lowest data byte, 55 hex, is loaded indirectly into the LS374(8E). through the adders 6E and 7E. When the LS645(9E) is enabled for data transfer from IB(7-0) to A(7-0), the outputs of 3D are tri-stated and pulled to TTL high. The carry-in of adder 7E also goes high which adds 256 to the requested address. The carry out of the adders is not used in the direct load mode resulting in the original IB(7-0) data bits being strobed into latch 8E. After this, a RST strobe is generated to transfer data from the LS593 registers to the internal 8bit counters. Data is then read back from the address counters.
CHK: The previous tests have checked the IB and other data

busses. Therefore, any problems are probably associated with either the address counter I.C.s or the enable,latch signals. Check that inputs from 3D are high when data is latched into 8E, and that 55 hex is loaded.

TEST: 'ADIN'
MESS: 'FAIL'
SCH: 4012-01, Sheet 4
DESC: Loads a 1 into the address counters,increments the address counters 8 times and reads the resulting address back. Then repeats the test starting at address FF (hex), and then address FFFF (hex). LS374(3D) is set to 1 which will increment register 8E each address cycle. See 'ADDR' test.
CHK: Failure of this test usually implies a problem with I.C. 3D, which auto-increments the address or possibly adders 6E & 7E. Also check 5F(S27) for the correct strobe lines.

TEST: 'ADAU'
MESS: 'FAIL'
SCH: 4012-01 Sheet 4
DESC: Loads zero into the address counters,128 into the auto-skip register 3D and checks for correct auto-incrementing of the address counters after generating address strobes. The test is performed 32 times (addresses 0 to 4096, in increments of 128). The addresses are read and checked after each of the 32 address strobes.
CHK: Since test 'ADDR' has passed, this test should only fail due to a faulty auto-increment register (3D) or faulty overflow logic from counters 5C and 5D.

TEST: 'ADOV'
MESS: 'FAIL'
SCH: 4012-01, Sheet 4
DESC: Loads FF FFFE (hex) into the address counters, increments two times and checks for overflow reset (address =0). The address overflow counter, 4B, is used to reset the memory modules' internal address counters to zero after the end of memory has been reached during writing or reading. This counter is incremented each time counter 5D increments (counts in 64K increments) and reaches its' terminal count when the memory space is exhausted. The overflow from 4B triggers 1G(LS74) to generate approximately a 50nsec. reset pulse, which resets the 4012 and memory module internal address counters. On the first address cycle the addresses

increment to FF FFFF,hex, and the next address cycle causes the overflow to reset the address counters and reload 4B.

CHK: Since the address counters have passed the three previous tests, any problems should be associated only with 4B or 1G. Check for 1G(11) toggling and, approximately, a 50nsec. pulse at 1G(8,9).

TEST: 'PTIN'
MESS: 'FAIL'
SCH: 4012-01, Sheet 1
DESC: Loads a 1 into the PTS counters, increments the counters 8 times and reads back the data. Repeats the same test starting with an initial count of FF and FFFF (hex).
CHK: Since the 'LPTS' test passed this test should only fail due to an LS593 counter or bad increment logic between the LS593s.

TEST: 'PTOV'
MESS: 'FAIL'
SCH: 4012-01, Sheet 1 and 2
DESC: Loads FF FFFE (hex) into the PTS counters, increments one time and checks for interrupt #3 on. When the PTS counters. reach the terminal count of FF FFFF(hex), the DMARCO goes low which turn on 2C (LS74), which in turn generates interrupt #3 to the 4012-02 board.
CHK: Since the PTS counters have passed the 'LPTS' and 'PTIN' tests the only problems should be due to faulty overflow circuitry or 2C not toggling.

TEST: 'MEM1'
MESS: 'FAIL'
SCH: 4012-01 and memory modules
DESC: This is is the first test for the memory modules. At this point all of the 4012-01 diagnostics have passed. This test performs the following functions:

1) Determines how much memory is on the TRAQ bus.
2) Checks that interrupt #6 in generated when the memory module returns the DARDY signal.

The 4012 assumes that there is at least 128K words of memory on the bus and will fail the test if no memory module responds with a DARDY, when address FFFF (hex) is addressed. The modules are organized as 32 bit words and each modules' internal address counters range from FFFF-0000,hex. This is equivalent to 64K,32bit words or

128K of 16 bits words. The test proceeds as:

1) Address 0000 FFFF is loaded into the memory modules.
2) A data cycle (DACYC) is generated.
3) The processor looks for interrupt #6 on.
4) If interrupt #6 is not on after the first DACYC, the test fails as either no memory is present or there are logic problems. If interrupt #6 is on, the address is incremented by 64K (i.e. to 1 FFFF, hex) and loaded into the memory module, which generates a DACYC. This continues unless a DARDY is not returned signifying no more memory is present.

CHK: Check the I.D. switches on the memory modules. One of the units must have I.D.=0. Also check the TRAQ bus cable. If the test still fails, set another module on the bus to I.D.=0 (set the original modules' I.D. = 7) and rerun the test.If the test now passes, the original module was faulty. If the test still fails, probe the DARDY signal on the 4012, sheet 2. DARDY is an open collector signal so if any module is faulty, the line could be held down.

TEST: 'MEM2' (except 4012P)
MESS: 'FAIL'
SCH: memory modules
DESC: This test writes the address of the first word in each 32bit,64k memory block on the TRAQ bus. I.E. the word at location 0000 is loaded with 0000 and then checked. The word at address 1 0000 (hex) is loaded with 1 0000 and then checked,..etc. This is a very rough memory test to quickly see if there are any gross memory failures. This test will usually pickup any bad memory chips that are totally failing.
CHK: Check which memory module has it SEL LED on. This is where the failure is occurring. Probe the datalines (synchronizing with DARDY to locate the bad memory chip).

TEST: 'MEM4'
MESS: '0' '1' '2' .....
SCH: memory module
DESC: This is the final diagnostic test and tests all the memory on the TRAQ bus in 1k block increments. Data is written into memory using the address counters in the 4012-01. A 1 Mhz clock is used to write the data. After the memory block is written, the processor reads and checks every 64th memory location. If the test fails, the processor will remain in a loop writing/reading at the block that failed. The value displayed on the LEDs

is the block being tested.

CHK: Check that the 1 Mhz clock is working. If no clock is present, check the clock circuitry on the 4012-02 board. Otherwise, check the module for faulty logic or a bad memory locations.

FUNCTIONAL DESCRIPTION

The 4012 consists of three printed circuit boards:

1) 4012-02 which contains the microprocessor,clock circuitry,CAMAC control interface, and non-real time controls for the TRAQ bus.
2) 4012-03, a small front panel board, which contains the LED displays,and control switches.
3) 4012-01 which controls all real time data flow between the signal conversion units,the memory storage units and CAMAC data readout.

The following discussion assumes the reader has enough electronics background to troubleshoot the 4012. Most troubleshootingshould be done using the power-up diagnostics, however, there are possible logic failures that will not be detected.

(NOTE: refer to the 4012 schematics)

4012-02 Sheet 1

This sheet shows the interface logic to the front panel 4012-03 board and CAMAC.

LS640(5L) and LS08(6L)

These I.C.s are the main interface to the front panel 'FUNCTION' and 'VALUE' switches. The two switches are infinitely rotating (i.e.- the number of functions/values are not limited by the number of switch positions). The processor continually scans the encoded positions of the switches and looks for an increment/decrement to the next position. As soon as a change of position is detected, the processor enters an algorithm to debounce the contacts.

LS01 (5K 4,5,6)

This gate generates an interrupt whenever the front panel 'start/stop' switch is depressed. Once interrupted the processor reads which switch was hit (either MD0 or MD1).

LS642 (9A,10A)

These two I.C.s put the TRAQ I.D.(4012) on the CAMAC bus when F(3) is received.

LS642(9C,10C),LS374(9E,10E)

The two latches are used to hold data for CAMAC readout. R1-R8 data is held in 10E and latched be CAMLALO and 9E,latched by CAMLAUP holds R9-R16.

LS534 (7A,8A)

These two latches hold and invert data from W16-W1 for the

processor to read. The data word is read one byte at a time.

The remaining logic on this page is used for CAMAC controls. The controls are decoded using two PROMs (4A,5A) to generate commands. The logic at the lower right of the page generates Q response for F(17) and F(0) commands. When the processor is ready to receive an F(17) command or data is available for readout with F(0), the processor sets 5C(9) high using CAMQST. On the next CAMAC command, regardless if it's F(17) or F(0), the leading edge of N will set 4D(8) low. If this command is an F(17) or F(0), a Q=1 is returned and the Q logic reset.

4012-02 Sheet 2

This sheet contains the logic control for the CLK1, CLK2 and other logic. Crystal oscillator 10G supplies the main time base both for the clock circuitry and the processor. I.C.s 8K and 10H (LS390) divide the clock down to 10 Mhz and 10Khz. I.C. 7H (S151) is a multiplexer which selects either the 10Mhz or 10Khz time base. CLK1 frequency is programmed by register 6F (LS374) which loads counters 7G,6G,5G (LS160) and divides down the time base. CLK2 is switched in by disabling 6F and enabling 5F.

4012-02 Sheet 3

This page shows the microprocessor control section of the TRAQ system. The 4012 uses a T.I. 9995 16 bit processor. It has a byte wide data path but all internal registers are 16 bit. There is 64K of address space. The schematic shows the address' allocated to most of the memory,PROM and other devices. I.C. 1E is an 8 X 8K PROM which contains the TRAQ code. I.C. 1C is an 8 X 2K RAM used to store variables and can be changed to an 8 X 8K RAM for field upgrade. Locations 1E and 2E are reserved for future code development or memory storage (16K bytes).

The system memory map is:

MEMORY ADDRESS:	USED FOR:
0000-1FFF	PROM CODE
A000-BFFF	PROM CODE OR RAM (FUTURE)
C000-DFFF	RAM STORAGE
E000-FFFF	PROM CODE OR RAM (FUTURE)
6000-603F	NON-VOLATILE RAM STORAGE
8000	INTERRUPT CONTROL CHIP
2000-5FFF	TRAQ CONTROL

XYCOR (1L)

This I.C. stores control parameters and is composed of both a normal RAM (64 bytes) and a non-volatile RAM. On power-up the AR line is strobed which moves the contents of the non-volatile RAM into the standard RAM. The 4012 loads a check pattern into the XYCOR chip and after power-up diagnostics, checks the pattern for data integrity.If the result is correct, the XYCOR contents are used for control parameters and if incorrect, a default set is used. The standard RAM is stored in the non-volatile RAM by strobing the ST input. There is special gating on this line, using the one-shot at 5H to gate spurious signals from loading false data into the chip.

AM9519 (1L)
The AM9519 is an interrupt control chip which generates an interrupt signal (GINT) to the processor whenever an interrupt (IN0-IN7) occurs. The chip contains internal registers to enable/disable interrupts and record the interrupt states.
LS645 (3L,2L,2K) These I.C.s buffer data and control signals to the 4012-01 board.

TMS9902 (3D), AM26LS32 (3C), AMLS30 (5D)
These I.C.s form the RS232 port interface for the processor.

4012-01 Sheet 1

The 4012-01 board controls all real time data flow between the signal conversion units, the memory modules, and CAMAC. There are four busses on this board:

1) 32 bit IB(31-0) bus
2) 16 bit MD(15-0) bus
3) 8 bit PD(7-0) bus

The IB bus is used for the main data and address flow. Data from the signal conversion module comes in at 4C,3A (LS374) and 3C,4A (LS645). Data from the signal conversion units is 16 bits wide and is converted to 32 bits by the LS374s, which form a one word buffer. The second word is transferred directly onto the IB bus by the LS645s and then both words are simultaneously latched into the LS646s.

The LS646s are the data/address interface to the TRAQ bus. These devices are capable of latching data on both the A and B inputs. Also data may flow directly through. The processor controls the setup of the LS646s according to the operations required. When the system is sampling,data is latched into the B inputs and outputted through A. When the system is reading data which requires address cycles to be generated (if NOC>1), addresses are generated from the address logic(sheet 4) and flow transparently through the B side of the LS646s. The resulting data from the memory modules is latched into the A side of the LS646s and read to CAMAC through buffers 5B,7D,6B,8D,7A,and 8A. However, when data is being displayed, the A side of the LS646s is transparent and data is latched into 7C and 8C for display.

5B,7D,6B and 8D multiplex data to/from the 32 bit IB bus to the 16 bit MD bus. The MD bus talks to CAMAC and multiplexes to the 8 bit processor bus through 7B and 8B.

9D,6C, and 6D form a 24 bit counter which is used to count post-trigger samples, when sampling, and the number of samples to read/display, when sampling is completed. The counter uses LS593s which internally are composed of both an eight bit register and eight bit counter. The processor loads the complement of the number of counts into the LS593 registers one byte at a time. This number is then loaded into the counters whenever the LO-DMA_CNT goes low. When the counter overflows, an interrupt is generated to the processor to tell it that sampling/reading/displaying is finished.

8C,7C and 9C form the display circuit. 8C and 7C (LS174s) latch data, which comes through the LS646s and enabled buffers. 9C (AM 6012) is a 12 bit D/A converter with current outputs. 9B (NE531) converts the current outputs to voltage. The output range is +/- 10 volts.

4012-01 Sheet 2

This sheet shows the random logic used to control the TRAQ bus and associated logic. 1A,1C,2E and 2D form the main interface to

the signal conversion units, generating timing signals for the memory modules. The SAM-CLK signal is generated from the 4012-02 board and passed to the signal conversion units to initiate conversions. When data is available, the signal conversion unit responds with DAAV (Data Available) low, which is gated through 2E (LS51),toggling 2D. 2D will fire one-shot 1D every other DAAV which in turn loads two data words into the memory modules (by generating a data cycle -DACYC). DAAV also fires the one-shot at 1C which controls a 125 nsec. or 200 nsec. data transfer cycle from signal conversion units to the 4012 and into the memory modules. Since the speed of the memory RAMs is either 250ns or 400ns/cycle (32 bit), data cannot be transferred out of the signal conversion units faster than 125ns or 200ns (16 bit). The logic composed of 2D,1D and 1C gates off the refresh to the memories. On the positive edge of the sampling clock, 1C will turn on for 50 nsec., clear the one-shot at 1D and turn 2D off which in turn disables the refresh. Refresh will be reenabled 10 usec later when 1D turns off, unless a DAAV is received which retriggers the device. As long as DAAVs appear within 10 usec, of the sampling clock, the refresh will stay off. This is only required if data is to be transferred at the maximum bus rate of one sample/200 nsec. The logic will handle all devices which convert within 10 usec from receipt of the sampling clock and are readout (DAAV-DAACPT) faster than 5usec/sample. If the signal conversion units have a conversion time greater than 10 usec then the one-shot at 1C must be set to 400nsec. or greater.

The logic at the lower left is used for slave-controllers and the control firmware is not implemented in the present software revision..

The logic on the right side of the sheet is used to multiplex signals to the LS646s. 4F(LS32) allows the processor to latch data individually into the the LS646s. Multiplexer, 3F (LS157) enables 2D to latch data during the sampling sequence. The logic composed of 1E and 1F is used during readout. When NOC=1, then both the upper and lower 16 bit data word in the memory modules contains information for channel 1. (In all other modes ,NOC= 2,4,6,...256, even channels are stored in the lower 16 bit word and odd channels in the upper word). When data is read from the memory, the two words are latched simultaneously into the LS646s. This logic is used to toggle one word and the next word from the LS646s onto the CAMAC dataway. For NOC=1, addresses are not generated for readout since data is stored sequentially in the memory. If NOC>1, then an address cycle is generated for every read/displaycycle and the logic at 1E,1F is disabled.

4012-01 Sheet 3

This page contains control registers and strobe generators for the processor to direct data flow on the 4012-01. 3G,4G and 4D (LS259) generate strobe pulses to various logic circuits. The numbers shown on the schematic in parentheses are the processor addresses for the signal. 3E and 4E (LS374) enable and disable data paths. The circuitry at 6G (PROM), and 5H form a decoding

device used to enable/disable special data paths. If the DYNAMIC signal at 4E(2) is on, then the data paths are only enabled when the processor addresses them. However if DYNAMIC is low, the paths are always enabled as addressed by the contents of 5H (LS373).
This is used during sampling/displaying or reading when the processor is not actively involved in data transfers.

4012-01 Sheet 4

The logic composed of 1B(LS640), 2B(LS593) and 3B(LS645) generates the channel number of the data being transferred from the signal conversion unit to the 4012. The processor loads the complement of NOC, number of active channels, into 2B through 3B. 2B counts up to 255 and then reloads itself. The inverter,1B, buffers the address on the signal conversion bus. The 4012 sequentially reads the data from the signal conversion units starting at the highest active channels decrementing to channel zero.

The remaining logic is used for address counting and generation. I.C.s 5D,5C (LS593) form the upper 16 bits of the 24 bit address counter. 8E & 3D (LS374),9E(LS645),6E & 7E (LS283) form the lower 8 bits. See the diagnostic section of this manual for the description of the circuit. When data is being loaded into the memories, this address counter is synchronized with the memory address counters. The processor reads this counter at the end of sampling to figure out where the last sample is located in memory. I.C. 4B (LS593) is a memory overflow counter and resets the memory address counters to zero when memory space is exhausted. During readout the address counter generates address cycle to fetch data. Data in the memory modules is stored sequentially. I.E.

ADDRESS: 0	SAMPLE 1 CHANNEL 1	SAMPLE 1 CHANNEL 2
1	1	3	1	4
2	.	.	.	.
.	1	NOC-1	1	NOC

During readout the 4012 must read data sequentially from the same channel. This requires that the logic skip certain address depending on the number of active channels. Since CAMAC readout can proceed at a 1Mhz rate, this is too fast for the processor to keep up with and requires hardware auto skip on the address logic.

CALIBRATION

ADJUSTING THE 4012A OR 4012P FOR 5/8 MHz OPERATION

(Refer to 4012A-01 schematic, sheet 2 and the 4012A-01 assembly drawing and Diagram 3).

1. 8MHz operation:

   A. Remove the jumper (E9) between R9 and R2.
   B. Install the jumper (E8) between R21 and R2
   C. Connect the 4012 to a memory and at least two ADC channels.
   D. Power up the 4012 and set NOC to at least 2 with CLK1 set to the maximum allowable sampling rate.
   E. Start sampling.
   F. Trigger an oscilliscope with the 'clock out' signal from the 4012.
   G. Connect an oscilliscope probe to 1A(10) on the 4012A-01 board. This is the DAACPT signal and you should see a burst of pulses for each clock pulse from the 4012. The number of DAACPT pulses corresponds to the number of channels converting. Adjust 21 to space the DAACPT pulses 110-115ns apart.

2. 5 MHz operation:

   A. Remove the E9 jumper and install the E8 jumper.
   B. Follow (B-G) above except adjust R2 for 190-195 ns timing for DAACPT pulses.

OPTIONS

CLK2 BIT SET:

The 4012 is normally delivered with the 16th data bit set to the CLK2 status detect line. Whenever CLK2 is active the 16th bit of the data will be set to one. This option can be defeated by removing the jumper or the 4012-01 board (left side) from E1 to E3 and installing a jumper from E1 to E2. This allows the 16th data bit from the signal channels to be stored in memory.

INSTALLATION OF TRAQ FIRMWARE

Firmware for the 4012 is programmed into two 64k EPROMs which can be field upgraded by installing new EPROM chips into the control board*. Occasionally DSP may send out new revisions of this software. To install the new EPROMs place the unit on a table with the front panel facing you and:

1) Remove the backpanel and open the unit (it may be necessary to remove the right side panel).
2) Remove the 28 pin integrated circuits in sockets E1 and E2* which are located at the top of the right side printed circuit board. The I.C. will have a revision number on it such as REV 1.10. Be sure to note the orientation which has pin 1 facing the rear of the module.
3) Install the new EPROMs in the same sockets with the same orientation.
4) Close the unit and remount the rear panel.
5) Install the unit in the crate and turn the power on. After diagnostics are complete the new revision number should be displayed.
6) If the unit does not power-up properly check for bent pins or incorrect installation of the EPROMs.

*Note that revision levels prior to Rev.1.10 required only one EPROM chip

MODEL 5000
256k MEMORY
MODULE

OPERATIONAL DESCRIPTION

GENERAL

Model 5000 is a 256K sample memory module which stores data from the TRAQ 4012 controller or other TRAQ processors. Memory in the unit is organized as 32bit words. The 5000 can write/read data at a maximum rate of 5.0 Megasamples/second (a sample is a 16 bit data word).

All communication with the module is through the front panel TRAQBUS connector; the CAMAC connector supplies power only. The TRAQBUS is a multiplexed 24 bit addrress/32 bit data bus with the ability to write/read data up to 8.0 Megasamples/second. The memory consists of 200nsec, 64k dynamic RAMS with on board refresh control.

FRONT PANEL INDICATORS & CONTROLS

LED INDICATORS:

ADCY — Momentary LED. Inidicates that an address cycle has been generated.

DACY — Momentary LED. Indicates that a data cycle has been generated.

RFCY — Momentary LED. Indicates that memory refresh cycles are being generated.

RFEN — Indicates that refresh cycles are enabled.

[NOTE: RFCY & RFEN should be on when the 5000 is not connected to the TRAQBUS]

WRITE — Indicates that the module is enabled for writing data to memory (when the LED is on) or reading to the 4012 (when the LED is off).

SEL — Indicates that the module is selected for reading/writing. Only one 5000 module is selected at a time.

ID2-ID0 — Indicates the position of the module I.D. switches.

TERM — Indicates that bus termination is installed (not normally used).

MODULE I.D. SWITCHES:

ID2,ID1,ID0 — Three switches which set the module identification number. The I.D. LEDs are on when the switch is in the 'on' position. Up to eight 5000 modules can be installed on the TRAQ bus and these switches determine which module will be 'module 0','module 1', etc. The I.D. switches must be set so that one module has I.D. zero, one module I.D. one, ...(up to the number of installed modules -1).

Module I.D.	switch settings: ID2	ID1	ID0	Use this setting if:
0	off	off	off	one or more modules are installed
1	off	off	on	two " " " " "
3	off	on	off	three " " " " "
3	off	on	on	four " " " " "
4	on	off	off	five " " " " "

Module I.D.	switch settings: ID2	ID1	ID0	Use this setting if:
5	on	off	on	six " " " " "
6	on	on	off	seven " " " "
7	on	on	on	eight modules are installed

Modules can be placed anywhere in the crate (relative to the 4012),regardless of I.D. number. Anytime modules are added to the TRAQ system or I.D. numbers changed, the 4012 should be reset or repowered to initiate diagnostics.

TRAQ BUS 50 pin connector to interface to the TRAQ bus.

FUNCTIONAL DESCRIPTION

[Refer to schematics, Sheet 1 and 2]

SHEET 1:

This sheet contains all of the control logic for the unit. Timing is generated from a 40Mhz crystal which is divided down to 20Mhz to generate two synchronous clocks (1P 5,6). Timing circuitry composed of S112s (2P,1S) and S174(2U) generate the RAS,CAS timing to read,write and refresh the memories.

When the RFSHEN on the TRAQ bus is high the unit is enabled to refresh the dynamic memories. The RC oscillator at 1V is set to refresh at a 10-20 Khz rate. The positive going edge of the clock initiates a refresh cycle. Refresh is disabled during high speed data transfers since the data transfer itself refreshes the memory. The eight bit LS593 generates refresh addresses.

If the READ line is enabled, address cycles load an address from the TRAQBUS into the address counters and then readout data. The trailing edge of ADDCYC initiates the read cycle. DARPY is generated when data is ready from the read cycle. (the 4012 uses the trailing edge of DARPY to latch data). If the INC (pin 36,TRAQ bus) is enabled, then the address counters increment at the end of the cycle.

Data cycles are similar to address cycles except that no address is loaded. If INC is enabled, the address counters are incremented. DACYC is used to load data at high rates. The TRAQ controller sets the initial address using ADDCYC. After this addresses are generated internally in the 5000. If the data rate is high enough, the 4012 will turn off the refresh enable line.

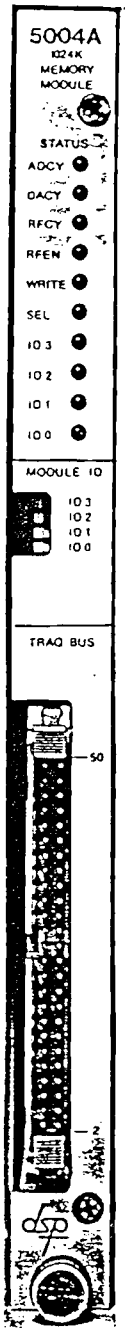
SHEET 2:

This sheet shows the data/address interface to the TRAQ bus. I.C.s 7AB,7AC,6AB,6AC are bidirectional buffers which receive data/addresses for loading and transmit data to the 4012 for reading. All lines on the TRAQ bus have optional A.C. termination. This is not normally used unless long cable lengths are desired between the 4012 and 5000 modules.

MODELS 5003 (512K) and 5004 (1024K)
MEMORY MODULES

OPERATIONAL DESCRIPTION

GENERAL



Models 5003/5004 are 512K/ 1024K sample memory modules which stores data from the TRAQ 4012 controller or other TRAQ processors.

Memory in the units is organized as 32bit words. The units can write/read data at a maximum rate of 5.0 Megasamples/second (a sample is a 16 bit data word). A maximum of 16 modules can be daisy chained on the TRAQBUS to give a maximum capacity of 8 Megasamples for the 5003 and 16 Megasamples for the 5004.

All communication with the module is through the front panel TRAQBUS connector; the CAMAC connector supplies power only. The TRAQBUS is a multiplexed 24 bit address/32 bit data bus with the ability to write/read data up to 8.0 Megasamples/second. The memory consists of 150 nsec, 256k dynamic RAMS with on board refresh control.

FRONT PANEL INDICATORS & CONTROLS

LED INDICATORS:

ADCY — Momentary LED. Inidicates that an address cycle has been generated.

DACY — Momentary LED. Indicates that a data cycle has been generated.

RFCY — Momentary LED. Indicates that memory refresh cycles are being generated.

RFEN — Indicates that refresh cycles are enabled.

[NOTE: RFCY & RFEN should be on when the module is not connected to the TRAQBUS]

WRITE — Indicates that the module is enabled for writing data to memory (when the LED is on) or reading to the 4012 (when the LED is off).

SEL — Indicates that the module is selected for reading/writing. Only one memory module is selected at a time.

ID3-ID0 — Indicates the position of the module I.D. switches.

MODULE I.D. SWITCHES:

ID3,ID2, ID1,ID0 — Four switches which set the module identification number. The I.D. LEDs are on when the switch is in the 'on' position. Up to 16 memory modules can be installed on the TRAQBUS and these switches determine which module will be 'module 0','module 1', etc. The I.D. switches must be set so that one module has I.D. zero, one module I.D. one, ...(up to the number of installed modules -1).

Module switch settings:

Module I.D.	ID3	ID2	ID1	ID0	Use this setting if:
0	off	off	off	off	one or more modules are installed
1	off	off	off	on	two " " " " "
3	off	off	on	off	three " " " " "
3	off	off	on	on	four " " " " "
4	off	on	off	off	five " " " " "
5	off	on	off	on	six " " " " "
6	off	on	on	off	seven " " " " "
7	off	on	on	on	eight modules are installed
.					
.					
15	on	on	on	on	sixteen modules are installed

Modules can be placed anywhere in the crate (relative to the 4012),regardless of I.D. number. Anytime modules are added to the TRAQ system or I.D. numbers changed, the 4012 should be reset or repowered to initiate diagnostics.

TRAQ BUS — 50 pin connector to interface to the TRAQBUS.

FUNCTIONAL DESCRIPTION

[Refer to schematics, Sheet 1 and 2]

SHEET 1:

This sheet contains all of the control logic for the unit. Timing is generated from a 20Mhz crystal which clocks a programmable logic chip (PAL). This chip (2S) controls all the memory control lines, RAS, CAS , etc. and arbitrates between refresh and data cycles.

When the RFSHEN on the TRAQ bus is high the unit is enabled to refresh the dynamic memories. The RC oscillator at 2R is set to refresh at a 100 Khz rate. The positive going edge of the clock initiates a refresh cycle. Refresh is disabled during high speed data transfers since the data transfer itself refreshes the memory. If the READ line is enabled, address cycles load an address from the TRAQBUS into the address counters and then readout data. The trailing edge of ADDCYC initiates the read cycle. DARPY is generated when data is ready from the read cycle. (the 4012 uses the trailing edge of DARPY to latch data). If the INC (pin 36,TRAQ BUS) is enabled, then the address counters increment at the end of the cycle.

Data cycles are similar to address cycles except that no address is loaded. If INC is enabled the address counters are incremented. DACYC is used to load data at high rates. The TRAQ controller sets the initial address using ADDCYC. After this addresses are generated internally in the module. If the data rate is high enough, the 4012 will turn off the refresh enable line.

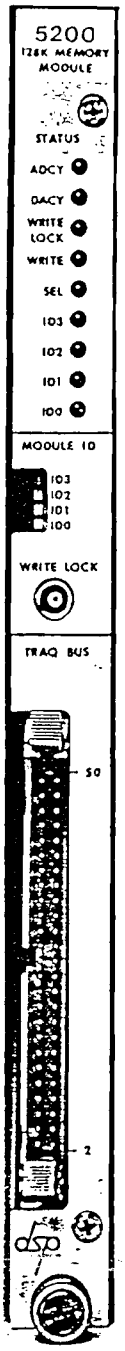
SHEET 2:

This sheet shows the data/address interface to the TRAQBUS. I.C.s 6V,6U,5V,5U are bidirectional buffers which receive data/addresses for loading and transmit data to the 4012 for reading.

MODEL 5200
128k MEMORY
MODULE

OPERATIONAL DESCRIPTION

GENERAL



DSP model 5200 is a 256k byte (128k sample) memory module which stores data from the TRAQ 4012 controller or other TRAQ processors with a maximum transfer rate of 8 megasamples/ second (each sample is a 16 bit data word). Memory in the unit is organized as one 64K block of 32 bit words (each data transfer consists of two samples, i.e. two, 16 bit words).

Up to sixteen 5200 modules can be daisy chained together on the TRAQBUS to give a maximum memory size of 2 Megasample. Each 5200 module contains its own Ni-Cad recharge-able battery for data retention. Data should be maintained for a minimum of one year under battery power. The Ni-Cad battery is in the recharge mode whenever CAMAC power is on.The 5200 also contains special signals (WRITE LOCK) which can be used to protect the memory contents from being overwritten.

All communication with the module is through the front panel TRAQBUS connector; the CAMAC connector supplies power only. The TRAQBUS is a multiplexed 24 bit address / 32 bit data bus with the ability to write/read data at a 4.0 Mhz word (32 bit) rate (8 Mhz sample rate). The memory consists of 32, 150 nsec, 64k static RAMS with battery backup for one year of data retention.

FRONT PANEL INDICATORS & CONTROLS

LED INDICATORS:

ADCY	Momentary LED. Inidicates that an address cycle has been generated.
DACY	Momentary LED. Indicates that a data cycle has been generated.
WRITE LOCK	Indicates that the memory cannot be over-written. (See Write Lock input signal below).
WRITE	Indicates that the module is enabled for writing data to memory (when the LED is on) or reading to the 4012 (when the LED is off). Note: Write Lock overrides this signal. Memory is only written into if the Write LED is on and the Write Lock LED is off.
SEL	Indicates that the module is selected for reading/writing. Only one 5200 module is selected at a time.
ID3-ID0	Indicates the position of the module I.D. switches. (see below)

MODULE I.D. SWITCHES:

ID3,ID2,ID1 ID0 — Four switches which set the module identification number. The I.D. LEDs are on when the switch is in he 'on' position. Up to sixteen 5200 modules can be installed on the TRAQBUS and these switches determine which module will be 'module 0','module 1', etc. The I.D. switches must be set so that one module has I.D. zero, one module I.D. one, ...(up to the number of installed modules -1).

Module switch settings:

Module I.D.	ID3	ID2	ID1	ID0	Use this setting if:
0	off	off	off	off	one or more modules are installed
1	off	off	off	on	two " " " " "
3	off	off	on	off	three " " " "
3	off	off	on	on	four " " " " "
4	off	on	off	off	five " " " " "
5	off	on	off	on	six " " " " "
6	off	on	on	off	seven " " " "
7	off	on	on	on	eight modules are installed
.					
15	on	on	on	on	sixteen modules are installed

Modules can be placed anywhere in the crate (relative to the 4012),regardless of I.D. number. Anytime modules are added to the TRAQ system or I.D. numbers changed, the 4012 should be reset or repowered to initiate diagnostics.

SIGNALS

WRITE LOCK — TTL signal, LEMO type input connector, internally pulled-up to 5 volts by a 10 Kohm resistor. Whenever the Write Lock input signal (WLIS) is driven to a TTL low, the 5200 memory cannot be overwritten with new data. WLIS is also connected to the TRAQBUS so that all 5200 modules will be write locked simultaneously. (Note: The actual WLIS input impedance is therefore 10Kohms divided by the number of 5200 modules on the TRAQBUS.) When power is applied to the 5200 an internal signal generates a write lock. As the 4012 starts its power-up diagnostics it will reset the internal write lock unless the WLIS signal is present. The presence of the WLIS will always prohibit overwriting the memory.

TRAQ BUS — 50 pin flat cable type connector which interfaces the 5200 to the TRAQBUS.

FUNCTIONAL DESCRIPTION

Refer to schematics, Sheet 1 , 2 and 3]

SHEET 1

This sheet contains all of the control logic for the unit. Timing is generated from a 40Mhz crystal. Timing circuitry composed of S74 (2L) and S174,S175(2K,1K) generate the timing to read and write memories.

Address cycles (ADCY) load an address from the TRAQBUS into the address counters and then readout data if the READ line is enabled. The trailing edge of ADDCYC initiates the read cycle. DARPY is generated when data is ready from the read cycle. (the 4012 uses the trailing edge of DARPY to latch data). If the INC (pin 36,TRAQ bus) is enabled, then the address counters increment at the end of the cycle.

Data cycles (DACY) are similar to address cycles except that no address is loaded. If INC is enabled, the address counters are incremented. DACY is used to load data at high rates. The TRAQ controller sets the initial address using ADDCYC. After this, addresses are generated internally in the 5200. The 5200 has a power-up write lock circuit composed of HC74 (3K) and components (CR10, C4, and R4). On power-up pin 9 of 3K should always be low. This will protect data in the 5200 until the 4012 issues a RST command. Write lock can also be generated by an external signal. If present, this signal is transmitted on the TRAQBUS to other 5200s.

SHEET 2 and SHEET 3

These sheets show the data/address interface to the TRAQBUS. I.C.s 5M, 5N, 6M, 6N are bidirectional buffers which receive data/addresses for loading and transmit data to the 4012 for reading. Also shown is the battery backup and recharging circuit.

TRAQ DIGITIZER MODULES

TRAQ data acquisition is performed by modular Analog-to-Digital Convertors (ADCs). These modules include the 8 channel, 100KHz DSP 2812, 2825, 2860 and the DSP 2824, a 12bit 2MHz ADC. Multiple modules may be connected to form a multichannel (256 maximum) system. Features common to all DSP data acquisition modules are:

1) High Resolution
2) Simultaneous Sampling
3) Fully Independent Channels
4) Modularity

Each channel is fully independent, incorporating an individual fully differential amplifier, track and hold, and ADC. This allows any or all channels to be used simultaneously at a constant data acquisition rate.

TRAQ DIGITIZER MODULE SPECIFICATIONS

SPECIFICATION		2812	2814	2825	2860	2824	UNITS
Number of Channels		8	4	4	4	1	Module
RESOLUTION		12	14	12	12	12	Bits
INPUTS							
Voltage Range				+/-5			Volts
Impedance		100		100	100	100	kOhms
Bandwidth	(0.5dB)	100K	100K	200K	500K	1M	Hz
	(3dB)	200K	100M	250K	1M	2M	Hz
CMRR	(dc-100Hz)	72	80	72	72	72	dB
CMVR				+/- 12			Volts
Protection (dc)				+/- 50			Volts
Type				Differential			
ACCURACY (DC)							
Gain Error				+/- 0.1			%
Offset Error				+/- 0.1			%of FS
Integral Non-Linearity				+/- 0.5			LSB
Differential Non-Linearity				1			LSB
SAMPLING RATE		100K	100K	250K	1M	2M	Hz
APERTURE DELAY				<25			NSec
CHANNEL-CHANNEL SKEW				<100			NSec
POWER REQUIREMENTS							
+24 Volts		0.15	0.25	0.25	0.25	0.1	Amps/Module
+ 6 Volts		1.5	1.7	1.7	1.7	1.0	Amps/Module
- 6 Volts		0.55	0.0	0.0	0.0	0.7	Amps/Module
-24 Volts		0.15	0.27	0.7	0.27	0.1	Amps/Module
Power Consumption		2.4	5.0	5.0	5.0	15.0	Watts/Chan
TEMPERATURE RANGE							
Specifications				10 - 55			Celsius
Storage				-5 - 85			Celsius

FRONT PANEL DESCRIPTION

The front panel of a TRAQ Data Acquisition module is divided into 3 functional areas:

STATUS

MODULE ID

SIGNAL INPUT

ADC MODULE FRONT PANEL

STATUS — Acquisition status and module identification (address).

CNVT — Indicates module is performing analog to digital conversions. The indicator will appear to be continuously on for sampling rates greater than 10 samples per second.

SEL — Indicates module is currently selected for data transfer from the internal data buffer. The indicator will appear to be continuously on for rates greater than 10 samples per second.

ID3I . . ID0 — Indicates module identification number (module address) as determined by MODULE ID switches.

MODULE ID — Determines Module ID (module address) as used in conjunction with the 4012 controller. Up to 16 modules may be configured in a single system.

ID	ID3	ID2	ID1	ID0	
00	0	0	0	0	First Module
01	0	0	0	1	Second Module
.	.	.	.	.	.
15	1	1	1	1	Final Module

INPUT — Input signal connections to each of four channels. Connector mates with:

LEMO - F0.302 NYL U/3.7 or equivalent.

BIPOLAR/UNIPOLAR INPUT OPTION

Two signal input modes are available on each ADC channel. These are:

MODE	MAXIMUM INPUT	MINIMUM INPUT	0Volt CODE
BIPOLAR*	+4.998	-5.00	2048
UNIPOLAR	+4.998	0.00	0

*Factory setting

Independent mode selection is available for each channel. Selection is made via jumpers within the module. Refer to the MODULE INFORMATION section of the manual for their locations.

CONTROLLER OPTION

The data acquisition modules must be configured for the applicable controller to which they will be attached. The options are:

MODE	TRAQ CONTROLLER
I	DSP 4012
II	DSP 4012A, DSP 4012P

Refer to the MODULE INFORMATION section for the option installation instructions.

MODULE I.D. SWITCH SETTINGS:

Data Acquisition module IDs must be set according to the following rules:

i/.

Module ID	Switch Settings				Channel Numbers			
	ID3	ID2	ID1	ID0	2812	2825	2850	2824
0	0	0	0	0	1-8	1-4	1-4	1
1	0	0	0	1	8-16	5-8	5-8	2
.	.	.	.	.		....		
15	1	1	1	1	120-128	60-64	60-64	16

ii/. A module with an ID = 0 must be present in the system.

iii/. Module IDs must be contiguous (i.e. no gaps in channel numbers are allowed).

iv/. Module IDs must be unique (i.e. no modules with identical channel numbers are allowed).

Note that the physical placement of modules on the TRAQ bus is not restricted.

The module ID is defined by the 4 front panel binary coded switches.

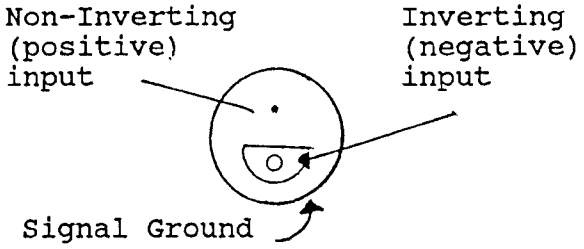
SIGNAL CONNECTION

Each ADC channel has a high impedance, wide bandwidth differential amplifier input.

Connector compatibility

LEMO RA0.302NYL dual pin connector
mates with LEMO F0.302NYLU/3.7

Pinout



2812M

AMP 204731-1 w/ 205172-8 Female Pins
mates with AMP 204744-1 w/ 203816-3

CHANNEL	+IN	-IN	SIG GND
1	1A	2A	1B
2	1C	2C	2B
3	4A	5A	4B
4	4C	5C	5B
5	8A	9A	8B
6	8C	9C	9B
7	11A	12A	11B
8	11C	12C	12B

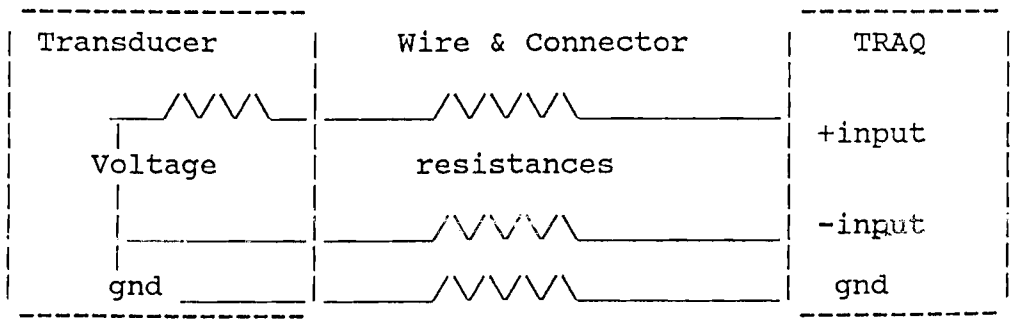
In order to maintain signal quality and, therefore, digitizer accuracy , certain signal conditioning procedures must be observed when connecting the TRAQ system to a signal source.

1. Use differential connections for analog signals. If the source is single ended, connect one side of the differential pair to the source ground. (Figure 1).

2. Use twisted pair shielded cables.

3. Shield all analog signals to minimize interchannel coupling and noise pickup. Ground all shields at a single, common ground to avoid ground loops.

4. Use low impedance sources, cabling, and connections. The DSP ADCs can resolve a voltage change of 0.005 volts. The signal source impedance, as measured at the TRAQ channel input, must be less than 200 Ohms in order to maintain system accuracy.



DATA ACQUISITION MODULE SPECIFIC INFORMATION

The following sections describe in detail each of the TRAQ Data Acquisition modules. This includes information on selecting available options, calibration procedures and technical descriptions.

MODEL 2812 12BIT / 100KHz / 8 CHANNEL ADC

OPTIONS

UNIPOLAR/BIPOLAR SIGNAL INPUT

To select BIPOLAR input option, install jumper at position labelled "B1" adjacent to the AD7572 component at the desired channel.

To select UNIPOLAR input option, install jumper at position labelled "UNI" adjacent to the AD7572 component.

CALIBRATION AND ALIGNMENT

Each channel of the DSP 2812 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left hand side cover. Drawing 2812A-01-AD indicates the location of each channel and the adjustments for each.

BIPOLAR MODE CALIBRATION

1. Set channel to bipolar mode according to section 3.1.

2. Set digitizer sampling clock to 100KHz.

3. Connect +ve channel input to gnd.
   Connect -ve channel input to gnd.

4. Digitize and average over 10 data samples.
   Adjust R21 for averaged reading of 2048.

5. Connect +ve channel input to gnd.
   Connect -ve channel input to +4.900 volt reference.

6. Digitize and average over 10 data samples.
   Adjust R22 for averaged reading of 41.

7. Connect +ve channel input to +4.900 volt reference.
   Connect -ve channel input to +4.900 volt refrence.

8. Digitize and average over 10 data samples.
   Adjust R25 for averaged reading of 2048.

UNIPOLAR MODE

1. Perform BIPOLAR MODE calibration first.

2. Set channel to unipolar mode according to section 3.1.

3. Set digitizer sampling clock to 100KHz.

4. Connect +ve channel input to +5.000 volt reference.
   Connect -ve channel input to gnd.

5. Digitize and average over 10 data samples.
   Adjust R21 for averaged reading of 2048.

COMMON MODE REJECTION

1. Set channel to bipolar mode according to section 3.1.

2. Connect +ve channel input to 10 v pk-pk 25 KHz sinewave.

3. Digitize and display reconstructed data.
   Adjust R25 for minimum amplitude display.

MODEL 2824 12BIT / 2MHz / 1 CHANNEL ADC

OPTIONS

CALIBRATION AND ALIGNMENT

Access to the DSP 2824 gain, offset, and common-mode rejection adjustments is achieved by removing the left hand side cover. Drawing 2824-01-AD indicates the locations of these adjustments.

BIPOLAR MODE CALIBRATION

1. Connect both inputs of the unit under test to system ground. Adjust R30 until the digital data from the unit under test reads 2048 (decimal).

2. Connect the noninverting input of the unit under test to the precision DC source. Set the source output voltage to 4.974 volts. Adjust R9 until the digital data from the unit under test reads 4085.

3. Repeat step 1. If no adjustment is necessary, continue to step 4; otherwise repeat steps 1 and 2 until there is no change when step 1 is repeated.

4. Connect both inputs of the unit under test to the precision voltage source. Adjust R10 until the digital data from the unit under test reads 204B.

UNIPOLAR MODE CALIBRATION

1. Select BIPOLAR MODE and perform BIPOLAR MODE calibration.

2. Select UNIPOLAR MODE.

3. Connect both non-inverting and inverting inputs to ground. Adjust R30 until a digital reading of between 0 and 1 is recorded.

MODEL 2825 12 BIT / 250 KHz / 4 CHANNEL ADC

OPTIONS

UNIPOLAR/BIPOLAR SIGNAL INPUT

To select BIPOLAR input option, install jumper at position labelled "BI" for the desired channel(s).

To select UNIPOLAR input option install jumper at position labelled "UNI" for the desired channel(s).

CONTROLLER OPTION

To select Mode I (4012) install jumpers at positions labelled "TRAQ I" (3 positions). Remove all jumpers at "TRAQ I" positions.

To select Mode II (4012A, 4012P), install jumpers at positions labelled "TRAQ II" (2 positions). Remove all jumpers at "TRAQ I" positions.

CALIBRATION and ALIGNMENT

Each channel of the DSP 2825 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left hand side cover. Drawing 2860-01-AD indicates the location of each channel and the adjustments for each.

BIPOLAR MODE CALIBRATION

1. Set channel to bipolar mode according to section 3.1.

2. Set digitizer sampling clock to 1MHz.

3. Connect 0.000 volt reference to + input of channel.
   Connect 0.000 volt reference to - input of channel.

4. Adjust R12 (Offset) so that the digitized readout from the 4012 controller (averaged over 10 samples) reads 2047.5 (+/- 0.5).

5. Connect +4.900 volts reference to + input of channel.
   Connect 0.000 volts reference to - input of channel.

6. Digitize and average over 10 data samples.
   Adjust R27 (+Gain) for averaged reading of 4054 (+/- 0.5).

7. Connect +4.900 volt reference to + input of channel.
   Connect +4.900 volt reference to - input of channel.

8. Digitize and average over 10 data samples.
   Adjust R34 (-Gain) for averaged reading of 2047.5 (+/-0.5).

MODEL 2860 12BIT / 1MHz / 4 CHANNEL ADC

OPTIONS

UNIPOLAR/BIPOLAR SIGNAL INPUT

To select BIPOLAR input option, install jumper at position labelled "BI" for the desired channel(s).

To select UNIPOLAR input option install jumper at position labelled "UNI" for the desired channel(s).

CONTROLLER OPTION

To select Mode I (4012) install jumpers at positions labelled "TRAQ I" (3 positions). Remove all jumpers at "TRAQ I" positions.

To select Mode II (4012A, 4012P), install jumpers at positions labelled "TRAQ II" (2 positions). Remove all jumpers at "TRAQ I" positions.

CALIBRATION and ALIGNMENT

Each channel of the DSP 2860 has an individual set of calibration adjustments. Access to the offset, gain, and common mode rejection trims is achieved by removing the left hand side cover. Drawing 2860-01-AD indicates the location of each channel and the adjustments for each.

BIPOLAR MODE CALIBRATION

1. Set channel to bipolar mode according to section 3.1.

2. Set digitizer sampling clock to 1MHz.

3. Connect 0.000 volt reference to + input of channel.
   Connect 0.000 volt reference to - input of channel.

4. Adjust R12 (Offset) so that the digitized readout from the 4012 controller (averaged over 10 samples) reads 2047.5 (+/- 0.5).

5. Connect +4.900 volts reference to + input of channel.
   Connect 0.000 volts reference to - input of channel.

6. Digitize and average over 10 data samples.
   Adjust R27 (+Gain) for averaged reading of 4054 (+/- 0.5).

7. Connect +4.900 volt reference to + input of channel.
   Connect +4.900 volt reference to - input of channel.

8. Digitize and average over 10 data samples.
   Adjust R34 (-Gain) for averaged reading of 2047.5 (+/-0.5).

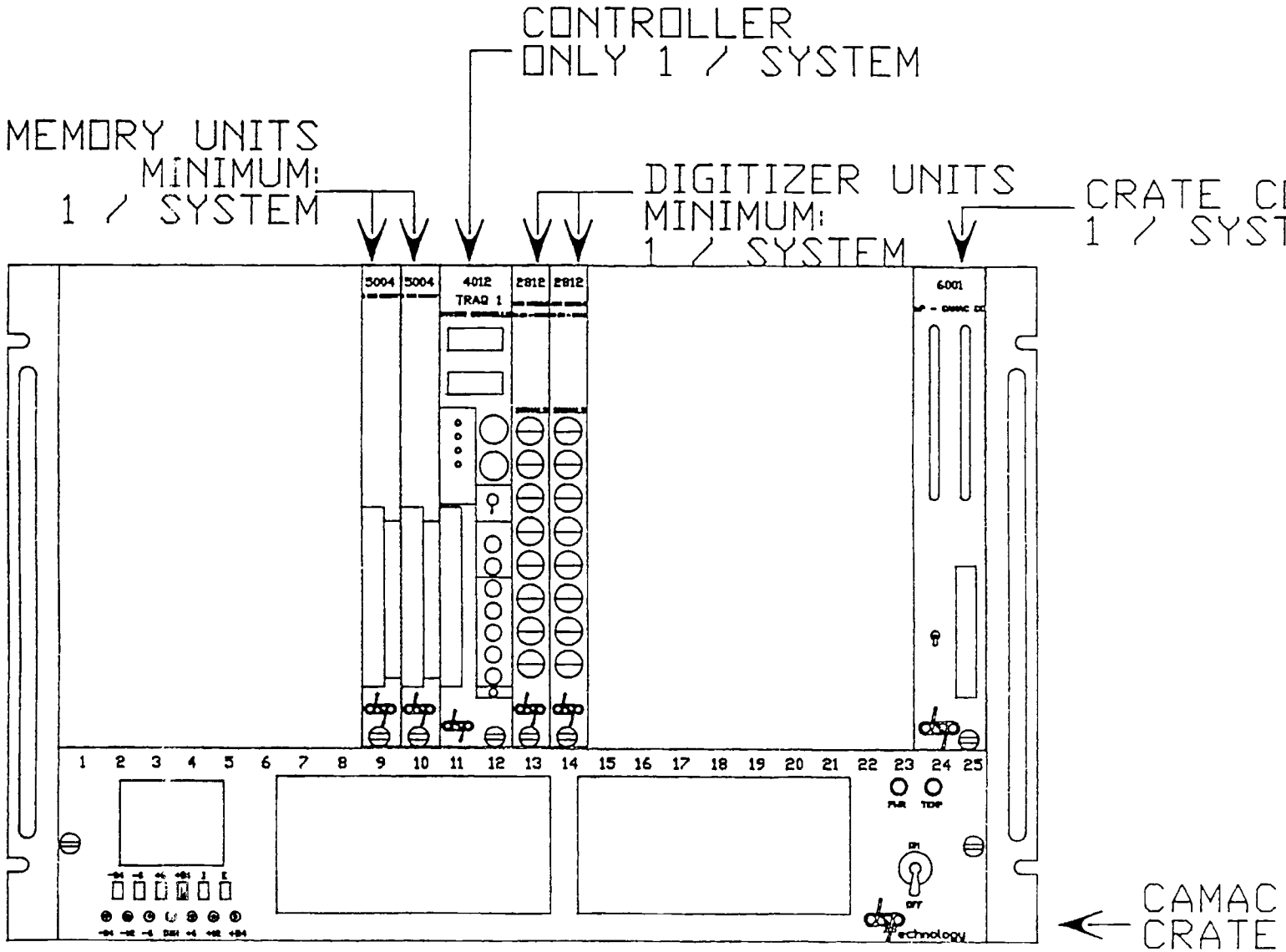
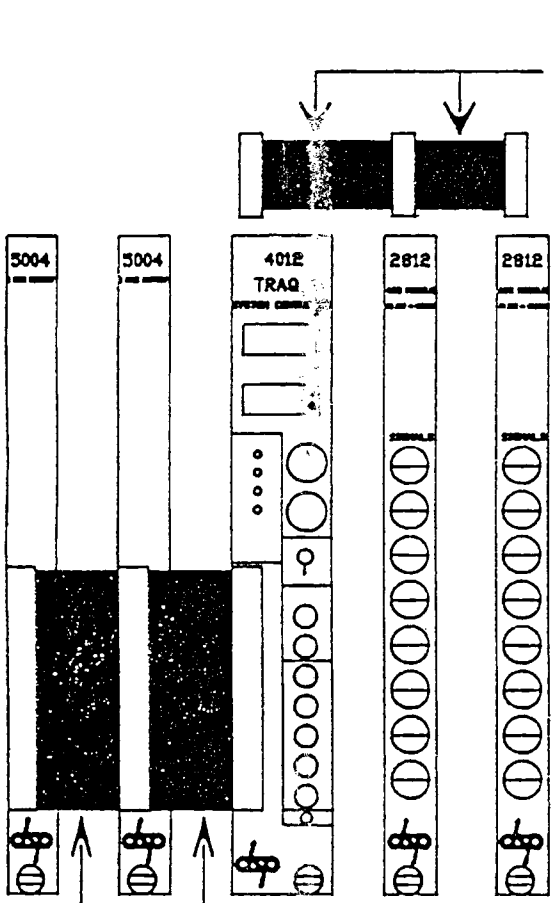


DIAGRAM 1
TRAQ CONFIGURATION DRAWING



40 PIN DAISY CHAINED CONNECTOR
CONNECTS TO:
REAR OF 4012 CONTROLLER
& REAR OF EACH DIGITIZER MODULE

DIAGRAM 2
TRAQ
SYSTEM
INTERCONNECT

50 PIN DAISY CHAINED CONNECTOR
CONNECTS FROM 4012 CONTROLLER
TO EACH MEMORY MODULE

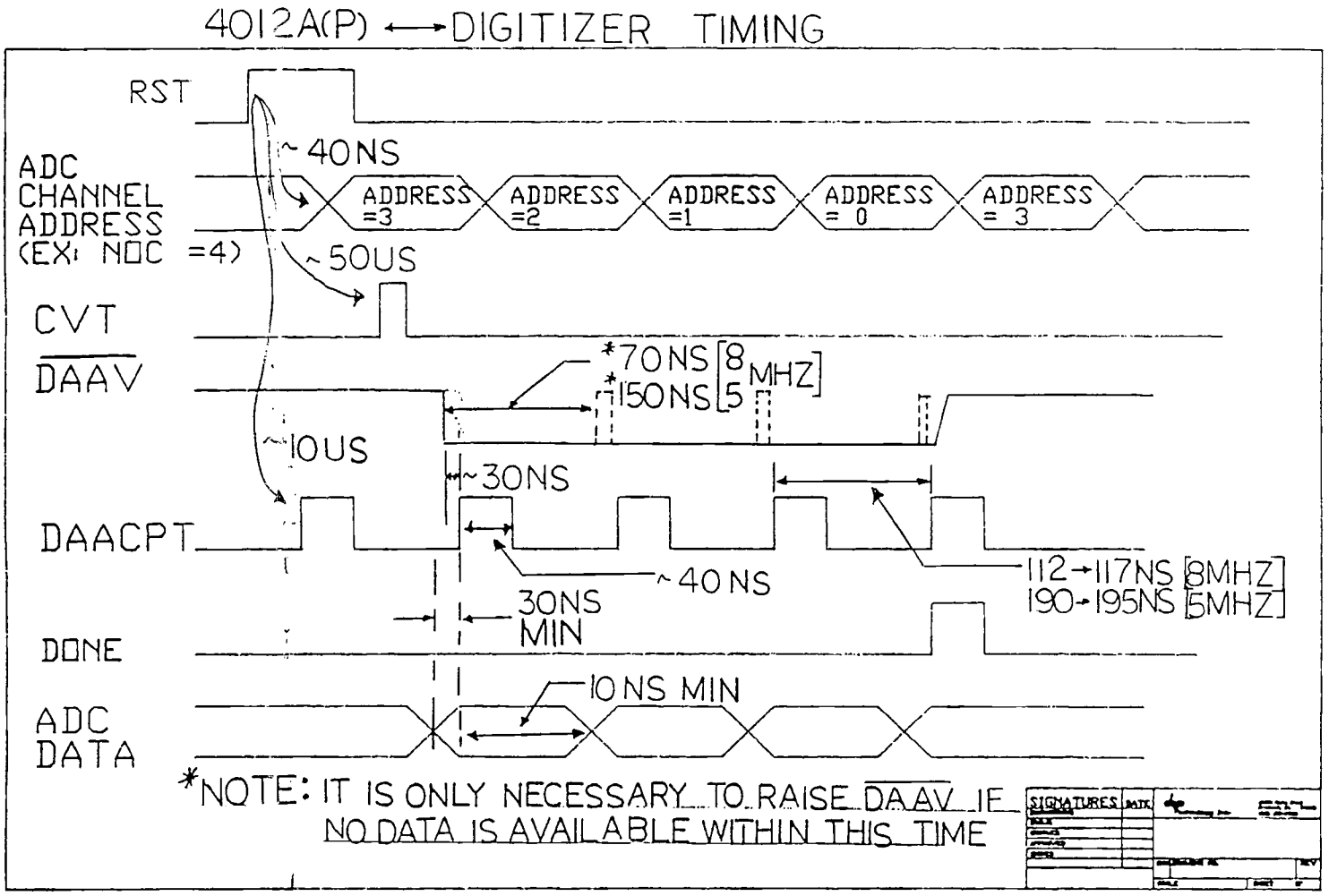

4012A(P) ⟷ DIGITIZER TIMING
RST
~40NS
ADC CHANNEL ADDRESS (EX: NOC =4)
ADDRESS =3
ADDRESS =2
ADDRESS =1
ADDRESS = 0
ADDRESS = 3
~50US
CVT
DAAV
*70NS [8 MHZ]
*150NS [5
~10US
~30NS
DAACPT
~40 NS
112→117NS [8MHZ]
190→195NS [5MHZ]
30NS MIN
DONE
10NS MIN
ADC DATA
*NOTE: IT IS ONLY NECESSARY TO RAISE DAAV IF NO DATA IS AVAILABLE WITHIN THIS TIME
SIGNATURES

DIAGRAM 3