

# Using VME to Leverage Legacy CAMAC Electronics into a High Speed Data Acquisition System<sup>1</sup>

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## Abstract

We report on the first full scale implementation of a VME based Data Acquisition (DAQ) system at the Stanford Linear Accelerator Center (SLAC). This system was designed for use in the End Station A (ESA) fixed target program. It was designed to handle interrupts at rates up to 120 Hz and event sizes up to 10,000 bytes per interrupt. One of the driving considerations behind the design of this system was to make use of existing CAMAC based electronics and yet deliver a high performance DAQ system. This was achieved by basing the DAQ system in a VME backplane allowing parallel control and readout of CAMAC branches and VME DAQ modules. This system was successfully used in the Spin Physics research program at SLAC ( E154 [1] and E155 [2]).

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## Summary

With the approval for 50 GeV upgrade to the A-line for precision nucleon polarized structure function measurements it became necessary to also upgrade the data acquisition system used in End Station A (ESA). The experiments for this program would be implemented to be triggerless [1][2]. This would allow the electronics to capture as complete a snapshot as practical of the events generated by each beam spill passing through the target. This approach would lead to large data rates and consequently to large collected data volumes.

Our design goals for the data acquisition were to have high data rates capabilities, reuse existing CAMAC electronics, and to be reasonably priced. Other design criteria were that the DAQ should be easily reconfigurable, meaning that the exact detector configuration should not be built into the DAQ software but should instead be specified in a setup file. And that the DAQ be implemented in such a way so as to be easily upgradable to handle higher data rates. We chose the VME system on which to build the DAQ, mainly for its flexibility and the availability of a wide variety of DAQ modules and interfaces to other bus architectures, like CAMAC, Fastbus, etc. We chose BiRa 1711 list driven VME to CAMAC interfaces which use the VSB bus (VME Subsystem Bus extension) for data readout. The list processing capabilities of these modules allows the CAMAC data readout to proceed independently of other Real-Time activities. The use of VSB for readout can be utilized to transfer data from these modules into the VME system without interfering with other data movement on the VME backplane. These features help offset the inherently slow data movement on the CAMAC highway. Multiple VME to CAMAC interfaces are used to process the data in parallel thus further increasing the data throughput from CAMAC into the VME. The VME crates are linked with a reflective memory network used to synchronize various tasks executing on processors in these crates as well as building the event data and passing that data from the Real-Time part of the system to the non-Real-Time part which logs the data to archive media and distributes some of this data for online analysis. The non-Real-Time part of the DAQ consists of one VME crate which houses a processor module operating under a System V Unix, and an FDDI interface which links this VME crate to a logging workstation and other computers which serve and control a tape silo robot system. The logging workstation was dedicated to run tasks which receive data from the VME system, write the data to a disk staging pool and initiate transfer of the data from the disk staging pool to the silo tapes.

The actual implementation of the VME subsystem of the DAQ is shown in Figure 1. Three VME crates are used. The crate labeled "remote" is placed near the detectors on the experimental hall floor mainly to minimize the cost of the cable plant needed to bring the detector signals into the DAQ. The remaining two VME crates are located in the "counting house" at a distance approximately 400 feet from the detectors. The "remote" VME crates controls two CAMAC branches which process signals from all experiment detectors. The VME crate labeled "local" controls one CAMAC branch which processes signals from electron beam monitoring and control electronics.

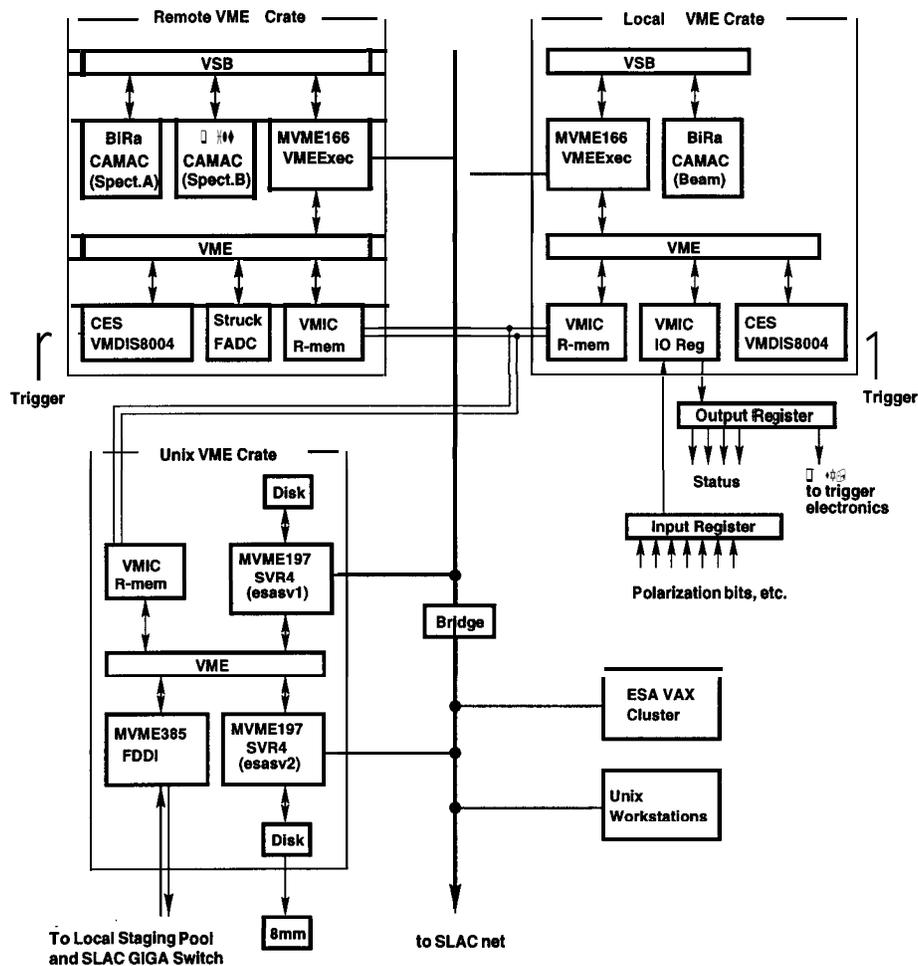


Figure 1: Block Diagram of the Real-Time and Unix VME Components

At this time, two major experiments and several test beam experiments have been completed which used this VME based DAQ system [1][2][3]. Initially this system was capable of handling sustained data rates up to 700 Kbytes/sec. Performance was boosted by moving the readout of a block of LeCroy TDC modules (LRS3377) from CAMAC highway to an external ECL bus which brought the data directly into a VME memory module at approximately 10 times the CAMAC highway speed without CPU involvement. With this modification, the system was capable of handling sustained data rates slightly in excess of 1 Mbyte/sec.

Figures 2 through 14 are taken from the poster presentation of this work shown at the IEEE 1997 Nuclear Science Symposium, Nov. 9-15, in Albuquerque, New Mexico.

## **Functional Requirements:**

- Multiple data collection points separated by up to 500 feet.
- CAMAC interfaces to read out over 1600 channels of multi-hit TDC's, over 600 channels of ADC, and other miscellaneous modules.
- Support for VME based Flash ADC's.
- 120 Hz nominal trigger rate and 10,000 bytes of data per trigger (data rates in excess of one megabyte per second).
- System configurable via setup files to specify the experiment specific CAMAC and VME input/output operations.
- Logging to SLAC central tape silo facility.

Figure 2: Functional Requirements for DAQ System (from IEEE Poster)

## System Components:

- DEC Vax VMS workstations for running monitoring and control software.
- IBM RS6000 class UNIX workstations for logging data to the SLAC tape silo (includes FDDI interface) and for “online” data analysis.
- Real-time components housed in standard 6-U VME crates with VSB back plane overlays.
- MVME197 VME CPU board running SVR4.3 as the data logging interface.
- MVME385 VME FDDI interface.
- MVME166 VME CPU board running VMEexec for the Real-time processors (includes support for VSB bus).
- **BiRa** 1711 VME-CAMAC Parallel Branch Highway (CC-A2 compatible) interface modules (connect to the VSB bus).
- VMIVME5550 VME Reflective Memory modules.
- VMIVME2532 VME-32 channel Input/Output module.

Figure 3: System Components for DAQ System (from IEEE Poster)

## Description:

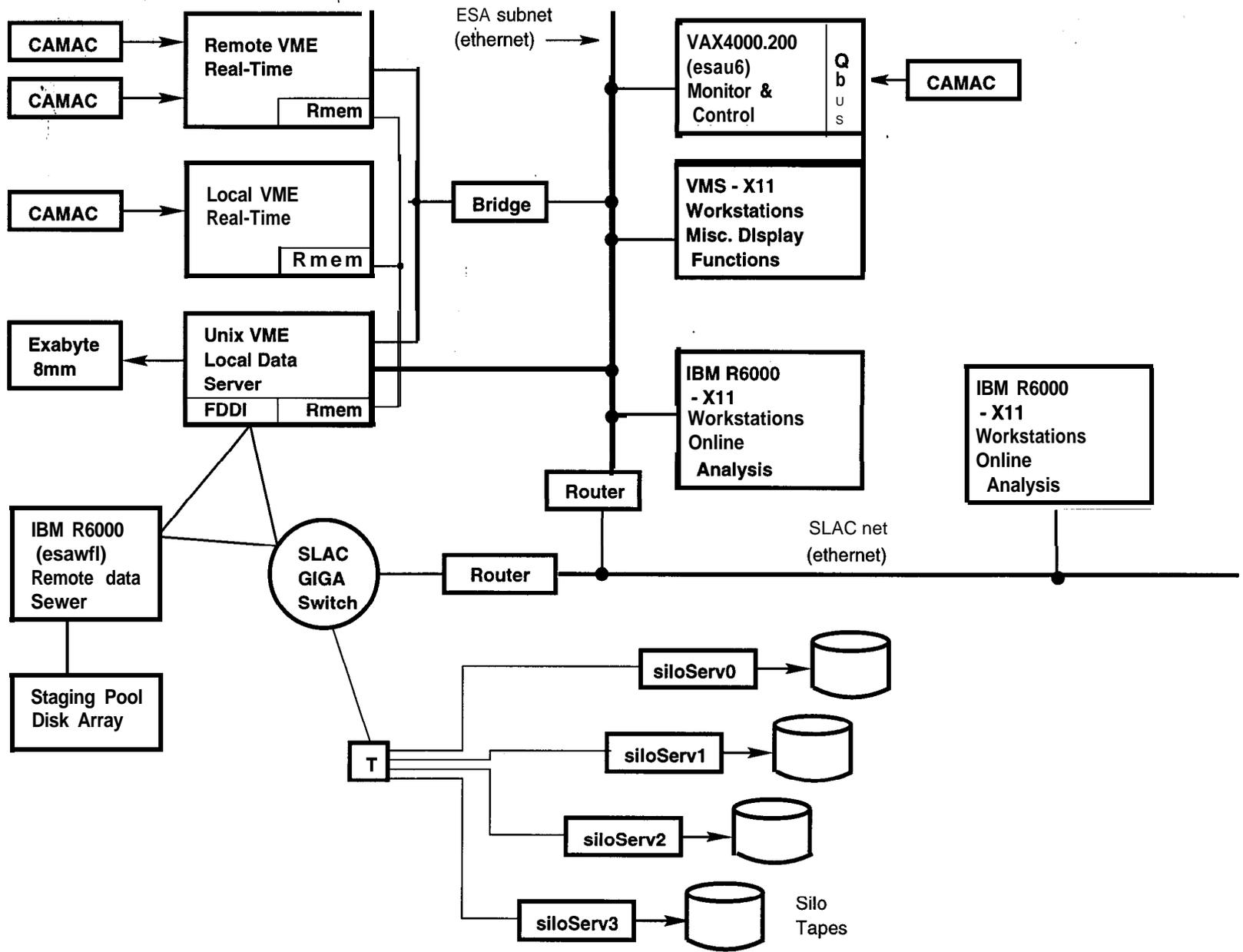
- The Data Acquisition System is composed of a number of discrete subsystems which are distributed over several different computing platforms. These subsystems include Experiment Control & Monitoring (high/low voltage monitoring, target selection, etc.), Real-time Data Acquisition components, and the Data Logging subsystem. All of these subsystems communicate with each other via ethernet and/or FDDI (using client-server communication technology) and "Reflective Memory Buffers" (using simple handshaking protocols).
- The Experiment Control & Monitoring and Data Logging subsystems run on a variety of standard workstations (VAX VMS and UNIX). Messages are exchanged between these components and to/from the Real-time components over standard ethernet. Data and logging control messages are exchanged between the logging interface of the Real-time component and the Data Logging subsystem over FDDI.
- The Real-time subsystem is distributed in three VME crates. Two of these crates contain the Real-time components and interface modules. The third VME crate contains the interface to Data Logging subsystem for logging data to the SLAC central tape facility. All three crates are connected via "Reflective Memory buffers" which provides for data exchange between the crates without CPU overhead.
- The logging interface VME crate contains an MVME197 CPU board running a variant of the System V UNIX operating system. This CPU removes events from the reflective memory buffer in that crate, packages them for transmission to the logging system and sends them to the logging system via a fibre optic link (FDDI).
- Each Real-time VME crate contains a MVME166 CPU board running VMEexec. This CPU controls the CAMAC interface modules, and any VME data acquisition modules in that crate. The CPU builds events into the reflective memory buffer in that crate (each Real-time crate contributing its part towards the full event).
- The two Real-time VME crates serve distinct functions. One crate collects data from the electron beam monitoring system and interfaces with the experiment triggering and control components. This crate contains an interface to CAMAC and a VME based IO board for digital signal exchange with the experiment (e.g. computer busy to suppress triggers). The second VME crate reads out the experiment spectrometer electronics. This crate contains two CAMAC interfaces to allow parallel readout of the large number of CAMAC channels for enhanced data throughput. Five VME based Flash ADC's are also located in this crate. These crates can be spatially separated by up to 500 feet.
- BiRa Systems 1711 VME-CAMAC interfaces are used in the Real-time system. These modules are loaded with a list of CAMAC operations to be carried out at each trigger and can read out a number of CAMAC modules before requiring CPU attention.

Figure 4: DAQ System Description (from IEEE Poster)

## System Performance and Experience:

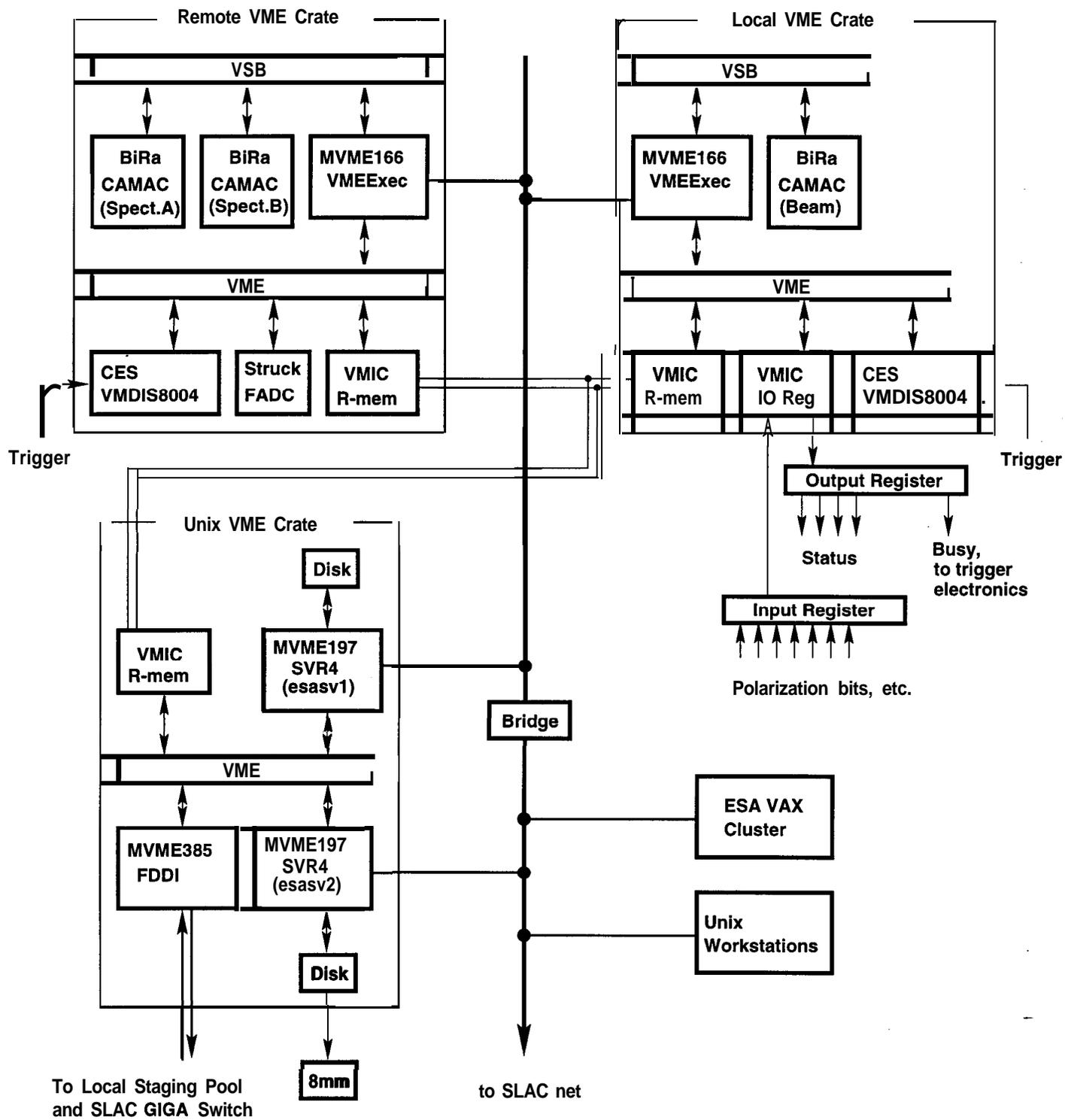
- The general performance of the system was quite good. VMEexec provided a robust base for building the Real-time software components. The hardware architecture of the Real-time system allowed for a software design with multiple tasks conducted in parallel to provide higher data throughput than could be achieved with the individual components. The readout of modules via the CAMAC dataway was the biggest bottle neck for achieving high data rates. This was overcome in part by using multiple VME-CAMAC interfaces. In addition, since the CAMAC interfaces operated by processing a list of commands at each interrupt, the VME CPU was free to process other tasks (reading out VME based data acquisition modules and transferring the previous event data into the reflective memory event buffers) while the CAMAC data was being transferred into the local memory of the VME-CAMAC interface, further improving system performance. The system was designed so that further improvements could be made as needed (for example, adding an additional CPU to transfer data from the CAMAC interfaces to VME memory via the VSB bus while the main CPU transferred data across the VME back plane).
- In the initial use of this system (E154), the design goal of one megabyte per second was not reached. System throughput reached a peak of about 700 Kbytes/sec, limited largely by the CAMAC dataway speed. To improve performance read out of the bulk of the CAMAC TDC's was moved off of the CAMAC dataway. This was possible because these TDC's (LeCroy 3377) support an ECL read out bus. Using this bus, data is transferred directly from the TDC's into a VME based memory module, at 10 times the data rate of the CAMAC dataway. This change to the read out allowed the system to achieve the design goal of 1 Mbytes/sec (E155).
- Other factors limiting the maximum data rate include the speed of the reflective memory bus, CPU interrupt overhead, and FDDI speed. The reflective memory modules used in this system transmit data between each module over a twisted pair backbone. At the crate separation needed (500 feet), this bus runs at only 1.5 Mbytes/sec. It is planned to replace this bus with a fibre optic bus running 5 to 10 times faster to remove this component as a limiting factor. The CAMAC interfaces can only handle about a quarter of the CAMAC modules they service before requiring CPU attention. With only one CPU in the crate servicing two CAMAC interfaces, a significant performance hit is taken as these two interfaces compete for attention. This problem can be easily alleviated in future experiments by adding a second CPU to this crate to handle the second CAMAC interface should that be required. It is hoped that future experiments will rely on VME and other non-CAMAC dataway devices. Finally, the FDDI network in use at SLAC can currently only support data transfer rates slightly in excess of 2 Mbytes/sec with full handshaking between the data source and sink (limited mainly by the driver for the FDDI interfaces on the IBM RS6000 workstations). SLAC is continuing to upgrade and improve the network and rates up to 6 to 8 Mbytes/sec should be easily achievable if needed (using 100 Mbit/sec networks).

Figure 5: DAQ System Performance (from IEEE Poster)



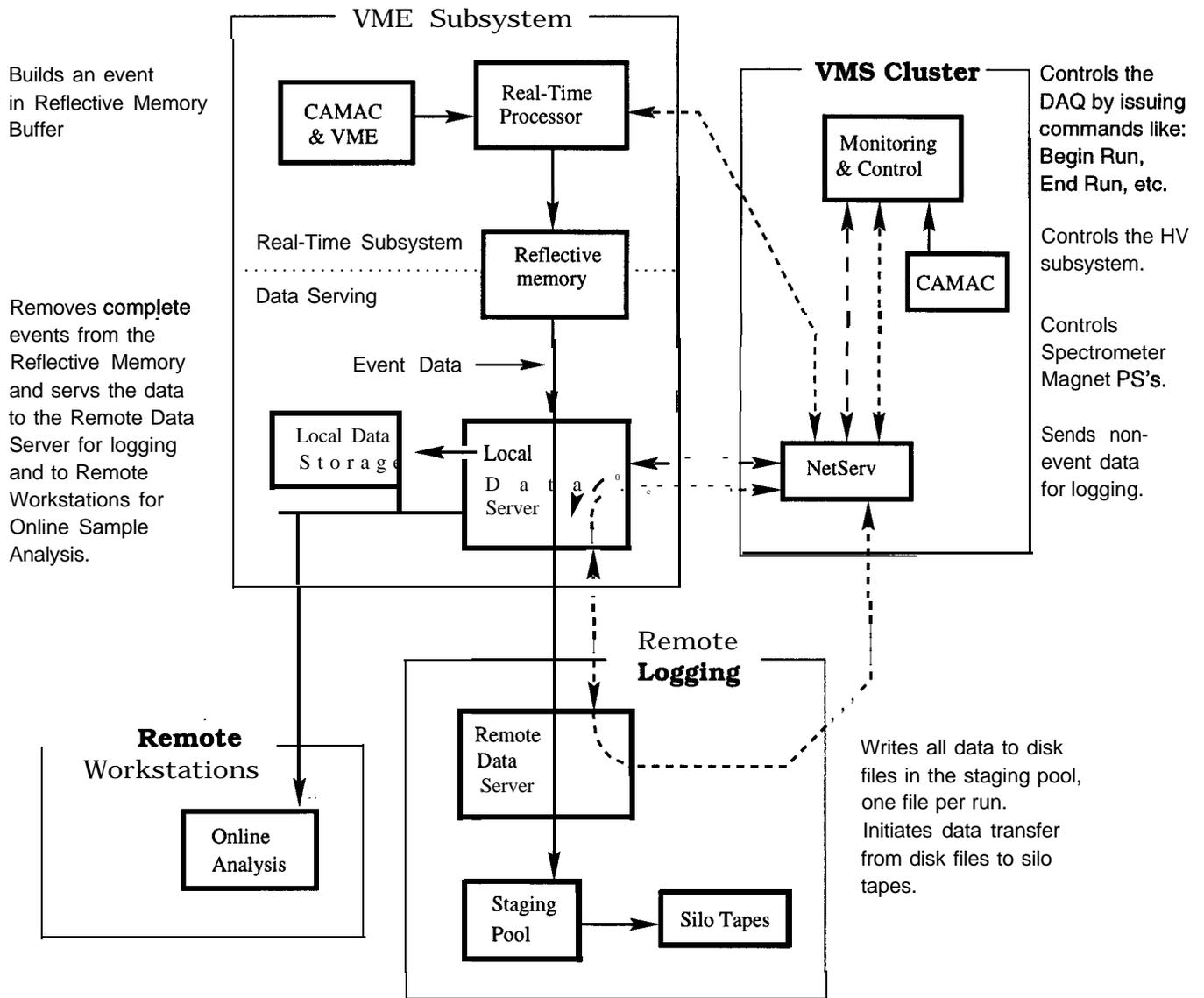
**Hardware Components**

Figure 6: Block Diagram of DAQ (from IEEE Poster)



## VME Subsystems

Figure 7 Block Diagram of Real-Time Components (from IEEE Poster)



### Data Flow Diagram

- data path
- - non-event data
- message & control

Figure 8: Block Diagram Showing Data/Control Paths (from IEEE Poster)

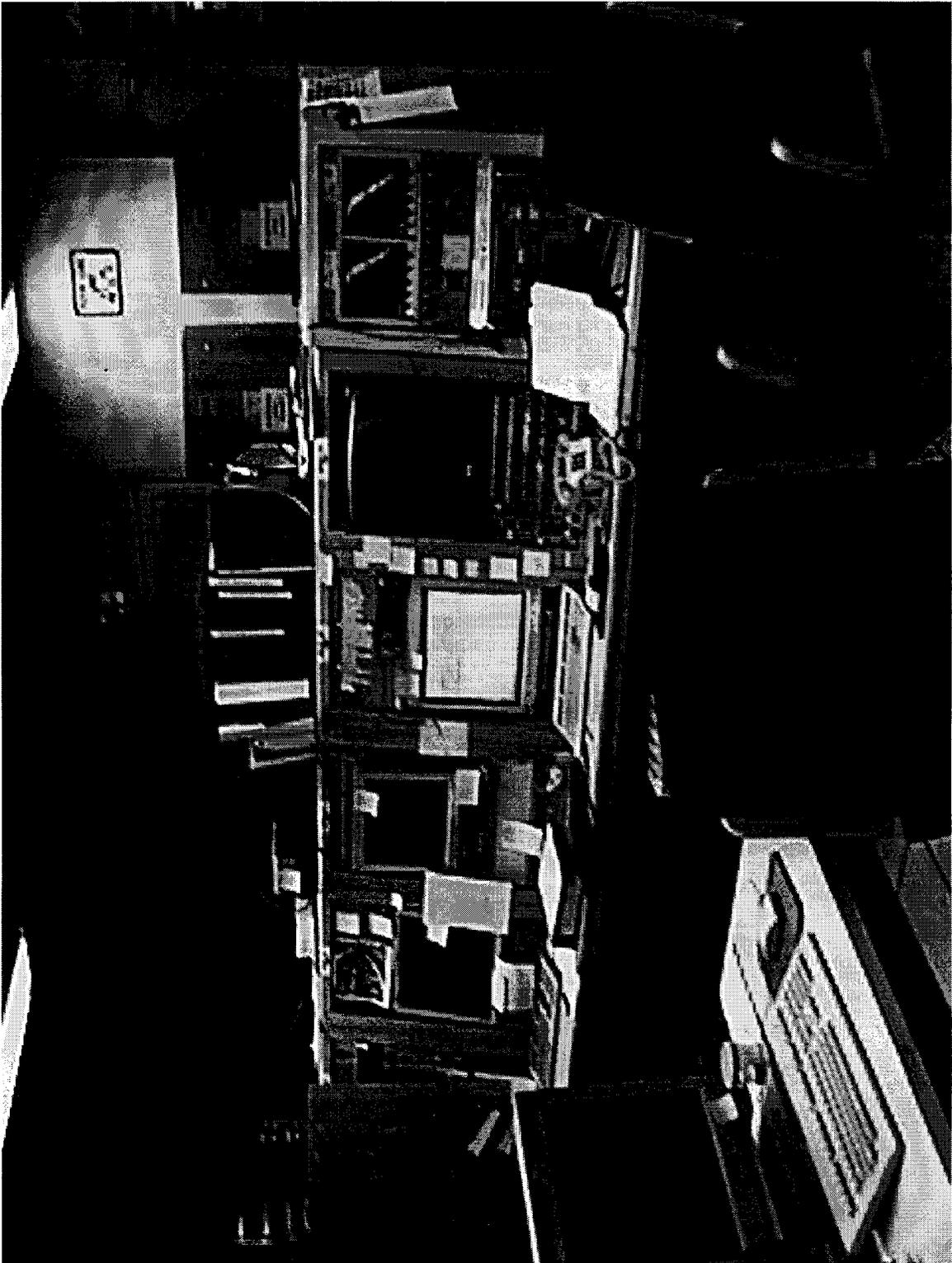


Figure 9: Experiment Control Console (from IEEE Poster)



Figure 10: Experiment, Trigger Electronics (from IEEE Poster)

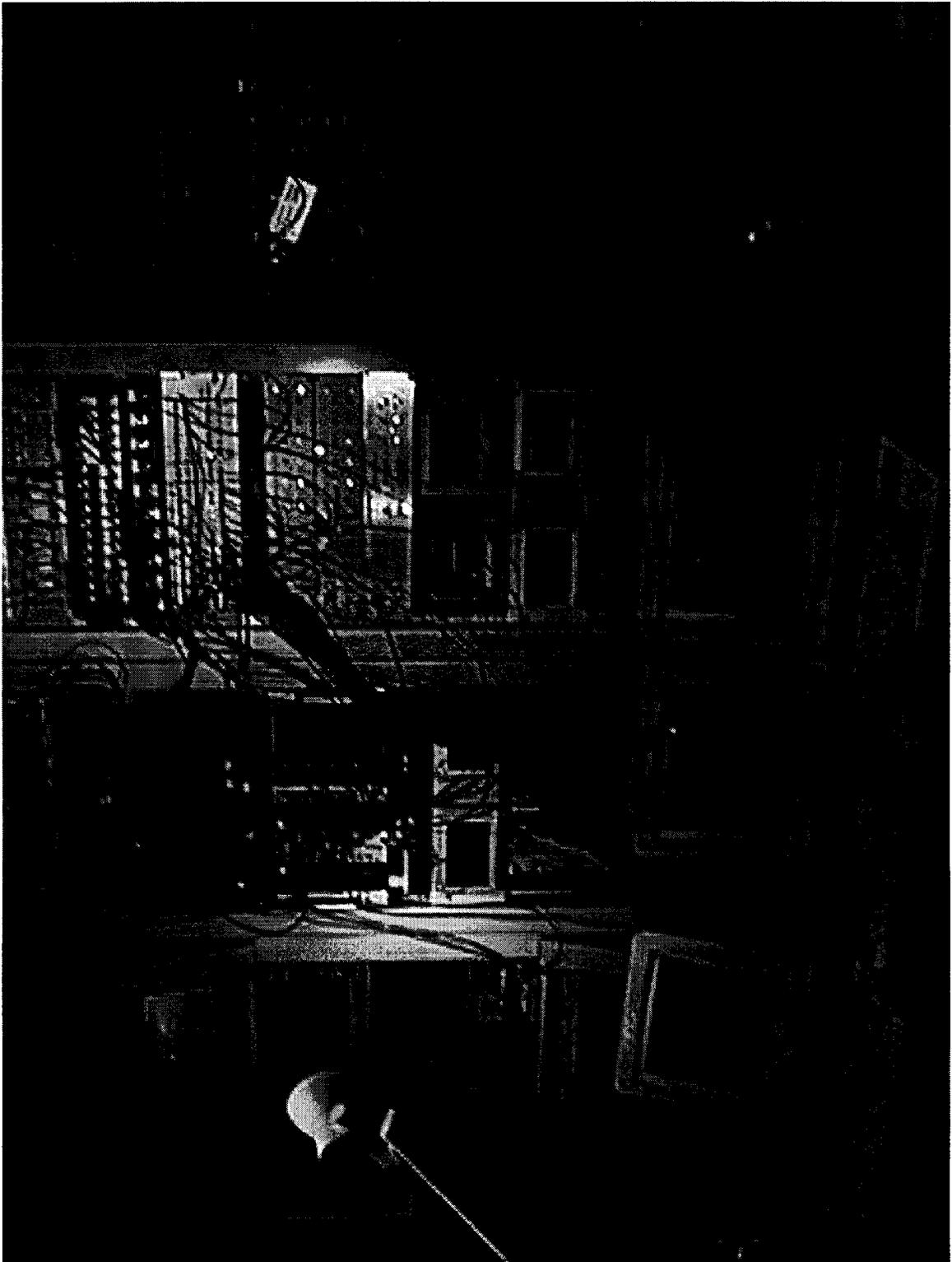


Figure 11: Local VME Systems and Supporting Electronics (from IEEE Poster)

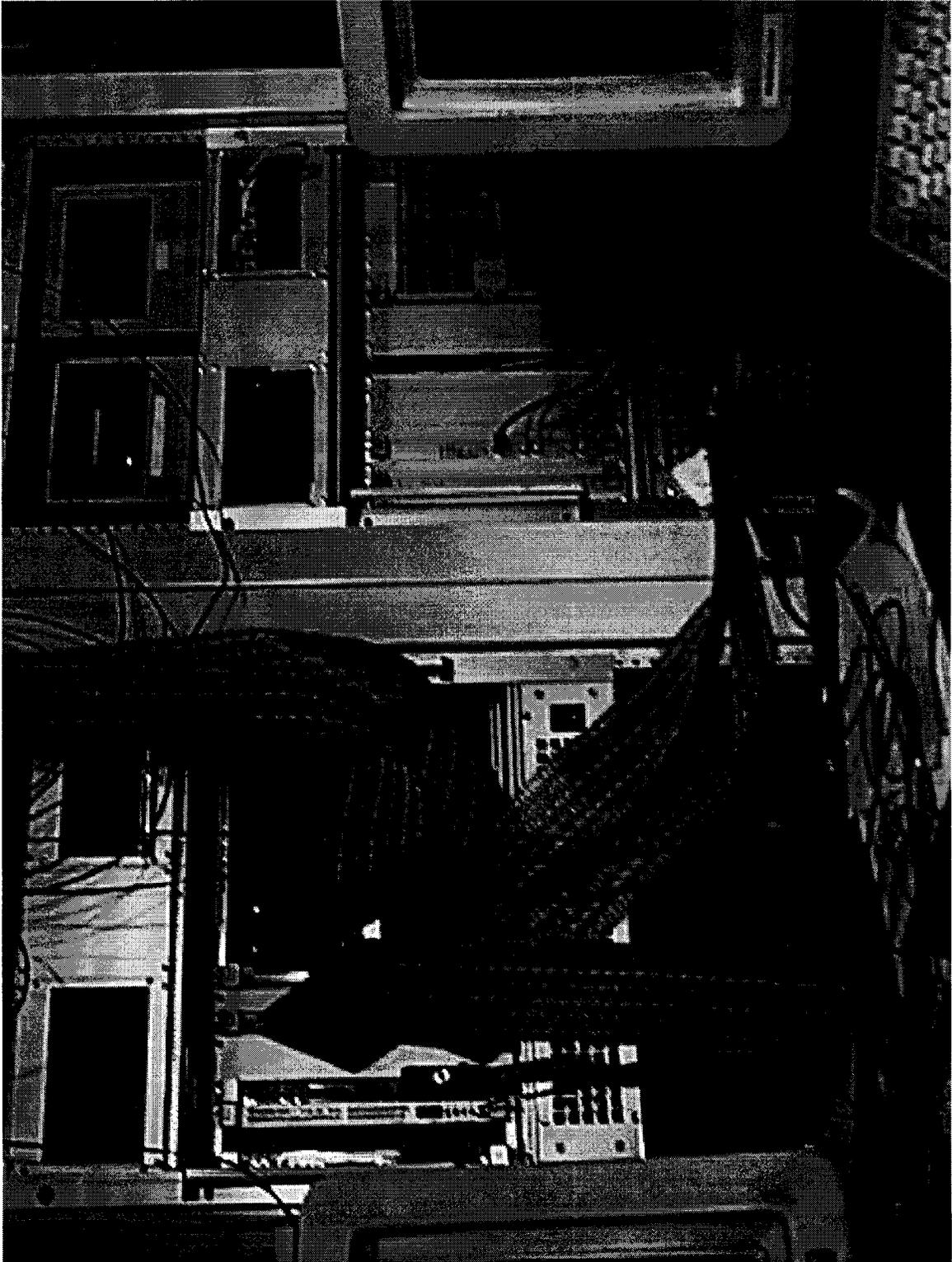


Figure 12: Detail of Local VME Systems (from IEEE Poster)

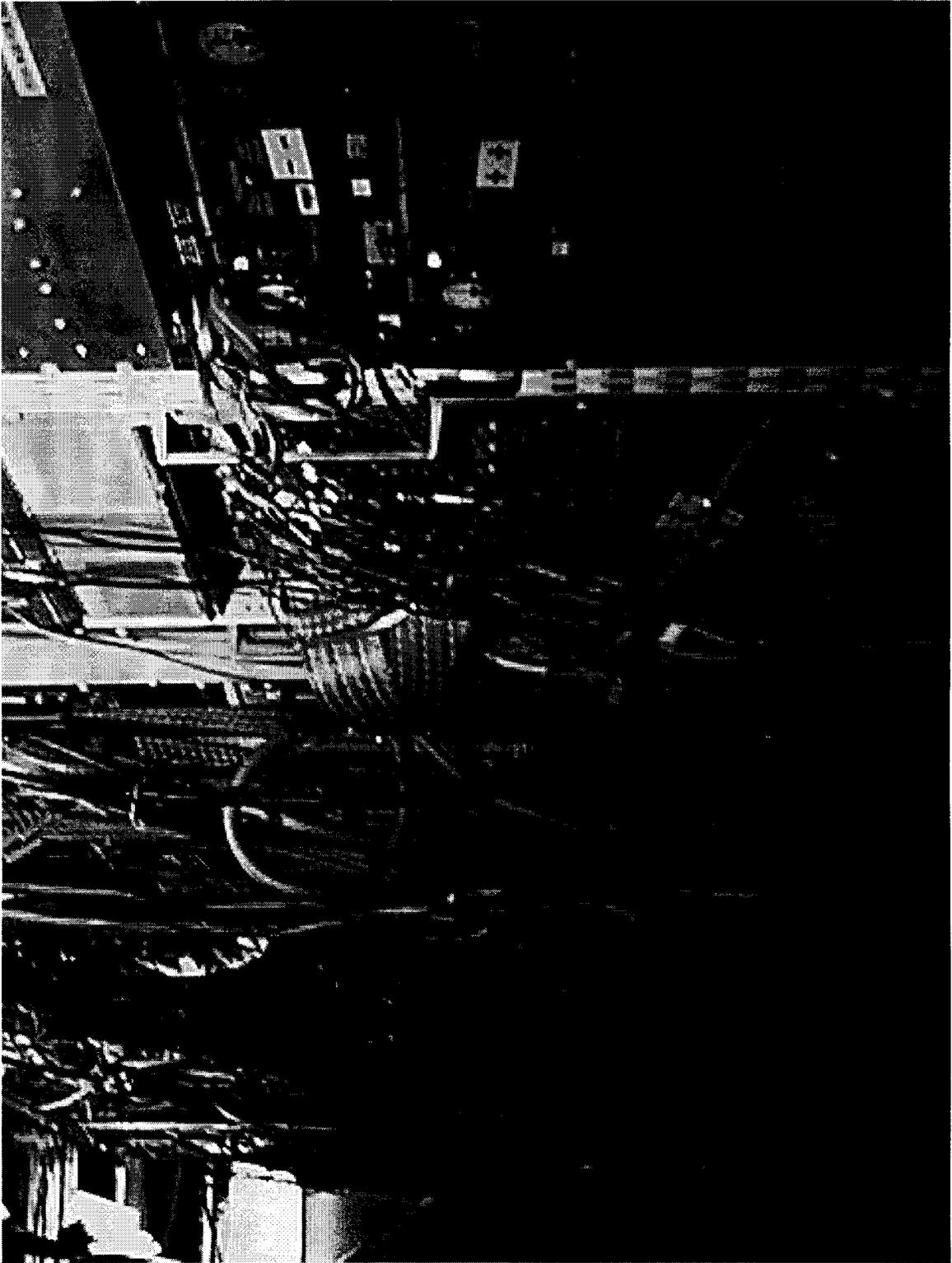


Figure 13: Remote VME System and Read-Out Electronics (from IEEE Poster)

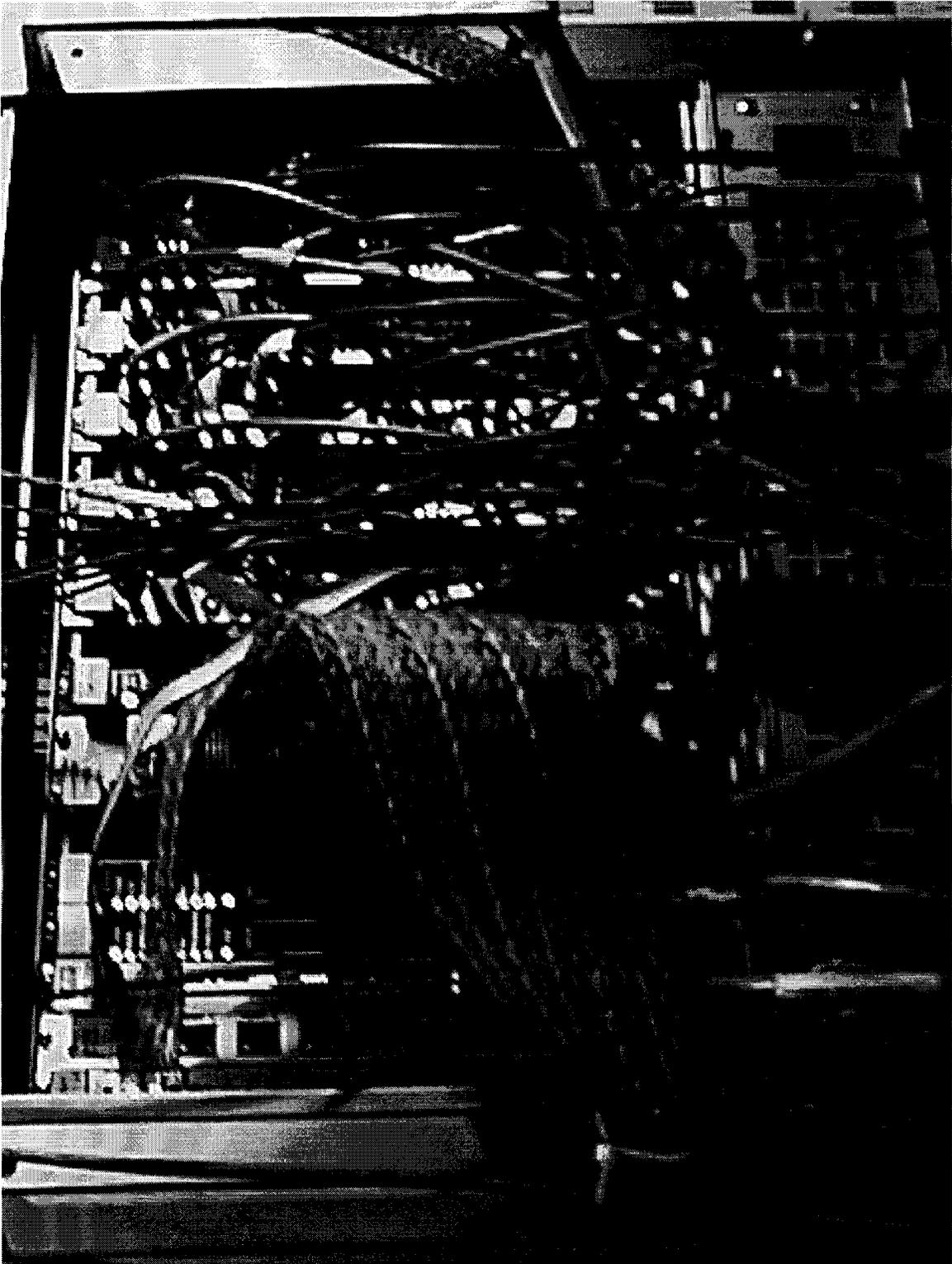


Figure 14: Detail of Remote VME System (from IEEE Poster)

## References

- [1] "A Proposal for a Precision Measurement of the Neutron Spin Structure Functions Using a Polarized  $He_3$  Target", SLAC-PROPOSAL-E-154, Oct. 1993, 36pp.
- [2] "Measurement of Nucleon Spin Structure at SLAC in End Station A", SLAC-PROPOSAL-E-155, Jan. 1994, 56pp.
- [3] "Gamma Large Area Silicon Telescope (GLAST): Applying Silicon Strip Detector Technology to the Detection of Gamma Rays in Space", SLAC-PUB-6267, Jun 1993, also *Nucl. Instrum. Meth.* A342, 302-307, 1994. See also Michelson, P. F., *et. al.*, "Development of GLAST, A Broadband High Energy Gamma-Ray Telescope using Silicon Strip Detectors", NASA Advanced Missions Concept NRA 94-OSS-15.