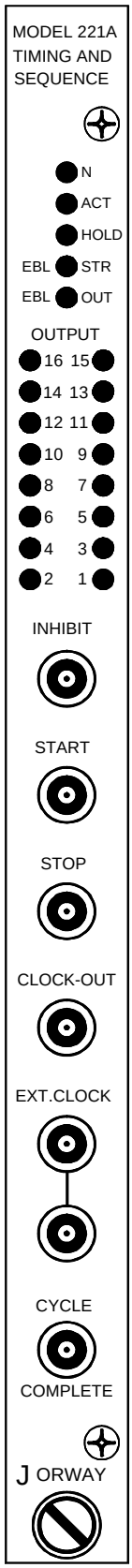
MODEL 221A

16 CHANNEL TIMING /SEQUENCE

Upgraded Model 221

* Channel output changed from 12 to 16 channels - less than $100 per channel
* Memory increased to 512K words per channel, enough for a programmable clock useful as a transient recorder clock.
* Maximum clock rates now 10 MHz up from 1 MHz
* Programmable logic states for outputs, logic 1 as TTL high or TTL low signal
* Programmable Output Mode, traditional gate signal or internal clock for gate interval, useful as transient recorder clocks



INTRODUCTION This Timing and Sequence Module is a general purpose device, designed to provide a serial sequence of 16 time related signals. A stored program of up to 512K set points determine timing and logic state of 16 output channels. The Model 221A, an upgrade of the popular Model 221 preserves most of the features of the Model 221 while enhancing performance and adding new features. The maximum memory capacity has been expanded to 512K set points as compared to 4K size for the former model. The large memory size allows channels to be programmed as a variable clock for use in clocking transient recorders. The programmed STOP set point value of 16,277,215 is preserved so sequences with fewer set points is maintained. The output word size has been increased to 16 bits. A 34 pin rear connector accommodates the extra 4 bits however the lower 26 pin are identical to the Model 221 for compatibility. A 26 wire ribbon crimped into a 34 pin header will allow connection to existing Model 221 applications.

Some differences exist between the 221 and 221A models. The Model 221A has eliminated the seldom used Inhibit Switch although it can be provided on special order. Two bussed Lemo connectors are provided for the External Clock Input to make daisy-chaining easier. The Model 221A provides a new signal, CLOCK OUTPUT which is useful in synchronizing multiple modules to operate from the same clock source.

BASIC OPERATION The timing sequence is determined by the value set in a 512K word by 24 bit set point memory and a 512K word x 16 bit output memory. Each of the possible 512K set points can be programmed to occur at any fixed time up to 16,777,215 clock intervals. Set points must be set in ascending values with minimum interval of 0.1 or 1.0 microsecond with a respective 10 MHz or 1 MHz clock. When started and cycle active, counting of clock intervals begins and as each set point is reached, the output memory determines the state of all sixteen outputs. Each output may be made to change state or remain at its previous level. Once the module is started, all other start trigger inputs are ignored until either a stop, reset and enable operation occur. Once triggered and cycle active, the application a stop trigger will cause the cycle to be put on hold. At this point operation will not continue and the sixteen outputs will remain in their current state. The subsequent application of a start trigger input will cause the cycle to continue from the point where "hold" occurred.

CLOCK This module uses a clock derived from either an external clock input or from an internal 10 MHz oscillator.. When the internal 1 MHz rate is selected, the 10 MHz oscillator is synchronized and counted down to 1 MHz as a basic clock rate for the module and the output sequence will begin within approximately 200 ns of the start signal. The basic clock of 1 MHz or the external clock is further divided by 10 to provide a 10 usec clock for set point timing and a total sequence length of 167.7 seconds. The internal oscillator or external clock may also be used at rates up to 10 MHz for a 100 ns timing resolution in the Model 221A.

INTERNAL MEMORY Set point times are stored in ascending order in a 24 bit wide by 512K word memory. A separate 16 bit by 512K long output memory is used to store the output word data associated with each set point. Memories can be written as well as read from the dataway to aid in diagnostic testing. A common 24 bit address counter is used for both memories. In addition read and write of memories auto increment the memory address. A separate load memory address counter command allows access to single memory words for read or write. For fewer than the maximum number of set points all ones (16,777,215) written into the set point memory will terminate cycle execution. Cycle execution is also terminated by (a) address overflow (greater than 512K set points,(b) Set point overflow (address counter overflow, or (c) any command which terminates the active cycle (F(9)A(0) or ZS2.

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RECYCLE MODE In normal operation when the cycle is completed all outputs and external clock are disabled. Dataway commands must be issued to re-enable the output and external start. An program switch allows selection of a feature called RECYCLE. When selected as "on" clearing of the output and external clock enable will not occur at cycle complete. This allows the 221A once configured for operation to repeat its sequence each time a start trigger is generated. With the polarity selectability of inputs and output control signals it is possible to connect the cycle complete pulse to the external start input so that a start occurs on the trailing edge of cycle complete, i.e. positive cycle complete and negative external start. Once started the sequence will be repeated until reset or disabled.

ADDITIONAL MODEL 221A MODES Two programmable features provide alternatives for the 16 bit output word.

1. Output Polarity Control Register: The normal output generates a high TTL signal for a logic "1" programmed into the output memory. A reset or inhibited output is a TTL low. The Model 221A has a Polarity Control Register which will reverse the output polarity on a individual channel basis. A logic "1" written into the Polarity Register will cause the output to change polarity for that corresponding bit in the Output Memory i.e. Logic "1" written to the Output Memory will cause a TTL low to be issued at the output. A module Clear F(9)A(0) or output inhibit will cause the output to assume a TTL high level. The Polarity Control Register is cleared by power-up, dataway ZS2 or F(9)A(1) but is not cleared by the normal module Clear F(9)A(0) so that the control setting are preserved during normal operation.

2. Gated Clock Outputs: On a individual channel basis an output channel can be selected to output the internal System Clock during the period when the Output Memory is programmed for a logic "1". This feature can be used to generate programmed bursts of clock signals for devices such as transient recorders. Like the Output Polarity Register, the Output Clock Register is cleared only by Power-up, ZS2 or a command F(9)A(1) specifically for the Gated Clock Register.

ANALOG OUTPUT OPTION (Not included in standard Model 221A,see separate ALALOG OPTION data sheet for details)
A single digital to analog channel can be selected to decode up to 12 output word bits. This programmable feature can be selected to decode either bits 1 thru 12 or 4 thru 16. A reduced range of 8 bits (8 thru 16) or 4 bits (12 thru 16) can also be selected. DAC programming can be either of 2 ways, (a) DAC value and digital channel value share the same set point or (b) a special bit selects whether the output memory word is a digital value or a DAC value. If the DAC value is in the 1 thru 12 range then bit 16 is used as the control bit. If the DAC value is any range to bit 16 then bit 1 is the control bit. This control bit allows up to 15 digital channels as well as a 12 bit DAC value by interleaving set points with digital and analog values. Analog resolution is 12 bits, accuracy is 10 bits. Analog slew rate is 10 microseconds.

MODULE INPUTS Input Impedance, 50 Ohms (Internal jumper allows removal of 50 Ohm termination

Start LEMO:	TTL high going signal (Polarity switch +, ON) initiates a sequence if external start has been enabled.
Stop LEMO:	TTL high going signal (Polarity switch +, ON) puts the sequence on hold if the cycle is active.
Inhibit LEMO:	TTL high going signal (Polarity switch +, ON) disables module outputs. Once disabled by the Inhibit the output remains inhibited even if the Output Enable command is given. A module reset F(9)A(0) is required to clear the inhibit. An internal strap is available to prevent the inhibit from operating.
External Clock	TTL signal used to provide system clock. Negative edge is active edge for sequence timing

MODULE OUTPUTS

Cycle Complete:	A positive going TTL pulse 1 usec wide will occur whenever an active cycle is terminated.
CLOCK-OUT	TTL signal for Master/Slave operation of multiple modules. Master/Slave switch selects clock mode
Output Word:	The 16 bit module sequence word will occur at a 34 pin ribbon type connector at the module rear. Outputs will be Logic "1" true, +2 volts minimum into 50 ohms and Logic "0" 0 to +.4 volts.
Reset:	A negative going 200 ns TTL pulse capable of driving 10 TTL loads will be generated during at the rear 34 pin ribbon type connector for driving other modules i.e. Model 222 Buffer Module.

FRONT PANEL INDICATORS (LED)

N:	N indicator is illuminated for 100 ms or the duration of N whenever the module is addressed.
Outputs	A front panel LED is illuminated for a high TTL signal on each appropriate output line.
Active:	"ACT" LED is illuminated whenever the module has been started and a cycle is being executed. The LED will remain on even if a Hold has been initiated.
Hold:	"HOLD" LED is illuminated whenever the cycle is active and a Hold has been triggered. It will go off when the sequence is restarted or the sequence is terminated or reset.
Outputs Enabled:	"EBL OUT" LED is illuminated when ever the module outputs have been enabled.
Start Enabled:	"EBL STR" LED is illuminated whenever the external start function has been enabled.

USER SELECTABLE OPTIONS

SW# A DIP switch accessible at the module bottom edge allows for the following user controllable options.

1	Selects (On) system clock as 10 MHz, (Off) is 1 MHz.
2	Selects (On) system clock divide by 1, (Off) divide by 10.
3	Selects (On) external clock input, (Off) basic system clock - 1 MHz internal clock or 10 MHz with sw #1.
4	Master/Slave operation: (On) Slave operation, (Off) Master operation. Also selects Clock Out Mode.
5 to 8	Inhibit(5), Cycle Complete(6), Start(7), Stop(8), can be independently selected for opposite polarity (function as high going, SW ON or a low going signal, SW OFF).
9	Recycle Operation: (On) disabled, (Off) enabled.
10	LAM generation: (On) LAM at end of active cycle, (Off) at beginning of active cycle.
	PCB jumper X21-X22 disables inhibit functions.

TYPICAL OPERATION The module is initially reset assuring that the active state is disabled. This reset by either Z·S2 of F(9)·A(0) will also clear the memory address to zero. Otherwise a write memory address F(16)·A(2) of 0 data may be used. The memories can now be loaded. The following is a illustration of a load sequence:

STEP #	COMMAND	DATA VALUE	STEP #	COMMAND	DATA VALUE
1	F(16)·A(0)	Data=5, Word 1	6	F(16)·A(1)	Data=0 (Word 1 occurs at start time)
2	F(16)·A(0)	Data=7, Word 2	7	F(16)·A(1)	Data=1 (Word 2 occurs at 1 usec)
3	F(16)·A(0)	Data=2, Word 3	8	F(16)·A(1)	Data=5 (Word 3 occurs at 5 usec)
4	F(16)·A(0)	Data=0, Word 4	9	F(16)·A(1)	Data 16,777,215 (Word 4 indicates sequence is to be terminated).
5	F(9)·A(0)	(Clear address to zero)	10	F(9)·A(0)	(Clear address to zero)

After the load sequence, the memory can be readback if desired but a clear memory address must be the last command to assure address 0. Also a F(18)A(1) with data = 4 sets Output #3 for the Gated Clock Option.

An output cycle is executed by F(26)·A(1) to enable Output Word then either F(25)·A(0) for dataway start or F(26)·A(2) and External Start. The following output will occur:

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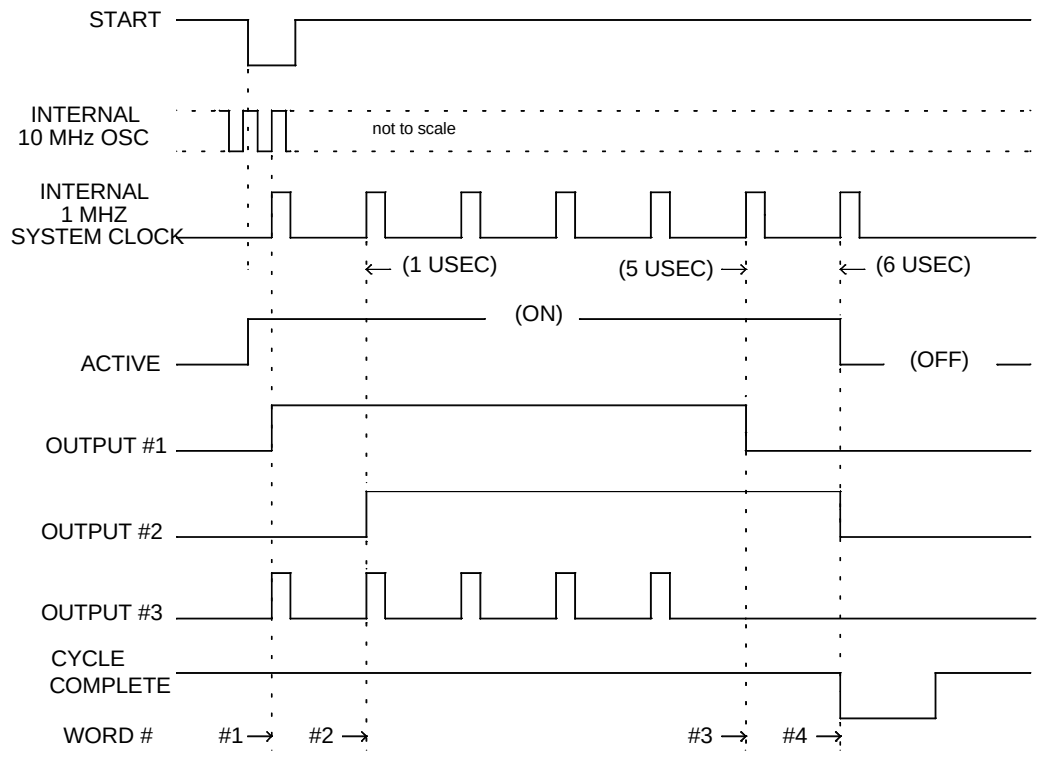

To repeat the sequence may require an enable output F(26)·A(1) and an appropriate start.

MODEL 221 CAMAC COMMANDS

*F(0)·A(0)	Read Output Word Memory on Rl thru R16 (R1-LSB) and increment address.
*F(0)·A(1)	Read Set Point Memory on R1 thru R24 (R1-LSB) and increment address.
*F(0)·A(2)	Read Memory Address on R1(LSB) -R16
F(1)·A(0)	Read Status Register, R1 (Bit 1) thru R16 Bit 1 0= Output Disabled, 1= Enabled Bit 2 0= Output Inhibited, 1= no Inhibit Bit 3 0= Ext. Start Disabled 1= Enabled Bit 4 0= Cycle Cleared 1= Cycle Active Bit 5 0= No Cycle Hold 1= Cycle Active but on Hold Bit 6 0= Clock Divide by 1 (1usec) 1= Divide by 10 (10usec) Bit 7 0= Clock Internal 1= External Bit 8 1= Select 10MHz clock 0= normal Bit 9 Master/Slave, 1= Slave Selected Bit 10 Inhibit Input, Polarity , 0= +, 1= - Bit 11 Cycle Comp Out, 0= +, 1= - Bit 12 Ext Start Input, 0= +, 1= - Bit 13 External Stop Input, 0= +, 1= - Bit 14 0= Recycle Disabled, 1= Enabled Bit 15 LAM, 1 = @ Start, 0 = @ Stop Bit 16 Reserved, set = 0
*F(1)·A(1)	Read Gated Clock Option Register on R1 thru R16 (R1-LSB). “1” = Clk Enabled.
*F(1)·A(2)	Read Polarity Option Register on R1 thru R16 (R1-LSB). “1”= Output Logic 1 Low
#*F(1)·A(3)	Read DAC Status Register if Option installed. See separate Option data sheet
F(1)·A(6)	Read module id #. Produces a read word equivalent to decimal 221.
F(8)·A(0)	Test LAM, Q=1 if LAM is set & enabled
F(9)·A(0)	Reset: Clears Memory Address and Output Register. Disables Sequence Cycle Active, Cycle Hold. Inhibits Module Outputs and disables External Start if RECYCLE not selected.
*F(9)·A(1)	Resets all Option Registers
F(10)·A(0)	Clear LAM
F(11)·A(0)	Selects Hold State if cycle is active.
*F(16)·A(0)	Write Output Word Memory on W1 thru W16 (W1-LSB) and increment address.
*F(16)·A(1)	Write Set Point Memory on W1 thru W24 (W1-LSB) and increment address.
*F(16)·A(2)	Write Memory Address Register on W1 thru W16 (W1-LSB).
*F(18)·A(0)	Write directly to Output Register on W1 thru W16 (W1-LSB).
*F(18)·A(1)	Write Gated Clock Option Register on W1 thru W16 (W1-LSB). “1” = Clk Enabled.
*F(18)·A(2)	Write Polarity Option Register on W1 thru W16 (W1-LSB). “1”= Output Logic 1 Low.
#*F(18)·A(3)	Write DAC Status Register if Option installed. See separate Option data sheet.
#*F(18)·A(4)	Write DAC Register direct if Option installed. See separate Option data sheet.
F(24)·A(0)	Disable LAM.
F(24)·A(1)	Disable Module Output Word.
F(24)·A(2)	Disable External Start.
F(25)·A(0)	Dataway Start Commands-Sets Sequencer to active state.
F(26)·A(0)	Enable LAM
F(26)·A(1)	Enable Module Output Word
F(26)·A(2)	Enable External Start
Z·S2	Resets Module; Same as F(9)A(0)
X	X is generated for all above F & A commands.
Q	A conditional Q is generated for F(8)A(0). Q is generated for all other F & A commands except for those identified by * which will may result in a Q=0 signifying execution has not taken place because a timing cycle is active and in process.
#	Note: Commands dentified by # exist only when the Analog Option is installed.